PCI-946-1 & P3S440BX

PENTIUM III® SBC

Technical Reference Manual

Version 1.4, June 2002

Note: The latest releases of the Technical Reference Manuals are available at:

ftp://ftp.kontron.ca/Support/Product_Manuals/

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Ref. : M946R1_TECH

Historical

Rel.	Date	Comments
1.0	Aug-1999	Initial document release.
1.1	Nov-1999	N/A
1.2	Sep-2000	N/A
1.3	Mar-2002	- Replace all Teknor occurrences by Kontron. - Update to Kontron Logo.
1.4	Apr-23-2002	- Remove “Documentation Survey” manual revision identification. - Add link to the FTP site on initial page. - In section 1.1 replace " The PCI-948 SBC and P3S440BX..." by " The PCI-946-1 SBC and P3S440BX..." - Changed the cover page for the new Kontron template. - Appendix, section D, page D-8, J20 and J21, changed the PS/2 connector illustration (pin 1 and 2 were inverted)

FOREWORD

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Printed in Canada.

PCI-946-1 and P3S440BX
Technical Reference Manual

Your comments are valuable for us and will contribute to improve the quality of this product by complementing and returning this form.

1. Overall rating of the Technical Reference Manual: ❑ Excellent ❑ Satisfactory ❑ Fair ❑ Poor
2. Was the information you were seeking easy to find? ❑ Yes ❑ No

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3. What section of this manual do you refer to the most? _____
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   In terms of complexity: ❑ Too technical ❑ Just OK ❑ Not technical enough

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616 Curé Boivin, Boisbriand
(Québec) CANADA J7G 2A7

Optional

Name _____
Company _____
Address _____
_____

FCC Compliance Statement

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

European Statement

Warning

This is a class B product. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Safety Standard

UL Recognized Component, File # E186339 vol. 1 section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**.

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

There is danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

IMPORTANT

This manual covers both PCI-946-1 and P3S440BX Single Board Computers where the difference resides in the usage of the Celeron® and Pentium® III® processor respectively.

POWERING-UP THE BOARD

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with the PCI-946-1 and P3S440BX installed in the system, a monitor and a mouse connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our technical Support department for assistance.

BIOS UPGRADE & AUTOMATIC CPLD HARDWARE UPGRADE

During the first system boot up after you update the Boot Block Flash BIOS with the UPGBIOS utility, the BIOS may need to upgrade the CPLD devices. **In such a case, do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperative if you disturb the CPLD hardware upgrade process!**

If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.

Rebooting in 5 second(s).
```

If the update is not successful, the following message appears under the "Status:" line:

```
ERROR: general failure programming CPLDs!

Please contact Kontron's technical support.
```

You must contact Kontron's technical support for further instructions.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

STATIC ELECTRICITY

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Kontron immediately.

When unpacking you will find:

1. One PCI-946-1 or P3S440BX Single Board Computer.
2. One Quick Reference sheet
3. One CDROM containing drivers.

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4. SOFTWARE SETUPS

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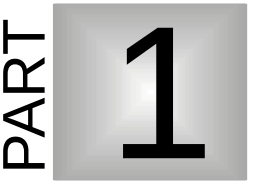

1 PRODUCT DESCRIPTION

1. **PRODUCT OVERVIEW**
2. **PRODUCT SPECIFICATIONS**

1.1 PRODUCT OVERVIEW

The PICMG compliant PCI-946-1 Single Board Computer (SBC) is built around an Intel Celeron processor running at a speed ranging from 300 to 433 MHz, in a PPGA package supported by an on die 128KB, 64-bit L2 Cache and a 66MHz Front Side Bus (FSB)

The PICMG compliant P3S440BX SBC is built around an Intel Pentium® III processor running at a speed ranging from 600 to 750 MHz, in a FC-PGA package supported by an on die 256KB, 64-bit L2 Cache and a 100MHz FSB.

The PCI-946-1 SBC and P3S440BX both offer the superior performance of the P6 microarchitecture meeting the unique low power consumption and smaller package requirements of the embedded application market.

1.2. PCI-946-1 AND P3S440BX PRODUCT SPECIFICATIONS

FEATURES	DESCRIPTIONS
Processor Option	**PCI-946 Rev. 1:** PICMG Single Board Computer supports Intel's PPGA Celeron Processor (370-pin PPGA 'Plastic Pin Grid Array') at 300, 366, and 433MHz. Supports Front Side Bus (FSB) speeds of 66 MHz **P3S440BX:** PICMG Single Board Computer supports Intel's FC-PGA Pentium® III Processor (370-pin FC-PGA form factor) at 600, 700, and 750MHz Supports Front Side Bus (FSB) speeds of 100MHz The Pentium® III uses a 370-pin FC-PGA form factor.
Chipset	The Intel 82440BX AGPset.
Internal Secondary Cache	16/16Kbytes Instruction/Data CPU-internal L1 cache. 4GB cacheable memory. **PCI-946 Rev. 1** : 128KB internal 64-bit wide SBP non-blocking ECC Level 2 running at full CPU core speed for the. **P3S440BX SBC** 256KB 64-bit wide Advanced Transfer Cache (on die, full speed L2 cache with ECC) for the
System Memory	Three 168-pin latching DIMM sockets, 64/72-bit. ECC support and parity supported with 72-bit modules. Up to 768 MB with 2, 4, 8, 16 or 32M x 64/72, 100MHz SDRAM (PC 100) non-ECC mode (single bit error correction, double bit detection via Intel 82440BX AGPset); all 768MB cacheable. Uses 3.3V, single-sided or double-sided 168-pin DIMMs.
Data Path	64-bit on CPU and memory bus 32-bit on the PCI bus 16-bit on the ISA bus

PCI-946-1 and P3S440BX Technical Specifications (cont'd)

FEATURES	DESCRIPTIONS
Bus Interfaces	Front Side Bus **PCI-946 :** 66MHz **P3S440BX :** 100MHz AGP Bus 66MHz PCI Bus 33MHz ISA Bus 8.33MHz Quick Switches to support up to 20-slot backplane.
Interrupts	11 edge sensitive and configurable 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility. All ISA onboard interrupts are PnP compliant.
DMA Channels (ISA)	Four 8-bit, three 16-bit Supports scatter / gather, Fast Type-F DMA
Flash Memory	2 Mb (256KB) Boot Block for BIOS field upgrade 4 KB Serial EEPROM for user configuration
CompactFlash™ Disk	Optional bootable CompactFlash™ module interfaces to secondary IDE channel, user upgradeable, master/slave.
PCI Ethernet Interface	Intel 82559 Fast Ethernet controller (Intel EthernetExpress Pro100+ equivalent) supports 10Base-T and 100Base-Tx Ethernet interface options via an RJ-45 connector on the board's I/O bracket. LED indicators are supported on the connector. Software drivers are supported for the most popular operating systems.

PCI-946-1 and P3S440BX Technical Specifications (cont'd)

FEATURES	DESCRIPTIONS
PCI SCSI Interface	SCSI controller Adaptec AIC-7880 (AHA-2940AU equivalent). Supports Wide-Ultra SCSI (16-bit, 40MB/s and data bursts to the host at full PCI speeds) via the 68-pin Wide-Ultra SCSI connector. Fast SCSI II 8-bit, 10MB/s) Fast-20 SCSI II (8-bit, 20MB/s) Accessory adapter cables available from Kontron. Active termination is provided onboard (enabled by jumpers). A SCSISelect Configuration Utility is available. Software drivers are supported for the most popular operating systems.
Serial Ports	Support two RS-232 serial ports, with RS-422/RS-485 available on Serial Port 2. 16C550 compatible with internal 16-byte FIFO buffers for more efficient data transfers. Configurable COM1-4 with BIOS selectable IRQs and adressing. The serial ports support VT100 mode for remote BIOS setup and console redirection.
Basic Interface Devices	Supports PS/2 mouse, AT standard keyboard, speaker, reset switch and hard disk LED.
Parallel Port	Supports multiple mode parallel port (Strandard, IEEE 1284, SPP, EPP, ECP) ; BIOS selectable IRQs and addressing.
Universal Serial Bus (USB)	Supports two USB ports. USB voltages protected by self-resetting fuse. Cable assembly, which provides two USB ports on a bracket, available for connection to USB 10-pin header. Cable/bracket assembly to be sold as a separate accessory.

PCI-946-1 and P3S440BX Technical Specifications (cont'd)

FEATURES	DESCRIPTIONS
Video Support	High performance 64-bit Frame AGP (Accelerated Graphic Port) video. 2MB SDRAM Video Memory 83MHz SDRAM memory (C&T 69000A). Supports CRT displays with resolution of up to 1024x768, 64K colors, non-interlaced or 1280x1024x256 colors, non-interlaced. Compatible with CGA, EGA, Hercules, MDA, VGA, SVGA, XGA and SXGA. Software drivers are available for the most popular operating systems.
Clock/Calendar	Real-time clock with 256 byte battery backup CMOS RAM
BIOS	Award Elite BIOS in Boot Block Flash with recovery code; save CMOS in Flash option and boot from LAN Capability. Auto configuration, extended setup. CC00-E000 address blocking; PnP tables. Setup console redirection to serial port (VT100 mode) with CMOS setup access. Software enable/disable of onboard Ethernet and SCSI. hardware enable/disable of onboard video. Diskless, keyboardless and videoless operation extensions. System, video, LAN and SCSI BIOS shadowing. Programmable bus and I/O speeds, and memory states. Advanced security feature for floppy and HDD. DMI & HDD S.M.A.R.T. support. Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), Advanced thermal management, resume overheat alarm, auto slow down, and Green support.

PCI-946-1 and P3S440BX Technical Specifications (cont'd)

FEATURES	DESCRIPTIONS
Supervisory	Two-stage software programmable watchdog timer drives NMI on 1st stage, system reset on 2nd stage. Time out from 16ms to 4.25min. CPU temperature monitor/alarm. Board temperature sensor. Power failure/low battery detector. Two end-user defined open-drain general purpose I/O; SMBus, I^2C Bus.
Serial ID Number Device	Serial ID Tag for unique board identification. The 48-bit serial number device contains the board's unique serial number. The number can be read by software. For instructions on accessing this device, contact Kontron's Technical Support.
4KB Serial EEPROM	The 4KB serial EEPROM device is non-volatile memory. This storage area is completely user-defined. For instructions on accessing this device, contact Kontron's Technical Support.
Watchdog Timer	A two-stage software programmable watchdog timer drives a NMI on 1st stage, and the system reset on 2nd stage.
Power Fail Detection	Monitoring either the real time clock and CMOS RAM power source (3.6V onboard or offboard battery), or an offboard battery of arbitrary voltage (a resistor must be installed to provide the appropriate voltage attenuation).
Thermal Management	Advanced thermal management with resume and overheat alarm for CPU including an audio alarm. Auto Slow Down CPU When Over Temperature.

PCI-946-1 and P3S440BX Technical Specifications (cont'd)

FEATURES	DESCRIPTIONS
Hardware Monitoring System	A system hardware circuit monitors all system voltages, ambient temperature and fan speed.
Battery	A built-in lithium battery is provided for data retention of CMOS memory.
Operating Systems	Supports all operating systems developed for x86 and Pentium® processors. PC and MS-DOS™, Windows® 3.X, Windows® 95/98, Windows® NT 4.0/5.0, OS/2® Warp; SCO UNIX™, QNX™. NOVELL™; UnixWare™.
Boot Block Flash BIOS	The 256KB Boot Block Flash device contains all the board's BIOSs and is used for storing the nonvolatile configuration required for Plug and Play. The protected boot block section allows for the reprogramming of the BIOS.
Power Supply	Voltage: VCore set by CPU VID; 3.3V ±5% ; +5V ±5% ; +12V ±5% PCI-946 Rev. 1: On-board switching regulators for 2.0V (Vcore), and 3.3 VDC (Vio). **Current Ratings (Celeron)** Frequency (MHz) 300 366 433 566 Current (Amps) 3.26 3.60 3.82 3.18 P3S440BX: On-board switching regulators for 1.6V (Vcore), and 3.3 VDC (Vio). **Current Ratings (Pentium III)** Frequency (MHz) 600 700 Current (Amps) 2.92 4.12
Mechanical	Board Dimensions: 338 x 122 x 36mm at CPU FAN (13.32" x 4.80" 1.4 in. at CPU / Fan) Conforms to IEEE P996 PC/AT bus, PCI Rev. 2.1 & PICMG Rev. 2.0 standards

PCI-946-1 and P3S440BX Technical Specifications (cont'd)

FEATURES	DESCRIPTIONS
Temperature	Operating Temperature 0 to 60ºC (32º to 140ºF) with airflow Humidity 5 to 95% @ 40ºC / 104ºF non-condensing Storage: Temperature -40 to +70ºC / -40º to 158ºF Humidity 0% to 95% R.H. @ 40ºC/104ºF non-condensing
Reliability	SCSI termination, USB and mouse / keyboard voltage protected by self-resetting fuses. Unique silicon serial number accessible via software. 2 year limited warranty. Designed to meet or exceed: Safety: UL 1950 ; CSA C22.2 No 950 ; EN 60950, IEC 950 EMI/EMC: FCC 47 CFR Part 15/CISPR22; CE Mark to EN55022/EN50082

PART 2

2. ONBOARD FEATURES

1. SYSTEM CORE
2. ETHERNET INTERFACES
3. I/O DEVICES
4. PARALLEL PORT
5. SERIAL PORTS
6. USB PORTS
7. STORAGE
8. VIDEO FEATURES
9. POWER SUPPLY INTERFACE

2.1. SYSTEM CORE

2.1.1. Processors

The following processors can be installed on the PCI-946-1:

PPGA Celeron Processors running at 300, 366, 433, MHz and future processors as technology evolves.

The Celeron Processor and its cooling fan assembly are factory installed and the speed of the processor is preset to its nominal value (maximum internal speed).

The following processors can be installed on the P3S440BX:

FC-PGA Pentium® III Processors running from 600 to 750 MHz and future processors as technology evolves.

The Pentium® III processor and its cooling fan assembly are factory installed and the speed of the processor is preset to its nominal value (maximum internal speed).

BIOS Setups

See Section 6-13: *AWARD Setup Program, CPU/Board Features Setup* option

The processor must be mounted to the board using the J22 socket. A fan connector referred to as J24 provides the power voltage for the CPU fan assembly.

NOTE

Celeron processors have fixed built-in multipliers and cannot be changed.

2.1.2. Memory

The board supports up to 768MB of 64/72-bit Synchronous DRAM (SDRAM) divided-up into three DIMM sockets (J13, J16 and J18). The minimum configuration is 16MB (one SDRAM module installed in socket J18).

Related Jumpers
None

BIOS Setups
See Section 4.1.6 – *AWARD Setup Program, Chipset Features Setup* option

The following SDRAM modules are supported:

- 16MB (2Mx64 or 2Mx72)
- 32MB (4Mx64 or 4Mx72)
- 64MB (8Mx64 or 8Mx72)
- 128MB (16Mx64 or 16Mx72)
- 256MB (32Mx64 or 32Mx72)

NOTE

The total size of the system memory available on the board is equal to the sum of the memory module sizes installed in the DIMM sockets.

2.1.3. Battery

The battery is required to keep the BIOS settings and the real-time clock stored into the CMOS RAM. The board is shipped from factory with the battery electrically disconnected from the board. Before powering the board, the battery must be connected using the W4 CMOS backup source jumper.

Related Jumpers

W4: Internal or external CMOS backup source selection
Setups are described in Section 2 – *Setting Jumpers*

BIOS Settings

None

The battery specifications are as follows: 3.6V Lithium battery, 0.37A/h

Installation

- Connect the battery to the B1 header. The positive pin of the battery is located at the bottom center.

- The onboard battery power can be replaced by an external power source by connecting a 3.6V power to the J14 External Battery connector. When using an off board battery source, W4 jumper must be set to position 2-3.

Warning

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

2.2. ETHERNET

The Ethernet interface is available through the J20 RJ-45 connector located on the edge bracket.

The 10Mbps or 100Mbps (10Base-T, 100Base-Tx) network speed is automatically detected and selected.

Related Jumpers
None

BIOS Settings
The onboard Ethernet feature is enabled by default.
To change settings, see Section 4.1.10: *AWARD CMOS Setup Utility, Integrated Peripherals Setup* option

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The 10Base-T interface uses UTP (Unshielded Twisted Pair) cables, category 5, 4 or 3 (5 is better) while the 100Base-TX interface requires category 5 UTP cables.

NOTE

To boot the board from LAN, the *Boot from LAN First* option must be *enabled* using the AWARD CMOS Setup Utility, BIOS Features Setup (see Section 4.2.2).

The Ethernet controller has specific drivers for various operating systems and software. To install these drivers, refer to the Utility Disk containing the Ethernet drivers for your operating system (see Section 8 - Installing Drivers).

2.3. I/O DEVICES

2.3.1. I/O Connections

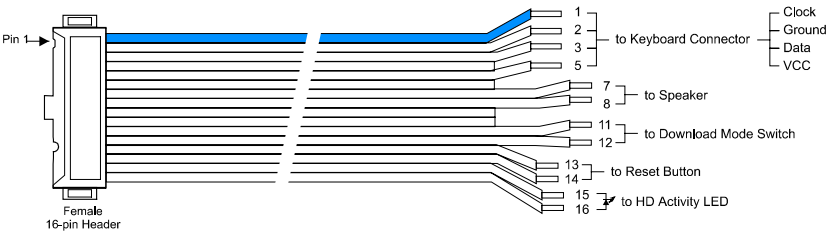
Standard AT keyboard, speaker port, reset button and hard disk LED signals are issued on the J11 multifunction header.

A 22" multifunction flat cable (Kontron part number 150-018-01) is provided with the board for connecting the respective devices.

Related Jumpers
None

BIOS Settings
None

Signals on the flat cable are issued as follows:



2.3.2. Keyboard

The simplest way to connect a PS/2 keyboard to the board is to use the J23 standard PS/2 keyboard connector (mini-DIN) on the edge bracket. No additional cabling is required. The onboard keyboard controller is 8042 software compatible.

Related Jumpers
None

BIOS Settings
To setup keyboard typematic features, refer to Section 4.1.5: *AWARD CMOS Setup Utility, BIOS Features Setup* option

2.3.3. PS/2 Mouse

The easiest way to connect a PS/2 mouse to the board is to use the J21 standard PS/2 mouse connector (mini-DIN) on the edge bracket. No additional cabling is required.

Related Jumpers
None

BIOS Settings
To enable automatically the PS/2 mouse when installed, refer to Section 4.1.10 *AWARD CMOS Setup Utility, Integrated Peripherals Setup* option

A PS/2 mouse header (J15) is also provided on board. To connect a mouse through this header, a shielded PS/2 mouse adapter cable is required. It is available from Kontron as 18" shielded mouse cable, part number 150-337-00.

⚠ CAUTION

While it is also possible to connect a mouse through the J15, PS/2 mouse header, do not connect two PS/2 mice simultaneously to the board. This can damage the mouse interface. The same also applies to possible connection of a keyboard through the multifunction header (J11), do not connect two keyboards simultaneously to the board. This can damage the keyboard interface.

2.4. PARALLEL PORT

The Parallel Port is available through the J12 26-pin connector. It is bi-directional and supports the Standard, EPP and ECP operating modes.

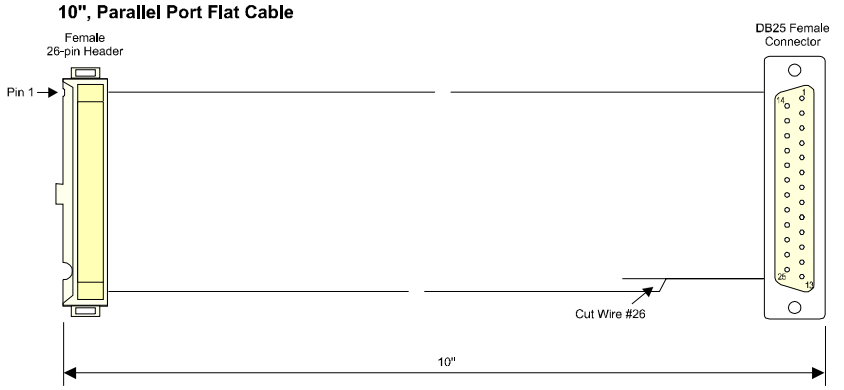
Related Jumpers

None

BIOS Settings

To setup the Parallel Port, refer to Section 4.1.10: *AWARD CMOS Setup Utility, Integrated Peripherals* option

The usual way to use the parallel port is to issue signals from the J12 26-pin connector to a standard 25-pin D-Sub connector using an adapter cable. Such a cable is available from Kontron (Part Number: 150-172). One cable is supplied with your board.



2.5. SERIAL PORTS

Two full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbaud.

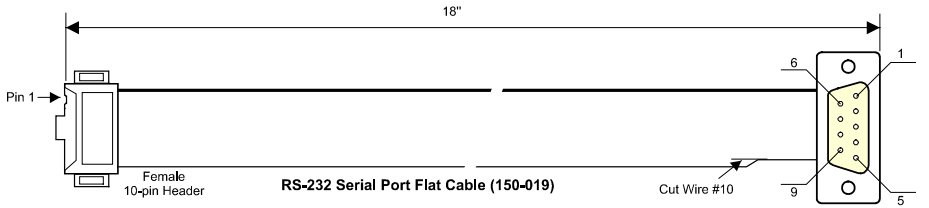
2.5.1. Serial Port 1

The Serial Port 1 is available through the J7, 10-pin connector and supports the RS-232 operation mode. It is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode

Related Jumpers
None

BIOS Settings
To setup the Serial Port 1, refer to Section 4.1.10 – *AWARD CMOS Setup Utility, Integrated Peripherals Setup* option

The usual way to use to the serial port is to issue its signals through a 10-pin header/9-pin D-Sub adapter cable. An 18 inches 10-pin header/9-pin D-Sub adapter cable is available from Kontron: Part number 150-019. Two cables are provided with your board.



While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron by contacting the Sales Department.

2.5.2. Serial Port 2

The Serial Port 2 is available through the J8 10-pin connector, and supports both RS-232, RS-422 and RS-485 operation modes.

Related Jumpers

W2 and W3: to connect/disconnect Serial Port 2 termination resistors
Setups are described in Section 3.2 – *Setting Jumpers*

BIOS Settings

To setup the Serial Port 2, refer to Section 4.1.10: *AWARD CMOS Setup Utility, Integrated Peripherals Setup* option

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The usual way to use the serial port is to issue signals through a 10-pin header/9-pin D-Sub adapter cable (see description provided for the Serial Port 1).

2.5.2.1. RS-232 Mode

By default, the Serial Port 2 is configured for RS-232 operation mode. To change the operating mode, refer to Section 4.1.10: *AWARD CMOS Setup Utility*, *Integrated Peripherals Setup* option.

2.5.2.2. RS-422/RS-485 Modes

Use the *AWARD CMOS Setup Utility*, *Integrated Peripherals Setup* option, to select the operation mode within RS-232, RS-422 or RS-485.

In RS-422 and RS-485 modes, transmitting and receiving use differential signals in either full-duplex (RS-422) or party line (RS-485) communication.

Communicating with differential signals requires one pair of wires for RS-485 and two pairs for RS-422 (one for transmission and one for reception).

For a better noise rejection, the use of twisted pair cable is highly recommended. This will enable faster serial transmissions over greater distances than with the common RS-232 cables.

If the board is installed at one end of the network and the Serial Port 2 is configured for communicating in RS-422 or RS-485 mode, use the W2 and W3 jumpers to connect the RS-485/RS-422 termination resistors (120 ohms) while the board is terminating the network.

2.5.2.3. RS-422 - Full Duplex Operation

The RS-422 protocol uses both RX and TX lines during a communication session. Upon power-up or reset, the Serial Port 2 interface circuits are automatically configured for full duplex operation. Pins 3 and 4 of J8 act as the receiver lines and pins 5 and 6 act as the transmitter lines.

In RS-422 mode, the software should not use the handshake signals (e.g., DSR, DTR), since they are not connected. However, software handshaking can be used (e.g., XON-XOFF).

2.5.2.4. RS-485 - Party Line Operation

The RS-485 offers to multiple station the ability to transmit and receive over the same pair of wires (RX outputs: pins 3 and 4 of J8), and share the same communication line with multiple stations.

The RS-485 protocol offers advantages such as increased speed over long distances, improved reliability over similar RS-232 setups, the ability to share transmission line, and simpler cabling requirements than the RS-422 protocol.

In this configuration, only one system takes control of the communication at a time.

Upon power-up or reset, the transceiver is by default in "receiver mode" to avoid line perturbation.

2.6. USB PORTS

The board provides a dual-USB interface through the J10 10-pin header. To connect standard USB devices, a USB cable/bracket assembly is required. It is available from Kontron: part number 150-316-00. One is provided with your board.

Related Jumpers

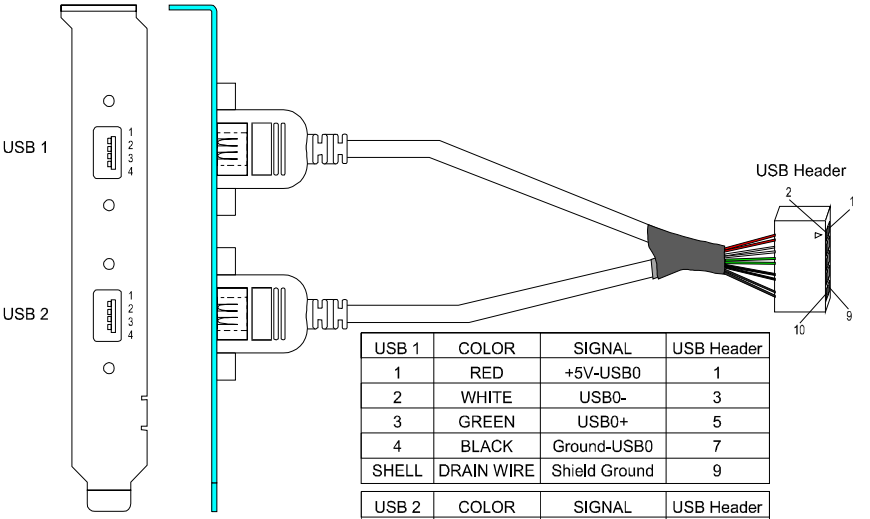
None

BIOS Settings

If required USB keyboard support for DOS and BIOS can be activated at the BIOS level.

Refer to Section 4.1.10: *AWARD CMOS Setup Utility, Integrated Peripherals Setup* option

The USB cable/bracket assembly is described as follows:



USB 1	COLOR	SIGNAL	USB Header
1	RED	+5V-USB0	1
2	WHITE	USB0-	3
3	GREEN	USB0+	5
4	BLACK	Ground-USB0	7
SHELL	DRAIN WIRE	Shield Ground	9

USB 2	COLOR	SIGNAL	USB Header
1	RED	+5V-USB1	2
2	WHITE	USB1-	4
3	GREEN	USB1+	6
4	BLACK	Ground-USB1	8
SHELL	DRAIN WIRE	Shield Ground	10

2.7. STORAGE DEVICES

2.7.1. Floppy Disk Drives

Two floppy disk drive units can be connected to the board through the J6 Floppy Disk connector using a standard IBM 34-pin flat ribbon cable. An 18" floppy disk cable is available from Kontron: part number 150-051. One cable is provided with your board.

Related Jumpers

None

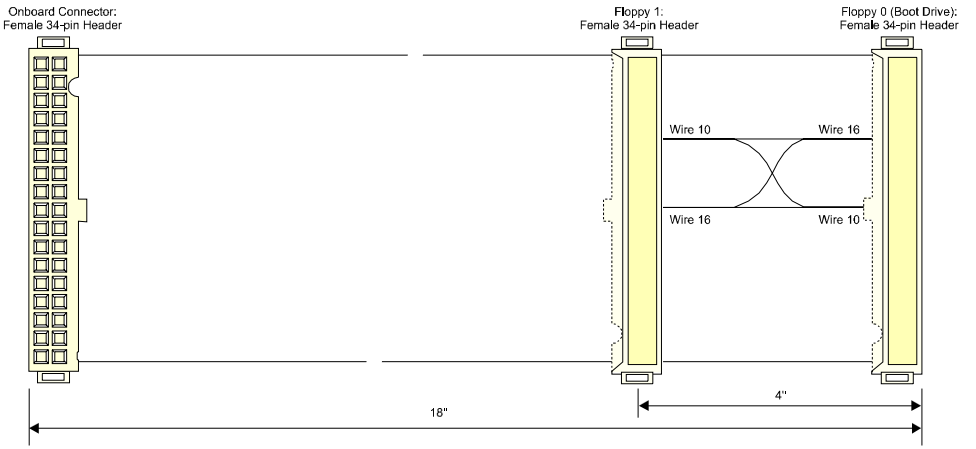
BIOS Settings

To define the Floppy Disk installation, refer to Section 4.1.4: *AWARD CMOS Setup Utility, Standard CMOS Setup* option

To enable/disable the system to boot from the floppy disk, refer to Section 4.1.5: *AWARD CMOS Setup Utility, BIOS Features Setup* option

---

The floppy disk cable is illustrated below:



2.7.2. IDE Devices

Two IDE interfaces are provided to support up to four IDE devices, such as hard disks, CD-ROM, and ZIP drives. The interfaces are referred to as Primary (J5 connector) and Secondary (J9 connector). Connections are supported through 40-pin dual row headers.

Related Jumpers

None

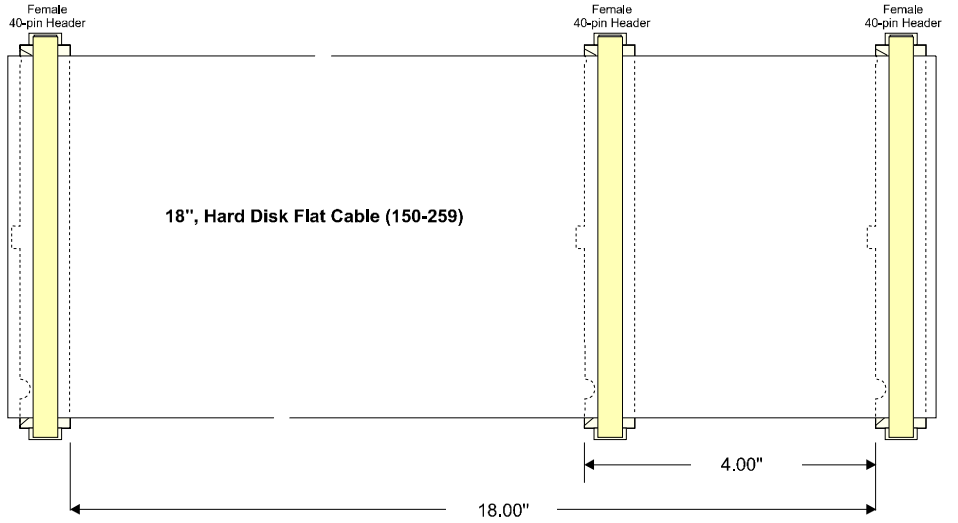
BIOS Settings

To detect a hard disk drive type, refer to Section 4.1.4: *AWARD CMOS Setup Utility, Standard CMOS Setup* option

To enable/disable the system to boot from the floppy disk, refer to Section 4.1.5: *AWARD CMOS Setup Utility, BIOS Feature Setup* option

To connect one IDE interface, use a 40-pin flat ribbon cable. An 18 inches length cable is available from Kontron: part number 150-259. One is provided with your board.

The cable is illustrated below:



2.7.3. SCSI Devices

The board supports PCI Ultra Fast/Wide SCSI 3 with operation up to 40 MB/s and data bursts to the host at full PCI speeds, Fast and Ultra SCSI 2 Adaptec AIC 7880.

The PCI Wide-Ultra SCSI 3 port is available at J4. A wide SCSI cable, 68-pin male to 68-pin male is supplied with the PCI-946 (part number 150-371-00).

You can access the PCI Fast and Ultra SCSI 2 through J3 using a 50 pin SCSI cable. This cable is supplied with the PCI-946 (part number 150-183).

Related Jumpers

W6 to determine the SCSI mode (8-bit or 16-bit)
W7 to set the board as terminated or not

BIOS Settings

Setup is described in Section 4.1.10 – *AWARD CMOS Setup Utility, Integrated Peripherals* option
The onboard SCSI interface is enabled by default.
To change setups, see Section 4.1.10 *AWARD CMOS Setup Utility, Integrated Peripherals* option

2.7.3.1. SCSI activity monitoring

The SCSI activity status signal is available through J2 (2-pin lock header). Connect the LED as follows: anode (red lead) on pin 1 and cathode (black lead) on pin 2. No external current limiting resistor is required since it is already present on the board (330 ohm resistor).

50-pin Fast SCSI and Fast-20 SCSI devices are also supported using a 68-pin to 50-pin adapter cable.

NOTE

Ensure that the onboard SCSI controller is enabled in the AWARD CMOS Setup Utility, Integrated Peripherals.

The Adaptec SCSISelect configuration software is provided with the board to configure or view the default SCSI settings of the host adapter (See Section 7 Configuring SCSI). It replaces the <Ctrl-A> feature on standard Adaptec controllers

The EZ-SCSI software is provided with the board to install the appropriate driver for your specific operating system.

Ensure that the onboard SCSI controller is enabled in the *AWARD CMOS Setup Utility*, *Integrated Peripherals.* To boot from the SCSI device, please refer to the *AWARD CMOS Setup Utility*, *BIOS Features* option.

NOTE

The Adaptec SCSISelect configuration software is provided with the board to configure or view the default SCSI settings of the host adapter (See Section 7 *Configuring SCSI*). It replaces the <Ctrl-A> feature on standard Adaptec controllers.

The EZ-SCSI software is provided with the board to install the appropriate driver according to your specific operating system.

2.7.4. Compact FlashDisk

The PCI-946 board also supports standard CompactFlash disks through a CompactFlash module. It is supported on the board as a standard IDE drive and connects to the Primary EIDE interface. The CompactFlash drive can be set as a Master or Slave device and combined with any standard hard disk drive.

Related Jumpers

W10 to set CompactFlash Disk as Master or Slave
Setup is described in Section 3.2 – *Setting Jumpers*

BIOS Settings

Since a CompactFlash Disk is the same as an IDE Hard Disk, refer to section 4.1.5 and 4.1.10 (*AWARD CMOS Setup Utility) to set options for this drive: master or slave, boot disk, etc.*

CompactFlash is installed on the C-FLASH connector. The board supports an IDE compatible flash disk by using a CompactFlash module (Kontron part number T069). CompactFlash (C-Flash) disks are the world's smallest resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power.

The CompactFlash disk connects directly on the Primary EIDE interface. It must be declared the same way as a standard hard disk using the *AWARD CMOS Setup Utility* (*IDE HDD Auto Detection* function).

To setup the CompactFlash disk for Master or Slave configuration, use the W10 jumper located on the SBC.

NOTE

Since data is accessed as an IDE drive, no specific flash disk driver is required for most operating systems.

2.8. VIDEO FEATURES

The CRT display connects directly to the J18 standard VGA 15-pin D-Sub connector located on the edge bracket.

Related Jumpers

W1 to enable or disable the onboard video controller
W9 to assign the PCI INTA to the onboard video controller
Setup is described in Section 3.2 – *Setting Jumpers*

BIOS Settings

Refer to Section 4.1.6: *AWARD CMOS Setup Utility, Chipset Features Setup* for RAM cache and video BIOS shadow capabilities

When the PCI INTA is assigned to the video controller (W9 shorted), the video controller will issue an interrupt request signal when the end of an active field (VSYNC pulse to the CRT monitor) is reached. By default the interrupt is disabled.

2.9. POWER SUPPLY

When used as a stand-alone system, the PCI-946 must be powered through the J1 Power connector. When installed on a backplane, the power is drawn to the board through the power lines of the ISA and PCI edge bracket.

Related Jumpers

None

BIOS Settings

See Power Management options described in Section 4.1.7: *AWARD CMOS Setup Utility, Power Management Setup* option

The power requirements are specified as follows:

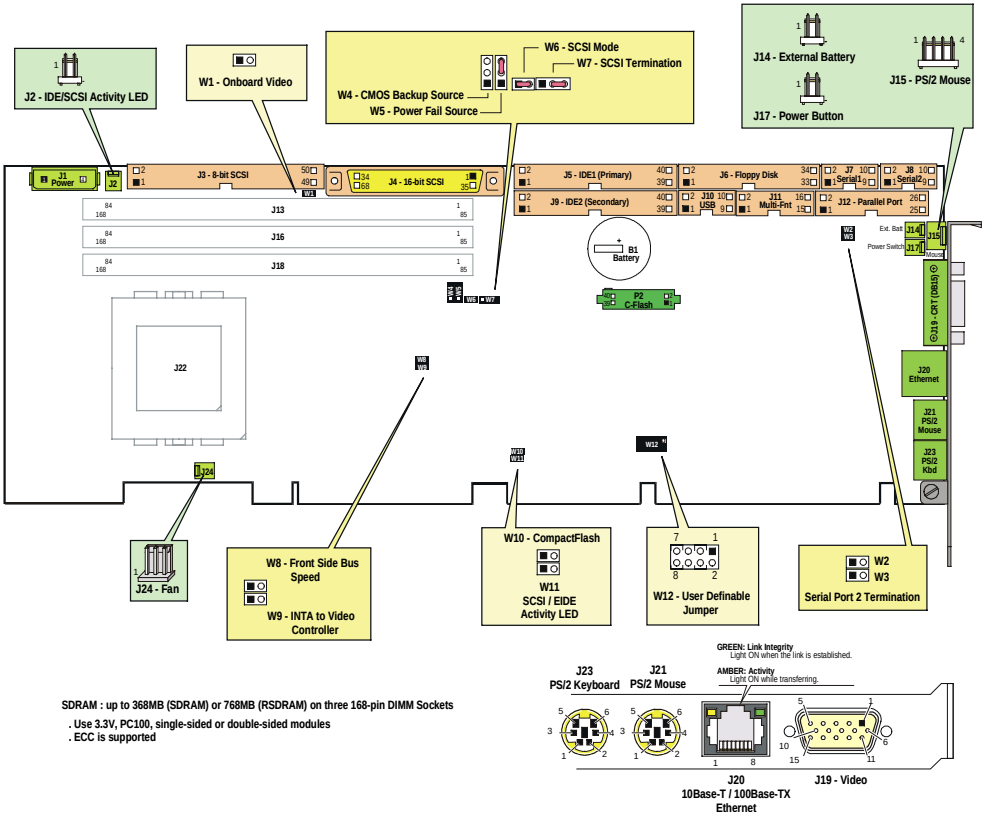
Part	Voltage Core (V)	Frequency INT/BUS (MHz)	Vcc Power MAX (Watts)	Vcc Power TYP (Watts)	Vcc Suspended Mode (Watts)	+12V (Watts)	Ambient Maximum Temp. ºC
Celeron 300A MHz	2.0	300/66	21.35	16.3	7.4	2.1	65
Celeron 366 MHz	2.0	366/66	24.2	18.0	7.4	2.1	65
Celeron 433 MHz	2.0	433/66	26.2	19.1	7.5	2.1	65
Celeron 566 MHz	1.5	566/66	19.0	15.9	7.9	2.1	60
Pentium® III 600E MHz	1.65	600/100	23.4	18.6	8.3	2.1	60
Pentium® III 700 MHz	1.65	700/100	26.9	20.6	8.5	2.1	TBD

PART 3

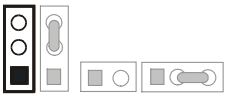
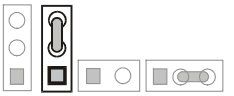
3 INSTALLING THE BOARD

1. CONNECTOR AND JUMPER LOCATIONS
2. SETTING JUMPERS
3. SUPERVISORY REGISTERS
4. ONBOARD INTERCONNECTIVITY
5. CUSTOMIZING THE BOARD
6. INSTALLING DRIVERS

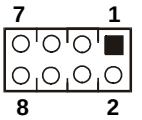
3.1. PCI-946 & P3S440BX CONNECTOR AND JUMPER LOCATIONS



3.2. SETTING JUMPERS

JUMPER	CONFIGURATION (Default Settings = *)
W1 	**W1- Onboard Video** Enabled * — off Disabled — on
W2 W3 	**W2, W3 - Serial Port 2 Termination** Set in RS-485 Mode only — W2 / W3 Termination Enabled — on / on Termination Disabled * — off / off
W4 	**W4 - CMOS Backup Source** Onboard Battery — 1 - 2 External Power (3.6V only) — 2 - 3 No Power (clear CMOS) * — off **There is a danger of explosion if the battery is incorrectly replaced. Replace only with thesame or equivalent type. Dispose of used batteries according to the manufacturer's instructions.**
W5 	**W5- Power Fail Source Selection** External Power (through J14) — 1 - 2 Onboard Battery * — 2 - 3 *To prevent the board from spurious PFI, the jumper cap must always be installed at either 1-2 or 2-3 position.*

Jumper Settings (cont'd)

<table>
<tr><th>JUMPER</th><th>CONFIGURATION (DEFAULT SETTING = *)</th></tr>
<tr><td> 
W6</td><td>
<table>
<tr><th colspan="2">W6 - SCSI Mode</th></tr>
<tr><td>16-bit : Wide Ultra SCSI II *</td><td>on</td></tr>
<tr><td>8-bit : Fast SCSI II and Fast-20 SCSI II</td><td>off</td></tr>
</table>
</td></tr>
<tr><td> 
W7</td><td>
<table>
<tr><th colspan="2">W7 - SCSI Termination</th></tr>
<tr><td>Controlled by Software</td><td>1-2</td></tr>
<tr><td>Board is hardware terminated *</td><td>2-3</td></tr>
<tr><td>No Termination</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W8  </td><td>
<table>
<tr><th colspan="2">W8 - Front Side Bus Speed</th></tr>
<tr><td>66MHz</td><td>on</td></tr>
<tr><td>66MHz / 100MHz *</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W9  </td><td>
<table>
<tr><th colspan="2">W9 - INTA Assigned to Video Controller</th></tr>
<tr><td>Enabled</td><td>on</td></tr>
<tr><td>Disabled</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W10  </td><td>
<table>
<tr><th colspan="2">W10 - CompactFlash</th></tr>
<tr><td>Master</td><td>on</td></tr>
<tr><td>Slave *</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W11  </td><td>
<table>
<tr><th colspan="2">W11 - SCSI / EIDE Activity Led</th></tr>
<tr><td>Combined</td><td>on</td></tr>
<tr><td>Eide only *</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W12  </td><td>
<table>
<tr><th colspan="3">W12 - User Definable Jumpers</th></tr>
<tr><td></td><td>on</td><td>off</td></tr>
<tr><td>1-2</td><td>User Defined</td><td>User Defined</td></tr>
<tr><td>3-4</td><td>User Defined</td><td>User Defined</td></tr>
<tr><td>5-6</td><td>VT-100 Mode</td><td>Normal Mode</td></tr>
<tr><td>7-8</td><td>Reserved</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

3.3. SUPERVISOR REGISTERS

The PCI-946-1 and P3S440BX provide a set of programmable I/O registers to setup the Intel PIIX4 (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-19Fh, 290h-29Fh or 390h-39Fh using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

The Supervisor Registers consist of six I/O registers which are used to configure and control the special features of the board, such as the Analog Watchdog, the Programmable Watchdog and the Power Fail Detection.

These registers are 8-bit wide and can be located at three different I/O base addresses: 190h, 290h or 390h.

When setting Register x90h at one base address, all the other registers are located at the same base address plus one, two, three and so on. To select the base address, use the *AWARD CMOS Setup Utility Chipset Features Setup* (see Section 4.1.6).

This section includes a description of each I/O register and bit available for programming and configuring the PCI-946-1 and P3S440BX.

3.3.1. Register x90h: Serial port

Bit	7	6	5	4	3	2	1	0
Reset				0	0	0		
Read				RS485	RS232	ST1		
Write				RS485	RS232	ST1		

Used by the BIOS during the POST only.

Serial port 2 configuration/use

ST1 Enable RTS2 to be used as 485TX enable when in 485 mode (1: enable, 0: disable).

RS232 Enable RS-232 mode for serial port 2 (1: enable, 0: disable).

RS485 Enable RS-422/RS-485 mode for serial port 2 (1: enable, 0: disable).

> **NOTE**
>
> The RS232 and RS485 bits are initialized by the BIOS during POST (Power-On Self Test). If a modification of these bits is required, be aware that there is a hardware protection so that RS232 and RS485 buffers cannot be activated at the same time. This protection is provided at the register level. If you write to x90h register with bits 3 and 4 set, you will actually write 0 in both of these bits. This condition can be read back.

3.3.2. Register X91h: Reset History & CPU Fault

Bit	7	6	5	4	3	2	1	0
Reset								
Read	PBRES		WDO					
Write								

Used by the BIOS at runtime; do not write to this register.

Reset history

PBRES This bit is set when the reset button is pressed. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

WDO This bit is set when a reset is produced by the watchdog. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

* = Active low signal

3.3.3. Register x92h: Clearing Reset History & Lock for Watchdog

Bit	7	6	5	4	3	2	1	0
Reset						1		1
Read						LOCK		CLRHIS*
Write						LOCK		CLRHIS*

Not used by the BIOS.

Reset history

CLRHIS* A 0-1 pulse will clear all reset history bits (refer to the x91h register described previously). In normal operation, always keep the CLRHIS* bit to "1" otherwise the reset source will not be captured (the history latch are disabled when CLRHIS* is "0").

Programmable watchdog

LOCK When set, the state of the enable bit for the programmable watchdog (WDEN) cannot be changed.

* = Active low signal

3.3.4. Register x93h:

Silicon ID Chip Interface, Local I^2C, System Monitor Connector Interface

Bit	7	6	5	4	3	2	1	0
Reset				X	1		1	1
Read				X	IDCHIP (pin)		SCL (pin)	SDA (pin)
Write				RESERVED	IDCHIP (reg.)		SCL (reg.)	SDA (reg.)

Not used by the BIOS.

Silicon ID chip

IDCHIP Used to read the onboard silicon serial number using the Dallas Semiconductor one-wire protocol.

User EEPROM

SCL/SDA Clock and data I^2C link to user EEPROM.

3.3.5. Register x94h & x95h

These registers are reserved.

3.3.6. Register x96h: Programmable Watchdog

Bit	7	6	5	4	3	2	1	0
Reset	0	1	1	1				
Read	WDEN	WDS2	WDS1	WDS0				
Write	WDEN	WDS2	WDS1	WDS0				

Not used by the BIOS.

WDEN When this bit is set, the programmable watchdog is enabled with the current timeout specified by WDS[2..0] (refer to the dual-stage programmable watchdog description in Section 5-1).
To avoid accidental deactivation of the watchdog, the bit WDEN is normally locked by the bit LOCK of register x92h (see register x92h description).

WDS[2..0] Timeout selection.

3.3.7. Register x97h: NMI sources & mask

Bit	7	6	5	4	3	2	1	0
Reset	0				0		0	
Read	BatFltEn	BatFlt		FanFlt	FanFlt En		WdNmiEn	WdNmi
Write	BatFltEn				FanFlt En		WdNmiEn	

Not used by the BIOS, except when the Whatchdog option is enabled and after POST.

WdNmi	Watchdog NMI: NMI from the Watchdog timeout.
WdNmiEn	Enable NMI from the Watchdog.
BatFlt	Battery Fault: NMI from power failure detection.
BatFltEn	Enable NMI from BatFlt.
FanFlt	Fan Fault: NMI from CPU fan failure detection
FanFltEn	Enable NMI from FanFlt

All bits are active "1" regardless of the electrical state of the signal. Inversion is provided by the hardware when required. When an NMI source is enabled, the corresponding event is latched until the enable bit is cleared. When the enable bit is cleared, the status bit reflects the signal (not latched).

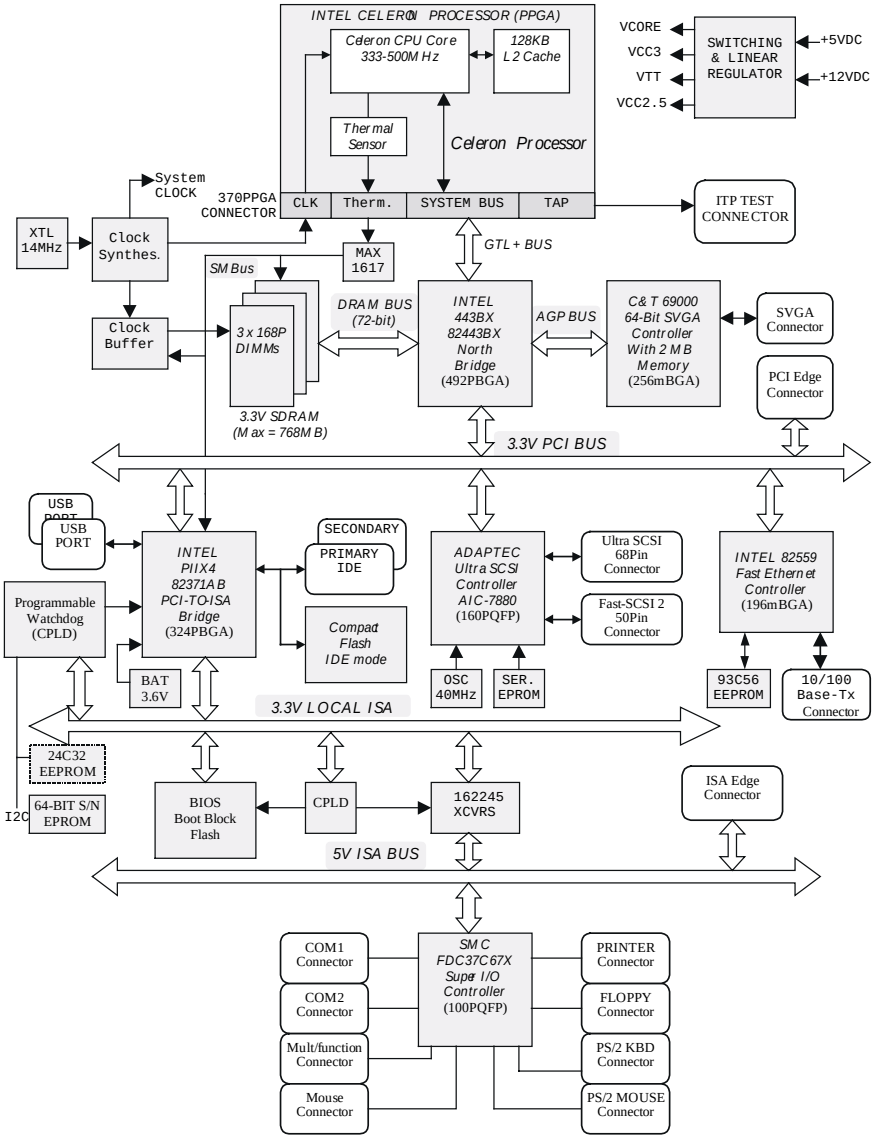
The NMI itself is generated through the IOCHK* signal. As a result, it can be monitored on the ISA backplane, and the NMI handler must reset the IOCHK* latch.

> **NOTE**
>
> When a watchdog NMI occurs, the CPU must trigger or disable the watchdog within 1ms or the watchdog will generate a master reset. Knowing that an NMI is the highest priority interrupt on the CPU, if the CPU cannot answer the NMI within 1ms then there is a major problem and the best thing to do is to reset everything. Normally, the CPU will answer the NMI and re-trigger the watchdog for the time it needs to shut down properly.

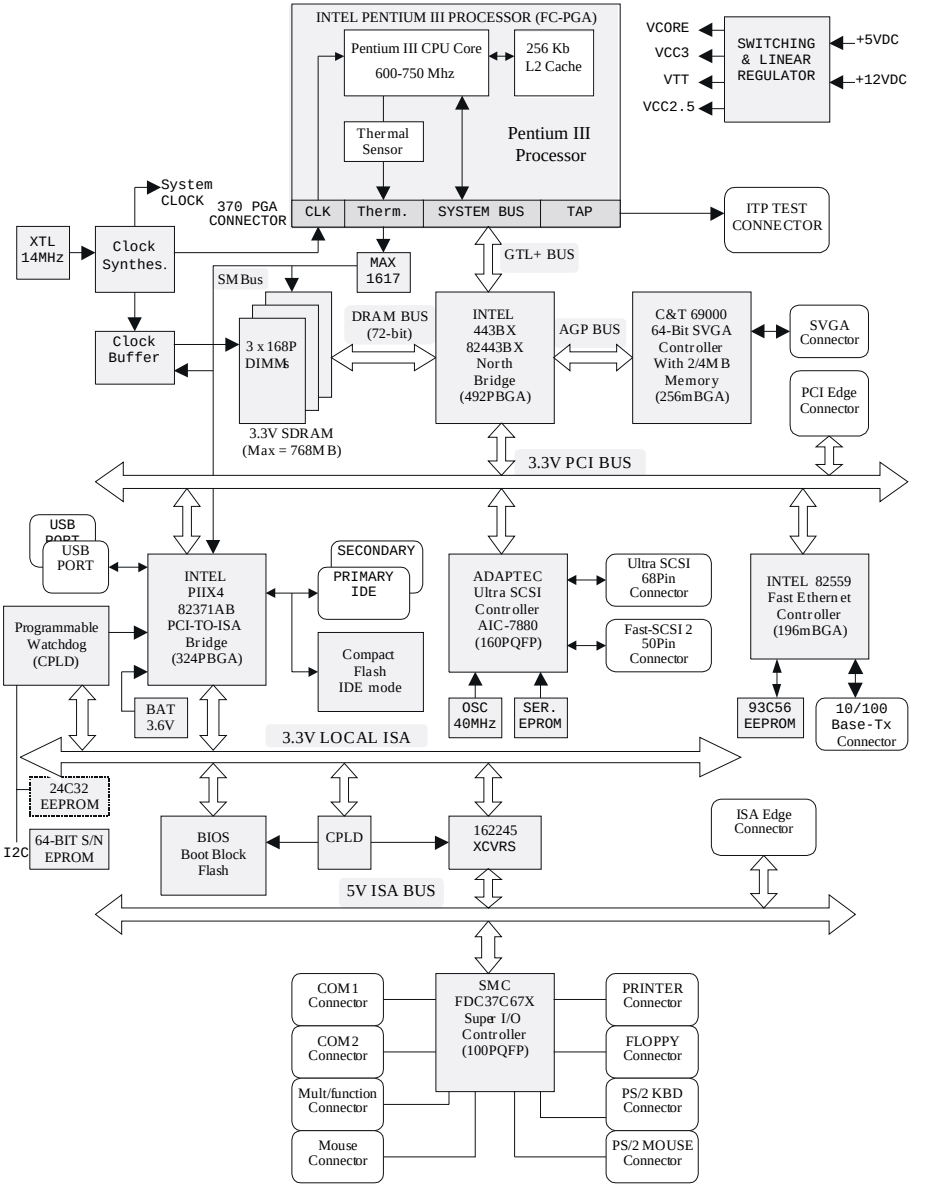
* = Active low signal

3.4. ONBOARD INTERCONNECTIVITY

3.4.1. PCI-946-1 Block Diagram



3.4.2. P3S440BX Block Diagram



3.4.3. Single Board Computer Main Features

The PCI-946-1 and P3S440BX are powerful computing engines. In addition to the CPU core, it is supplemented by an extensive set of interfaces using five key components:

- An Intel 443BX Chipset interfaces with the processor (host), system memory, video controller, and Primary PCI bus (3.3V / 33MHz).
- An 69000 Accelerator with integrated memory
- An Adaptec Ultra SCSI Controller
- PCI-to-ISA bridge - 82371AB PIIX4 from Intel: interface the ISA bus to the Primary PCI bus.
- A 37C67X Super I/O Controller

3.4.4. Celeron and Pentium® III processors

The PCI-946-1 SBC support the Intel's Celeron 300AMHz, 366MHz, 433MHz and 566MHz. The P3S440BX support the Intel's low power Pentium® III processor running at 600MHz 700MHz (higher clock speeds will be available when Intel releases the corresponding parts).

The PCI-946-1 SBC consists of a Celeron processor core with an integrated second level cache of 128KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance 66MHz front side bus.

The P3S440BX SBC consists of a Pentium® III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance 66/100MHz front side bus.

The processor interfaces to the 440BX AGPset through the 64-bit low power GTL + data bus interface.

3.4.5. North Bridge Chipset

This chipset consist of 443BX AGPset, 64/72-bit SDRAM data interface with ECC support, Low Power GTL Bus, five PCI arbitration channels, PCI bus rev. 2.1, Accelerated Graphics Port Interface (AGP). The bus is optimized for 100MHz operation.

3.4.6. 21554 PCI-to-PCI Bridge

The 21554 is a PCI peripheral chip that performs PCI bridging functions for embedded and intelligent I/O applications. The 21554 is a "non-transparent" PCI-to-PCI bridge that acts as a gateway to an intelligent subsystem. It allows a local processor to independently configure and control the local subsystem. The 21554 implements an I_2O message unit that enables any local processor to function as an intelligent I/O processor (IOP) in an I_2O-capable system.

Unlike a transparent PCI-to-PCI bridge, the 21554 is specifically designed to bridge between two processor domains. The processor domain on the primary interface of the 21554 is also referred to as the host processor. The secondary bus interfaces to the local domain and the local processor. Special features include support of independent primary and secondary PCI clocks, independent primary and secondary address spaces, and address translation between primary (host) and secondary (local) domains.

The 21554 supports a 64-bit primary PCI bus, a 64-bit secondary PCI bus, and a maximum operation frequency of 33MHz.

3.4.7. 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4)

The PCI-to-ISA bridge is configured to support signals to directly drive IDE interfaces, USB ports, and standard Serial Ports (1 and 2), floppy disk drives, mouse and keyboard through a super I/O controller (FDC37C672).

3.5. CUSTOMIZING THE BOARD

3.5.1. Processor

The PCI-946-1 SBC is shipped with the PPGA Celeron Processors running at 300, 366 or 433, MHz and future processors as technology evolves. It is equipped with a passive heat sink that provides adequate cooling in a 150LFM airflow environment.

The P3S440BX SBC is shipped with the FC-PGA Pentium® III Processors running from 600 to 700 MHz and future processors as technology evolves. It is equipped with a passive heat sink that provides adequate cooling in a 150LFM airflow environment

CAUTION

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU

Before installing a processor on your board, **you must contact our technical support** for the installation procedure

3.5.2. Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).

When replacing, the battery must be connected as follows:

WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

3.5.3. Installing the Memory

3.5.3.1. SDRAM System Memory

The PCI-946-1 and P3S440BX support three industry standard 168-pin DIMMs (Dual In-Line Memory Module) sockets for memory configuration from 32MB to 768MB of Synchronous DRAM.

The memory characteristics must conform to the following:

- 1.15 inch height, 168-pin DIMM
- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided
- Unbuffered 100MHz (SDRAM),
- Serial Presence Detect (SPD) EEPROM,
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Only the P3S440BX SBC is compliant with Intel's PC SDRAM Unbuffered DIMM Specification (100MHz) Rev. 1.0. The PCI-946-1 FSB runs at 66MHz.

At least 32MB of memory must be installed on the board for proper operation. Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the three DIMM sockets.

NOTE

When populating with more than one memory module, each socket must be installed with the same memory type (64/72-bit), however the capacity of each module may be different from the other.

The recommended DIMM devices are listed in the table below.

Vendor's part number	DIMM's description	Vendor's Name
CTK32M/P100S	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	CENTON
4X72CQ2X8S4E	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	ROCKY MOUNTAIN RAM
DIM-200472V2S08G1	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	SHIKATRONICS
DIM200472V5S08G	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	SHIKATRONICS
CTK64M/P100S	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	CENTON
8X72PC8X8S4E	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	ROCKY MOUNTAIN RAM
DIM200872V4S8G1	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	SHIKATRONICS
CTK128M/P100S	ECC SDRAM 128MB 16M*72 PC100 1.15"	CENTON
DIM-201672V4S08G1	ECC SDRAM 128MB 16M*72 PC100 1.15"	SHIKATRONICS
VM374S1723-GL	ECC SDRAM 128MB 16M*72 PC100 1.15"	VIRTIUM
CFHKQARV4VU420G	ECC SDRAM 256MB 32M*72 PC100 1.15"	CENTON
CTK256M/P100S	ECC SDRAM 256MB 32M*72 PC100 1.15"	CENTON
DIM203272VDS08GS	ECC SDRAM 256MB 32M*72 PC100 1.15"	SHIKATRONICS
VM374S3323-GL	ECC SDRAM 256MB 32M*72 PC100 1.15"	VIRTIUM

3.5.3.2. DIMM Installation

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the faceplate is facing you.
2. Hold the module vertically so that the bottom connector key is at right. Install the DIMM straight down into the DIMM socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

3.5.4. Power Fail Monitoring

The power failure detector status can be readout from one bit of the system register located at the address 0 x 191h Bit 0. The detection conforms to the following conditions (* = active low signal):

It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.
It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). An interrupt handler can then service the interrupt. If you choose not to generate an NMI, you can use an algorithm to detect a low battery condition and respond accordingly.

For more information, contact the Technical Support department

3.5.5. Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The PCI-946-1 and P3S440BX provide a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

Dual Stage Watchdog

Enabling the Programmable Watchdog

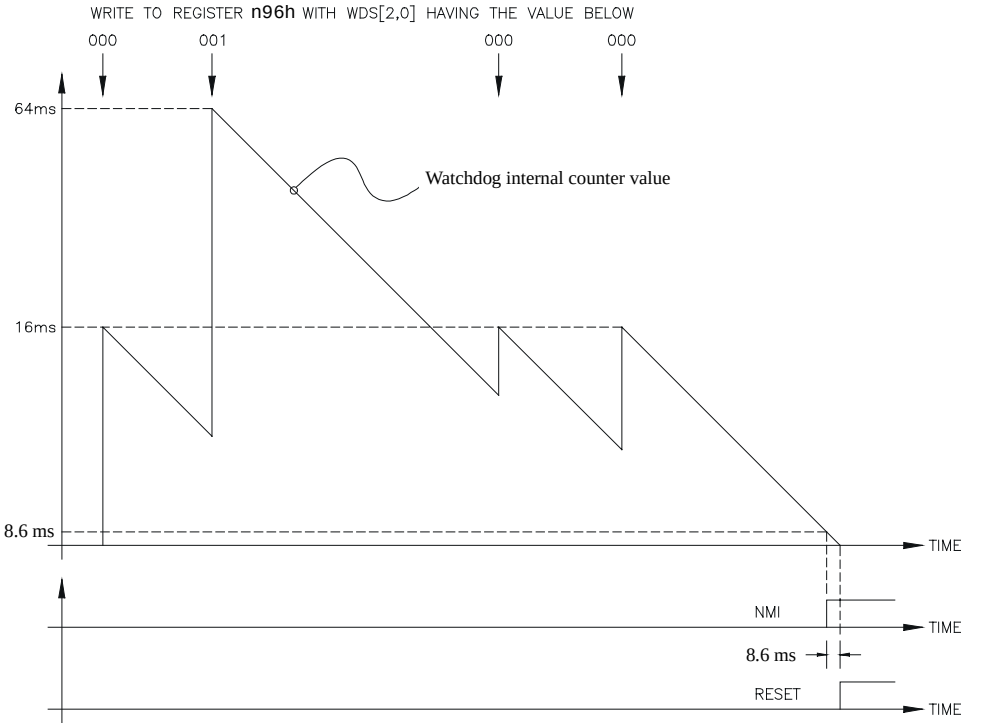
To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register n92h (bit 2), then set the bit WDEN (bit 7) in register n96h and relock it by setting the lock bit in register n92 (bit 2). The following is an example in C language:

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void ArmWatchdog(void)
{
    outp(TekReg+2,  inp(TekReg+2) & 0xFB);      // unlock watchdog enable bit
    outp(TekReg+6,  inp(TekReg+6) | 0xF0);      // enable and trigger at max time-out
    outp(TekReg+2,  inp(TekReg+2) | 0x04);      // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n96h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n96h description). For a fixed time-out, the software simply writes a constant in register n96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register n96h (n = 1, 2 or 3). The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)     // select timeout at runtime: 0x80 = 0.016s,
                               // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates an NMI interrupt (if enabled in register n96h, bit 7). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n96h description for a suggestion on how to do this.
The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

A reset from the programmable watchdog is latched for reset source identification; see reset history description in Section 4.3.

3.5.6. Thermal Management

The thermal management is built around two digital temperature sensors and a thermal watchdog. Both devices can be programmed to set their outputs when the temperature of the processor or the ambient temperature exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

Please refer to Section 4.1.10 *CPU/Board Features Setup– Thermal Management Options* for a complete information on thermal management setups.

3.6. INSTALLING DRIVERS

3.6.1. SCSI Drivers

To install the appropriate driver for your specific operating system, use the EZ-SCSI software located on the CD-ROM (provided with your board).

3.6.2. Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

3.6.3. Ethernet Drivers

Various driver are provided for different operating systems and software. To install a driver, refer to the Setup program and the ReadMe.bat file located on the CD-ROM (provided with your board).

3.6.4. Chipset Driver for Windows 95

The Windows 95 driver for the Intel PIIX4 and 440BX chipset is provided on the the CD-ROM (provided with your board).

3.6.5. Other Drivers

For other operating system drivers and installation instructions or for more information, contact Kontron's Technical Support department.

PART 4

4. SOFTWARE SETUPS

2. BIOS SETUP PROGRAM

3. UPDATING OR RESTORING THE BIOS IN FLASH

4. VT100 MODE

4.2. AWARD BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the *Boot from LAN first* option to “Enabled” in the BIOS Setup’s *BIOS Features Setup*
2. Follow the complete procedure in the Boot from LAN utility CDROM.

4.2.2 ACCESSING THE BIOS SETUP PROGRAM

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the PCI-946-1 and P3S440BX peripheral processor. The PCI-946-1 AND P3S440BX uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

> ⚠ CAUTION
>
> Before modifying CMOS setup parameters, ensure that the W4 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- Hit the DELETE key when the message - "Press DEL to Enter SETUP" appears near the bottom of the screen.

The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

KONTRON T1005 BIOS VERSION 2.0 CMOS SETUP UTILITY AWARD SOFTWARE, INC. (2A69TU00)	
STANDARD CMOS SETUP	LOAD BIOS DEFAULTS
BIOS FEATURES SETUP	LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP	SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP	USER PASSWORD
PNP/PCI CONFIGURATION	IDE HDD AUTO DETECTION
CPU/BOARD FEATURES SETUP	SAVE & EXIT SETUP
INTEGRATED PERIPHERALS	EXIT WITHOUT SAVING
Esc : Quit F10 : Save & Exit Setup	↑ ↓ → ← : Select Item (Shift)F2 : Change Color
Time, Date, Hard Disk Type . . .	

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default settings consist of the **safest** set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP Default values provide **optimum performance** settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.2.1. Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory, etc.).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speed, thermal management and board monitoring options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are **fail safe** settings, which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the **optimal** settings that provide the optimum performance for all devices and system features. **If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.**
Supervisor/User Password Setting	Change, set or disable the password. It allows you to limit the access to the system and the Setup, or only to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE hard disk drives parameters and puts them in the Standard CMOS Setup page.
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

4.2.2. Setups

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To enter in a submenu, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item a the left.
→	Moves to the item at the right.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F1	Help Menu
F2 / <Shift>F2	At the main menu, change the color of the menu.
F5	When in the Main Menu: Restores the previous setup values for all the BIOS parameters (except Standard CMOS Setup) which were displayed when you entered the program. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Restores the previous setup values for that setup screen only.
F6	When in the Main Menu: Loads the BIOS Defaults of all the BIOS parameters (except Standard CMOS Setup). The BIOS Defaults are fail safe settings, which consists of the safest set of parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in the Main Menu: Loads the Setup Defaults for all the BIOS parameters (except Standard CMOS Setup). When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the Setup Defaults for the BIOS parameters for that setup screen only. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
F10	When in the Main Menu: Saves all the CMOS changes and exit.

4.2.3. Standard CMOS Setups

Function	Description
Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the PCI-946-1 and P3S440BX boards. The Primary and Secondary controllers can both have two disks: Master Disk or Slave Disk. Only three settings are available for the hard disk type: Auto, User and None. Type 1 to 46 are not predefined in the system: Use auto or enter the parameters for the type in the user-defined.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

4.2.4. BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En. / Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self-test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appears.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required running the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (BMP) picture will appear during the POST or you can have your logo being displayed. Contact the technical Support (see Appendix G).
Boot from LAN First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the "Boot from LAN" utility CDROM.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). **Note: The Boot from LAN First and Raid Card Boot First options take precedence over this option.**
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select NO on the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialization. 0 is disabled.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, Normal	If you have set a password, select whether the password is required every time the system boots (“System” option), or only when you enter Setup (“Setup” option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Boot Up NumLock Status	On	On	On, Off	Control the state of the NumLock key when the system boots. When set to “On”, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6-30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250-1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat when you hold down a key).
VT100 Settings				
Comport	1	1	1,2	Use this option to select which COM port will be used for VT100
Speed	Auto	Auto	Auto, 2400, 9600, 19200, 38400, 57600, 115200	Select the baud rate of COM port. used in VT100 mode.
Parity	None	None	None, Odd, Mark, Even, Space	Use this option to select the parity.
Data	8	8	7, 8	Use this option to specify the number of data bits being used.
Stop	1	1	1, 2	Use this option to specify the number of stop bits being used.

4.2.5. Chipset Features Setup

This part of the setup allows you to define chipset-specific options and features.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. **Note: processors provided by Kontron support ECC. However, not all Pentium®® II / III processors support ECC. Check Intel's website to know if your processor supports ECC:** http://developer.intel.com/support/ processors/Pentium®II/identify.htm.
SDRAM RAS-to-CAS Delay	3	3	2, 3	**Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options, if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.** This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activate command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles is allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done. This option will work in ECC mode only if all installed memory banks supports ECC (Error Checking and Correction)
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some off-board video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 8-bit and 16-bit I/O.
16 Bit I/O Recovery Time	2	1	1-4, NA	

Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Address	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type	AT	AT	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in megabytes of the AGP Aperture.
Video BIOS Shadow	En.	En.	En./Dis.	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (on board or off-board), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF	En.	En.	En./Dis.	
CC000-CFFFF	En.	En.	En./Dis.	
D0000-D3FFF	En.	En.	En./Dis.	
D4000-D7FFF	En.	En.	En./Dis.	
D8000-DBFFF	En.	En.	En./Dis.	
DC000-DFFFF	En.	En.	En./Dis.	

4.2.6. Power Management Setup

This part of the setup configures power conservation options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	En.	En./Dis.	The Advanced Configuration and Power Interface (ACPI) allows Operating System Direct Power Management (OSPM) and make advanced configuration architectures possible. When Enabled, the OS supports ACPI or OSPM (e.g., Win98, and Windows 2000 **Note: When Enabled, and the OS is ACPI compliant, the OS setting take precedence over all settings in this menu.**
Power Management	User Def.	User Def.	User Define, Min Saving, Max Saving	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS can control the PM by APM calls. If No, the BIOS will control the PM (Power Management)
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	Blank Screen V/H SYNC+Blank, DPMS,	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Standby	Standby	NA, Suspend, Standby, Doze,	As the system moves from lesser to greater power-saving modes, select the mode **in which you want the monitor to blank.**
Doze Mode	Dis.	Dis	Disable 1min to 1h	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	Dis.	Disable 1min to 1h	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the non-essential devices are shut off while all other devices still operate at full speed.
Suspend Mode	Dis.	Dis.	Disable 1min to 1h	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	Dis.	Disable 1-15min	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock **does not run.** When 12.5% is selected, the CPU is running at nearly Full Speed and if 75% is selected, the CPU will be idle 75% of time.
PCI / VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN	Instant-off	Instant-off	Instant-off, Delay 4 sec.	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.

Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a serial port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Reload Global Timer Events:				
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

4.2.7. PnP/PCI Configuration

This part of the setup configures PnP/PCI options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "**Yes**" if you want the OS to allocate resources according to Plug and Play standards, or "**No**" if you want the same resource allocations at every system boot-up. Select "**No**" when the OS is **not** Plug and Play (for example, DOS). **Note: When set to "Yes", only the boot devices will get Resources.**
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear as well as Used Mem Base Address and Lenght as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Used MEM length	16K	16K	16K, 32K, 48K, 64K	Select a base address for the memory area used by any peripheral that requires high memory. When this option is not set to N/A, the menu for used memory lengths available is displayed.

4.2.8. CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Current Processor(s) Speed	nnn	nnn	nnn	This option displays the current processor speed.
Front Side Bus Speed	nnn	nnn	nnn	This option displays the current Front Side Bus speed. This speed is selected by the CPU auto-detection logic.
Thermal Management Options:				
. Thermal Management	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
. Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
. CPU 1 Die Temperature	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	50	50	10-70	The CPU will be slowed down when it reaches the selected Overheat Alarm (°C) temperature. Full speed will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	70	70	30-90	The CPU will be slowed down when it reaches the selected Overheat Alarm (°C) temperature. Full speed will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm
. CPU1 Local Temperature	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down when it reaches the selected Overheat Alarm (°C) temperature. Full speed will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	50	50	30-90	
Save CMOS in Flash	Dis.	Dis.	En./Dis.	Saving CMOS memory content into Flash Memory will prevent to loose CMOS options when battery fails.
Watchdog Timer	Dis	Dis	En./Dis.	This option enables the Watchdog option when the POST is running.
Watchdog After POST	Ds	Dis	En./Dis.	This option enables Watchdog circuit after the POST sequence
Watchdog Duration (ms)	262144	262144	64 to 262144	Use this option to setup duration time (in ms) of the Watchdog timing circuitry.
Current CPU Fan 1 and Fan 2 speed	-	-	Varies	Speed sensing device sets this value according to the fan speed. If no fan is installed or if a fan has no tachymetric capability, this value will be 0.
Current Vcpp1 and 2	-	-	Varies	This value is set according to the actual value of Vcpp1 & Vcpp2
Vin values : +12V, +5V, +3.3V, +2.5V	-	-	Varies	The values of these voltages are each displayed according to the current value.

4.2.9. Integrated Peripherals

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
On-Chip Primary IDE controller	En.	En.	En./Dis.	Select Enabled to activate the IDE controller. The four options below appear only if the On-Chip Primary option is enabled.
Master PIO Slave PIO	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
Master UDMA Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Ethernet Controller 1	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	OS	OS	OS/BIOS	This option is for DOS and BIOS support only (Win 95 has it is own drivers). **It does not enable or disable the USB controller.**
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	En.	En.	En./Dis.	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1	3F8/ IRQ4	3F8/ IRQ4	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3	Select a COM port address and IRQ# for Serial Port 1
Onboard Serial Port 2	RS-232	RS-232	RS-232 RS-422 RS-485	Select a COM port address for Serial Port 2.
Onboard Parallel Port	378/ IRQ7	378/ IRQ7	Disabled 3BC/IRQ7 378/IRQ7 278/IRQ5	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9	SPP, EPP1.9+SP P, ECP ECP+EPP1. 9, Normal, EPP1.7+SP P, ECP+EPP1. 7	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the parallel port.

4.3 UPDATING OR RESTORING THE BIOS IN FLASH

4.3.1 UBIOS.EXE 4.0 - BIOS update and copy utility

> ➲ IMPORTANT
> **This utility is used to update the BIOS on Kontron's single board computer. To ensure the success of this operation, please read entirely these instructions before using this program.**

You can run this utility in 2 different modes:

1. Interactive Mode: In this mode the program is menu-driven. This mode is explained in section 4.2.4.
2. Batch Mode: It is also possible to run the program without menus by a command, which specifies the selected options and files with parameters. This mode is explained in section 4.2.5.

4.3.2 How to do a successful update

UBIOS needs to be run in DOS 3.3 or higher or compatible environment.

1. Take note of your special BIOS options such as drive settings, hard disks and custom settings. After the update, these options will be set to their default values and all changes will need to be re-entered.
2. Ensure you have the proper BIOS file required to execute the update. These files may be obtained from Kontron WEB site, by Kontron technical support or by UBIOS itself. Refer to the 'How to do a successful copy' for details about the last source.
3. Boot in a driver free environment. **No Hi-memory driver must be loaded**. To boot with a free environment, follow these steps:
   - **In DOS**: Boot with the F5 key pressed, this will disable config.sys and autoexec.bat interaction.
   - **In Windows 9x**: Boot with the F8 key pressed and choose *'safe mode command prompt only'* option.
4. Call the UBIOS program and follow the instruction menu. To do a complete BIOS update, select item 'A) Update all BIOS'.

4.3.3 How to do a successful copy

Follow the same procedure as above.

To do a complete BIOS copy, select item '**a) Copy all BIOS'.**

Advanced functionality

Advanced functionality is resumed in the UBIOS help mode.
To call UBIOS help page, use UBIOS /?

VT-100 mode

UBIOS can be used without a screen in Kontron's VT-100 mode. This mode transfers all screen and keyboard text activity through the serial port.

To use UBIOS in vt-100, use the /vt argument like: UBIOS /vt

In this mode, scan code keys are not transmitted. These keys include the 'home', 'end', 'Pg Up', 'Pg Dn' keys that can be useful to UBIOS. To bypass this limitation, the numerical keypad can be used.

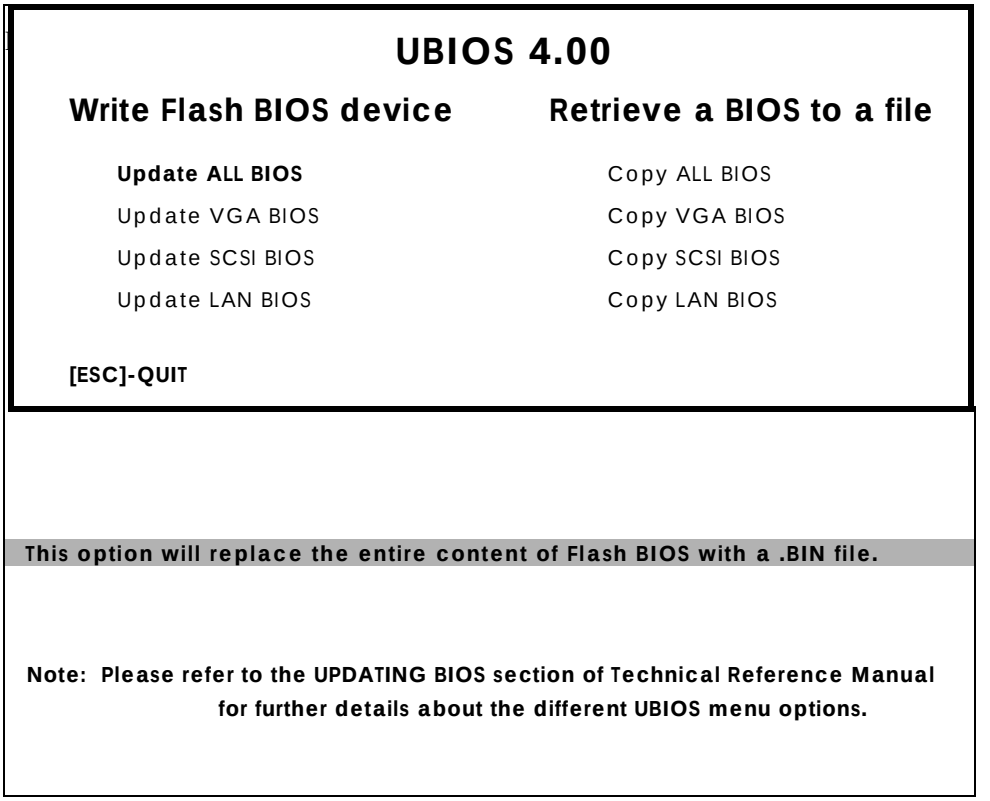
'7' will be assigned to 'home',
'8' to the up arrow,
'9' to 'Pg Dn'
…
'5' will be assigned to the 'Esc' key.

4.3.4 UBIOS - Interactive Mode

To run the program in interactive mode, type "UBIOS" from the DOS prompt and the UBIOS 4.0 presentation screen will be displayed. To continue, hit any key on the keyboard. This brings you to the main menu.

4.3.4.1 Main Menu

The main menu appears below:



The main menu displays two groups of options: Write Flash BIOS device and Retrieve a BIOS to a file. The first group allows you to update the Flash BIOS device with a BIOS file stored on disk. The second group allows you to copy the contents of the Flash BIOS device to files on disk.

In the above menu, the option **Update ALL BIOS** is highlighted and the option is described in the shaded row below. Move the arrow keys to highlight other options.

To **select** the highlighted option, press ENTER.
To **exit the program**, press the ESC key when you are in the main menu.

There are four types of BIOS files appearing on the main menu:

1. ALL BIOS File: This file combines all BIOS files contained in the Flash BIOS device in a single file. It has the .BIN extension.

2. VGA BIOS File: This file contains the VGA BIOS section of the Flash BIOS. There are two possible types of VGA BIOS files: files with the .VGA extension (supports CRT displays only) and files with the .BFP extension (supports CRT and Flat Panel displays).

3. SCSI BIOS File: This file contains the SCSI BIOS section of the Flash BIOS. It has the .BIN or .SCS extension.

4. LAN BIOS File: This file contains the LAN BIOS section of the Flash BIOS. It has the .BIN extension.

4.3.4.2 Updating the Flash BIOS

If you select one of the **Update** options from the main menu, a screen similar to the following is displayed:

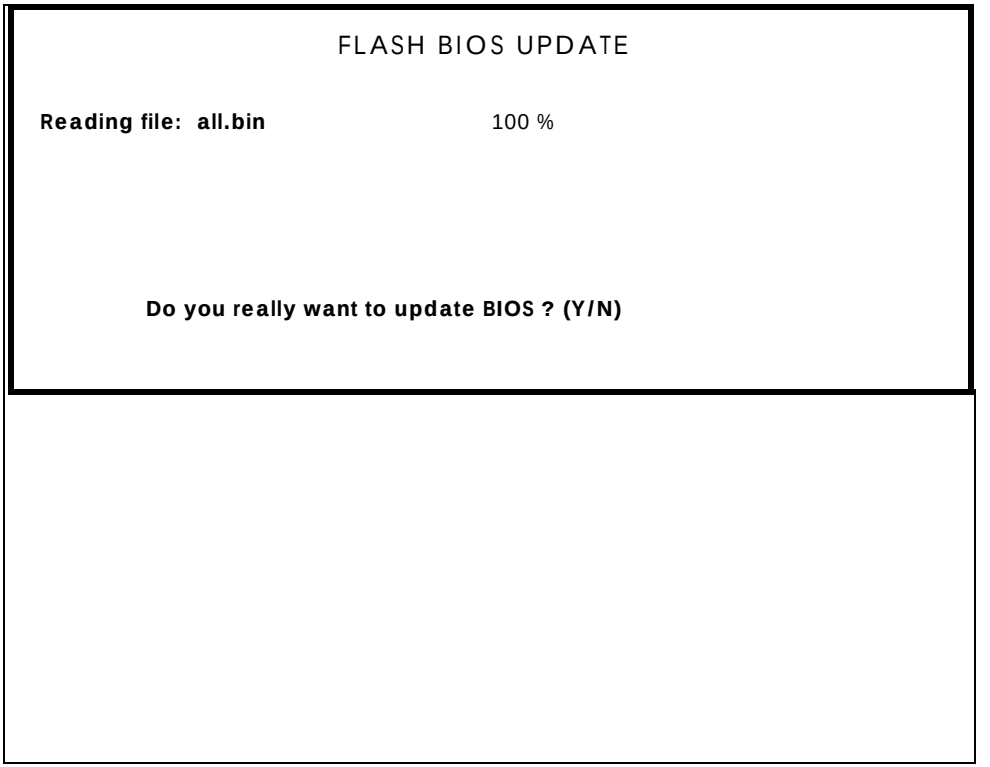
You are currently using:	**TEK1005** **MAIN BIOS VERSION: 0.0.1**
Current directory is:	**C:**
Searching for file:	***.bin**
File Number – SELECT drive.	**[ESC] – Quit this menu Drive letter to change**
File: **1- ALL.BIN**	**Documentation: NOT AVAILABLE**

Files of the type you selected in the main menu and which are in the current directory are displayed in the **File** window.

To change directory, type the drive letter. If there are any files of the type you selected in this directory, they will be displayed in the **File** window.

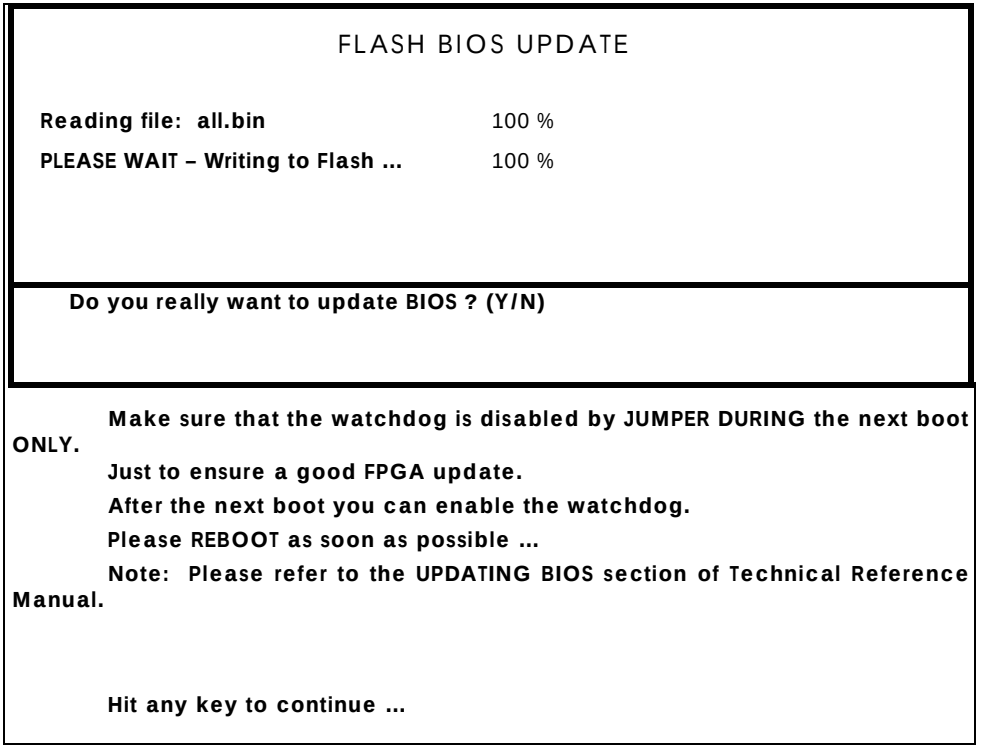
The **Documentation** window displays “NOT AVAILABLE”. It will be used in the future for displaying the contents of a .doc file.

If you want to return to the previous menu, press the ESC key.
To select a file from the **File** window, in order to update the Flash BIOS with this file, type the file number which appears before the filename in the list. A new screen is displayed as shown below. This is the Flash BIOS Update screen. You must first confirm if you want to update the Flash BIOS with the selected file (the filename appears next to **Reading file)**, by typing "Y" for Yes, "N" for No.



If you choose to update the file, by typing "Y", the program will write the file to Flash. The progress of the operation is indicated in percentage completed, next to **PLEASE WAIT – Writing to Flash …**

When the update is over the screen will appear as follow:

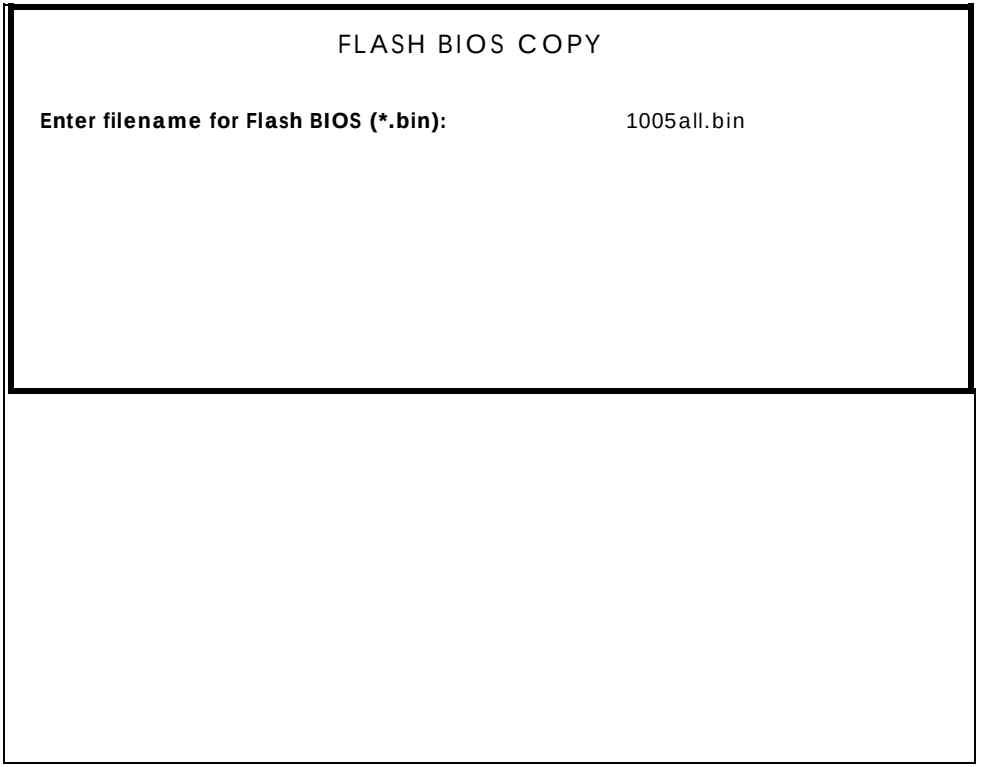


To return to the main menu, hit any key on the keyboard.

NOTE
There may be slight changes to the Flash BIOS Update screen compared to those shown here for an Update ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

4.3.4.3 Copying Flash BIOS

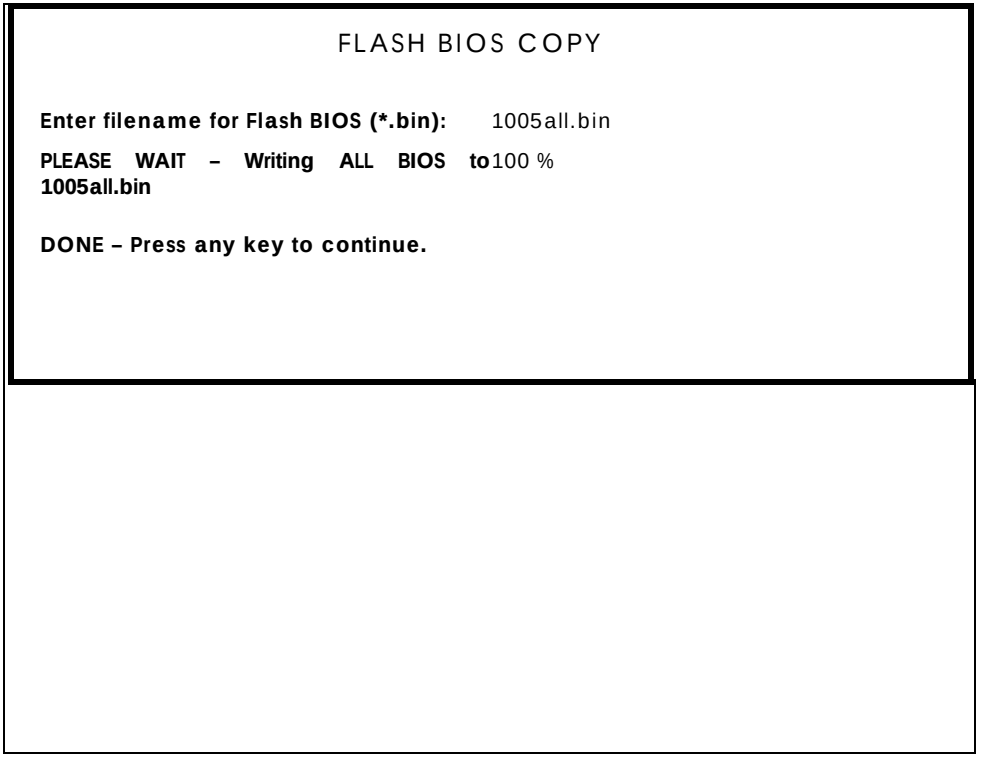
If you select one of the **Copy** options from the main menu, a screen similar to the following is displayed:



You begin a Flash Copy operation, by typing a filename (including the extension) for the file you are creating. In the above example, the filename entered was “1005all.bin”.

Press ENTER to proceed.

The progress of the operation will display on the screen in percentage completed. The example shown on the following page is for the Copy ALL BIOS option.



If the filename entered for the BIOS file already exists, the following message will appear on the screen:

File already exits! Overwrite? (Y/N)

If you choose to overwrite the existing file, its content will be lost.

To return to the main menu, hit any key on the keyboard.

> **NOTE**
> There may be slight changes to the Flash BIOS Copy screen compared to those shown here for a Copy ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

4.3.5 UBIOS – Batch Mode

While files can be manually selected using the Interactive Mode, Flash BIOS Update or Copy can be achieved through Batch Mode.

The command line format is as follows:

UBIOS /B [operation] [filetype] [filename] [options] where:

/B or /-B specifies that this is a Batch Mode command.

[operation] is the Flash BIOS operation you wish to perform, and can be replaced with one of three letters: U for Update, C for Copy, or V for Verify (used to compare the contents of the Flash BIOS device and the specified BIOS file).

[filetype] is the filetype of the BIOS file to program (with an update operation) or to create (with a copy operation), and can be replaced with one of the following:

ALL	for All BIOS files in a single file with the .BIN extension,
VGA	for VGA BIOS file with the .VGA or .BFP extension,
SCSI	for SCSI BIOS file with the .BIN extension,
LAN	for LAN BIOS file with the .BIN extension.

[filename] is the name of the BIOS file (including the extension) to program (with an update operation) or to create (with a copy operation), and can be replaced with the filename which corresponds to the filetype. For example, if "VGA" was listed as filetype, then the filename could be "FLAT.BFP".

[options] these are optional parameters that may be added:

/C This option will not clear the CMOS Setup when updating main BIOS (AWARD BIOS), however this is not recommended since the CMOS Setup should be updated when the main BIOS is changed.

/R Instructs UBIOS to reset the board upon completion of the operation.

/VT For VT100 compatibility.

/? To get a summary of the Batch Mode options from UBIOS. It will display a Batch options summary of valid UBIOS command lines. The same help information will also be displayed each time UBIOS detects an error in the command line.

4.4 VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.4.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.4.2 Setup & Configuration

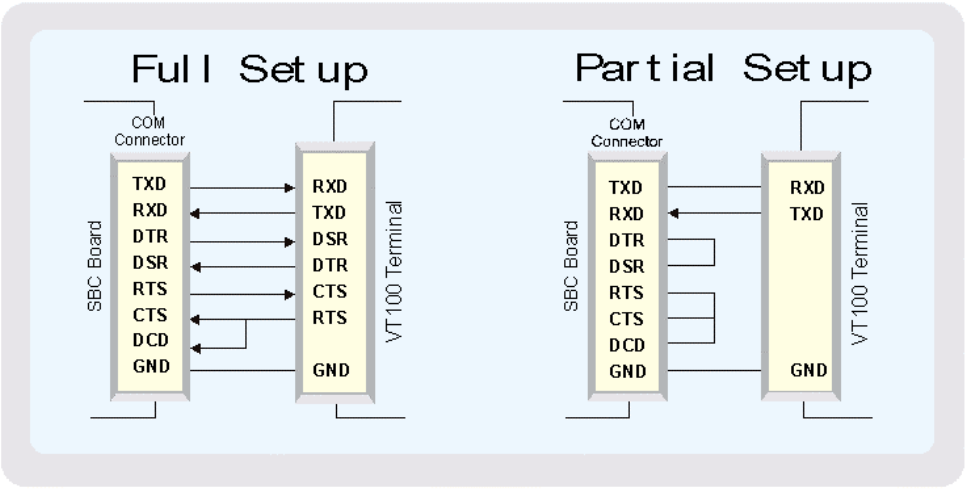
Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "BIOS Feature Setup"
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> NOTE
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



4.4.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

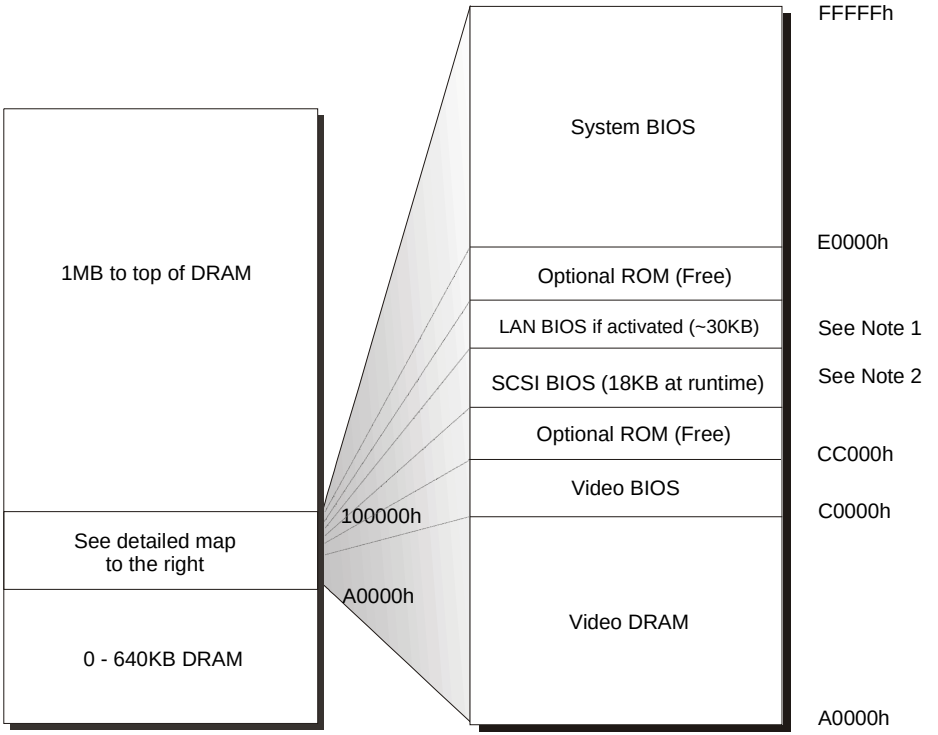
E. BIOS SETUP ERROR CODES

F. EMERGENCY PROCEDURE

G. GETTING HELP & RMA

A MEMORY & I/O MAPS

A.1 MEMORY MAPPING



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

A.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
x90-x9F				Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B IRQ AND DMA LINES

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	Secondary IDE * or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.

1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.2 DMA CHANNELS

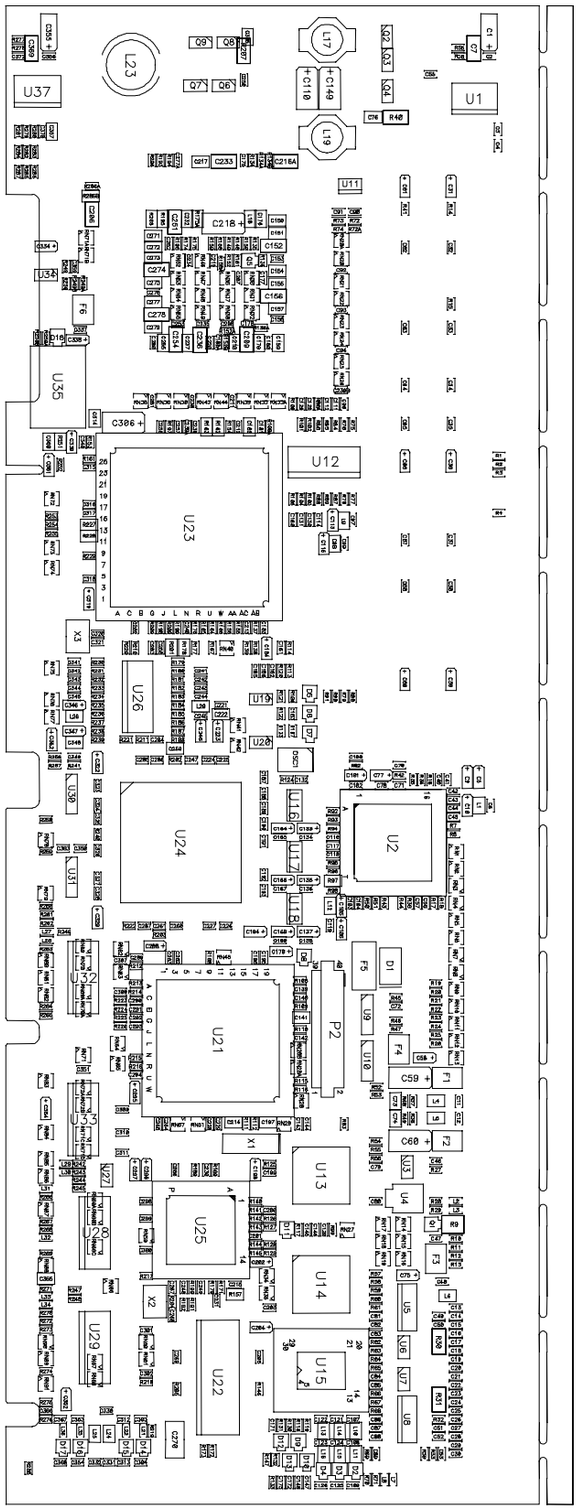
The PCI-946-1 and P3S440BX integrate the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

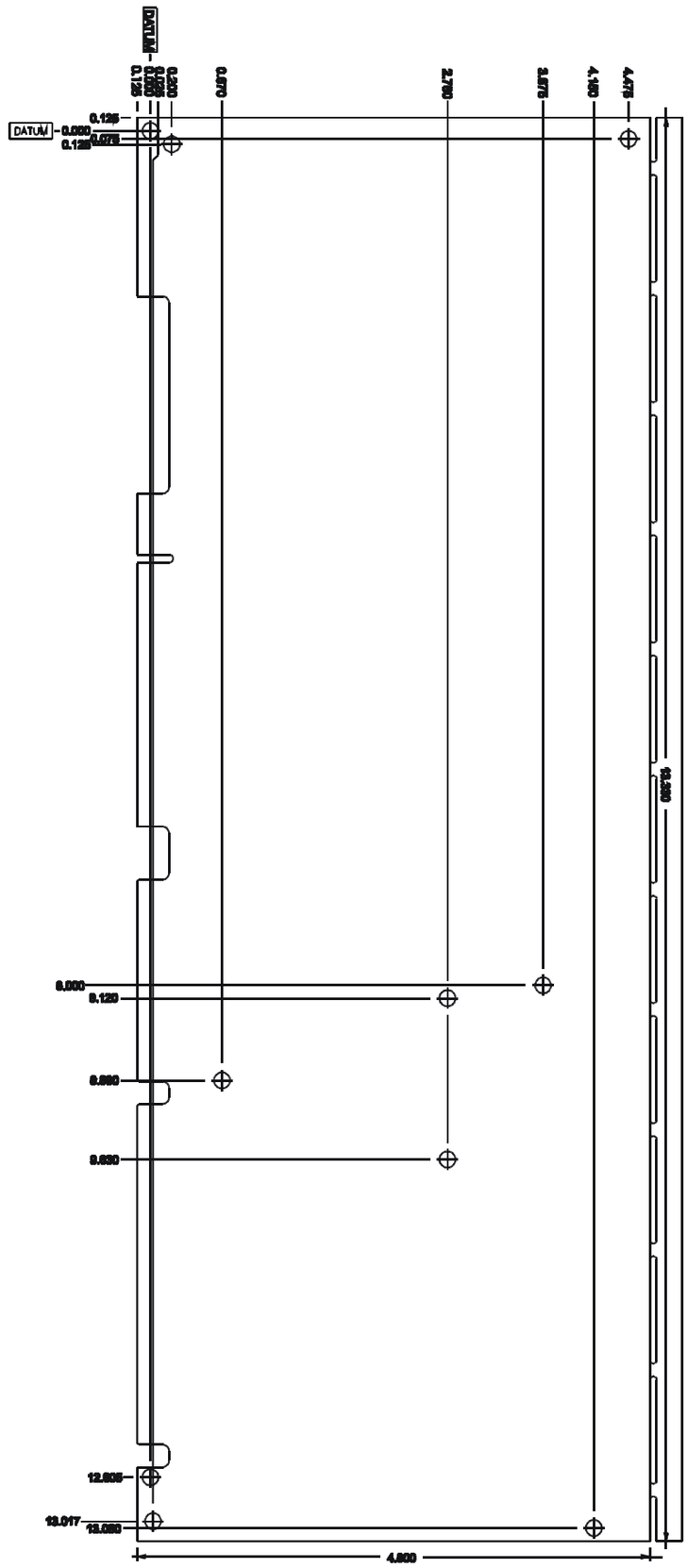
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C BOARD DIAGRAMS

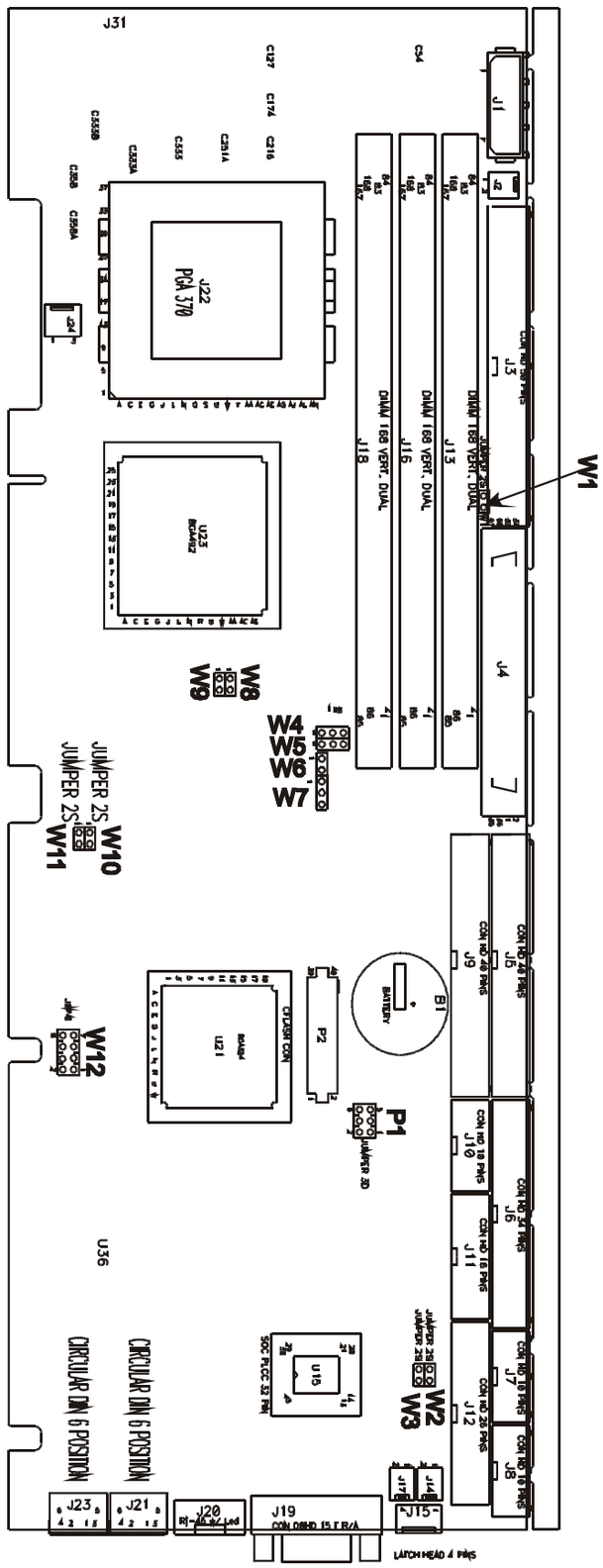
C.1 ASSEMBLY TOP DIAGRAM - PCI-946-1 AND P3S440BX



C.2 MOUNTING HOLES - PCI-946-1 AND P3S440BX



C.3 CONNECTOR C.S. - PCI-946-1 AND P3S440BX



D CONNECTOR PINOUTS

D.1 PCI-946-1 AND P3S440BX CONNECTORS AND HEADERS

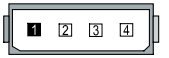
Connectors and Headers on the cPCI-MXP	
J1	Power Supply Connector
J2	EIDE/SCSI ACTIVITY LED Header
J3	8-bit SCSI Interface Connector
J4	16-bit SCSI Interface Connector
J5 & J9	Primary & Secondary Connectors
J6	Floppy Drive Connector
J7	Serial Port 1 – RS-232
J8	Serial Port 2 – RS-232, RS-422, RS-485
J10	USB Header
J11	Multi-Function Connector
J12	Parallel Port
J13	Memory 256Kb SDRAM DIMM 168-Pin Connector
J14	External Battery Connector
J15	PS/2 Mouse Header
J16	Memory 256Kb SDRAM DIMM 168-Pin Connector
J17	Power On/Off Button Connector
J18	Memory 256Kb SDRAM DIMM 168-Pin Connector
J19	CRT VGA Connector
J20	Ethernet 10Base-T/100Base-TX Connector
J21	PS/2 Mouse Connector
J22	PGA 370 or FC-PGA 370 CPU Socket
J23	PS/2 Keyboard Connector
J24	CPU Fan and Tachometer Header
P2	CompactFLASH Disk Connector
B1	CMOS Battery Backup connector

D.2 CONNECTOR PINOUTS

D.2.1 Power Supply Connector (J1)

Signal	
+12V	1
GND	2
GND	3
VCC	4

Top View



D.2.2 EIDE/SCSI ACTIVITY LED Header (J2)

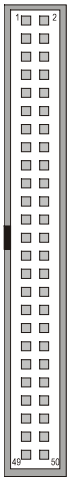
Signal	
+5V fused	1
LED signal	2

Front View

D.2.3 8-bit SCSI Interface Connector (J3)

Pin Number	Signal
1	GND
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	GND
19	GND
21	GND
23	GND
25	N.C.
27	GND
29	GND
31	GND
33	GND
35	GND
37	GND
39	GND
41	GND
43	GND
45	GND
47	GND
49	GND

Top View



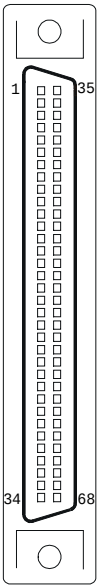
Pin Number	Signal
2	SD0
4	SD1
6	SD2
8	SD3
10	SD4
12	SD5
14	SD6
16	SD7
18	SDP
20	GND
22	GND
24	GND
26	Term Power
28	GND
30	GND
32	SATN
34	GND
36	SBSY
38	SACK
40	SRST
42	SMSG
44	SSEL
46	SCD
48	SREQ
50	SIO

* Active Low Signal

D.2.4 16-bit SCSI Interface Connector (J4)

Pin Number	
Signal	
GND	1
GND	2
GND	3
GND	4
GND	5
GND	6
GND	7
GND	8
GND	9
GND	10
GND	11
GND	12
GND	13
GND	14
GND	15
GND	16
Term Power	17
Term Power	18
Not Connected	19
GND	20
GND	21
GND	22
GND	23
GND	24
GND	25
GND	26
GND	27
GND	28
GND	29
GND	30
GND	31
GND	32
GND	33
GND	34

Top View



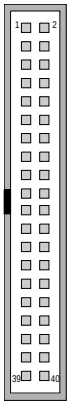
Pin Number	
	Signal
35	D12*
36	D13*
37	D14*
38	D15*
39	DPH*
40	D0*
41	D1*
42	D2*
43	D3*
44	D4*
45	D5*
46	D6*
47	D7*
48	DPL*
49	GND
50	GND
51	Term Power
52	Term Power
53	Not Connected
54	GND
55	ATN*
56	GND
57	BSY*
58	ACK*
59	RST*
60	MSG*
61	SEL*
62	C/D*
63	REQ*
64	I/O*
65	D8*
66	D9*
67	D10*
68	D11*

* Active Low Signal

D.2.5 Primary & Secondary EIDE Connector (J5 & J9)

Pin Number	
Signal	
RESET*	1
DD7	3
DD6	5
DD5	7
DD4	9
DD3	11
DD2	13
DD1	15
DD0	17
GND	19
DMARQ	21
DIOW*	23
DIOR*	25
IORDY	27
DMACK*	29
INTRQ	31
DA1	33
DA0	35
CS0*	37
LED (DASP*)	39

Top View



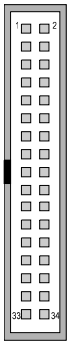
Pin Number	
	Signal
2	GND
4	DD8
6	DD9
8	DD10
10	DD11
12	DD12
14	DD13
16	DD14
18	DD15
20	Not Connected (KEY)
22	GND
24	GND
26	GND
28	GND (CSEL)
30	GND
32	Not Connected (IOCS16*)
34	Not Connected (PDIAG*)
36	DA2
38	CS1*
40	GND

* Active Low Signal

D.2.6 Floppy Drive Connector (J6)

Pin Number	
Signal	
GND	1
GND	3
GND	5
GND	7
GND	9
GND	11
GND	13
GND	15
Not Connected	17
GND	19
GND	21
GND	23
GND	25
Not Connected	27
PRESENT* (GND)	29
GND	31
Not Connected	33

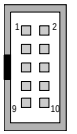
Top View



Pin Number	
	Signal
2	DRVEND*
4	Not Connected
6	Not Connected
8	INDEX*
10	MTR0*
12	FPDS1*
14	FPDS0*
16	MTR1*
18	FPDIR*
20	STEP*
22	WDATA*
24	WGATE*
26	TRK0*
28	WRTPRT*
30	RDATA*
32	HDSEL*
34	DSKCHG*

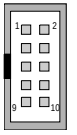
* Active Low Signal

D.2.7 Serial Port 2 & 1 - (J7 & J8) RS-232

Pin Number		Top View	Pin Number	
Signal				Signal
DCD	1		2	DSR
RXD*	3		4	RTS
TXD*	5		6	CTS
DTR	7		8	RI
GND	9		10	Not Connected

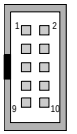
* Active Low Signal

D.2.8 Serial Port 2 - (J8) RS-422/RS-485

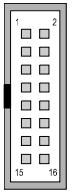
Pin Number		Top View	Pin Number	
Signal				Signal
Leave Floating	1		2	Leave Floating
RX(-)	3		4	RX(+)
TX(-)	5		6	TX(+)
Leave Floating	7		8	Leave Floating
GND	9		10	Not Connected

* Active Low Signal

D.2.9 USB Header (J10)

Pin Number		Top View	Pin Number	
Signal				Signal
+5V fused	1		2	+5V fused
USBP0-	3		4	USBP1-
USBP0+	5		6	USBP1+
GND	7		8	GND
GND	9		10	GND

D.2.10 Multi-Function Connector (J11)

Pin Number		Top View	Pin Number	
Signal				Signal
KCLK	1		2	GND
KDAT	3		4	GND
+5V fused	5		6	+5V fused
SPKR	7		8	+5V fused
Not connected	9		10	GND
DOWNLD*	11		12	GND
PBRES*	13		14	GND
HDACT*	15		16	+5V fused

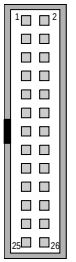
* Active Low Signal

D.2.11 Parallel Port Connector (J12)

D.2.12 Standard Mode

Pin Number	
Signal	
STB*	1
PD0	3
PD1	5
PD2	7
PD3	9
PD4	11
PD5	13
PD6	15
PD7	17
ACK*	19
BUSY	21
PE	23
SLCT	25

Top View



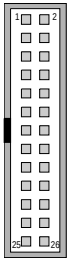
Pin Number	
	Signal
2	ALF*
4	ERR*
6	INIT*
8	SLCTIN*
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

* Active Low Signal

D.2.13 EPP Mode

Pin Number	
Signal	
WRITE*	1
PD0	3
PD1	5
PD2	7
PD3	9
PD4	11
PD5	13
PD6	15
PD7	17
INTR	19
WAIT*	21
N.C.	23
N.C.	25

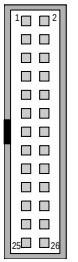
Top View



Pin Number	
	Signal
2	DATASTB*
4	N.C.
6	N.C.
8	ADDRSTRB*
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

* Active Low Signal

D.2.14 ECP Mode

Pin Number		Top View	Pin Number	
Signal				Signal
STROBE*	1		2	AUTOFD*, HOSTACK[2]
PD0	3		4	FAULT*[1], PERIPHRQST*[2]
PD1	5		6	INIT*[1], REVERSERQST*[2]
PD2	7		8	SELECTIN*[1,2]
PD3	9		10	GND
PD4	11		12	GND
PD5	13		14	GND
PD6	15		16	GND
PD7	17		18	GND
ACK*	19		20	GND
BUSY, PERIPHACK[2]	21		22	GND
PERROR, ACKREVERSE[2]	23		24	GND
SELECT	25		26	GND

* Active Low Signal, [1] Compatible Mode, [2] High Speed Mode

D.2.15 External Battery Header (J14)

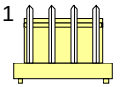
Signal	
Battery (+)	1
Battery (-)	2

Front View

D.2.16 PS/2 Mouse Header (J15)

Signal	
MCLOCK	1
GND	2
MDATA	3
+5V fused	4

Front View



D.2.17 Power Button Connector (J17)

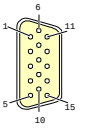
Signal	
PWRBTN	1
GND	2

Top View

D.2.18 CRT VGA Interface Connector (J19)

Signal		Signal		Signal	
RED	1	Analog GND	6	Not Connected	11
GREEN	2	Analog GND	7	DDC data	12
BLUE	3	Analog GND	8	HSYNC	13
Not Connected	4	Not Connected	9	VSYNC	14
GND	5	GND	10	DDC clock	15

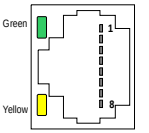
Front View



D.2.19 Ethernet 10Base-T/100Base-TX Connector (J20)

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

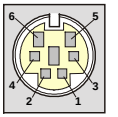
Front View



D.2.20 PS/2 Mouse Connector (J21)

Signal	
MDATA	1
Not Connected	2
GND	3
5V fused	4
MCLOCK	5
Not Connected	6

Front View

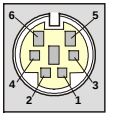


(Connector front view)

D.2.21 PS/2 Keyboard Connector (J23)

Signal	
KDATA	1
Not Connected	2
GND	3
+5V fused	4
KCLOCK	5
Not Connected	6

Front View



(Connector front view)

D.2.22 CPU Fan Header (J24)

Signal	
SENSE	1
+12V fused	2
GND	3

D.2.23 CompactFlash™ Disk Pinout (P2)

Pin Number	Signal Flow	Signal	Pin Number	Signal Flow	Signal
1	I/O	DD11	2	-	GND
3	I/O	DD12	4	I/O	DD3
5	I/O	DD13	6	I/O	DD4
7	I/O	DD14	8	I/O	DD5
9	I/O	DD15	10	I/O	DD6
11	O	CS1*	12	I/O	DD7
13	-	DMACK*	14	O	CS0*
15	-	DMARQ	16	O	DIOR*
17	I/O	PDIAG*	18	O	DIOW*
19	I	IRQ15	20	-	VCC (+5V)
21	-	VCC (+5V)	22	-	VCC (+5V)
23	-	GND	24	-	GND
25	O	RESET*	26	-	GND
27	O	W10 Jumper Select	28	O	DA2
29	O	DA1	30	I	*DASP
31	O	DA0	32	-	I/ORDY
33	I/O	DD0	34	I/O	DD8
35	I/O	DD1	36	I/O	DD9
37	I/O	DD2	38	I/O	DD10
39	-	Not Connected	40	-	GND

*** Active low signal**

D.2.24 PCI Bus Edge Connector

Pin Number component side		Pin Number solder side		Pin Number component side		Pin Number solder side	
+5V (TRST*)	E1	F1	N.C. (-12V)	C/BE0*	E52	F52	AD08
+12V	E2	F2	N.C. (TCK)	N.C. (3.3V)	E53	F53	AD07
N.C. (TMS)	E3	F3	GND	AD06	E54	F54	N.C. (+3.3V)
TD	E4	F4	TD	AD04	E55	F55	AD05
+5V	E5	F5	+5V	GND	E56	F56	AD03
INTA*	E6	F6	+5V	AD02	E57	F57	GND
INTC*	E7	F7	INTB*	AD00	E58	F58	AD01
+5V	E8	F8	INTD*	+5V	E59	F59	+5V
CLKC	E9	F9	REQ3*	REQ64*	E60	F60	ACK64*
+5V	E10	F10	REQ1*	+5V	E61	F61	+5V
CLKD	E11	F11	GNT3*	+5V	E62	F62	+5V
GND	E12	F12	GND				
GND	E13	F13	GND				
GNT1*	E14	F14	CLKA				
RST*	E15	F15	GND				
+5V (I/O)	E16	F16	CLKB				
GNT0*	E17	F17	GND				
GND	E18	F18	REQ0*				
REQ2*	E19	F19	+5V				
AD30	E20	F20	AD31				
N.C. (+3.3V)	E21	F21	AD29				
AD28	E22	F22	GND				
AD26	E23	F23	AD27				
GND	E24	F24	AD25				
AD24	E25	F25	N.C. (+3.3V)				
GNT2*	E26	F26	C/BE3*				
N.C. (+3.3V)	E27	F27	AD23				
AD22	E28	F28	GND				
AD20	E29	F29	AD21				
GND	E30	F30	AD19				
AD18	E31	F31	N.C. (+3.3V)				
AD16	E32	F32	AD17				
N.C. (+3.3V)	E33	F33	C/BE2*				
FRAME*	E34	F34	GND				
GND	E35	F35	IRDY*				
TRDY*	E36	F36	N.C. (+3.3V)				
GND	E37	F37	DEVSEL*				
STOP*	E38	F38	GND				
N.C. (+3.3V)	E39	F39	LOCK*				
SDONE (N.C.)	E40	F40	PERR*				
SBO* (N.C.))	E41	F41	N.C. (+3.3V)				
GND	E42	F42	SERR*				
PAR	E43	F43	N.C. (+3.3V)				
AD15	E44	F44	C/BE1*				
N.C. (+3.3V)	E45	F45	AD14				
AD13	E46	F46	GND				
AD11	E47	F47	AD12				
GND	E48	F48	AD10				
AD09	E49	F49	GND				

* Active Low Signal, N.C. Not Connected

D.2.25 ISA Bus Edge Connector

Pin Number component side		Pin Number solder side		Pin Number component side		Pin Number solder side	
IOCHK*	A1	B1	GND	SBHE*	C1	D1	MEMCS16*
SD7	A2	B2	RESETDRV	LA23	C2	D2	IOCS16*
SD6	A3	B3	+5V	LA22	C3	D3	IRQ10
SD5	A4	B4	IRQ9	LA21	C4	D4	IRQ11
SD4	A5	B5	N.C. (-5V)	LA20	C5	D5	IRQ12
SD3	A6	B6	DRQ2	LA19	C6	D6	IRQ15
SD2	A7	B7	N.C. (-12V)	LA18	C7	D7	IRQ14
SD1	A8	B8	ZEROWS*	LA17	C8	D8	DACK0*
SD0	A9	B9	+12V	MEMR*	C9	D9	DRQ0
IOCHRDY	A10	B10	GND	MEMW*	C10	D10	DACK5*
AEN	A11	B11	SMEMW*	SD8	C11	D11	DRQ5
SA19	A12	B12	SMEMR*	SD9	C12	D12	DACK6*
SA18	A13	B13	IOW*	SD10	C13	D13	DRQ6
SA17	A14	B14	IOR*	SD11	C14	D14	DACK7*
SA16	A15	B15	DACK3*	SD12	C15	D15	DRQ7
SA15	A16	B16	DRQ3	SD13	C16	D16	+5V
SA14	A17	B17	DACK1*	SD14	C17	D17	MASTER*
SA13	A18	B18	DRQ1	SD15	C18	D18	GND
SA12	A19	B19	REFRESH*				
SA11	A20	B20	SYSCLK				
SA10	A21	B21	IRQ7				
SA9	A22	B22	IRQ6				
SA8	A23	B23	IRQ5				
SA7	A24	B24	IRQ4				
SA6	A25	B25	IRQ3				
SA5	A26	B26	DACK2*				
SA4	A27	B27	TC				
SA3	A28	B28	BALE				
SA2	A29	B29	+5V				
SA1	A30	B30	OSC				
SA0	A31	B31	GND				

* Active Low Signal, N.C. Not Connected

E BIOS SETUP ERROR CODES

E.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	-	Success of the boot block recovery code. The board is ready to be manually reset.

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

E.1.1 If a message is displayed, it will be accompanied by:

E.1.1.1 "PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

E.3.1.1 CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W4. The board is shipped with W4 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

E.3.1.2 CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

E.3.1.3 DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

E.3.1.4 KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

E.3.1.5 OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

E.3.1.6 PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

E.4 POST CODES

POST #	Designation	Description
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization. Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.
07	Test CMOS Interface and Battery Status	1. Install the Kontron segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).
08	Program Chipset default	Program Chipset default (show POST BEh).
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). *14. Kill Onboard PnP IO.* *15. PnP Early Initialization.* *16. PnP System Resource:* *1. Get ESCD.* *2. Create default SYSTEM_MAP.* *3. Decode/Record ISA ESCD resources.* *4. Record I/O port for PnP operation.* 17. Chipset Early Shadow.

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary).	Boot Block 1st : Verify BIOS checksum.
		2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	*1. On M1 set the cache for the memory installed.* *2. On PCI, do a PCI ROM init.* 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

POST #	Designation	Description
17	Test Struck 8259's Interrupt Bits	Nothing
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.
1A-1E	Reserved	Reserved
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33-3C	Reserved	Reserved
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F-40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. | Boot Block <u>in EMERGENCY</u>: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48-4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	*Ask password security if needed.*
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.

POST #	Designation	Description	
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.	
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.	
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.	
54-5F	Reserved	Reserved	
60		Store boot partition of head & cylinder.	
61	Final Init	*For last µs detail before boot.*	
62	Num Lock ON	Put Num Lock ON and Daylight Saving.	
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.	
64-7F	Reserved	Reserved	
80	Kontron Segment Move 1	Install the Kontron segment from Flash to DC00:0h.	
81	Kontron Segment Move 2	Install the Kontron segment from DC00:0h to 7000:0h.	
82	Kontron Segment Move 3	Install the Kontron segment from 7000:0h to EC00:0h.	
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.	
84	Kontron CRC Check	Check if Kontron block have a valid CRC. If not, the Emergency procedure is launched.	
85-AF	Reserved	Reserved	
B0	Spurious	If interrupt occurs in protected mode.	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2-BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature “*BBSS*”.
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	

POST #	Designation	Description
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.
CB-CF	Reserved	Reserved
D0	Power Management Full speed	Trying to go back or into full speed mode.
D1	Power Management -- Doze mode	Trying to go or in Doze mode.
D2	Power Management—Sleep mode	Trying to go or in Sleep mode.
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4-DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1-EE	Setup Page	Page 1 to Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0-FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

F EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error occurred during the Boot Block Flash BIOS update (when using UBIOS utility program or if you meet one of the following symptoms at anytime:

1. No POST code on a power up (when using a POST card).
2. System stops at POST 41(when using a POST card) and associated beep code is generated (Refer to Section E.1).
3. Board does not boot, even after usual hardware and connection verifications.

F.1 HOW TO RUN EMERGENCY PROCEDURE

F.1.1 To run an EMERGENCY PROCEDURE, proceed as follows:

1. Remove battery jumper.
2. Disable the Power Fail Detection function.
3. Connected a 1.44MB floppy drive (drive A) to the board, and insert the EMERGENCY diskette, that you previously created, in it.
4. Power on the board. (Note that no VGA is present during this procedure.)
5. Boot block flash update will be completed when the POST code 55 is displayed (when using a POST card) or the associated beep code sounds (indicated in Section E-5).
6. After the procedure is successfully completed, power down the board, install your battery and Power Fail Detection jumpers.
   The boot block flash BIOS should be correctly programmed and the system should run properly.

NOTE

See section F.2 Generate a Emergency Floppy Diskette.

F.2 GENERATE AN EMERGENCY FLOPPY DISKETTE :

F.2.1 Use a system that has a 1.44 Mbytes floppy drive A.

1. Insert the Kontron Emergency Diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available on Kontron's CDROM).
3. Insert a DOS formatted floppy diskette in drive A.
4. At the DOS prompt of your hard drive (same path of the two files WDISK.COM and EMERDISK.TEK), type WDISK EMERDISK.TEK then press Enter key.
5. The program may display one of the following messages:

F.1.1.1 "Emergency Code transferred"

The emergency diskette has been successfully created. Take the appropriate actions and restart from the step 4) when you see the following messages.

F.1.1.2 "Write to disk failure!"

Verify if your floppy diskette is write-protected.

F.1.1.3 "The file to program in flash was not found"

F.1.1.3.1 Be sure that EMERDISK.TEK file is in your current path.

"Unable to read the binary file" or "Unable to close the opened file"

Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

F.1.1.4 "Unable to allocate a memory block of 256 Kbytes"

F.1.1.4.1 Not enough memory to run the WDISK program.

G GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you may reach us at the above numbers or by writing to :

Kontron Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

G.1 LIMITED WARRANTY

Kontron Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

G.2 RETURNING DEFECTIVE MERCHANDISE

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:
- The Kontron Invoice number
- Your purchase order number
- The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.
3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.
4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:
- Make a copy of the request form on the following page.
- Fill out the form and be as specific as you can about the board's problem.
- Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
6) When returning a Kontron board:
   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.
   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Teknor's Technical Support department in Canada at (450) 437-8053