Harris Semiconductor

APPNOTE

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Harris Wireless Products

Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the AM79C930 Media Access Controller

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Introduction

This document includes a description of the HW/SW interface for the IEEE802.11 target radio architecture based on the Harris PRISM™ chip set and the AMD Media Access Controller (MAC) AM79C930 processor. The information includes all the necessary interface requirements that can be used to control the PRISM radio with any other controller or processor that does not necessarily target IEEE802.11. The design example, though, addresses special design issues interfacing with the AM79C930.

Hardware Configuration

The block diagram in Figure 1 is intended to show a top level view of the basic hardware devices comprising the radio design. The detailed list of all signal interfaces required between MAC and the Physical Layer (PHY) or the PRISM radio are listed in Table 1 of this document.

List of Signals

Table 1 summarizes the signals that are required to control the PHY radio operations. The first column lists the PHY signal name, the second column indicates whether the signal is an output or an input to the MAC, the next column contains a brief description of each listed signal and the last two columns indicate the HW component part number and the pin connection for each of the listed signals at both the PHY and the MAC ends.

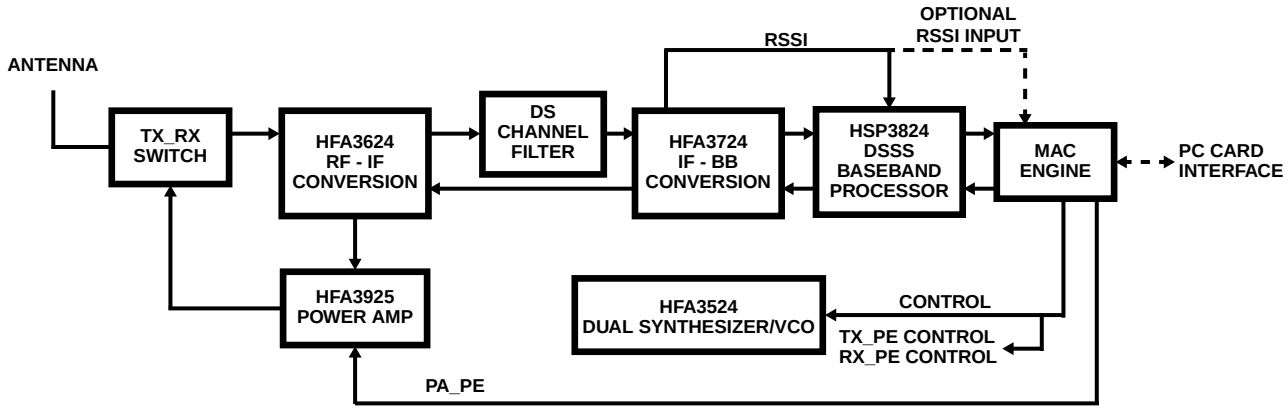


FIGURE 1. PRISM™ CHIPSET SYSTEM BLOCK DIAGRAM

Summary List of MAC-PHY Interface Signals

TABLE 1. MAC-PHY INTERFACE SIGNALS

PHY SIGNAL NAME	I/O FROM/ TO MAC	DESCRIPTION	PHY PART/PIN NUMBER	MAC PIN NUMBER AM79C930
SYNTH_DATA	O	Serial Data Bus (Synthesizer)	HFA3524 (12)	MAC (102)
SYNTH_CLK	O	Serial Control Clock (Synthesizer)	HFA3524 (11)	MAC (101)
SYNTH_LE	O	Load Enable (Synthesizer)	HFA3524 (13)	MAC (3)
RX_PE	O	Receive Power Enable (RF/IF Converter)	HFA3624 (28)	MAC (126)
TX_PE	O	Transmit Power Enable (RF/IF Convt.)	HFA3624 (15)	MAC (142)
RX_PE	O	Receive Power Enable (Qmodem)	HFA3724 (21, 43, 54, 74)	MAC (126)
TX_PE	O	Transmit Power Enable (Qmodem)	HFA3724 (22, 41)	MAC (142)
SEL0	O	Low Pass Filter Control (Qmodem)	HFA3724 (17)	MAC (132)
SEL1	O	Low Pass Filter Control (Qmodem)	HFA3724 (16)	MAC (141)
TX_PE_BB	O	Transmit Power Enable (transmit port)	HSP3824 (2)	MAC (131)
TXD	O	Transmit Data (Transmit Port)	HSP3824 (3)	MAC (121)
TXCLK	I	Transmit Clock (Transmit Port)	HSP3824 (4)	MAC (115)
TX_RDY	I	Transmit Data Ready (Transmit Port)	HSP3824 (5)	MAC (91)
RX_PE_BB	O	Receiver Power Enable (Receive Port)	HSP3824 (33)	MAC (122)
MD_RDY	I	MAC Data Ready (Receive Port)	HSP3824 (34)	MAC (95)
RXD	I	Receive Data (Receive Port)	HSP3824 (35)	MAC (123)
RXCLK	I	Receive Clock (Receive Port)	HSP3824 (36)	MAC (124)
CS	O	Chip Select (Control Port)	HSP3824 (9)	MAC (107)
AS	O	Address Strobe (Control Port)	HSP3824 (23)	MAC (105)
R/W	O	Read/write Strobe (Control Port)	HSP3824 (8)	MAC (103)
SCLK	O	Serial Control Clock (Control Port)	HSP3824 (24)	MAC (101)
SDATA	I/O	Bi-directional Serial Data Bus (Cnt. Port)	HSP3824 (25)	MAC (102)
CCA	I	Clear Channel Assessment	HSP3824 (32)	MAC (96)
RESET	O	Master Reset	HSP3824 (28)	MAC (118)
PA_PE	O	Transmit Amplifier Power Enable (RFPA)	HFA3925 (11,18, 23)	MAC (131)
OSC_START	O	VCO Enable Circuit	VCO Startup Circuit	MAC(92)
RADIO_PE	O	Radio Power Enable.	RADIO	MAC (2)

Interface Signal Description

Table 2 Consists of a functional description for each of the PHY signals that are part of the HW/SW interface.

TABLE 2. MAC-PHY INTERFACE SIGNALS

SIGNAL NAME	SIGNAL DESCRIPTION
SYNTH_DATA	Binary serial data input used to configure the PHY RF frequency synthesizer (HFA3524). Data is entered MSB first. A single data transfer is 22-bits wide. This is a high impedance CMOS input to the PHY.
SYNTH_CLK	This is the clock for the SYNTH_DATA. The data is clocked in the appropriate synthesizer register on the rising edge of SYNTH_CLK. This is a high impedance CMOS input to the PHY.
SYNTH_LE	Load enable for the PHY RF frequency synthesizer (HFA3524). When signal goes active (High), data stored in the shift register is loaded in one of the 4 synthesizer operational registers as defined by the control bits which are the two LSBs of the SYNTH_DATA.
SEL0, SEL1	Digital control input to the PHY. Selects four programmed cut off frequencies for both receive and transmit channels of the analog baseband LPF. Tuning speed from one cutoff to another is less than 1ms. For IEEE802.11 the 8.8MHz cutoff frequency is used. SEL1 SEL0 Cutoff Frequency — SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz — HI LO 8.8MHz LO HI 4.4MHz — HI HI 17.6MHz
TX_PE	Transmit Channel Power Enable Control Input. TTL compatible input. Enable logic level is High. This signal controls several IF/RF components of the PHY transmit chain. It is driving a total of 3 PHY inputs of the PHY components HFA3634 and HFA3724.
RX_PE	Receive Channel Power Control Input. TTL compatible input. Enable logic level is High.This signal controls several IF/RF componets of the PHY. It is driving a total of 5 PHY inputs of the PHY components HFA3624 and HFA3724.
TX_PE_BB	TX_PE_BB is an input from the Media Access Controller (MAC). The rising edge of TX_PE_BB will start the internal transmit state machine of the PHY digital modem and the falling edge will inhibit the state machine. TX_PE _BB en velopes the transmit data.
TXD	TXD is an input, used to transfer serial Data or Preamble/Header information bits from the MAC to the PHY digital modem (HSP3824). The data is received serially with the LSB first. The data is clocked in the HSP3824 at the falling edge of TXCLK.
TXCLK	TXCLK is a clock output used to receive the data on the TXD from the MAC to the PHY digital modem (HSP3824), synchronously. Transmit data on the TXD bus is clocked into the PHY on the falling edge.
TX_RDY	When the HSP3824 is configured to generate the Preamble and Header information internally, TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HSP3824 is ready to receive the data packet from the network processor over the TXD serial bus. TX_RDY returns to the inactive state when TX_PE goes inactive indicating the end of the data transmission. TX_RDY is an active high signal. This signal is meaningful only when the HSP3824 generates its own Preamble.
CCA	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm is user programmable and makes its decision as a function of RSSI, Energy detect (ED), Carrier Sense (CRS) and the CCA watch dog timer. The CCA algorithm and its programmable features are described in the data sheet of the HSP3824 PHY component. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). NOTE: This polarity is programmable and can be inverted.
RXD	RXD is an output to the MAC transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD-RDY.
RXCLK	RXCLK is the output bit clock to the MAC. This clock is used to transfer Header information and data through the RXD serial bus to the MAC. This clock reflects the bit rate in use. RXCLK will be held to a logic "0" state during the acquisition process of the PHY. RXCLK becomes active when the PHY enters in the data demodulation mode, im mediately following signal acquisition. This occurs once bit sync is declared and a valid signal quality estimate is made, when comparing the programmed signal quality thresholds.
MD_RDY	MD_RDY is an output signal to the MAC, indicating a data packet is ready to be transferred to the MAC. MD_RDY is an active high signal and it envelopes the data transfer to the MAC over the RXD serial bus. MD_RDY returns to its inactive state when there is no more receiver data, when the programmable data length counter reaches its value or when the link has been interrupted. MD_RDY remains inactive during preamble synchronization. MD_RDY can be programmed to become active after the SFD detection in the protocol or after the CRC check field in the Header.

TABLE 2. MAC-PHY INTERFACE SIGNALS (Continued)

SIGNAL NAME	SIGNAL DESCRIPTION
RX_PE_BB	When active, digital modem receiver of the PHY is configured to be operational, otherwise the digital modem receiver (HSP3824) is in standby mode. This is an active high input signal.
SD	SD is a serial bi-directional data bus which is used to transfer address and data to/from the internal registers of the PHY digital modem. The bit ordering of an 8-bit word is MSB first. The first 8-bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read from that register.
SCLK	SCLK is the clock for the SD serial bus of the PHY digital modem. The data on SD is clocked at the rising edge. SCLK is an input clock to the PHY digital modem (HSP3824). The maximum rate of this clock is 10MHz.
AS	AS is an address strobe used to envelope the Address or the data on SD of the PHY digital modem. This is an input signal to the PHY digital modem (HSP3824) Logic 1 = envelopes the address bits. Logic 0 = envelopes the data bits.
R/W	R/W is an input to the PHY digital modem (HSP3824) used to change the direction of the SD bus when reading or writing data on the SD bus. R/W must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
CS	CS is a chip select for the PHY digital modem to activate the serial control port. This is an input signal to the PHY. The CS doesn't impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, AS and R/W become "don't care" signals.
RESET	Master reset for the PHY digital modem (HSP3824). When active, TX and RX functions are disabled. If RESET is kept low the HSP3824 goes into the power standby mode. RESET does not alter any of the configuration register values nor does it preset any of the registers into default values. The device requires programming upon power-up. RESET can be either active or inactive during programming of the device.
PA_PE	Enable for the PHY RF power amplifier (HFA3925) to start transmission. This is a digital interface. A Logic "1" enables the transmission.
OSC_START	Enable for the VCO Startup Circuit. A low going pulse of 200 $\pm$10μs is required to activate the VCO after programming the synthesizer.
RADIO_PE	Enable for power regulators and clocks driving the PHY. A logic "1" enables operation, a logic "0" puts the complete PHY in a power down mode.

HW/SW Interfaces

There are four primary HW/SW interfaces that are used for configuration and during normal operation of the device. The interfaces are power on initialization, transmit mode operation, receive mode operation and power shut down mode. These interfaces are summarized as follows

- The **Initialization & Control Interface,** which is used to configure, write and/or read the status of the physical layer digital modem and the RF synthesizer. This interface is required to configure the programmable portions of the PHY during power up and coming out of certain power down modes. This interface is also used during operations for real time reconfiguration of PHY parameters and / or for reading PHY status.
- The **TX Interface**, which is used to control the transmit data transfers between the MAC and the physical layer. It is also used to control all PHY devices for the transmit chain of the radio.
- The **RX Interface**, which is used to control the receive data transfers between the MAC and the physical layer. It is also used to control all PHY devices for the receive chain of the radio.
- The **Power Down Interface**, which is used to set the physical layer into one of three power savings modes.

INITIALIZATION & CONTROL INTERFACE

This HW/SW interface is used to configure and monitor the programmable registers of the PHY. There are two PHY devices that contain programmable registers:

- The digital modem
- The RF frequency synthesizer. This interface is required to configure the PHY radio upon power up initialization and to monitor status during normal operation. This interface is also used to select or switch the frequency channel as required for the transmit and receive operations.

Digital Modem Interface

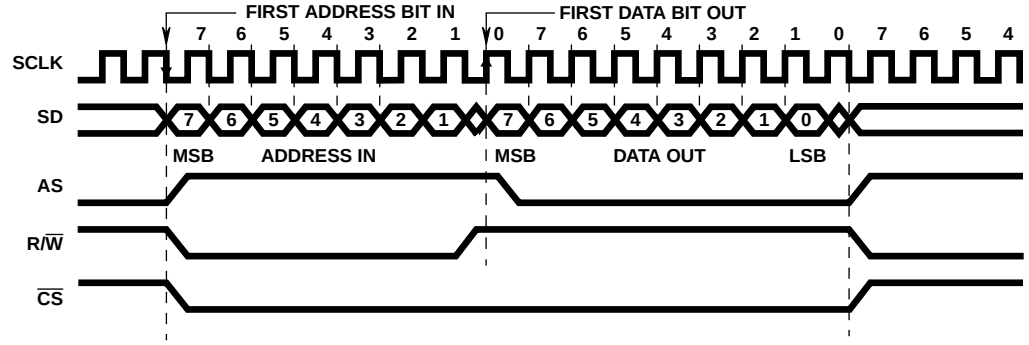
The signals necessary to accomplish the functions of this interface are:

CS: Chip select
AS: Address strobe
R/W: Read / Write strobe
SD: Serial Data.
SCLK: Serial Data Clock.

This HW/SW interface is required to configure the digital modem registers and performs all read and write operations to and from the digital modem. The serial control interface is used to serially write and read data to/from the digital

modem. This serial interface can operate up to a 10MHz rate or the maximum sampling clock rate of the PHY (whichever is lower). The sampling or master clock of the physical layer is designated as MCLK and must be running during programming. This interface is used to program and to read all internal registers. The first 8-bits always represent the address followed immediately by the 8 data bits for that register. The serial transfers are accomplished through the serial data signal (SD). SD is a bi-directional serial data bus. An Address Strobe (AS), Chip Select (CS), and Read/Write (R/W) are also required as handshake signals for this interface. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided to the PHY. The timing relationships of these signals are illustrated in Figure 2. AS is active high during the clocking of the address bits. R/W is high when data is to be read, and low when it is to be written. CS must be active (low) during the entire data transfer cycle. CS selects the device. The serial control interface operates asynchronously from the TX and RX interfaces and can accomplish data transfers independent of the activity at the other digital or analog interfaces. CS does not effect the TX or RX operation of the device; impacting only the operation of the Control interface.

CONTROL PORT READ TIMING



CONTROL PORT WRITE TIMING

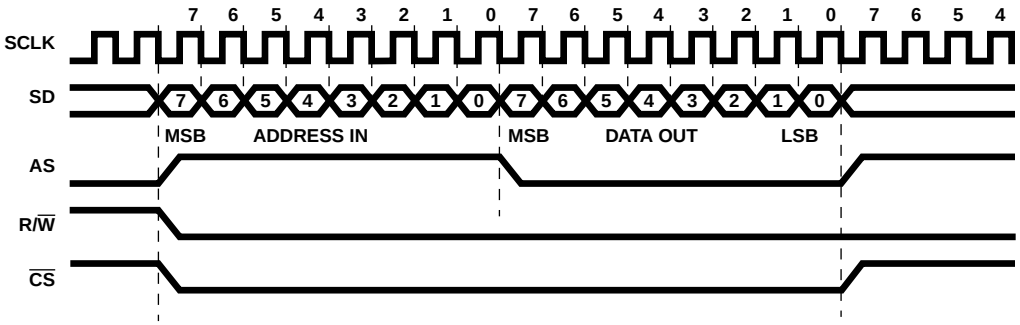


FIGURE 2. DIGITAL MODEM CONTROL INTERFACE

PHY Modem Configuration

The PHY modem has 57 internal registers that can be configured through the control interface. These registers are listed in Table 3 below. The table lists the configuration register number, a brief name describing the register, and the HEX address to access each of the registers. The type indicates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high & low bytes). Table 3 indicates the proper modem register configuration to implement the IEEE802.11 requirements as of the JULY 95 proposed draft.

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR0	MODEM CONFIG. REG #1	R/W	00	1E
CR1	MODEM CONFIG. REG #2	R/W	04	82
CR2	MODEM CONFIG. REG #3 ytd	R/W	08	23
CR3	MODEM CONFIG. REG #4	R/W	0C	03
CR4	INTERNAL TEST REGISTER #1	R/W	10	00
CR5	INTERNAL TEST REGISTER #2	R/W	14	00

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR6	INTERNAL TEST REGISTER #3	R	18	-
CR7	MODEM STATUS REGISTER #1	R	1C	-
CR8	MODEM STATUS REGISTER #2	R	20	-
CR9	I/O DEFINITION REGISTER	R/W	24	00
CR10	RSSI VALUE REGISTER	R	28	-
CR11	ADC_CAL_POS REGISTER	R/W	2C	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F
CR16	SCRAMBLE_TAP (RX & TX)	R/W	40	48
CR17	CCA_TIMER_TH	R/W	44	2C
CR18	CCA_CYCLE_TH	R/W	48	03
CR19	RSSI_TH	R/W	4C	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05
CR21	RX_SPREAD SEQUENCE (LOW)	R/W	54	B8
CR22	RX_SQ1_ACQ (HIGH) THRESHOLD	R/W	58	01
CR23	RX_SQ1_ACQ (LOW) THRESHOLD	R/W	5C	E8
CR24	RX_SQ1_ACQ (HIGH) READ	R	60	-
CR25	RX_SQ1_ACQ (LOW) READ	R	64	-
CR26	RX_SQ1_DATA (HIGH) THRESHOLD	R/W	68	00
CR27	RX_SQ1_DATA (LOW) THRESHOLD	R/W 6C	00	
CR28	RX_SQ1_DATA (HIGH) READ	R	70	-
CR29	RX_SQ1_DATA (LOW) READ	R	74	-
CR30	RX_SQ2_ACQ (HIGH) THRESHOLD	R/W	78	00
CR31	RX_SQ2_ACQ (LOW) THRESHOLD	R/W	7C	CA
CR32	RX_SQ2_ACQ (HIGH) READ	R	80	-
CR33	RX_SQ2_ACQ (LOW) READ	R	84	-
CR34	RX_SQ2_DATA (HIGH) THRESHOLD	R/W	88	FF
CR35	RX_SQ2_DATA (LOW) THRESHOLD	R/W	8C	FF
CR36	RX_SQ2_DATA (HIGH) READ	R	90	-
CR37	RX_SQ2_DATA (LOW) READ	R	94	-
CR38	RX_SQ_READ FULL PROTOCOL	R	98	-
CR39	RESERVED	W	9C	00
CR40	RESERVED	W	A0	00
CR41	UW_TIME_OUT_LENGTH	R/W	A4	90
CR42	SIG_DBPSK FIELD	R/W	A8	0A
CR43	SIG_DQPSK FIELD	R/W	AC	14

TABLE 3. CONFIGURATION AND CONTROL PHY REGISTER LIST (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	REGISTER DATA HEX
CR44	RX_SER_FIELD	R	B0	-
CR45	RX_LEN FIELD (HIGH)	R	B4	-
CR46	RX_LEN FIELD (LOW)	R	B8	-
CR47	RX_CRC16 (HIGH)	R	BC	-
CR48	RX_CRC16 (LOW)	R	C0	-
CR49	UW (HIGH)	R/W	C4	F3
CR50	UW (LOW)	R/W	C8	A0
CR51	TX_SER_F	R/W	CC	00
CR52	TX_LEN (HIGH)	R	D0	-
CR53	TX_LEN (LOW)	R	D4	-
CR54	TX_CRC16 (HIGH)	R	D8	-
CR55	TX_CRC16 (LOW)	R	DC	-
CR56	TX_PREM_LEN	R/W	E0	80

Synthesizer Interface

The following signals are required to accomplish the functions of this interface:

Synth_Data: Serial Synthesizer Data
Synth_Clk: Synthesizer Data Clock
Synth_LE: Synthesizer Load Enable

These signals are utilized to configure the RF frequency synthesizer. The synthesizer tunes the radio to the appropriate receive and transmit channels. Figure 3 illustrates the required timing to write the appropriate frequency to the PHY synthesizer.

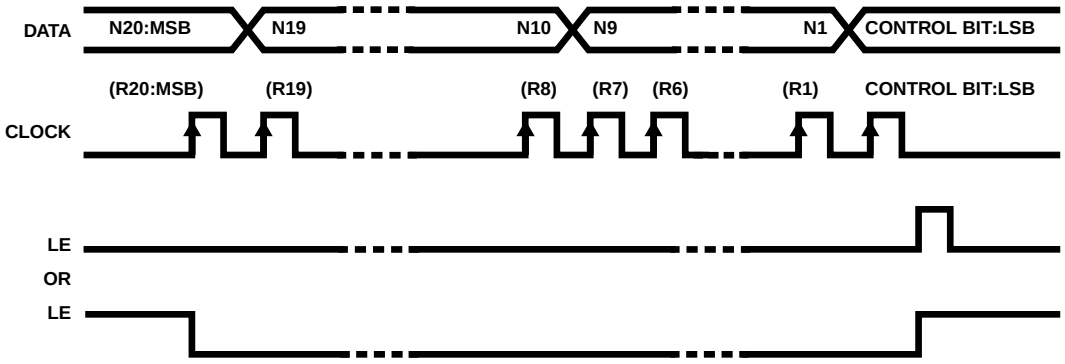


FIGURE 3. SYNTHESIZER SERIAL DATA INTERFACE

The following Data patterns are required to initialize the PHY synthesizer for IEEE802.11 operation. It should be noted that the register order is important with IF R first followed by IF N, RF R, and RF N. Also note that when powering up or coming out of Power Down Mode #2 (see page 10). The 4 registers should be written to twice. This is because the device RF and IF sections should be enabled before configuring the R and N pairs; and this effectively occurs if the values below are written twice in the IF R, IF N, RF R, RF N order. Also note that the OSC_START signal must follow any synthesizer programming cycle.

```
SYNTH_DATA   16,1801h    ;IF R Counter register
SYNTH_DATA   6, 60h       initialization.
SYNTH_DATA   16,4118h    ;IF N Counter register
SYNTH_DATA   6,04h        initialization.
SYNTH_DATA   16,1801h    ;RF R Counter register
SYNTH_DATA   6,68h        initialization.
```

The Harris_Freq_Table holds the 22-bit values for the synthesizer RF N Counter control register. Each entry is comprised of three bytes. Eight bits of the first byte is serially shifted out to the synthesizer (MSBit first), followed by 8-bits of the second byte (MSBit first), followed finally by the 6 MSBits of the third byte (MSBit first). The two LSBits of the third byte in each entry are ignored. The synthesizer configuration for each of the 12 IEEE802.11 channels is shown below.

```
Harris_Freq_Table   label byte
        db          02h, 011h, 04Ch     ;Channel 1
        db          02h, 011h, 09Ch     ;Channel 2
        db          02h, 011h, 0ECh     ;Channel 3
        db          02h, 018h, 03Ch     ;Channel 4
        db          02h, 018h, 08Ch     ;Channel 5
        db          02h, 018h, 0DCh     ;Channel 6
        db          02h, 019h, 02Ch     ;Channel 7
        db          02h, 019h, 07Ch     ;Channel 8
        db          02h, 019h, 0CCh     ;Channel 9
        db          02h, 020h, 01Ch     ;Channel 10
        db          02h, 020h, 06Ch     ;Channel 11
        db          02h, 021h, 0CCh     ;Channel 12
```

TX INTERFACE

The signals required for the control of the transmit functions of the radio are:

- TX_PE_BB: Transmit power enable for digital modem
- TXD: Transmit digital data
- TXCLK: Transmit data clock
- TX_RDY: Transmit data ready
- TX_PE: Transmit power enable for RF and IF sections
- PA_PE: Power amplifier transmit enable
- SEL 0,1: Selection of appropriate baseband LPF
- CCA: Clear channel assessment indicator from PHY

To initiate the transmit operation the MAC generates TX_PE. The Preamble and Header are then generated by the PHY. Finally, when cued, the MAC delivers the data packet to the PHY for transmission. The transmit data digital interface transfers the data that needs to be transmitted serially to the PHY. The data is modulated and transmitted as soon as it is received from the MAC. The serial digital data is input to the PHY through TXD using the falling edge of TXCLK to clock it in the PHY. TXCLK is an output from the PHY. A timing diagram of the transmit signal sequence is shown on Figure 4.

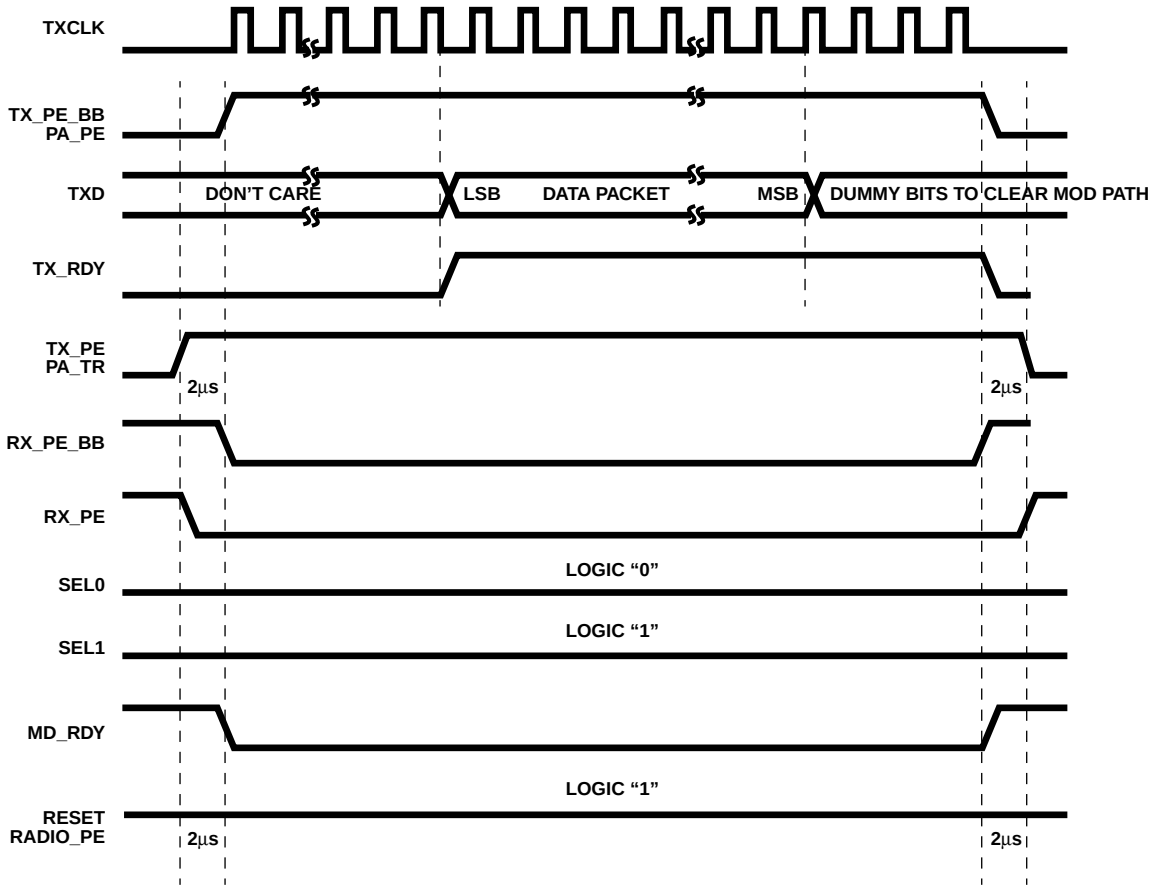


FIGURE 4. TRANSMIT TIMING DIAGRAM

The preamble and PHY header transmission is always at a 1Mbps (BPSK) data rate. The MAC header and data that follows can be either at 1Mbps (BPSK) or at 2Mbps (QPSK). To avoid rate switching within any single transmission between the MAC-PHY interface, the TXCLK will always be at the higher rate of 2Mbps. This implies that each of the BPSK symbols needs to be coming into the PHY twice. The MAC needs to send the same BPSK symbol twice at a rate of 2Mbps and this action will make it equivalent to the required BPSK symbol rate of 1Mbps. If QPSK data bits follow the PHY header, they will be sent from the MAC to the PHY only once at the 2Mbps rate.

The MAC initiates the transmit sequence by asserting TX_PE. Then TX_PE_BB envelopes the transmit data packet on TXD. The PHY responds by generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE_BB goes back to its inactive state indicating the end of the data packet. In addition Figure 4 illustrates the state of the PHY receive signals while transmitting as well as, the power enable, reset, and filter select proper signal states.

The PHY supports two possible data transfer scenarios, one where the preamble and header fields are generated within the PHY and one where the MAC generates the preamble and header fields. The scenario described herein assumes that the PHY generates the preamble and PHY header.

During this mode the PHY will immediately start transmitting the preamble and header as internally generated. Data available on TXD upon assertion of TX_PE_BB would be ignored. When the internally generated preamble and header are finished the PHY asserts TX_RDY. This signals the MAC to begin sending the data packet. TX_RDY assertion timing is programmable via Configuration Register (CR) 1. The timing diagram of this TX scenario, where the preamble and header are generated internal to the PHY, is illustrated on Figure 4.

One other signal that can be used to assist MAC transmit decisions as part of the TX interface is the Clear Channel Assessment (CCA) signal which is an output from the PHY. The CCA provides the indication that the channel is clear of energy and the transmission will not be subject to collisions. CCA can be monitored by the MAC to assist in deciding when to initiate transmissions. The CCA indication can be bypassed or ignored by the MAC without impacting any of the physical layer operations. The state of the CCA does not effect the transmit operation of the PHY. TX_PE and TX_PE_BB will always initiate the transmit state independent of the state of CCA. The CCA timing is not shown in the timing diagram of Figure 4 since it is an optional signal and does not influence the PHY transmit operations.

Signals TX_RDY, TX_PE_BB and TXCLK can be set individually, by programming CR9, as either active high or active low signals.

To avoid increasing throughput delays it is critical that the timing of TX_PE and RX_PE are as close to complementary of each other as possible.

When first attempting to transmit upon power-up, PA_PE must stay low for at least 10ms after RADIO_PE goes high.

RX INTERFACE

The signals that control the receive functions of the radio are:

- RX_PE_BB: Receive power enable for digital PHY modem
- MD_RDY: MAC data ready, enveloping the MAC data packet from the PHY
- RXD: Receive serial baseband data to the MAC
- RXCLK: Receive data clock to the MAC
- RX_PE: Receive power enable for the RF and IF section of the PHY radio
- SEL 0,1: Receive LPF frequency select

Timing diagram, Figure 5 illustrates the relationships between the various signals required to control the PHY during the receive operations.

The receive data interface of the PHY digital modem (RXD) serially outputs the demodulated data to the MAC. The data is output as soon as it is demodulated by the PHY. RX_PE and RX_PE_BB must be at their active state throughout the receive operation. When RX_PE, RX_PE_BB are inactive the PHY receive functions, including acquisition,. will be in a stand by mode. The timing relationships between RX_PE and RX_PE_BB, as well as, the state of the transmit signals, power enable signals, reset and filter select signal states are illustrated on Figure 5 for the receive operation during the reception of a single packet.

RXCLK is an output from the PHY and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the PHY and it envelopes the valid data on RXD. MD_RDY is programmable and is asserted either after the Start Frame Delimiter field has been detected or immediately after the CRC field of the header has been checked. MD_RDY is programmed through CR3, bit-7 to select when it will be asserted. The PHY may also be programmed to ignore error detection during the CRC check of the header fields. If programmed to ignore errors the device continues to output the demodulated data in its entirety regardless of the CRC check result. This option is programmed through CR2, bit-5.

The preamble and PHY header are always received at a 1Mbps (BPSK) data rate. The MAC header and data that follows can be either at 1 Mbps (BPSK) or at 2 Mbps (QPSK). To avoid rate switching within any single packet reception between the MAC-PHY interface, the RXCLK will always be at the higher rate of 2 Mbps. This implies that each of the BPSK symbols is coming out of the PHY twice. The PHY sends to the MAC the same BPSK symbol twice at a rate of 2 Mbps and this action will make it equivalent to the required BPSK symbol rate of 1Mbps. If QPSK data bits follow the PHY header, they will be sent to the MAC from the PHY only once at the 2 Mbps rate.

If rate switching is not an issue for the controller (MAC) then the HSP3824 can be configured to rate switch within the packet. The HSP3824 can automatically switch from BPSK to the QPSK rate at the appropriate time.

Note that RXCLK and RXD become active after acquisition, well before MD_RDY is asserted. MD_RDY returns to its inactive state under the following conditions:

- The number of data symbols, as defined by the length field in the protocol, has been received and output through RXD in its entirety (normal condition).
- PN tracking is lost during demodulation.
- RX_PE_BB is deactivated by the MAC.

MD_RDY can be configured through CR9, bit-6 to be active low, or active high.

To avoid increasing throughput delays it is critical that the timing of TX_PE and RX_PE are as close to complementary of each other as possible.

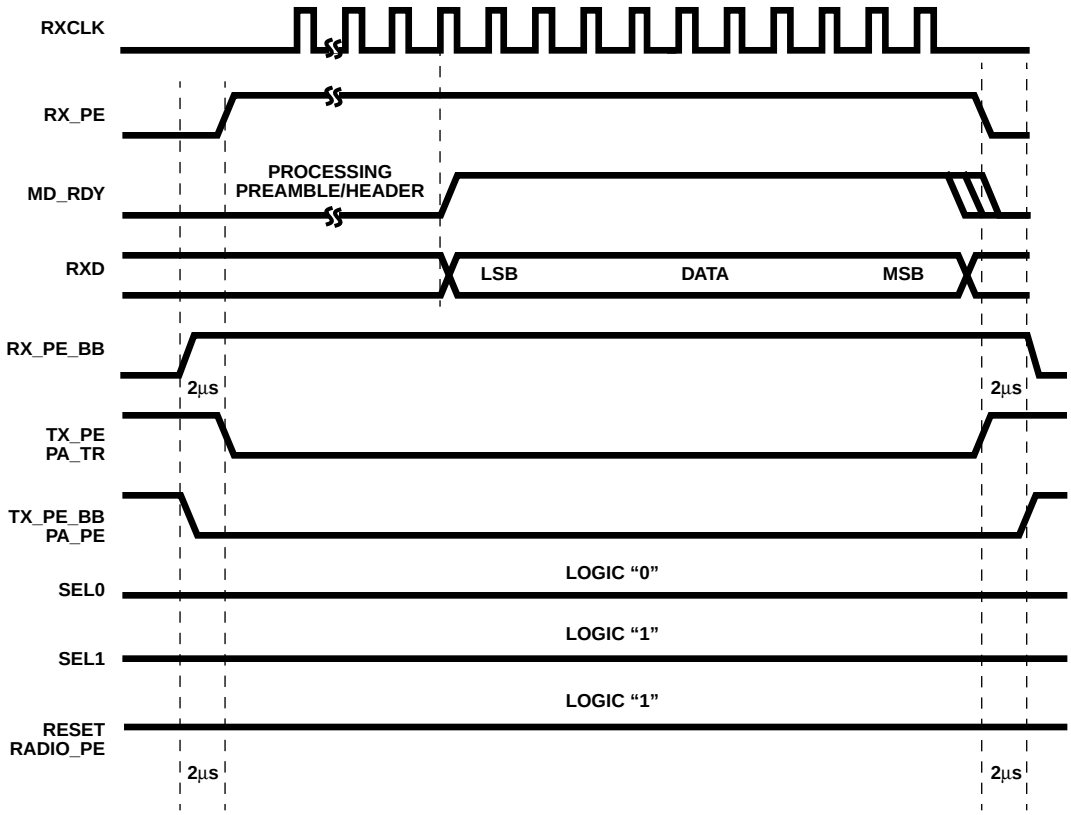


FIGURE 5. RECEIVE TIMING DIAGRAM

POWER DOWN MODES

The power consumption modes of the PHY are controlled by the following control signals:

- Receiver Power Enable (RX_PE & RX_PE_BB), which disable the radio receiver when inactive.
- Transmitter Power Enable (TX_PE & TX_PE_BB & PA_PE), which disable the radio transmitter when inactive.
- Reset (RESET), which puts the digital receiver in a sleep mode when it is asserted at least 2 MCLK's after RX_PE is set at its inactive state.
- RADIO_PE, which disables power regulators and all digital clocks to the PHY.
- In addition the radio RF synthesizer is programmable and can be set at a maximum power savings mode.

Utilizing the availability of the signals above there are three power savings modes defined:

- Power Down mode #1: During this mode the current consumption of the radio is estimated at 38mA. The radio can not receive or transmit when configured for this mode. When in this mode, it takes 25µs. to return the radio in its operational mode. when set in this mode, the PHY maintains its configuration data. There is no need to reprogram any of the radio register values. To activate Power Down mode #1 the following signals need to be set at the states shown below:

RX_PE: LOW
RX_PE_BB: LOW
TX_PE: LOW
TX_PE_BB: LOW
PA_PE: LOW
RESET: LOW
RADIO_PE: HIGH

- Power Down mode #2: During this mode the current consumption of the radio is estimated at 23mA. The radio cannot receive or transmit when configured for this mode. When in this mode, it takes 2ms. to return the radio in its operational mode. During this mode the synthesizer is programmed into its power savings mode. When set at this mode, the PHY maintains its configuration data. There is no need to reprogram any of the radio register values. However, the Synthesizer needs to be reprogrammed according to Synthesizer Interface Section on page 7.

To activate Power Down mode #2 the following signals need to be set as shown below:

RX_PE: LOW
RX_PE_BB: LOW
TX_PE: LOW
TX_PE_BB: LOW
PA_PE: LOW
RESET: LOW
RADIO_PE: HIGH

In addition the Synthesizer needs to be programmed via the synthesizer configuration interface as shown below:

```
SYNTH_DATA   16,1801h        ;IF R Counter register
SYNTH_DATA   6,0h             initialization.

SYNTH_DATA   16,0C118h       ;IF N Counter register
SYNTH_DATA   6,04h            initialization.

SYNTH_DATA   16,1801h        ;RF N Counter register
SYNTH_DATA   6,68h            initialization.

SYNTH_DATA   16,8211h        ;RF N Counter register
SYNTH_DATA   6,4Ch            initialization.
```

- Power Down mode #3: During this mode the current consumption of the radio is estimated at 1ma. The radio can not receive or transmit when configured for this mode. When set in this mode, it takes 15ms. to return the radio to its operational mode. When set in this mode, the PHY does not maintain its register configuration. All radio register values need to be reprogrammed to resume operation. This holds for both the PHY digital modem (HSP3824) and the PHY frequency synthesizer (HFA3925). To activate Power Down mode #3 the following signals need to be set as shown below:

RX_PE: Don't Care
RX_PE_BB: LOW
TX_PE: Don't Care
TX_PE_BB: LOW
PA_PE: LOW
RESET: LOW
RADIO_PE: LOW

When first attempting to transmit upon power-up, PA_PE must stay low for at least 10ms after RADIO_PE goes high.

Appendix A

Control Register Values for Single Antenna Acquisition

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR0	MODEM CONFIG. REG #1	R/W	00	3C	64
CR1	MODEM CONFIG. REG#2	R/W	04	00	00
CR2	MODEM CONFIG. REG#3	R/W	08	07	24
CR3	MODEM CONFIG. REG#4	R/W	0C	04	87
CR4	INTERNAL TEST REGISTER#1	R/W	10	00	00
CR5	INTERNAL TEST REGISTER #2	R/W	14	00	00
CR6	INTERNAL TEST REGISTER#3	R/W	18	00	00
CR7	MODEM STATUS REGISTER #1	R	1C	X	X
CR8	MODEM STATUS REGISTER #2	R	20	X	X
CR9	I/O DEFINITION REGISTER	R/W	24	00	00
CR10	RSSI VALUESTATUS REGISTER #2	R	28	X	X
CR11	ADC_CAL_POS REGISTER	R/W	2C	01	01
CR12	ADC_CAL_NEG REGISTER	R/W	30	FD	FD

Appendix A

Control Register Values for Single Antenna Acquisition (Continued)

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR13	TX_SPREAD SEQUENCE (HIGH)	R/W	34	05	05
CR14	TX_SPREAD SEQUENCE (LOW)	R/W	38	B8	B8
CR15	SCRAMBLE_SEED	R/W	3C	7F	7F
CR16	SCRAMBLE_TAP (RX & TX)	R/W	40	48	48
CR17	CCA_TIMER_TH	R/W	44	2C	2C
CR18	CCA_CYCLE_TH	R/W	48	03	03
CR19	RSSI_TH	R/W	4C	1E	1E
CR20	RX_SPREAD SEQUENCE (HIGH)	R/W	50	05	05
CR21	RX_SREAD SEQUENCE (LOW)	R/W	54	B8	B8
CR22	RX_SQ1_ IN_ACQ(HIGH) THRESHOLD	R/W	58	01	01
CR23	RX-SQ1_ IN_ACQ(LOW) THRESHOLD	R/W	5C	E8	E8
CR24	RX-SQ1_ OUT_ACQ(HIGH) READ	R	60	X	X
CR25	RX-SQ1_ OUT_ACQ (LOW) READ	R	64	X	X
CR26	RX-SQ1_ IN_DATA (HIGH) THRESHOLD	R/W	68	0F	0F
CR27	RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD	R/W	6C	FF	FF
CR28	RX-SQ1_ OUT_DATA (HIGH) READ	R	70	X	X
CR29	RX-SQ1_ OUT_DATA (LOW) READ	R	74	X	X
CR30	RX-SQ2_ IN_ACQ (HIGH) THRESHOLD	R/W	78	00	00
CR31	RX-SQ2- IN-ACQ (LOW) THRESHOLD	R/W	7C	CA	CA
CR32	RX-SQ2_ OUT_ACQ (HIGH) READ	R	80	X	X
CR33	RX-SQ2_ OUT_ACQ (LOW) READ	R	84	X	X
CR34	RX-SQ2_IN_DATA (HIGH) THRESHOLD	R/W	88	09	09
CR35	RX-SQ2_ IN_DATA (LOW) THRESHOLD	R/W	8C	80	80
CR36	RX-SQ2_ OUT_DATA (HIGH) READ	R	90	X	X
CR37	RX-SQ2_ OUT_DATA (LOW) READ	R	94	X	X
CR38	RX_SQ_READ; FULL PROTOCOL80211	R	98	X	X
CR39	RESERVED	W	9C	X	X
CR40	RESERVED	W	A0	X	X
CR41	UW_TIME_OUT_LENGTH	R/W	A4	90	90

Appendix A

Control Register Values for Single Antenna Acquisition (Continued)

REGISTER	NAME	TYPE	REGISTER ADDRESS IN HEX	QPSK	BPSK
CR42	SIG_DBPSK Field	R/W	A8	0A	0A
CR43	SIG_DQPSK Field	R/W	AC	14	14
CR44	RX_SER_Field	R	B0	X	X
CR45	RX_LEN Field (HIGH)	R	B4	X	X
CR46	RX_LEN Field (LOW)	R	B8	X	X
CR47	RX_CRC16 (HIGH)	R	BC	X	X
CR48	RX_CRC16 (LOW)	R	C0	X	X
CR49	UW -(HIGH)	R/W	C4	F3	F3
CR50	UW _(LOW)	R/W	C8	A0	A0
CR51	TX_SER_F	R/W	CC	00	00
CR52	TX_LEN (HIGH)	R	D0	X	X
CR53	TX_LEN(LOW)	R	D4	X	X
CR54	TX_CRC16 (HIGH)	R	D8	X	X
CR55	TX_CRC16 (LOW)	R	DC	X	X
CR56	TX_PREM_LEN	R/W	E0	80	80

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