Data Conversion Products



■ MICRO NETWORKS

Index by Part Number

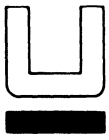
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Bold Copy = New Products

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MICRO NETWORKS

Data Conversion Products Catalog

Mission Statement

Our mission is to be an acknowledged leader in supplying innovative analog signal processing microcircuits whose high performance and quality uniquely meet the needs of our customers.

We will achieve this by serving customers in a superior manner with:

- leading-edge products
- strong technical support
- advanced manufacturing techniques
- on-time delivery

By matching our capabilities and customers' needs, we will best achieve our profit-growth objectives.

We recognize that loyal, productive employees are our most important resource. Therefore, we will provide a safe, clean working environment and foster open communications, mutual respect and trust at all levels. We will encourage participation of all employees and recognize and reward their efforts in meeting our goals and our customers' expectations. We will provide equal opportunity in employment and promote employee development and advancement.

Successful innovation and the willingness to take risks are key to achieving individual and company growth.

Our relationships with customers, suppliers, community and government will be characterized by mutual understanding and trust. We are committed to conducting our business in an ethical and responsible manner.

History

Shortly after its creation in 1969, Micro Networks earned the reputation as the innovative leader in the design and manufacturing of high reliabiity, dual-in-line packaged, data-acquisition and conversion products for military/aerospace, industrial and commercial applications. As recent product introductions and technical innovations indicate, we still merit that reputation earned 23 years ago. What follows is a historical summary of the unique technical and practical achievements in Micro Networks continued advancement of data conversion technology.

1969—Micro Networks is created to design, develop, manufacture and market highly reliable, hybrid, DIP, data-acquisition and conversion products for military/aerospace, industrial and commercial applications.

1970—Micro Networks introduces the world's first thin-film hybrid data converter (MN302, 8-bit D/A) pioneering the active laser trimming of thin-film resistor networks.

1971—The first complete, voltage-output, 8-bit (MN307), 10-bit (MN310) and 12-bit (MN312) D/A converters are introduced. These are the first such devices to incorporate internal references and current-to-voltage output amplifiers.

1973—The first successive approximation A/D converter in a DIP, the 8-bit MN502, is introduced, and MN3850 and MN3860 become the first 12-bit D/A's to guarantee true 12-bit performance over the full −55°C to +125°C temperature range.

1974—Micro Networks introduced the first 12-bit succcessive approximation A/D converters in DIP's. Designated MN5200 and MN5210, they become the only 12-bit A/D's for the next 5 years to guarantee ±½LSB linearity and no missing codes from −55°C to +125°C. These units become the most popular 12-bit A/D's for military/aerospace applications and eventually become the first hybrid A/D's to have a slash sheet (38510/120).

1976—The first, complete, single package data acquisition system (DAS), MN7100 (8 bits, 8 channels), is introduced.

1977—The first, ultra low-power, 8-bit (MN5065, 53mW), 12-bit (MN5250, 56mW) and 14-bit (MN5260, 215mW) DIP-packaged A/D's are introduced.

1978—MN5500 is the first 12-bit A/D to incorporate a complete microprocessor interface (chip enable, chip select, address decode, R/W, 3-state, etc.); while MN5280 is the first 16-bit, successive approximation A/D in a DIP. In the same year, MN7140 is the first complete, 12-bit DAS to operate from −55°C to +125°C, and MN5410 is the first 12-bit, autoranging (16-bit dynamic range) A/D.

1979—Micro Networks refines thin-film processing and assembly techniques and wins the race to introduce the first 12-bit A/D capable of operating at 200°C in down-hole, oil-exploration applications.

1980—Micro Networks wins another race introducing the first 12-bit A/D in a DIP to convert in 1 microsecond. For years, MN5245 is the only DIP A/D to use low-resolution, monolithic flash converters in a two-step (subranging) conversion approach.

1982—MN5290 and MN5291 16-bit A/D's are the first A/D's to guarantee better than 12-bit performance from −55°C to +125°C and the first 16-bit DIP A/D's that can be successfully screened to MIL-STD-883.

1983—MN574A is introduced as the first commercially available hybrid A/D converter to employ gate-array technology. MN379 is the first track-hold (T/H) amplifier to directly drive ultra high-speed 8 and 9-bit flash converters.

1985—Micro Networks introduces the MN5420 Hardware Autoranging A/D. This industry-first 12-bit A/D automatically senses the amplitude of its input signal and selects one of nine input gain ranges to optimize the accuracy of its 12-bit 1μsec A/D. The 16-bit floating-point output (mantissa and exponent) covers a 20-bit dynamic range.

1986—Micro Networks revamps its process and quality-control documentation; adds 17,000 sq. ft. of new clean-room facility; undergoes a D.E.S.C. audit; and receives MIL-STD-1772 Certification. After having used FFT testing as an in-house development tool since 1979, we introduce the first products in the MN6000 Series of high-speed, wide-bandwidth, FFT-tested, sampling A/D converters.

1987—MN5295 becomes the industry's first high-speed (17μsec) 16-bit A/D to meet full military requirements (−55°C to +125°C operation, MIL-STD-883 screening).

1988—Micro Networks submits its qualification samples; receives MIL-STD-1772 qualification; and is added to the Hybrid Microcircuits Qualified Manufacturers List.

1989—Micro Networks established a modem link with the Defense Electronic System Center (DESC) to support the development of Standardized Military Drawings (DESC SMD). Micro Networks obtained listings for many standard device types (including MN5200/5210 Series, MN5290/5295, etc.)

1990—Micro Networks introduces its first Flash A/D Converter the MN5903 (6-bit, 75MHz). Additionally, the MN6400 is the first in a series of true 16-bit self-calibrating Sampling A/D converters to be announced. Custom hybrids become a key product line for Micro Networks.

1991—MN5902 (8-bit, 20MHz) and MN5906 (6-bit, 50MHz) are Micro Networks first CMOS monolithic Flash A/D converters to be announced. These devices provide high-speed performance in combination with the low-power characteristics of their CMOS design. The MN6400 Series of self-calibrating devices are expanded with the MN6405 and MN6450. The MN6900 (8-bit, 500MHz) and MN6901 (8-bit, 250MHz) Sampling A/D converters are also released for application in ultra-high-speed digitizing systems.

1992—Micro Networks introduces the MN4000, a performance upgrade to industry-standard "0010" and "0025" type T/H amplifiers. The MN4000 offers an excellent combination of high-resolution and high-speed. Additionally, the MN7450 is Micro Networks first 8-channel, 16-bit, 50kHz, single-package DAS. More to come!

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Still Available

The following is a list of older Micro Networks converter products. Although our newer converters provide higher performance at lower cost, we realize that is is often not economical for you, the customer, to redesign existing systems or products. Consequently, we reiterte our commitment to continue to supply these devices for as long as possible; however, we are compelled to point out that component unavailability and/or manufacturing practicalities may, on occasion, make it impossible for us to keep that commitment. Please contact our Sales/Marketing Department for information on price and delivery, lead times, minimum order quantities, and recommended alternatives for new designs.

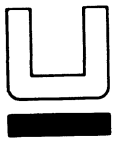
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MN301
MN302
MN303
MN306
MN308
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MN312
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MN333
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MN2006
MN2120
MN3010
MN3013
MN3015
MN3100
MN3300
MN3310
MN3311
MN3660
MN5110
MN5111
MN5610
MN5611
MN5612
MN5613
MN5614
MN5615
MN5616
MN5700
MN7100
MN1900
MN375
MN5280
MN5282
MN6231
MN6232

Discontinued

Unfortunately, there are some devices that, because of obsolete or unavailable materials or discontinued manufacturing processes, we are unable to supply. Please contact our Marketing/Applications Department for advice regarding alternate device types.

MN0405
MN0605
MN0805
MN350
MN351
MN352
MN5260
MN5815
DAC80-CCD-I
DAC80-CCD-V
DAC85-CCD-I
DAC85-CCD-V
MN5820
MN5420
MN565A
MN542
DAC812
MNHT-0010
MNHT-0025
MNHT-378
MNSA-1020
MNSA-1040
MNSA-1205
MNSA-1210
MN5900
MN5901

Quality Control and High Reliability Processing



MICRO NETWORKS



MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

Quality Control and High Reliability Screening

Micro Networks is MIL-STD-1772 Certified and Qualified

Micro Networks has long been recognized as a leading supplier of thin and thick-film, hybrid, data-acquisition and conversion products for demanding military and aerospace applications. In addition to utilizing proven hybrid assembly techniques, many new products from Micro Networks are designed and implemented using state-of-the-art monolithic design and fabrication technologies.

Our products are presently employed in a wide variety of applications ranging from missile-guidance and satellite systems to critical ground support and test equipment. Our modern facility in Worcester, Massachusetts was designed and built for the production of thin and thick-film hybrid and monolithic microcircuits and is capable of producing in excess of one-half million devices annually.

Micro Networks imposes tight quality control on all aspects of design and manufacturing. Our Quality Control Department oversees all aspects of high reliability product processing and screening. The Quality Assurance Department sets the material standards, specifies manufacturing flow, controls processing screening standards, maintains lot traceability, and continuously monitors all parameters critical to product quality.

In order to enhance Micro Networks position as an industry leader in the design and manufacture of high-reliability hybrid and monolithic microcircuits, Micro Networks has implemented a Total Quality Management Program. This program has been successful in fostering a company-wide culture of quality consciousness that ensures continuous improvement in the quality of products and services delivered to our customers. We believe that by following the precepts of TQM, we can fully satisfy the quality and customer-service expectations of today's marketplace.

An effective Statistical Process Control (SPC) program plays an important role in any TQM process. Selecting the correct processes to monitor, determining the capabilities of those critical processes, monitoring them, and implementing corrective actions quickly and effectively are vital to resolving problems, improving quality, and reducing costs.

Our Total Quality Management program here at Micro Networks provides our operators and inspectors with contemporary SPC training programs allowing us to reduce process variability thereby improving overall quality and delivery performance.

MIL-STD-1772 QUALIFIED MANUFACTURERS LISTED — Micro Networks is fully certified and qualified to MIL-STD-1772, and is listed in the Qualified Manufacturers List (QML) maintained by the Defense Electronics Supply Center (DESC). Only those products that are manufactured, assembled, and tested in acordance with MIL-H-38534 (Hybrid Microcircuits, General Specification for) in a QML-listed facility may bear the "CH" certification mark for non-SMD-controlled hybrid microcircuits or the "QML" certification mark for SMD-controlled (Standard Military Drawing) devices.

STANDARDIZED MILITARY DRAWINGS (SMD) — Our MIL-STD-1772 qualification enables us to participate in DESC's Standardized Military Drawing program. This program was conceived to eliminate redundant documentation for commonly used standard devices in military applications. This program significantly reduces the need for unique OEM-produced Source/Specification Control Drawings (commonly referred to as SCD's) and has become a preferred method of procurement for buyers of military hybrid and monolithic integrated circuits. SMD's are described in the DOD-STD-100 document. This program also supports the Department of Defense's parts-control program in acordance with MIL-STD-965.

Micro Networks has taken an active roll in supporting the DESC SMD program by establishing in-house word-processing capability for SMD creation, and maintaining a dedicated PC-Modem connection with DESC for the transmitting and receiving of DESC SMD documentation. Micro Networks welcomes our customers to join us in sponsoring the creation of new SMD's for our standard catalog items.

Many of Micro Networks standard products families are available as either compliant MIL-H-38534 or as DESC SMD devices. See Table 1 for listing of devices currently (at the time of this printing) available as compliant MIL-H-38534 devices. See Table 2 for those devices currently (at the time of this printing) available in accordance with a DESC SMD.

Please contact your local Sales Representative or the factory for current information regarding availability of either compliant or SMD devices or for assistance in creating new SMDs for Micro Networks products.

NON-JAN MULTICHIP AND OTHER NON-JAN MICROCIRCUITS — Custom monolithics, non-JAN multichip and all other non-JAN microcircuits except hybrids described or implied to be compliant with Method 5004 and Method 5005 of MIL-STD-883 must meet the requirements of paragraph 1.2.1.b of MIL-STD-883. MIL-STD-1772 QML listed manufacturers such as Micro Networks already meet most of these requirements: as they are very similar. By exercising proper control over the source of chip suppliers, Micro Networks is able to offer compliant monolithic and multichip microcircuits. These compliant devices have a quality factor (utilized for reliability calculations per MIL-HDBK-217) two and a half times better than non-compliant devices.

PREDICTING DEVICE RELIABILITY — For the purpose of predicting the reliability of electronic equipment and systems, the military has developed quality factors for component parts. While many factors are involved in determining these theoretical failure rates, only the quality factor Π_Q and the application-environment factor Π_E appear in all models. All system failure rates are directly dependant on these factors.

MIL-HDBK-217 governs the procedures for determining theoretical failure rates and quality factors for hybrid integrated microcircuits used in military electronic systems. Table 5.1.2.9-6 of the handbook specifies that hybrid

circuits supplied to the Class-B requirements of MIL-STD-883 by fully qualified, QML-listed manufacturers must have a designated Π_Q of 0.5, as compared to a Π_Q of 1.0 for devices tested in accordance with Method 5008 of MIL-STD-883, but from a non-QML-listed supplier. In other words, a compliant device supplied by Micro Networks has twice the theoretical reliability of a similar device from a non-QML-listed supplier. Furthermore, compliant Class-B devices are rated forty times more reliable than products from non-compliant suppliers, subjected to unscreened devices.

ENVIRONMENTAL STRESS SCREENING — Micro Networks produces products that represent the end result of all the very best disciplines: innovative designs, strict adherence to established design rules, superior materials and components, tightly monitored and controlled processes, stringent test procedures, and effective corrective measures that permanently fix problems. All of these desciplines are essential to the manufacture of a superior-quality, highly-reliable product.

Our customers are producing complex, high-performance equipment that must operate in unusually demanding environments and under uncommonly stressful conditions. These programs require a high degree of assurance that the products designed into these systems will meet the expected level of reliability and performance. For these programs that do not require MIL-H-38534 compliant devices or for non-military applications where enhanced reliability is required, Micro Networks offers devices which are Environmentally Stressed Screened.

These Environmentally Stressed Screened devices are screened to the test methods of MIL-STD-883, Method 5008. However, these devices should not be confused with compliant MIL-H-38534 devices. Differences between Environmentally Stressed Screened and Compliant devices lie in the additonal requirements for full compliance with MIL-H-38534 requirements: Element Evaluation, In Process Controls and Screening and Quality Conformance Inspection.

Environmentally Stressed Screened devices offer designers a cost-effective solution to their particular system requirements.

CAPABILITIES — Micro Networks, in support of our military business, maintains in-house test capability for performing the following tests:

Hermetic Seal	Thermal Shock
Stabilization Bake	Solderability
Burn-in/Life Test	Bond Strength
Temperature Cycle	Internal Visual
Constant Acceleration	X-Ray
Marking Permanence	XRF
PIND	Die Shear

When required, additional testing is performed at DESC-approved test laboratories.

Compliant MIL-H-38534 Device Families		Future Compliant (1)
ADC87	MN3860	MN374
DACHK	MN5100/5101	MN3003 Series
DAC88	MN5120/30/40 Series	MN5160
MN0300A	MN5150	MN5295/96
MN343/344	MN5200 Series	MN5249
MN346/347	MN5210 Series	MN6249
MN370/371	MN5245/5246	MN6290/6291
MN373	MN5250 Series	MN6295/6296
MN376	MN5290	MN6405
MN379	MN5825	MN6450
MN2020	MN6400	MN6500
MN3000 Series	MN7120	MN6774
MN3008/3009	MN7130	MN7140/43
MN3014	MN7145/46/47 Series	MN7208
MN3020	MN7150-8	MN7216
MN3040	MN7150-16	MN7450
MN3290-V Series		MN7451
MN3348		
MN3349		

Table 1. Compliant MIL-H-38534 Device Families

NOTES: 1. Contact factory for availability of future compliant products.

Sampling A/D Converters

Part No.	DESC 5962-	Page Number
MN6227T/B	8998401HXX*	5-41
MN6228T/B	8998402HXX*	5-41
MN6295T/B	8998301HXX*	5-71
MN6296T/B	8998302HXX*	5-71
MN6400T/B	9177001HXX*	5-79

A/D Converters

MN5200H/B	8958301YX	6-77
MN5201H/B	8958303YX	6-77
MN5202H/B	8958305YX	6-77
MN5203H/B	8958302YX	6-77
MN5204H/B	8958304YX	6-77
MN5205H/B	8958306YX	6-77
MN5206H/B	8958307YX	6-77
MN5210H/B	8958401YX	6-85
MN5211H/B	8958403YX	6-85
MN5212H/B	8958405YX	6-85
MN5213H/B	8958402YX	6-85
MN5214H/B	8958404YX	6-85
MN5215H/B	8958406YX	6-85
MN5216H/B	8958407YX	6-85
MN5245H/B	8959501XX	6-99
MN5245FH/B	8959501YX	6-99
MN5245AH/B	8959502XX	6-99
MN5245AFH/B	8959502YX	6-99
MN5246H/B	8959503XX	6-99
MN5246FH/B	8959503YX	6-99
MN5246AH/B	8959504XX	6-99
MN5246AFH/B	8959504YX	6-99
MN5290H/B	8956301HXX	6-127
MN5291H/B	8956302HXX	6-127
MN5295H/B	8956901HXX	6-135
MN574AT/B	8512702XX**	6-23
ADC87H/B	8850802XX	6-17

D/A Converters

Part No.	DESC 5962-	Page Number
MN3008H/B	8768801XX	7-39
MN3009H/B	8768802XX	7-39
MN3020H/B	8971801XX	7-43
MN370H/B	8981401XX*	7-29
MN371H/B	8981402XX*	7-29
MN3860H/B	9057001HXX	7-65
DAC87H/B	8300301JC**	7-21
MN3290T/B-V	8953103HYX	7-51
MN3291T/B-V	8953104HYX	7-51
MN3292T/B-V	8953102HYX	7-51

T/H Amplifiers

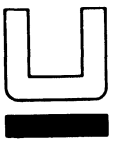
MN346H/B	8994001HXX	8-13
MN376H/B	9073001HXX*	8-31
MN4000H/B	9085601HXX*	8-53

Data Acquisition

MN7130H/B	9057101HXX*	9-9
MN7140H/B	9079701HXX	9-15

*Release Pending
**Pursuing Listing on Existing SMD
If the device type you're interested in is not listed, please consult factory.

Table 2. DESC Standardized Military Drawings (SMD) Cross Reference.



MICRO NETWORKS



MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

Custom Capabilities

Custom Hybrid Microcircuits

Capabilities

EXPERTISE THROUGH EXPERIENCE

- Years of military/high reliability experience
- Micro Networks fastest-growing line
- Specialty: analog and analog/digital interface
- Thick-film, thin-film, chip-and-wire expertise
- Proven program-management techniques

CUSTOMS DEVELOPED AT MICRO NETWORKS

- Highpass, Lowpass and Bandpass Filters
- High-Speed Line Driver
- Geometric ADC with Autoranging
- Precision Voltage Regulators
- Precision Signal-Conditioning Circuits
- Custom ADCs and DACs
- Data-Acquisition Circuits
- Programmable-Gain Amplifiers
- Motor-Drive Hybrids

LIBRARY OF BUILDING BLOCK CHIPS

- Flash A/D Converters
- D/A Converters
- Autocalibrating A/D Converters
- Error-Correction ASICs
- T/H Amplifier Front Ends
- High-Precision NiCr Resistors

Partial Program List

AIRCRAFT	SHIPBOARD	MISSILE
A-6F	MK 46	AMRAAM
B-1	MK 50	PATRIOT
F-1	BSY I	ROLAND
F-14	BSY II	CROTALE
F-15	RAPLOC	PENGUIN
F-16	SQS56	MAVERICK
F-18	SQQ89	HARM

Custom Hybrid Capabilities

Custom hybrid circuits represent Micro Networks' fastest-growing product line. These circuits are a natural outgrowth of the company's many years of experience in designing, manufacturing, and testing precision, hybrid-based signal-processing circuits. The rich diversity of technologies and materials available for both passive and active circuit elements makes custom hybrid circuits the solution of choice in the most demanding applications.

Hybrid circuits have long been the preferred circuit solution in military/aerospace environments, whose state-of-the art performance requirements preclude the use of monolithic integrated circuits, and whose limited space mandates the smallest possible physical volume. Custom hybrid circuits from Micro Networks are designed into aircraft (F-14, F-16, F-18, A-6F); shipboard systems (BSY1, BSY2, MK46, MK50, RAPLOC, SQ56, SQQ89); and missiles (AMRAAM, Patriot), to name just a few applications.

Micro Networks' success in custom hybrid circuits is inextricably linked to the company's commitment to quality (see the section entitled, Quality Control and High-Reliability Screening). Quality consciousness pervades all departments at Micro Networks. From order entry to the shipping dock, quality is a philosophy of life, not something that's tested-in. Micro Networks was one of the first manufacturers certified and qualified to DESC's MIL-STD-1772 standard for hybrid facilities. From the beginning, Micro Networks has specialized in the production of microcircuits that satisfy the rigorous requirements of MIL-STD-883 and MIL-H-38534.

Micro Networks' philosophy in developing and producing custom hybrid circuits is to successfully serve our customers' needs through a combination of:

- Commitment
- Integrity
- Competence
- Qualified facilities
- Qualified and dedicated personnel

ENGINEERING RESOURCES — Micro Networks' staff of design engineers possesses a wealth of multi-disciplinary skills. Their many years of experience in designing analog/digital interface circuits provides broad-based proficiency in analog, digital, and mixed-signal electronics. In the development of a custom hybrid, MN's engineering staff works closely with the customer, in one of several ways:

Build-to-print. This is the one-for-one translation of an existing circuit design to hybrid form, retaining all component types, values, and tolerances appearing in the original schematic diagram.

Black box. Given a circuit's input/output specifications, MN's engineers can design an appropriate circuit and translate it to optimal hybrid form.

"Grey box". Based on an existing schematic diagram and input/output specifications, MN's engineers can often effect major or minor modifications that make the circuit more suitable for hybrid fabrication.

"Grey box" design demands a great deal of engineering expertise. Given the constraints on hybrid-circuit designs--component availability, value limits and tolerances, and other factors--it is often possible to modify an existing circuit design to enhance the resulting hybrid circuit's manufacturability, cost- effectiveness, and performance.

In black box and "grey box" design endeavors, Micro Networks' engineers have an extensive library of building-block circuit functions to draw upon. Available circuit blocks previously developed for both standard and custom products include flash A/D converters, D/A converters, error-correction ASICs, and track/hold amplifier stages.

Micro Networks' engineering department has a full range of design, engineering, and simulation tools to facilitate rapid and accurate custom-hybrid design. These tools include a computer-based hybrid layout system, SPICE software for circuit simulation, and thermal-modeling software. For quick sample turnaround, the engineering department has a dedicated prototype assembly area. For those cases where it is advantageous to design an ASIC chip for use in a custom hybrid, Sun workstations and Cadence CAD software provide the capability to design both CMOS and bipolar IC chips.

Custom hybrid circuits successfully developed and produced by Micro Networks include: data-acquisition systems; A/D and D/A converters; track/hold amplifiers; precision switched-gain amplifiers; lowpass, bandpass, and highpass filters; low-noise amplifiers; low-dropout regulators; multichannel amplifiers; transceivers; line drivers; smart Darlington drivers; actuator drivers; phase-locked-loop circuits; a 20-bit dynamic-range A/D converter, and a host of others.

This extraordinary diversity of circuit functions, precision and speed requirements, analog/digital interface environments, and packaging solutions has endowed Micro Networks' engineering staff with an unparalleled wealth of experience, and more-than-ample expertise to undertake any conceivable custom- hybrid project.

TECHNOLOGY AND FACILITIES — One of the major advantages of hybrid circuits is the ability to combine diverse materials, components, and technologies that would be impractical or impossible to incorporate in monolithic ICs. As an example, Micro Networks employs both thick-film and thin-film processes in the design of its resistor networks and single-layer and multilayer substrates. Thick-film resistors

provide maximum economy in most circuit applications; in applications demanding extremely tight tolerances, resistor-to-resistor matching, or precise temperature tracking, nickel-chromium thin-film resistors provide the ultimate in electrical characteristics. Both sputtering and evaporation systems are available for depositing thin-film conductors and resistors.

Manual or automatic laser-trim stations provide either passive (trim to resistor value) or active (trim for circuit performance) adjustments for resistor networks and assembled hybrids. In mounting components on substrates, Micro Networks uses conductive or non- conductive epoxy, eutectic, or solder bonding techniques. For making circuit connections, manual and fully automatic wire-bonding stations accommodate gold and aluminum wires of a wide range of diameters. Packaging options presently available from Micro Networks include: DIPs, SIPs, LCCs, metal bathtubs, TO-5, and TO-3.

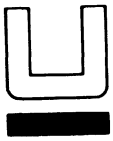
Micro Networks' test department and test equipment are ideally geared to the production testing of custom hybrid circuits. Several LTX and Eagle automatic test systems provide rapid, economical, and repeatable tests of analog, digital, and mixed-signal functions. A team of experienced test programmers ensures rapid turnaround for new designs. In addition to these automatic production test systems, Micro Networks' test- engineering department is adept at designing specialized test systems for low-volume projects or for circuits that require special testing techniques.

PROGRAM MANAGEMENT — It is Micro Networks' standard procedure to appoint an experienced program manager to direct the development efforts for new custom hybrid projects. The duties of the program manager include:

- Provide a single communications interface between the customer and Micro Networks;
- Participate in design reviews;
- Coordinate schedule reviews and manage program meetings;
- Develop status reports and action plans;
- Develop and maintain computer-based PERT and Gantt charts for use as management and communication tools;
- Serve as the customer's advocate to Micro Networks' management.

The unique combination of engineering expertise, hybrid-technology mastery, and proven program-management excellence makes Micro Networks eminently qualified to meet the most demanding custom-hybrid challenges.

Tutorial – Understanding Data Converters



MICRO NETWORKS



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Understanding Data Converters

INTRODUCTION

Analog to Digital and Digital to Analog Converters are collectively referred to as Data Converters, and their usage has paralleled the availability of digital computing power increasing enormously since the early fifties. Analog to digital (A/D) and digital to analog (D/A) converters are the interface between the physical parameters of the real world, which are analog, and the digital world of computation and control systems. Data converters find applications in widely diverse fields ranging from the digital multimeter on your bench to sophisticated inertial guidance systems capable of targeting a missile to within thousands of feet after thousands of miles of flight. Other typical applications include high efficiency, emission reducing electronic fuel systems, computer-based energy management systems, and the industrial and process control systems that refine our fuel, prepare and package our food, and process the plethora of chemicals required by our complex society.

The present situation involving data converters is very complex. He (she) is a rare engineer who has not had at least a casual acquaintance with data converters and an equally rare one who can claim to clearly understand them. This is partly due to the fact that converters are such rapidly-evolving (and sometimes confusing) components. They are made in high resolutions and accuracies by only a few manufacturers. Data sheets range from excellent to abominable. Specification parameters are sometimes confusing and not well standardized. Packaging ranges from modules and printed circuit boards to standard Dual-in-Line packages, and contents range from complete functions to various "bits and pieces" that require the addition of other components entailing perhaps more importantly, the consideration of additional error sources.

In this tutorial section we hope to share with you our hundred odd years of cumulative data converter experience and give you the tools that will enable you to compare different design approaches and manufacturers so you will be able to select the most cost effective components and approaches for your specific data converter application.

At Micro Networks, our philosophy is that all converter specifications should be defined from a "black box" (equivalent circuit) point of view. An input/output transfer function should be defined, clearly described, and bounded by *maximum* error specifications, both at room temperature and over the full operating temperature range. Individual errors should be combined to give overall error specifications whenever the individual specifications are not of any pertinence, and specification parameters should be clearly defined.

As you use this catalog, you will see this philosophy reflected in our data sheets. You will find more accuracy specifications, clear definitions, and generously populated maximum columns. But now onto the meat—how to understand and work with data converters and their specification sheets.

DATA CONVERTER TRANSFER FUNCTIONS

Let's begin at the beginning, with the data converter input/output transfer functions. Figure 1 shows the ideal digital input/analog output transfer function of a 3 bit, 0 to + 10V output range, binary coded digital to analog converter (D/A).

Figure 2 shows the ideal digital input/analog output transfer function of a 3 bit, ± 10V output range, offset binary coded D/A converter.

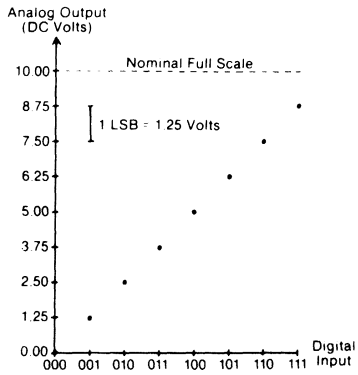


Figure 1. Digital input/analog output transfer function of an ideal, 3-bit, 0 to + 10V output range, binary coded D/A converter.

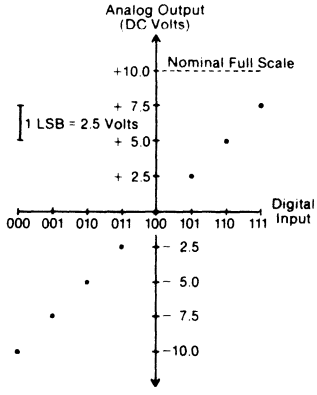


Figure 2. Digital input/analog output transfer function of an ideal, 3 bit, ± 10V output range, offset binary coded D/A converter.

The transfer functions are discontinuous with a unique one-to-one correspondence between digital input codes and analog output voltages. For each input code there is one and only one output level. The number of different input codes is equal to 2^n where n is equal to the number of digital input bits. A 3 bit D/A has $2^3 = 8$ different input codes; an 8 bit D/A

has $2^8 = 256$ different input codes; a 12 bit D/A has $2^{12} = 4096$ input codes; etc... The 3 bit D/A of Figure 2 operates as follows:

For a Digital Input of			The Analog Output Voltage Is
MSB	Bit 2	LSB	
0	0	0	− 10.0V
0	0	1	− 7.5V
0	1	0	− 5.0V
0	1	1	− 2.5V
1	0	0	0.0V
1	0	1	+ 2.5V
1	1	0	+ 5.0V
1	1	1	+ 7.5V

The analog output of a D/A converter changes in discrete analog steps with changes in digital input. The smallest *change* in output level that can be generated by a D/A converter,i.e., the change from one analog output level to an adjacent level, is the value assigned to the converter's Least Significant Bit (LSB). The smallest change in output level a D/A can produce is a measure of its resolving power; it is its *resolution*. Resolution is also expressed in bits. In this example we have a 3 bit converter; its resolution is 3 bits. Resolution can also be expressed in terms of the number of output levels the device has; for a 3 bit device the number is eight. The value of the LSB (also called a quantum) is equal to the converter's Full Scale Range (FSR) divided by the number of different input codes, i.e., the number of different output levels (2^n). A D/A converter's *Full Scale Range* is equivalent to the *nominal* peak to peak voltage (or current for current-output devices) of the converter's output range. For the 3 bit 0 to + 10V output range D/A of Figure 1, FSR = 10 volts, and 1 LSB = $10V/2^n = 10V/8 = 1.25$ volts. For the 3 bit ± 10V output range D/A of Figure 2, FSR = 20 volts, and 1 LSB = $20V/2^n = 20V/8 = 2.5$ volts. Table I shows the weights and amplitudes of LSB's for higher resolution converters.

Notice in Figures 1 and 2 that when all the digital inputs are turned "on", i.e., when the digital input is 111, the output of the converter doesn't quite make it to its nominal full scale value. It always falls 1 LSB short. This is due to the fact that the value of bit 1 (the Most Significant Bit or MSB) is FSR/2, the value of bit 2 is FSR/4, and the value of bit 3 (LSB) is FSR/8. When all the bits are "1", the output level will be the value of bit 1 (MSB) plus that of bit 2 plus that of bit 3 (LSB), i.e., its level will be ($\frac{1}{2} + \frac{1}{4} + \frac{1}{8}$) = $\frac{7}{8}$ FSR. Therefore, the actual positive full scale output of the D/A in Figure 1 is + 8.75V, not 10V, and the actual positive full scale output of the D/A in Figure 2 is + 7.5V, not 10V. For simplicity and convenience, however, data converters will usually have their analog input or output defined according to its nominal full scale (FS) value or its nominal FSR rather than to its actual FS or FSR.

Invariably, you'll see D/A transfer functions depicted as staircases. If one displays the D/A transfer function on a scope while stepping the input and sweeping the output at the right speed, one can make the transfer function look like the staircase one often sees, but the theoretical transfer function is a series of points as shown in Figures 1 and 2. A given digital input produces one and only one analog output level (voltage or current), and there are only 2^n (n = number of input bits) possible inputs (outputs).

When a manufacturer measures the accuracy of a D/A converter, he attaches his voltmeter or scope to the output, applies digital data to the inputs, and measures the output to see how close the levels are to what they're supposed to be.

The ideal analog input/digital output transfer function of a 3 bit, 0 to + 10V input range, straight binary coded analog to digital converter (A/D) is shown in Figure 3. The ideal analog input/digital output transfer function of a 3 bit, ± 10V input range, offset binary coded A/D converter is shown in Figure 4. The transfer functions are discontinuous and there is *not* a unique one-to-one relationship between analog input and digital output. A given digital output can be produced by more than one analog input. An A/D converter "quantizes" a continuous analog input signal into a set of discrete output states. The number of possible output states (codes) is equal to 2^n when n is the number of digital output bits. A 3 bit A/D has 8 output codes; an 8 bit A/D has 256 output codes; a 12 bit A/D has 4096 output codes, etc. Oftentimes you'll see A/D transfer functions plotted as staircases. This is a confusing misrepresentation. It is impossible for the digital outputs to

BIT	2^{-n} (Fraction)	"dB"	$1/2^n$ (Decimal)	%	ppm	Voltage (FSR = 10 Volts)	Voltage (FSR = 20 Volts)
MSB	2^{-1} 1/2	− 6	0.5	50	500,000	5	10
2	2^{-2} 1/4	− 12	0.25	25	250,000	2.5	5
3	2^{-3} 1/8	− 18.1	0.125	12.5	125,000	1.25	2.5
4	2^{-4} 1/16	− 24.1	0.0625	6.2	62,500	0.625	1.25
5	2^{-5} 1/32	− 30.1	0.03125	3.1	31,250	0.3125	0.625
6	2^{-6} 1/64	− 36.1	0.015625	1.6	15,625	0.15625	0.3125
7	2^{-7} 1/128	− 42.1	0.007812	0.8	7,812	0.078125	0.15624
8	2^{-8} 1/256	− 48.2	0.003906	0.4	3,906	0.039062	0.078125
9	2^{-9} 1/512	− 54.2	0.001953	0.2	1,953	0.019531	0.039062
10	2^{-10} 1/1,024	− 60.2	0.0009766	0.1	977	0.009766	0.019531
11	2^{-11} 1/2,048	− 66.2	0.00048828	0.05	488	0.0048828	0.009766
12	2^{-12} 1/4,096	− 72.2	0.00024414	0.024	244	0.0024414	0.0048828
13	2^{-13} 1/8,192	− 78.3	0.00012207	0.012	122	0.0012207	0.0024414
14	2^{-14} 1/16,384	− 84.3	0.000061035	0.006	61	0.00061035	0.0012207
15	2^{-15} 1/32,768	− 90.3	0.0000305176	0.003	31	0.000305176	0.00061035
16	2^{-16} 1/65,536	− 96.3	0.0000152588	0.0015	15	0.000152588	0.000305176
17	2^{-17} 1/131,072	− 102.3	0.00000762939	0.0008	7.6	0.0000762939	0.000152588
18	2^{-18} 1/262,144	− 108.4	0.000003814697	0.0004	3.8	0.00003814697	0.0000762939
19	2^{-19} 1/524,288	− 114.4	0.000001907349	0.0002	1.9	0.00001907349	0.00003814697
20	2^{-20} 1/1,048,576	− 120.4	0.0000009536743	0.0001	0.95	0.000009536743	0.00001907349

Table 1. Binary bit weights and amplitudes.

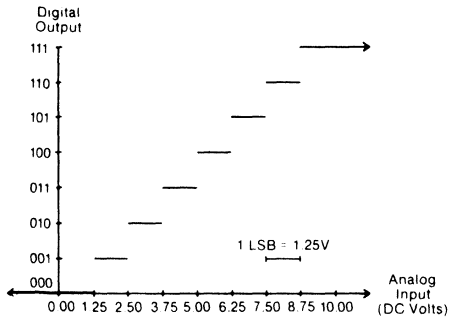


Figure 3. Analog input/digital output transfer function of an ideal, 3 bit, 0 to + 10V input range, binary coded A/D converter.

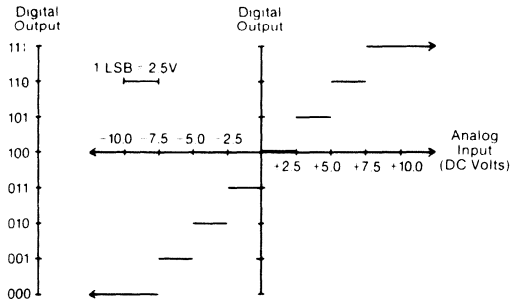


Figure 4. Analog input/digital output transfer function of an ideal, 3 bit, ± 10V input range, offset binary coded A/D converter.

exist in any but the 2^n states indicated. The "rise" portions of the staircase do not exist. Return to Figure 4. This 3 bit A/D operates as follows:

For an Input Voltage Between	The A/D Output Will Be MSB	Bit 2	LSB
< − 7.5V	0	0	0
− 7.5V and − 5.0V	0	0	1
− 5.0V and − 2.5V	0	1	0
− 2.5V and 0.0V	0	1	1
0.0V and + 2.5V	1	0	0
+ 2.5V and + 5.0V	1	0	1
+ 5.0V and + 7.5V	1	1	0
> + 7.5V	1	1	1

The arrows at the ends of the transfer function indicate that analog inputs greater than + 7.5V (up to the device's maximum allowed positive input voltage) all give a 111 output and that analog inputs less than − 7.5V (down to the maximum allowed negative input voltage) all give a 000 output. Also note that digital output words correspond not to single analog input voltages, but to "bands" or "ranges" of input voltage. The width of each band is the quantization size or the quantum; it is the value assigned to the converter's Least Significant Bit (LSB), and it is again equivalent to the converter's Full Scale Range (FSR) divided by 2^n (n = number of bits). An A/D's FSR is equivalent to the *nominal* peak-to-peak value of its input range. For the 0 to + 10V input range 3 bit A/D of Figure 3, FSR = 10 volts, and 1 LSB = $10V/2^n = 10V/8$ = 1.25 volts. For the ± 10V input range 3 bit A/D of Figure 4, FSR = 20 volts and 1 LSB = $20V/2^n = 2.5$ volts. The value of an LSB is the smallest analog change or difference which can be distinguished or resolved by the A/D. It is an indicator of converter resolution. As with D/A's, A/D resolution is usually expressed as the number of output bits or as the number of output states. See Table I.

Return again to Figures 3 and 4. Note again the quantization effect. Many different analog inputs may yield the same digital output. This is what quantization is all about. In Figure 3, any analog input between + 1.25V and + 2.50V gives a digital output of 001. 001 is the digital output for a "band" of analog input voltages that is 1 LSB wide. If we assign the code 001 to the nominal midrange of the input band for which it is valid, we can say that 001 corresponds to input voltages of + 1.875V ± 0.625 volts, which can be written as + 1.875V ± 1/2 LSB. The ± ½ LSB is the quantization uncertainty or the quantization noise. You'll often see it referred to on A/D data sheets as *Inherent Quantization Error.* It's unavoidable, and its magnitude is always an irreducible ± ½ LSB. If you want to reduce its effect, you'll have to go to a converter that has higher resolution, i.e., one that has more output codes and therefore, a smaller LSB. If you went to a 12 bit A/D with a ± 10V input range, each digital output word would represent a band of input voltages only 0.00488 volts wide. This band is still 1 LSB wide, but now an LSB is a lot smaller. Digital output codes are always going to stand for "bands" or "ranges" of input voltage. You've got to round off somewhere.

For the purposes of specifying and testing A/D converters, it is difficult and time consuming to measure the center of a quantization level (the + 1.875V in this example). The only points along A/D's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next.

Note in Figure 4 that the digital output changes from 000 to 001 as the input is increased from some more negative voltage to − 7.5V. It changes from 001 back to 000 as the input is decreased from some more positive voltage to − 7.5V. This voltage, − 7.5V, is the Minus Full Scale LSB Transition Voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "0". If the LSB output were tied to an LED and the converter were continuously converting, the LED would flicker on and off when the input voltage was at − 7.5V. For this reason, transition voltages are often called "flicker" voltages. Notice that the 011 to 100 transition (called the "major transition" because all the output bits change) ideally occurs at the zero volt analog input. At this point, under the conditions described above, all the output bits would be flickering. Lastly, the Positive Full Scale LSB Transition Voltage, the voltage at which the LSB flickers while the other bits remain "1", is ideally + 7.5V.

Analog Input (DC Volts)	Digital Output MSB	LSB
+ 10.0	111	
+ 7.5	11ϕ	
+ 2.5	10ϕ	
0.0	ϕϕϕ	
− 2.5	01ϕ	
− 7.5	00ϕ	
− 10.0	000	

Figure 5. Example of how digital output coding tables appear on Micro Networks' A/D converter data sheets. This table describes the A/D of Figure 4. With the converter continuously converting, the output bits indicated as ϕ will change from a "1" to a "0" or vice versa as the input passes through the voltage level indicated. The digital output changes from 000 to 001 (or vice versa) at an input level of − 7.5V. Input signals below this level will give an output of all "0's". The digital output changes from 011 to 100 (all bits change) at an input of zero volts. The digital output changes from 110 to 111 (or vice versa) at an input of + 7.5V. Any voltage greater than + 7.5V will give an output of all "1's".

Many converter users don't realize that transition voltages are what manufacturers look for when testing A/D converter Linearity and Accuracy. When a manufacturer tests the accuracy or linearity of an A/D converter, he attaches his voltmeter to the input to see if the transition voltages are where they are supposed to be. Micro Networks has begun to include transition voltages in the Output Coding Tables appearing in our A/D converter data sheets. Figure 5 shows the coding table that Micro Networks would use to describe the A/D of Figure 4. If one wanted to depict the A/D transfer function as a set of points (similar to a D/A transfer function) one can simply plot the transition voltages and suffer no loss of information. This is done in Figure 6. Notice that an A/D always has one less transition ($2^n - 1$) than the number of output codes (2^n).

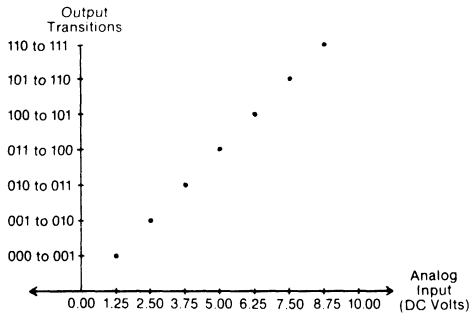


Figure 6. The digital output transitions of Figure 3 are plotted as a function of input voltage. This plot conveys all the information of Figure 3.

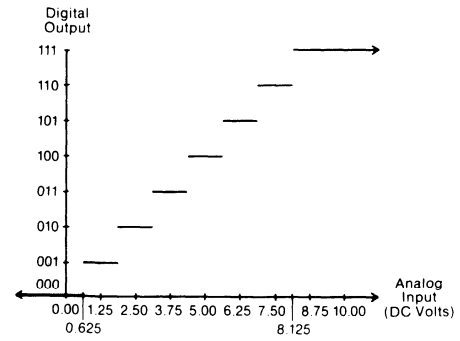


Figure 7. Analog input/digital output transfer function of an ideal, 3 bit, 0 to + 10V input range, binary code A/D converter trimmed so its first transition (000 to 001) occurs at + ½ LSB (+0.625V) and its last transition (110 to 111) at FS-3/2 LSB (+8.125V).

Lastly, note in Figure 3 that the LSB does not become a "1" until the analog input reaches a full LSB. Some manufacturers will design their A/D's so that the transfer function is pushed down ½ LSB, i.e., the LSB becomes a "1" when the input reaches + ½ LSB. This is shown in Figure 7. The rationale behind the transfer function of Figure 3 is to have the transfer function symmetrical within the entire input range. The first transition occurs 1 LSB above zero; the last 1 LSB below 10V. The code 001 corresponds to inputs between 1 and 2 LSB's.

The rationale behind the transfer function of Figure 7 is to have the output codes centered in the input bands corresponding to LSB increments. The first transition occurs at ½ LSB above zero; the last ½ LSB below 10V. The code 001 corresponds to inputs of 1 LSB ± ½ LSB. Throughout this discussion we will use A/D transfer functions similar to those of Figures 3 and 4 because we feel the symmetrical nature of the plot will simplify specification parameter demonstrations.

GROUPING CONVERTER SPECIFICATIONS

For the purpose of clarifying and simplifying the explanation of converter specifications, we have divided the specs into two major categories: the Performance Specifications and the Design Specifications. The Performance Specifications have been further subdivided into the Relative Performance Specifications, the Absolute Performance Specifications, and the Dynamic Specifications. The pertinent specs falling into each category are summarized in the diagrams below. We feel that classifying the definitions in this manner will clarify and reinforce their meanings and help us make a point.

PERFORMANCE SPECIFICATIONS

Relative Performance Specifications	Absolute Performance Specifications
Integral Linearity	Full Scale Absolute Accuracy Error
Differential Linearity	Unipolar Offset Error
Relative Accuracy	Bipolar Offset Error
Monotonicity (D/A's)	Unipolar Zero Error
No Missing Codes (A/D's)	Bipolar Zero Error
Gain Error	Drift Specifications
Drift Specifications	

Dynamic Specifications
- Settling Time (D/A's)
- Output Slew Rate (D/A's)
- Conversion Time (A/D's)
- Throughput Rate (A/D's)
- Throughput Rate (A/D's)
- Clock Frequency (A/D's)

DESIGN CHARACTERISTICS AND REQUIREMENTS
- Power Supply Range
- Power Supply Rejection
- Current Drains
- Power Consumption
- Reference Voltage
- Reference Current

D/A CONVERTERS	A/D CONVERTERS
Digital Input Coding	Digital Output Coding
Input Logic Levels	Output Logic Levels
Input Loading	Drive Capability (Fanout)
Glitch Energy	Input Logic Levels
Compliance Voltage	Input Loading
Output Load Current	Pulse Widths:
For D/A's with Input Registers:	1) Start Command
1) Latch Enable Pulse Width	2) Clock Low
2) Data Setup Time	3) Clock High
3) Data Hold Time	Start Signal Setup Time
Others	Others

The RELATIVE PERFORMANCE SPECIFICATIONS describe how the points that form a D/A's actual transfer function or the quantization bands that form an A/D's actual transfer function relate to each other as a group. Are they all there? How close to each other are they? Do they form a straight line? etc.. The Relative Performance Specs look at the *shape, conformity,* and *orientation* of the transfer function, not at its *location* on its axes. The single most important Relative Performance spec is Integral Linearity. The other important Relative Performance Specifications are Differential Linearity, Monotonicity (for D/A's), No Missing Codes (for A/D's), and Gain Error. Gain Error is adjustable on most converters available today. For all but the most sophisticated converters however, none of the other Relative Performance Specifications are adjustable.

The ABSOLUTE PERFORMANCE SPECIFICATIONS describe what the Relative Performance Specs do not, the location of the transfer function on its axes. They do not concern themselves with the fine details of the transfer function. For all practical purposes, they assume the transfer function is a straight line and question how this line relates to the axes it is plotted on. Does it pass exactly through zero? How close is its positive full scale endpoint to where it is supposed to be? How close is its negative full scale endpoint to where it is supposed to be? All of the Absolute Performance Specifications are types of Absolute Accuracy Errors, and they must be specified without adjustment, i.e., they must apply before any optional gain and offset adjusting has been performed. The specs we will discuss are Absolute Accuracy Error, Unipolar Offset Error, Bipolar Offset Error, Unipolar Zero Error, and Bipolar Zero Error.

The DYNAMIC SPECIFICATIONS are really only two specs. They basically tell a user how fast an A/D or a D/A gets its job done. For many users, they are the most important specs. We will discuss Settling Time for D/A's and Conversion Time for AD's.

The DESIGN SPECIFICATIONS describe the properties and requirements of converters that are fixed by design. For the most part, they are selfexplanatory, and we will not spend much time discussing them. Normally, designers do not choose converters based on their Design Specifications. Occasionally, someone will need an ultra-low power device or maybe an A/D that definitely has to be able to drive CMOS, but usually people will select a converter based on its Performance Specifications and tailor their system to meet the converter's Design Specifications.

DRIFT SPECIFICATIONS—Almost all of the important converter performance specifications are temperature sensitive, i.e., they drift with temperature. These temperature instabilities are important and are usually specified in terms of the resultant change in a particular parameter (a delta) for a given change in temperature, i.e., their units are usually V/°C, %FSR/°C, ppm/°C, ppm of FSR/°C, (fractions of an LSB)/°C, or total change over a specific temperature range. Drift specifications are called Temperature Coefficients, Tempcos, or T.C.'s. The T.C.'s we will concern ourselves with are those for Integral Linearity, Differential Linearity, Gain, Offset (Unipolar and Bipolar), and Absolute Accuracy. The effects of each on converter performance will be discussed within the section devoted to the appropriate room temperature specification.

Most converter drifts are fairly linear, and manufacturers will invariably assume they are linear when testing and measuring them. To measure or test a tempco, a manufacturer will measure a given parameter at two different operating temperatures and calculate the tempco as the total change in the parameter divided by the change in temperature. Normally, if a manufacturer is guaranteeing performance over a 0°C to +70°C temperature range, he will make test measurements at 0°C, at +25°C, and at +70°C. The range chosen for calculating the T.C. can be 0°C to +25°C, +25°C to +70°C, or 0°C to +70°C. Each may give a different number for the T.C., and the largest number should be the one that appears on the device data sheet.

Let's clarify ppm's before we get too far along since most tempcos will appear as some number of ppm's/°C. PPM stands for parts per million and can be thought of the same a one thinks about percentages.

$$1\text{ppm} = 1/10^6 = 10^{-6} = 0.000001 = 0.0001\%$$
$$1\text{ppm of FSR} = 1/10^6\text{FSR} = 0.0001\%\text{FSR}$$
$$1\% = 10^4\text{ppm} \qquad 1\%\text{FSR} = 10^4\text{ppm of FSR}$$

If a certain parameter is specified at +25°C and carries with it a T.C. of ±20ppm/°C and the converter is presently operating in an environment whose ambient temperature is +125°C, we can expect the parameter to have changed (in the worst case) by an amount Δ = change in temperature times the tempco.

$$\Delta = \Delta T \times (\text{T.C.})$$
$$\Delta = [\,(+125\,^\circ\text{C}) - (+25\,^\circ\text{C})\,] \times (\pm 20\text{ppm}/^\circ\text{C})$$
$$\Delta = (100\,^\circ\text{C}) \times (\pm 20\text{ppm}/^\circ\text{C})$$
$$\Delta = \pm 2000\text{ppm} = \pm 0.2\%$$

The total value of the parameter at +125°C will be equal to its room temperature value plus its drift component (±0.2%).

DIGITAL TO ANALOG CONVERTERS—RELATIVE PERFORMANCE SPECIFICATIONS.

INTEGRAL LINEARITY—Integral Linearity, Integral Linearity Error, Linearity Error, Linearity, and Non-Linearity are all the same specification. They are not the same as Differential Linearity which is discussed in the next section. Integral Linearity is a measure of the "straightness" of a D/A converter's transfer function. Refer to Figures 1 and 2. All the points that constitute a D/A's transfer function should theoretically form a perfectly straight line when connected together. Figure 8 shows what an actual D/A transfer function may look like. Integral Linearity is a measure of how far the points deviate from a reference straight line drawn through them as a group. Integral Linearity Error is usually expressed in portions of an LSB (± ¼ LSB, ± ½ LSB, ± ¾ LSB, etc.). Oftentimes, if linearity error is greater than ± 1 LSB, it will be expressed in %FSR or ppm of FSR.

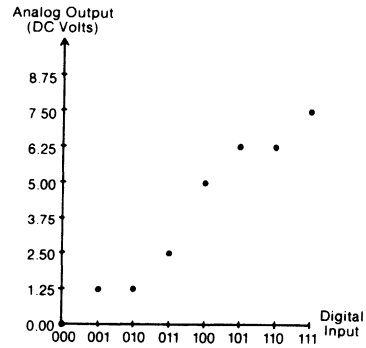


Figure 8. Transfer function of a nonideal, 3 bit, 0 to +10V D/A converter. Output points not forming a straight line is an Integral Linearity Error. c.f. Figure 1.

There are presently two accepted definitions of Integral Linearity; the two differ according to how they dictate the reference straight line should be drawn.

1) END-POINT LINEARITY of a D/A converter is a measure of the greatest deviation of the analog output values from a straight line *drawn between the end-points* of the converter's actual transfer function.

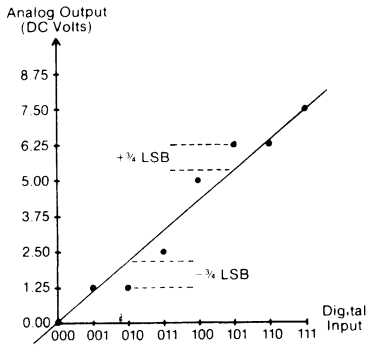


Figure 9. According to the end-point definition of Integral Linearity, the transfer function of Figure 8 has a ± ¾ LSB Integral Linearity Error. The most deviate points are + ¾ LSB and – ¾ LSB away from a straight line drawn through the endpoints.

Figure 9 shows the actual D/A transfer function of Figure 8 with a straight line drawn between its end-points. The "actual" end-points of the transfer function are the measured output voltages that appeared when the digital inputs were 000 and 111. Notice in Figures 8 and 9 that the actual end-points are not the same as the ideal end-points of Figure 1 and that the reference straight line passes through the actual and not the ideal end-points. The fact that the end-points and the rest of the points that comprise the transfer function are not located on the axes exactly where they are supposed to be does not matter right now—that's an accuracy error. Linearity views the points as an independent set and concerns itself only with how the points relate to each other, not to the axes. Note that the most deviate transfer function points are ± ¾ LSB above and below the line and that therefore, this converter has ± ¾ LSB Integral Linearity according to the end-point definition.

2) BEST-FIT STRAIGHT LINE LINEARITY of a D/A converter is a measure of the deviation of the analog output values from a *best-fit straight line* drawn through the group of points that comprise the converter's actual transfer function. "Best-fit" does not have a mathematical definition; the line is determined empirically by manipulation and can be defined simply as the line that yields the best linearity spec.

Figure 10 repeats the non-ideal D/A transfer function of Figure 8 with a "best-fit" straight line drawn through the transfer function. Notice that the line does not pass through the transfer function end-points and that the furthest points away from the line are only ± ½ LSB away. This converter has ± ½ LSB Integral Linearity according to the best-fit straight line definition. If you find it difficult to think in terms of a best-fit straight line, you can simply say that all the points of the transfer function fall in a band 1 LSB wide.

In actuality, if a D/A converter has ± ½ LSB Linearity according to either definition, all of its transfer function points will fall in a band 1 LSB wide. The converter that is ± ½ LSB linear according to the end-point definition will, by definition, have its endpoints in the center of the band. The converter that's

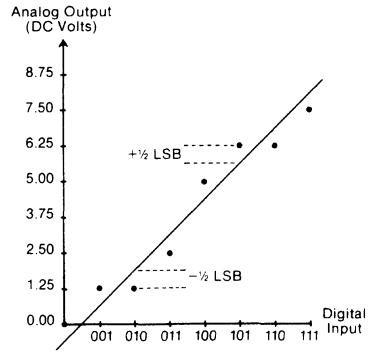


Figure 10. According to the best-fit definition of Integral Linearity, the transfer function of Figure 8 has a ± ½ LSB Integral Linearity Error. The most deviate points are + ½ LSB and – ½ LSB away from the best-fit straight line.

± ½ LSB linear according to the best-fit definition may have its endpoints anywhere within the band. Along that same line of thought, best-fit linearity specifications will always be symmetrical (± ¼ LSB, ± ½ LSB, etc.) while end-point linearity specifications may be asymmetrical (such as + ½ LSB – ¾ LSB).

Micro Networks feels that Integral Linearity is one of the most important converter specifications, and we contend that an n bit converter is not a true n bit converter unless it guarantees ± ½ LSB Integral Linearity (by either definition) over whatever temperature range it is to be used.

The traditional definition of linearity is the best-fit definition. End-point linearity is growing in popularity as a result of the microprocessor revolution. Many people are using distributed processors located near A/D converters and software to correct for converter inaccuracies. This is usually accomplished by locating the actual transfer function end-points and relating the rest of the points to a hypothetical straight line connecting the end-points. If linearity is specified according to the end-point definition, a user already knows how far away from the hypothetical line the rest of the transfer function points are and the corrected accuracy will be as good as the converter's linearity. If linearity is specified according to the best-fit definition, the user will not know how his hypothetical straight line compares to the best-fit straight line used to measure the linearity. For the person not using either hardware or software to correct the accuracy of their converter, it makes no difference which definition of linearity has been used by the manufacturer.

In a strict mathematical sense, the end-point definition is a more conservative measure of Integral Linearity than the best-fit definition. A converter tested to some linearity (say ± ½ LSB) according to the best-fit definition may be half as linear (twice as nonlinear or ± 1 LSB) according to the end-point definition. In reality, the reference line used for either definition almost always turns out to be the same line, and in all but the most sophisticated applications, a user would be hard pressed to tell the difference between a converter that was ± ½ LSB linear according to the best-fit definition and one that was ± ½ LSB linear according to the end-point definition.

People often speak of converter linearity in terms of bits. They will say a converter has 12 bit linearity if its linearity spec is equivalent to ± ½ LSB for 12 bits (± 0.012% FSR), regardless of the number of input or output bits the converter actually

has. They'll say it has 11 bit linearity if its linearity spec is equivalent to ± ½ LSB for 11 bits (±0.024%FSR); or 8 bit linearity if its linearity spec is equal to ± ½ LSB for 8 bits (±0.195%FSR). You'll come across 14 bit converters with 12 bit linearity and 12 bit converters with 11 bit linearity. You'll see 12 bit converters that have 12 bit linearity at room temperature, but their linearity drifts to 10 bits at +125°C (see Linearity Drift). You will also see devices whose linearity exceeds their resolution. Some 12 bit converters have 13 bit linearity, i.e., their linearity spec is ±0.006%FSR (½ LSB for 13 bits, ¼ LSB for 12 bits). Many 8 bit converters will have better than 8 bit linearity.

For D/A converters, ± ½ LSB Integral Linearity (by either definition) guarantees *Monotonicity* and ± 1 LSB *Differential Linearity*. For most converters, Integral Linearity is *not* adjustable.

DIFFERENTIAL LINEARITY—Differential Linearity is also called Differential Linearity Error or Differential Nonlinearity. If the digital input code to a D/A is changed from its present code to either the next higher or next lower code, the analog output level should increase or decrease an amount equivalent to one LSB. In other words, adjacent digital codes should result in measured output values that are exactly one LSB apart. Any deviation of the actual "step" size from the ideal one LSB is called a Differential Linearity Error or a Differential Nonlinearity, and the error is usually expressed in (sub)multiples of an LSB.

A maximum Differential Linearity Error of ± ½ LSB means that output step sizes can have a height of 1 LSB ± ½ LSB, i.e., the output voltage can change anywhere from ½ to 1½ LSB's when the input changes from one code to the next.

Figures 11 through 14 show sketches of a 3 bit, 0 to +10V, binary coded, D/A transfer function. The first (Figure 11) is ideal; it is a repeat of Figure 1. Each output step is 1 LSB high,and the Differential Linearity Error is zero LSB's. The second (Figure 12) has ± ½ LSB Differential Linearity Error. Note that some steps are ½ LSB high (1 LSB-½ LSB) others are 1½ LSB's high (1 LSB + ½ LSB). Figure 13 shows the transfer function of a D/A with ± 1 LSB Differential Linearity. Some steps are 0 LSB's high and others are 2 LSB's high. This converter is still monotonic. Figure 14 shows the transfer function of a *nonmonotonic* converter. Its Differential Linearity is ± 1½ LSB's. Note that some steps are negative ½ LSB (1 LSB-1½ LSB) while others are 2½ LSB's (1 LSB + 1½ LSB).

Converters with Differential Linearity Errors greater that ± 1 LSB may be Nonmonotonic (see section discussing Monotonicity).

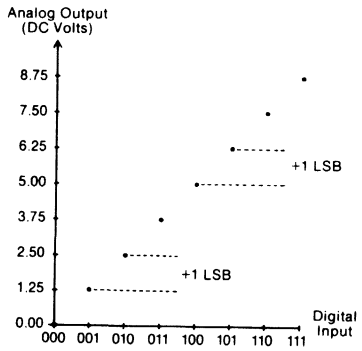


Figure 11. A repeat of the ideal, 3 bit, D/A transfer function of Figure 1. Each output step or discontinuity is 1 LSB high.

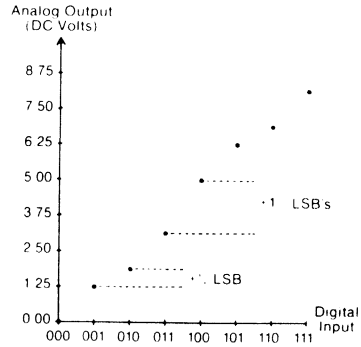


Figure 12. Nonideal, 3 bit, D/A transfer function having a ± ½ LSB Differential Linearity Error. Some of the output steps are + ½ LSB high; others are + 1½ LSB's high.

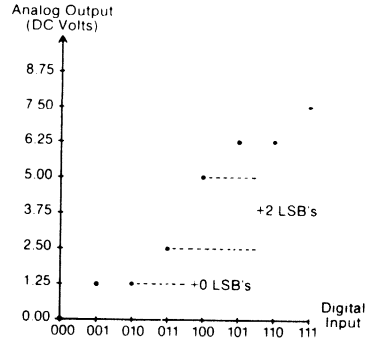


Figure 13. Nonideal, 3 bit, D/A transfer function having a ± 1 LSB Differential Linearity Error. Some of the output steps are 0 LSB's high (no change in output voltage following a change in input code); others are + 2 LSB's high.

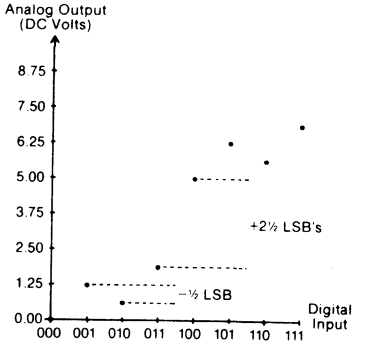


Figure 14. Nonideal, 3 bit, D/A transfer function having ± 1½ LSB Differential Linearity Error. Some of the output steps are − ½ LSB high (output goes down when input goes up); others are + 2½ LSB's high. This converter is nonmonotonic.

Return to Figures 12 and 13. Both of these converters still have better than ± ½ LSB Integral Linearity according to the best-fit straight line definition but not according to the end-point definition. ± ½ LSB Integral Linearity by *either* definition, however, guarantees that Differential Linearity Error will be better than ± 1 LSB, i.e., maximum Differential Linearity Error has an upper bound equal to two times the Integral

Linearity Error. It can be less than 2X Linearity, however, and some manufacturer may choose to test and specify it as being such. For example, a converter may specify ± ½ LSB Integral Linearity and ± ¾ LSB Differential Linearity. If it specifies ± ½ LSB Integral Linearity and says nothing about Differential Linearity, one can only assume that maximum Differential Linearity will be ± 1 LSB.

Two last comments—maximum Differential Linearity Error does not allow one to infer anything about Integral Linearity Error. One popular manufacturer, for example, advertises their 12 bit D/A as having ± ½ LSB Differential Linearity from -55 °C to + 125 °C. Integral Linearity, however, over the same temperature range is specified at ± 2 LSB's (10 bit Integral Linearity).

Differential linearity errors do not have to be symmetrical. If a converter had no output steps smaller than + ½ LSB and none larger than + 2 LSB's, its Differential Linearity Error would be − ½, + 1 LSB.

MONOTONICITY—Monotonicity is more a property of a D/A converter than it is a specification. Either a converter is monotonic or it is not. The relevant specification is the temperature range over which Monotonicity is guaranteed. Monotonicity means that the analog output of a D/A does not decrease as the digital input is increased nor increase as the digital input is decreased. This definition allows the output to remain the same as the digital input is increased or decreased. It is the same as saying that the derivative of the transfer function is always greater than or equal to zero.

Micro Networks prefers a slightly more strict definition which demands that the analog output always increase (decrease) as the digital input is increased (decreased).

Another way of defining Monotonicity is to say that Differential Linearity Error must be less than − 1 LSB. In other words, steps can be any size as long as they are greater than zero, i.e., as long as they are positive. Monotonicity is a very important parameter for D/A's used in servo applications. One always wants to be sure that a system drive signal is going up or down when it is supposed to. Nonmonotonicity can result in positive feedback and loop instabilities.

Monotonicity does not guarantee Differential Linearity (other than to the degree just stated), nor does it guarantee Integral Linearity. Monotonic converters can have very large positive steps or series of smaller positive steps that result in highly nonlinear transfer functions. The transfer functions of Figure 15 are monotonic but nonlinear.

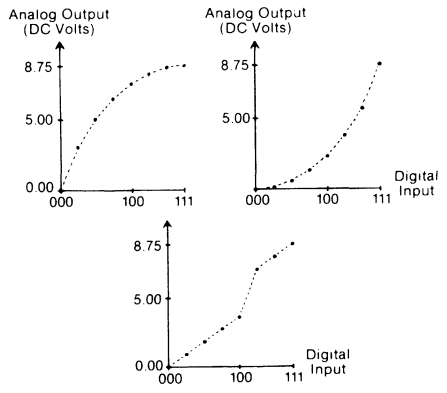


Figure 15. Three examples of D/A transfer functions that are monotonic but highly nonlinear. Monotonicity guarantees that Differential Linearity will be > − 1 LSB, but it gives no guarantees about Integral Linearity.

Beware of converters that guarantee Monotonicity and even Differential Nonlinearity over some temperature range but do not mention what happens to Integral Linearity over the same range. They could exhibit severe "bowing" of the transfer function as shown in Figures 15a and 15b.

REMEMBER: ± ½ LSB Integral Linearity Error will guarantee Monotonicity and Differential Linearity Error better than ± 1 LSB. Monotonicity and Differential Linearity, however, give no guarantees about Integral Linearity. A Monotonic transfer function is not necessarily a straight one.

INTEGRAL AND DIFFERENTIAL LINEARITY DRIFTS—

Recall that Integral Linearity is usually specified as a % of FSR or in fractions of an LSB. Integral Linearity Tempcos are usually given in ppm's of FSR/ °C. If a 12 bit D/A converter has ± ½ LSB (± 0.012% FSR) Integral Linearity at + 25 °C and a ± 1ppm of FSR/ °C Linearity Tempco, its Linearity at + 125 °C will be equal to its room temperature value plus its drift from + 25 °C to + 125 °C. The drift will equal:

$\Delta = \Delta T \times (T.C.)$
$\Delta = (100\,^{\circ}C) \times (\pm 1\text{ppm of FSR}/\,^{\circ}C)$
$\Delta = \pm 100\text{ppm of FSR}$
$\Delta = \pm 0.01\%\text{FSR}$

Therefore, at + 125 °C, the converter Linearity becomes (room temp value) + (drift) = (± 0.012% FSR) + (± 0.01% FSR) = ± 0.22% FSR. ± 0.22% FSR is almost equivalent to 1 LSB for 12 bits (0.024% FSR) or ½ LSB for 11 bits. Therefore, at + 125 °C this converter would only have 11 bit Integral Linearity which would mean that its effective resolution has been reduced to 11 bits. In other words, the converter manufacturer is saying that at + 125 °C, he no longer guarantees Monotonicity.

Most Micro Networks converters are guaranteed to be ± ½ LSB Linear at room temperature and ± ½ LSB Linear over their entire operating temperature range. For converters that don't hold ± ½ LSB Linearity over temperature, we will give a Linearity spec at + 25 °C and another spec that applies over the entire operating temperature range. Our MN565AJ 12-bit D/A, for example, guarantees ± ½ LSB Linearity at room temperature and ± ¾ LSB from 0°C to +70°C.

Recall that Differential Linearity Error is usually specified as a % of FSR or in fractions of an LSB. Differential Linearity Tempcos are usually given in ppm's of FSR/ °C. If a 12 bit D/A converter has a maximum Differential Linearity of ± ½ LSB at + 25 °C and a Differential Linearity Tempco of ± 2ppm of FSR/ °C, its Differential Linearity at + 125 °C will be:

± ½ LSB + [(100 °C) × (± 2ppm of FSR/ °C)]
± ½ LSB + (± 200ppm of FSR)
± 0.012% FSR + (± 0.02% FSR)
± 0.32% FSR.

This is greater than ± 1 LSB. At + 125 °C, this 12 bit converter may have become nonmonotonic. We say "may have become nonmonotonic" because it is possible that the converter transfer function bowed upwards such that the step sizes got larger but the device stayed monotonic. Normally, however, when this type of drift phenomenon occurs, the manufacturers will be proud of the fact that they have maintained Monotonicity and will say something to the effect of "Monotonicity guaranteed over temperature". If such a statement does not appear, a user can only assume that the converter became nonmonotonic when Differential Linearity exceeded ± 1LSB. At what temperature did that occur for the device mentioned above? At what temperature did its Differential Linearity Drift exceed ± ½ LSB? ± ½ LSB = ± 0.012% of FSR = 120ppm of FSR. If Differential Linearity Drift is ± 2ppm of FSR/ °C, it will take 60 °C for the drift to equal ± ½ LSB. Therefore, the converter became nonmonotonic at + 25 °C + (+ 60 °C) = + 85 °C.

What Differential Linearity Drift would a 12 bit D/A that guaranteed ± ½ LSB Differential Linearity at room temperature (+25°C) have to maintain in order to maintain Monotonicity up to +125°C? ± ½ LSB = 120ppm of FSR. 120ppm of FSR/ΔT = 120ppm of FSR/100°C = 1.2ppm of FSR/°C

Lastly, recall that ± ½ LSB Integral Linearity guarantees Monotonicity and Differential Linearity less than ± 1 LSB for D/A converters. A D/A that guarantees ± ½ LSB Linearity and Monotonicity at room temperature and then gives an Integral Linearity Drift specification without specifically stating what happens to Monotonicity or Differential Linearity over temperature is *not* guaranteeing monotonicity at any temperature other than +25°C.

RELATIVE ACCURACY—Relative Accuracy is a confusing specification, and you will not see it used on a Micro Networks data sheet. It is the data converter specification that has the greatest variety of definitions from different manufacturers. Micro Networks defines the Relative Accuracy of a D/A converter to be the measure of how accurate any of the D/A's output states are *relative* to a straight line drawn between the endpoints of the D/A's actual transfer function. Relative Accuracy is usually expressed in (sub)multiples of LSB's or in %FSR, and according to our definition, is exactly the same as Integral Linearity Error according to the end-point definition. Relative Accuracy does not include Gain and Offset Errors (to be discussed).

Some manufacturers have defined D/A Relative Accuracy to be the accuracy of any output state relative to the converter reference. This may be a fine definition for fixed external reference or for multiplying D/A converters, but it makes little sense when applied to the large majority of internal reference Dual-in-Line packaged D/A's. Most of these devices are functionally laser trimmed as assembled devices, and neither the manufacturer not the user ever know what the actual voltage of the internal reference is.

As a data converter specification, Relative Accuracy has two uses. Firstly, many manufacturers will use it for the purpose of informing a user how accurate, relative to the ideal, he/she can expect his/her D/A to be after its initial Gain and Offset Errors have been adjusted to zero through the use of trimming potentiometers. As an example, take the 3 bit, 0 to +10V D/A we've been discussing. If the manufacturer guarantees Relative Accuracy = ± ½ LSB, and the user adjusts the output so it is exactly 0V when the input is 000 and exactly +8.75V when the input is 111, every other analog output will be within ± ½ LSB (0.625 volts) of where it is ideally supposed to be. In this respect, we agree with the manufacturer who defines Relative Accuracy to be"...the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated". The second use of Relative Accuracy is that some manufacturers will use it in lieu of an Integral Linearity Error spec. This is fine if the intent is not to deceive. We stated earlier that in order for an n bit converter to be a true n bit converter, its Integral Linearity Error should be no worse than ± ½ LSB for n bits. Many times, when Relative Accuracy appears in lieu of Integral Linearity Error, we have noticed the error to be greater than ± ½ LSB.

Beware of high resolution converters (12 bits and up) that spec "accuracies" better than ± 2 LSB's. As a practical matter, such levels are difficult to achieve in state-of-the-art D/A's without external gain and offset adjustments. The manufacturer probably means Relative Accuracy.

GAIN ERROR—Gain Error is also called Range Error, Scale Error, or Scale Factor Error, and it has a number of differently stated definitions that all basically mean the same thing. Gain Error is a measure of the deviation from the ideal of the slope of a converter's transfer function. The slope of a converter's transfer function is defined as the slope of a straight line connecting its endpoints. The slope of the ideal transfer function as plotted in Figures 1 and 2 is 45° or 1. A device with negative Gain Error would have a less steep transfer function. A device with positive Gain Error would have a more steep transfer function. See Figure 16. Gain Error is normally

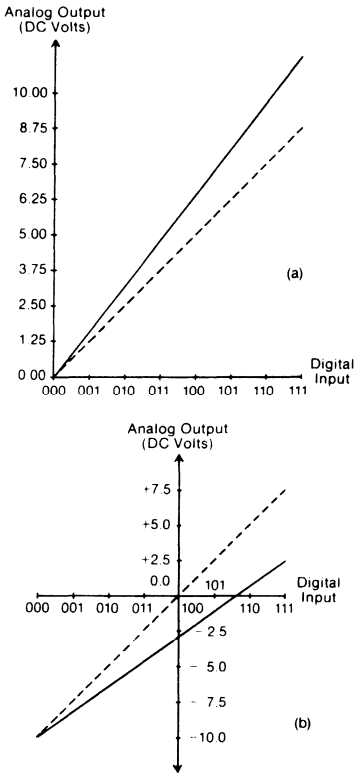


Figure 16. Sketches show the effect of positive Gain Error on the transfer function of a unipolar D/A converter (a) and the effect of negative Gain Error on the transfer function of a bipolar D/A converter (b). The ideal transfer functions are shown as broken lines; the transfer functions with Gain Error as solid lines.

measured using one of two methods. In method 1, a unipolar converter is first offset adjusted, either through hardware or software, until the zero end of its transfer function is pulled exactly into zero. A bipolar converter is first offset adjusted until the negative full scale end of its transfer function is pulled into its ideal value. Then the positive full scale output values are measured and compared to the ideal values. For the unipolar converter, Gain Error will be the difference between the measured and the ideal full scale output expressed as a % of the ideal output level. For the bipolar converter, Gain Error will be the difference between the measured and the ideal values of the total change from the negative full scale output to the positive full scale output expressed as a percentage of the ideal value. Method 2 consists of measuring the unipolar converter's actual, unadjusted positive full scale output and subtracting its actual zero output. For bipolar converters, the actual, unadjusted positive full scale output is measured and the actual minus full scale output is subtracted from it. The difference between the

resulting number and the ideal value for this number (FSR -1 LSB) expressed as a % of the ideal is the Gain Error. Gain Error can be defined as the difference between the measured and the ideal values of the converter's full output range (which is equivalent to the converter's FSR −1 LSB). Because the final number that results from measuring Gain Error by either method is a voltage, Gain Error specifications may sometimes appear in units of % FSR.

EXAMPLE: Recall the 3 bit, 0 to + 10V D/A of Figure 1. Its output for a 000 input is supposed to be 0V. Its output for a 111 input is supposed to be + 8.75V. Its ideal full output range is equal to + 8.75V −0V = + 8.75 volts (FSR −1 LSB). If its actual 000 output was + 0.05V and its actual 111 output was + 8.85V, its actual full output range would be + 8.80 volts. Its Gain Error would be (8.80 − 8.75)/8.75 = 0.57%. See Figure 17. If the converter's actual 000 output was −0.05V and its actual 111 output was + 8.70V, its actual full output range would be + 8.75V and its Gain Error would be zero. It would have an Offset Error and hence an Absolute Accuracy Error, but it would not have Gain Error. See Figure 17 and please read the sections describing Absolute Accuracy and Offset Error.

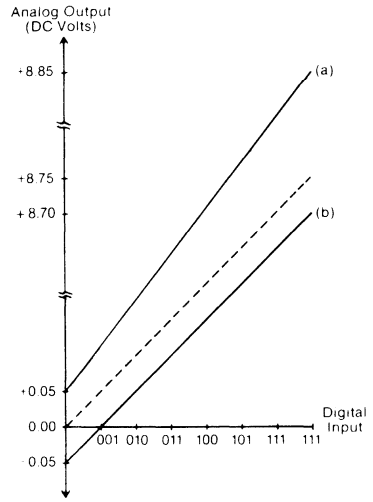


Figure 17. The ideal D/A transfer function is sketched as the broken line. The solid line above it has a positive 0.57% Gain Error (a). The solid line below it has zero Gain Error (b).

Gain Error is not an accuracy measurement, although as you will see, it can be used to calculate a converter's Absolute Accuracy Error when this spec is not given.

D/A CONVERTERS—ABSOLUTE PERFORMANCE SPECIFICATIONS

ABSOLUTE ACCURACY ERROR—The Absolute Accuracy Error of a voltage output D/A converter is the difference between the actual, *unadjusted* output voltage that appears following the application of a *given* digital input code and the ideal or expected output voltage for that code. This difference is usually expressed in LSB's or %FSR.

The two key words in this definition are "unadjusted" and "given". "Unadjusted" means just that; a D/A converter's Absolute Accuracy has to be measured before any optional gain and offset adjusting is performed. This is how Absolute Accuracy differs from Relative Accuracy. Absolute Accuracy tells you how accurate your converter is going to be if you simply plug it in, power it up, and start converting. Relative Accuracy tells you how accurate it will be after you go through the gain and offset error adjusting procedure. "Given" refers to the fact that any Absolute Accuracy specification has to be accompanied by some indication of where along the converter's input/output transfer function the spec applies, i.e., at what input code the Absolute Accuracy of the output is to be measured.

Because Absolute Accuracy Error is measured and specified without adjustment, it includes all factors that may be affecting a converter's accuracy at the point of measurement—Offset Error, Gain Error, Linearity Error, and Noise Error. Refer back to Figure 1. Assuming the transfer function is linear, the two key points necessary to fully describe this converter's Absolute Accuracy are at positive full scale (digital input 111) and at zero (digital input 000). To avoid ambiguity, the specs would be called Unipolar Positive Full Scale Absolute Accuracy Error and Unipolar Zero Absolute Accuracy Error (also called Unipolar Zero Error). Refer back to Figure 2. The three key points necessary to adequately describe the Absolute Accuracy of this device are at positive full scale (digital input 111), negative full scale (digital input 000), and zero (digital input 100). The three relevant specifications are Bipolar Positive Full Scale Absolute Accuracy Error, Bipolar Negative Full Scale Absolute Accuracy Error, and Bipolar Zero Absolute Accuracy Error (also called Bipolar Zero Error).

FULL SCALE ABSOLUTE ACCURACY—This is the Absolute Accuracy Error measured when the output of a D/A is supposed to be at its full scale value. Some manufacturers will draw a distinction between Unipolar and Bipolar Positive and Negative Full Scale Absolute Accuracy Errors. Micro Networks normally does not. For a converter's unipolar positive, unipolar negative, or bipolar output ranges, our Full Scale Absolute Accuracy Error specification refers to either the positive or negative full scale point or both, whichever is appropriate. Take our MN3013 and MN3014 8 bit D/A's for example. These devices have user-selectable output ranges of 0 to + 10V, 0 to − 10V, ± 5V, and ± 10V, and our data sheet gives a single Full Scale Absolute Accuracy Error specification. The spec applies to all the full scale output points, i.e., it means Unipolar Positive Full Scale Absolute Accuracy when using the 0 to + 10V range; Unipolar Negative Full Scale Absolute Accuracy when using the 0 to − 10V range; and both Bipolar Positive and Bipolar Negative Full Scale Absolute Accuracies when using the bipolar ranges. We will call out the different Full Scale Absolute Accuracy Errors separately only if they have different values.

ZERO ERROR—This is the Absolute Accuracy Error measured when the output of the D/A is supposed to be zero volts. Micro Networks will draw a distinction between Unipolar and Bipolar Zero Errors for converters that have different values for these two specifications. Otherwise, we will simply give a single Zero Error specification. Our MN3850 and MN3860 12 bit D/A's have user-selectable output ranges of 0 to + 5V, 0 to + 10V, ± 2.5V, ± 5V, and ± 10V, and the data sheet lists a single Zero Error of ± 0.05% FSR at + 25°C and ± 0.1% FSR over the entire operating temperature range. This spec applies to both Unipolar and Bipolar Zero Error depending upon which output range is being used.

Unipolar and Bipolar Full Scale Absolute Accuracy and Zero Errors are summarized in Figure 18. The transfer function shown in Figure 19 has a Negative Full Scale Absolute Accuracy Error of + 2.5 volts (+ 1 LSB), a Bipolar Zero Error of − 0.625 volts (− ¼ LSB), and a Positive Full Scale Absolute Accuracy Error of − 3.125 volts (− 1¼ LSB's). As will be explained in the following sections, Full Scale Absolute Accuracy and Zero Errors are the way in which Micro Networks prefers to specify converter accuracy.

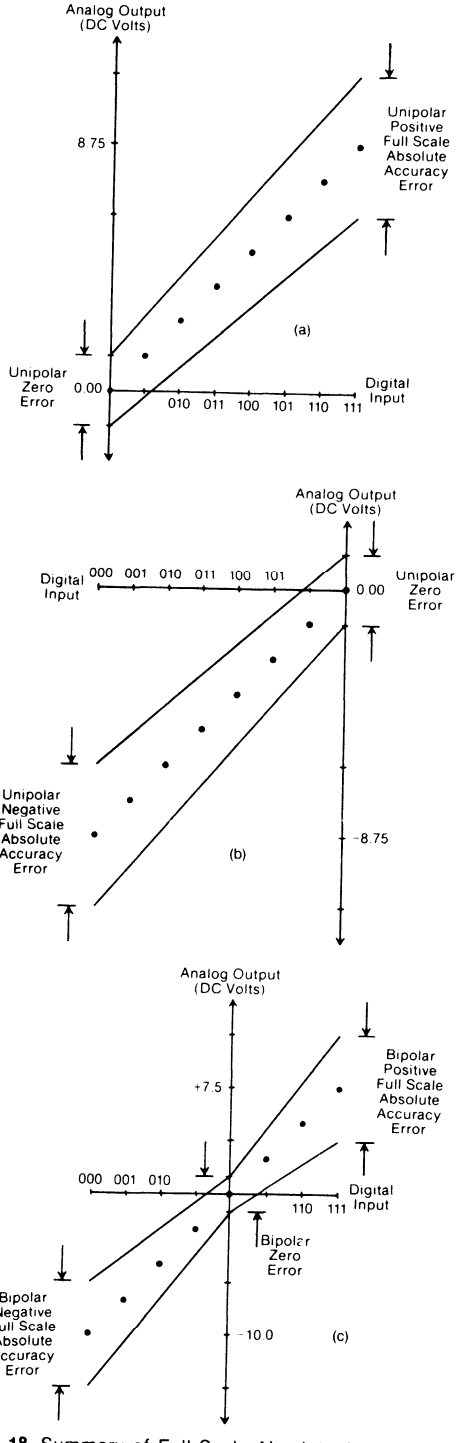


Figure 18. Summary of Full Scale Absolute Accuracy and Zero Errors for unipolar positive D/A converters (a), for unipolar negative D/A converters (b), and for bipolar D/A converters (c).

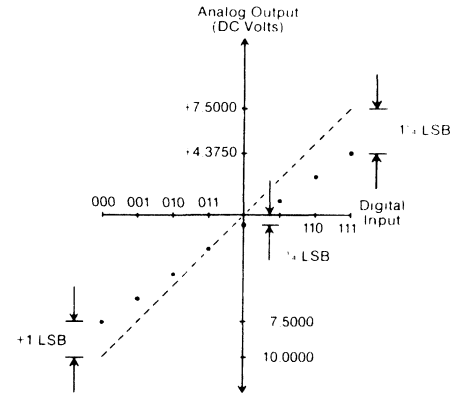


Figure 19. Example of a 3 bit, ± 10V output range D/A converter with a Bipolar Negative Full Scale Absolute Error of +2.5 volts (1 LSB), a Bipolar Zero Error of − 0.625 volts (− ¼ LSB), and a Bipolar Positive Full Scale Absolute Accuracy Error of − 3.125 volts (− 1¼ LSB's).

OFFSET ERROR—D/A Offset Error is an Absolute Accuracy Error that by definition has to be measured at a particular place along the converter's transfer function. It is the only widely used converter spec that is not a "black box" type of specification. The user has to have some understanding of how the converter works because the point of error measurement (the point where the spec applies) is determined by converter design. Linearity Error, Absolute Accuracy Error, Gain Error, and the other performance specifications relate only to a converter's transfer function and allow the user to think of the converter as a "black box". For this reason, Micro Networks does not like to specify Offset Errors. A converter's Offset Error will always be the same as either our Zero Error or Full Scale Absolute Accuracy Error,and we much prefer these specs, for we believe that most converter users prefer to think of converters as building blocks with certain input/output characteristics and that they really don't care what goes on inside of them. Many of our data sheets do list Offset Errors, however; the specs are there solely to facilitate comparing our converters to those of other manufacturers who prefer to spec Offset Errors.

For a quick understanding of how most D/A converters operate, see Figure 20. The figure is a simplified schematic for the 3 bit, 0 to + 10V, straight binary coded D/A whose transfer function is shown in Figure 1. The converter consists of 3 binary weighted current sources, 3 digitally-controlled electronic switches, and an output operational amplifier that converts the switch currents to an output voltage. The current sources are constant; they always push the current indicated (½ mA for the MSB current source, ¼ mA for the Bit 2 current source, and ⅛ mA for the Bit 3 current source) in the direction indicated. The digitally-controlled electronic switches are simple; they are connected directly to the D/A's digital inputs. When a logic "1" is applied to a given digital input, the respective switch moves to the right connecting its current source to the summing junction of the output amplifier. When a logic "0" is applied, the given switch moves to the left disconnecting the current source from the summing junction and connecting it to ground. The current labeled I_{DAC} is the total current being pulled from the amplifier summing junction by the current sources. The output op amp is an an inverting amplifier configuration with a 10Ω feedback resistor such that the D/A output voltage (V_{out}) is always equal to $I_{DAC} \times 10K\Omega$.

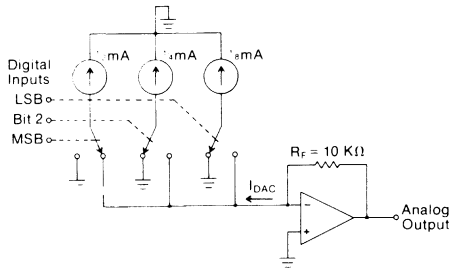


Figure 20. A simplified schematic for the 3 bit 0 to + 10V D/A of Figure 1. A logic "1" applied moves the switches to the right. A logic "0" applied moves the switches to the left.

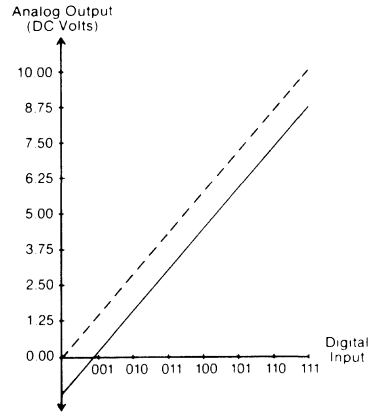


Figure 21. Unipolar Offset Error has the effect of displacing the transfer function along the voltage (output) axis parallel to itself. The broken line shows the ideal D/A transfer function. The solid line shows the transfer function of a D/A that has a Negative Unipolar Offset Error.

When the code 000 is applied, all the switches are to the left, and all the current sources are connected to ground. $I_{DAC} = 0$, and $V_{out} = 0$. When the code 100 is applied (the state indicated in the sketch), the MSB current source is connected to the output op amp, and the other current sources are connected to ground. $I_{DAC} = ½$ mA, and $V_{out} = +5V$. When the code 110 is applied, $I_{DAC} = ½ + ¼ = ¾$ mA; $V_{out} = +7.5V$. When the code 111 is applied, $I_{DAC} = ½ + ¼ + ⅛ = ⅞$mA; $V_{out} = +8.75V$. That's simple enough. If this converter were constructed with electronic switches that went to the left with "1's"applied and to the right with "0's"applied, we'd have a 3 bit, 0 to + 10V D/A with complementary binary coding. 000 applied would move all the switches to the right. I_{DAC} would equal ⅞ mA, and V_{out} would be + 8.75V. 111 applied would move all the switches to the left. I_{DAC} would equal 0 mA, and V_{out} would be OV.

D/A converter Offset Error (actually, in this example, because we are discussing a unipolar converter we should specify Unipolar Offset Error, but the definition is the same) is the Absolute Accuracy Error measured when the digital inputs are such that I_{DAC} is supposed to equal zero. Offset Error is usually measured in volts and specified in LSB's or % FSR. It is I_{DAC} not equalling zero when it is supposed to coupled with the offset error of the output op amp that result in D/A Offset Error. I_{DAC} not equalling zero is primarily due to switch leakage in the "off" state.

Offset Error adds a constant error voltage, the offset voltage, to all the output levels of a voltage output D/A. It has the effect of sliding the transfer function up or down along the output (voltage) axis parallel to itself. Figure 21 shows the transfer function of a unipolar D/A that has *only* Unipolar Offset Error, i.e., it has no Gain Error.

"Why," you may be asking, "do I have to understand how the converter works to understand Offset Error? Why don't you simply say it's the error measured when the output is supposed to be zero volts? How is it different from Zero Error?" For 90% of unipolar converters it isn't. For these devices there is no difference between Unipolar Offset and Unipolar Zero Error. There is a distinct subset of Unipolar D/A converters, however, for which Unipolar Offset Error has to be measured at one of the full scale outputs. These will be discussed shortly. For bipolar D/A's, Bipolar Offset Error is hardly ever measured at the zero volt output. This will also be discussed shortly.

Virtually all converter users think that Offset Error is the same as Zero Error. It is not.

Many manufacturers will define D/A Offset Error to be the analog output error that occurs when the digitally-controlled switches are in the "off" position. This definition is the same as the $I_{DAC} = 0$ definition, but it is confusing because it is often not clear what "off" means for complementary coded converters.

What is Bipolar Offset Error? First we have to understand how bipolar converters work. First we must realize that the bipolar transfer function looks just like a unipolar one that had been offset (moved down) ½ FSR (the value of an MSB). This offsetting effect is accomplished in actual converters by adding a constant current (equivalent to the MSB current) to the summing junction of the output amplifier. See Figure 22. It is the same as Figure 20 except that an additional ½ mA current source has been permanently attached to the summing junction of the output op amp. The result is that V_{out} now equals ($I_{DAC} - ½$ mA) × 10K. Therefore, when the input code is 100, $I_{DAC} = ½$ mA, and $V_{out} = 0V$. When the code is 111, $I_{DAC} = ⅞$ mA, and $V_{out} = +3.75V$. The 0 to + 10V D/A converter of Figure 20 has become a ±5V D/A converter.

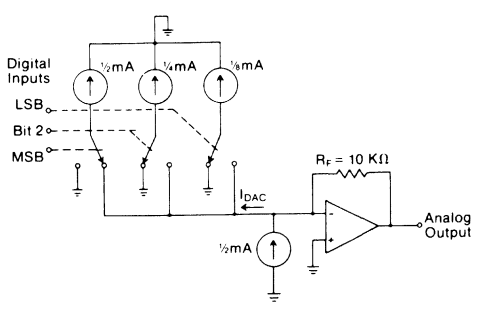


Figure 22. The 0 to + 10V 3 bit D/A of Figure 20 has been converted into a ± 5V 3 bit D/A by attaching a ½ mA constant current source to the summing junction of the output op amp.

Bipolar Offset Error is still the Absolute Accuracy Error measured when the digital inputs are such that I_{DAC} is supposed to = 0. It is I_{DAC} not equalling zero and the permanently attached ½ mA current source not equalling exactly ½ mA coupled with the offset error of the output op amp that result in Bipolar Offset Error. For this converter, as well as for 90% of all other bipolar D/A's, Bipolar Offset Error occurs at the minus full scale output. It is not equivalent to Bipolar Zero Error. For these converters, it is the same as Negative Full Scale Absolute Accuracy Error. As you might suspect, there is a subset of bipolar D/A converters for which the $I_{DAC} = 0$ condition occurs at positive full scale. These will also be discussed shortly.

Bipolar Offset Error affects a converter's transfer function the same way Unipolar Offset Error does. It slides the function up or down along the voltage axis parallel to itself adding a constant offset voltage to each output level. The transfer function of a bipolar converter having only Bipolar Offset Error (no Gain Error) is sketched in Figure 23. Let's now explore the subsets of converters mentioned above, those unipolar D/A's whose Unipolar Offset Error does not occur at zero and those bipolar D/A's whose Bipolar Offset Error does not occur at their minus full scale point. Figure 24 shows a popular digital to analog conversion technique that employs PNP transistors acting as equally weighted current sources and an R-2R resistor ladder acting as a current dividing network. For years, the only 12 bit D/A's capable of holding ± ½ LSB linearity over the −55°C to +125°C temperature range were designed this way. The circuit shown is for a 3 bit voltage output D/A. The output range is 0 to −10 volts such that a 000 digital input (TTL levels) will give a zero volt output and a 111 input will give a −8.75V output (minus full scale plus 1 LSB). One least significant bit (LSB) will be equal to 10 volts/2^3 = 1.25 volts. The transfer function is sketched in Figure 25.

Digital signals applied to the appropriate input pins turn the current sources (transistors Q_2, Q_3, and Q_4) on or off. The R-2R ladder network divides each transistor's collector current between ground and the converter's output op amp in a manner such that the portion of each collector current that reaches the output op amp is binarily weighted according to the transistor's position.

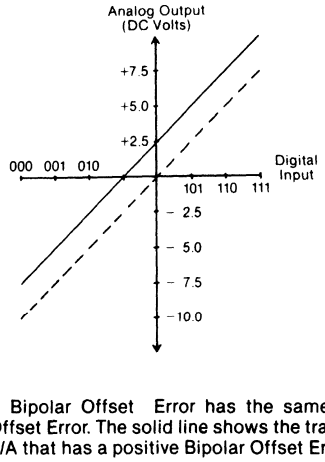


Figure 23. Bipolar Offset Error has the same effect as Unipolar Offset Error. The solid line shows the transfer function of a D/A that has a positive Bipolar Offset Error.

The reference voltage ($-V_{REF}$) is equal to −10V, and R_{REF} is equal to 20K. Node A is a virtual ground. I_{C1}, the collector current of transistor Q_1, equals V_{REF}/R_{REF} = +0.5mA, and $I_{E1} = I_{C1}$. The transistor bases are strapped together, and the R_E's are chosen such that the bases are biased at +1.4V. Op amp A_2 is used to maintain Node B at a constant voltage as the transistors are switched on and off and the I_E's change. Assuming the transistors are in their forward active regions of operation and all the R_E's are equal to each other (and not worrying about the switching diodes right now) makes $I_{E1} = I_{E2} = I_{E3} = I_{E4}$ and $I_{C1} = I_{C2} = I_{C3} = I_{C4}$. The transistor emitters (the switching diode anodes) are all at approximately +2.0V (transistor V_{BE} = −0.6V). The cathodes of the switching diodes (D_1, D_2, D_3) are the digital inputs to the converter. Digital signals applied to the converter's digital inputs turn the switching diodes and hence the transistors on and off. A TTL logic "0" (+0.8V maximum) applied to the converter's digital inputs (the diode cathodes) will forward bias the diodes. This results in the emitter voltages being pulled down to 1.4 volts (+0.8V for the digital input plus +0.6V for the diode drop) removing forward bias from the base emitter junction and turning off the transistors. Collector currents go to zero. The currents that flow through the R_E's are sunk in the digital signal sources. The application of a TTL logic "1" (+2.0V minimum) to the converter's digital inputs reverse biases the switching diodes bringing the transistor emitters back up to +2.0V. This turns the transistors on driving collector current into the R-2R resistor network.

The output amplifier summing junction node has been broken apart to show I_{DAC} as the current coming out of transistors Q_2, Q_3, and Q_4 and the R-2R ladder network into the summing junction. If all the digital inputs are "0's", transistors Q_2, Q_3, and Q_4 will be turned off, and I_{DAC} should equal zero. If the bit 1 (MSB) input has a "1" applied, and bits 2 and 3 have "0's" applied, I_{C2} and I_{C3} will equal zero and I_{DAC} will equal $I_{C4} = I_{C1} = +0.5$ mA. With the two bipolar offset connections (C_1 and C_2) open, all of I_{DAC} becomes I_F. With the feedback resistor R_F = 10K, the output voltage will equal $-R_F I_F = -(10K) \times (+0.5\ mA) = -5V$. With a "1" applied to the bit 2 digital input and "0's" applied to the bit 1 and bit 3 inputs, I_{C2} and I_{C4} will be zero and I_{C3} will equal +0.5 mA. The ladder network will divide I_{C3} so that I_{DAC} will equal +0.25 mA. V_{out} will now equal −2.5V. With a "1" applied to the bit 3 (LSB) input and "0's" applied to bits 1 and 2, I_{C3} and I_{C4} will be zero, and I_{C2} will equal +0.5 mA. This will be divided such that I_{DAC} will equal +0.125mA and V_{out} will equal −1.25 volts.

When all the digital inputs have "1's" applied, I_{DAC} will be equal to the sum of the currents that resulted when the "1's" were applied separately, i.e., I_{DAC} = 0.5 mA + 0.25 mA + 0.125 mA = 0.875 mA. V_{out} will now equal −8.75 volts. The rest of the output voltages for the remainder of the input codes can be calculated by simply adding the appropriate combination of voltage for each bit individually. The entire digital input/analog output transfer function is shown in Figure 25. This 3 bit D/A converter has a 0 to −10V output range, and its Unipolar Offset Error (the Absolute Accuracy Error measured when I_{DAC} is supposed to equal zero) must be measured with a 000 digital input, i.e., at its zero volt output. No problems! Let's now convert our 0 to −10V unipolar D/A into a ±5V bipolar D/A. This is accomplished by making bipolar offset connection C_1. The C_1 connection results in a constant current $I_{BO1} = V_{REF}/R_{BO1}$ = 10V/26.67 KΩ = +3.75mA being pulled out of the output op amp summing junction in the direction indicated. I_F is now equal to $I_{DAC} - I_{BO1}$. Therefore, when the digital inputs of the converter are all "0's" and $I_{DAC} = 0$, I_F will equal $-I_{BO1}$ (which is constant at −0.375mA), and V_{out} will equal +3.75 volts. With a "0" applied to the bit 1 digital input and "1's" applied to the bit 2 and bit 3 inputs, I_{DAC} will equal +0.375mA. $I_F = I_{DAC} - I_{BO1}$ will now equal zero, and V_{out} will equal zero. With all "1's" applied to the digital inputs, I_{DAC} will equal +0.875mA and I_F will

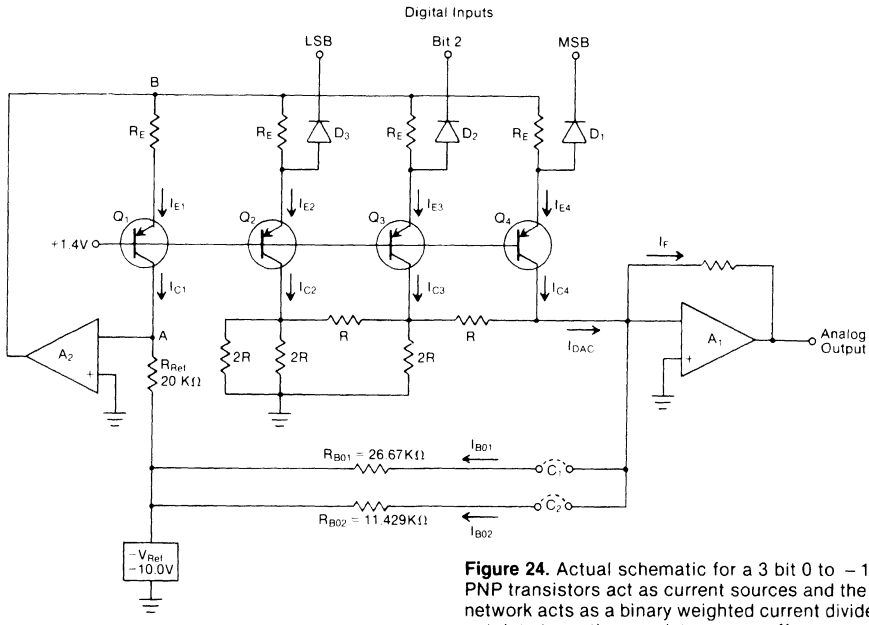


Figure 24. Actual schematic for a 3 bit 0 to − 10V D/A. The PNP transistors act as current sources and the R-2R ladder network acts as a binary weighted current divider. Digital input data turns the transistors on or off.

now equal + 0.5mA. V_{out} will equal − 5.0 volts. The transfer function for the ± 5V output range converter will be that shown in Figure 26b. Comparing Figure 26b to Figure 26a shows graphically that to convert a unipolar negative (0 to − 10V) 3 bit D/A to a bipolar ± 5V 3 bit D/A, the transfer function is offset (pushed up) an amount equal to the weight of bits 2 and 3 (3.75 volts). Again, this is effected electronically by pulling a constant current equivalent to the bit 2 plus 3 current (0.375mA) out of the output amplifier summing junction, i.e., through the feedback resistor.

Where does Bipolar Offset Error have to be measured? According to its definition, it has to be measured when I_{DAC} is supposed to equal zero. This occurs with a digital input of 000 and an analog output of + 3.75V. Bipolar Offset Error, at least for this converter, has to be measured at its positive full scale output, not at its negative full scale output. It is I_{DAC} not equalling zero and I_{BO1} not equalling + 0.375mA coupled with op amp offset error that cause Bipolar Offset Error. Finally, to make our original 0 to − 10V converter into a 0 to + 10V converter, the transfer function must be offset full scale. The 0 to + 10V transfer function is shown in Figure 26c. Comparing this to Figure 26a shows that the original transfer function must be offset (pushed up) an amount equal to the weight of all the digital inputs (8.75 volts). To accomplish this electronically, the C_2 offset connection has to be made (C_1 is now open). The C_2 connection results in a constant current of $I_{BO2} = V_{REF}/R_{BO2}$ = 10V/11.429K = + 0.875mA being pulled out of the output op amp summing junction in the direction indicated. I_F now equals $I_{DAC} - I_{BO2}$. Therefore, when the converter's digital inputs are all "0's" ($I_{DAC} = 0$), I_F equals $-I_{BO2}$(constant at − 0.875mA), and V_{out} will equal + 8.75V. With a "1" applied to the bit 1 digital input and "0's" applied to the bit 2 and bit 3 digital inputs, I_{DAC} will equal + 0.5mA. $I_F = I_{DAC} - I_{BO2}$ will now equal − 0.375mA and V_{out} will equal + 3.75V. With all "1's" applied to the digital inputs, I_{DAC} will equal + 0.875mA and I_F will now equal 0mA. V_{out} now equals zero volts. Again, the unipolar positive (0 to + 10V) transfer function is shown in Figure 26c. Where does Unipolar Offset Error now have to be measured? I_{DAC} is supposed to equal zero when the converter output is at its positive full scale output (+ 8.75V). Therefore, Unipolar Offset Error has to be measured there, not at the zero volt output. Notice how the digital coding differs for the unipolar positive and unipolar negative ranges. For the unipolar negative range (Figure 26a), a 000 digital input gave zero volts output. For the unipolar positive range (Figure 26c), a 000 digital input gives a + 8.75V (full scale minus 1 LSB) output. In order to get zero volts out of the unipolar positive converter, one has to apply a 111 digital code. Applying this code to the unipolar negative converter gives a − 8.75V (minus full scale plus 1 LSB) output.

The reason we have gone through all of this in such detail is to show precisely why we don't like Offset Error as a data converter specification. Some manufacturers will include in their data sheets an explanation of Offset Error so the user can know where the spec applies. Others simply use the term Off-

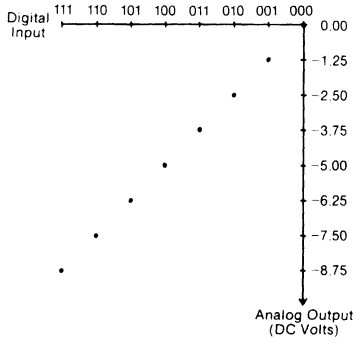


Figure 25. Digital input/analog output transfer function of the 0 to − 10V 3 bit D/A of Figure 24.

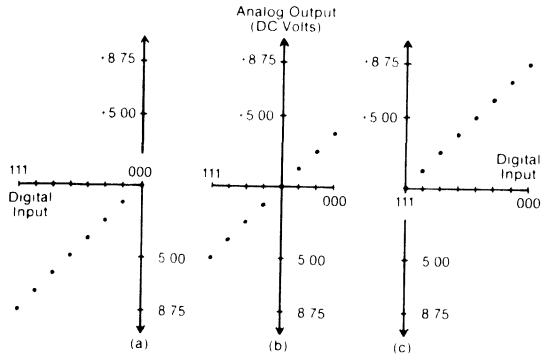


Figure 26. The 0 to − 10V 3 bit D/A transfer function (a) of Figure 25 is turned into that for a ± 5V 3 bit D/A (b) by making the C_1 offset connection. It is turned into that for a 0 to + 10V 3 bit D/A (c) by making the C_2 offset connection. Notice how subtracting a constant offsetting current from the summing junction of the output op amp affects the transfer function.

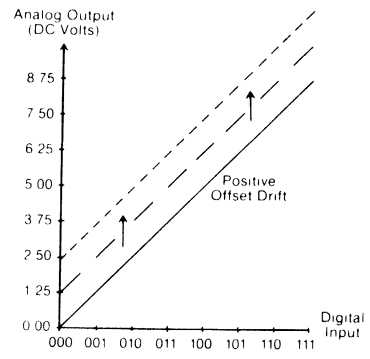


Figure 27. Offset Drift slides the transfer function parallel to itself along the voltage axis. The transfer function motion indicated would occur for a positive offset drift.

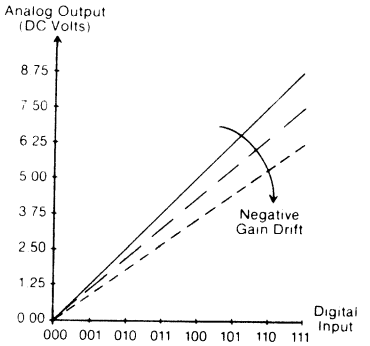


Figure 28. Gain Drift rotates the transfer function around the point at which Offset Error occurs. The transfer function motion indicated would occur for a negative gain drift.

set to mean Zero Error. Again, Micro Networks takes the position that a user should not have to understand the inner workings of any converter he/she is considering using, and that Offset Error, because it is defined according to these inner workings, is an ambiguous spec that should be avoided when specifying converters. We prefer to specify the accuracy of a converter's input/output characteristic using Full Scale Absolute Accuracy and Zero Errors.

OFFSET AND GAIN DRIFT—Offset Error is usually expressed in LSB's or %FSR and Offset Drift is usually expressed in ppm's of FSR/°C. If a D/A converter has a room temperature (+ 25 °C) Offset Error of ± 0.1%FSR and an Offset Drift of ± 5ppm of FSR/°C. Its Offset Error at + 85 °C will equal its room temperature value plus a drift component. The drift component will equal (ΔT) × (Offset T.C.) = (60 °C) × (± 5ppm of FSR/°C) = ± 300ppm of FSR = ± 0.03%FSR. The total Offset Error at + 85 °C will equal (± 0.1% FSR) + (± 0.03% FSR) = ± 0.13% FSR. At + 125 °C, the total Offset Error will equal ± 0.15% FSR. As Offset drifts, the transfer function moves parallel to itself along the voltage (output) axis. See Figure 27.

Gain Error is usually expressed as a %, and Gain Drift is usually expressed in ppm's/°C. If a D/A converter has a room temperature (+ 25 °C) Gain error of ± 0.2% and a Gain Drift of ± 20ppm/°C, its total Gain Error at + 85 °C would be ± 0.32%, and its total Gain Error at + 125 °C would be ± 0.4%. Gain Drift has the effect of rotating the D/A transfer function around the point at which Offset Error occurs. See Figure 28.

For the unipolar D/A, Gain and Offset Drift are the result of indepedent error sources, and their combined net effect on the transfer function as temperature changes is unpredictable. Figure 29a shows a unipolar unit exhibiting positive Offset Drift and positive Gain Drift. Its Absolute Accuracy Drift is equal to the sum of Gain and Offset Drift. Figure 29b shows a unipolar unit exhibiting negative Offset Drift and positive Gain Drift in a manner such that Full Scale Absolute Accuracy does not drift at all. If the directions of Offset and Gain Drift are not known, a user can only assume that worst case Unipolar Absolute Accuracy Drift will be equal to the sum of the two drift specs.

For the bipolar D/A, Bipolar Offset and Gain Drifts interact in a complicated manner that results in Absolute Accuracy Drift being less than the sum of the two specs. This will be discussed shortly.

ABSOLUTE ACCURACY vs. GAIN AND OFFSET

Presently, Micro Networks manufactures D/A and A/D converters for two main types of users, and we specify these converters accordingly. The first type of user is in the commercial/industrial marketplace. We understand this user to be very cost conscious and willing to go through a gain and offset adjusting procedure to achieve the greatest accuracies from his/her converters. Our experience tells us that these users expect to be able to purchase lower cost converters by not demanding maximum limits on room temperature Absolute Accuracies. They do however, demand good Linearities and hence good Relative Accuracies. They also demand accurate Linearity, Gain, and Offset Drift specifications because they usually design equipment to operate over known limited temperature ranges. The second type of user is in the military/aerospace marketplace. This user has to design equipment to operate within specification over the entire − 55 °C to + 125 °C temperature range, and he/she wants to avoid the use of adjusting potentiometers because of their inherent unreliability and their need for periodic recalibration. This user cannot concern himself/herself with drift specifications, but demands Absolute Accuracy and Linearity specs guaranteed from − 55 °C to + 125 °C.

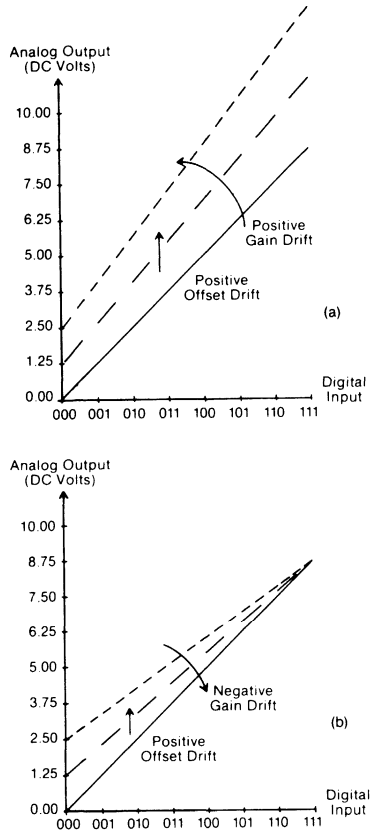


Figure 29. Positive Unipolar Offset and Gain Drifts add together to give a positive Absolute Accuracy Drift (a). It is possible for Offset and Gain Drifts to be in opposite directions such that Full Scale Absolute Accuracy Drift is zero (b).

It is this second type of application that we would like to discuss in detail. We would like to explain why we feel that the converter to be used in an application in which its initial Gain and Offset Errors are not going to be adjusted out with external potentiometers is much better specified with Zero and Full Scale Absolute Accuracy Errors than it is with Gain and Offset Errors, both at room temperature and over any specified operating temperature range.

For all practical purposes, the transfer function of a data converter with halfway decent linearity can be considered to be a straight line, and the converter's accuracy specifications should describe the position of the straight line relative to its axes, i.e., they should describe how close the straight line comes to the ideal. There are two simple ways to describe the plot of a straight line on a set of rectangular axes. The line can be described by two points or by a point and slope (angle). Micro Networks prefers the two-point technique (our two points being our Zero Error and Full Scale Absolute Accuracy Error) to the point-slope technique (the point being Offset Error and the slope being Gain Error). We prefer our method for no fewer than four good reasons:

1) Offset Error is confusing.
2) The Gain-Offset Method calls for extra, often complicated, mathematical manipulation on the part of the user to determine converter accuracy at transfer function points other than that at which Offset Error occurs and at temperatures other than +25°C.
3) The Gain-Offset Method may reject units whose Gain and Offset Errors have opposite polarities resulting in acceptable accuracy.
4) The Absolute Accuracy method allows us to specify much tighter Bipolar Zero Errors than the competition without affecting our overall yields.

Let's discuss these points one at a time. The ambiguity of Offset we have already addressed in the section labeled "Offset Error".

To address point 2, we have to answer the question "How does one go about determining the Absolute Accuracy of a D/A converter that lists only Offset and Gain Errors on its data sheet?" At room temperature, one can simply add the two errors. Take an industry-standard 12 bit D/A like the DAC80. Most manufacturers of this device will list the following specifications at room temperature.

Unipolar Offset Error	±0.15%FSR (Maximum)
Bipolar Offset Error	±0.15%FSR (Maximum)
Gain Error	±0.3%

The DAC80's Unipolar Offset Error occurs at its zero volt output, and its Bipolar Offset Error occurs at its minus full scale output. Therefore, at room temperature, its Unipolar Zero Error will equal its Unipolar Offset Error (±0.15%FSR), and its Unipolar Positive Full Scale Absolute Accuracy Error will equal the sum of its Unipolar Offset and Gain Errors (±0.45%FSR). This means that when operating at +25°C on the 0 to +10V output range, the unadjusted DAC80's actual full scale output voltage may be as much as ±0.45%FSR (which equals 45mV or almost 19 LSB's) away form its ideal value (+9.9976V) and still be within spec. The limits are summarized in Figure 30.

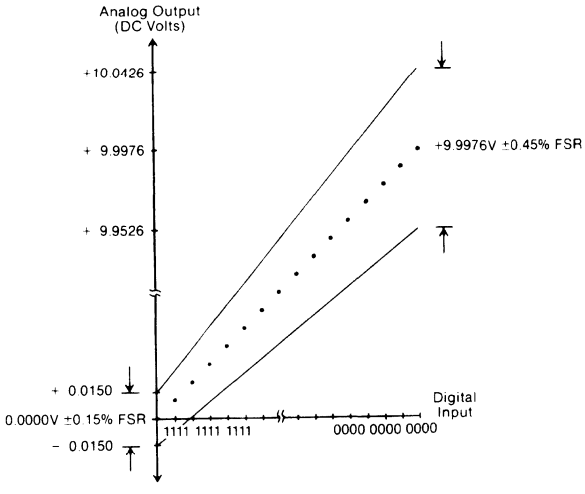


Figure 30. At +25°C, the DAC80's Unipolar Positive Full Scale Absolute Accuracy Error (±0.45% FSR) is equal to the sum of its Unipolar Offset Error (±0.15% FSR) and its Gain Error (±0.3%). The dots show the ideal transfer function for the 0 to +10V output range. The solid lines are the Absolute Accuracy limits.

For bipolar ranges, the Negative Full Scale Absolute Accuracy Error will equal the Bipolar Offset Error (±0.15%FSR). The Positive Full Scale Absolute Accuracy Error will equal the sum of the Bipolar Offset and Gain Errors (±0.45%FSR). The Bipolar Zero Error will equal the sum of the Bipolar Offset Error and ½ the Gain Error (±0.3%FSR). These limits are summarized in Figure 31.

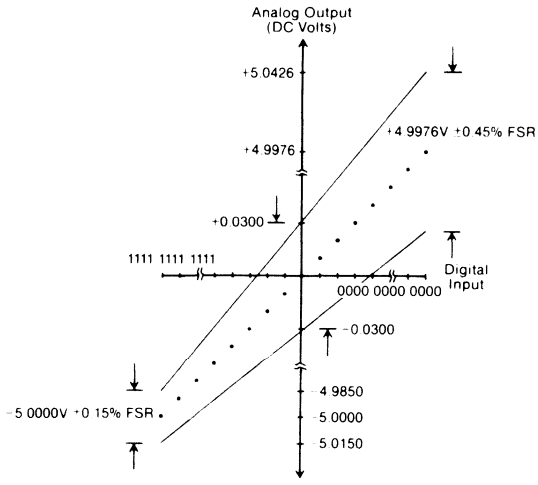


Figure 31. At +25°C, the DAC80's Bipolar Absolute Accuracy is equal to the sum of its Bipolar Offset Error and its Gain Error. The dots show the ideal transfer function for the ±5V output range. The solid lines are the Absolute Accuracy limits.

To calculate the Absolute Accuracy of a DAC80 at temperatures other than +25°C, users can make use of the converter's Gain, Offset, and Reference Drift specifications. The data sheet lists the following:

Gain Drift	±30ppm/°C (Maximum)
Gain Drift Exclusive of Reference Drift	±10ppm/°C (Maximum)
Reference Drift	±20ppm/°C (Maximum)
Unipolar Offset Drift	±3ppm/°C (Maximum)
Bipolar Offset Drift	±15ppm/°C (Maximum)

Let's find the Unipolar and Bipolar Absolute Accuracies of the DAC80 at +70°C. For unipolar ranges, the calculations are simple. Zero Error at +70°C will be the same as Unipolar Offset Error at +70°C; it will be equal to the room temperature value plus the drift component. The change in temperature (ΔT) from +25°C to +70°C is 45°C. Therefore, the drift component is (45°C)×(±3ppm of FSR/°C) = ±135ppm of FSR = ±0.0135%FSR, and the total Unipolar Offset Error at +70°C will equal ±0.15%FSR ± 0.0135%FSR = ±0.1635%FSR (maximum). The Positive Full Scale Absolute Accuracy Error at +70°C can be calculated in two ways. The first method simply adds the Unipolar Offset Error at +70°C to the Gain Error at +70°C. The Gain Error at +70°C will equal the room temperature value plus the drift component: ±0.3% + (45°C)×(±30ppm/°C) = ±0.3% + 1350ppm = ±.435%. The Positive Full Scale Absolute Accuracy Error at +70°C will equal ±0.1635% FSR ±0.435% FSR = ±0.5985% FSR. These limits are summarized in Figure 32.

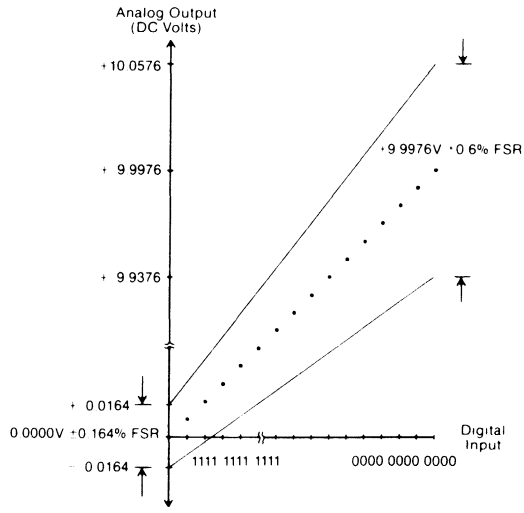


Figure 32. Unipolar Absolute Accuracy of the DAC80 at +70°C is equal to the sum of Unipolar Offset Error at +70°C and Gain Error at +70°C.

Calculating Bipolar Absolute Accuracies at temperatures other than +25°C is not so simple. Negative Full Absolute Accuracy Error at +70°C is equal to Bipolar Offset Error at +70°C (±0.2175%FSR) but Positive Full Scale Absolute Accuracy Error at +70°C is not equal to the sum of Bipolar Offset Error at +70°C and Gain Error at +70°C. This is due to the fact that the largest portions of Gain Drift and Bipolar Offset Drift are the result of reference drift, and in the bipolar mode, these components partially cancel each other making Positive Full Scale Absolute Accuracy Drift much less than the sum of Gain and Bipolar Offset Drift. As a rule of thumb, Positive Full Scale Absolute Accuracy Drift will be equal to ½ the Reference Drift plus the Gain Drift Exclusive of Reference Drift plus the Bipolar Offset Drift Exclusive of Reference Drift. If these drift specifications are not listed on the manufacturer's data sheet, the following rules can usually be applied:

Reference Drift = ⅔ of Gain Drift

Gain Drift Exclusive of
Reference Drift = ⅓ of Gain Drift

Bipolar Offset Drift Exclusive of
Reference Drift = ⅓ of Bipolar Offset Drift

Applying these rules to the DAC80 gives the result that the total Positive Full Scale Absolute Accuracy Drift will equal ±10 ± 10 ± 5ppm of FSR/°C. Bipolar Positive Full Scale Absolute Accuracy Error at +70°C will equal the room temperature spec (±0.45%FSR) plus the drift component. The drift component will be (45°C)×(±25ppm of FSR/°C) = ±1125ppm of FSR = ±0.1125 of FSR and the Positive Full Scale Absolute Accuracy Error at +70°C will equal ±0.45 ± 0.1125 = ±0.5625%FSR which is better than the Unipolar Positive Full Scale Absolute Accuracy Error at +70°C. The results are summarized in Figure 33. I think we have made our point. It takes a lot more work than it should for a user to figure out how accurate a converter is going to be when he/she intends to use it without initial gain and offset adjustments, and the device is specified with initial Gain and Offset Errors and the appropriate drift specifications. The situation is complicated by the fact that many manufacturers who choose to give room temperature Gain and Offset Errors only give typical values for these specs.

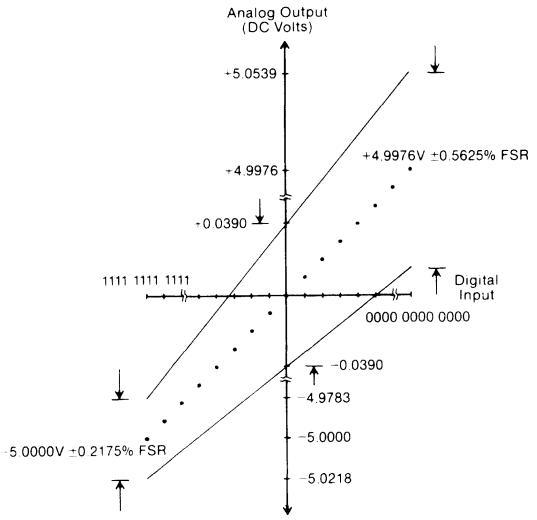


Figure 33. Bipolar Absolute Accuracy of the DAC80 at + 70 °C is better than the sum of Bipolar Offset Error at + 70 °C and Gain Error at + 70 °C.

Point 3 was that we felt the Gain-Offset technique could result in the rejection of units that had perfectly good accuracy. This point needs clarification, and we think this is best accomplished graphically. We will give one example here and further examples in the discussion of point 4. Figure 34 shows the Absolute Accuracy limits of a 3 bit, 0 to + 10V output range D/A that has a maximum Unipolar Offset Error of ± 12.5% FSR (± 1 LSB) and a maximum Gain Error of ± 14.3% (this Gain Error spec results in a maximum Gain Error of ± 1 LSB when the converter is at its full scale output).

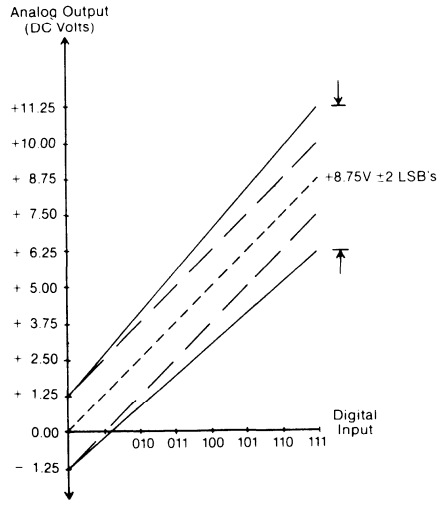


Figure 34. The solid lines show the Absolute Accuracy limits of a 3 bit 0 to + 10V D/A that has a Unipolar Offset Error of ± 12.5% FSR (± 1 LSB) and a Gain Error of ± 14.3%.

The ideal transfer function is the short-dashed line. The long-dashed lines show the Offset Error, and the solid lines show the Absolute Accuracy Limits fixed by the sum of Gain and Offset Errors. We are assuming that the device's Offset Error occurs at its zero volt output. Fig. 35 plot (a) is the transfer function of a D/A converter that has the maximum allowable Gain and Offset Errors, i.e., the transfer function tracks the upper limit of Absolute Accuracy. It has a Zero Error of + 1 LSB and a Positive Full Scale Absolute Accuracy Error of + 2 LSB's. Fig. 35 plot (b) is the transfer function of a D/A that has − ½ LSB Offset Error and + 21.45% Gain Error (1½ times the allowable limit). This unit would be rejected for exceeding the Gain Error specification yet its Zero Error is twice as good as that of the previous unit (− ½ LSB compared to + 1 LSB) and its Positive Full Scale Absolute Accuracy Error is also twice as good as the "good" unit (+ 1 LSB compared to + 2 LSB's). The user who is not performing initial gain and offset adjusting would actually prefer the "bad" unit.

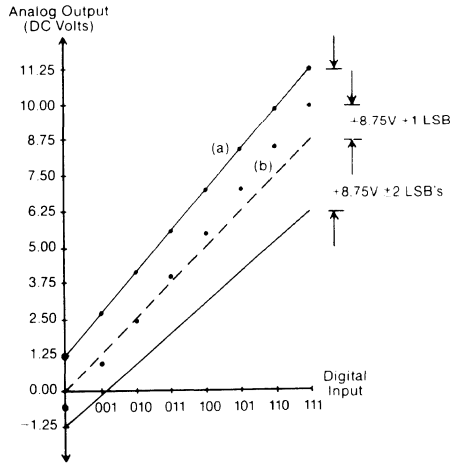
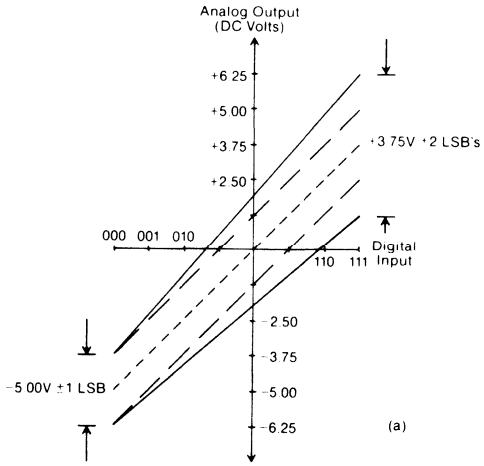


Figure 35. Transfer function (a) is that of a 3 bit 0 to + 10V D/A that has the maximum Gain and Offset Error allowed in Figure 34. Unipolar Zero Error = + 1 LSB. Full Scale Absolute Accuracy Error = + 2 LSB's. Transfer function (b) is that of a 3 bit 0 to + 10V D/A that has a Unipolar Offset Error (Zero Error) = − ½ LSB and Gain Error = + 21.45%. The result is a Full Scale Absolute Accuracy Error of + 1 LSB.

Point 4 refers only to bipolar converters, but we want to preface our discussion by saying that for unipolar converters there really is not a whole lot of difference between specifying Gain and Offset Errors and Full Scale Absolute Accuracy and Zero Errors. We saw in the discussion of point 2 that as long as a user knows where the Offset Error specification applies, all he/she has to do is add the Gain and Offset Errors at any temperature to find the Full Scale Absolute Accuracy and Zero Errors at that temperature.

As we also saw in the discussion of point 2, the situation is not the same for the bipolar converters. Let's review what the Gain-Offset technique says about the Absolute Accuracy of bipolar converters. Figure 36 shows the Absolute Accuracy limits of 3 bit, ± 5V output range D/A that has a maximum Bipolar Offset Error of ± 1 LSB and a maximum Gain Error of

± 14.3%. The sketch is the same as that of Figure 32 offset half scale. We are assuming that this device's Bipolar Offset Error occurs at its minus full scale output. As you can see, the Absolute Accuracy limits are in the shape of a "fan" and henceforth, we shall call the Gain-Offset technique of specifying accuracy the fan Method. As temperature changes, gain and offset drift in an interacting manner resulting in a new Fan at each temperature. The result is still a fan-shaped limit, however, and its bipolar offset end (the minus full scale end in this example) is always tighter than its other end (the positive full scale end in this example).



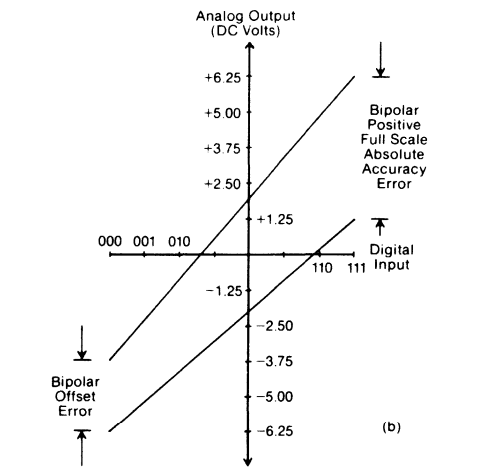


Figure 36. Absolute Accuracy limits of a 3 bit ± 5V D/A with a ± 1 LSB Bipolar Offset Error and a ± 14.3% Gain Error (a). Absolute Accuracy limits are in the shape of a "Fan" (b).

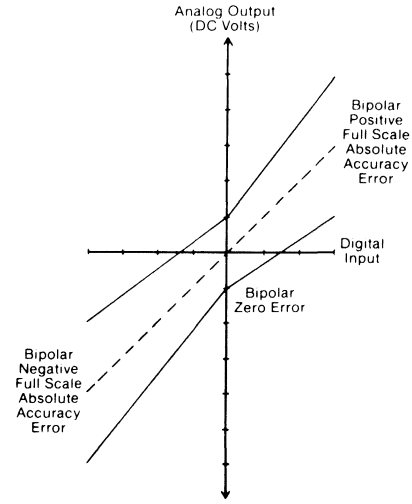


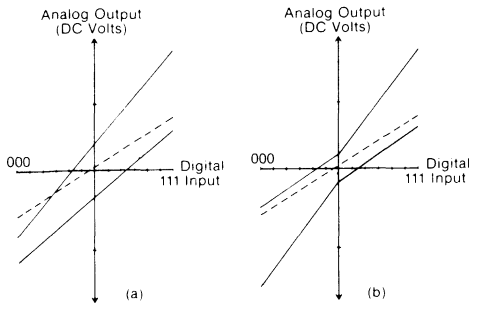
Figure 37. Micro Networks prefers to loosen the Negative Full Scale Absolute Accuracy Error and tighten the Bipolar Zero Error gving Absolute Accuracy limits that resemble a "Butterfly".

Micro Networks specifies the accuracy of bipolar converters using a Negative Full Scale Absolute Accuracy Error, a Positive Full Scale Absolute Accuracy Error, and a Bipolar Zero Error. We usually make our Positive and Negative Full Scale Error specifications equal to each other and much greater than our Bipolar Zero Error resulting in Absolute Accuracy limits that resemble a "butterfly" (see Figure 37). Henceforth, we will refer to our technique as the Butterfly Method.

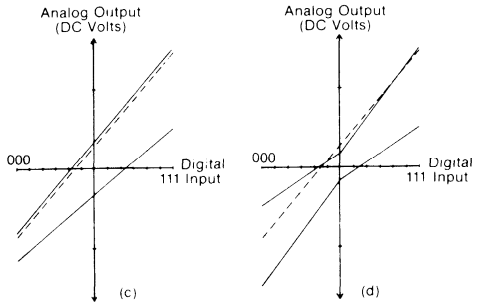
As stated earlier, we feel the Butterfly Method allows us to specify much tighter Bipolar Zero Errors than the Fan Method does. Let's see why. The tight end of the Fan limits is always the Bipolar Offset Error specification, and Bipolar Offset Error is an error source that most manufacturers have a pretty good handle on. Therefore, either because of tradition or through an effort to make their converters look as good as possible on paper, these manufacturers will specify tight Bipolar Offset Errors. Because Gain Error is much more difficult and more expensive to control, these manufacturers have to open up the other end of the Fan in order to get decent product yields. The result is that the *Bipolar Zero Error* specification has to be opened up to accommodate the Gain Error.

In reality, thanks to laser trimming, Bipolar Zero Error is about as easy to control as Bipolar Offset Error is, and Micro Networks has chosen to relax our Negative Full Scale Absolute Accuracy Error and tighten up our Bipolar Zero Error. In other words, for every unit that has a good Negative Full Scale Absolute Accuracy Error and poor Bipolar Zero Error there is a unit that has a poor Negative Full Scale Absolute Accuracy Error and a good Bipolar Zero Error. Micro Networks has chosen to call the latter "good" units and former "bad" units. Manufacturers who test to the Fan Method are calling the latter "bad" units and the former "good" units. See Figure 38.

Why do we feel our "good" units are better than their "good" units? Firstly, for most D/A and A/D converters used in closed loop control applications, Bipolar Zero Accuracy is much more important than Negative Full Scale Accuracy. Take a look at our MN3850H and MN3860H 12 bit D/A converters. These devices guarantee ±0.1%FSR maximum Bipolar Zero Error over the entire −55°C to +125°C operating temperature range. You cannot buy a 12 bit D/A with a better



Figures 38a and 38b. The unit whose transfer function is shown as the dashed line has a large Bipolar Offset Error and a small Bipolar Zero Error. It fails the Fan limits and passes the Butterfly limits.



Figures 38c and 38d. The unit whose transfer function is shown as the dashed line has a small Bipolar Offset Error and a large Bipolar Zero Error. It passes the Fan limits and fails the Butterfly limits. Which is the more accurate device?

Bipolar Zero Error. Secondly, we see very few bipolar applications in which it is necessary to have a Negative Full Scale absolute Accuracy Error that is better than the Positive Full Scale Absolute Accuracy Error, especially at the expense of Bipolar Zero Error.

We have made our case. A good percentage of Micro Networks converters are designed without the option for external gain and offset adjusting. These devices were designed for simplicity of use, and all of them are specified with maximum Full Scale Absolute Accuracy and Zero Errors at room temperature and over the specified operating temperature range. Please feel free to contact our Applications Staff if you have any questions concerning how and why we specify our converters the way we do.

D/A CONVERTERS—DYNAMIC SPECIFICATIONS

SETTLING TIME—Settling Time is defined as the total elapsed time between the application of a new input code and the point at which the analog output has entered and remained within some specified percentage of its final value. Normally, the input code change should be such that the D/A output is forced over its full range, i.e., the code change should be from all "1's" to all "0's" or vice versa. The specified limits of the final error band are placed around the output's final value, not its ideal value. See Figure 2. Suppose this 3 bit, ± 10V D/A gave an actual output of + 7.25V (instead of the ideal + 7.5V) when its input was all "1's". To measure settling time, one would start at a 000 input, apply a 111 input, and measure how long it took for the output to reach and remain within the band defined as "final value ± ½ LSB" (+ 7.25 ± 1.25 volts).

If a Settling Time spec is given for a 1 LSB change, the change should be that occurring when the MSB just turns on or off, i.e., when the digital input goes from a "0" and all "1's" to a "1" and all "0's" or vice versa. This is the situation in which the greatest output glitch and therefore the longest settling for a 1 LSB change occurs. In most D/A applications, Output Slew Rate will not be an important parameter if Settling Time is properly specified.

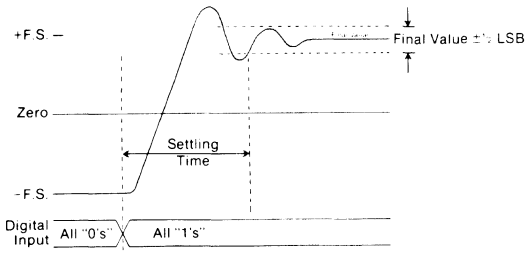


Figure 39. Settling Time is the elapsed time between the application of a new input code and the point at which the analog output enters and remains within the band described as final value ± ½ LSB.

SUCCESSIVE APPROXIMATION A/D CONVERSION

The technique of A/D conversion most widely used in data acquisition applications is that of "successive approximations". This is primarily due to the fact that successive approximation A/D conversion offers excellent tradeoffs in resolution, speed, accuracy, and cost. The highest resolution devices can convert 16 bits in tens of microseconds with some models selling for under $200. 12 bit units can convert in under 2μsec and sell for under $40. 8 bit units can convert in hundreds of nanoseconds and sell for a few bucks.

Virtually all successive approximation (SA) analog to digital converters are voltage input devices, and the conversion process is remarkably similar to finding the weight of an unknown object using a chemist's balance and a set of binarily weighted known weights (e.g., ½ lb., ¼ lb., ⅛lb., $\frac{1}{16}$ lb(= 1 oz.), ½ oz., ¼ oz., etc.). All of the A/D converters presently manufactured by Micro Networks are successive approximation types. Figure 40 shows a simplified block diagram for a 3 bit, 0 to + 10V successive approximation A/D. Figure 41 is its timing diagram. The circuit consists of a block of controlling logic and flip flops known as a successive approximation register (SAR), a current output D/A converter with reference, a clock, and a comparator. The outputs of the SAR's four flip flops act as both the direct (parallel) data outputs of the converter and the digital drive for the internal D/A converter. When the appropriate signal is applied to the converter's Start Convert input, the Status output rises to a "1" indicating that the converter is in the process of performing a conversion and that digital output data is not valid. At the same instant, the digital outputs of the SAR all go to "0" except for the MSB which is set to a "1". In this state (called the reset state), the digital output of the A/D is 100, and the current (I_{DAC}) coming out of the internal D/A is the MSB current.

The analog input signal dropped across R_{in} produces a current I_{in}. The D/A continuously converts the digital output of the A/D into an equivalent analog current that the comparator continuously compares to I_{in}. The comparator output

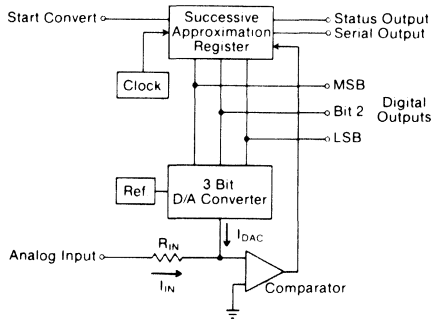


Figure 40. Block diagram of a 3 bit successive approximation A/D converter. This technique is very similar to weighing an unknown on a chemist's balance.

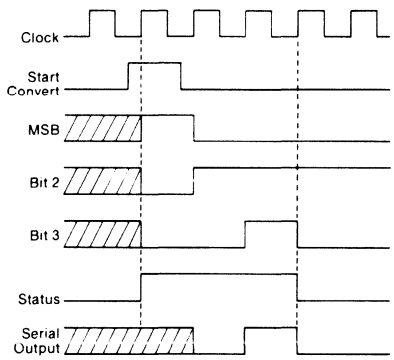


Figure 41. Timing diagram for the 3 bit A/D of Figure 40. After a conversion has been initiated, each output bit is set to its final value on successive rising clock edges.

("1" or "0") informs the SAR whether the present digital output (100 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the start signal has been applied, the SAR's logic will make a decision and set the MSB to its final state ("1" or "0") and bring bit 2 up to a "1". The digital output is now X10. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final state, and brings bit 3 up to a logic "1". The digital output is now XX1. On the next rising clock edge, the SAR reads the comparator feedback and sets the LSB to its final state. If this were more than a 3 bit A/D, this successive approximation procedure would continue in order of descending bit weights until all the output bits had been set. The rising clock edge that sets the LSB to its final state also drops the Status output to a "0" indicating that the conversion has been completed and that the digital output data is now valid. Data will remain valid as long as the status is a "0".

There is also a Serial Data output. The data is in nonreturn-to-zero format (NRZ) with each bit being present on the output line for one clock period following the rising clock edge that set that bit to its final value. Serial data is valid on falling clock edges, and these edges can be used to clock serial data into receiving registers.

The analog input to an S/A type A/D should not change during the conversion time. The conversion time is defined as the width of the Status output pulse and it is strictly a function of clock frequency. If the input were to change during a conversion, the output code would no longer accurately represent the analog input unless the new value were larger than the sum of the weights already present by an amount less than the sum of the untried weights. Since this is a not-often-fulfilled requirement, it is common to employ a sample-hold device ahead of the converter to retain the input value that was present at the instant the conversion starts and maintain it constant throughout the conversion. The Status output of the converter could be used to release the sample-hold from its hold mode at the end of conversion. A sample-hold may not be needed if the signal (by itself, or with filtering) varies slowly enough and is sufficiently noise-free that significant changes will not occur during the conversion interval.

Accuracy, linearity, and speed are primarily affected by the properties of the D/A converter, the reference, and the comparator. In general, the settling time of the D/A converter and the response time of the comparator are considerably slower than the switching time of the digital elements and will limit conversion speed. The differential nonlinearity of the D/A converter will be reflected in the differential nonlinearity of the resulting A/D converter. If the D/A converter is non-monotonic, one or more codes may be missing from the A/D converter's output range. Bipolar A/D's are created by using bipolar D/A's with appropriate input scaling.

The SAR's employed by Micro Networks in most of our SA type A/D converters are complementary coded. This means that in the reset state the MSB is a "0" and the other bits are "1's", and as each bit is set to its final value, the succeeding bit is dropped to a "0" rather than being raised to a "1". At the end of a conversion, the Status rises to a "1" rather than dropping to a zero. The fact that we use complementary coded SAR's makes very little difference since we normally also use complementary coded D/A's internal to the A/D's. The final result is that most of our A/D's are complementary rather than straight binary coded.

Figure 42 is a repeat of Figure 3. It is the transfer function of a 3 bit, 0 to +10V input range, binary coded A/D converter. Figure 43 is a repeat of Figure 4. It is the transfer function of a 3 bit, ±10V input range, offset binary coded A/D converter. Recall our brief discussion of the A/D transfer function at the beginning of this tutorial. The only points along an A/D's analog input/digital output transfer function that can quickly

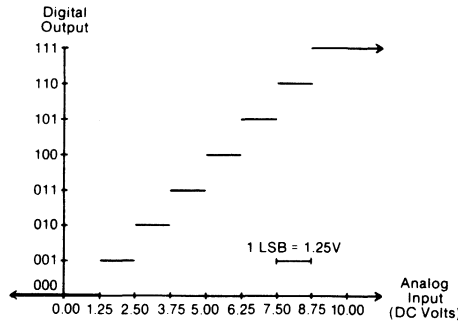


Figure 42. Analog input/digital output transfer function of an ideal, 3 bit, 0 to + 10V input range, binary coded A/D converter.

and accurately be detected and measured are the transition voltages, the analog input voltages at which the digital outputs change from one code to the next.

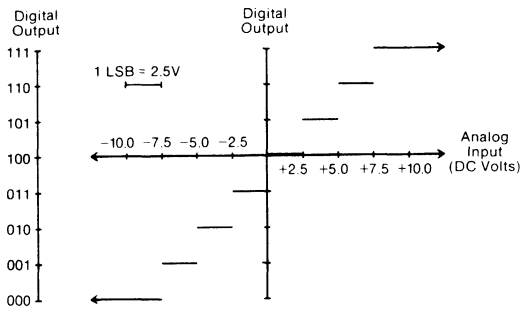


Figure 43. Analog input/digital output transfer function of an ideal, 3 bit ± 10V input range, offset binary coded A/D converter.

Notice in Figure 43 that the digital output changes from 000 to 001 as the input is increased from some more negative voltage to − 7.5V. It changes from 001 back to 000 as the input is decreased from some more positive voltage to − 7.5V. This voltage, − 7.5V, is the Minus Full Scale LSB Transition Voltage. It is the voltage at which the LSB changes from "1" to a "0" or vice versa while all other bits remain "0". Note that the 011 to 100 transition (called the major transition because all the output bits change) ideally occurs at the zero volt analog input, and that the Positive Full Scale LSB Transition Voltage, the voltage at which the LSB changes while the other bits remain "1", is ideally + 7.5V.

Most converter users don't realize that transition voltages are what manufacturers look for when testing A/D converter Linearity and Accuracy. When a manufacturer tests the accuracy of an *A/D* converter, he attaches his voltmeter to the *input* to see if the transition voltages are where they're supposed to be. If one wanted to depict the A/D transfer function as a set of points (similar to a D/A transfer function) one simply has to plot the transition voltages with no loss of information. This is done in Figure 44.

This section now continues with a discussion of Relative and Absolute Performance Specifications for A/D converters. The discussions of individual parameters will not be as detailed as they were for D/A converters since most of the observations made earlier pertain to both D/A's and A/D's. In particular, the arguments against the use of Offset Errors and the reasons why Micro Networks prefers to specify bipolar accuracies according to the Butterfly Method rather than to the Fan Method pertain equally to both A/D's and D/A's.

ANALOG TO DIGITAL CONVERTERS - RELATIVE PERFORMANCE SPECIFICATATIONS

INTEGRAL LINEARITY — As was the case with D/A's, the integral Linearity of A/D converters is a measure of the "straightness" of the converter's input/output transfer function. For D/A's, Integral Linearity described how close the points that were the analog output voltages were to a straight line drawn through them. For A/D's, it describes how close the points that are the transition voltages are to a straight line drawn through them. Figure 45 is a blow-up of the first four levels of the transfer function of Figure 42. The transition voltages, the analog input voltages at which the digital output change from one code to the next, are circled at the left end of each level (one could have just as easily chosen the

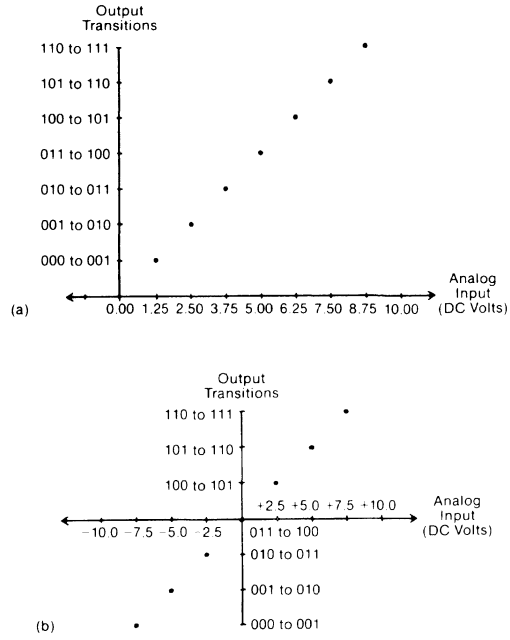


Figure 44. The digital output transitions of Figures 42 and 43 are plotted as a function of input voltage. These plots convey all the information of Figures 42 and 43.

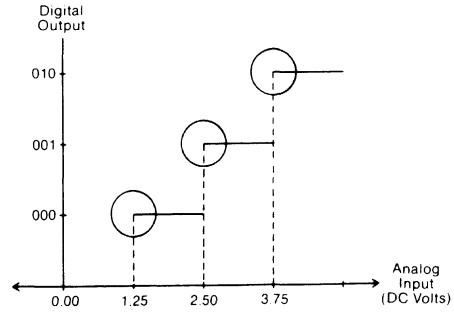


Figure 45. The first 4 transitions of Figure 42 are expanded to clarify what points along the A/D transfer function we are calling the transition voltages.

right ends) and also indicated on the horizontal (analog) axis. These are the points for which linearity has to be tested, and the reference straight line can be drawn according to either an end-point definition or a best-fit definition (see D/A Integral Linearity). A/D Integral Linearity Error is usually expressed in fractions of an LSB (± ¼ LSB, ± ½ LSB, etc.) or in %FSR or ppm's of FSR.

Figure 46 shows a nonlinear, 3 bit A/D transfer function. Some of its bands are wider than 1 LSB; some are narrower than 1 LSB. Figure 47 plots the transition voltages of Figure 46, and Figure 48 shows that the transfer function of Figure 46 has ± ⅜ LSB Linearity Error according to the best-fit definition.

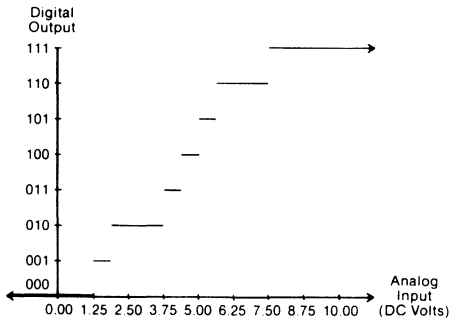


Figure 46. Nonideal, 3 bit, 0 to + 10V input range A/D converter. Output levels greater or less than 1 LSB wide result in an Integral Linearity error.

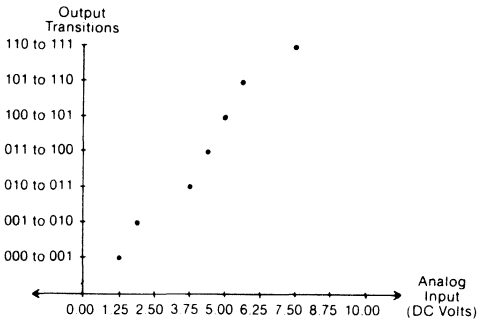


Figure 47. The transition voltages of figure 46 are plotted against analog input.

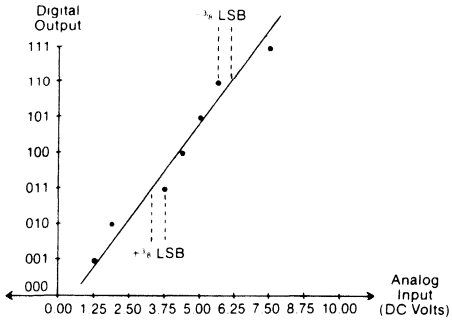


Figure 48. The A/D transfer function fo Figure 46 is shown to have ± ⅜ LSB Integral Linearity according to the best-fit straight line definition.

A few manufacturers have defined Integral Linearity for A/D converters to be the deviation of the "midpoints" of the levels from a straight line drawn through them. Micro Networks does not accept this definition, and Figure 49 demonstrates why. If the 3 bit D/A of Figure 49a were used to construct a 3 bit successive approximation A/D, the A/D's transfer function would look like that shown in Figure 49b. Drawing a straight line through the centers of the levels leads one to conclude that the A/D has perfect linearity, obviously it does not. Figure 49c shows that plotting and drawing a straight line through the transition voltages gives this A/D ± ⅜ LSB Integral Linearity Error (according to the best-fit definition).

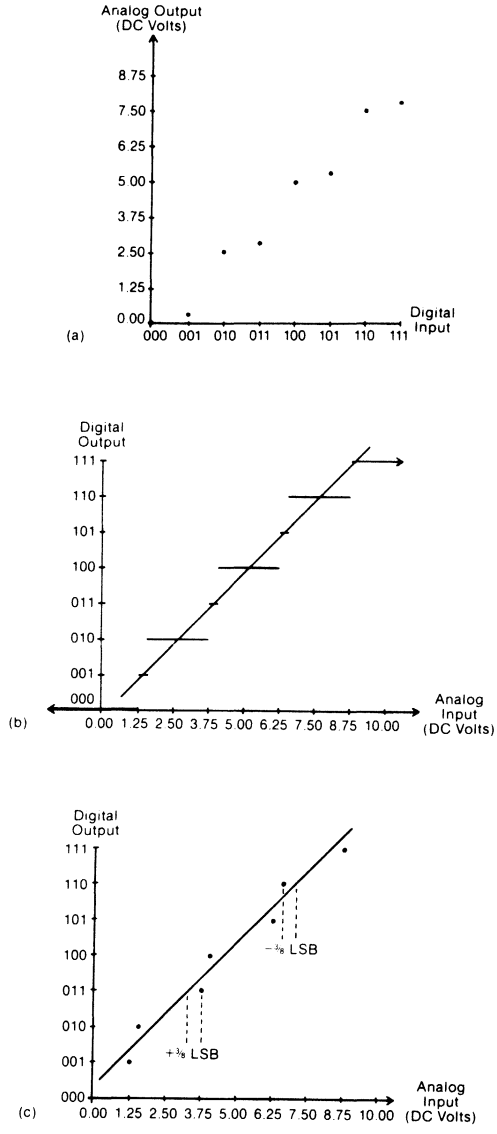


Figure 49. If the 3 bit D/A whose transfer function is shown in (a) is used to make a 3 bit successive approximation A/D, the A/D's transfer function will be that shown in (b). If one uses the midpoints of the levels and not the transition points to test Integral Linearity, this obviously nonlinear A/D would have perfect linearity. (c) shows that when the transition points are used, the device has ± ⅜ LSB linearity according to the best-fit definition.

Micro Networks feels that Integral Linearity is one of the most important A/D converter specifications, and we contend that an n bit converter is not a true n bit converter unless it guarantees at least ± ½ LSB Linearity over whatever temperature range it is to be used. For A/D converters, ± ½ LSB Integral Linearity by either definition will guarantee No Missing Codes and Differential Linearity Error better than ± 1 LSB.

DIFFERENTIAL LINEARITY ERROR—All the steps of the D/A transfer function were supposed to be 1 LSB high. All the levels or bands of the A/D transfer function are supposed to be 1 LSB wide. A/D Differential Linearity Error is a measure of the distance between transition voltages (i.e., a measure of the widths of input voltage bands), with any deviation of the actual "distance" from the ideal 1 LSB appearing as the error. The amount of error is usually expressed in fractions of an LSB.

A maximum Differential Linearity Error of ± ½ LSB means that the "distance" between transition voltages can be as large as 1 LSB ± ½ LSB, i.e., the input voltage may have to increase or decrease as little as ½ LSB or as much as 1½ LSB's before an output transition occurs. See Figure 50. The transfer function of Figure 50 has some levels that are ¼ LSB wide and one that is 1¾ LSB's wide. Its Differential Linearity Error is ± ¾ LSB. Integral Linearity Error better than ± ½ LSB by *either* definition guarantees that Differential Linearity Error will be better than ± 1 LSB, i.e., maximum Differential Linearity Error has an upper bound equal to two times Integral Linearity Error. It can be less than 2X Linearity, however, and some manufacturers may choose to test and specify it as being such. For example, a converter may specify ± ½ LSB Integral Linearity and ± ¾ LSB Differential Linearity. If it specifies ± ½ LSB Integral Linearity and says nothing about Differential Linearity, one can only assume that maximum Differential Linearity will be ± 1 LSB.

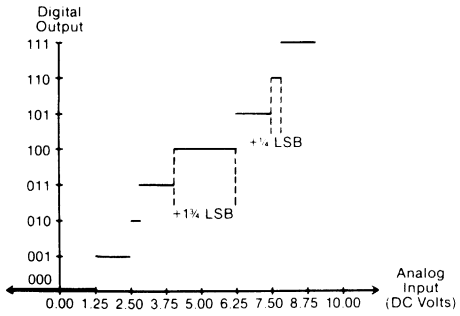


Figure 50. Demonstration of an A/D transfer function with ± ¾ LSB Differential Linearity Error. Some levels are + ¼ LSB wide; others are + 1¾ LSB wide.

Maximum Differential Linearity Error does not allow one to infer anything about Integral Linearity Error. The transfer function of Figure 51 has ± ½ LSB Differential Linearity Error but ± ⅝ LSB Integral Linearity Error. Lastly, what happens if Differential Linearity Error is ± 1 LSB? Some of the levels will be 2 LSB's wide; others will be 0 LSB's wide. Zero LSB's wide means that the level does not exist and that the converter misses a code.

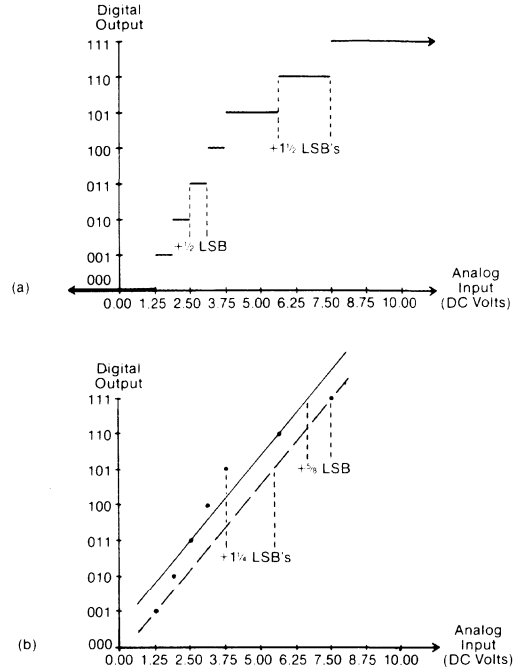


Figure 51. Differential Linearity does not guarantee Integral Linearity. The A/D transfer function shown in (a) has ± ½ LSB Differential Linearity but ± ⅝ LSB Integral Linearity according to the best-fit definition and + 1¼ LSB Integral Linearity according to the end-point definition.

NO MISSING CODES—No Missing Codes is to A/D converters what monotonicity is to D/A converter's (see Monotonicity). There is really no need to specify Monotonicity for successive approximation A/D converters. These devices are monotonic by design; if the input voltage goes up, the output code goes up. The question is how high up does the output go? Does it jump up so high as to miss the next output level? Look at Figure 52. When the input voltage to this

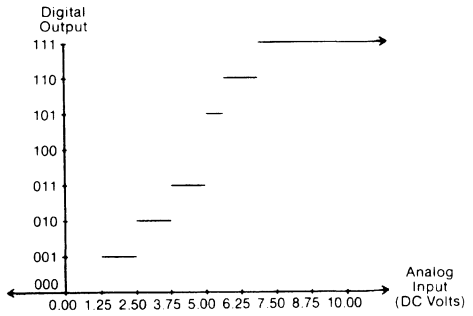


Figure 52. This A/D transfer function shows the digital output going from 011 to 101 as the analog input increases. The code 100 is missing.

converter gets to + 2.5V, the output code becomes 011. The output stays on this code while the input voltage increases to + 3.75V. Now the output changes to the code 101. The code 100 was missed. A successive approximation A/D misses codes when its internal D/A is nonmonotonic. The A/D whose transfer function is shown in Figure 52 was constructed using the D/A of Figure 53. Notice how the nonmonotonic D/A input (100) is the missing A/D code.

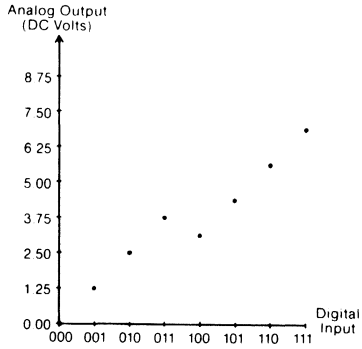


Figure 53. The A/D converter whose transfer function is shown in Figure 52 was built with the nonmonotonic D/A whose transfer function is shown here. The A/D misses a code (100) at the point at which the D/A is nonmonotonic.

Like Monotonicity, No Missing Codes is more a property of a converter than it is a specification. The relevant specification is "the temperature range over which no missing codes is guaranteed". No Missing Codes is an important parameter. One always wants to make sure that all 2^n output codes are achievable for an n bit converter. If an n bit converter misses a code at its major transition (the most likely place for this to occur) it might as well be an (n-1) bit converter.

Remember: ± ½ LSB Integral Linearity will guarantee No Missing Codes and Differential Linearity Error better than ± 1 LSB. However, No Missing Codes and Differential Linearity Error better than ± 1 LSB do not guarantee ± ½ LSB Integral Linearity. Many converters will guarantee No Missing Codes over some temperature range, but they won't guarantee ± ½ LSB Integral Linearity.

INTEGRAL AND DIFFERENTIAL LINEARITY DRIFT—See this section under D/A converters for an explanation of how to calculate the magnitude of Integral and Differential Linearity Drifts over a given temperature range.

A 12 bit A/D converter that guarantees ± ½ LSB (± 0.012% FSR) Integral Linearity Error at + 25 °C and gives an Integral Linearity Drift of ± 1 ppm of FSR/ °C will have an Integral Linearity of ± 0.022% FSR at + 125 °C. ± 0.022% FSR is almost equivalent to 1 LSB for 12 bits (0.024% FSR) or ½ LSB for 11 bits. Therefore, at + 125 °C this converter would only have 11 bit Integral Linearity which would mean that its effective resolution has been reduced to 11 bits. In other words, the manufacturer of this converter is saying that at + 125 °C, Differential Linearity Error can be as bad as ± 2 LSB's (for 12 bits) and that he no longer guarantees No Missing Codes.

Most Micro Networks A/D converters are guaranteed to be ± ½ LSB Linear at room temperature and ± ½ LSB Linear with No Missing Codes over their entire operating temperature range. For converters that don't hold ± ½ LSB Linearity over temperature, we will give a Linearity spec at +25°C and another Linearity spec that applies over the entire operating temperature range. Our MN574AT 12-bit A/D, for example guarantees ± ½ LSB Integral Linearity at room temperature and ± 1 LSB from −55°C to +125°C. A 12-bit A/D converter that guarantees ± ½ LSB Differential Linearity Error at + 25 °C and gives a Differential Linearity Drift of ± 2ppm of FSR/ °C will have a Differential Linearity Error of ± 0.032% FSR at + 125 °C, and ± 0.032% is equivalent to approximately 1 ½ LSB's. At 125 °C this A/D may have missing codes. We say "may have missing codes" because it is possible that the converter transfer function bowed upwards such that the levels got wider and then smaller such that no codes were missed. Normally, however, when this type of drift phenomenon occurs, the manufacturers will be proud of the fact that they have maintained No Missing Codes and will say something to the effect of "No Missing Codes guaranteed over temperature". If such a statement does not appear, a user can only assume that the converter began to miss codes when Differential Linearity exceeded ± 1LSB. At what temperature did that occur for the device mentioned above? At what temperature did its Differential Linearity Drift exceed ± ½ LSB? ± ½ LSB = ± 0.012% of FSR = ± 120ppm of FSR. If Differential Linearity Drift is ± 2ppm of FSR/ °C, it will take 60 °C for the drift to equal ± ½ LSB. Therefore, the converter began to miss codes at + 25 °C + (60 °C) = + 85 °C.

What Differential Linearity Drift would a 12 bit A/D that guaranteed ± ½ LSB Differential Linearity at room temperature (+ 25 °C) have to maintain in order to guarantee No Missing Codes up to + 125 °C? ± ½ LSB = 120ppm of FSR. 120ppm of FSR/ΔT = 120ppm of FSR/100 °C = 1.2ppm of FSR/ °C.

Lastly, recall that ± ½ LSB Integral Linearity guarantees No Missing Codes and Differential Linearity Error less than ± 1 LSB for A/D converters. An A/D that guarantees ± ½ LSB Linearity and No Missing Codes at room temperature and then gives an Integral Linearity Drift specification without specifically stating what happens to Differential Linearity or Missing Codes over temperature is *not* guaranteeing No Missing Codes at any temperature other than + 25 °C.

GAIN ERROR—As was the case with D/A's, A/D Gain Error is a measure of the deviation from the ideal of the slope of a converter's transfer function. The slope of an A/D converter transfer function can be defined as the slope of a straight line from its first transition to its last transition. The slope of the ideal transfer function, as plotted in Figures 42 and 43 is 45 ° or 1. A device with positive Gain Error would have a more steep transfer function. A device with negative Gain Error would have a less steep transfer function. See Figure 54. A/D Gain Error is usually measured by first locating the "first" and "last" transitions of a converter's transfer function. The first

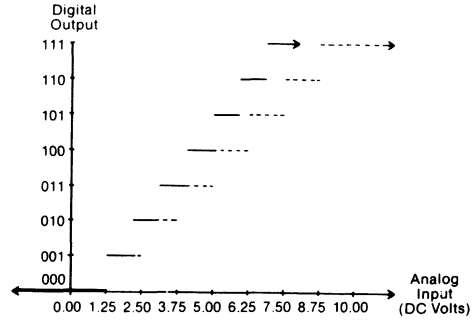


Figure 54. Example of a unipolar A/D transfer function exhibiting positive Gain Error. The ideal transfer function is shown as the broken line.

transition for a unipolar A/D is the one closest to zero for unipolar positive devices and the one closest to the negative full scale point for unipolar negative devices. The first transition for a bipolar device is the one closest to the negative full scale point. The last transition is the last one at the other end of the transfer function. Gain Error is the difference between the real and the ideal values of the full analog interval between these two voltages.

Return to Figure 43. For this A/D, the ideal first transition voltage is −7.5V, and the ideal last transition voltage is +7.5V. The ideal difference between these two points is 15 volts (FSR—2 LSB's). If the transfer function of Figure 43 had an actual first transition at −8.0V and an actual last transition at +7.75V the difference would be 15.75 volts. The difference between the ideal and actual values for this number would be 15.75 − 15.00 = 0.75 volts. Expressed as a percentage, this gives a Gain Error of 0.75/15 = 5%. Note that this is a negative Gain Error, the transfer function would be less steep than ideal. For those who like to express Gain Error in % FSR, the error would be 0.75 volts/FSR = 0.75 volts/20 volts = 3.75% FSR.

Gain Error is not an accuracy measurement, although as you will see, it can be used to calculate an A/D converter's Absolute Accuracy Error when this spec is not given.

RELATIVE ACCURACY—As we stated in the D/A section, Relative Accuracy is a confusing specification, and you will not see it used on a Micro Networks data sheet. It is the data converter specification that has the greatest variety of definitions from different manufacturers. Micro Networks defines the Relative Accuracy of an A/D converter to be the measure of how accurate any of the A/D's transition voltages are *relative* to a straight line drawn between the first and last transitions of the A/D's actual transfer function. Relative Accuracy is usually expressed in (sub)multiples of LSB's or in %FSR, and according to our definition, is exactly the same as Integral Linearity Error according to the end-point definition. Relative Accuracy does not include Gain and Offset Errors (to be discussed).

As a data converter specification, Relative Accuracy has two uses. Firstly, many manufacturers will use it for the purpose of informing a user how accurate, relative to the ideal, he/she can expect his/her A/D to be after its initial Gain and Offset Errors have been adjusted to zero through the use of trimming potentiometers. As an example, take the 3 bit, 0 to +10V A/D of Figure 42. If the manufacturer guarantees Relative Accuracy = ± ½ LSB, and the user adjusts the converter so that its 000 to 001 transition occurs at an input voltage of exactly +1.25 volts and its 110 to 111 transition occurs at an input voltage of exactly +8.75 volts, every other transition voltage will be within ± ½ LSB (± 0.625 volts) of what it is supposed to be. The second use of Relative Accuracy is that some manufacturers will use it in lieu of an Integral Linearity Error spec. This is fine if the intent is not to deceive. We stated earlier that in order for an n bit converter to be a true n bit converter, its Integral Linearity Error should be no worse than ± ½ LSB for n bits. Many times, when Relative Accuracy appears in lieu of Integral Linearity Error, we have noticed the error to be greater than ± ½ LSB. Beware of high resolution (12 bits and up) A/D converters or Data Acquisition Systems that spec "accuracies" better than ± 2 LSB's. As a practical matter, such levels are difficult to achieve in state-of-the-art A/D's without external gain and offset adjustments. The manufacturer probably means Relative Accuracy.

A/D CONVERTERS—ABSOLUTE PERFORMANCE SPECIFICATIONS

ABSOLUTE ACCURACY ERROR—The Absolute Accuracy Error of a voltage input A/D converter is the difference between the actual, *unadjusted,* analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR.

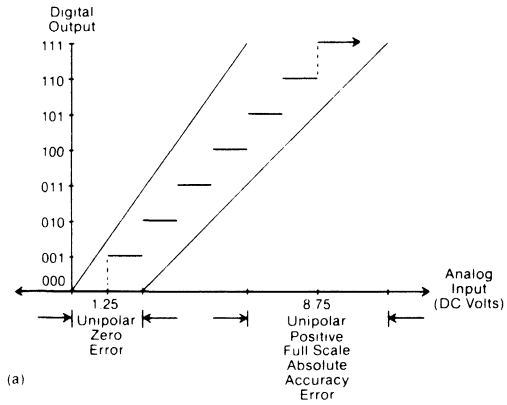
The two key words in this definition are "unadjusted" and "given". "Unadjusted" means just that; an A/D converter's Absolute Accuracy has to be measured before any optional gain and offset adjusting is performed. This is where Absolute Accuracy differs from Relative Accuracy. Absolute Accuracy tells you how accurate your converter is going to be if you simply plug it in, power it up, and start converting. Relative Accuracy tells you how accurate it will be after you go through the gain and offset error adjusting procedure. "Given" refers to the fact that any Absolute Accuracy specification has to be accompanied by some indication of where along the converter's input/output transfer function the spec applies, i.e., for which digital output transition is the Absolute Accuracy of the input voltage to be measured. If no such indication is given, a user can only assume that a given Absolute Accuracy Error spec applies over the converter's entire input/output range, i.e., it applies to every transition. Because Absolute Accuracy Error is measured and specified without adjustment, it includes all factors that may be affecting the converter's accuracy at the point of measurement—Offset Error, Gain Error, Linearity Error, and Noise Error.

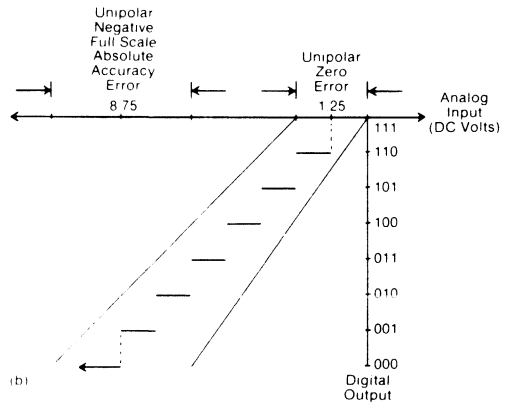
Refer back to Figure 42. Assuming the transfer function is linear, the two key points necessary to fully describe this A/D converter's Absolute Accuracy would be at positive full scale (110 to 111 transition) and at zero (000 to 001 transition). To avoid ambiguity, the specs would be called Unipolar Positive Full Scale Absolute Accuracy Error and Unipolar Zero Absolute Accuracy Error (also called Unipolar Zero Error). Refer back to Figure 43. The three key points necessary to adequately describe the Absolute Accuracy of this device are at positive full scale (110 to 111 transition), negative full scale (000 to 001 transition), and zero (011 to 100 transition). The three relevant specifications are Bipolar Positive Full Scale Absolute Accuracy Error, Bipolar Negative Full Scale Absolute Accuracy Error, and Bipolar Zero Absolute Accuracy Error (also called Bipolar Zero Error).

FULL SCALE ABSOLUTE ACCURACY ERROR—This is the Absolute Accuracy Error measured for the output transition that brings the digital output to the code representing a full scale input. If it is the positive full scale code, some people may refer to the transition as the "last" transition. If it is the negative full scale code (for unipolar negative or bipolar converters) some people may refer to the transition as the "first" transition. We avoid this terminology because in complementary coded converters, it is not clear what first and last transitions mean.

Some manufacturers will draw a distinction between Unipolar and Bipolar Positive and Negative Full Scale Absolute Accuracy Errors. Micro Networks normally does not. For unipolar positive, unipolar negative, or bipolar input ranges, our Full Scale Absolute Accuracy Error specification refers to either the positive or negative full scale point or both, whichever is appropriate. Take our MN5200 and MN5210 Series 12 bit A/D's. These devices offer input ranges of 0 to −10V, 0 to +10V, ±5V, and ±10V, and our data sheet lists a single Full Scale Absolute Accuracy Error. The spec applies for all the full scale output points, i.e., it means Unipolar Positive Full Scale Absolute Accuracy when using the 0 to +10V range, Unipolar Negative Full Scale Absolute Accuracy when using the 0 to −10V range, and both Bipolar Positive and Bipolar Negative Full Scale Absolute Accuracies when using the bipolar ranges. We will list the errors separately if they have different values.

ZERO ERROR—This is the Absolute Accuracy Error measured for the output transition that brings the digital output to the code corresponding to an input of zero volts. Micro Networks will draw a distinction between Unipolar and





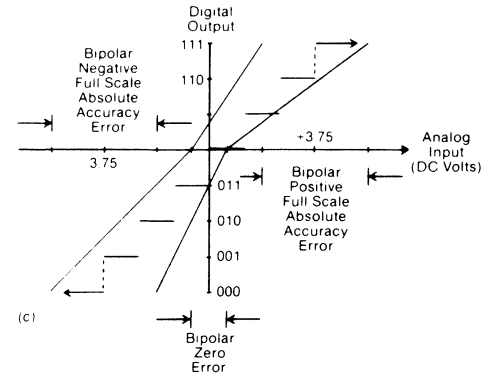


Figure 55. Summary of Full Scale Absolute Accuracy and Zero Errors for unipolar positive A/D converters (a), for unipolar negative A/D converters (b), and for bipolar A/D converters (c).

Bipolar Zero Error for converters that have different values for these two specifications. Otherwise, we simply give a single Zero Error specification.

Full Scale Absolute Accuracy and Zero Error are summarized in Fig. 55. If an A/D converter is linear, i.e., if its Integral Linearity Error is less than ± ½ LSB, the Absolute Accuracy of any transition can be found through interpolation of the Full Scale and Zero Errors as the sketches show. The 3 bit A/D whose transfer function is shown in Figure 56 has a Negative Full Scale Absolute Accuracy Error of – 1.25 volts (– 1 LSB), a Bipolar Zero Error of – 0.625 volts (– ½ LSB), and a Positive Full Scale Absolute Accuracy Error of zero volts. As was explained in the D/A section, Full Scale Absolute Accuracy and Zero Errors are the way in which Micro Networks prefers to specify converter accuracy.

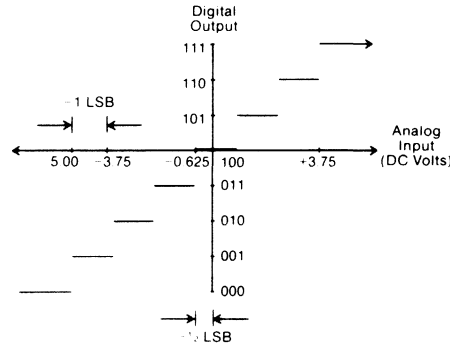


Figure 56. Example of a 3 bit, ± 5V input range A/D converter with a Negative Full Scale Absolute Accuracy of – 1.25 volts (– 1 LSB), a Bipolar Zero Error of – 0.625 volts (– ½ LSB), and a Positive Full Scale Absolute Accuracy Error of zero.

OFFSET ERROR—Micro Networks does not emphasize A/D Offset Error as being an important specification for the same reason we don't emphasize D/A Offset Error. You have to understand the inner workings of an A/D in order to understand exactly where its Offset Error specification applies. Let us simply say that an A/D's Offset Error has to be measured when the D/A internal to the A/D would have its Offset Error measured. The A/D's Offset Error should be measured when the current coming out of the internal D/A is zero. This may occur at the first transition (000 to 001) or it may occur at the last transition (110 to 111); you have to know how the A/D works to know where its Offset Error specification applies.

An A/D's Offset Error is often but not always equivalent to its Zero Error.

An A/D's Offset Error will always be the same as either its Zero Error or its Full Scale Absolute Accuracy Error, and we much prefer these specs, for as we stated previously, we believe that most converter users prefer to think of converters as building blocks with certain input/output characteristics, and they really don't care what goes on inside of them. Many of our data sheets do list Offset Errors, however; the specs are there solely to facilitate comparing our converters to those of other manufacturers who prefer to spec Offset Error.

A/D CONVERTERS —DYNAMIC SPECIFICATIONS

CONVERSION TIME—Conversion Time is exactly that—the time required for an A/D converter to perform a single conversion. For successive approximation A/D's, Conversion Time can be defined as the width of the converter's status output

pulse. See Figure 41. Conversion Time is not equivalent to the time it takes an A/D in a system to produce new valid output data. There are two pitfalls users should be aware of. The first is that for a high percentage of SA type A/D converters, output data is not valid when the converter's status line indicates that the converter is done converting. Normally, due to different propagation delays for high and low signals, the LSB will not achieve its final value until some time after the status changes. This delay is normally only tens of nanoseconds, but if you're not aware of it, you'll get erroneous LSB data when using the status to strobe a register to latch your output data. You may have to add a delay. The other problem occurs at the other end of a conversion, at the start. Most SA type A/D converters don't start the instant a start signal comes along. They reset on a rising clock edge after the start signal has changed levels. There is usually a setup time requirement that says you have to change the start some time before the clock edge, usually tens of nanoseconds. See Figure 41. Oftentimes, the conversion won't continue until the start signal returns to its original level, so you'll want to have it return before the next clock edge or suffer additional delay. The net result of setup time and LSB delay is that it will normally take at least one additional clock period beyond the status period to update valid digital output data.

Another thing users should be aware of is that SA type A/D converters calling for external clocks will require the generation of a precise frequency to achieve the fastest conversion times.

Text and sketches by Chuck Sabolis

Track and Hold Amplifiers

Track and Hold (T/H) and Sample and Hold (S/H) amplifiers are widely used in data acquisition, data distribution, and analog signal processing systems. They are devices that accurately store analog voltages. They could be called "voltage memories". Their single most popular application is to "freeze" the input voltage to an A/D converter at the instant a conversion begins and to hold this voltage constant during the conversion process. In this application as in most, the characteristics of the T/H or S/H are crucial to overall system accuracy, especially in high speed or high resolution systems. Micro Networks manufactures a number of T/H amplifiers. In this section, we will discuss some of the problems encountered in T/H design and operation and explain how Micro Networks has minimized their effects. We will define key T/H specifications and explain what to look for on manufacturers' data sheets. Lastly, we will demonstrate three popular T/H applications: an A/D aperture reducer, a D/A deglitcher, and a peak detector.

WHEN IS A T/H A S/H?

In general, people will use the terms Sample and Hold and Track and Hold interchangeably. There is a distinct difference between the two, however. Both are linear circuits that have three operational terminals and two modes of operation. The terminals are the analog input terminal, the analog output terminal, and the digital control terminal. The operating modes are obviously the track mode and the hold mode for the T/H and the sample mode and the hold mode for the S/H. When a T/H is in the track mode, its output follows or tracks and is equal to its input. When commanded into the hold mode, the T/H's output becomes constant and equal to its input value at the instant the device was commanded into the hold mode. A T/H can remain in either operational state indefinitely. A S/H cannot operate indefinitely in either mode. When commanded to the sample mode, it will take a very fast sample and immediately go back into the hold mode. It normally spends most of its time in the hold mode with its output at some fixed voltage; it cannot track an input signal. A T/H amplifier can be used as a S/H. A true S/H amplifier cannot be used as a T/H. In practice, most sample/hold amplifiers manufactured today are actually track and hold amplifiers. The few true S/H amplifiers made today will clearly be labeled as being such. Figure 1 summarizes the difference between T/H and S/H amplifiers.

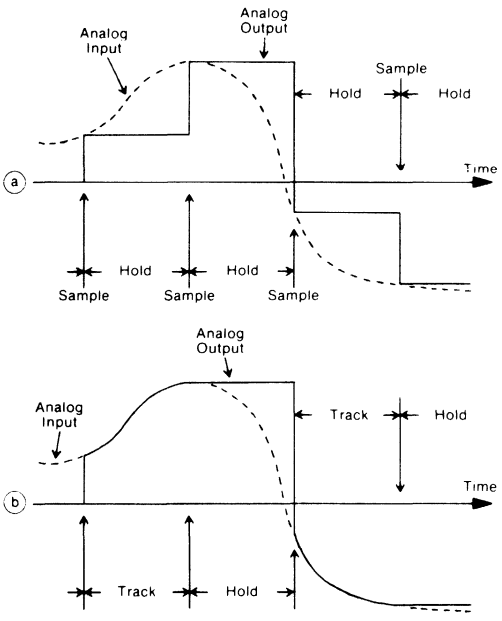


Figure 1. A sample and hold amplifier (1a.) takes a quick sample of the input signal and immediately returns to the hold mode. A track and hold amplifier (1b.) can track the input for part of the time and hold it for the rest of the time. A T/H can remain indefinitely in either operational mode.

THE CIRCUITS AND THEIR PROBLEMS

Figure 2 shows a T/H circuit in its simplest form. The circuit consists of an electronically controlled switch and a hold capacitor. When the switch is closed, the voltage at the input terminal appears across the capacitor, and the output voltage will equal the input voltage. If the input voltage now changes, the capacitor will charge or discharge and the output voltage will follow. When the switch is opened, the capacitor retains its charge and the output voltage remains equal to the input voltage at the instant the switch was opened.

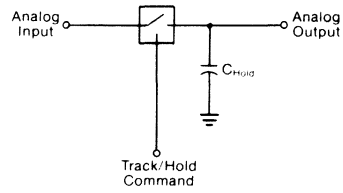


Figure 2. In a simple track and hold circuit, when the switch is closed the output voltage equals the input voltage. When the switch is opened, the capacitor retains its charge and the output voltage remains constant.

The electronic switch is digitally driven. For Micro Networks T/H's, a logic "0" applied to the unit's control input commands the device into the hold mode. A logic "1" commands it to the track mode.

If the electronic switch is a FET, its gate can be driven directly or through an appropriate driving circuit. In either case, the "speed" with which this circuit's analog output can follow its analog input will be determined by the time constant of the switch "on" resistance and the hold capacitor, providing the input is driven from a low impedance source. Adding a fast, high impedance buffer amplifier (voltage follower) in front of the switch not only charges the hold capacitor from a low impedance source, it gives the overall T/H circuit a high input impedance. This is important since in some applications, the T/H will be operating at the output of a high impedance signal source, and the source should not be overloaded. The speed, accuracy, and drive capability of the input buffer will obviously affect the overall response of the T/H circuit, and the buffer should be carefully chosen. The ability of the circuit to hold a voltage will depend on how quickly the capacitor loses its charge after the switch has opened. Since in this example, the capacitor is connected directly to the T/H output, the output loading is important. This condition is eliminated by placing a second buffer (voltage follower) between the hold capacitor and the T/H output. This buffer should be a fast, FET-input device with a very high input

Tutorial

impedance and a low input bias current to prevent hold capacitor charge from leaking off too rapidly. It should also have a low output impedance enabling the T/H to drive relatively low input impedance devices such as most A/D converters (typically 2KΩ to 20KΩ input impedance). Similiarly, to prevent capacitor leakage, the FET switch should have a low "off" leakage, and the hold capacitor should be a low leakage device with a high insulation resistance. Most hybrid T/H's with internal hold capacitors will employ NPO ceramic capacitors. Other acceptable capacitor types are polystrene, polypropylene, polycarbonate, and Teflon. Figure 3 shows the simple circuit of Figure 2 with input and output buffers added.

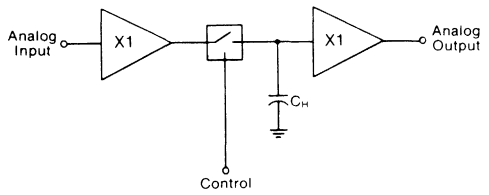


Figure 3. Adding a buffer in front of the switch quickens capacitor charging and gives the T/H high input impedance. Adding a buffer behind the hold capacitor reduces capacitor charge bleeding and output droop.

The track and hold circuit as described so far (Figure 3) can be extremely fast if a fast switch and fast followers are employed. It will be reasonably accurate; however, accuracy will be limited by offset, gain, and linearity errors in the followers as well as by imperfections in the switch. The main problem with the switch is capacitance—both across it from input to output and between its output and its control (gate) input (see Figure 4). Capacitance across the switch (source-drain capacitance in the case of a FET switch) will cause some of the input signal to be coupled through to the holding capacitor even when the switch is off. This is called "feed-through". Capacitance between the switch output and its gate input (gate-drain capacitance in the case of a FET switch) will cause a step or "pedestal" in the hold voltage as the switch is turned off. This pedestal error results from a phenomenon called charge injection or charge dumping. Refer to Figure 4. The gate to drain capacitance of the FET switch couples the switch-control voltage (V_g) on the gate to the hold capacitor. When the switch is turned from on to off, an amount of charge equal in magnitude to C_{gd} times the change in FET gate voltage ($Q = C_{gd} \Delta V_g$) transfers from the hold capacitor to the gate drive circuit. This produces an error in hold voltage equivalent to the product of the step in gate voltage and the gate to drain capacitance divided by the hold capacitance.

$$\Delta V_H = \frac{Q}{C_H} = \frac{C_{gd} \Delta V_g}{C_H}$$

Since increased speed is often obtained by reducing the size of the hold capacitor, pedestal error may become unacceptably high. Compounding this problem in a floating-switch type track and hold such as the one we have been describing, is the fact that the apparent gate signal amplitude will change as the analog signal changes. Return again to Figure 4. The switching voltage applied to the gate of the FET will usually step between two fixed levels, but the instantaneous voltage appearing at the drain of the FET will be equal to V_H and changing all the time. Therefore, the amount of charge injected and hence the magnitude of pedestal error will be a function of the instantaneous analog voltage present on C_H when V_g changes. In other words, pedestal

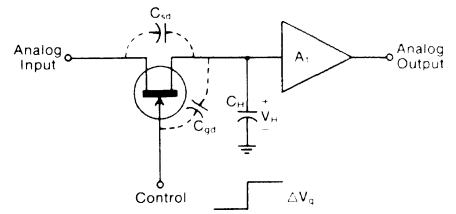


Figure 4. FET source to drain capacitance causes feed-through. Gate to drain capacitance results in charge injection when the FET gate voltage changes causing Pedestal.

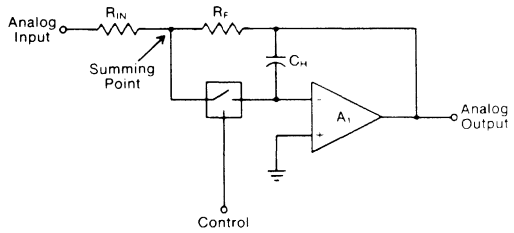


Figure 5. Pedestal amplitude dependence upon input voltage level is eliminated by having the FET drain operate at virtual ground. The drain voltage of the FET in Figure 4 is equal to V_H and changes with input voltage. The circuit above does not eliminate pedestal but keeps it constant.

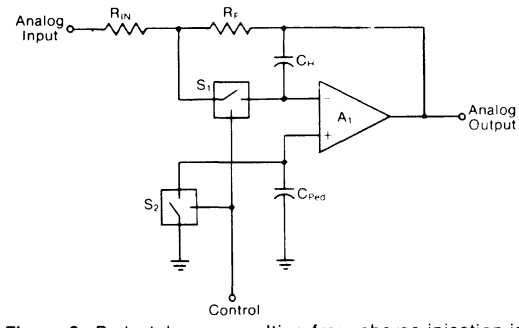


Figure 6. Pedestal error resulting from charge injection is compensated for by adding to the amplifier's non-inverting terminal a switch (S_2) and capacitor (C_{Ped}) circuit the same as the main switch (S_1) and hold capacitor circuit. Equal and opposite charge injections result in pedestal cancellation. c.f. Figure 5.

error, already a problem by its mere presence, will vary in magnitude with analog signal level, possibly in a non-linear manner.

One solution to this problem is to place the switch in the circuit in such a way that it never sees a voltage change while in the track mode. Such a circuit is the "summing-point switch" type track and hold of Figure 5. In its most basic form, the circuit consists of an op-amp wired for inverting gain with a switch between the summing point and the inverting input of the amplifier. The hold capacitor is placed between the amplifier output and its inverting input, where it will acquire the inverse of the analog input signal as long as the switch is closed and R_{IN} equals R_F, i.e., the circuit has unity gain. When the switch is opened, the amplifier becomes, in effect, a unity gain follower with an output offset with respect to the grounded non-inverting input equal to the voltage present on the holding capacitor at the moment the

switch opens. A pedestal will be generated by charge injection as before, but its amplitude will not be a function of the analog input voltage.

Although constant in amplitude, the pedestal generated by a summing-point-switch track and hold may still be unacceptable. It is possible to remove most or all of it by inducing a step of equal amplitude on the non-inverting input of the amplifier. One way to accomplish this is to place a switch of the same type as the summing point switch (S_1) in parallel with a capacitor the same value as the hold capacitor between the non-inverting input and ground (see Figure 6). This auxiliary switch (S_2) is driven by the same gate signal that drives the main switch so that when a hold command is given, equal amounts of charge are transferred into both the holding and pedestal compensation capacitors (C_{Ped}). Any pedestal which still remains due to a slight switch or capacitor mismatch can be eliminated by adjusting the value of the pedestal compensation capacitor.

WHAT ABOUT FEEDTHROUGH?

As previously mentioned, another problem caused by switch capacitance is feedthrough. Switch capacitance induced feedthrough will have an amplitude equal to the summing point signal amplitude times the switch source-drain capacitance (C_{sd}) divided by the hold capacitance (C_H). One means of reducing this effect is to employ a summing point clamp. This may be a FET switch to ground or simply a back-to-back diode pair (see Figure 7) used to restrict the voltage swing at the summing point during the hold mode. If a FET switch to ground is used, it must be turned off while in track to allow the summing point to move slightly. The back-to-back diodes, however, may be left in place at all times since in normal operation the summing point is a virtual ground and need only move small amounts in response to high speed signals. An added benefit of the summing point clamp is that by restricting the voltage swing on the switch input, the gate signal need not move as far to insure complete turn-off under all input/output conditions.

As with pedestal, the only effective means of completely eliminating feedthrough (at least at low frequencies) is to cancel it by injecting a signal of equal amplitude and opposite polarity. This can be done by capacitively coupling the summing point to the non-inverting input of the amplifier, either with a small capacitor (C_{Fdtu} in Figure 7) or by using

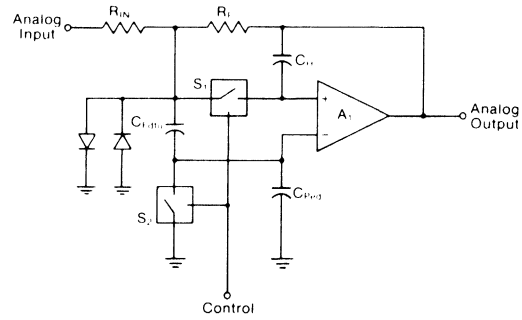


Figure 7. Capacitance coupled feedthrough is reduced with the addition of a back-to-back diode pair to the summing point. The diodes restrict the voltage swing at the summing point while in the hold mode. Capacitively coupling the amplifier non-inverting input to the summing point with a capacitor (C_{Fdtu}) equal in magnitude to C_{sd}(see Figure 4) effectively eliminates this component of feedthrough.

another switch of the same type as the main switch permanently wired in the off state.

The switch is not the only path for feedthrough; some input signal can travel directly to the output through the feedback resistor. In this case it is the ratio of the feedback resistor to the output impedance of the amplifier that determines feedthrough amplitude. Also, feedback path induced feedthrough will be in phase with the input while summing point switch feedthrough will be out of phase. It is the feedback path feedthrough that will tend to dominate at higher frequencies as the output impedance of the amplifier increases. This type of feedthrough is very difficult to cancel, and may therefore be a limiting factor in high speed track and holds. The only way to combat it, besides using a faster amplifier, is to use larger feedback resistors. This procedure, while reducing feedthrough, may also affect speed by increasing the time constant with any capacitance associated with the summing point.

So far in the discussion, it has been assumed that when the main switch (S_1) is closed, the summing point drives the hold

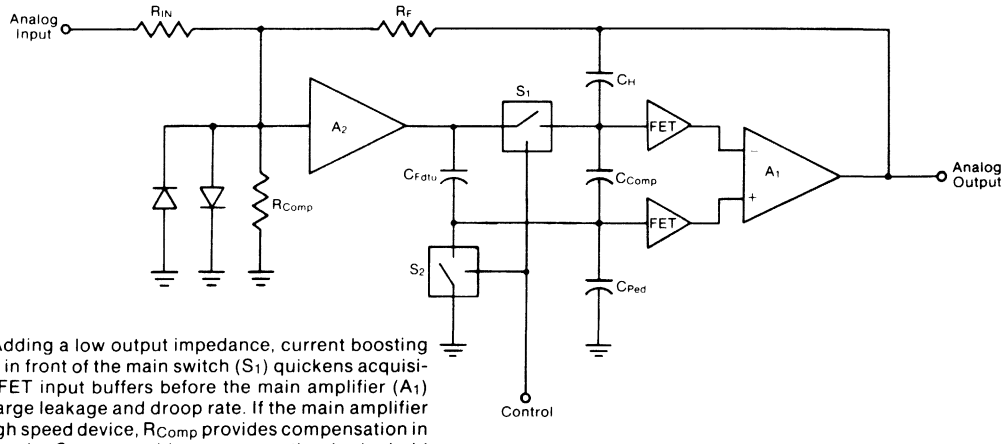


Figure 8. Adding a low output impedance, current boosting buffer (A_2) in front of the main switch (S_1) quickens acquisition time. FET input buffers before the main amplifier (A_1) reduce charge leakage and droop rate. If the main amplifier (A_1) is a high speed device, R_{Comp} provides compensation in the track mode. C_{Comp} provides compensation in the hold mode. This is the basic circuit employed in MN343, MN344, MN346 and MN347 T/H amplifiers.

capacitor directly. This condition may limit the speed of the device since the time constant generated by the holding capacitor and the feedback resistor (together with the on-resistance of the switch) will determine the time required by the track and hold to aquire the input to any given accuracy. Return to Figure 5. With $R_F = 2K\Omega$ and $C_H = 2000_pF$ (assume R_{on} for the FET is negligible compared to the $2K\Omega$) $\tau = R_F C_H = 4\ \mu Sec$. Therefore, to charge C_H to within 0.01% (½ LSB for a 12 bit converter) of its final value will take about 9 time constants or 36 μsec.

Reducing the feedback resistors and/or reducing the value of the hold capacitor may improve speed but only by sacrificing performance in the areas of feedthrough and pedestal. One solution is to insert a voltage follower (A_2) into the feedback loop, i.e., between the summing point and the switch (see Figure 8). It is now this amplifier and not the main amplifier that provides the current to charge the hold capacitor. The hold capacitor can now acquire a voltage at a rate determined by the output current capability of the follower, providing the slew rate of the main amplifier and its output drive capacity are sufficient. Output settling time can still be limited by capacitance at the summing point, but its value is now greatly reduced and consists mainly of the summing point clamp and follower input capacitance.

Adding the buffer allows us to increase the values of R_{IN} and R_F which in turn reduces feedback path induced feedthrough and increases T/H input impedance.

WHAT ABOUT THE HOLD MODE?

Once the track and hold has aquired a desired voltage, it must be able to hold it for a reasonable length of time to within given limits of drift. The main cause of any change in output voltage will be a loss of charge from the hold capacitor to the virtual ground at the inverting input of the amplifier. Leakage from the pedestal compensation capacitor, if used, to the non-inverting input node of the amplifier will have a similar effect but in the opposite direction. Assuming the off-resistance of the switches used is very high, most of the leakage will be into the amplifier inputs. This can be reduced considerably by placing suitable FET input followers in front of the amplifier (see Figure 8). The followers, however, will lose their effectiveness somewhat at higher temperatures due to the doubling of gate leakage experienced by FET's every 10° C. Capacitor characteristics such as leakage and dielectric absorbtion or "soakage" will add to the problem, so choose carefully. The net effect versus time of hold capacitor charge loss is termed "droop rate."

TIMING, WHEN IS THE T/H REALLY HOLDING?

We said earlier that the T/H's FET switches are driven from an "appropriate driving circuit." Switching the track and hold from one mode to the other involves converting the logic "1" or "0" at the unit's control input (usually TTL or ECL) to a driving signal capable of opening or closing the appropriate switches. The output of the driving circuit (gate circuit) will depend on what types of switches are to be driven and may even involve two or more outputs delayed so as to activate switches in a predetermined sequence. Sequential switching may be required when, for example, the main summing point switch must be opened prior to applying an active summing point clamp so as to avoid the large step that would result from grounding a "live" summing point. The gate circuit must act quickly, with whatever delay that does exist being as consistant as possible. The length of the gate circuit delay can be compensated for to some extent by adding analog input delay or possibly by advancing the control input slightly. However, variations in gate circuit delay will result in errors since the analog signal may change significantly over the period of time during which the T/H is actually moving into the hold mode. The slope of the output of the gate circuit is also important, as it may determine how quickly the switch itself takes to turn off. Speed is critical here for the same reason that consistency in gate delay is important: it is needed to pinpoint the exact time at which the analog input is held. In spite of all these considerations, the chain of events set in motion by activating the gate circuit is not ended even when all the switching has been done. When switching into "track", the analog input must still be aquired; and when switching into "hold", the output must settle in response to being hit with any residual pedestal and/or spikes generated by the switching process.

A discussion of the factors governing the selection of the main amplifier (A_1 in Figures 4-8) might prove useful at this point. The main amplifier is undoubtedly the most important element in determining the overall speed and accuracy characteristics of the track and hold, and it will usually consume most of the power. Its slew rate may limit the slew rate of the track and hold, and in any case, will determine the upper limit of the current output requirements placed on the follower driving the hold capacitor (see Figure 8). As mentioned previously, the output impedance of the main amplifier will have a marked effect on feedthrough, especially at the higher frequencies. The amplifier's settling time will be the limiting factor in determining the settling time of the whole circuit; however, delays in the feedback loop will also have an effect here. It is quite often the case that the faster amplifiers will not be unity gain compensated and must be run at higher gains to achieve their specified settling times. In order for the track and hold to maintain stability and an overall gain of one (or at least minus one), some form of frequency compensation must be applied. While in the "track" mode, compensation can be applied to the summing point in the form of a resistor to ground (R_{Comp} in Figure 8). The value is selected so that its ratio to the value of the feedback resistor gives the closed loop gain required to maintain stability and best settling time. Since this internal loop gain will increase any offset by the same amount, a capacitor is sometimes inserted in series with the compensation resistor to eliminate it from the loop at low frequencies and D.C. where compensation is not needed. When in the "hold" mode, compensation can be applied by means of a capacitor between the inverting and non-inverting inputs of the amplifier (C_{Comp} in Figure 8). Once again its value is chosen to give the required gain when compared in value with the holding capacitor. This capacitor will, of course, have no effect on offset but may affect speed slightly.

SPECIFICATION DEFINITIONS

Specific definitions of terms have not been stressed so far in this discussion. This was done in the belief that definitions would have more meaning after the operation of the track and hold circuit as a whole had been presented. Although the definitions of the terms used to describe various effects are quite important, there appears to be some ambiguity and even some difference of opinion when it comes to interpreting actual manufacturers' data sheets. Terms containing the word "aperture" appear to be particularly confusing and are rarely clearly defined. The following list contains what are believed to be the most logical and often used definitions for the terms given, at least when they are applied to sample and hold and track and hold circuits. Refer to Figure 9 for clarification.

ACQUISITION TIME The elapsed time between the application of a "track" command and the point at which the analog output has arrived at within a specified percentage of its final value. Acquisition time will include gate delay, amplifier settling time, and any time spent slewing between voltages. Because of slew rate limitations, actual acquisition time will depend upon the amplitude of the voltage change to be acquired. When specifying acquisition time, both the analog output step size and the permitted error band must be given.

For the MN343 and MN346, for example, Micro Networks specifies Acquisition Time for a 20 volt step settling to within ±0.01% FSR of its final value.

APERTURE The time required by the main signal-path switch to change from a low-impedance state to a high-impedance state, thereby placing the circuit in the "hold" mode. It is determined by the gate circuit output slew rate and/or by the characteristics of the switch itself and does not include other gate circuit characteristics such as gate delay (see Aperture Delay). While normally short enough to be neglected, it will affect the precision with which the exact point at which the hold mode begins can be known. Aperture is rarely specified on manufactures' data sheets. When it does appear, the manufacture invariably means Aperture Delay.

APERTURE DELAY, APERTURE TIME, APERTURE TIME DELAY The time lag between the application of the "hold" command and the instant the output stops tracking the input. "Stops tracking" can be defined as being able to meet the feedthrough attenuation specification. Aperture Delay is determined primarily by the switch drive circuit and includes aperture.

APERTURE JITTER A rapid and random fluctuation in Aperture Delay brought about by noise in the gate circuit. It will appear as a variation in Aperture Delay from sample to sample. Errors resulting from aperture jitter will increase in direct proportion to the slope of the analog input signal.

APERTURE TIME Equivalent term for Aperture Delay.

APERTURE UNCERTAINTY Sometimes used synonymously with Aperture Jitter, Aperture Uncertainty should also include middle and long-term fluctuations in Aperture Delay brought about by the combined effects of temperature, aging, and digital input speed and amplitude on the gate circuit.

CHARGE INJECTION, CHARGE TRANSFER, CHARGE DUMPING In a T/H or S/H, Charge Injection is the phenomenon of moving a small amount of charge from the main signal path switch to or from the hold capacitor during switch turn-off. It is caused by the change in switch controlling voltage being coupled through switch capacitance to the hold capacitor. It is the cause of Pedestal.

DROOP RATE The rate of change in output voltage with time while in the hold mode. Droop results from charge lost by the hold capacitor and pedestal compensation capacitor (if used) to the input nodes of the main amplifier. Droop rate will normally change with temperature, and therefore should always be specified at a given temperature. Micro Networks specifies maximum droop rates over fixed temperature ranges.

FEEDTHROUGH The amount of analog input signal coupled through to the analog output while the circuit is in the hold mode. It may have any phase relationship with the input and will normally increase at higher frequencies.

FEEDTHROUGH ATTENUATION The ratio of feedthrough amplitude to the analog input signal amplitude while in the hold mode. It is usually expressed in dB's with the most negative values being, of course, the most desirable. It should be specified at a given frequency or as a function of frequency. A graph is preferable.

FULL POWER BANDWIDTH, LARGE SIGNAL BANDWIDTH The frequency at which a full scale input /output sine wave becomes slew rate limited.

GAIN, GAIN ACCURACY The ratio of the change in analog output voltage to the change in analog input voltage while in the track mode. Gain Accuracy refers to how close the slope of the T/H's input/output transfer function approximates the slope of the ideal transfer function. Positive or negative unity gain is most common for track and hold circuits, but any value is possible.

GATE DELAY Equivalent term for Aperture Delay.

LINEARITY The maximum deviation from the best-fit straight line approximation to the input/output transfer function of the track and hold. Linearity is usually expressed as a

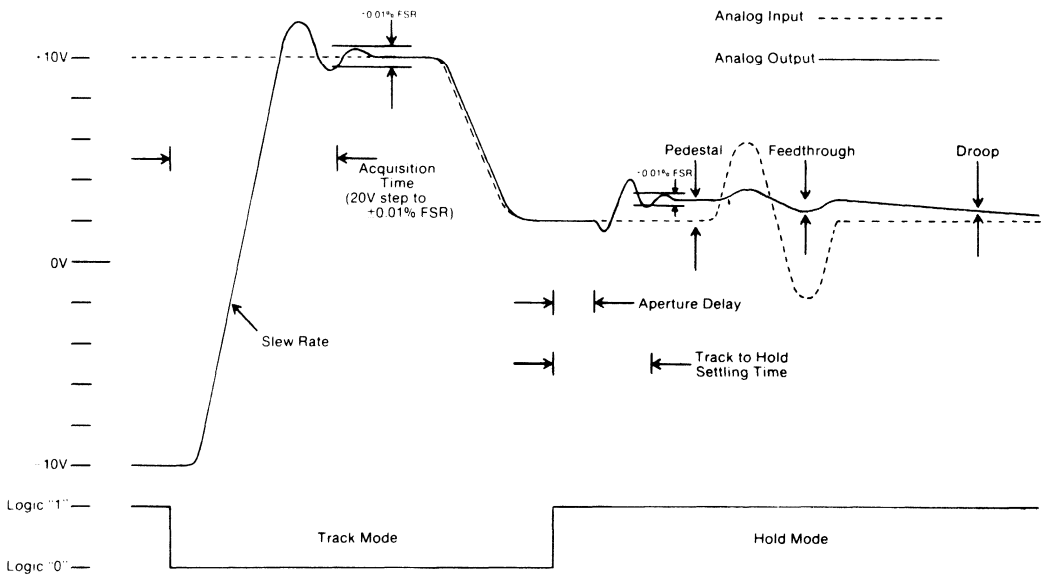


Figure 9. Summary of T/H specifications. The broken line is the T/H's analog input. The solid line shows its analog output. The T/H has a ±10V analog input range. The lower trace is the digital T/H command signal. A logic "O" puts the T/H into the track mode. A logic "I" puts it into the hold mode. Refer to the text for the specification definitions.

percentage of the T/H's full-scale voltage swing. A T/H used in an n bit system should be linear to within ±½ LSB for n bits.

OFFSET (TRACK MODE) The D.C. voltage appearing at the analog output while in the track mode with the analog input grounded. It will usually be temperature dependant, and this dependance should be specified. To avoid confusion, Micro Networks calls this parameter Track Offset or Sample Offset. Offset (Hold Mode) or Hold Offset refers to the voltage with respect to ground appearing at the output immediately after the circuit is commanded into the hold mode with the input grounded. Hold Offset can be as large as Track Offset plus Pedestal Error.

PEDESTAL An unwanted D.C. step in the output voltage occurring as the circuit is driven into the hold mode. It is the result of unequal charge transfer to the input nodes of the main amplifier during the switching operation. It may also be called Sample to Hold or Track to Hold Offset.

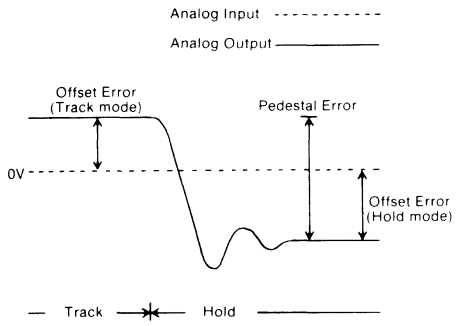


Figure 10. Summary of Offset (Track Mode), Offset (Hold Mode) and Pedestal Errors. Broken line is T/H analog input. Solid line is analog output. Analog input level equals zero volts.

SAMPLE AND HOLD A linear circuit capable of holding the instantaneous value of its analog input signal present at the moment a "sample" command is given. The circuit is normally in the "hold" mode and cannot "track" an input. Output droop prevents the circuit from holding a signal idefinitely.

SAMPLE RATE The maximum frequency at which a complete sample and hold operation can be performed while remaining within specified accuracy limits. It will be the inverse of the period determined by adding Acquisition Time and Track to Hold Settling Time.

SETTLING TIME (TRACK MODE) The time required for the track and hold output to stabilize in the track mode to within specified limits of its final value following a step change applied at the analog input.

SETTLING TIME (TRACK TO HOLD) The time required for the track and hold output to stabilize in the hold mode to within specified limits of its final value following the transition from the track mode.

SLEW RATE The maximum rate of change in voltage with respect to time that the analog output is capable of developing while attempting to track the input. The slope will usually be determined either by the main amplifier or by the current available for charging the holding capacitor. Slew rate will limit the full power bandwidth of the track and hold.

SMALL SIGNAL BANDWIDTH The maximum analog signal frequency that can be tracked before the gain is reduced by more than 3db. This presumes the signal amplitude is small enough so as not to be slew rate limited.

SUMMING POINT The point in the feedback loop of a summing-point-switch type track and hold circuit (see Figure 5) which is connected to the inverting input of the main amplifier to produce the inverting gain configuration required for tracking. It can also be used as a current-to-voltage input to the circuit, which can be convenient in some applications.

TRACK AND HOLD A linear circuit capable of holding the instantaneous value of the analog input signal present at the moment a "hold" command is given. The circuit can remain indefinitely in either mode, however, output droop will cause the accuracy of a held voltage to decrease with time.

APPLICATIONS

There are two basic types of applications for which track and hold circuits are normally used. One is the situation in which the instantaneous value of a rapidly changing analog signal must be stored temporarily so it can be measured or operated on by equipment with limited bandwidth. The other arises when it is desirable to eliminate some portion of an analog signal by holding a previous value during the interval in question.

An example of the first type is the use of a track and hold circuit at the input of an analog to digital converter. If the analog input of a Successive Approximation A/D Converter changes by more than ±½ LSB during the conversion interval, significant errors may result. To enable an A/D converter to accurately convert the instantaneous value of a high speed input signal, a track and hold is used in front of the A/D. It is timed to acquire the signal, track it, and hold it when necessary for as long as it takes to complete a conversion. With this arrangement, the A/D converter "sees" only the droop rate of the track and hold circuit, which usually is not a problem with relatively high speed A/D's.

An example of the second type is a D/A Deglitcher. When converting a digital signal into analog form, a D/A converter may produce spurious spikes or "glitches" in the analog output. These spikes are normally due to non-synchronous switching of current sources. In some applications these glitches may detract from overall circuit performance and must therefore be removed. One way to accomplish this is to follow the D/A converter with a track and hold circuit which is placed in the hold mode just before the digital inputs of the D/A are permitted to change state. It is then returned to the track mode when sufficient time has elapsed to insure the D/A analog output has settled to its new value. If the D/A converter is a current-output type, this output can often be fed directly into the summing point of the track and hold circuit. With this arrangement, the track and hold can be made to double as a current-to-voltage amplifier.

A third often mentioned application of track and hold circuits is in a peak detector. This is a circuit capable of storing the highest (or lowest) values an analog signal reaches during a given period of time. At first glance it seems quite simple to build, but real-world operating characteristics make the track and hold based peak detector a fairly difficult design problem.

The basic circuit consists of comparing the input and output of the track and hold with a voltage comparator and using the comparator output to control the gate (see Figure 11). When the input of the track and hold exceeds the output, the comparator selects the track mode. If the input falls below the output, the hold mode is selected and the previous peak is stored. Reversing the inputs of the comparator will reverse the polarity of the stored peak. A possible variation on this design involves comparing the summing point of the track and hold (if available) with ground.

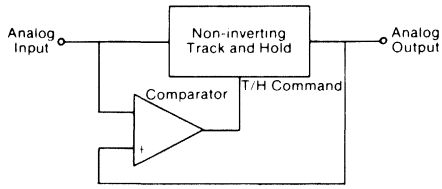
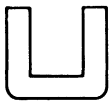


Figure 11. A T/H can be used to make a peak detector. The comparator compares the T/H's input and output. When the T/H input exceeds its output, the comparator selects the track mode. If the input falls below the output, the comparator selects the hold mode and the peak is stored.

Unfortunately, the circuit just described doesn't always work. One problem is that if the comparator does not select the hold mode whenever the input equals the output, the circuit will remain in track forever. To overcome this, the comparator input offset must be set to insure hold is selected when its inputs are equal. Too much offset will, however, produce an offset error in the held peak value. A more serious problem can result from hold pedestal. If pedestal polarity is such that it forces the comparator to go back into track immediately following the switch into hold, the output will oscillate around the input value and it will be impossible to hold a peak. For this reason, the pedestal polarity must always be in the same direction as the peak being held. This makes reversing the polarity of the peak detector difficult, since it is usually not practical to reverse the pedestal of the track and hold. Transients following a track command may result in errors if the track and hold is told to hold before it has settled. For this reason, a "pulse stretcher" should be used between the comparator and the logic input of the track and hold which will delay the hold command during the track-mode settling time. Speed will of course be limited by the pulse stretcher delay. A delay of five microseconds, for example, will result in a maximum speed of about 1KHz for 0.05% accuracy.

This discussion about peak detectors is given to illustrate some of the problems actually encountered when using track and hold circuits. (There are, in fact, better ways to construct peak detectors than by using a comparator with a track and hold, but they will not be dealt with here.) Track and hold circuits can be very useful in many designs, but an understanding of their problems and limitations is crucial in avoiding misapplication.

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Sampling A/D Converters

MN6000 Series Sampling A/D Converters

MN6000 Series Sampling A/D Converters are complete, single-package, high-resolution (12-16 bits), analog-to-digital (A/D) converters with internal, user-transparent, high-speed track-hold (T/H) amplifiers. This mating of Micro Networks proven A/D and T/H expertise is complimented by new testing and specification techniques that make MN6000 Series A/D's ideally suited for the repetitive sampling and digitizing of rapidly changing analog signals in "signal-processing" types of applications.

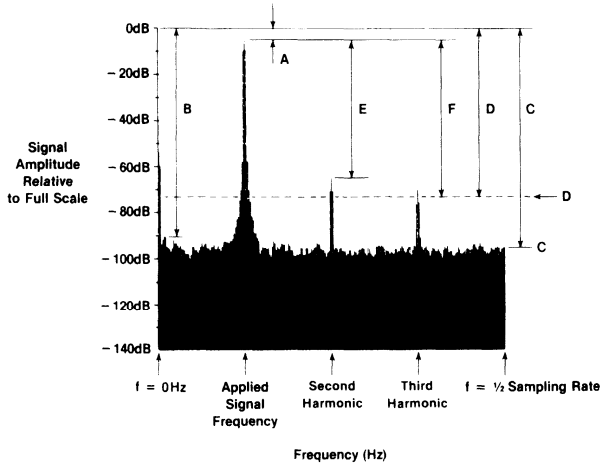
The A/D-converter sections of the products in this Series all use the successive-approximation (SA) A/D conversion technique. This approach has been proven to be the most practical for performing high-speed, high-resolution A/D conversions because of the excellent tradeoffs it offers in terms of speed, resolution, power consumption and size. The SA conversion technique, however, is notoriously poor in its ability to accurately convert dynamically changing (slewing) analog input signals. In fact, SA type A/D converters, by themselves, are effectively incapable of accurately converting anything other than d.c. signals. This inherent shortcoming is normally overcome by employing external T/H amplifiers in front of the A/D converters to track the changing input signal and instantaneously "freeze" it whenever an A/D conversion is to be performed. MN6000 Series A/D's now move the T/H internal to the A/D and eliminate it as a design concern.

For each A/D in the Series, the internal high-speed T/H amplifier is completely user transparent. The T/H's input is isolated from the outside world by either a high-impedance input buffer or a series resistor to a virtual ground. The output of the T/H is electrically compatible with and internally connected directly to the input of the A/D converter, and the operational state of the T/H is internally controlled by the A/D's status line. The need for potentially confusing T/H timing specifications like acquisition time, aperture delay, aperture jitter, etc. has been completely eliminated. MN6000 Series A/D's need only be clocked at the appropriate sampling rate, and all T/H timing parameters are accommodated.

Concerning test and specification techniques, traditional, essentially static, techniques for testing and specifying the relative-accuracy characteristics of A/D converters (integral linearity, differential linearity, no missing codes, etc.) have proven to be inappropriate and frequently inadequate for understanding the true dynamic "signal processing" capabilities of sampling A/D converters. That problem has now been overcome thanks to recently developed digital-signal-processing (DSP) technologies that enable us to easily evaluate the true, frequency-domain, signal-processing capabilities of sampling A/D's while operating them under dynamic-input conditions.

Each A/D in the MN6000 Series is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point Fast Fourier Transforms (FFT's). In the resulting spectra, signal level (rms), noise level (both peak and rms), signal-to-noise ratio (SNR, rms-to-rms) and harmonic distortion measurements are calculated, and each parameter is fully specified and guaranteed for each device over each operating temperature range. And all dynamic performance specifications are guaranteed while operating the A/D's at their maximum sampling rates with analog input signal frequencies up to the Nyquist limit (input frequency equal to ½ the sampling rate).

All A/D's in the MN6000 Series are packaged in 28 or 32-pin ceramic dual-in-lines. Resolutions range from 12 to 16 bits, with SNR performance ranging from 68dB to 84dB. Guaranteed harmonic distortion levels run as low as −88dB. All devices operate from ±15V and +5V supplies. Each device type within the Series offers assorted grades of temperature and electrical performance and optional high-reliability screening to MIL-STD-883 as described in the selection guide and individual device data sheets.



Sample Spectrum

512-point FFT; Hanning windowing; 10 spectra averaged

Vertical axis normalized for 0dB equal to full scale (r.m.s.). For an A/D with a ±10V input range, 0dB equals 7.07V r.m.s.

Horizontal axis equals 256 frequency bins. Each bin equals (sampling rate) ÷ 512Hz.

A = Signal amplitude (r.m.s.) relative to full scale (0dB)

B = Peak (spurious) noise level

C = Average noise level (noise floor)

D = R.m.s. noise level

E = Signal to harmonics

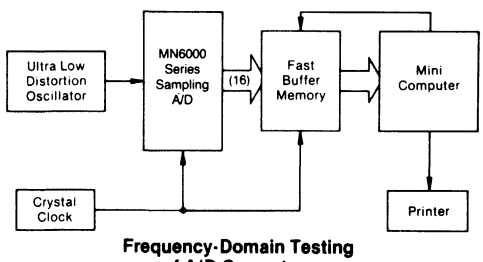
F = Signal to noise ratio (r.m.s.-to-r.m.s.)

INTERNAL T/H AMPLIFIER—The proliferating use of A/D converters in DSP applications has resulted in significantly greater demands on A/D's to be able to convert dynamic signals, particularly sinusoids. More and more frequently, T/H amplifiers are used with A/D's to enable them to accomplish this task.

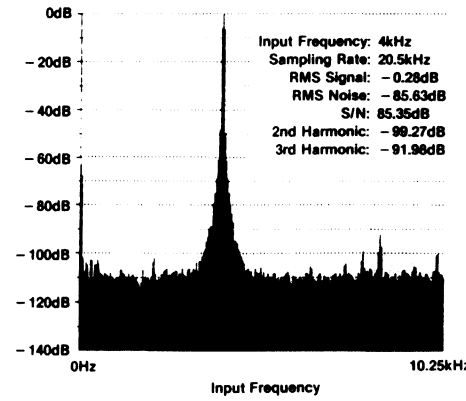
MN6000 Series A/D's are extremely user friendly. They have been configured in a manner that virtually eliminates all of the problems encountered when mating T/H's and successive approximation A/D's and driving the pair from real-world signal sources. The T/H is truly transparent. Either a high-impedance input buffer or a series resistor isolates it from the external signal source, and its output is internally connected directly to the input of the A/D converter. The output-current, impedance and transient-response characteristics of each T/H have been optimized for driving its respective SA A/D. More importantly, the critical dynamic characteristics of the T/H (aperture delay, aperture jitter, small and large signal bandwidths, droop rate, etc.) have been similarly optimized. However, most importantly, the critical inter-device timing relationships (T/H mode control, transient decay time, etc.) are all internally controlled by the A/D's timing and control circuitry. All that users need to provide externally is a start convert pulse.

The value of the hold capacitor used in each internal T/H has been selected so that T/H output droop, even over temperature, is not significant (greater than ± ½LSB) during the A/D's conversion time. Similarly, the offset and pedestal voltages, as well as the gain error, of the T/H do not contribute to the overall accuracy of the sampling A/D because each is effectively nulled out during our active laser trimming of the A/D converter.

FREQUENCY-DOMAIN TESTING—As stated earlier, all MN6000 Series A/D's are specified and tested statically, in the traditional manner (linearity, accuracy, offset error, current drains, etc.), and dynamically in the frequency domain. In the dynamic tests, the sampling A/D is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics −100dB) is used to generate a pure, full-scale, full-frequency sine wave that the A/D samples and digitizes at its specified maximum rate. The conditions are set to approach the Nyquist sampling limit (at least 2 samples per signal cycle; sampling frequency greater than 2 times signal frequency). A total of 512 sample-and-convert operations are performed, and the digital output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are read from the spectrum. A functional block diagram of the test setup and a sample spectrum appear below.



Frequency-Domain Testing of A/D Converters



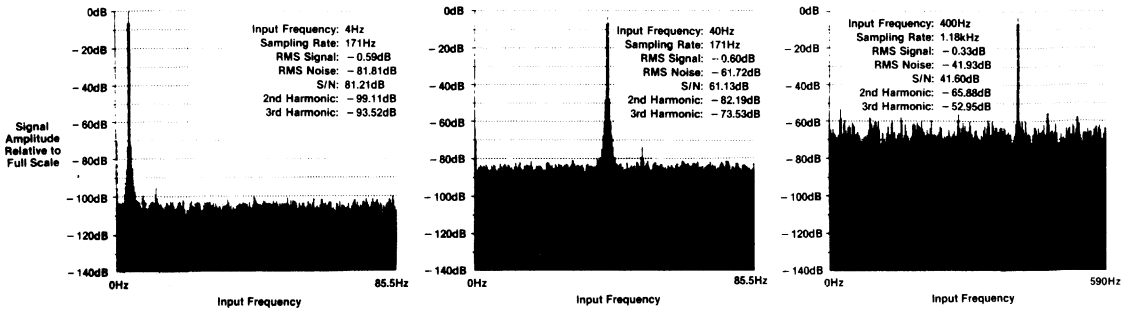
The spectrum shown is the real portion (imaginary portions of spectra are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate. The horizontal axis is divided into 256 frequency bins, each with a width of (sampling rate)/512. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

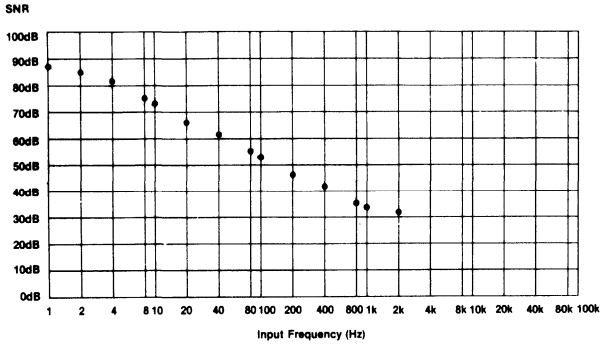
The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). Full-scale rms signals do not appear at −3dB levels because our FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the sampling A/D combined with that of the signal generator and test fixture. Second, third and higher-order harmonics, if they were either present in the input signal or created by the sampling A/D, appear respectively at 2f, 3f, etc.. Depending upon the frequency of the applied signal, the harmonics may or may not be aliased back into the spectrum. Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level to the strongest harmonic or spurious (nonharmonic) signal in the spectrum. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to the rms noise.

The term "noise" is generally used to describe what remains in the ouput spectrum after all fundamental, harmonic, d.c. and outstanding spurious components have been removed. It generally appears across all frequency bins at some relatively flat level sometimes referred to as the "noise floor". The rms noise, as described above, represents the broadband noise that would appear superimposed on the sinusoidal input signal if that signal were perfectly recreated from the stored digital output data. Virtually all the noise in the output spectrum is created either by the act of digitizing or by the A/D converter itself.

In a simple, first-order analysis, the noise in the output spectrum of an A/D converter can be traced to three sources. All three of these noise sources have the potential to manifest themselves as quasi-random relative-accuracy errors in any single A/D conversion of a static signal and subsequently, the potential to manifest themselves as broadband noise in a series of conversions of a dynamically changing signal. Two of these sources (quantization noise and converter noise) are effectively constant and do not change with input-signal frequency. The third (aperture noise) usually varies linearly as a function of input-signal frequency, basically doubling whenever input frequency doubles.

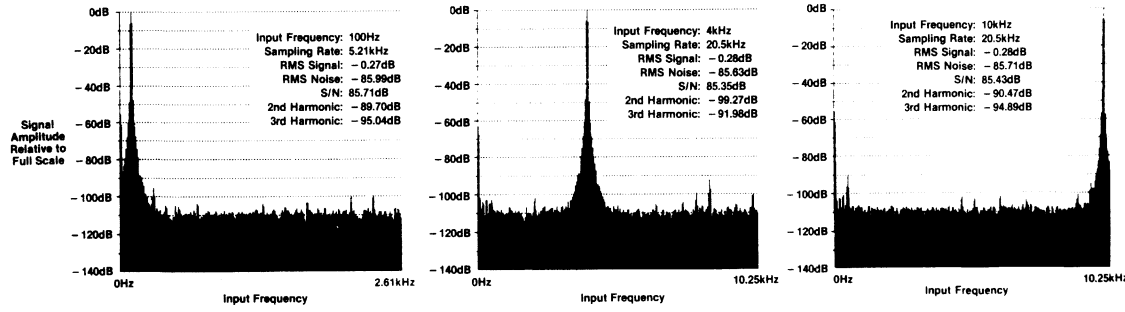
Effective Resolution v.s. Input Frequency
MN5290, 40μsec, 16-Bit A/D

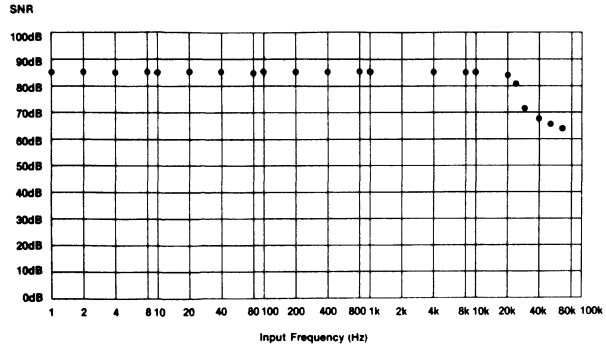




The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN5290 type 16-bit A/D converter without a companion T/H amplifier. The input signal frequencies are respectively 4Hz, 40Hz, and 400Hz. The A/D's conversion time is approximately 40μsec, and the sampling rates are respectively 171Hz, 171Hz, and 1.18kHz. The accompanying plot shows the rapid (6dB/octave) degradation of SNR (effective resolution) with increasing input frequency when SA type A/D converters are used to digitize dynamically changing input signals without the aid of a T/H amplifier.

Effective Resolution v.s. Input Frequency
MN6290, 20kHz, 16-Bit, Sampling A/D





The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN6290 16-bit sampling A/D. The input signal frequencies are respectively 100Hz, 4kHz, and 10kHz, and the sample/convert rates are respectively 5.21kHz, 20.5kHz, and 20.5kHz. The accompanying plot shows that MN6290's internal T/H amplifier enables the device to maintain near ideal SNR independent of increasing input frequencies. The aperture jitter of the T/H is small enough to maintain SNR for undersampled input frequencies, i.e., for frequencies greater than 10kHz.

Digitizing an analog signal quantizes it or "rounds it off". Digitizing or quantizing an analog signal with a 16-bit A/D effectively "rounds off" the signal to one of 65,536 possible discrete levels. This rounding off produces an inherent accuracy error in that the digital output no longer **exactly** represents the analog input. If one has an ideal A/D converter with all other accuracy-error sources driven to zero, the actual value of rounding-off error or quantization error can be as small as zero or as large as ± ½LSB from conversion to conversion. In a single conversion of a static input signal, quantization error is simply an accuracy error. It is impossible for a given conversion of an unknown signal to be more accurate than ± ½LSB. In a series of conversions of a dynamically changing signal, actual instantaneous quantization error varies from sample to sample and manifests itself as broadband noise. In the output spectrum, this noise limits the theoretically achievable signal-to-noise ratio to the following:

Ideal SNR=(6.02n+1.76) dB
n=number of bits

For an ideal 16-bit A/D, the theoretical noise floor in a 512-point FFT occurs around −122dB, and the theoretical SNR is 98dB. For an ideal 14-bit A/D and a 512-point FFT, the numbers are −110dB and 86dB respectively.

The second type of single-conversion accuracy error that manifests itself as broadband noise in the output spectrum results from the actual noise of the A/D converter itself. This "converter noise" is frequently referred to as "transition noise", and it manifests itself, among other ways, by allowing certain fixed, static, input signals to produce either of two adjacent output codes from one conversion to the next. In most A/D converters, the transition from one given digital output code to the next (or vice versa) does not always occur at exactly the same analog input voltage. The "transition voltage" varies from conversion to conversion, and this "transition noise" (the band of adjacent-code uncertainty) is normally on the order of ± 1/10 to ± 1/3LSB. It is caused by broadband noise and timing jitter in the A/D's constituent components (especially its comparator and reference circuit). In a single given A/D conversion, transition noise adds (or subtracts) to the device's static differential linearity error. Again, this phenomenon will manifest itself as an accuracy error in any single conversion and as noise in any series of conversions of a changing input signal.

The second noise component should be thought of simply as the "converter noise." Recall that quantization noise is a result of the digitizing process, and it limits SNR to some theoretical value. Its effect is independent of the type or kind of A/D converter used. Converter noise is a function of how "noisy" a selected A/D converter may be, and it reduces actual measured SNR's to a number less than the theoretical ideal.

The third component of A/D converter noise derives from the fact that SA type A/D converters (without companion T/H amplifiers) cannot accurately convert dynamically changing input signals. Because of the nature of the technique of successive approximations, it is imperative that A/D's using this technique maintain a stable input signal during their conversion (aperture) time. Slew rates in excess of (± ½LSB)/(conversion time) can cause accuracy errors in any individual conversion. In a series of conversions of a sinusoidal signal, the signal slew rate varies from sample to sample, and the consequent aperture (slew-rate) errors manifest themselves as broadband noise.

This third component of A/D noise is effectively eliminated by the sampling A/D's internal T/H. The T/H's ability to instantaneously freeze the slewing input signal (limited only by the T/H's aperture jitter) and hold it constant results in the A/D seeing a series of d.c. signals and not the sinusoid itself. The ability of MN6000 Series A/D's to maintain SNR over their full input bandwidth (up to the "Nyquist frequency" or ½ the sampling rate) is the result of their T/H's ability to limit the overall noise to the quantization noise plus the noise inherent in the A/D.

The plots on the previous page demonstrate that an A/D without a companion T/H is effectively incapable of accurately converting analog input signals above some critical frequency (slew rate) and that the A/D's SNR or "effective resolution" deteriorates at approximately 6dB/octave above that frequency. Basically, the A/D's quantization and converter noise remain constant while its aperture noise doubles each time the input frequency doubles.

The internal T/H's of MN6000 Series A/D's effectively eliminate aperture noise allowing the A/D's to maintain "low-frequency SNR" as the actual input frequency increases.

The plot below graphically illustrates the principles we have been discussing and focuses on A/D converter noise, not on SNR. Earlier, we discussed quantization noise (η_Q), converter noise (η_C) and slew rate or aperture noise (η_A) and how each individually contributes to broadband noise in an A/D's output spectrum. The plot below illustrates the relationship of the three noise components to each other as input signal frequency increases. If each of the three noise components is expressed in rms terms, the total rms noise (η_T) of the A/D converter will be the square root of the sum of the squares of its respective noise components. The vertical axis of the plot is the rms value of the A/D converter's total noise expressed in dB. The horizontal axis is the frequency of the A/D's analog input signal plotted on a logarithmic scale.

At very low (approaching d.c.) input frequencies, aperture noise effectively makes no contribution, and the total noise is equal to the rms summation of quantization noise and converter noise. As explained earlier, this initial noise level is greater than that solely attributable to theoretical quantization noise and is a constant term in the total rms noise equation shown below.

η_Q = Quantization Noise
η_C = Converter Noise
η_A = Aperture Noise (slew-rate noise)

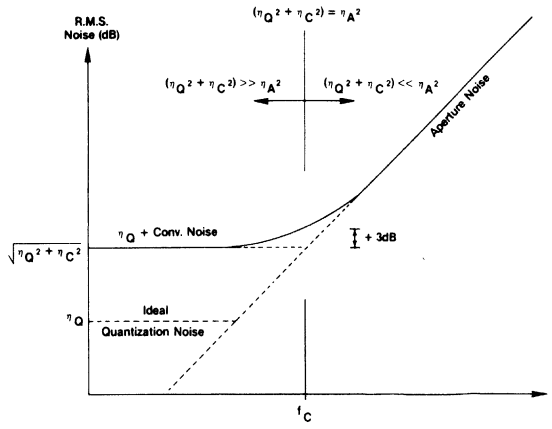
$$\eta\text{Total (rms)} = \sqrt{\eta_Q(\text{rms})^2 + \eta_C(\text{rms})^2 + \eta_A(\text{rms})^2}$$

$$\eta_T = \sqrt{(\eta_Q^2 + \eta_C^2) + \eta_A^2}$$

Constant Term

Frequency Dependent Term

As the input frequency increases, aperture noise begins to come into play. At some critical frequency (f_C), the contribution made by aperture noise will be equal to that of quantization plus converter noise, and the total noise will have risen 3dB above its initial value (SNR drops 3dB). Aperture noise increases 6dB for every octave increase in input frequency and eventually overwhelms the other noise compoents which have essentially remained constant. If one maintains a constant input level while increasing the input signal frequency through many decades, the plot of the A/D's SNR vs. input frequency should look like the inverse of the noise plot shown above. This is demonstrated in the actual plots of SNR vs. frequency for the MN5290 shown previously.



Sampling Analog-to-Digital Converters

Micro Networks Sampling A/D converters are complete, single-package, 8 to 16-bit resolution analog-to-digital converters with internal, user-transparent track-hold (T/H) amplifiers. The mating of our A/D converters designs with their companion T/H amplifiers and our proven specification techniques make these devices ideally suited for digitizing dynamic analog signals in many signal-processing type applications. These devices feature ease of use, internal user-transparent T/H amplifiers and FFT specification and testing.

New products include devices with 8, 12 and 16-bit resolution with sampling rates ranging from 40kHz to an impressive 500MHz. At 8-bits, we offer the MN6900 (500MHz sampling rate) and the MN6901 (250MHz sampling rate) each with an internal T/H amplifier. At 12-bits, new products include the ADS574 and ADS774 monolithic sampling A/D converters and the ADS7800. These devices digitize at 40kHz, 125kHz and 333kHz respectively. The ADS574 and ADS774 are sampling versions of the industry-standard ADC574 and ADC774 A/D converters. At 16-bit resolution, Micro Networks introduces additions to the MN6400 Family of self-calibrating Sampling A/D converters. The MN6405, MN6450 and MN6500 offer different data output formats (8X2 bytes, 16-bit parallel and serial) making them compatible with any high-resolution application.

ADS574
ADS774

12-Bit Monolithic
Sampling A/D Converters

FEATURES

- Internal T/H Function
- Complete with Internal:
  - Reference
  - Clock
  - Microprocessor Interface
- Single +5V Supply Operation
- High-Speed Sampling:
  - 40kHz (ADS574)
  - 125kHz (ADS774)
- Industry Standard Pinout Compatible with ADC574 and ADC774 Converters
- Guaranteed Static and Dynamic Performance
- Package Options: 0.6" and 0.3" DIPs, SOIC
- Low Power Consumption

MN6400 Family

50kHz, 16-bit
Self-Calibrating
Sampling A/D Converters

FEATURES

- 16-Bit No Missing Codes
- 50kHz Sampling Rate (47kHz, MN6450)
- Inherent Sampling Function
- Data Output Bus Driver (MN6400, MN6450)
- Complete — Contains:
  - T/H Function
  - Analog Input Buffer
  - Reference
  - Timing and Control Logic
  - μP Interface
- ± 1 LSB Intergral Linearity Error
- Fully Specified 0°C to +70°C (J and K Models)
  −55°C to +125°C (S and T Models)
- Small DIP Packaging:
  - MN6400, 28-Pin DIP
  - MN6405, 24-Pin DIP
  - MN6450, 32-Pin DIP

MN6900/MN6901

500MHz/250MHz
8-Bit
Sampling A/D Converters

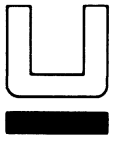
FEATURES

- Ultra-High-Speed Sampling Rates:
  - 500MHz (MN6900)
  - 250MHz (MN6901)
- High Effective Number of Bits (ENOB):
  - 7.0 Bits @250MHz (MN6900)
  - 6.8 Bits @125MHz (MN6901)
- 50Ω Input
- ± ½ LSB Integral Linearity Error
- Dual Interleaved Output Data Paths
- Latched ECL Data Outputs
- $<10^{15}$ Metastable Rates

Sampling Analog-to-Digital Converters

Resolution	Model Number	Input Voltage Range		Specified Temperature Range(°C)	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics	DIP Pkg.	DESC SMD (5962-)	Page No.
		Unipolar	Bipolar								
16-Bits	MN6500	0 to +5V 0 to +10V	±5V ±10V	0 to +70 -55 to +125	100kHz	50kHz	88dB	-96dB	24 Pin	Note 2	5-103
	MN6400	0 to +5V 0 to +10V	±5V ±10V	0 to +70 -55 to +125	50kHz	25kHz	88dB	-98dB	28 Pin	9177001	5-79
	MN6405	0 to +5V 0 to +10V	±5V ±10V	0 to +70 -55 to +125	50kHz	25kHz	88dB	-98dB	24 Pin	Note 2	5-87
	MN6295 MN6296	0 to +10V N.A.	±5V ±10V	0 to +70 -55 to +125	50kHz	25kHz	84dB	-88dB	32 Pin	8998301 8998302	5-71
	MN6450	0 to +5V 0 to +10V	±5V ±10V	0 to +70 -55 to +125	47kHz	23.5kHz	88dB	-98dB	32 Pin	Note 2	5-95
	MN6290 MN6291	0 to -10V N.A.	±5V ±10V	0 to +70 -55 to +125	20kHz	10kHz	84dB	-88dB	32 Pin	Note 2	5-59
12-Bits	MN6249	N.A.	±2.5V ±5V	0 to +70 -55 to +125	2MHz	1MHz	68dB	-72dB	40 Pin	Note 2	5-53
	ADS7800	N.A.	±5V ±10V	0 to +70 -55 to +125	333kHz	150kHz	68dB	-74dB (Note 1)	24 Pin	N.A.	5-33
	ADS774	0 to +10V 0 to +20V	±5V ±10V	0 to +70 -55 to +125	125kHz	50kHz	69dB	-72dB (Note 1)	28 Pin	N.A.	5-21
	MN6774	0 to +5V 0 to -10V	±5V ±10V	0 to +70 -55 to +125	100kHz	50kHz	70dB	-80dB	28 Pin	Note 2	5-109
	ADS574	0 to +10V 0 to +20V	±5V ±10V	0 to +70 -55 to +125	40kHz	20kHz	69dB	-72dB (Note 1)	28 Pin	N.A.	5-9
	MN6227 MN6228	0 to +10V N.A.	±5V ±10V	0 to +70 -55 to +125	33kHz	16.5kHz	70dB	-80dB	28 Pin	8998401 8998402	5-41
8-Bits	MN6900	N.A.	±270mV	0 to +70	500MHz	1.2GHz	45dB	N.A.	84 Pin (Quad)	N.A.	5-117
	MN6901	N.A.	±270mV	0 to +70	250MHz	1.2GHz	45dB	N.A.	84 Pin (Quad)	N.A.	5-129

NOTES: 1. Specification listed is for Total Harmonic Distortion.
2. Contact the factory for information regarding DESC SMD's for these device types.
✓ Indicates New Product.



MICRO NETWORKS



MICRO NETWORKS

324 Clark St., Worcester, MA 01606 (508) 852-5400

MICRO NETWORKS

ADS574

25μsec, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- **Low Cost**
- **Pin-Compatible with MN574/674/774**
- **Eliminates External S/H in Most Applications**
- **Complete, 25μsec, 12-Bit A/D Converter with Internal**
  - **Clock**
  - **Reference**
  - **Control Logic**
- **Full 8- or 16-Bit μP Interface:**
  - **3-State Output Buffer**
  - **Chip Select, Address Decode**
  - **Read/Write Control**
- **No-Missing-Codes Guaranteed Over Temperature**
- **Single +5V Supply Operation**
- **Low Power: 120mW Max**
- **Package Options**
  - **0.3" Plastic DIP**
  - **0.3" Hermetic DIP**
  - **0.6" Plastic DIP**
  - **0.6" Hermetic DIP**
  - **SOIC**

DESCRIPTION

The ADS574 is a complete, low-cost, 12-bit successive-approximation A/D converter with an internal sample/hold function. In most existing applications, it is drop-in compatible with non-sampling 574 types, and eliminates the need for an external S/H amplifier. The ADS574 uses an innovative, capacitor-array internal D/A converter, based on CMOS technology. The use of a CMOS architecture results in much lower power consumption and the ability to operate from a single +5V supply (the formerly required −12V or −15V supply is optional, depending on the application).

The ADS574 is complete with internal clock, reference, control logic, and 3-state output buffer. The interface logic provides for easy handshaking with most popular 8- and 16-bit microprocessors. The ADS574's 3-state output buffer connects directly to the μP's data bus, and is readable as either one 12-bit word or two 8-bit bytes. Chip select, chip enable, address decode (for short cycling), and read/write (read/convert) control inputs enable the ADS574 to connect directly to a system address bus and control lines, and to operate totally under processor control.

Internal scaling resistors allow a pin-selectable choice of four input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. The maximum throughput time (including both acquisition and conversion) for 12-bit conversions is 25μsec over the full operating-temperature range. The ADS574 is available for operation over the commercial (0°C to +70°C) and military (-55°C to +125°C) temperature ranges. Package options include 28-pin single (0.300) or double (0.600) plastic or hermetic ceramic DIPs, and 28-pin plastic SOIC. For availability of devices screened to MIL-STD-883, consult factory.

Model Number	Package	Temperature Range	Linearity Error Max (T_{min} to T_{max})
ADS574JE	0.3" Plastic DIP	0°C to +70°C	±1LSB
ADS574KE	0.3" Plastic DIP	0°C to +70°C	±½LSB
ADS574JP	0.6" Plastic DIP	0°C to +70°C	±1LSB
ADS574KP	0.6" Plastic DIP	0°C to +70°C	±½LSB
ADS574JU	SOIC	0°C to +70°C	±1LSB
ADS574KU	SOIC	0°C to +70°C	±½LSB
ADS574JH	0.6" Ceramic DIP	0°C to +70°C	±1LSB
ADS574KH	0.6" Ceramic DIP	0°C to +70°C	±½LSB
ADS574SF	0.3" Ceramic DIP	−55°C to +125°C	±1LSB
ADS574TF	0.3" Ceramic DIP	−55°C to +125°C	±¾LSB
ADS574SH	0.6" Ceramic DIP	−55°C to +125°C	±1LSB
ADS574TH	0.6" Ceramic DIP	−55°C to +125°C	±¾LSB

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ADS574 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	
J, K Grades	−40°C to +85°C
S, T Grades	−55°C to +125°C
Specified Temperature Range:	
J, K Grades	0°C to +70°C
S, T Grades	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} to Digital Ground	0 to −16.5V
V_{DD} to Digital Ground	0 to +7V
Analog Ground to Digital Ground	±1V
Control Inputs (CE, CS, A_0, 12/8, R/C) to Digital Ground	−0.5V to V_{DD} to +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Ground	±16.5V
$20V_{IN}$ to Analog Ground	±24V
Ref Out	Indefinite Short to Ground, Momentary Short to V_{DD}
Junction Temperature	+165°C
Lead Temperture (Soldering, 10 sec)	+300°C
Thermal Resistance Θ_{JA}: Ceramic	50°C/W
Plastic	100°C/W

ORDERING INFORMATION

PART NUMBER — **ADS574 T H**

Select suffix J, K, S or T for desired performance and specific temperature range.

Select suffix E, F, H, P or U for desired package option.

DESIGN SPECIFICATIONS ALL UNITS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, f_S = 40kHz, f_{IN} = 10kHz) (unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	15	21		kΩ
0 to +20V, ±10V	60	84		kΩ
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Current	−5	0.1	+5	μA
Input Capacitance		5		pF
DIGITAL OUTPUTS DB0 to DB11, Status				
Output Coding: Unipolar Ranges		Straight Binary		
(Note 1) Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" (I_{SOURCE} = 500μA)	+2.4			Volts
Logic "0" (I_{SINK} = 1.6mA)			+0.4	Volts
Leakage (DB0 to DB11) in High-Z State	−5	0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output Voltage (Pin 8)	+2.4	+2.5	+2.6	Volts
Available Output Source Current	0.5			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: V_{EE} Supply (Note 2)	−16.5		V_{DD}	Volts
Power Supply Range: V_{DD} Supply	+4.5		+5.5	Volts
Current Drains: I_{EE} (V_{EE} = −15V)		−1		mA
I_{DD}		+13	+20	mA
Power Dissipation V_{EE} = 0V to +5V		65	100	mW
DYNAMIC CHARACTERISTICS				
Sampling Rate (Max)	40			kHz
Aperture Delay t_{AP}				
With V_{EE} = +5V		20		nsec
With V_{EE} = 0V to −15V		4.0		μsec
Aperture Uncertainty (Jitter)				
With V_{EE} = +5V		300		psec rms
With V_{EE} = 0V to −15V		30		nsec rms
CONVERSION TIME (Including Acquisition Time)				
t_{AQ} + t_C at 25°C:				
8-Bit Cycle		16	18	μsec
12-Bit Cycle		22	25	μsec
12-Bit Cycle, T_{MIN} to T_{MAX}		22	25	μsec

PERFORMANCE SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, f_S = 40kHz, f_{IN} = 10kHz unless otherwise indicated)

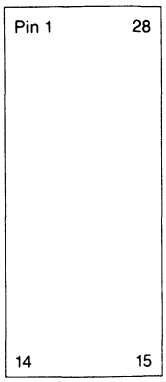
GRADE	ADS574J, S			ADS574K, T			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
RESOLUTION			12			12	Bits
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At 25°C:							
Linearity Error			±1			±½	LSB
Unipolar Offset Error (Notes 3, 4)			±2			±2	LSB
Bipolar Offset Error (Notes 3, 5)			±10			±4	LSB
Full-Scale Calibration Error (Notes 3, 6, 7)			±0.25			±0.25	%FSR
Inherent Quantization Uncertainty		±½			±½		LSB
T_{MIN} to T_{MAX}:							
Linearity Error: J, K, Grades			±1			±½	LSB
S, T Grades			±1			±¾	LSB
Full-Scale Calibration Error:							
Untrimmed: J, K Grades			±0.47			±0.37	%FSR
S, T Grades			±0.75			±0.5	%FSR
Trimmed to Zero at 25°C: J, K Grades			±0.22			±0.12	%FSR
S, T Grades			±0.5			±0.25	%FSR
Resolution for No Missing Codes	12			12			Bits
TEMPERATURE COEFFICIENTS (Note 8)							
Unipolar Offset			±5			±2.5	ppm/°C
Max. Change Over Temperature:			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max. Change Over Temperature: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration			±45			±25	ppm/°C
Max Change Over Temperature: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
AC ACCURACY (Note 9)							
Spurious-Free Dynamic Range	73	78		76	78		dB
Total Harmonic Distortion		−77	−72		−77	−75	dB
Signal-to-Noise Ratio	69	72		71	72		dB
Signal-to-(Noise+Distortion) Ratio (SINAD)	68	71		70	71		dB
Intermodulation Distortion (f_{IN1} = 10kHz; f_{IN2} = 11.5kHz)		−75			−75		dB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration (Note 10) +4.75V < V_{DD} < +5.25V			±½			±½	LSB

SPECIFICATION NOTES:

1. See table of transition voltages in section labeled Digital Output Coding.
2. The use of V_{EE} is optional. This input sets the mode for the internal sample/hold circuit. When V_{EE} = −15V, I_{EE} = −1mA typ; when V_{EE} = 0V, I_{EE} = ±5μA typ; when V_{EE} = +5V, I_{EE} = +167μA typ.
3. Adjustable to zero with external potentiometer.
4. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when the ADS574 is operating with a unipolar range. The ideal value for this transition is +½LSB. See section labeled Digital Output Coding.
5. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when the ADS574 is operating with a bipolar range. The ideal value for this transition is −½LSB. See section labeled Digital Output Coding.
   Listed specs assume a fixed 50Ω resistor between Ref Out (Pin 8) and Ref In (Pin 10) and a fixed 50Ω resistor between Ref Out (Pin 8) and Bipolar Offset (Pin 12) in bipolar configurations; or Bipolar Offset grounded in unipolar configurations. Full-scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. The ideal value for this transition is 1½LSBs below the nominal full-scale voltage. See section labeled Digital Output Coding.
7. FSR is a full-scale range. For the ±10V input range, FSR is 20V. For the 0 to +10V input range, FSR is 10V.
8. Temperature coefficient specifications assume the use of the internal reference.
9. Specifications assume V_{EE} = +5V, which starts a conversion immediately upon a Convert command. If V_{EE} = 0V to −15V, the ADS574 emulates standard ADC574 operation. In this mode, the internal sample/hold circuit acquires the input signal after receiving the Convert command, and does not assume that the input level had been stable before the arrival of the Convert command.
10. Worst-case change in accuracy, compared with accuracy with a +5V supply.

Specifications are subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	+5V Supply ($+V_{DD}$)	28	Status Output
2	Data Mode Select 12/$\overline{8}$	27	DB11 (MSB)
3	Chip Select $\overline{CS}$	26	DB10 (Bit 2)
4	Byte Address A_0	25	DB9 (Bit 3)
4	Read/Convert R/$\overline{C}$	24	DB8 (Bit 4)
6	Chip Enable CE	23	DB7 (Bit 5)
7	No Connect*	22	DB6 (Bit 6)
8	+2.5V Ref Out	21	DB5 (Bit 7)
9	Analog Ground	20	DB4 (Bit 8)
10	+2.5V Ref In	19	DB3 (Bit 9)
11	Mode Control V_{EE}	18	DB2 (Bit 10)
12	Bipolar Offset	17	DB1 (Bit 11)
13	10V Input	16	DB0 (LSB)
14	20V Input	15	Digital Ground

*No Internal Connection

DESCRIPTION OF OPERATION

The ADS574 is a complete 12-bit A/D converter. It uses the successive-approximation conversion technique and incorporates all required function blocks — capacitor-array D/A converter, comparator, clock, reference, and control logic. The CMOS-based capacitor-array architecture provides an inherent sample/hold function; the ADS574 is thus a sampling equivalent of the industry-standard 574 A/D converter. The device mates directly to most popular 8-, 16-, and 32-bit microprocessors and contains all the necessary address-decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most cases, the ADS574 will require only a power supply, a bypass capacitor, and two resistors to provide the complete A/D conversion function. The completeness of the device makes it most convenient to think of the ADS574 as a function block with specific input/output transfer characteristics; it is thus quite unnecessary to be concerned with its inner workings.

Operating the ADS574 under microprocessor control (note that it also functions as a stand-alone A/D) entails, in most applications, a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D, and also involves a write operation. Once the proper signals have been received and a conversion has begun, the ADS574 cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the ADS574's Status Output (also called Busy Line or End-of-Conversion (EOC) Line) rises to logic "1", indicating that a conversion is in progress. At the end of a conversion, the internal control logic will cause the Status Output to drop to 0, and will enable internal circuitry to allow reading output data by external command. By monitoring the state of the Status Output or by waiting an appropriate period of time, the microprocessor will know when the conversion is complete and that output data is valid and ready to be read.

If the ADS574 interfaces with 12-bit or wider microprocessors, it is possible to 3-state-enable all 12 output bits simultaneously, allowing data collection with a single read operation. If the ADS574 operates with an 8-bit processor, output data can be formatted to read in two 8-bit bytes. The first byte will contain the 8 most-significant bits (MSBs). The second byte will contain the remaining 4 least-significant bits (LSBs), in a left-justified format, with 4 trailing zeroes.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified performance from the ADS574. It is very important that the ADS574's power supply be filtered, well-regulated, and free from high-frequency noise. The use of a noisy supply may cause the generation of unstable output codes. It is advisable to bypass the +5V supply with a 10μF tantalum capacitor, located as close as possible to the converter. It is recommended to pay special attention to the avoidance of noise and spikes if a switching power supply is employed.

To avoid noise pickup, it is important to minimize coupling between analog inputs and digital signals. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly susceptible to noise. The circuit layout should be configured to locate the ADS574 and associated analog-input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended; careful printed-circuit construction is preferable. If external offset and gain-adjust potentiometers are used, the trimmers should be located as close to the ADS574 as possible. If no trims are required and fixed resistors are used, they should be situated as close to the converter as possible.

Analog (Pin 9) and Digital (Pin 15) Ground pins are not internally connected. It is advisable to tie them together as close to the converter as possible, preferably via a large analog ground plane beneath the package. If it is necessary to run these commons separately, it is recommended to connect a 10nF ceramic bypass capacitor between Pins 9 and 15, as close to the converter as possible. Pin 9 (Analog Ground) is the common reference point for the ADS574's internal reference. It should be connected as close as possible to the analog-input signal reference point.

CONTROL FUNCTIONS — Operating the ADS574 under microprocessor control is most easily understood by examining the various control-line functions in a truth table. Table 1 is a summary of the ADS574's control-line functions. Table 2 is the truth table that applies to these functions.

Unless Chip Enable (CE, Pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, Pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$, and A_0) will have no effect on the ADS574's operation. When CE and $\overline{CS}$ are both asserted, the signal applied to R/$\overline{C}$ (Read/Convert, Pin 5) determines whether a data Read (R/$\overline{C}$ = "1") or a Convert operation (R/$\overline{C}$ = "0") is initiated.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" =read) ("0"=convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode. A_0 selects 8-bit (A_0="1") or 12-bit (A_0="0") conversion mode. When reading output data in 2 8-bit bytes. A_0="0" accesses 8 MSBs (high byte) and A_0="1" accesses 4 LSBs and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1"=12 bits) ("0"=8 bits)	When reading output data, 12/$\overline{8}$="1" enables all 12 output bits simultaneously. 12/$\overline{8}$="0" will enable the MSbs or LSBs as determined by the A_0 line.

Table 1. ADS574 Control Line Functions

CONTROL INPUTS					ADS574 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSBs
1	0	1	0	1	Enables 4 LSBs and 4 Trailing Zeros

Table 2. Control Line Truth Table

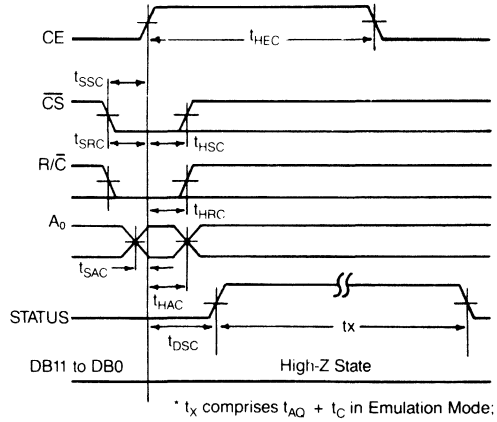
In the initiation of a conversion, the signal applied to A_0 (Byte Address/Short Cycle, Pin 4) determines whether a 12-bit conversion (A_0 = "0") or an 8-bit conversion (A_0 = "1") is initiated. It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0", and A_0 = "1" or "0" that initiates a convert operation. The actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$, as shown in Table 2 and the section entitled "TIMING — INITIATING CONVERSIONS". In the initiation of a conversion, the 12/$\overline{8}$ line has "don't care" status.

When reading digital output data from the ADS574, it is necessary to assert CE and $\overline{CS}$. The signals applied to 12/$\overline{8}$ and A_0 will determine the format of the output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is at logic "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line's state changes from "0" to "1".

If the 12/$\overline{8}$ line is at logic "0", output data will be accessible as two 8-bit bytes as detailed in the section entitled "TIMING — READING OUTPUT DATA". In this situation, A_0 = "0" will result in accessing the 8 MSBs. In this mode, only the 8 upper bits or the 4 lower bits can be accessed at one time, as addressed by A_0. In these applications, the 4 LSBs (Pins 16 to 19) should be hard-wired to the 4 MSBs (Pins 24 to 27). Thus, during a read operation, when A_0 is low, the upper 8 bits are enabled and they present data on Pins 20 through 27. See the section entitled "HARD-WIRING TO 8-BIT DATA BUSES".

TIMING — INITIATING CONVERSIONS — It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0", A_0 = "1" (initiate 8-bit conversion) or A_0 = "0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may occur simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60 nsec typ). If it is desirable that a particular one of these three inputs be responsible for initiating the conversion, the other two should be unchanging for a minimum of 50 nsec prior to the transition of the chosen input.

Because the ADS574's control logic latches the A_0 signal upon the initiation of a conversion, the A_0 line should be stable immediately prior to whichever of the cited transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a Read operation were occurring, and the result could be system bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.



* t_X comprises t_{AQ} + t_C in Emulation Mode; t_C only in S/H Control Mode.

Figure 1. Convert Timing

Figure 1 shows timing for a typical application. In this application, CS is brought low, R/C is brought low, and A_0 is set to its chosen value prior to CE's 0-to-1 transition. The sequence can be accomplished in a number of ways, including connecting CS and A_0 to address bus lines, connecting R/C to a read/write line (or its equivalent), and generating 0-to-1 transition on CE using the system clock. In this example, CS should be at logic "0" 50 nsec prior to the CE transition (t_{SSC} = 50 nsec min), R/C should be at logic "0" 50 nsec prior to the CE transition (t_{SRC} = 50 nsec min), and A_0 should be stable 0 nsec prior to the CE transition (t_{SAC} = 0 nsec min). The minimum pulse width for CE ="1"is 50 nsec (t_{HEC} = 50 nsec min) and both CS and R/C must be valid for at least 50 nsec while CE ="1"(t_{HSC} and t_{HRC} = 50 nsec min) while CE is high to

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{DSC}	STS Delay from CE		60	200	nsec
t_{HEC}	CE Pulse Width	50	30		nsec
t_{SSS}	$\overline{CS}$ to CE Setup	50	20		nsec
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		nsec
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		nsec
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		nsec
t_{SAC}	A_0 to CE Setup	0			nsec
t_{HAC}	A_0 Valid During CE High	50	20		nsec

Table 3. Convert Timing Parameters

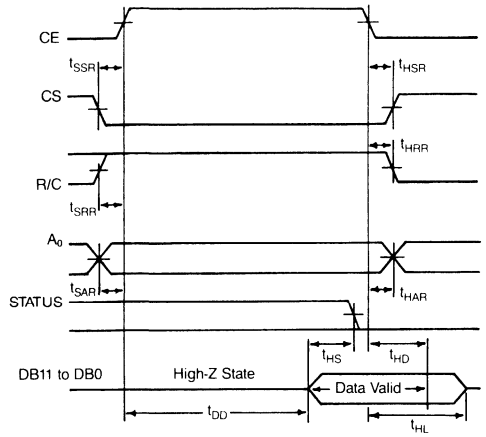


Figure 2. Read Timing

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{DD}	Access Time from CE		75	150	nsec
t_{HD}	Data Valid after CE Low	25	35		nsec
t_{HL}	Output Float Delay		100	150	nsec
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		nsec
t_{SRR}	R/$\overline{C}$ to CE Setup	0			nsec
t_{SAR}	A_0 to CE Setup	50	25		nsec
t_{HSR}	$\overline{CS}$ Valid after CE Low	0			nsec
t_{HRR}	R/$\overline{C}$ High after CE Low	0			nsec
t_{HAR}	A_0 Valid after CE Low	50			nsec
t_{HS}	STS Delay after Delay Valid	300	400	1000	nsec

Table 4. Read Timing Parameters

effectively initiate the conversion. Similarly, A_0 must be valid for at least 50 nsec (t_{HAC} = 50 nsec min) while CE is high to effectively initiate the conversion. The Status line rises to a logic"1"no later than 200 nsec after the rising edge of CE (t_{DSC} = 200 nsec max). Once Status is at logic "1", additional convert commands will be ignored until the ongoing conversion is complete. Table 3 gives the limits for the convert timing parameters.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status output = "1"), the ADS574's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates the conversion is complete, the combination of CE = "1", $\overline{CS}$ = "0", and R/$\overline{C}$ = "1" is used to activate the buffer and read the digital output data.

If the cited combination of control signals is satisfied and the 12/$\overline{8}$ line has logic "1" imposed, all 12 output bits will become valid simultaneously. If the 12/$\overline{8}$ line has logic "0" imposed, output data will be formatted for an 8-bit data bus.

Figure 2 shows timing for a typical application. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high, all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50 nsec prior to CE (t_{SSP} and t_{SAR} = 50 nsec min). R/$\overline{C}$ can become valid at the same time as CE (t_{SRR} = 0 nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which ensures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid typically 400 nsec before the falling edge of Status, as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TTL/CMOS compatible and may be actively driven. Table 4 gives the limits for the read timing parameters.

S/H CONTROL MODE AND NON-SAMPLING 574 EMULATION MODE — Figure 3 and Table 5 show the basic differences between the two operating modes. In both modes, the acquisition time is 4μsec typ. In the Control mode, during the 4μsec acquisition time, the input signal may not slew faster than the inherent slew rate of the ADS574. After the Convert command arrives, any changes in the input signal level have no effect on the conversion, as the input signal is already sampled and the conversion process begins immediately.

In the Control mode, a Convert command can provide some useful peripheral functions — for example, control an input MUX or a programmable-gain amplifier. In these applications, the input signal has time to settle before the subsequent acquisition occurs after the conversion. The internal sample/hold function keeps aperture jitter to a minimum; therefore, it is possible to digitize high input frequencies without the need for an external sample/hold amplifier.

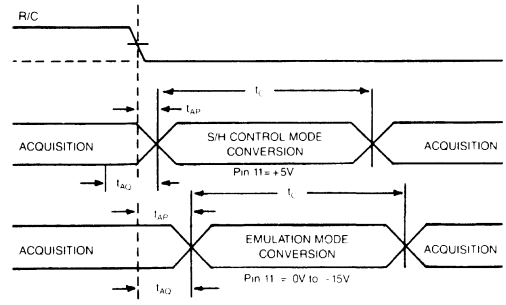


Figure 3. Signal Acquisition and Conversion Timing

SYMBOL	PARAMETER	S/H CONTROL TYP.	S/H CONTROL MAX.	EMULATION TYP.	EMULATION MAX.	UNITS
$t_{AQ}+t_C$	Throughput Times:					
	12-Bit Conversion	22	25	22	25	μsec
	8-Bit Conversion	16	18	16	18	μsec
t_C	Conversion Time:					
	12-Bit Conversion	18		18		μsec
	8-Bit Conversion	12		12		μsec
t_{AQ}	Acquisition Time	4		4		μsec
t_A	Aperture Delay	20		4000		nsec
t_J	Aperture Jitter	0.3		30		nsec

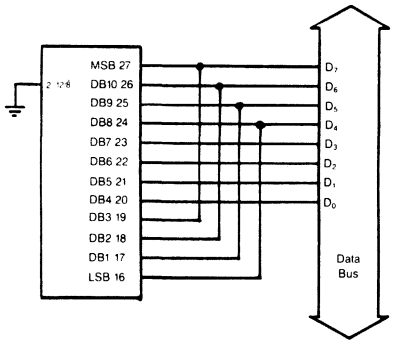
Table 5. Conversion Timing Over T_{MIN} to T_{MAX}

the Emulation mode, the ADS574 introduces a delay time between the Convert command and the start of conversion, in order allow the converter enough time to acquire the signal before the nversion. The delay causes an effective increase in aperture time om 0.02 μsec to 4 μsec, and allows the ADS574 to replace industry-andard, non-sampling 574 types in existing sockets. Slewing of e analog input prior to the Convert command has no effect on the curacy of the ADS574. In both the Control and Emulation modes, e internal sample/hold circuit begins slewing to track the input gnal immediately after the conversion is complete.

the Emulation mode, the ADS574 can replace existing, non-mpling 574 types in almost all applications, without any changes system hardware or software. It is not necessary that the input gnal be stable before a Convert command arrives, but it must re-ain stable during the acquisition period after the Convert com-and is received (as it must with other 574 types) for accurate per-mance. Unlike other, non-sampling 574 types, the ADS574 allows e input to begin slewing before the end of conversion (after the sec acquisition period), so it is possible to increase system oughput in many cases.

ARD-WIRING TO 8-BIT DATA BUSES — For applications with bit data buses, output lines DB4 to DB11 (Pins 20 to 27) should nnect directly to lines D_0 to D_7 in the system data bus. In addition, tput lines DB0 to DB3 (Pins 16 to 19) should connect to lines D_4 D_7 on the system data bus, and to ADS574 output lines DB8 to 311 (Pins 24 to 27). Figure 4 shows the proper connections. Thus nnected, if A_0 is low during a read operation, the upper 8 bits are abled and become valid on output pins 20 to 27. When A_0 is high ring an operation, the 4 LSBs are enabled on output pins 16 to and the 4 middle bits (Pins 20 to 23) are overridden with zeros.

	D7	D6	D5	D4	D3	D2	D1	D0
gh Byte = 0)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
w Byte = 1)	DB3	DB2	DB1	DB0	0	0	0	0



jure 4. Connection to 8-Bit Bus

AND-ALONE OPERATION — The ADS574 can be used in a nd-alone mode in systems having dedicated input ports and not juiring full bus-interface capability. In this mode, CE and 12/8 are d to logic "1" (they may be hard-wired to +5V), $\overline{CS}$ and A_0 are d to logic "0" (they may be grounded), and the conversion is con-led by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low suming a conversion is not already in progress), and all 12 bits he 3-state output buffers are enabled whenever R/$\overline{C}$ is brought h (assuming Status has already gone low, indicating completion conversion).

This configuration gives rise to two possible modes of operation. Conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. Figure 5 details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$, and they return to valid logic levels after the conversion cycle is completed. The Status output goes high 200 nsec after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 1000 nsec after data is valid (t_{HS}). In this mode, output data is available most of the time, and becomes invalid only during a conversion.

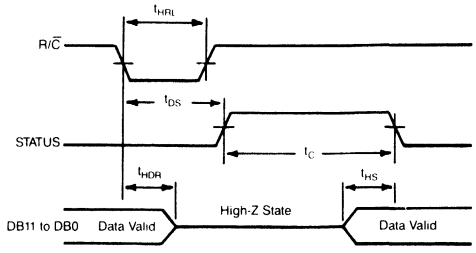


Figure 5. Stand Alone Mode With Negative Start Pulse.

Figure 6 details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to the high-impedance state and remain in that state until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible most of the time, and becomes valid only when R/$\overline{C}$ goes high. Table 6 gives the timing parameters for the two modes.

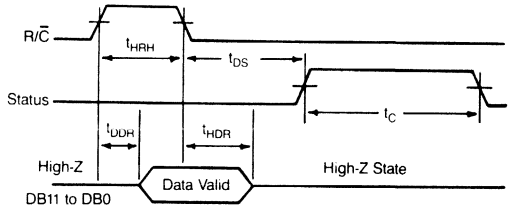


Figure 6. Stand-Alone Mode with Positive Start Pulse.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	25			nsec
t_{DS}	STS Delay after R/$\overline{C}$			200	nsec
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25			nsec
t_{HRH}	High R/$\overline{C}$ Pulse Width	100			nsec
t_{DDR}	Data Access Time			150	nsec

Table 6. Stand-Alone Mode Timing over T_{MIN} to T_{MAX}

UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating mode are shown in Figure 7. If the 0 to +10V input range is to be used, apply the analog input to Pin 13. If the 0 to +20V input range is to be used, apply the analog input to Pin 14. If the gain adjustment is not needed, replace trim potentiometer R_2 with a fixed, 50Ω ±1% metal-film resistor to meet all published specifications. If the offset adjustment is not needed, connect Pin 12 (Bipolar Offset) directly to Pin 9 (Analog Ground).

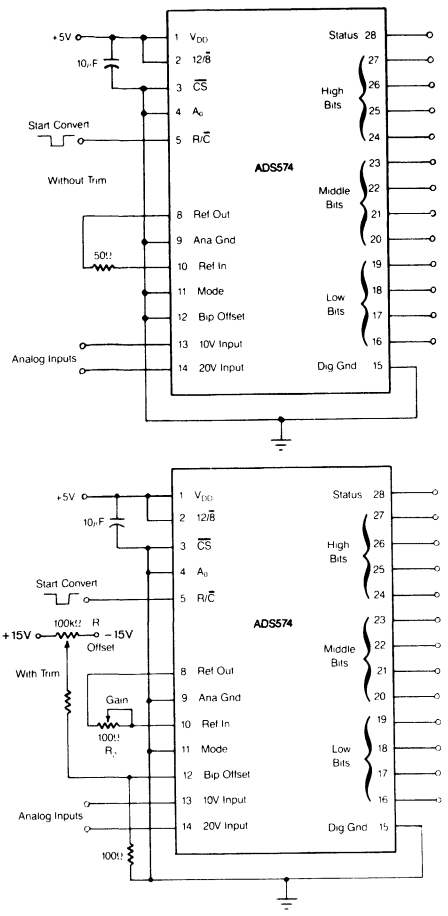


Figure 7. Unipolar Connections

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see section entitled "DIGITAL OUTPUT CODING"). If the offset adjustment is not used, the actual transition will occur within specified limits of its ideal value (+½LSB). For the 10V range, 1 LSB = 2.44mV. For the 20V range, 1 LSB = 4.88mV. To adjust the offset, apply an analog input equal to +½LSB and, with the ADS574 continuously converting, adjust the offset potentiometer "down" until the digital output is all ones, and then adjust "up" until the LSB "flickers" between "0" and "1".

Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the unipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal full-scale voltage for the selected input range. This corresponds to +9.9963V and +19.9927V, respectively, for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer "up" until the digital outputs are all ones, and then adjusting "down" until the LSB "flickers" between "0" and "1".

In some applications, it is desirable to have the LSB equal exactly 2.5mV (10.24V input range) or 5mV (20.48V input range). To implement these ranges, replace the 100 gain trimpot by a 50Ω fixed resistor. Then insert a 2.7kΩ trimpot in series with Pin 13 for a 10.24V range; Pin 14 for a 20.48V range. Offset trimming then proceeds as described earlier, and the gain trim is effected with the new trimpot.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating mode are shown in Figure 8. If the ±5V input range is to be used, apply the analog input to Pin 13. If the ±10V range is to be used, apply the analog input to Pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trimpots should be replaced by fixed, 50Ω ±1% metal-film resistors to meet all published specifications.

Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see section entitled "DIGITAL OUTPUT CODING"). Ideally, this transition should occur ½LSB below 0V, and if the bipolar offset adjustment is not used, the transition will occur within the specified limit of its ideal value. Offset adjustment in the bipolar configuration is performed not at the zero-crossing point but at the minus full-scale point. The procedure is to apply an analog input equal to −FS + ½LSB (−4.9988V for the ±5V range; −9.9976V for the ±0V range), and adjust the bipolar offset trimpot "down" until the digital output is all zeros. Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the bipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal positive full-scale value of the selected input range. This corresponds to +4.9963V and +9.9927V for the ±5V and ±10V ranges, respectively. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trimpot "up" until the digital outputs are all ones, then adjusting "down" until the LSB "flickers" between "1" and "0".

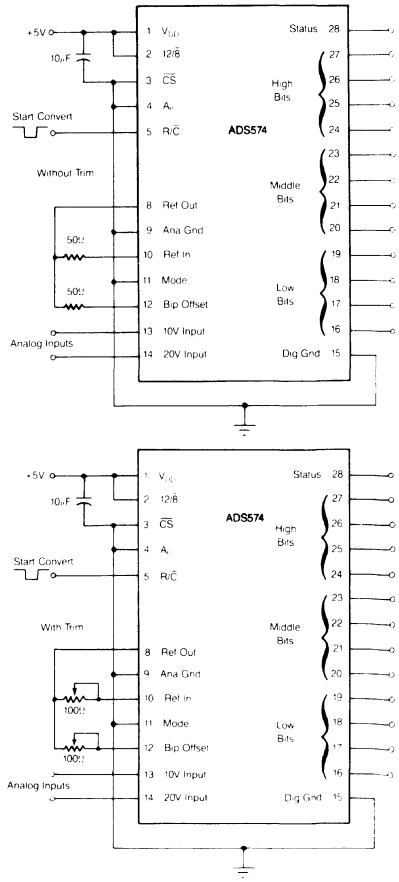


Figure 8. Bipolar Connections

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to +10V	0 to +20V	±5V	±10V	MSB LSB
+10.0000	+20.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+19.9927	+4.9963	+9.9927	1111 1111 111Ø *
+5.0012	+10.0024	+0.0012	+0.0024	1000 0000 000Ø *
+4.9988	+9.9976	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ *
+4.9963	+9.9927	−0.0037	−0.0073	0111 1111 111Ø *
+0.0012	+0.0024	−4.9988	−9.9976	0000 0000 000Ø *
0.0000	0.0000	−5.0000	−10.0000	0000 0000 0000

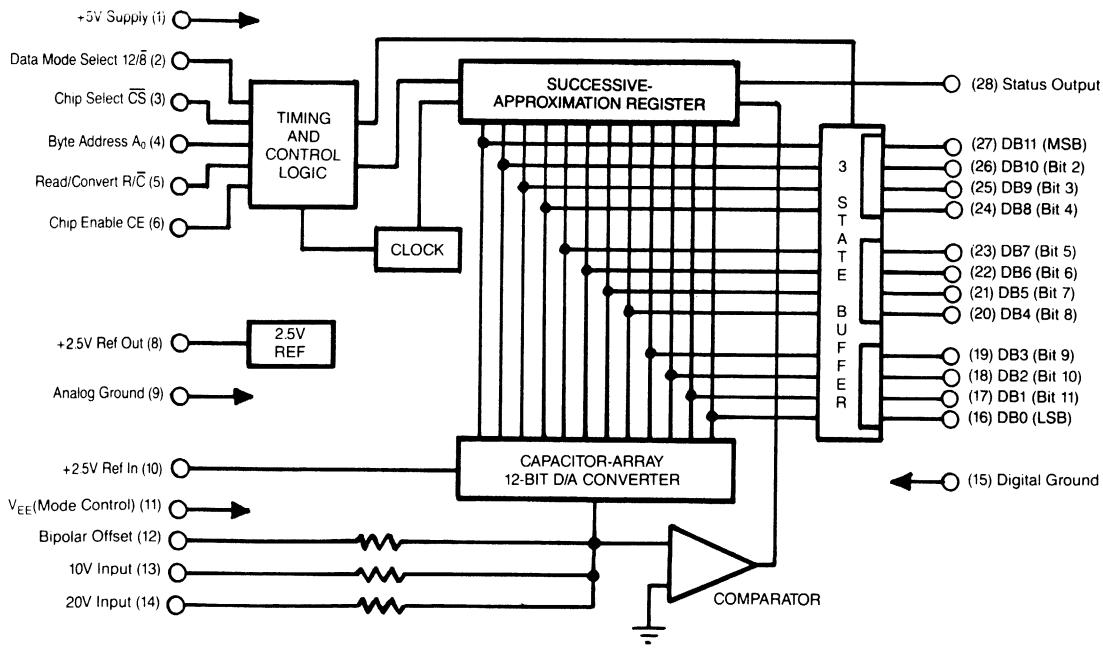
DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits =2.44mV. 1LSB for 11 bits =4.88mV.
4. For 0 to +20V or ±10V input ranges, 1LSB for 12 bits =4.88mV. 1LSB for 11 bits =9.77mV.

*Voltages given are the theoretical values for the transition indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADS574 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

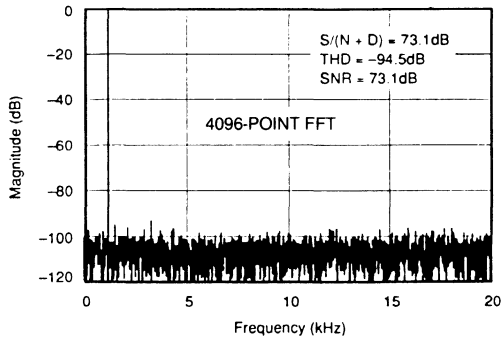
ADS574 BLOCK DIAGRAM



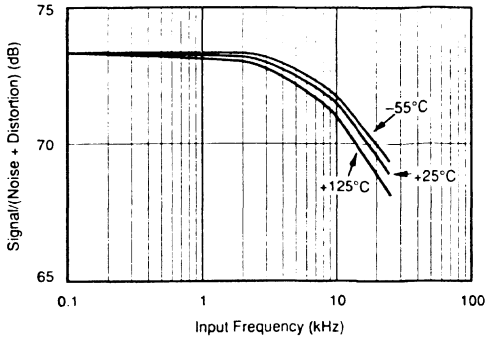
TYPICAL PERFORMANCE

(T_A =25°C, Supplies = +5V, ±10V Bipolar Input, f_{IN} =40kHz, unless otherwise indicated)

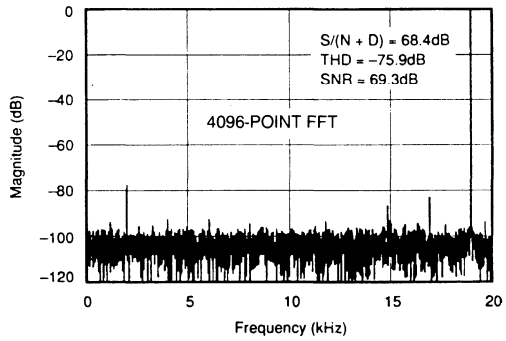
FREQUENCY SPECTRUM (±10V, 2kHz Input)



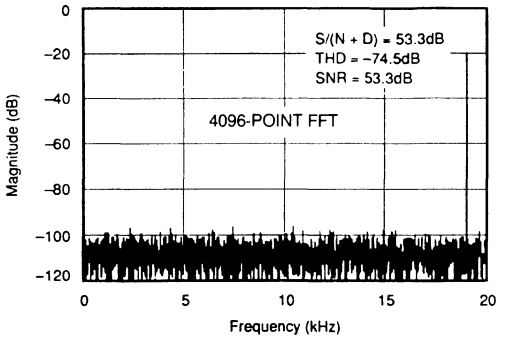
SIGNAL (NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



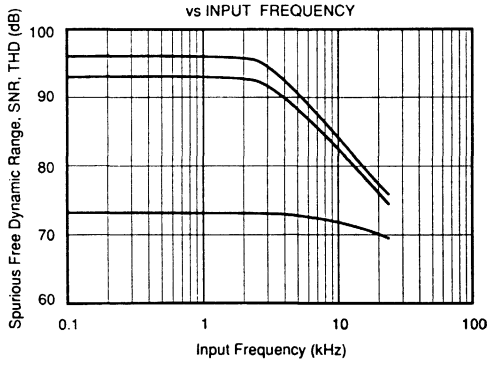
FREQUENCY SPECTRUM (±10V, 19kHz Input)



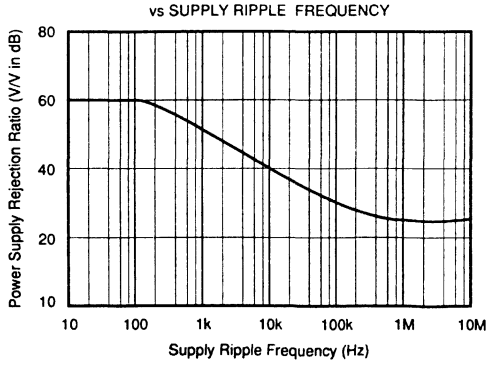
FREQUENCY SPECTRUM (±1V, 19kHz Input)



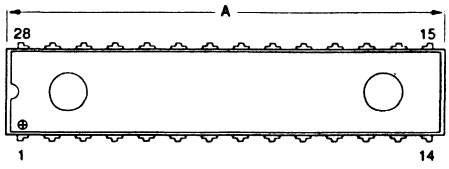
SPURIOUS FREE DYNAMIC RANGE, SNR AND THD
vs INPUT FREQUENCY



POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY

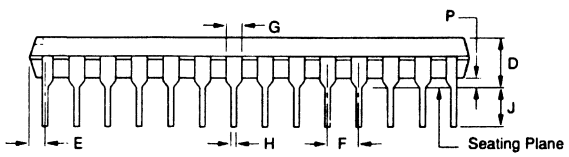


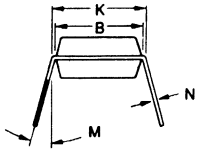
PACKAGE OUTLINES

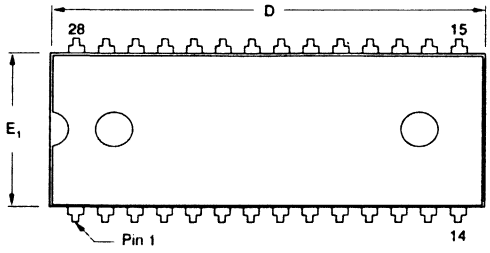


PACKAGE E. PLASTIC SINGLE DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02



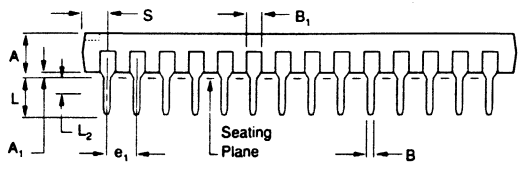


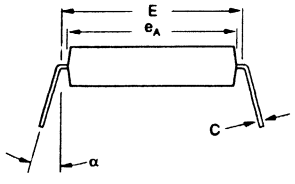


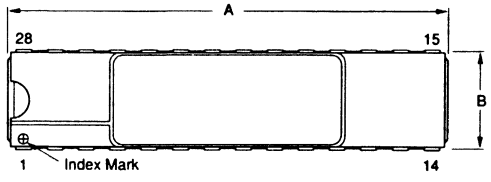
PACKAGE P. PLASTIC DOUBLE DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D (1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S (1)	.040	.080	1.02	2.03

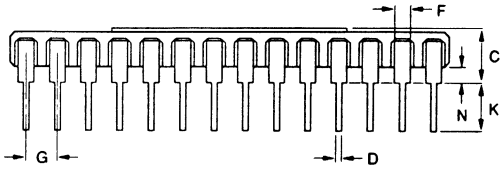


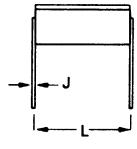




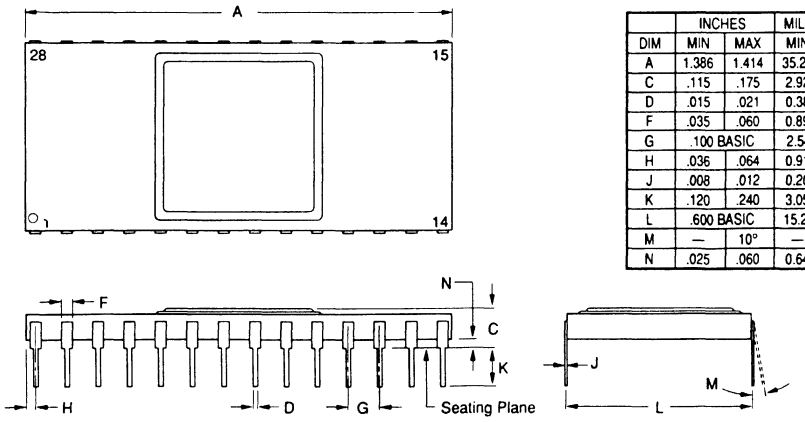
PACKAGE F. CERAMIC HERMETIC SINGLE DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52



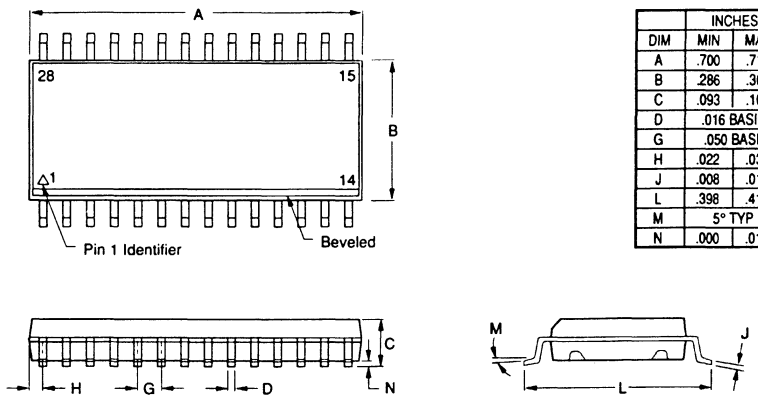


PACKAGE H. CERAMIC HERMETIC DOUBLE DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

PACKAGE U. PLASTIC SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

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MICRO NETWORKS

ADS774

8.5μsec, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- Low Cost
- Pin-Compatible with MN574/674/774
- Eliminates External S/H in Most Applications
- Complete, 8.5μsec, 12-Bit A/D Converter with Internal
  - Clock
  - Reference
  - Control Logic
- Full 8- or 16-Bit μP Interface:
  - 3-State Output Buffer
  - Chip Select, Address Decode
  - Read/Write Control
- No-Missing-Codes Guaranteed Over Temperature
- Single +5V Supply Operation
- Low Power: 120mW Max
- Package Options
  - 0.3" Plastic DIP
  - 0.3" Hermetic DIP
  - 0.6" Plastic DIP
  - 0.6" Hermetic DIP
  - SOIC

DESCRIPTION

The ADS774 is a complete, low-cost, 12-bit successive-approximation A/D converter with an internal sample/hold function. In most existing applications, it is drop-in compatible with non-sampling 774 types, and eliminates the need for an external S/H amplifier. The ADS774 uses an innovative, capacitor-array internal D/A converter, based on CMOS technology. The use of a CMOS architecture results in much lower power consumption and the ability to operate from a single +5V supply (the formerly required -12V or -15V supply is optional, depending on the application).

The ADS774 is complete with internal clock, reference, control logic, and 3-state output buffer. The interface logic provides for easy handshaking with most popular 8- and 16-bit microprocessors. The ADS774's 3-state output buffer connects directly to the μP's data bus, and is readable as either one 12-bit word or two 8-bit bytes. Chip select, chip enable, address decode (for short cycling), and read/write (read/convert) control inputs enable the ADS774 to connect directly to a system address bus and control lines, and to operate totally under processor control.

Internal scaling resistors allow a pin-selectable choice of four input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. The maximum throughput time (including both acquisition and conversion) for 12-bit conversions is 8.5μsec over the full operating-temperature range. The ADS774 is available for operation over the commercial (0°C to +70°C) and military (-55°C to +125°C) temperature ranges. Package options include 28-pin single (0.300) or double (0.600) plastic or hermetic ceramic DIPs, and 28-pin plastic SOIC. For availability of devices screened to MIL-STD-883, consult factory.

Model Number	Package	Temperature Range	Linearity Error Max (T_{min} to T_{max})
ADS774JE	0.3" Plastic DIP	0°C to +70°C	±1LSB
ADS774KE	0.3" Plastic DIP	0°C to +70°C	±½LSB
ADS774JP	0.6" Plastic DIP	0°C to +70°C	±1LSB
ADS774KP	0.6" Plastic DIP	0°C to +70°C	±½LSB
ADS774JU	SOIC	0°C to +70°C	±1LSB
ADS774KU	SOIC	0°C to +70°C	±½LSB
ADS774JH	0.6" Ceramic DIP	0°C to +70°C	±1LSB
ADS774KH	0.6" Ceramic DIP	0°C to +70°C	±½LSB
ADS774SF	0.3" Ceramic DIP	-55°C to +125°C	±1LSB
ADS774TF	0.3" Ceramic DIP	-55°C to +125°C	±¾LSB
ADS774SH	0.6" Ceramic DIP	-55°C to +125°C	±1LSB
ADS774TH	0.6" Ceramic DIP	-55°C to +125°C	±¾LSB

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ADS774 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	
J, K Grades	−40°C to +85°C
S, T Grades	−55°C to +125°C
Specified Temperature Range:	
J, K Grades	0°C to +70°C
S, T Grades	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} to Digital Ground	0 to −16.5V
V_{DD} to Digital Ground	0 to +7V
Analog Ground to Digital Ground	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/8, R/$\overline{C}$) to Digital Ground	−0.5V to V_{DD} to +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Ground	±16.5V
$20V_{IN}$ to Analog Ground	±24V
Ref Out	Indefinite Short to Ground, Momentary Short to V_{DD}
Junction Temperature	+165°C
Lead Temperature (Soldering, 10 sec)	+300°C
Thermal Resistance Θ_{JA}: Ceramic	50°C/W
Plastic	100°C/W

ORDERING INFORMATION

PART NUMBER — **ADS774 T H**

Select suffix J, K, S or T for desired performance and specific temperature range.

Select suffix E, F, H, P or U for desired package option.

DESIGN SPECIFICATIONS ALL UNITS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, f_S = 117kHz, f_{IN} = 10kHz) (unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	8.5	12		kΩ
0 to +20V, ±10V	35	50		kΩ
DIGITAL INPUTS CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Current	−5	0.1	+5	μA
Input Capacitance		5		pF
DIGITAL OUTPUTS DB0 to DB11, Status				
Output Coding: Unipolar Ranges (Note 1)		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" (I_{SOURCE} = 500μA)	+2.4			Volts
Logic "0" (I_{SINK} = 1.6mA)			+0.4	Volts
Leakage (DB0 to DB11) in High-Z State	−5	0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output Voltage (Pin 8)	+2.4	+2.5	+2.6	Volts
Available Output Source Current	0.5			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: V_{EE} Supply (Note 2)	−16.5		V_{DD}	Volts
Power Supply Range: V_{DD} Supply	+4.5		+5.5	Volts
Current Drains: I_{EE} (V_{EE} = −15V)		−1		mA
I_{DD}		+15	+24	mA
Power Dissipation V_{EE} = 0V to +5V		75	120	mW
DYNAMIC CHARACTERISTICS				
Sampling Rate (Max) T_{MIN} to T_{MAX}	117			kHz
25°C	125			kHz
Aperture Delay t_{AP}				
With V_{EE} = +5V		20		nsec
With V_{EE} = 0V to −15V		1.6		μsec
Aperture Uncertainty (Jitter)				
With V_{EE} = +5V		300		psec rms
With V_{EE} = 0V to −15V		10		nsec rms
Settling Time to 0.01% for Full-Scale Input Step		1.4		μsec
CONVERSION TIME (Including Acquisition Time)				
t_{AQ} + t_C at 25°C:				
8-Bit Cycle		5.5	5.9	μsec
12-Bit Cycle		7.5	8	μsec
12-Bit Cycle, T_{MIN} to T_{MAX}		8	8.5	μsec

PERFORMANCE SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, f_S = 117kHz, f_{IN} = 10kHz unless otherwise indicated)

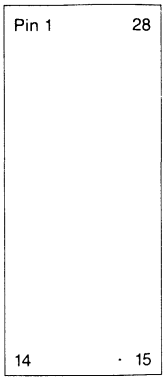
GRADE	ADS774J, S			ADS774K, T			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
RESOLUTION			12			12	Bits
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At 25°C:							
Linearity Error			±1			±½	LSB
Unipolar Offset Error (Notes 3, 4)			±2			±2	LSB
Bipolar Offset Error (Notes 3, 5)			±10			±4	LSB
Full-Scale Calibration Error (Notes 3, 6, 7)			±0.25			±0.25	%FSR
Inherent Quantization Uncertainty		±½			±½		LSB
T_{MIN} to T_{MAX}:							
Linearity Error: J, K, Grades			±1			±½	LSB
S, T Grades			±1			±¾	LSB
Full-Scale Calibration Error:							
Untrimmed: J, K Grades			±0.47			±0.37	%FSR
S, T Grades			±0.75			±0.5	%FSR
Trimmed to Zero at 25°C: J, K Grades			±0.22			±0.12	%FSR
S, T Grades			±0.5			±0.25	%FSR
Resolution for No Missing Codes	12			12			Bits
TEMPERATURE COEFFICIENTS (Note 8)							
Unipolar Offset			±5			±2.5	ppm/°C
Max. Change Over Temperature:			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max. Change Over Temperature: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration			±45			±25	ppm/°C
Max Change Over Temperature: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
AC ACCURACY (Note 9)							
Spurious-Free Dynamic Range	73	78		76	78		dB
Total Harmonic Distortion		−77	−72		−77	−75	dB
Signal-to-Noise Ratio	69	72		71	72		dB
Signal-to-(Noise+Distortion) Ratio (SINAD)	68	71		70	71		dB
Intermodulation Distortion (f_{IN1} = 20kHz; f_{IN2} = 23kHz)		−75			−75		dB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration (Note 10)							
+4.75V < V_{DD} < +5.25V							
Max. Change: J, K Grades			±½			±½	LSB
S, T Grades			±1			±1	LSB

SPECIFICATION NOTES:

1. See table of transition voltages in section labeled Digital Output Coding.
2. The use of V_{EE} is optional. This input sets the mode for the internal sample/hold circuit. When V_{EE} = −15V, I_{EE} = −1mA typ; when V_{EE} = 0V, I_{EE} = ±5μA typ; when V_{EE} = +5V, I_{EE} = +167μA typ.
3. Adjustable to zero with external potentiometer.
4. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when the ADS774 is operating with a unipolar range. The ideal value for this transition is +½LSB. See section labeled Digital Output Coding.
5. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when the ADS774 is operating with a bipolar range. The ideal value for this transition is −½LSB. See section labeled Digital Output Coding.
6. Listed specs assume a fixed 50Ω resistor between Ref Out (Pin 8) and Ref In (Pin 10) and a fixed 50Ω resistor between Ref Out (Pin 8) and Bipolar Offset (Pin 12) in bipolar configurations; or Bipolar Offset grounded in unipolar configurations. Full-scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. The ideal value for this transition is 1½LSBs below the nominal full-scale voltage. See section labeled Digital Output Coding.
7. FSR is a full-scale range. For the ±10V input range, FSR is 20V. For the 0 to +10V input range, FSR is 10V.
8. Temperature coefficient specifications assume the use of the internal reference.
9. Specifications assume V_{EE} = +5V, which starts a conversion immediately upon a Convert command. If V_{EE} = 0V to −15V, the ADS774 emulates standard ADC774 operation. In this mode, the internal sample/hold circuit acquires the input signal after receiving the Convert command, and does not assume that the input level had been stable before the arrival of the Convert command.
10. Worst-case change in accuracy, compared with accuracy with a +5V supply.

Specifications are subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	+5V Supply ($+V_{DD}$)	28	Status Output
2	Data Mode Select 12/$\overline{8}$	27	DB11 (MSB)
3	Chip Select $\overline{CS}$	26	DB10 (Bit 2)
4	Byte Address A_0	25	DB9 (Bit 3)
4	Read/Convert R/$\overline{C}$	24	DB8 (Bit 4)
6	Chip Enable CE	23	DB7 (Bit 5)
7	No Connect*	22	DB6 (Bit 6)
8	+2.5V Ref Out	21	DB5 (Bit 7)
9	Analog Ground	20	DB4 (Bit 8)
10	+2.5V Ref In	19	DB3 (Bit 9)
11	Mode Control V_{EE}	18	DB2 (Bit 10)
12	Bipolar Offset	17	DB1 (Bit 11)
13	10V Input	16	DB0 (LSB)
14	20V Input	15	Digital Ground

*No Internal Connection

DESCRIPTION OF OPERATION

The ADS774 is a complete 12-bit A/D converter. It uses the successive-approximation conversion technique and incorporates all required function blocks — capacitor-array D/A converter, comparator, clock, reference, and control logic. The CMOS-based capacitor-array architecture provides an inherent sample/hold function; the ADS774 is thus a sampling equivalent of the industry-standard 774 A/D converter. The device mates directly to most popular 8-, 16-, and 32-bit microprocessors and contains all the necessary address-decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most cases, the ADS774 will require only a power supply, a bypass capacitor, and two resistors to provide the complete A/D conversion function. The completeness of the device makes it most convenient to think of the ADS774 as a function block with specific input/output transfer characteristics; it is thus quite unnecessary to be concerned with its inner workings.

Operating the ADS774 under microprocessor control (note that it also functions as a stand-alone A/D) entails, in most applications, a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D, and also involves a write operation. Once the proper signals have been received and a conversion has begun, the ADS774 cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the ADS774's Status Output (also called Busy Line or End-of-Conversion (EOC) Line) rises to logic "1", indicating that a conversion is in progress. At the end of a conversion, the internal control logic will cause the Status Output to drop to "0", and will enable internal circuitry to allow reading output data by external command. By monitoring the state of the Status Output or by waiting an appropriate period of time, the microprocessor will know when the conversion is complete and that output data is valid and ready to be read.

If the ADS774 interfaces with 12-bit or wider microprocessors, it is possible to 3-state-enable all 12 output bits simultaneously, allowing data collection with a single read operation. If the ADS774 operates with an 8-bit processor, output data can be formatted to read in two 8-bit bytes. The first byte will contain the 8 most-significant bits (MSBs). The second byte will contain the remaining 4 least-significant bits (LSBs), in a left-justified format, with 4 trailing zeroes.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified performance from the ADS774. It is very important that the ADS774's power supply be filtered, well-regulated, and free from high-frequency noise. The use of a noisy supply may cause the generation of unstable output codes. It is advisable to bypass the +5V supply with a 10μF tantalum capacitor, located as close as possible to the converter. It is recommended to pay special attention to the avoidance of noise and spikes if a switching power supply is employed.

To avoid noise pickup, it is important to minimize coupling between analog inputs and digital signals. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly susceptible to noise. The circuit layout should be configured to locate the ADS774 and associated analog-input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended; careful printed-circuit construction is preferable. If external offset and gain-adjust potentiometers are used, the trimmers should be located as close to the ADS774 as possible. If no trims are required and fixed resistors are used, they should be situated as close to the converter as possible.

Analog (Pin 9) and Digital (Pin 15) Ground pins are not internally connected. It is advisable to tie them together as close to the converter as possible, preferably via a large analog ground plane beneath the package. If it is necessary to run these commons separately, it is recommended to connect a 10nF ceramic bypass capacitor between Pins 9 and 15, as close to the converter as possible. Pin 9 (Analog Ground) is the common reference point for the ADS774's internal reference. It should be connected as close as possible to the analog-input signal reference point.

CONTROL FUNCTIONS — Operating the ADS774 under microprocessor control is most easily understood by examining the various control-line functions in a truth table. Table 1 is a summary of the ADS774's control-line functions. Table 2 is the truth table that applies to these functions.

Unless Chip Enable (CE, Pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, Pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$, and A_0) will have no effect on the ADS774's operation. When CE and $\overline{CS}$ are both asserted, the signal applied to R/$\overline{C}$ (Read/Convert, Pin 5) determines whether a data Read (R/$\overline{C}$ = "1") or a Convert operation (R/$\overline{C}$ = "0") is initiated.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" =read) ("0"=convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode. A_0 selects 8-bit (A_0="1") or 12-bit (A_0="0") conversion mode. When reading output data in 2 8-bit bytes. A_0="0" accesses 8 MSBs (high byte) and A_0="1" accesses 4 LSBs and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1"=12 bits) ("0"=8 bits)	When reading output data, 12/$\overline{8}$="1" enables all 12 output bits simultaneously. 12/$\overline{8}$="0" will enable the MSbs or LSBs as determined by the A_0 line.

Table 1. ADS774 Control Line Functions

CONTROL INPUTS					ADS774 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSBs
1	0	1	0	1	Enables 4 LSBs and 4 Trailing Zeros

Table 2. Control Line Truth Table

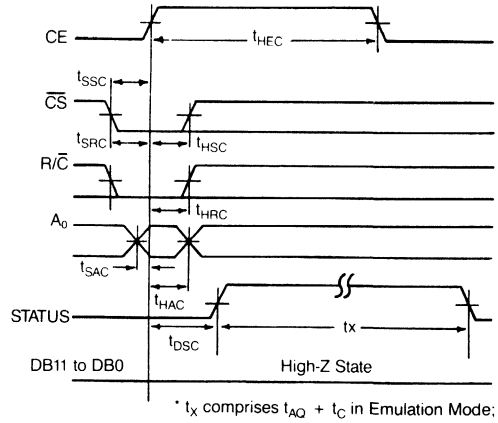
In the initiation of a conversion, the signal applied to A_0 (Byte Address/Short Cycle, Pin 4) determines whether a 12-bit conversion (A_0 = "0") or an 8-bit conversion (A_0 = "1") is initiated. It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0", and A_0 = "1" or "0" that initiates a convert operation. The actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$, as shown in Table 2 and the section entitled "TIMING — INITIATING CONVERSIONS". In the initiation of a conversion, the 12/$\overline{8}$ line has "don't care" status.

When reading digital output data from the ADS774, it is necessary to assert CE and $\overline{CS}$. The signals applied to 12/8 and A_0 will determine the format of the output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is at logic "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line's state changes from "0" to "1".

If the 12/$\overline{8}$ line is at logic "0", output data will be accessible as two 8-bit bytes as detailed in the section entitled "TIMING — READING OUTPUT DATA". In this situation, A_0 = "0" will result in accessing the 8 MSBs. In this mode, only the 8 upper bits or the 4 lower bits can be accessed at one time, as addressed by A_0. In these applications, the 4 LSBs (Pins 16 to 19) should be hard- wired to the 4 MSBs (Pins 24 to 27). Thus, during a read operation, when A_0 is low, the upper 8 bits are enabled and they present data on Pins 20 through 27. See the section entitled "HARD-WIRING TO 8-BIT DATA BUSES".

TIMING — INITIATING CONVERSIONS — It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0", A_0 = "1" (initiate 8-bit conversion) or A_0 = "0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may occur simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60 nsec typ). If it is desirable that a particular one of these three inputs be responsible for initiating the conversion, the other two should be unchanging for a minimum of 50 nsec prior to the transition of the chosen input.

Because the ADS774's control logic latches the A_0 signal upon the initiation of a conversion, the A_0 line should be stable immediately prior to whichever of the cited transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a Read operation were occurring, and the result could be system bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.



* t_X comprises t_{AQ} + t_C in Emulation Mode; t_C only in S/H Control Mode.

Figure 1. Convert Timing

Figure 1 shows timing for a typical application. In this application, $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, And A_0 is set to its chosen value prior to CE's "0"-to-"1" transition. The sequence can be accomplished in a number of ways, including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent), and generating "0"-to-"1" transition on CE using the system clock. In this example, $\overline{CS}$ should be at logic "0" 50 nsec prior to the CE transition (t_{SSC} = 50 nsec min), R/$\overline{C}$ should be at logic "0" 50 nsec prior to the CE transition (t_{SRC} = 50 nsec min), and A_0 should be stable 0 nsec prior to the CE transition (t_{SAC} = 0 nsec min). The minimum pulse width for CE = "1" is 50 nsec (t_{HEC} = 50 nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{DSC}	STS Delay from CE		60	200	nsec
t_{HEC}	CE Pulse Width	50	30		nsec
t_{SSS}	$\overline{CS}$ to CE Setup	50	20		nsec
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		nsec
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		nsec
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		nsec
t_{SAC}	A_0 to CE Setup	0			nsec
t_{HAC}	A_0 Valid During CE High	50	20		nsec

Table 3. Convert Timing Parameters

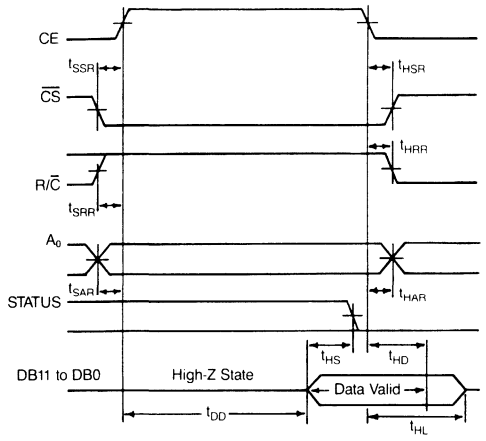


Figure 2. Read Timing

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{DD}	Access Time from CE		75	150	nsec
t_{HD}	Data Valid after CE Low	25	35		nsec
t_{HL}	Output Float Delay		100	150	nsec
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		nsec
t_{SRR}	R/$\overline{C}$ to CE Setup	0			nsec
t_{SAR}	A_0 to CE Setup	50	25		nsec
t_{HSR}	$\overline{CS}$ Valid after CE Low	0			nsec
t_{HRR}	R/$\overline{C}$ High after CE Low	0			nsec
t_{HAR}	A_0 Valid after CE Low	50			nsec
t_{HS}	STS Delay after Delay Valid	75	150	375	nsec

Table 4. Read Timing Parameters

50 nsec while CE = "1" (t_{HSC} and t_{HRC} = 50 nsec min) to effectively initiate the conversion. Similarly, A_0 must be valid for at least 50 nsec (t_{HAC} = 50 nsec min) while CE is high to effectively initiate the conversion. The Status line rises to a logic "1" no later than 200 nsec after the rising edge of CE (t_{DSC} = 200 nsec max). Once Status is at logic "1", additional convert commands will be ignored until the ongoing conversion is complete. Table 3 gives the limits for the convert timing parameters.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status output = "1"), the ADS774's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates the conversion is complete, the combination of CE = "1", $\overline{CS}$ = "0", and R/$\overline{C}$ = "1" is used to activate the buffer and read the digital output data.

If the cited combination of control signals is satisfied and the 12/8 line has logic "1" imposed, all 12 output bits will become valid simultaneously. If the 12/$\overline{8}$ line has logic "0" imposed, output data will be formatted for an 8-bit data bus.

Figure 2 shows timing for a typical application. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high, all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50 nsec prior to CE (t_{SSR} and t_{SAR} = 50 nsec min). R/$\overline{C}$ can become valid at the same time as CE (t_{SRR} = 0 nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which ensures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming CS is already low). Data actually becomes valid typically 150 nsec before the falling edge of Status, as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TTL/CMOS compatible and may be actively driven. Table 4 gives the limits for the read timing parameters.

S/H CONTROL MODE AND NON-SAMPLING 574 EMULATION MODE — Figure 3 and Table 5 show the basic differences between the two operating modes. In both modes, the acquisition time is 4 μsec typ. In the Control mode, during the 4μsec acquisition time, the input signal may not slew faster than the inherent slew rate of the ADS774. After the Convert command arrives, any changes in the input signal level have no effect on the conversion, as the input signal is already sampled and the conversion process begins immediately.

In the Control mode, a Convert command can provide some useful peripheral functions — for example, control an input MUX or a programmable-gain amplifier. In these applications, the input signal has time to settle before the subsequent acquisition occurs after the conversion. The internal sample/hold function keeps aperture jitter to a minimum; therefore, it is possible to digitize high input frequencies without the need for an external sample/hold amplifier.

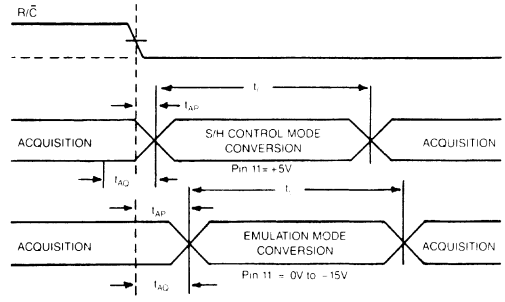


Figure 3. Signal Acquisition and Conversion Timing

SYMBOL	PARAMETER	S/H CONTROL TYP.	S/H CONTROL MAX.	EMULATION TYP.	EMULATION MAX.	UNITS
$t_{AQ}+t_C$	Throughput Times:					
	12-Bit Conversion	8	8.5	8	8.5	μsec
	8-Bit Conversion	6	6.3	6	6.3	μsec
t_C	Conversion Time:					
	12-Bit Conversion	6.4		6.4		μsec
	8-Bit Conversion	4.4		4.4		μsec
t_{AQ}	Acquisition Time	1.4		1.4		μsec
t_A	Aperture Delay	20		1600		nsec
t_J	Aperture Jitter	0.3		10		nsec

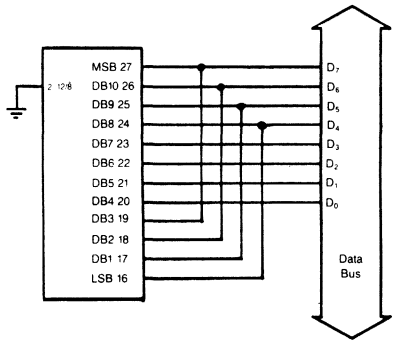
Table 5. Conversion Timing Over T_{MIN} to T_{MAX}

he Emulation mode, the ADS774 introduces a delay time between
Convert command and the start of conversion, in order to allow
converter enough time to acquire the signal before the conver-
n. The delay causes an effective increase in aperture time from
2 μsec to 1.6 μsec, and allows the ADS774 to replace industry-
ndard, non-sampling 774 types in existing sockets. Slewing of
analog input prior to the Convert command has no effect on the
curacy of the ADS774. In both the Control and Emulation modes,
internal sample/hold circuit begins slewing to track the input
nal immediately after the conversion is complete.

the Emulation mode, the ADS774 can replace existing, non-
mpling 774 types in almost all applications, without any changes
system hardware or software. It is not necessary that the input
nal be stable before a Convert command arrives, but it must re-
in stable during the acquisition period after the Convert com-
nd is received (as it must with other 774 types) for accurate per-
mance. Unlike other, non-sampling 774 types, the ADS774 allows
input to begin slewing before the end of conversion (after the
μsec acquisition period), so it is possible to increase system
oughput in many cases.

RD-WIRING TO 8-BIT DATA BUSES — For applications with
it data buses, output lines DB4 to DB11 (Pins 20 to 27) should
nect directly to lines D_0 to D_7 in the system data bus. In addition,
put lines DB0 to DB3 (Pins 16 to 19) should connect to lines D_4
D_7 on the system data bus, and to ADS774 output lines DB8 to
11 (Pins 24 to 27). Figure 4 shows the proper connections. Thus
nnected, if A_0 is low during a read operation, the upper 8 bits are
abled and become valid on output pins 20 to 27. When A_0 is high
ing an operation, the 4 LSBs are enabled on output pins 16 to
and the 4 middle bits (Pins 20 to 23) are overridden with zeros.

	D7	D6	D5	D4	D3	D2	D1	D0
gh Byte = 0)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
w Byte = 1)	DB3	DB2	DB1	DB0	0	0	0	0



ure 4. Connection to 8-Bit Bus

AND-ALONE OPERATION — The ADS774 can be used in a
nd-alone mode in systems having dedicated input ports and not
uiring full bus-interface capability. In this mode, $\overline{CE}$ and 12/$\overline{8}$ are
to logic "1" (they may be hard-wired to +5V), $\overline{CS}$ and A_0 are
to logic "0" (they may be grounded), and the conversion is con-
led by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low
suming a conversion is not already in progress), and all 12 bits
he 3-state output buffers are enabled whenever R/$\overline{C}$ is brought
h (assuming Status has already gone low, indicating completion
conversion).

This configuration gives rise to two possible modes of operation. Conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. Figure 5 details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$, and they return to valid logic levels after the conversion cycle is completed. The Status output goes high 200 nsec after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 1000 nsec after data is valid (t_{HS}). In this mode, output data is available most of the time, and becomes invalid only during a conversion.

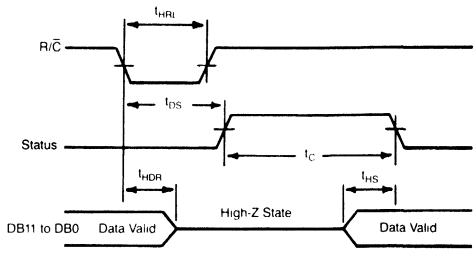


Figure 5. Stand-Alone Mode With Negative Start Pulse.

Figure 6 details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to the high-impedance state and remain in that state until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible most of the time, and becomes valid only when R/$\overline{C}$ goes high. Table 6 gives the timing parameters for the two modes.

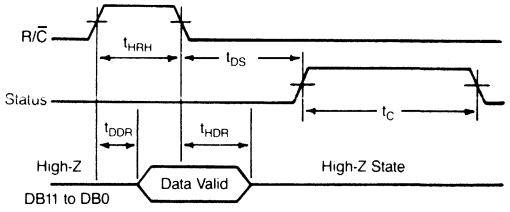


Figure 6. Stand-Alone Mode with Positive Start Pulse.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	25			nsec
t_{DS}	STS Delay after R/C			200	nsec
t_{HDR}	Data Valid after R/C Low	25			nsec
t_{HRH}	High R/C Pulse Width	100			nsec
t_{DDR}	Data Access Time			150	nsec

Table 6. Stand-Alone Mode Timing over T_{MIN} to T_{MAX}

UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating mode are shown in Figure 7. If the 0 to +10V input range is to be used, apply the analog input to Pin 13. If the 0 to +20V input range is to be used, apply the analog input to Pin 14. If the gain adjustment is not needed, replace trim potentiometer R_2 with a fixed, 50Ω 1% metal-film resistor to meet all published specifications. If the offset adjustment is not needed, connect Pin 12 (Bipolar Offset) directly to Pin 9 (Analog Ground).

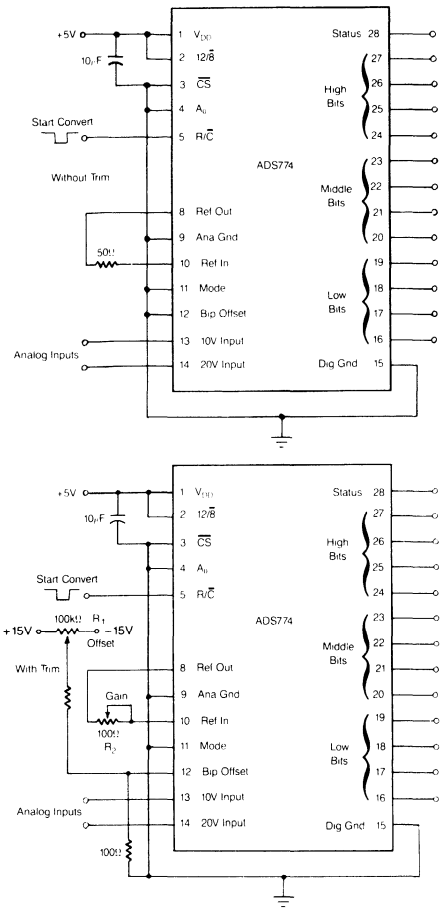


Figure 7. Unipolar Connections

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see section entitled "DIGITAL OUTPUT CODING"). If the offset adjustment is not used, the actual transition will occur within specified limits of its ideal value (+½LSB). For the 10V range, 1 LSB = 2.44mV. For the 20V range, 1 LSB = 4.88mV. To adjust the offset, apply an analog input equal to +½LSB and, with the ADS774 continuously converting, adjust the offset potentiometer down until the digital output is all ones, and then adjust up until the LSB "flickers" between "0" and "1".

Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the unipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal full-scale voltage for the selected input range. This corresponds to +9.9963V and +19.9927V, respectively, for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer up until the digital outputs are all ones, and then adjusting down until the LSB "flickers" between "0" and "1".

In some applications, it is desirable to have the LSB equal exactly 2.5mV (10.24V input range) or 5mV (20.48V input range). To implement these ranges, replace the 100Ω gain trimpot by a 50 Ω fixed resistor. Then insert a 2.7kΩ trimpot in series with Pin 13 for a 10.24V range; Pin 14 for a 20.48V range. Offset trimming then proceeds as described earlier, and the gain trim is effected with the new trimpot.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating mode are shown in Figure 8. If the ±5V input range is to be used, apply the analog input to Pin 13. If the ±10V range is to be used, apply the analog input to Pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trimpots should be replaced by fixed, 50Ω ±1% metal-film resistors to meet all published specifications.

Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see section entitled "DIGITAL OUTPUT CODING"). Ideally, this transition should occur ½LSB below 0V, and if the bipolar offset adjustment is not used, the transition will occur within the specified limit of its ideal value. Offset adjustment in the bipolar configuration is performed not at the zero-crossing point but at the minus full-scale point. The procedure is to apply an analog input equal to −FS + ½LSB (−4.9988V for the ±5V range; −9.9976V for the ±10V range), and adjust the bipolar offset trimpot "down" until the digital output is all zeros. Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the bipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal positive full-scale value of the selected input range. This corresponds to +4.9963V and +9.9927V for the ±5V and ±10V ranges, respectively. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trimpot "up" until the digital outputs are all ones, then adjusting "down" until the LSB "flickers" between "1" and "0".

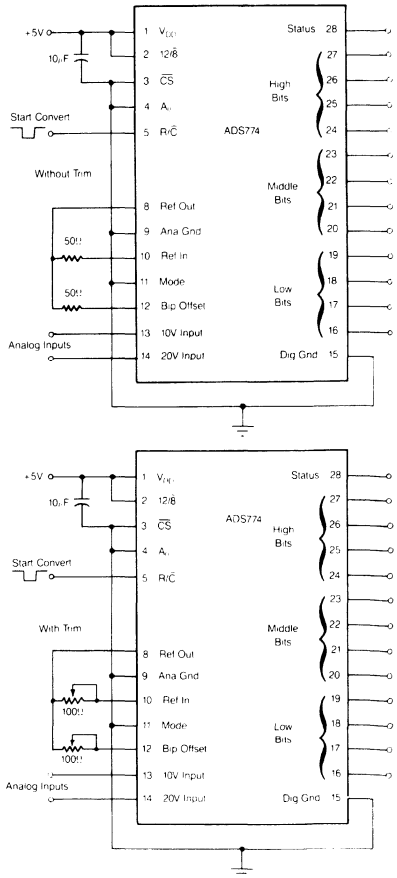


Figure 8. Bipolar Connections

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to +10V	0 to +20V	±5V	±10V	MSB LSB
+10.0000	+20.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+19.9927	+4.9963	+9.9927	1111 1111 111Ø *
+5.0012	+10.0024	+0.0012	+0.0024	1000 0000 000Ø *
+4.9988	+9.9976	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ *
+4.9963	+9.9927	−0.0037	−0.0073	0111 1111 111Ø *
+0.0012	+0.0024	−4.9988	−9.9976	0000 0000 000Ø *
0.0000	0.0000	−5.0000	−10.0000	0000 0000 0000

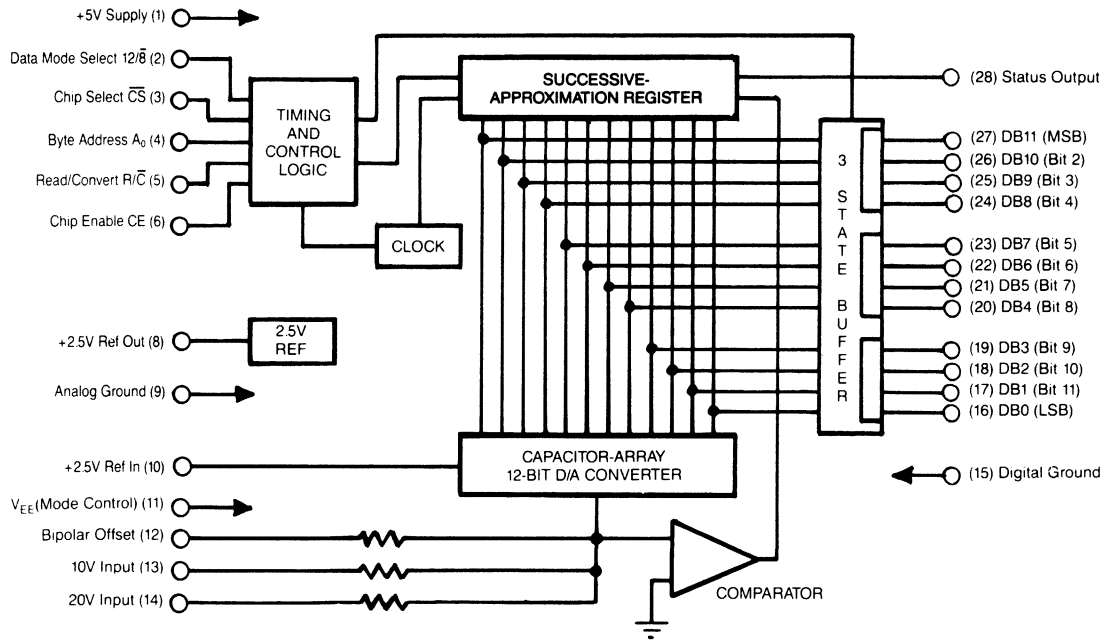
DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits =2.44mV. 1LSB for 11 bits =4.88mV.
4. For 0 to +20V or ±10V input ranges, 1LSB for 12 bits =4.88mV. 1LSB for 11 bits =9.77mV.

* Voltages given are the theoretical values for the transition indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADS774 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

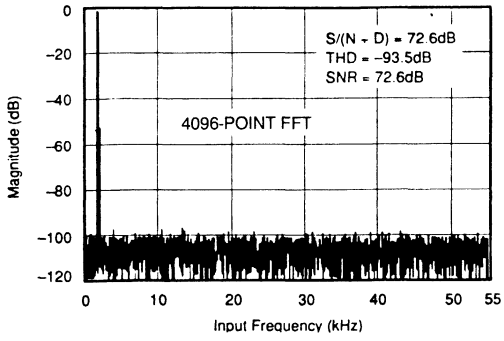
ADS774 BLOCK DIAGRAM



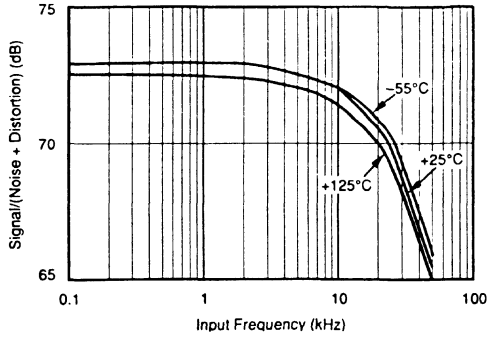
TYPICAL PERFORMANCE

(T_A =25°C, Supplies = +5V, ± 10V Bipolar Input, f_{IN} =110kHz, unless otherwise indicated)

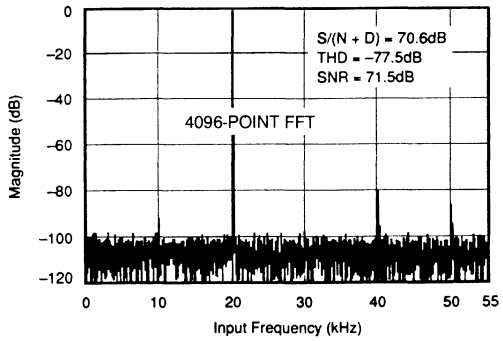
FREQUENCY SPECTRUM (±10V, 2kHz Input)



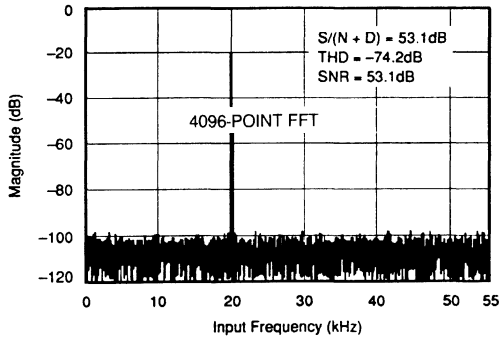
SIGNAL/(NOISE + DISTORTION) vs
INPUT FREQUENCY AND AMBIENT TEMPERATURE



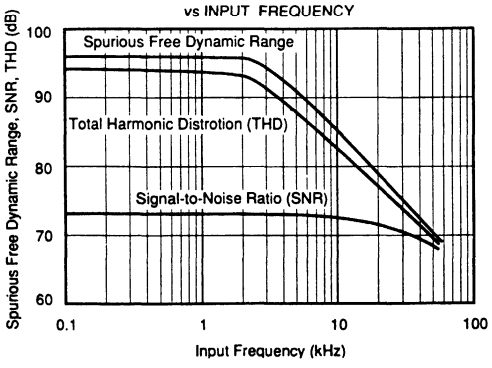
FREQUENCY SPECTRUM (±10V, 20kHz Input)



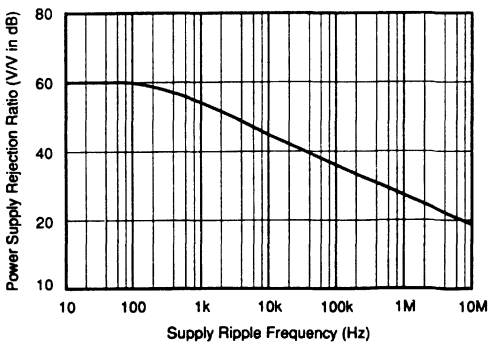
FREQUENCY SPECTRUM (±1V, 20kHz Input)



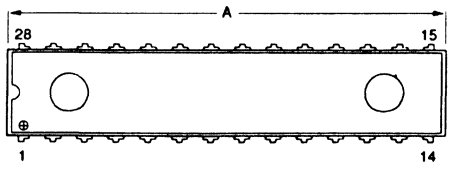
SPURIOUS FREE DYNAMIC RANGE, SNR AND THD
vs INPUT FREQUENCY



POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY

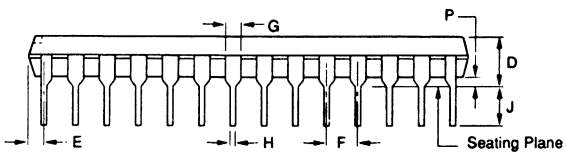


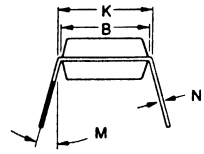
PACKAGE OUTLINES

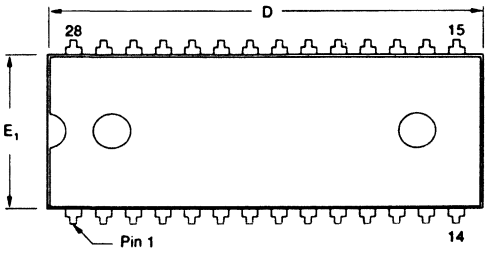


PACKAGE E. PLASTIC SINGLE DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02



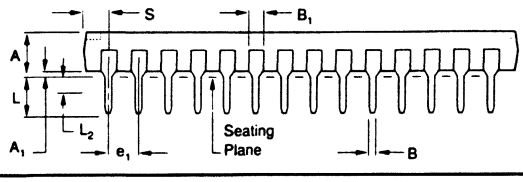


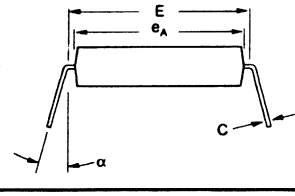


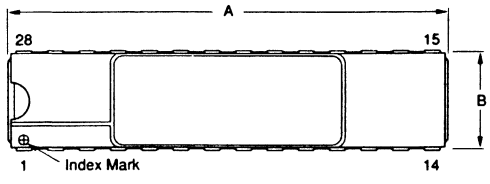
PACKAGE P. PLASTIC DOUBLE DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1(1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1(1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

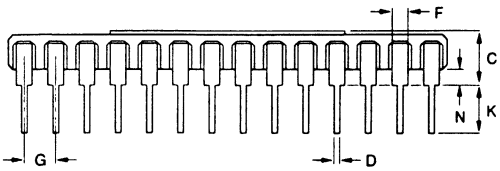


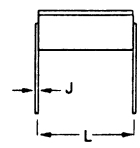




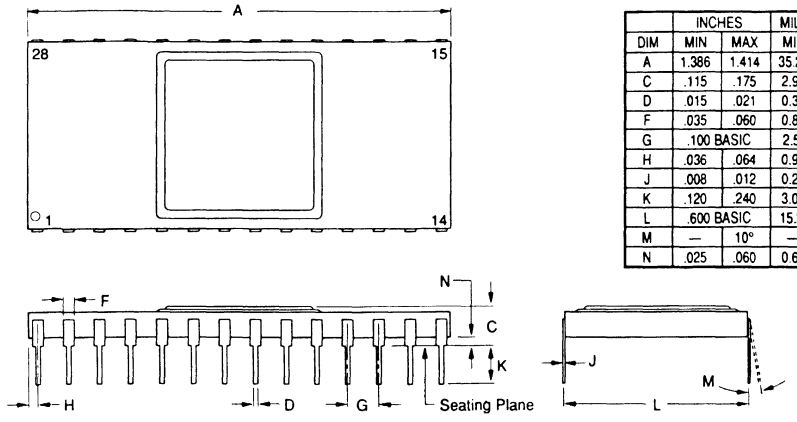
PACKAGE F. CERAMIC HERMETIC SINGLE DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52



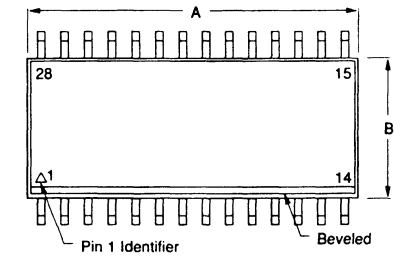


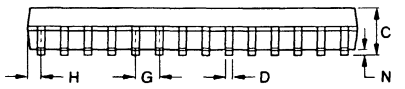
PACKAGE H. CERAMIC HERMETIC DOUBLE DIP

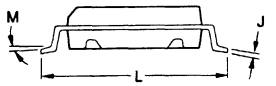


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

PACKAGE U. PLASTIC SOIC







DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MICRO NETWORKS

ADS7800

3μsec, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- 333kHz Over Temperature
- ±5V and ±10V Input Ranges
- AC and DC Performance Completely Specified
- Internal Sample/Hold, Clock, Reference, 3-State Buffer
- 215mW Power Dissipation
- No-Missing-Codes Over Temperature
- 8-Bit or 12-Bit Output Format
- Package Options
  - Plastic DIP
  - Hermetic DIP
  - SOIC

DESCRIPTION

The ADS7800 is a complete, low-cost, 12-bit successive-approximation A/D converter with an internal sample/hold function. The ADS7800 uses an innovative, capacitor-array internal D/A converter, based on CMOS technology. The use of a CMOS architecture results in extremely low power consumption. Total acquisition and conversion time of 3μsec results in a 333kHz sampling rate, over the entire operating temperature range. AC and DC performance are completely specified.

The ADS7800 is complete with internal clock, reference, control logic, and 3-state output buffer. The interface logic provides for easy hand-shaking with most popular 8- and 16-bit microprocessors. The ADS7800's 3-state output buffer connects directly to the μP's data bus, and is readable as either one 12-bit word or two 8-bit bytes. Chip select, high-byte enable, and read/write (read/convert) control inputs enable the ADS7800 to connect directly to a system address bus and control lines, and to operate totally under processor control.

Internal scaling resistors allow a pin-selectable choice of two input ranges: ±5V and ±10V. The ADS7800 is available for operation over the commercial (0°C to +70°C) and industrial (−40°C to +85°C) temperature ranges. Package options include 24-pin single (0.300″) plastic or hermetic ceramic DIPs, and 24-pin plastic SOIC. The ADS7800 operates from a +5V supply and either a −12V or −15V supply.

Model Number	Package	Temperature Range	Linearity Error Max (T_{min} to T_{max})	SINAD* (dB Min.)
ADS7800JP	Plastic DIP	0°C to +70°C	±1	67
ADS7800KP	Plastic DIP	0°C to +70°C	±½	69
ADS7800JU	Plastic SOIC	0°C to +70°C	±1	67
ADS7800KU	Plastic SOIC	0°C to +70°C	±½	69
ADS7800AH	Ceramic DIP	−40°C to +85°C	±1	67
ADS7800BH	Ceramic DIP	−40°C to +85°C	±½	69

*Signal-to-(Noise + Distortion) Ratio.

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ADS7800 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	
J, K Grades	0°C to +70°C
A, B Grades	−40°C to +85°C
Storage Temperature Range:	−65°C to +150°C
$+V_S$ to Digital Ground	+7V
$-V_S$ to Analog Ground	−16.5V
$+V_{SA}$ to $+V_{SD}$	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	−0.3V to V_S +0.3V
Analog Input to Voltage	±20V
Junction Temperature	+160°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation	750mW
Thermal Resistance Θ_{JA}:	
Plastic DIP	100°C/W
SOIC	100°C/W
Ceramic DIP	50°C/W

ORDERING INFORMATION

PART NUMBER ——— **ADS7800 J P**

Select suffix J, K, A or B for desired performance and specific temperature range.

Select suffix P, U or H for desired package option.

DESIGN SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = +5V$, $V_S = -15V$, $f_S = 333kHz$, unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		±10 and ±5		Volts
Input Impedance: ±10V	4.4	6.3	8.1	kΩ
±5V	2.9	4.2	5.4	kΩ
DIGITAL INPUTS CS, R/C, HBE				
Logic Levels: Logic "1"	+2.4		+5.3	Volts
Logic "0"	−0.3		+0.8	Volts
Loading: Logic "1"			+5	μA
Logic "0"			−5	μA
DIGITAL OUTPUTS DB0 to DB11, BUSY				
Output Format		12-Bit Parallel or 8-Bit/4-Bit		
Output Coding		Offset Binary		
Logic Levels: Logic "1" (I_{SOURCE} = 500μA)	+2.4		+5.0	Volts
Logic "0" (I_{SINK} = 1.6mA)	0		+0.4	Volts
Leakage (High-Impedance State)		±0.1	±5	μA
INTERNAL REFERENCE				
Reference Output Voltage (Pin 3)	1.9	2.0	2.1	Volts
Available Output Source Current		10		μA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: $-V_S$ Supply	−11.4	−15	−16.5	Volts
Power Supply Range: $+V_S$ Supply	+4.75	+5.0	+5.25	Volts
Current Drains: $-I_S$		3.5	6	mA
$+I_S$ (Total)		18	25	mA
Power Dissipation		135	215	mW
DYNAMIC CHARACTERISTICS				
Aperture Delay		13		nsec
Aperture Uncertainty (Jitter)		150		psec, rms
Transient Response, Full-Scale Step (Note 1)		130		nsec
Overvoltage Recovery, 2 X FS (Note 2)		150		nsec
CONVERSION TIME				
Conversion Only		2.5	2.7	μsec
Conversion + Acquisition		2.6	3.0	μsec
Throughput Rate	333	380		kHz

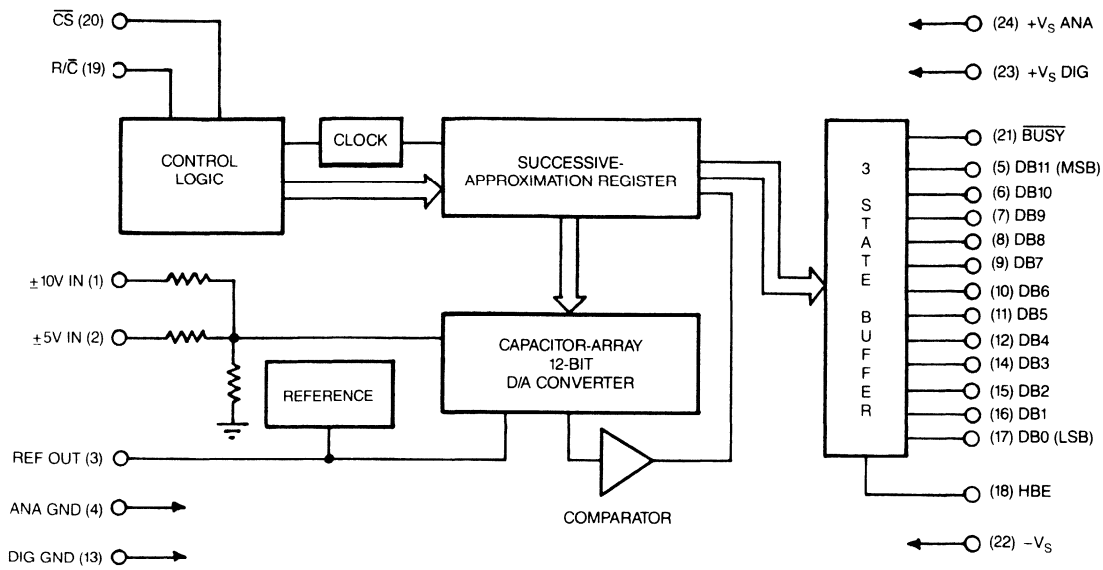
SPECIFICATION NOTES:

1. For 12-bit accuracy in specified time.
2. To specified performance in specified time.
3. Adjustable to zero with external trimpot.
4. Least Significant Bit. 1LSB=2.44mV for the ±5V range; 4.88mV for the ±10V range.
5. Characterized over T_{MIN} to T_{MAX} at +FS, 0V, and −FS. 0.1LSB is typical rms noise with worst-case conditions: +FS at +125°C.
6. All dB figures refer to ±10V or ±5V full-scale input.

CAUTION: These Devices are sensitive to electrostatic discharge. Proper anit-ESD IC handling procedures should be followed.

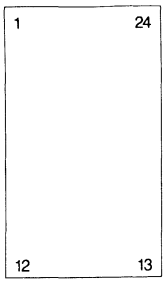
PERFORMANCE SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $+V_S = +5V$, $-V_S = -15V$, $f_S = 333kHz$, unless otherwise indicated)

MODEL	ADS7800JP/JU/AH			ADS7800KP/KU/BH			
TRANSFER CHARACTERISTICS	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
RESOLUTION			12			12	Bits
TRANSFER CHARACTERISTICS							
Full-Scale Error			±0.50			±0.35	%
Full-Scale Error Drift		6			6		ppm/°C
Integral Nonlinearity			±1			±½	LSB(Note 4)
Differential Nonlinearity			±1			±¾	LSB
Resolution for No Missing Codes	12			12			Bits
Bipolar Zero Error (Note 3)			±4			±2	LSB
Bipolar Zero Error Drift		1			1		ppm/°C
Transition Noise (Note 5)		0.1			0.1		LSB
AC ACCURACY (Note 6)							
Spurious-Free Dynamic Range	74	77		77	80		dB
Total Harmonic Distortion		−77	−74		−80	−77	dB
Signal-to-Noise Ratio	68	71		70	73		dB
Signal-to-(Noise+Distortion) Ratio (SINAD)	67	70		69	72		dB
Intermodulation Distortion (−6dB Signals) (f_{IN1} = 24.4kHz; f_{IN2} = 28.5kHz)		−77	−74		−77	−74	dB
POWER SUPPLY SENSITIVITY							
$-V_S = -13.5V$ to $-16.5V$			±½			±½	LSB
$-V_S = -11.4V$ to $-12.6V$			±½			±½	LSB
$+V_S = +4.75V$ to $+5.25V$			±1			±½	LSB
TEMPERATURE RANGE							
Specified: JP/JU/KP/KU Models	0		+70	0		+70	°C
AH/BH/ Models	−40		+85	−40		+85	°C
Storage	−65		+150	−65		+150	°C



ADS7800 BLOCK DIAGRAM

PIN DESIGNATIONS



1 ±10V Analog Input. Ground for ±5 range.
2 ±5V Analog Input. Ground for ±10V range.
3 +2V Reference Output
4 Analog Ground. Connect to Pin 13.
5 Data Bit 11 (MSB)
6 Data Bit 10
7 Data Bit 9
8 Data Bit 8
9 Data Bit 7 if HBE Low; "0" if HBE High.
10 Data Bit 6 if HBE Low; "0" if HBE High.
11 Data Bit 5 if HBE Low; "0" if HBE High.
12 Data Bit 4 if HBE Low; "0" if HBE High.
24 +5V Analog Power Supply. Connect to Pin 23.
23 +5V Digital Power Supply. Connect to Pin 24
22 −12V or −15V Negative Power Supply
21 $\overline{BUSY}$
20 $\overline{CS}$ Chip Select
19 R/C Read/Convert
18 HBE High Byte Enable
17 Data Bit 0 (LSB) if HBE Low, Data Bit 8 if HBE High.
16 Data Bit 1 if HBE Low; Data Bit 9 if HBE High.
15 Data Bit 2 if HBE Low; Data Bit 10 if HBE High.
14 Data Bit 3 if HBE Low; Data Bit 11 if HBE High.
13 Digital Ground. Connect to Pin 4.

DESCRIPTION OF OPERATION

The ADS7800 is a complete 12-bit A/D converter. It uses the successive-approximation conversion technique and incorporates all required function blocks — capacitor-array D/A converter, comparator, clock, reference, and control logic. The CMOS-based capacitor-array architecture provides an inherent sample/hold function. The device mates directly to most popular 8-, 16-, and 32-bit microprocessors and contains all the necessary address-decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most cases, the ADS7800 will require only power supplies and bypass capacitors to provide the complete A/D conversion function. The completeness of the device makes it most convenient to think of the ADS7800 as a function block with specific input/output transfer characteristics; it is thus quite unnecessary to be concerned with its inner workings.

BASIC OPERATION — Figure 1 gives the basic connections for operating the ADS7800 with the ±10V input range in Convert mode. The Convert command R/$\overline{C}$, applied to Pin 19, puts the ADS7800 in Hold mode and initiates the conversion. R/$\overline{C}$ must hold Pin 19 low for at least 40nsec. The $\overline{BUSY}$ signal on Pin 21 is held low during the conversion, and goes high after the conversion is completed and the data is transferred to the output latches. The rising edge of the signal on Pin 21 can thus serve to read the converted data.

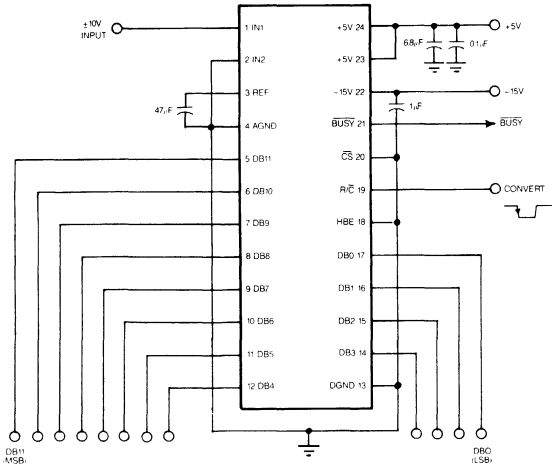


Figure 1. Basic ±10V Connection Diagram

During the conversion, the $\overline{BUSY}$ signal imposes the high-impedance state on the output data lines and also inhibits input lines. The inhibition causes Pin 19 to ignore any pulses, so new conversions cannot be initiated while a conversion is taking place, whether the pulses result from spurious sources or an attempt to short-cycle the conversion.

In Read mode, Pin 19 is held low, and a high-going pulse serves to read data and initiate a conversion. In Read mode, the rising edge of the R/$\overline{C}$ signal on Pin 19 enables the output data pins, thus validating the data from the previous conversion. The falling edge of R/$\overline{C}$ then puts the ADS7800 in Hold mode and initiates a new conversion. The ADS7800 will begin acquiring a new signal upon the completion of the conversion, even before the $\overline{BUSY}$ signal rises on Pin 21, and will track the input signal until the start of the next conversion, whether the ADS7800 is in Convert or Read mode.

The signal HBE on Pin 18 allows the ADS7800 to be used with an 8-bit bus. At the end of a conversion, a low input on Pin 18 loads the eight LSBs of data into the latches of Pins 9 through 12 and 14 through 17. A high signal on Pin 18 then loads the four MSBs into the latches of Pins 14 through 17, and Pins 9 through 12 are forced low. Figure 2 and Table 1 give the timing parameters for the basic acquisition and conversion operations.

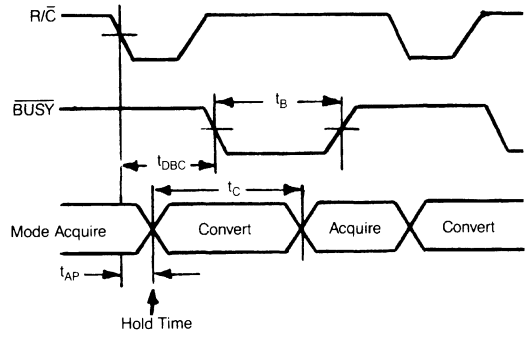


Figure 2. Conversion and Acquisition Timing

Symbol	Parameter	Typ	Max	Units
t_{DBC}	$\overline{BUSY}$ Delay from R/C	80	150	nsec
t_B	$\overline{BUSY}$ Low	2.5	2.7	µsec
t_{AP}	Aperture Delay	13		nsec
Δt_{AP}	Aperture Jitter	150		psec, rms
t_C	Conversion Time	2.47	2.70	µsec

Table 1. Acquisition and Conversion Timing

CONTROL FUNCTIONS — The ADS7800 offers easy interface to most digital systems, whether microprocessor-based or other. The ADS7800 can operate under complete microprocessor control, or in a stand- alone mode, in which it is controlled only by the R/$\overline{C}$ input on Pin 19. Microprocessor control entails initiating the conversion and reading the output data, either in one 12-bit parallel word or in two 8-bit bytes. All control inputs ($\overline{CS}$, R/$\overline{C}$, and HBE) are TTL- and CMOS-compatible. Tables 2 and 3 detail the functions of the control inputs.

Pin No.	Symbol	Function
18	HBE	High Byte Enable. When held Low, data output has 12-bit parallel format. When held High, 4 MSBs appear on Pins 14 to 17; zeros appear on Pins 9 to 12. Must be Low to initiate conversion.
19	R/$\overline{C}$	Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is Low, HBE is Low, and $\overline{BUSY}$ is High.
20	$\overline{CS}$	Chip Select. Outputs in High-Z state when $\overline{CS}$ is High. Must be Low to initiate conversion or read data.
21	$\overline{BUSY}$	Busy, Output Low during conversion. Data valid on rising edge in Convert mode.

Table 2. Role of Control Functions

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	Operation
1	X	X	1	None — Outputs in High-Z State.
0	1→0	0	1	Holds Signal and Starts Conversion.
0	1	0	1	3-State Output Buffers Enabled Upon End of Conversion.
0	1	1	1	Enable High Byte in 8-Bit Bus Mode.
0	1→0	1	1	Inhibits Start of Conversion.
X	X	X	0	Conversion in Progress. Outputs in High-Z State. New Conversion Inhibited Until End of Present Conversion.

X="Don't Care".

Table 3. Control Functions

In stand-alone mode, a single control line connected to R/$\overline{C}$ controls the ADS7800. $\overline{CS}$ and HBE are grounded in this mode. The output data is in 12-bit parallel format. Stand-alone mode is useful in systems using dedicated input ports that do not require full bus-interface capability.

A high-to-low transition on R/$\overline{C}$ initiates a conversion. The 3-state output latches are enabled when R/$\overline{C}$ and $\overline{BUSY}$ are high. Thus, two modes of operation are possible: Either positive or negative pulses can initiate a conversion. Either way, the R/$\overline{C}$ pulse must remain low for at least 40nsec.

Figure 3 and Table 4 give timing details for a conversion initiated by a negative R/$\overline{C}$ pulse. In this case (referred to as Convert mode), the 3-state outputs revert to the high-impedance state in response to the falling edge of R/$\overline{C}$, and become enabled for data access after the completion of the conversion.

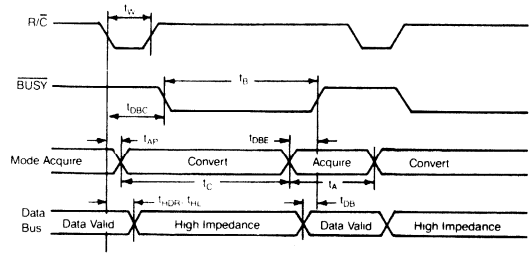


Figure 3. Timing with Negative R/C Pulse

Symbol	Parameter	Min.	Typ.	Max.	Units
t_W	R/$\overline{C}$ Pulse Width	40	10		nsec
t_{DBC}	$\overline{BUSY}$ Delay from R/$\overline{C}$		80	150	nsec
t_B	$\overline{BUSY}$ Low		2.5	2.7	μsec
t_{AP}	Aperture Delay		13		nsec
Δt_{AP}	Aperture Jitter		150		psec, rms
t_C	Conversion Time		2.47	2.7	μsec
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		nsec
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	nsec
t_A	Acquisition Time		130	300	nsec
$t_A + t_C$	Total Throughput Time		2.6	3.0	μsec
t_{HDR}	Valid Data Held after R/$\overline{C}$ Low	20	50		nsec
t_S	$\overline{CS}$ or HBE Low before R/$\overline{C}$ 1→0 Transition	25	5		nsec
t_H	$\overline{CS}$ or HBE Low after R/$\overline{C}$ 1→0 Transition	25	0		nsec
t_{DD}	Data Valid from $\overline{CS}$ Low, R/$\overline{C}$ High, and HBE as Selected (100-pF Load)		65	150	nsec
t_{HDR}	Valid Data Held after R/$\overline{C}$ Low	20	50		nsec
t_{HL}	Delay to High-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown)		50	150	nsec

Table 4. Timing Specifications Over T_{MIN} to T_{MAX}.

Figure 4 and Table 4 detail the timing considerations for a conversion initiated by a positive R/$\overline{C}$ pulse. In this case (referred to as Read mode), output data from a previous conversion is enabled during the high portion of R/$\overline{C}$. The falling edge of R/$\overline{C}$ initiates a new conversion, and the 3-state outputs revert to the high-impedance state until R/$\overline{C}$ again attains a high state.

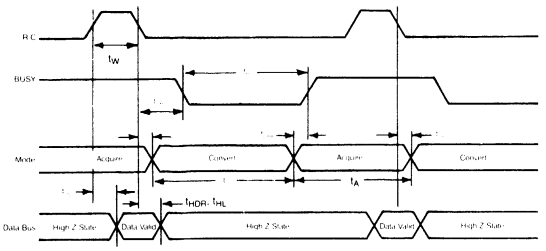


Figure 4. Timing with Positive R/$\overline{C}$ Pulse

TIMING — INITIATING CONVERSIONS — As seen in Table 1, only a negative-going transition on R/$\overline{C}$–no other combination of states or transitions–can initiate a conversion in the ADS7800. $\overline{CS}$ or HBE high, or $\overline{BUSY}$ low, will inhibit conversion. $\overline{CS}$ and HBE should be stable for at least 25 nsec prior to the R/$\overline{C}$ transition. Figure 5 shows the timing details for initiation of a conversion.

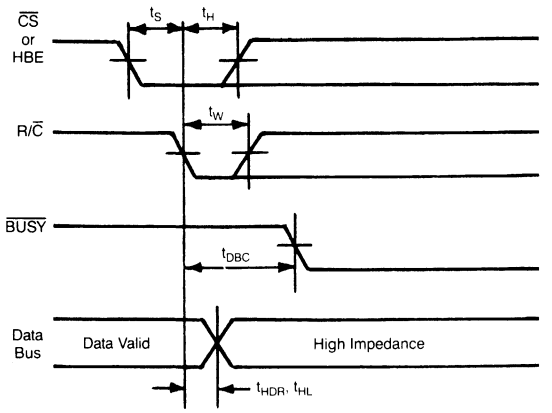


Figure 5. Conversion Initiation Timing

The $\overline{BUSY}$ line, in a low state only during a conversion, shows the status of the converter. During the conversion, the 3-state output latches remain in a high-impedance state; therefore, data is inaccessible during a conversion. During the conversion, the digital inputs $\overline{CS}$, R/$\overline{C}$, and HBE are immune to additional transitions, so conversions cannot be prematurely terminated or restarted.

TIMING — READING DATA — After the start of a conversion, the 3-state output buffers remain in a high-impedance state until the following logic combination exists: R/$\overline{C}$ is high, $\overline{BUSY}$ is high, and $\overline{CS}$ is low. When this combination occurs, the 3-state data lines are enabled in accordance with the state of HBE. Figure 6 and Table 4 give details of the timing relationships and specifications for reading data.

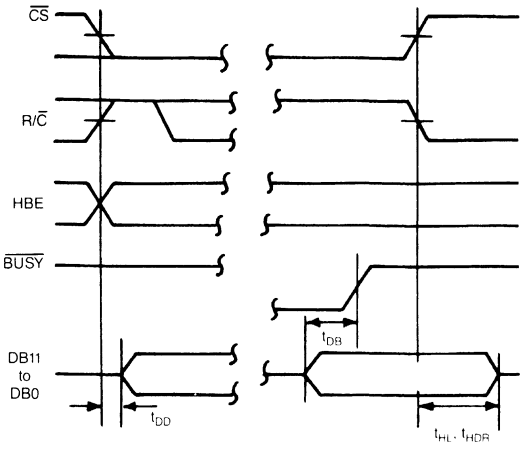


Figure 6. Read Cycle Timing

INTERNAL CLOCK — A factory-trimmed internal clock in the ADS7800 yields a typical conversion time of 2.47μsec at 25°C, and a maximum conversion time of 2.7μsec over the entire operating temperature range. This conversion time, coupled with a guaranteed maximum acquisition time of 300nsec, ensures a 333kHz minimum throughput rate under all conditions.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the ADS7800 are shown in Figure 7. If the ±5V input range is to be used, apply the analog input to Pin 2 and ground Pin 1. If the ±10V range is to be used, apply the analog input to Pin 1 and ground Pin 2. If either offset or gain adjustments are not to be used, the ADS7800 will perform to the limits in the specification table.

Bipolar offset (zero) error can be defined as the accuracy of the 0111 1111 1111 to 1000 0000 0000 transition voltage (-2.44mV for the ±10V range; -1.22mV for the ±5V range). With the ADS7800 converting continuously, adjust the 10kΩ trimpot "up" until the output code is 1000 0000 0000, then adjust "down" until all bits are "flickering" between "0" and "1".

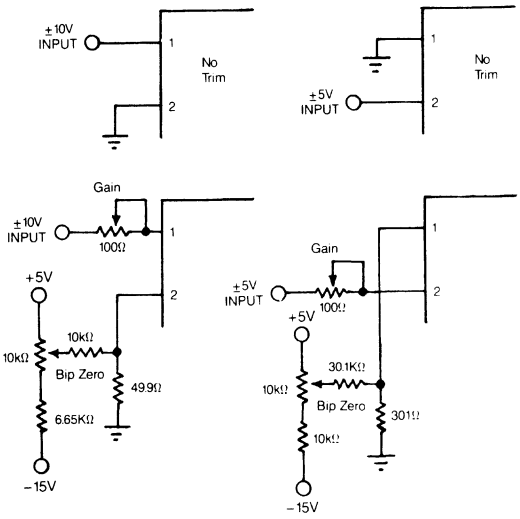


Figure 7. Connections and Calibration

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the bipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal positive full-scale value of the selected input range. This corresponds to +4.9963V and +9.9927V for the ±5V and ±10V ranges, respectively. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trimpot "up" until the digital outputs are all ones, then adjusting "down" until the LSB "flickers" between "1" and "0".

LAYOUT CONSIDERATIONS AND GROUNDING — The ADS7800 has two +5V supply pins: V_{SA} (Pin 24) and V_{SD} (Pin 23). To achieve maximum accuracy in the ADS7800, these supplies are not connected internally. They should be connected together on the printed- circuit board, at a point as close as possible to the ADS7800. Both supply lines should be well isolated from digital supplies that are subject to large load variations. As a general rule, it is good practice to isolate the analog portions of a system from the effects of digital switching by running a separate +5V supply line from a supply regulator to the analog components.

To minimize noise, the tied-together V_S Pins 23 and 24 should be bypassed to ground with a 6.8μF tantalum capacitor in parallel with a 0.1μF multilayer ceramic capacitor. The $-V_S$ Pin 22 should also be bypassed to ground with a 1μF tantalum capacitor. All bypass capacitors should be connected as close as possible to the ADS7800.

These bypassing measures are extremely important, as noise on the power-supply lines can degrade converter performance. It is necessary to pay special attention to filtering out noise and spikes when a switching power supply is used.

The analog (Pin 4) and digital (Pin 13) ground pins are also not connected internally, and should be connected together as close as possible to the ADS7800. The use of a ground plane on the printed- circuit board is highly recommended, as it optimizes high- frequency ground characteristics and reduces noise coupling into sensitive converter circuitry. It is especially important to reference the analog input to the analog ground on Pin 4, to eliminate from the input circuitry any voltage drops that might occur in the power-supply ground returns.

It is necessary to take the input impedance of the ADS7800 into account when designing the analog drive circuitry. The output impedance of the driver should be negligible with respect to the 6.3kΩ (±10V range) or 4.2kΩ (±5V range) input impedance of the ADS7800, or at least invariant with respect to signal level. Further, it is crucial to prevent any coupling between the analog input lines and digital signal lines. If these lines must cross, it is recommended that they do so at right angles, and with a minimum of crossover area. If they must run parallel for any distance, it is good design practice to insert a ground pattern between them as a shield. Any external trimpots used for full-scale or offset adjustments should be mounted as close to the converter as possible.

It is necessary to bypass the reference output (Pin 3) with a 22μF to 47μF, 2V tantalum capacitor. The drive capability of this pin is limited (10μA typ), so it is necessary to provide buffering if this reference voltage is to be used in other parts of the system.

POWER-SUPPLY SEQUENCING PRECAUTIONS — If the two +5V supply inputs of the ADS7800 are powered-up sequentially instead of simultaneously, the converter may experience latch-up and draw excessive current. Connecting the two supply pins together on the printed-circuit board will normally prevent this problem. However, the phenomenon can occur if the ADS7800 is plugged into a live socket-- for example, during incoming inspection or lab evaluation. In these cases, it is necessary to ensure that power is applied only after the ADS7800 has been plugged in.

AVOIDING TRANSIENT PHENOMENA — Various transients coupled into the ADS7800 can cause errors that may difficult to diagnose. If errors persist despite careful grounding and bypassing measures, they might find their origins in one or more not-so-obvious transient phenomena. A checklist of several transient-avoidance steps can be useful in designing a new system.

Transients that occur during critical periods in the conversion process can produce errors. For example, a clean, sharp Hold command ("1" to "0" transition on R/C) signal is crucial to error- free operation. This edge should be clean and sharp and free from significant ringing, especially in the 20nsec period after it occurs. Another not-so-obvious helpful design practice is to avoid any transitions on digital lines during the bit decisions in the conversion process. So it is prudent to avoid any changes in R/C at the time of any bit decisions. Keeping the R/C pulse short (< 100nsec) will avoid a transition at the time of the MSB decision, or keeping it long (> 2.7μsec) will avoid affecting the LSB decision.

High-speed bus transients can also couple into the ADS7800 via the data outputs, even when the output buffers are in the high- impedance state. If such transients exist, it is good practice to isolate them from the converter by providing additional buffering to the data outputs. The BUSY line can serve to enable these added buffers.

It goes without saying that transients on the analog inputs are to be avoided scrupulously, especially in the interval within ±20nsec of the "1"-to-"0" transition of R/C, when they may affect the charge transferred to the capacitor array. Careful layout and design of the analog drive circuitry are necessary to avoid these transients. Finally, in multiplexed systems, it is most prudent to switch channels in the multiplexer only after the conversion is complete. Otherwise, glitches or ringing in the switched signal may be coupled into the ADS7800 during the conversion process.

DIGITAL OUTPUT CODING

ANALOG INPUT (Volts)		DIGITAL OUTPUT
±5V	±10V	MSB LSB
+5.0000	+10.0000	1111 1111 1111
+4.9963	+9.9927	1111 1111 111Ø *
+0.0012	+0.0024	1000 0000 000Ø *
-0.0012	-0.0024	ØØØØ ØØØØ ØØØØ *
-0.0037	-0.0073	0111 1111 111Ø *
-4.9988	-9.9976	0000 0000 000Ø *
-5.0000	-10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

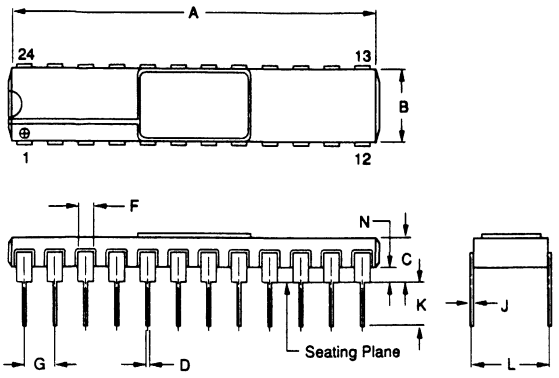
1. Output coding is offset binary.
2. For ±5V input range, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
3. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a logic "1" to a logic "0" or visa versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADS7800 operating on its ±10V input range, the transition from digital output 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of -9.9976 volts. Subsequently, any input voltage more negative than -9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of -0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

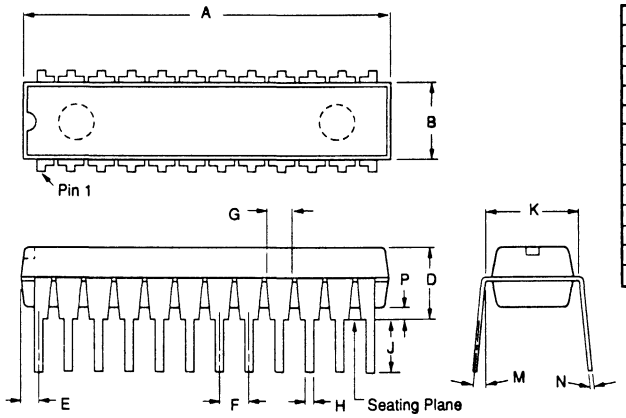
PACKAGE OUTLINES

PACKAGE H. CERAMIC HERMETIC DIP



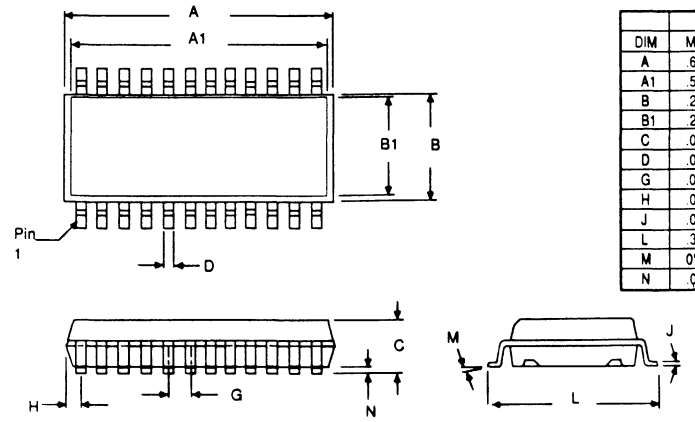
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.188	1.212	30.18	30.78
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

PACKAGE P. PLASTIC DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
D	.150	.170	3.81	4.32
E	.010	.080	.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78
H	.016	.020	0.41	0.51
J	.125		3.18	
K	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	.25	.76

PACKAGE U. PLASTIC SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.602	.618	15.29	15.70
A1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

MICRO NETWORKS

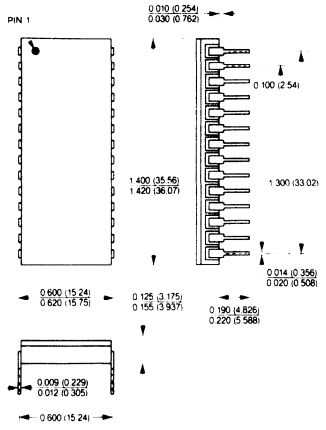
MN6227
MN6228

WIDEBAND, SAMPLING
12-Bit A/D
CONVERTERS

FEATURES

- **33kHz Sampling Rate With Internal T/H Amplifier**
- **16.5kHz Full-Power Input Bandwidth**
- **70dB Signal-to-Noise Ratio Over Full Bandwidth**
- **−80dB Harmonics Over Full Bandwidth**
- **Full 8 or 16-Bit μP Interface: CS, CE, R/C, A_0, 12/8 150nsec Bus Access Time**
- **Industry-Standard MN574A Package and Pinout**
- **1100mW Max Power**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**

28 PIN DIP



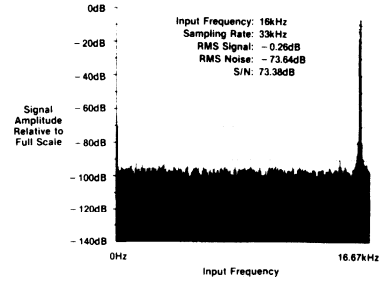
Dimensions in Inches (millimeters)

DESCRIPTION

MN6227 and MN6228 are the first, general-purpose, high-speed, 12-bit, sampling A/D converters designed and specified for contemporary DSP applications in the fields of spectrum analysis, voice recognition, vibration analysis, signature recognition, and others. These devices consist of high-speed (25μsec), μP interfaced (CS, CE, read/convert, 3-state buffer, etc.), successive-approximation type, 12-bit A/D converters with internal, high-speed, track-hold (T/H) amplifiers. They have the ability to accurately sample and digitize transient or periodic input signals with slew-rate and frequency content orders of magnitude higher than can be converted by an A/D without a companion T/H.

MN6227 (10V input span) and MN6228 (20V input span) are configured in a manner that makes the T/H transparent to the user. There are no confusing acquisition time, aperture delay, or aperture jitter specifications. These are true sampling, broadband A/D converters that are specified accordingly. Sampling rate, analog-input full-power bandwidth, harmonic distortion, and signal-to-noise ratio (SNR, rms-to-rms) are all fully specified. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's (see sample spectrum below).

These devices are packaged in small, low-profile, 28-pin, side-brazed, ceramic DIP's and have the industry-standard MN574A pinout. Devices are fully specified for 0°C to +70°C (J and K models) or −55°C to +125°C (S and T models) operation.



May 1988

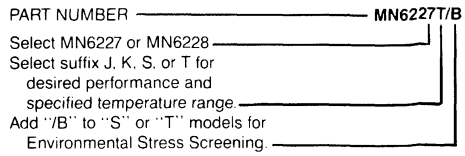
MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN6227 MN6228 WIDEBAND SAMPLING 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6227J, K; MN6228J, K	0°C to +70°C
MN6227S, S/B, T, T/B	−55°C to +125°C
MN6228S, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+V_{dd} +0.5) Volts
Analog Inputs: Pins 10 and 12	±15 Volts
Pin 13 (MN6227)	±15 Volts
Pin 14 (MN6228)	±15 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref Out (Pin 8) Short Circuit Duration	Continuous to Ground

ORDERING INFORMATION



DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: MN6227		0 to +10, ±5		Volts
MN6228		±10		Volts
Input Impedance (Note 16): Resistance	1	5		Mohm
Capacitance		50		pF
Input Bias Current Over Full Temperature Range (Note 16):		±100	±600	nA
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8				
Logic Levels: Logic "1"	+2.4			Volts
Logic "0"			+0.8	Volts
Loading: Logic Currents		±1	±10	μA
Input Capacitance (Note 16)		5		pF
DIGITAL OUTPUTS DBO — DB11, STS				
Output Coding (Note 2): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" (I_{source} ≤ 320μA)	+2.4			Volts
Logic "0" (I_{sink} ≤ 1.6mA)			+0.4	Volts
Leakage (DBO—DB11) in High-Z State		±1	±10	μA
Output Capacitance (Note 16)		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10	+10.1	Volts
Drift (Note 16)		±15		ppm/°C
Output Current (Notes 3, 16)			1	mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supplies	±14.5	±15	±15.5	Volts
+V_{dd} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection (Note 14): +V_{CC} Supply	−50			dB
−V_{CC} Supply	−50			dB
+V_{dd} Supply	−50			dB
Current Drains: +V_{CC} Supply		+22	+28	mA
−V_{CC} Supply		−34	−40	mA
+V_{dd} Supply		+9	+15	mA
Power Consumption		885	1095	mW

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated)

DYNAMIC CHARACTERISTICS	MN6227J MN6228J	MN6227K MN6228K	MN6227S MN6228S	MN6227T MN6228T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	33	33	33	33	kHz
Maximum A/D Conversion Time (Note 5)	25	25	25	25	μsec
Signal-to-Noise Ratio (SNR, Note 6):					
Initial (+25°C) (Minimum)	68	70	68	70	dB
T_{min} to T_{max} (Minimum, Note 7)	66	68	66	68	dB
Harmonics and Spurious Noise (Note 8):					
Initial (+25°C) (Minimum)	−77	−80	−77	−80	dB
T_{min} to T_{max} (Minimum, Note 7)	−74	−77	−74	−77	dB
Input Signal Full-Scale Bandwidth (Minimum, Note 9)	16.5	16.5	16.5	16.5	kHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C) (Maximum)	±1	±½	±1	±½	LSB
T_{min} to T_{max} (Maximum, Note 7)	±1	±½	±1	±1	LSB
Resolution for Which No Missing					
Codes is Guaranteed: Initial (+25°C)	11	12	11	12	Bits
T_{min} to T_{max} (Note 7)	11	12	11	12	Bits
Unipolar Offset Error (Notes 10, 11):					
Initial (+25°C) (Maximum)	±2	±2	±2	±2	LSB
Drift (Maximum)	±10	±5	±10	±5	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±2	±1	±4	±2	LSB
Bipolar Zero Error (Notes 10, 12):					
Initial (+25°C) (Maximum)	±4	±4	±4	±4	LSB
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±3	±2	±6	±4	LSB
Full Scale Accuracy Error (Notes 10, 13):					
Initial (+25°C) (Maximum)	±0.2	±0.1	±0.2	±0.1	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.4	±0.2	±0.7	±0.4	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.2	±0.1	±0.5	±0.3	%FSR
Drift (Maximum)	±50	±25	±50	±25	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±10	±5	±20	±10	LSB

SPECIFICATION NOTES:

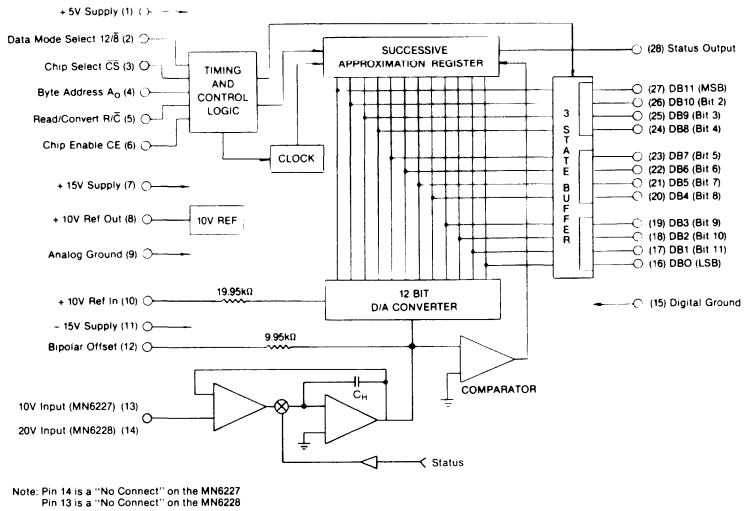
1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. See table of transition voltages in section labeled Digital Output Coding.
3. If the internal reference is used to drive an external load, the load should not change during a conversion.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 33kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at rates of 40kHz or higher.
5. Whenever the Status Output (pin 28) is low (logic "0"), the internal T/H is in the track mode and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0db) at any frequency up to 16.5kHz.
7. MN6227J, K and MN6228J, K are fully specified for 0°C to +70°C operation. MN6227S, S/B, T, T/B and MN6228S, S/B, T, T/B are fully specified for −55°C to +125°C operation.
8. This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
9. This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 33kHz rate.
10. Adjustable to zero with external potentiometer.
11. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN6227 on its unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
12. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN6227/6228 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding. Listed specs assume fixed 50Ω resistors between Ref Out (pin 8) and Ref In (pin 10) and between Ref Out (pin 8) and Bipolar Offset (pin 12).
13. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 to 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding. Listed specs assume fixed 50Ω resistors between Ref Out (pin 8) and Ref In (pin 10) and between Ref Out (pin 8) and Bipolar Offset (pin 12).
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
15. Listed maximum change specifications for unipolar offset, bipolar zero and full-scale accuracy correspond to the maximum change from the initial value (+25°C) to the value at T_{min} or T_{max}.
16. These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

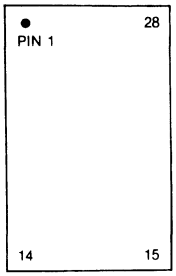
Part Number	Input Voltage Range		Specified Temperature Range	No Missing Codes	Integral Linearity	Minimum Sampling Rate	Minimum input Bandwidth	SNR	Harmonics
	Unipolar	Bipolar							
MN6227J	0 to +10V	±5V	0°C to +70°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6227K	0 to +10V	±5V	0°C to +70°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6227S	0 to +10V	±5V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6227S/B	0 to +10V	±5V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6227T	0 to +10V	±5V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6227T/B	0 to +10V	±5V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6228J	N.A.	±10V	0°C to +70°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6228K	N.A.	±10V	0°C to +70°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6228S	N.A.	±10V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6228S/B	N.A.	±10V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6228T	N.A.	±10V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6228T/B	N.A.	±10V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB

BLOCK DIAGRAM



Note: Pin 14 is a "No Connect" on the MN6227
Pin 13 is a "No Connect" on the MN6228

PIN DESIGNATIONS



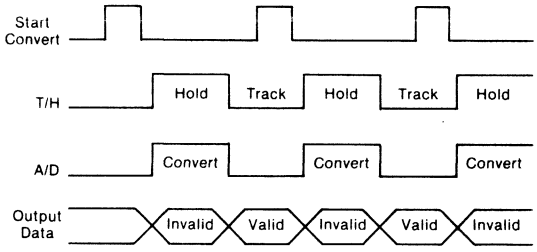
(1)	+5V Supply (+V_{dd})	(28)	Status Output
(2)	Data Mode Select 12/$\overline{8}$	(27)	DB11 (MSB)
(3)	Chip Select $\overline{CS}$	(26)	DB10 (Bit 2)
(4)	Byte Address A_0	(25)	DB9 (Bit 3)
(5)	Read/Convert R/$\overline{C}$	(24)	DB8 (Bit 4)
(6)	Chip Enable CE	(23)	DB7 (Bit 5)
(7)	+15V Supply (+V_{cc})	(22)	DB6 (Bit 6)
(8)	+10V Ref Out	(21)	DB5 (Bit 7)
(9)	Analog Ground	(20)	DB4 (Bit 8)
(10)	+10V Ref In	(19)	DB3 (Bit 9)
(11)	−15V Supply (−V_{cc})	(18)	DB2 (Bit 10)
(12)	Bipolar Offset	(17)	DB1 (Bit 11)
(13)	Analog Input MN6227 (N.C. MN6228)	(16)	DB0 (LSB)
(14)	Analog Input MN6228 (N.C. MN6227)	(15)	Digital Ground

DESCRIPTION OF OPERATION

MN6227 and MN6228 are complete, 12-bit A/D converters with internal microprocessor-interface logic and internal track-hold (T/H) amplifiers. They have been designed to repetitively sample and digitize dynamically changing input signals in DSP-type applications. The A/D-converter sections of these devices employ the successive-approximation (SA) conversion technique, and A/D's of this type, while offering excellent tradeoffs in terms of speed, resolution, and power consumption, are nortoriously poor in their ability to accurately convert dynamically changing (slewing) analog-input signals. In fact, the A/D converter section of the MN6227/6228 has a 25μsec conversion time, and if it did not have a T/H, it would be effectively incapable of accurately digitizing a signal slewing more than ± ½ LSB during that period. This corresponds to an input slew-rate limit of ± 0.098mV/μsec (for a device with a ± 10V input range) or a full-scale, sinusoidal, input bandwidth of 1.56Hz. The input bandwidth of MN6227/6228 is increased more than 4 orders of magnitude by its internal T/H amp. When these converters are commanded to perform a conversion, the T/H instantaneously "freezes" the input signal and holds it constant while the A/D converter performs a conversion.

The T/H is configured in such a manner as to be transparent to the user. A high-impedance input buffer isolates it from the external signal source, and its output is internally connected directly to the A/D. Its operational state is controlled by the A/D in the sense that whenever the A/D is performing a conversion (Status Line = "1"), the T/H is driven into its hold mode, and when the A/D is between conversions (Status Line = "0"), the T/H is in its track (signal acquistion) mode.

MN6227/6228 TIMING



When the A/D is not converting and the T/H is acquiring a new signal, digital output data from the previous conversion is valid and ready to be read.

MN6227/6228 are designed such that when conversions are initiated at any rate up to 33kHz, enough time remains between the falling edge of Status and the next Start Convert command for the T/H to fully acquire its next sample. When the device is clocked at a 33kHz sampling rate, the T/H has the ability to accurately acquire, track, and hold full-scale input signals with frequency components up to 16.5kHz. In most DSP-type applications, MN6227/6228 will be required to repetitively sample and digitize input signals with frequencies below 16.5kHz. This will ensure that the Nyquist criterion of sampling 2 times per period is achieved. Similarly, it ensures that the sampling (and digitizing) frequency (33kHz) is at least 2 times the signal frequency.

In most applications, MN6227/6228 will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete sampling/conversion function. The completeness of the device makes it most convenient to think of MN6227/6228 as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating MN6227/6228 under microprocessor control (it also functions as a stand-alone A/D) will consist, in most applications, of a series of read and write operations. Initiating a conversion involves sending a command from the processor to the A/D and is essentially a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN6227/6228's Status Line (also called Busy Line or End of Conversion (E.O.C.)) will rise to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Line to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Line or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

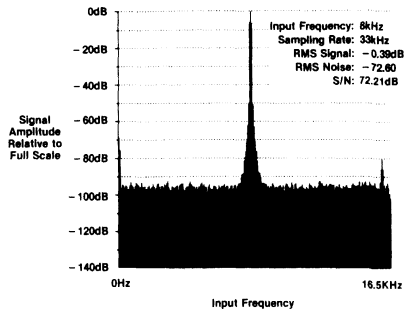
If MN6227/6228 is to be operated with 12-bit or greater microprocessors, all 12 output bits can be 3-state enabled simultaneously permitting data collection with a single read operation. If MN6227/6228 is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's) in a left justified format with 4 trailing "0's".

THE INTERNAL T/H AMPLIFIER

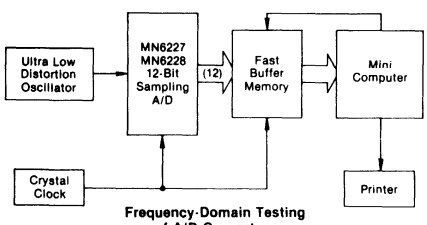
As stated earlier, MN6227/6228's internal T/H amplifier is configured in such a way as to be transparent to the user. The T/H's output is connected directly to the input of the A/D converter, and its operational mode is controlled directly by the Status output of the A/D converter. Consequently, users of MN6227/6228 need not burden themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6227/6228 and are, in fact, impossible to directly test considering that the T/H output and control lines are not accessible at the device pins. The manner in which MN6227/6228 is specified (input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc.) obviates the need for knowing the specific T/H time-domain performance specifications, however, we do supply typical values for critical T/H parameters on the following page.

Note that the static errors (gain error, track-mode offset error, and pedestal) of the T/H function add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D-converter offset error. However, when the A/D offset is functionally laser trimmed, it is done with the whole device sampling at a 33kHz rate and the T/H is in the hold mode whenever trimming is actually performed. Consequently, all error sources are compensated for. All static errors on MN6227/6228 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

Typical T/H Performance Specifications	
Gain Error	± 0.01%
Gain Linearity Error	± 0.005% FSR
Track-Mode Output Offset Error	± 0.5mV
Pedestal	± 1mV
Acquisition Time: 10V step to ± 0.01%	1μsec
20V step to ± 0.01%	2μsec
Track-Hold Transient Settling (to ± 1mV)	250nsec
Slew Rate	± 40V/μsec
Full Power Bandwidth	500kHz
Effective Aperture Delay Time	− 25nsec
Aperture Jitter	0.5nsec
Droop Rate	± 0.1μV/μsec
Hold-Mode Feedthrough Attenuation	− 80 dB



FREQUENCY-DOMAIN TESTING — MN6227/6228 is specified and tested statically in the traditional manner (linearity, accuracy, offset error, current drains, etc.) and dynamically in the frequency-domain. In the dynamic tests, MN6227/6228 is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics −90dB) is used to generate a pure, full-scale, 16kHz sine wave that MN6227/6228 samples and digitizes at a 33kHz rate. These conditions (signal period = 62.5μsec, sampling interval = 30μsec) approach the Nyquist sampling limit (at least 2 samples per signal cycle; sampling frequency greater than 2 times signal frequency). A total of 512 sample-and-convert operations are performed, and the digital-output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are read from the spectrum. A functional block diagram of the test setup appears below, and a sample spectrum appears above.



Frequency-Domain Testing of A/D Converters

The spectrum above is the real portion (imaginary portions of spectrums are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate (16.5kHz in this case). The horizontal axis is divided into 256 frequency bins, each with a width of 64.45Hz. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

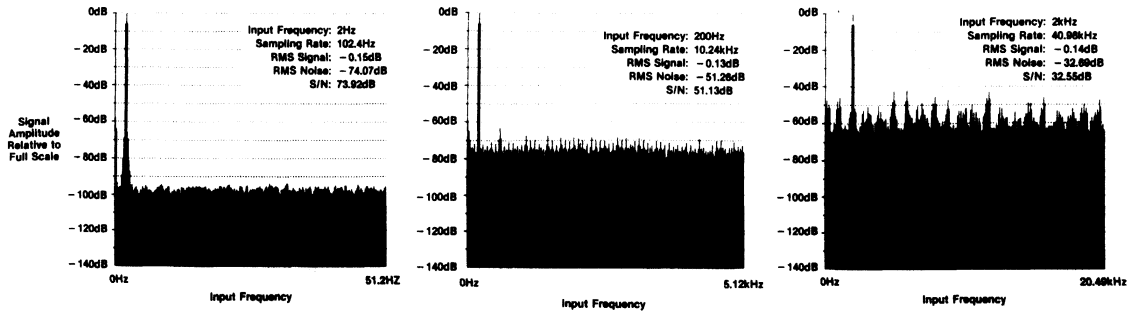
The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). The sample spectrum above is the result of averaging 10 512-point FTT's run on data taken from an MN6227 operating on its bipolar input range (± 5V) with a full-scale input sine wave ($v(t) = 5\sin\omega t$) at a frequency of 8kHz. In the spectrum, the full-scale input signal appears at 8kHz at a level of −0.39dB. Full-scale rms signals do not appear at −3dB levels because the FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the MN6227 combined with that of the signal generator and test fixture. A second harmonic, if it were either present in the input signal or created by the MN6227, would appear at 16kHz. If a third harmonic were present, it would be aliased back into the spectrum and appear at 9kHz. Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level to the strongest harmonic or spurious (nonharmonic) signal in the spectrum. In the sample spectrum above, the strongest harmonic is the second. It appears at a level of −80.29dB, and the signal to harmonics ratio is equal to 79.9dB. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to the rms noise. For the above spectrum, the normalized rms signal level is −0.39dB; the rms noise level is −72.60dB and the SNR is 72.21dB.

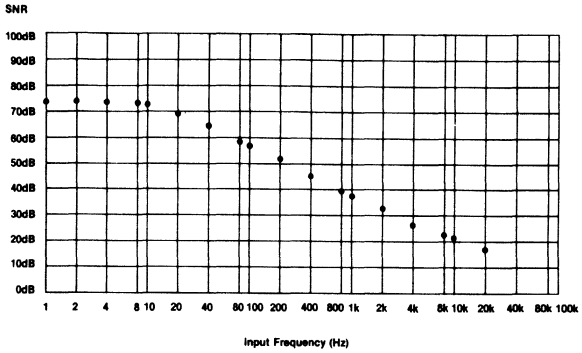
The term "noise" is generally used to describe what remains in the output spectrum after all fundamental, harmonic, d.c., and outstanding spurious components have been removed. It generally appears across all frequency bins at some relatively flat level sometimes referred to as the "noise floor". The rms noise, as described above, represents the broadband noise that would appear superimposed on the sinusoidal input signal if that signal were perfectly recreated from the stored digital-output data. Virtually all the noise in the output spectrum is created either by the act of digitizing or by the A/D converter itself.

In a simple, first-order analysis, the noise in the output spectrum of an A/D converter can be traced to three sources. All three of these noise sources have the potential to manifest themselves as quasi-random relative-accuracy errors in any single A/D conversion of a static signal and subsequently, the potential to manifest themselves as broadband noise in a series of conversions of a dynamically changing signal. Two of these noise sources (quantization noise and converter noise) are effectively constant and do not change with input-signal frequency. The third (aperture noise) usually varies linearly as a function of input-signal frequency, basically doubling whenever input frequency doubles.

Digitizing an analog signal quantizes it or "rounds it off". Digitizing or quantizing an analog signal with a 12-bit A/D effectively "rounds off" the signal to one of 4096 possible discrete levels. This rounding off produces an inherent accuracy error in that the digital output may no longer **exactly** represent the analog input. If one has an ideal A/D converter with all other accuracy-error sources driven to zero, the actual value of rounding-off error or quantization error can be as small as zero or as large as ± ½LSB from conversion to conversion. In a single conversion of a static input signal,

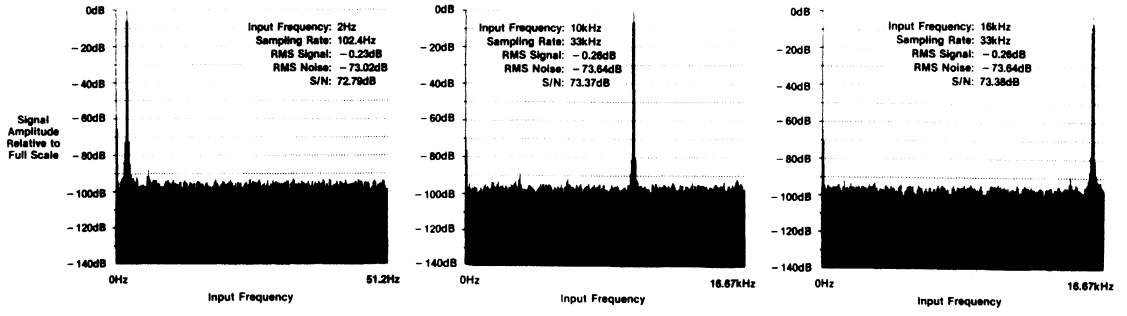
Effective Resolution vs. Input Frequency
MN574A, 25μsec, 12-Bit A/D

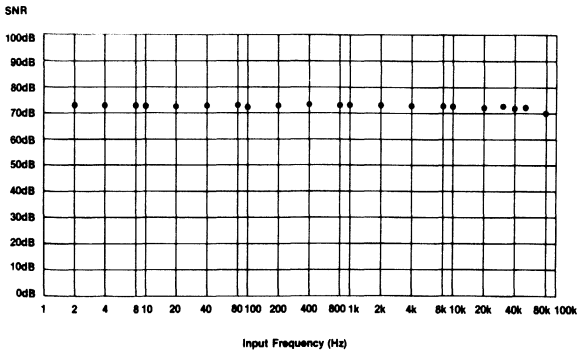




The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN574A type 12-bit A/D converter without a companion T/H amplifier. The input signal frequencies are respectively 2Hz, 200Hz, and 2kHz. The A/D's conversion time is approximately 25μsec; the sampling rates are respectively 102.4Hz, 10.24kHz, and 40.98kHz. The accompanying plot shows the rapid (6dB/octave) degradation of SNR (effective resolution) with increasing input frequency when SA type A/D converters are used to digitize dynamically changing input signals without the aid of a T/H amplifier.

Effective Resolution vs. Input Frequency
MN6227, 33kHz, 12-Bit, Sampling A/D





The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN6227 12-bit sampling A/D. The input signal frequencies are respectively 2Hz, 10kHz, and 16kHz, and the sample/convert rates are respectively 102.4Hz, 33.33kHz, and 33.33kHz. The accompanying plot shows that MN6227's internal T/H amplifier enables the device to maintain near ideal SNR independent of increasing input frequencies. The aperture jitter of the T/H is small enough to maintain SNR for undersampled input frequencies, i.e., for frequencies greater than 16.5kHz.

quantization error is simply an accuracy error. It is impossible for a given conversion of an unknown signal to be more accurate than ± ½LSB. In a series of conversions of a dynamically changing signal, actual instantaneous quantization error varies from sample to sample and manifests itself as broadband noise. In the output spectrum, this noise limits the theoretically achievable signal-to-noise ratio to the following:

$$\text{Ideal SNR} = (6.02n + 1.76)\text{dB}$$

$$n = \text{number of bits}$$

For an ideal 12-bit A/D, the theoretical noise floor in a 512-point FFT occurs around −98dB, and the theoretical SNR is 74dB. For an ideal 11-bit A/D and a 512-point FFT, the numbers are −92dB and 68dB respectively.

The second type of single-conversion accuracy error that manifests itself as broadband noise in the output spectrum results from the actual noise of the A/D converter. This "converter noise" is frequently referred to as "transition noise" and manifests itself, among other ways, by allowing certain fixed, static, input signals to produce either of two adjacent output codes from one conversion to the next. In most A/D converters, the transition from one given digital output code to the next (or vice versa) does not always occur at exactly the same analog input voltage. The "transition voltage" varies from conversion to conversion, and this "transition noise" (the band of adjacent-code uncertainty) is normally on the order of ± 1/10 to ± 1/3 LSB. It is caused by broadband noise and timing jitter in the A/D's constituent components (especially its comparator and reference circuit). In a single given A/D conversion, transition noise adds (or subtracts) to the device's static differential linearity error. Again, this phenomenon will manifest itself as an accuracy error in any single conversion and as noise in any series of conversions of a changing input signal.

This second noise component should be thought of simply as the "converter noise". Recall that quantization noise is a result of the digitizing process, and it limits SNR to some theoretical value. Its effect is independent of the type or kind of A/D converter used. Converter noise is a function of how "noisy" a selected A/D converter may be, and it reduces actual measured SNR's to a level something below ideal. Hence MN6227/6228 guarantees 70dB and not 74dB initial room-temperature SNR.

The third component of A/D converter noise derives from the fact that SA type A/D converters (without companion T/H amplifiers) cannot accurately convert dynamically changing input signals. Because of the nature of the technique of successive approximations, it is imperative that A/D's using this technique maintain a stable input signal during their conversion (aperture) time. Slew rates in excess of (± ½LSB) / (conversion time) can cause accuracy errors in any individual conversion. In a series of conversions of a sinusoidal signal, the slew rate varies from sample to sample, and the consequent aperture (slew-rate) errors manifest themselves as broadband noise.

This third component of A/D noise is effectively eliminated by MN6227/6228's internal T/H. The T/H's ability to instantaneously freeze the slewing input signal (limited only by the T/H's aperture jitter) and hold it constant results in the A/D seeing a series of d.c. signals and not the sinusoid itself. MN6227/6228's ability to maintain SNR over its full input bandwidth (up to the "Nyquist frequency" or ½ the sampling rate) is the result of the T/H's ability to limit the overall noise to the quantization noise plus the noise inherent in the A/D.

The plots on the previous page demonstrate that an A/D without a companion T/H is effectively incapable of accurately converting analog input signals above some critical frequency (slew rate) and that the A/D's SNR or "effective resolution" deteriorates at approximately 6dB/octave above that frequency. Basically, the A/D's quantization and converter noise remain constant while its aperture noise doubles each time the input frequency doubles.

MN6227/6228's internal T/H effectively eliminates aperture noise allowing the A/D to maintain "low-frequency SNR" as the actual input frequency increases.

APPLICATIONS INFORMATION

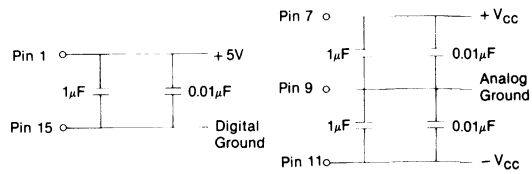
LAYOUT CONSIDERATIONS AND GROUNDING—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN6227/6228. It is critically important that the device's power supplies be filtered, well-regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power-supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (Digital Ground) and the $+V_{CC}$ and $-V_{CC}$ pins should be decoupled directly to pin 9 (Analog Ground). Suitable decoupling capacitors are 1μF tantalum type in parallel with a 0.1μF ceramic discs.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN6227/6228 and associated analog-input circuitry as far as possible from logic circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to MN6227/6228 as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to MN6227/6228. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a nonpolarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for MN6227/6228's internal reference. It should be connected as close as possible to the analog input signal reference point.

POWER SUPPLY DECOUPLING



CONTROL FUNCTIONS—Operating MN6227/6228 under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN6227/6228 control-line functions. Table 2 is the control-line Truth Table.

Table 1: MN6227/6228 Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0→1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1→0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1→0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0→1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

Unless Chip Enable (CE, Pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, Pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$, and A_0) will have no effect on MN6227/6228 operation. When CE and $\overline{CS}$ are both asserted; the signal applied to R/$\overline{C}$ (Read/Convert, Pin 5) determines whether a data read (R/$\overline{C}$ = "1") or a convert operation (R/$\overline{C}$ = "0") is initiated.

Table 2: MN6227/6228 Truth Table

CONTROL INPUTS					MN6227/6228 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (2.4V minimum).
2. "0" indicates TTL logic zero (0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicate logic transitions (edges).
5. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4LSB's	

When initiating a conversion, the signal applied to A_0 (Byte Address/Short Cycle, Pin 4) determines whether a 12-bit conversion is initiated (A_0 = "0") or an 8-bit conversion is initiated (A_0 = "1"). It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0" and A_0 = "1" or "0" that initiates a convert operation, and the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$ as shown in the Truth Table and as described below in the section labeled Timing-Initiating Conversions. When initiating conversions, the 12/$\overline{8}$ line is a "don't care".

When reading digital output data from MN6227/6228, CE and $\overline{CS}$ must be asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine the format of output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is a "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line goes from a "0" to a "1".

If the 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit bytes as described below in the section labeled Timing-Reading Output Data. In this situation, A_0 = "0" will result in the 8 MSB's being accessed and A_0 = "1" will result in the 4 LSB's and 4 trailing zeros being accessed. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 though 27. When A_0 goes high, the upper 8 data bits are disabled, the 4 LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23.

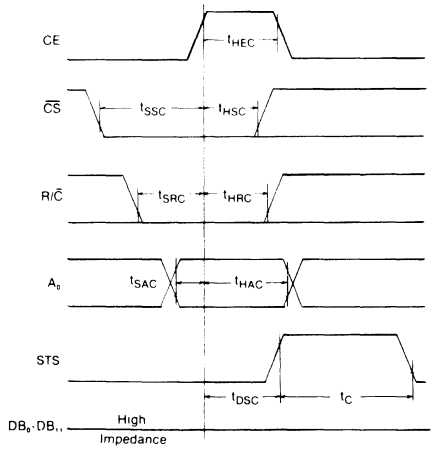
TIMING—INITIATING CONVERSIONS—It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0" and A_0 = "1" (initiate 8-bit conversion) or A_0 = "0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$. The A_0 line should be stable immediately prior to whichever of the above transitions is used to initiate a conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation, and it is not recommended to use this line to initiate conversion in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a read operation were occuring, and the result could be system bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.

Timing for a typical application is shown below. In this application $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE becoming a "1". This sequence can be accomplished in a number of ways including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent) and generating a CE 0→1 transition using the system clock. In this example $\overline{CS}$ should be a "0" 50nsec prior to the CE transition (t_{SSC} = 50nsec min). R/$\overline{C}$ should be a "0" 50nsec prior to the CE transition (t_{SRC} = 50nsec min), and A_0 should be stable 0nsec prior to the CE transition (t_{SAC} = 0nsec min). The minimum pulse width for CE = "1" is 50nsec (t_{HEC} = 50nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50nsec while CE = "1" (t_{HSC} and t_{HRC} = 50nsec min) to effectively initiate the conversion. A_0 must be valid for at least 50nsec (t_{HAC} = 50nsec min) while CE is high to effectively initiate the conversion. The Status Line rises to a "1" no more than 200nsec after the rising edge of CE. (t_{DSC} = 200nsec max). Once the Status = "1", additional convert commands will be ignored until the conversion is complete.

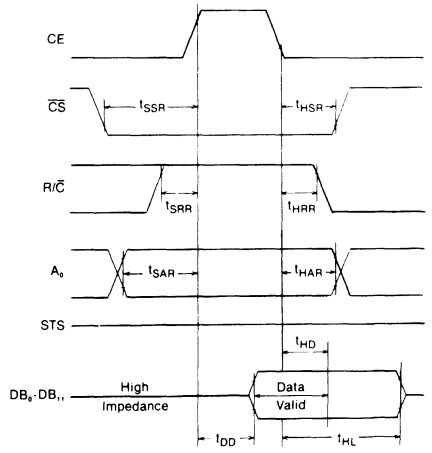
TIMING—RETRIEVING DATA—The combination of CE = "1", $\overline{CS}$ = "0", and R/$\overline{C}$ = "1" is required to access digital output data. If the above combination of control signals is met and the 12/$\overline{8}$ line has a "1" applied, all twelve output bits will become valid simultaneously. If the 12/$\overline{8}$ line has a "0" applied, output data is formatted for an 8-bit data bus, and the 8 MSB's will become valid when the above condition is met with A_0 = "0" while the 8 LSB's (4 data bits and 4 trailing "0's") will become valid whenever A_0 = "1". Data access can be initiated by either the rising edge of CE or the falling edge of $\overline{CS}$.

Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50nsec prior to CE (t_{SSR} = 50nsec min, t_{SAR} = 50nsec min). R/$\overline{C}$ can become valid the same time as CE (t_{SRR} = 0nsec min). In the 8-bit bus interface mode (12/$\overline{8}$ = "0"), A_0 must be stable at least 50nsec prior to CE going high. A_0 may be toggled at anytime without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point where CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low).



Convert Start Timing



Read Cycle Timing

MN6227/6228 TIMING SPECIFICATIONS:

CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0	0		ns
t_{HAC}	A_0 Valid During CE High	50	20		ns
t_C	Conversion Time				
	8-Bit Cycle	15	13	17	μs
	12-Bit Cycle	10	20	25	μs

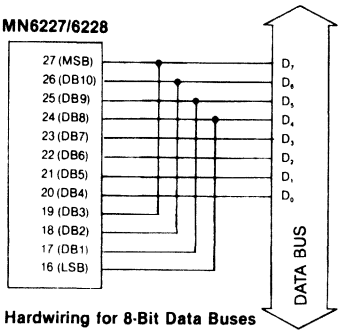
MN6227/6228 TIMING SPECIFICATIONS:

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0	0		ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0	0		ns
t_{HAR}	A_0 Valid After CE Low	50	25		ns

HARDWIRING TO 8-BIT DATA BUSES—For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN6227/6228 output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte ($A_0 = 0$)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte ($A_0 = 1$)	DB3	DB2	DB1	DB0	0	0	0	0



Hardwiring for 8-Bit Data Buses

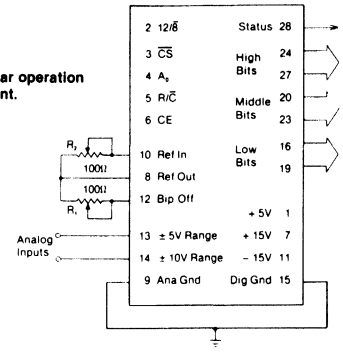
UNIPOLAR OPERATION AND CALIBRATION—Analog input connections and calibration circuits for the unipolar operating mode is shown below. When the 0 to + 10V input range is used, apply the analog input to pin 13 of the MN6227. If gain adjustment is not used, replace trim pot R_2 with a fixed 50Ω ± 1% metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, this transition will occur within ± 2 LSB's of its actual ideal value (+ ½ LSB). For the 10V range, 1 LSB = 2.44mV. To offset adjust, apply an analog input equal to + ½ LSB and with the MN6227 continuously converting, adjust the offset potentiometer "down" until the digital output is all "0's" and then adjust "up" until the LSB just changes from a "0" to a "1". The offset adjust circuit has a range of approximately ± 15mV, and different offsets can be set for different system requirements.

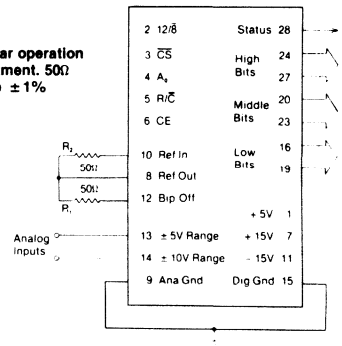
Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal full scale of the selected input range. This voltage is + 9.9963V for the 10V unipolar input range. Gain trimming is accomplished by applying this voltage and adjusting the gain potentiometer "up" until the digital outputs are all "1's" and then adjusting down until the LSB just changes from a "1" to a "0".

If a 10.24V (2.5mV/bit) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor, and a 200Ω trim pot inserted in series with the analog input to pin 13. Offset trimming proceeds the same. Gain trimming is now accomplished with the new pots.

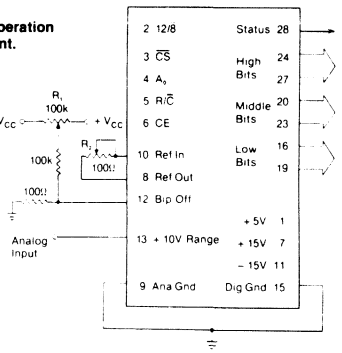
MN6227/6228 bipolar operation with trim adjustment.



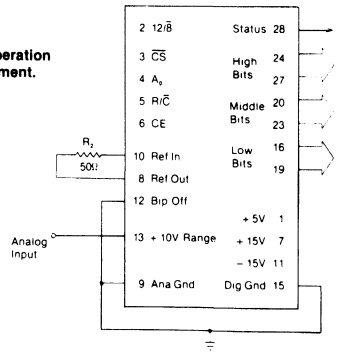
MN6227/6228 bipolar operation without trim adjustment. 50Ω resistors should be ±1% metal film.



MN6227 unipolar operation with trim adjustment.



MN6227 unipolar operation without trim adjustment.



BIPOLAR OPERATION AND CALIBRATION—Analog input connections and calibration circuits for the bipolar operating modes are shown on the previous page. If the ± 5V input range is to be used on MN6227, apply the analog input to pin 13. If the ± 10V range is to be used on MN6228, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustment are not to be used, the trim pots R_1 and R_2 can be replaced with fixed 50Ω ± 1% metal-film resistors to meet all published specifications.

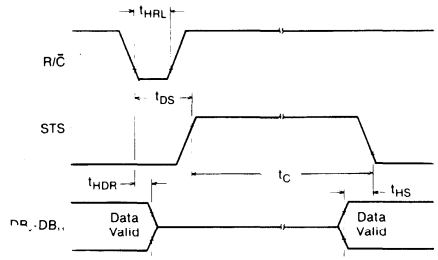
Bipolar zero error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition is supposed to occur ½ LSB below zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the minus full scale point. The procedure is to apply an analog input equal to − FS + ½ LSB (− 4.9988V for the ± 5V range, − 9.9976V for the ± 10V range) and adjust the bipolar offset trim pot "down" until the digital output is all "0's". Then adjust "up" until the LSB just changes from "0" to a "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal positive full scale value of the selected input range. This voltage is + 4.9963V and + 9.9927V respectively for the ± 5V and ± 10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "up" until the digital outputs are all "1's" and then adjusting "down" until the LSB just changes from a "1" to a "0".

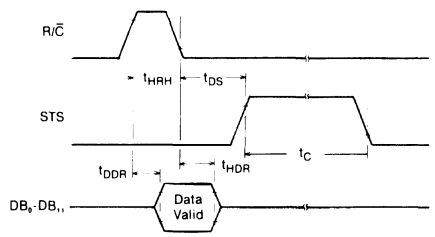
STAND-ALONE OPERATION

The MN6227/6228 can be used in a "stand-alone" mode in systems having dedicated input ports and not requiring full bus interface capability. In this mode, CE and 12/$\overline{8}$ are tied to logic "1", $\overline{CS}$ and A_0 are tied to logic "0", and the conversion is controlled by R/$\overline{C}$. A conversion is initiated when R/$\overline{C}$ is brought low, and all 12 bits of the three-state output buffers are enabled when R/$\overline{C}$ is brought high. This gives rise to two possible modes of operation; conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. The timing diagram below details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The Status line goes high 200ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

The timing diagram below details operation with a positive start pulse, Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next rising edge of R/$\overline{C}$.



Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion



High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)			DIGITAL OUTPUT
0 to + 10V	± 5V	± 10V	MSB LSB
+ 10.0000	+ 5.0000	+ 10.0000	1111 1111 1111
+ 9.9963	+ 4.9963	+ 9.9927	1111 1111 111Ø*
+ 5.0012	+ 0.0012	+ 0.0024	1000 0000 000Ø*
+ 4.9988	− 0.0012	− 0.0024	ØØØØ ØØØØ ØØØØ*
+ 4.9963	− 0.0037	− 0.0073	0111 1111 111Ø*
+ 0.0012	− 4.9988	− 9.9976	0000 0000 000Ø*
0.0000	− 5.0000	− 10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input range, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to + 10V or ± 5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For ± 10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN6228 operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of − 9.9976 volts. Subsequently, any input voltage more negative than − 9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of − 0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at + 9.9927 volts. An input more positive than + 9.9927 volts will give all "1's".

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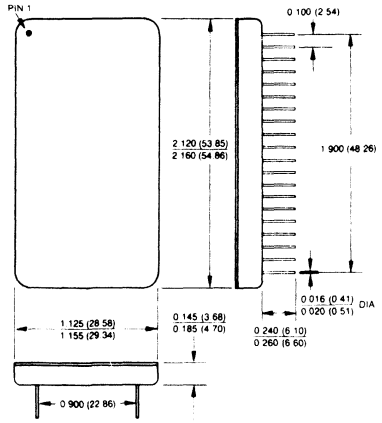
MN6249

2MHz, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- **2MHz Sampling Rate With Internal T/H Amplifier**
- **12MHz Input Bandwidth**
- **FFT Testing**
- **Minimum 68dB Signal-to-Noise Ratio to Nyquist**
- **Typical −78dB Harmonics Over Full Bandwidth**
- **Small 40-Pin DIP**
- **No Missing Codes Guaranteed Over Temperature**
- **TTL Compatible Digital Inputs and Outputs**
- **3-State Output Buffer**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

40 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN6249 is a 2MHz, 12-bit sampling A/D converter which offers outstanding dynamic as well as static performance. This sampling A/D contains an internal T/H amplifier and a 12-bit, subranging A/D converter in a single, 40-pin, triple-wide DIP package. The internal T/H amplifier allows the A/D converter to digitize 1MHz full-scale input signals at rates up to 2MHz. Each device is fully FFT (Fast Fourier Transform) tested using contemporary DSP technology and guarantees up to 68dB minimum signal-to-noise ratio (SNR, rms-to-rms) and up to −78dB harmonics and spurious noise.

MN6249 is configured such that the internal T/H amplifier is completely transparent. The T/H's operational mode is internally controlled by the A/D timing logic. Users need only supply start convert commands at the desired sampling rate. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's. This type of configuration and specification/testing eliminates the need for potentially confusing and often misleading T/H specifications like aperture delay, aperture jitter, charge injection, etc., and also eliminates frustrating attempts to translate data-converter time-domain specifications into frequency-domain performance.

MN6249 is an excellent choice for digitizing analog signals in systems that require both high-resolution and high-speed in as small a package as possible. Typical applications include spectrum, vibration, waveform and transient analysizers; radar, sonar and video digitizers; medical imaging equipment; digital filters; and multiplexed or simultaneous-sampling data-acquisition systems.

MN6249 is manufactured in Micro Networks MIL-STD-1772 qualified facility, and for military/aerospace and harsh environment industrial applications, the MN6249 H/B is available with Environmental Stress Screening while the MN6249 H/B CH is 100% screened to MIL-H-38534.

Contact factory for availability of CH devices.

February 1990

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN6249 2MHz 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN6249J, K	0°C to +70°C (case)
MN6249S, T	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 19)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 25)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 5, 29, 40)	−0.5 to +7 Volts
−5.2V Supply (−Vee, Pin 14)	0 to −7 Volts
Digital Inputs (Pins 7, 12)	−0.5 to +5.5 Volts
Analog Inputs:	
10V Range (Pin 16)	−7 to +7 Volts
5V Range (Pin 17)	−3.5 to +3.5 Volts
Reference Output Current	10mA

ORDERING INFORMATION

PART NUMBER — MN6249X/B

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" suffix to "S" or "T" models for Environment Stress Screening.

Add "CH" suffix to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V, −Vee = −5.2V unless otherwise indicated)

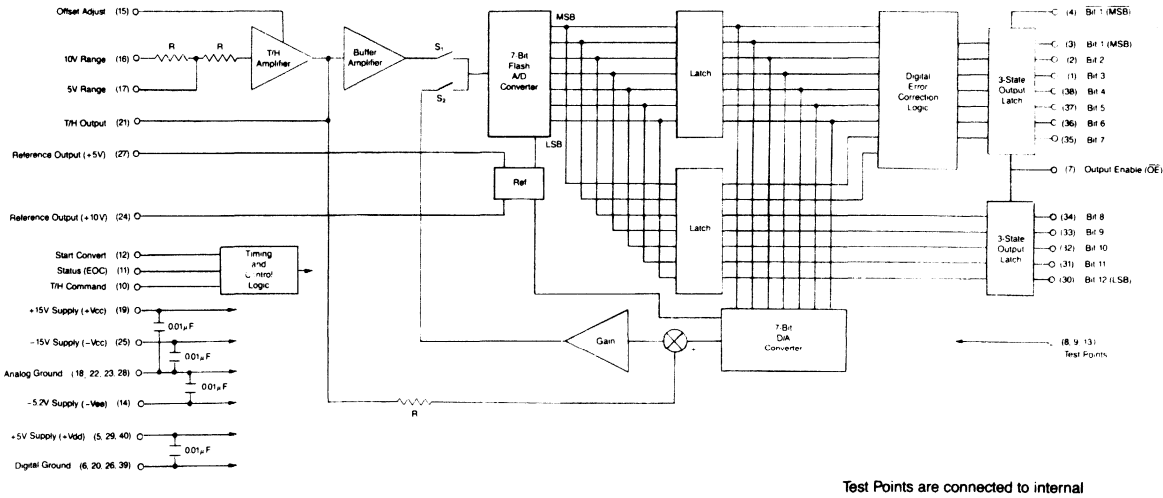
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V Range		±2.5		Volts
10V Range		±5.0		Volts
Input Impedance (Note 1): Resistance: 5V Range		500		Ω
10V Range		1000		Ω
Capacitance		10		pF
Offset Adjustment Range: 5V Range		±50		mV
10V Range		±100		mV
DIGITAL INPUTS (Start Convert, $\overline{OE}$)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.7V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−0.4	mA
DIGITAL OUTPUTS (Parallel, Status, T/H Control, $\overline{MSB}$)				
Output Coding		COB		
		CTC		
Logic Levels: Logic "1" ($I_{source} \leq 100\mu A$)	+2.7			Volts
Logic "0" ($I_{sink} \leq 2mA$)			+0.5	Volts
Leakage Current (B1 - B12 in High-Z State): Logic "1" (V_{OH} = +2.7V)			+10	μA
Logic "0" (V_{OL} = +0.4V)			−10	μA
INTERNAL REFERENCE				
Reference Output (Pin 24): Voltage		+10		Volts
Drift (Note 1)		±10		ppm/°C
Output Current (Notes 1, 2)		2		mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc Supply	±14.5	±15.0	±15.5	Volts
+Vdd Supply	+4.75	+5.0	+5.25	Volts
−Vee Supply	−5.0	−5.2	−5.4	Volts
Power Supply Rejection (Note 3): +Vcc Supply	−50	−65		dB
−Vcc Supply	−50	−70		dB
+Vdd Supply	−35	−50		dB
−Vee Supply	−60	−80		dB
Current Drains: +Vcc Supply		65	75	mA
−Vcc Supply		80	95	mA
+Vdd Supply		210	240	mA
−Vee Supply		50	60	mA
Power Consumption		3485		mW

DYNAMIC CHARACTERISTICS	J	K	S	T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	2	2	2	2	MHz
Maximum A/D Conversion Time (Note 5)	400	400	400	400	nsec
Signal-to-Noise Ratio (SNR, Note 6): Initial (+25°C)	66	68	66	68	dB
T_{min} to T_{max} (Note 11)	64	66	64	66	dB
Harmonics and Spurious Noise (Note 7): Initial (+25°C)	−70	−72	−70	−72	dB
T_{min} to T_{max} (Note 11)	−67	−70	−67	−70	dB
Small Signal Bandwidth	12	12	12	12	MHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C)	1	1	1	1	LSB
T_{min} to T_{max} (Note 11)	1.5	1	1.5	1	LSB
Resolution for No Missing Codes: Initial @ +25°C	12	12	12	12	Bits
T_{min} to T_{max} (Note 11)	12	12	12	12	Bits
Bipolar Zero Error (Notes 8, 9): Initial (+25°C)	0.3	0.2	0.3	0.2	%FSR
T_{min} to T_{max}	0.5	0.4	0.5	0.4	%FSR
Full-Scale Accuracy Error (Notes 8, 10): Initial (+25°C)	0.25	0.20	0.25	0.20	%FSR
T_{min} to T_{max} (Note 11)	0.40	0.30	0.40	0.30	%FSR

SPECIFICATION NOTES:

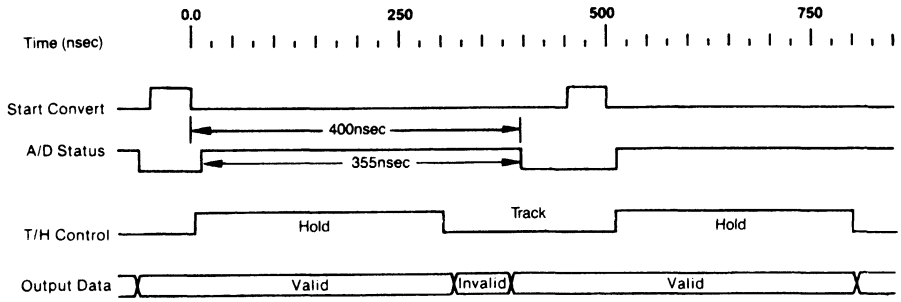
1. This parameter is listed for reference only and is not tested.
2. If the internal reference is used to drive an external load, the load must not change during a conversion.
3. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or the 0000 0000 0000 to 0000 0000 0001 output transition occurs versus a change in power supply voltage.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 2MHz rate. Obviously, the devices may be operated at lower sampling frequencies if desired.
5. When Status is high, the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input (0dB) sine wave at any frequency up to 941.41 KHz and is specified as a minimum.
7. This parameter represents the highest signal-to-non-fundamental component ratio (harmonic or spurious, in-band or out-of-band) in the output spectrum and is specified as a minimum.
8. Adjustable to zero with an external potentiometer.
9. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000. The ideal value at which this transition should occur is $-\frac{1}{2}$LSB.
10. Full-scale accuracy specifications apply at both positive and negative full-scale and are defined as the differences between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0001 to 0000 0000 0000 for positive full-scale and from 1111 1111 1110 to 1111 1111 1111 for negative full-scale. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full-scale voltage. The latter ideally occurs ½LSB above the nominal negative full-scale voltage.
11. MN6249J and MN6249K are specified for 0°C to +70°C operation. MN6249S, S/B and MN6249T, T/B are fully specified for −55°C to +125°C operation.

BLOCK DIAGRAM



Test Points are connected to internal circuitry and should not be connected to externally.

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Minimum start convert pulse width is 50nsec. The rising edge of start convert resets internal timing circuits ensuring that T/H Control (pin 10) is set to a logic "0" and that the first conversion made upon "powerup" is valid. The falling edge of Start Convert initiates the conversion, and Start Convert must remain low for 350nsec minimum.
2. Status rises to a "1" typically 45nsec after the falling edge of Start Convert.
3. Conversion time is defined as the time from the falling edge of Start Convert to the falling edge of Status and is specified as 400nsec maximum.
4. Digital output data from the previous conversion remains valid typically 280nsec after the falling edge of Start and 235nsec after the rising edge of Status.
5. Digital output data is valid on the falling edge of Status.
6. Output data is enabled and becomes valid a maximum of 50nsec after Output Enable ($\overline{OE}$, pin 7) is brought low.
7. The falling edge of T/H Control occurs 300nsec maximum after the falling edge of Start Convert.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN6249 is a 12-bit, sampling, A/D converter consisting of a high-speed A/D converter and its companion T/H amplifier. The A/D section is a multistage (two-step) A/D converter. It employs the Micro Networks Serial-Parallel conversion technique (sometimes referred to as the subranging technique) with digital error correction. The technique uses two 7-bit flash A/D converters (actually a single 7-bit flash converter is used twice) in a configuration that yields a resolution (12 bits) that is beyond the practical limits of what can be achieved in a single high-resolution flash converter. For a detailed discussion of the Serial-Parallel conversion technique and digital error correction, please refer to the MN5245/5246 data sheet.

The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec (100nsec maximum if continuously converting at maximum conversion rate) and must remain low during the conversion for a minimum of 350nsec. The rising edge of Start Convert resets the timing logic ensuring that all timing pulses are set to the proper state and that the first conversion following "power on" produces valid digital output data. The falling edge of Start Convert initiates the conversion setting T/H Control Output and Status (E.O.C.) to logic "1's". The T/H Control Output signal remains a logic "1" for 300nsec maximum after the falling edge of Start Convert and returns to a logic "0" when the "analog-processing" portion of the conversion is complete. Status remains a logic "1" for 400nsec maximum after the falling edge of Start Convert. Status returning low signifies that the conversion process is complete and that parallel output data is valid.

The internal T/H amplifier enables the MN6249 to sample and digitize analog input signals while maintaining SNR (rms-signal-to-rms-noise) and harmonic distortion performance specifications. The T/H amplifier's mode of operation is controlled by the internal control logic circuitry. When a conversion is initiated by the falling edge of Start Convert, the T/H amplifier is switched from the track mode to the hold mode, indicated by the T/H Control Output changing from a logic "0" to a logic "1". The internal T/H amplifier remains in the hold mode during the "analog processing" portion of the conversion cycle. Once the analog processing is complete, and the analog input signal no longer needs to be held at a constant value, the T/H is switched to track mode to acquire and track the next analog input signal to be converted (T/H Control Output changes from a logic "1" to a logic "0"). This allows the T/H amplifier's acquisition time to overlay the "digital processing" portion of the conversion cycle.

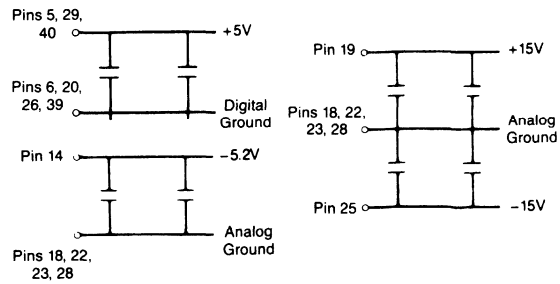
Valid parallel output data is available on the falling edge of Status and remains valid during the next conversion for 280nsec (typ) after the next falling edge of Start Convert. See Timing Diagram. This allows the use of rising and falling edges of either Start Convert or Status for latching output data.

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracy and performance from the MN6249. Analog Ground (pins 18, 22, 23, 28) is not connected internally to Digital Ground (pins 6, 20, 26, 39). All ground pins should be tied together as close to the unit as possible and connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

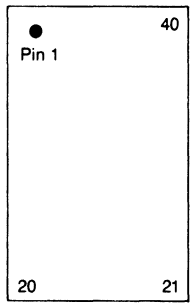
Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

A 0.1μF capacitor should be connected from Gain Adjust (pin 27) to system analog ground.



POWER SUPPLY DECOUPLING

N DESIGNATIONS



1	Bit 3	40	+5V Supply (+Vdd)
2	Bit 2	39	Digital Ground
3	Bit 1 (MSB)	38	Bit 4
4	$\overline{\text{Bit 1 (MSB)}}$	37	Bit 5
5	+5V Supply (+Vdd)	36	Bit 6
6	Digital Ground	35	Bit 7
7	Output Enable ($\overline{\text{OE}}$)	34	Bit 8
8	T.P.	33	Bit 9
9	T.P.	32	Bit 10
10	T/H Control Output	31	Bit 11
11	Status (EOC)	30	Bit 12 (LSB)
12	Start Convert	29	+5V Supply (+Vdd)
13	T.P.	28	Analog Ground
14	−5.2V Supply (−Vee)	27	Gain Adjust
15	Offset Adjust	26	Digital Ground
16	10V Range	25	−15V Supply (−Vcc)
17	5V Range	24	Reference Output (+10V)
18	Analog Ground	23	Analog Ground
19	+15V Supply (+Vcc)	22	Analog Ground
20	Digital Ground	21	T/H Output

ıs: "Test Points" (T.P.) are connected to internal circuitry and should not be connected to externally.

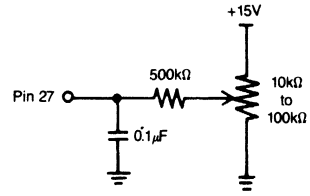
'ERNAL T/H AMPLIFIER — As stated earlier, MN6249's inter- T/H amplifier is configured in such a way as to be transparent ıe user. The T/H's output is connected directly to the input of the) converter, and its operational mode is controlled directly by the ırnal control logic circuitry. Consequently, users of the MN6249 ıd not burden themselves with oftentimes confusing T/H ıcifications like acquisition time, aperture-delay time, aperture r, droop rate, etc.. These parameters are not specified for 6249 and are, in fact, impossible to directly test considering that T/H output and control lines are not accessible at the device pins. ı manner in which MN6249 is specified (input bandwidth, sampl- rate, signal-to-noise ratio, harmonic distortion, etc.) obviates the ıd for knowing the specific T/H time-domain performance cifications.

e that the static errors (gain error, track-mode offset error, and estal) of the T/H function will add directly to the corresponding ırs of the A/D converter but that both are effectively nulled with functional laser trimming of the A/D. T/H offset error and estal, for example, add directly to A/D-converter offset error. ıever, when the A/D offset is functionally laser trimmed, it is done ıe 2MHz sampling rate with the T/H is in the hold mode. Consen- ntly, all error sources are compensated for. All static errors on 5249 (accuracy error, unipolar offset error, bipolar zero error, etc.) tested and specified as full input-output transfer specifications include both the T/H and A/D.

TUS OUTPUT/DATA VALID—The Status or End of Conversion).C., pin 11) is set to a logic "1" by the falling edge of Start Con- remains high during the conversion; and is set to a logic "0" n the conversion is complete. Digital output data is valid on the ıg edge of Status and remains valid 280nsec after Start Con- goes low initiating the next conversion. When making suc- ıive conversions, any of the edges occurring during the begin- of the data-valid period (fall of Status, falling edge of the next t Convert, rising edge of Status, etc.) are best suited for this pur- ɜ. Also, output data can be enabled during this data-valid period ringing Output Enable ($\overline{\text{OE}}$, pin 7) low. The delay from the fall- ɜdge of $\overline{\text{OE}}$ to output data enabled is 50nsec maximum.

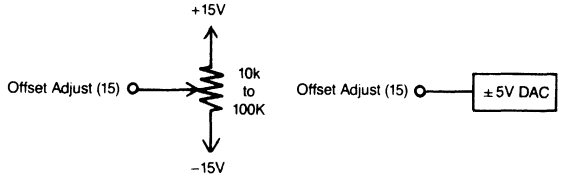
N ADJUST — Pin 27 on MN6249 serves a unique function. The ce's internal +5V ±2% reference is brought out at this point can be used to drive external loads. If used for this purpose, 27 should be buffered with a FET-input device as drawing more than 5μA from the internal reference will affect MN6249 accuracy and linearity. Pin 27 can also be used as a Reference In point if it is necessary to operate MN6249 from an external reference. An application requiring an external reference might be one in which it is necessary to have a number of devices operate from the same reference in order to track each other in changing temperatures. The applied reference should be +5V ±250mV.

Pin 27 also functions as the gain-adjust point for MN6249. Gain adjustment is accomplished using a 10kΩ to 100kΩ trimming potentiometer and a 500kΩ series resistor as shown below. The series resistor can be ±20% carbon composition or better. The multiturn potentiometer should have a TCR of 100ppm/°C or less to minimize drift with temperature. Gain adjusting is normally accomplished by applying the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition is ideally supposed to take place and adjusting the pot until the transition is observed.



Gain Adjust Range= ±0.2% FSR

OFFSET ADJUST — Initial offset error of the MN6249 can be adjusted to zero by applying a voltage to Offset Adjust (pin 15). A 50μΩ resistor is connected from Offset Adjust (pin 15) to the internal T/H amplifier's summing junction. This allows the output of a voltage-output DAC or the wiper of a potentiometer to be connected directly to Offset Adjust (pin 15).



ORDERING INFORMATION

Part Number	Specified Temperature Range	No Missing Codes Over Temp.	Integral Linearity Over Temp.	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics
MN6249J	0°C to +70°C	12 Bits	±1.5LSB	2MHz	1MHz	66dB	−70dB
MN6249K	0°C to +70°C	12 Bits	±1LSB	2MHz	1MHz	68dB	−72dB
MN6249S	−55°C to +125°C	12 Bits	±1.5LSB	2MHz	1MHz	66dB	−70dB
MN6249S/B[1]	−55°C to +125°C	12 Bits	±1.5LSB	2MHz	1MHz	66dB	−70dB
MN6249S/B CH[2]	−55°C to +125°C	12 Bits	±1.5LSB	2MHz	1MHz	68dB	−70dB
MN6249T	−55°C to +125°C	12 Bits	±1LSB	2MHz	1MHz	68dB	−72dB
MN6249T/B[1]	−55°C to +125°C	12 Bits	±1LSB	2MHz	1MHz	68dB	−72dB
MN6249T/B CH[2]	−55°C to +125°C	12 Bits	±1LSB	2MHz	1MHz	68dB	−72dB

1. Includes Environmental Stress Screening.
2. Fully compliant to MIL-H-38534.

DIGITAL OUTPUT CODING

Analog Input		Digital Output
±5V	±2.5V	MSB LSB
−5.0000	−2.5000	1111 1111 1111
−4.9988	−2.4994	1111 1111 111Ø*
−0.0036	−0.0018	1000 0000 000Ø*
−0.0012	−0.0006	ØØØØ ØØØØ ØØØØ*
+0.0012	+0.0006	0111 1111 111Ø*
+4.9964	+2.4982	0000 0000 000Ø*
+5.0000	+2.5000	0000 0000 0000

NOTES:

1. For a 12-bit converter with a 5 Volt FSR, 1LSB=1.22mV. For a 12-bit converter with a 10 Volt FSR, 1LSB=2.44mV.
2. Coding is complementary offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

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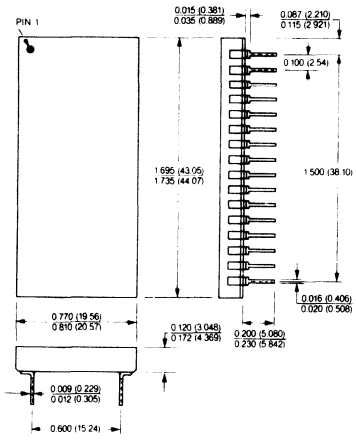
MN6290
MN6291

LOW-DISTORTION
SAMPLING, 16-Bit
A/D CONVERTERS

FEATURES

- **20kHz Sampling Rate With Internal T/H Amplifier**
- **10kHz Full-Power Input Bandwidth**
- **84dB Signal-to-Noise Ratio Over Full Bandwidth**
- **−88dB Harmonics Over Full Bandwidth**
- **FFT Testing**
- **Serial and Parallel Outputs**
- **1.5 Watts Max Power**
- **Standard 32-Pin DIP**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

32 PIN DIP

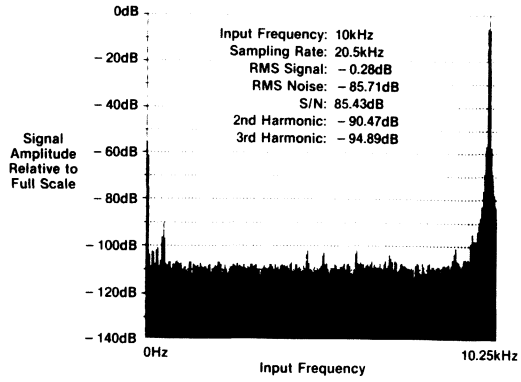


Dimensions in Inches
(millimeters)

DESCRIPTION

The MN6290 Series of Low-Distortion, 16-Bit, Sampling, A/D Converters offers an outstanding combination of resolving power, conversion speed, low noise, and low harmonic distortion. These SA type A/D's are packaged in small, 32-pin, double-wide DIP's and have internal track-hold (T/H) amplifiers that enable them to accurately sample and digitize 10kHz full-scale input signals at rates up to 20kHz. Each device is fully FFT (Fast Fourier Transform) tested using contemporary DSP technology and guarantees up to 84dB signal-to-noise ratio (SNR, rms-to-rms) and up to −88dB harmonics and spurious noise.

MN6290 (10V input span) and MN6291 (20V input span) are configured in a manner that makes their internal T/H completely user transparent. A high-impedance (5MΩ) input buffer isolates the T/H from its signal source, and the T/H's operational mode is internally controlled by the A/D's status line. Users need only supply start-convert pulses at the desired sampling rate. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's. This type of configuration and testing eliminates the need for potentially confusing and misleading T/H specifications like aperture delay, aperture jitter, charge injection, etc., and also eliminates historically frustrating attempts to translate data-converter time-domain specifications into frequency-domain performance.



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MN6290, MN6291 SAMPLING 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6290J, K; MN6291J, K	0°C to +70°C
MN6290S, S/B, T, T/B	−55°C to +125°C
MN6291S, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 27)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 23)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 29)	0 to +7 Volts
Digital Inputs (Pins 30, 32)	0 to +5.5 Volts
Analog Inputs (Pins 7, 8)	±15 Volts
Analog Ground (Pins 9, 26) to Digital Ground (Pin 31)	±1 Volt
Ref Out (Pin 8) Short Circuit Duration	Continuous to Ground

ORDERING INFORMATION

PART NUMBER ——— **MN6290T/B CH**

Select MN6290 or MN6291

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, $\pm V_{cc}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: MN6290		0 to +10, ±5		Volts
MN6291		±10		Volts
Input Impedance (Note 17): Resistance		5		Mohm
Capacitance		50		pF
Input Bias Current Over Full Temperature Range			±600	nA
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−0.8	mA
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 2): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 320\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 3.2mA$)			+0.4	Volts
INTERNAL REFERENCE				
Reference Output (Pin 24): Voltage	+9.9	+10	+10.1	Volts
Drift (Note 17)		±15		ppm/°C
Output Current (Notes 3, 17)			1	mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: $\pm V_{CC}$ Supply	±14.5	±15	±15.5	Volts
$+V_{dd}$ Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection (Note 14): $+V_{CC}$		±0.003	±0.02	%FSR/% Supply
$-V_{CC}$		±0.003	±0.02	%FSR/% Supply
$+V_{dd}$		±0.001	±0.01	%FSR/% Supply
Current Drains: $+V_{CC}$ Supply		+33	+48	mA
$-V_{CC}$ Supply		−34	−40	mA
$+V_{dd}$ Supply		+28	+35	mA
Power Consumption		1150	1500	mW

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated)

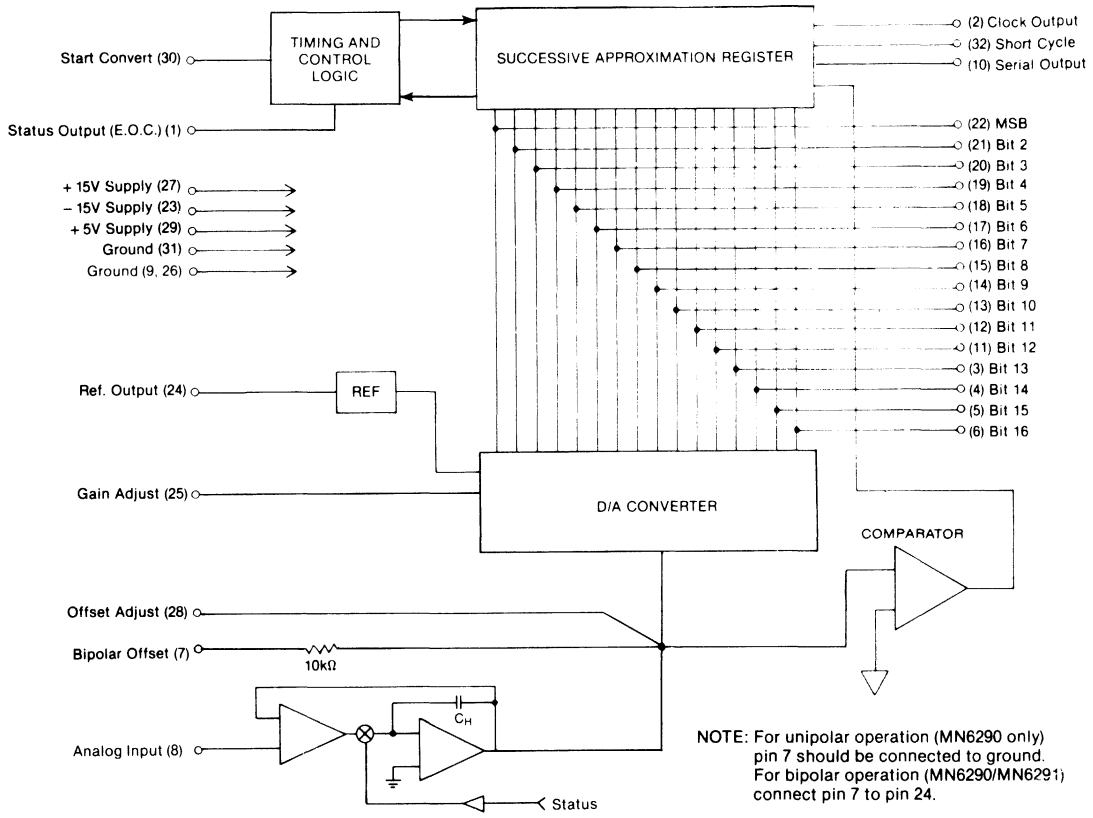
DYNAMIC CHARACTERISTICS	MN6290J MN6291J	MN6290K MN6291K	MN6290S MN6291S	MN6290T MN6291T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	20	20	20	20	kHz
Maximum A/D Conversion Time (Note 5)	40	40	40	40	μsec
Signal-to-Noise Ratio (SNR, Note 6):					
Initial (+25°C) (Minimum)	80	84	80	84	dB
T_{min} to T_{max} (Minimum, Note 7)	78	82	78	82	dB
Harmonics and Spurious Noise (Note 8):					
Initial (+25°C) (Minimum)	−85	−88	−85	−88	dB
T_{min} to T_{max} (Minimum, Note 7)	−82	−85	−82	−85	dB
Input Signal Full-Scale Bandwidth (Minimum, Note 9)	10	10	10	10	kHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C) (Max. Note 16)	±0.006	±0.003	±0.006	±0.003	%FSR
T_{min} to T_{max} (Maximum, Note 7)	±0.012	±0.006	±0.012	±0.006	%FSR
Resolution for Which No Missing					
Codes is Guaranteed: Initial (+25°C)	13	14	13	14	Bits
T_{min} to T_{max} (Note 7)	13	14	13	14	Bits
Unipolar Offset Error (Notes 10, 11):					
Initial (+25°C) (Maximum)	±0.05	±0.05	±0.05	±0.05	%FSR
Drift (Maximum)	±15	±7.5	±15	±7.5	ppm of FSR/°C
Max Error T_{min} to T_{max} (Note 15)	±0.12	±0.084	±0.2	±0.125	%FSR
Bipolar Zero Error (Notes 10, 12):					
Initial (+25°C) (Maximum)	±0.075	±0.05	±0.075	±0.05	%FSR
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
Max Error T_{min} to T_{max} (Note 15)	±0.15	±0.1	±0.225	±0.15	%FSR
Full Scale Accuracy Error (Notes 10, 13):					
Initial (+25°C) (Maximum)	±0.2	±0.1	±0.2	±0.1	%FSR
Max Error T_{min} to T_{max} (Note 15)	±0.35	±0.2	±0.5	±0.3	%FSR
Drift (Maximum)	±30	±20	±30	±20	ppm of FSR/°C

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. See table of transition voltages in section labeled Digital Output Coding.
3. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 7 connected to pin 24), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 20kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at rates of 25kHz or higher.
5. Whenever the Status Output (pin 1) is low ("logic "0"), the internal T/H is in the track mode, and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0db) at any frequency up to 10kHz.
7. MN6290J, K and MN6291J, K are fully specified for 0°C to +70°C operation. MN6290S, S/B, T, T/B and MN6291S, S/B, T, T/B are fully specified for −55°C to +125°C operation.
8. This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
9. This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 20kHz rate.
10. Adjustable to zero with external potentiometer.
11. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6290 on its unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
12. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6290/6291 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
13. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
15. Listed maximum error-over- temperature specifications for unipolar offset, bipolar zero and full-scale accuracy correspond to the combination of maximum room-temperature errors and worst-case drift conditions to describe the worst-case error that might be encountered over the entire specified temperature range.
16. ±0.006%FSR is equivalent to ±½LSB for 13 bits and is equal to ±0.6mV for a device with a 10V full scale range (0 to +10V or ±5V input range). ±0.003%FSR is equivalent to ±½LSB for 14 bits and is equal to ±0.3mV for a device with a 10V full scale range.
17. These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

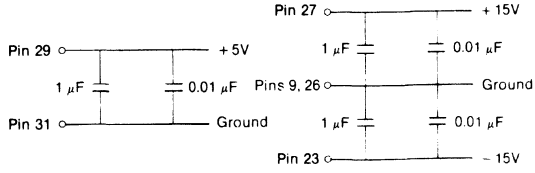
LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN6290/6291. The units' three ground pins (pins 9, 26, and 31) are not connected to each other internally. They must be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between analog ground pins (pins 9 and 26) and digital ground (pin 31) as close to the unit as possible. Wide conductor runs should be employed.

Coupling between analog inputs and digital signals should be minimized to avoid nosie pick-up. Bipolar Offset (pin 7), Analog Input (pin 8), Offset Adjust (pin 28) and Gain Adjust (pin 25) are particularly noise susceptable. Care should be taken to avoid long runs or runs close to digital lines when utiiizing these inputs. Input signal lines should be a short as possible. In bipolar operation, where Bipolar Offset (pin 7) is connected to Reference Output (pin 24), a short jumper should be used. For external offset adjustment, the series resistor(s) should be located as close to Offset Adjust (pin 28) as possible. A 0.01μF capacitor should be connected between Gain Adjust (pin 25) and Analog Ground as close to the package as possible. An 0.01μF capacitor should be connected from Reference Output (pin 24) to Analog Ground.

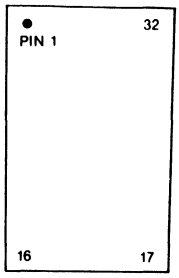
Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN6290/6291. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

If short-cycling is not used the Short-Cycling pin (pin 32) must be connected to +5V (pin 29).

POWER SUPPLY DECOUPLING



PIN DESIGNATIONS



1	Status (E.O.C.)	32	Short Cycle
2	Clock Output	31	Digital Ground
3	Bit 13	30	Start Convert
4	Bit 14	29	+5V Supply ($+V_{dd}$)
5	Bit 15	28	Offset Adjust
6	Bit 16 (LSB)	27	+15V Supply ($+V_{cc}$)
7	Bipolar Offset	26	Analog Ground
8	Analog Input	25	Gain Adjust
9	Analog Ground	24	Reference Output (+10V)
10	Serial Output	23	−15V Supply ($-V_{cc}$)
11	Bit 12	22	Bit 1 (MSB)
12	Bit 11	21	Bit 2
13	Bit 10	20	Bit 3
14	Bit 9	19	Bit 4
15	Bit 8	18	Bit 5
16	Bit 7	17	Bit 6

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—MN6290 and MN6291 are 16-bit, sampling, A/D converters. Each contains a 16-bit successive-approximation type A/D and a companion track-hold (T/H) amplifier. The T/H's enable MN6290 and MN6291 to accurately and repetitively sample and digitize dynamically changing input signals in both traditional data-acquisition and contemporary DSP-type applications.

Successive approximation (SA) type A/D converters, when operated without the aid of T/H amplifiers, are severely limited in their ability to accurately convert changing analog input signals. The traditional rule of thumb for guaging such performance is that the A/D's are incapable of accurately converting signals that are slewing faster than (± ½LSB)/(conversion time). For a 14-bit A/D with an input range of ± 10V and a conversion time of 40μsec, this corresponds to an input slew-rate limit of ± 7.6μV/μsec. If one wishes to express the slew-rate limit as a bandwidth for a full-scale input sinusoid, it corresponds to 0.24Hz.

The proliferating use of A/D converters in DSP applications has resulted in significantly greater demands on A/D's to be able to convert dynamic signals, particularly sinusoids. More and more frequently, T/H amplifiers are used with A/D's to enable them to accomplish this task.

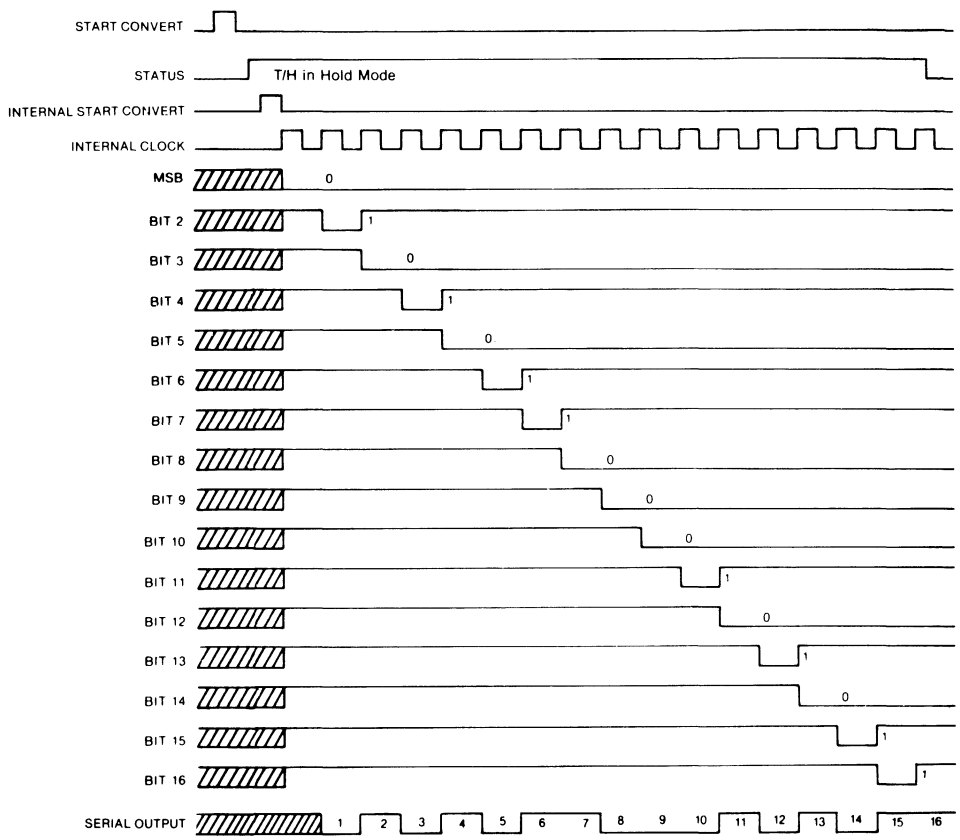
MN6290/6291 are extremely user friendly. They have been configured in a manner that virtually eliminates all of the problems encountered when mating T/H's and successive approximation A/D's and driving the pair from real-world signal sources. The T/H is truly transparent. A high-impedance (5Mohm) input buffer isolates it from the external signal source, and its output is internally connected directly to the input of the A/D converter. The output current, impedance and transient-response characteristics of the T/H have been optimized for driving the 16-bit SA A/D. More importantly, the critical dynamic characteristics of the T/H (aperture delay, aperture jitter, small and large signal bandwidths, droop rate, etc.) have been similarly optimized. Most importantly, the critical inter-device timing relationships (T/H mode control, transient decay time, etc.) are internally controlled by MN6290/6291's timing and control circuitry. All that users need to provide externally is the start convert pulse.

The falling edge of the start convert pulse activates MN6290/6291's internal timing circuitry. Immediately, the T/H (which has been in the track or signal-acquisition mode up until this time) is driven into the hold mode instantaneously "freezing" the value of the analog input signal. Simultaneously, MN6290/6291's status output (also called "End of Conversion" or E.O.C.) is set to a logic "1" indicating that the T/H is now in hold; that an A/D conversion is now in progress; and that the parallel output data (from the previous conversion) is no longer valid. MN6290/6291's internal timing logic now provides approximately 1 μsec of delay to permit the track-to-hold switching transient at the output of the T/H to decay. Subsequently, the internal clock is started, and the 16-bit A/D conversion of the held signal proceeds.

The value of the hold capacitor used in MN6290/6291's internal T/H has been selected so that T/H output droop, even over temperature, is not significant (greater than ± ½LSB) during the A/D's conversion time. Similarly, the offset and pedestal voltages, as well as the gain error, of the T/H do not contribute to the overall accuracy of the sampling A/D because they are effectively nulled out during our active laser trimming of the A/D converter.

At the completion of the A/D conversion, MN6290/6291's internal control logic turns off the internal clock; drops the status output back to a logic "0"; and commands the T/H back into the track mode to acquire a new input signal. Status going low signifies that the conversion is complete and that the parallel output data is valid. A 20nsec delay has been added between the finalization of the LSB and the falling edge of status. This ensures that all output bits are valid when status falls and permits the use of this trailing edge to clock data into output latches. Output data remains valid until the falling edge of the next start convert pulse.

TIMING DIAGRAM



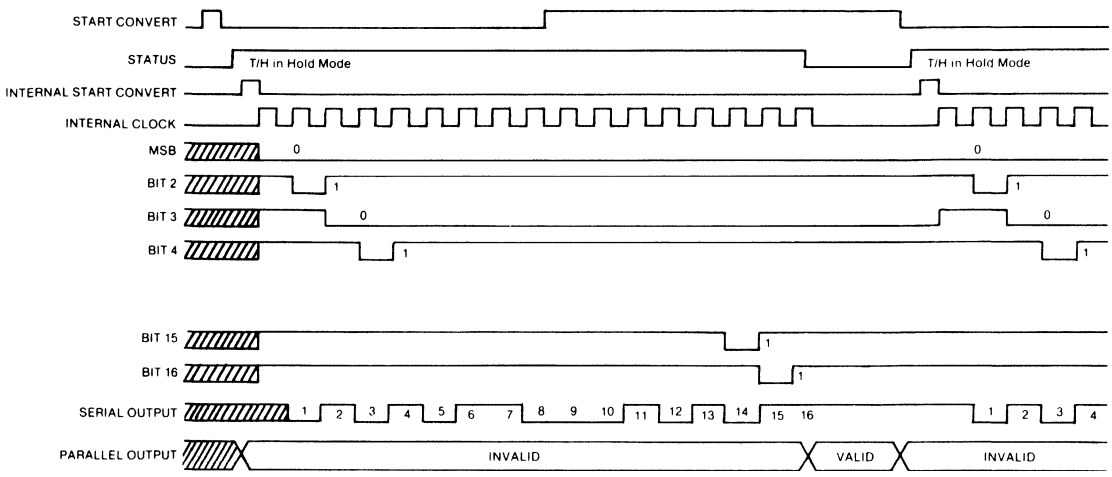
SPECIFICATIONS (T_A = +25°C, supply voltages ±15V and +5V unless otherwise specified)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits) (Note 6)		35	40	μsec
Internal Clock Frequency (Notes 4, 8)	404	462		kHz
Start Convert Pulse Width (Notes 2, 7)	40			nsec
Delay Falling Edge of Start to (Note 8): Status = "1" Clock Output = "1"		30 400		nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20	100		nsec
Delay LSB Valid to Falling Edge of Status (Notes 3, 8)	20	40		nsec

TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command can be either a positive or negative pulse at least 40nsec wide. Conversions are initiated on the falling edge of the Start Convert command.
3. Data will be valid 20nsec prior to the falling edge of Status (E.O.C.).
4. The internal clock is enabled and the conversion commences following an internal delay which allows for T/H switching and settling.
5. When the converter is initially "powered up" it may come on at any point in the conversion cycle.
6. Conversion time is defined as the width of the Status (E.O.C.) pulse.
7. The minimum time between falling edges of the Start Convert command is 50μsec.
8. These parameters are listed for reference only and are not tested.

APPLICATIONS INFORMATION



TIMING DIAGRAM — The above timing diagram illustrates the relationships of the external and internal timing pulses discussed in the following sections. Additionally, the above diagram shows the beginning of a second conversion and of particular interest, the relationship of Start Convert, Status (E.O.C.), Serial Output and Parallel Output from one conversion to another.

START CONVERT — The falling edge of the start convert signal initiates the sampling/digitizing cycle. Either positive, negative or symetrical pulses can be used to initiate conversions provided that the start convert signal has a minimum positive pulse width of 40nsec. To achieve guaranteed performance, the maximum repetition rate of the start convert signal is 20kHz. Obviously, MN6290/6291 may be operated at lower sampling rates if desired. If necessary, the start convert signal may be set to a logic "1" after the conversion has begun, however, the next falling edge should not occur until the ongoing conversion is complete and a minimum of 10μsec has been allowed for the internal T/H amplifier to acquire and track the next analog input voltage to be sampled and digitized. See diagram above.

STATUS OUTPUT — The Status Output (End of Conversion (E.O.C.), pin 1) will be set to a logic "1" 30nsec (typical) after the falling edge of Start Convert; will remain a logic "1" during the conversion; and will be set to a logic "0" when the conversion is complete. The falling edge of status occurs a minimum of 20nsec after the LSB output bit is set to its final value (delay from LSB bit valid to falling edge of Status is 20nsec min). Therefore, the Status Output may be used to latch valid digital output data. If the latches selected require more than 20nsec of set-up time, simple gate delays can be used to delay the falling edge of Status. See diagram above.

SHORT CYCLE — For applications requiring fewer than 16 bits of resolution, MN6290/6291 can be truncated or short cycled to the desired number of bits with a proportionate decrease in the A/D conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle input (pin 32). For example, to truncate at 14 bits, connect Bit 15 (pin 5) to the Short Cycle input (pin 32); converting will stop and the Status Output (End of Conversion (E.O.C.), pin 1) will be set to a logic "0" a minimum of 20nsec after bit 14 has been set.

PARALLEL OUTPUTS — During the succesive approximation process the weight of each bit is compared to the value of the analog input voltage. The converter is reset to MSB-0111 1111 1111 1111-LSB by the rising edge of the first clock pulse. Subsequent rising clock edges set the bit previously tested to its final state and brings the next bit to be tested to a logic "0". This process continues until all bits have been tested and the Status Output returns to a logic "0". Valid parallel output data can only be latched at the end of the sample/conversion cycle.

The LSB bit is valid 20nsec prior to the falling edge of Status Output (E.O.C.), therefore, this edge may be used to latch parallel output data. While the converter is idling (Status Output is "0"), the parallel output data from the most recent conversion remains valid until the start of the next conversion cycle.

SERIAL OUTPUT — Serial output data is provided only during the conversion process and is in a NRZ (non-return to zero) format. The data is coded the same as parallel output data and is synchronous with the internal clock. Each serial output bit is valid 20nsec after the rising clock edge (serial output data lags parallel output by one clock cycle, see timing diagram) and can be strobed into a shift register by rising edges of the internal clock.

DIGITAL OUTPUT CODING

ANALOG INPUT			DIGITAL OUTPUT
0 to + 10V	± 5V	± 10V	MSB LSB
+ F.S.	+ F.S.		1111 1111 1111 1111
+ F.S. − 3/2 LSB	+ F.S. − 3/2 LSB		1111 1111 1111 111Ø*
+ 1/2 F.S. + 1/2 LSB	+ 1/2 LSB		1000 0000 0000 000Ø*
+ 1/2 F.S. − 1/2 LSB	− 1/2 LSB		ØØØØ ØØØØ ØØØØ ØØØØ*
+ 1/2 F.S. − 3/2 LSB	− 3/2 LSB		0111 1111 1111 111Ø*
+ 1/2 LSB	− F.S. + 1/2 LSB		0000 0000 0000 000Ø*
0	− F.S.		0000 0000 0000 0000

CODING NOTES:

1. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV. 1LSB for 14 Bits = 610.4μV.
2. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV. 1LSB for 14 Bits = 1.22mV.
3. For unipolar ranges, the coding is straight binary.
4. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN6290/MN6291 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the ± 10V range, the transition from output code 1111 1111 1111 1111 to output code 1111 1111 1111 1110 (or vice versa) will ideally occur at an input of + 9.999542V (+ F.S. − 3/2LSB). Subsequently, any voltage greater than + 9.999542V will give a digital output of all "1's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of − 0.000153 volts. The 0000 0000 0000 0000 to 0000 0000 0000 0001 transition will occur at − 9.999847V. An input more negative than this level will give all "0's."

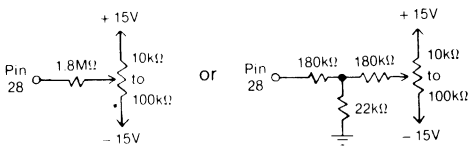
INPUT RANGE SELECTION

Part Number	Range	Connect Pin 7 to Pin
6290	0 to + 10V	Ground
6290	± 5V	24
6291	± 10V	24

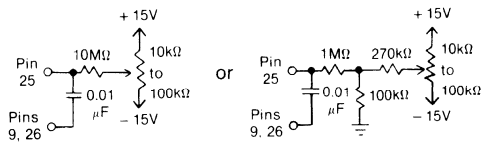
OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS — Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 28 should be left open. A 0.01μf capacitor should be tied from Gain Adjust (pin 25) to Analog Ground (pins 9,26).

ZERO ADJUSTMENT — Connect the zero adjust potentiometer as shown below. For unipolar ranges (MN6290 only), apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off.

For bipolar ranges (MN6290 and MN6291), apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "flickering."



GAIN ADJUSTMENT — Connect the gain potentiometer as shown below and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off. A 0.01μf capacitor should be connected from Gain Adjust (pin 25) to Analog Ground (pins 9, 26).



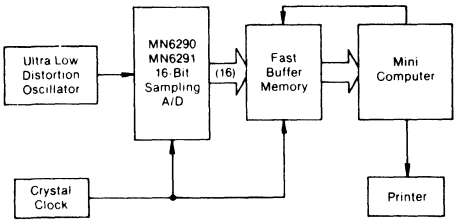
THE INTERNAL T/H AMPLIFIER

As stated in the Description of Operation, MN6290/6291's internal T/H amplifier is transparent to the user. The T/H's output is connected directly to the A/D's input and its operational mode is controlled by the Timing and Control Logic (see Block Diagram). The user is not required to supply additional support timing circuits sometimes necessary when mating an A/D with its companion T/H. Additionally, MN6290/6291 users need not concern themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6290/6291 and are, in fact, impossible to directly test because the T/H's output and control line are not accessable at the device pins. Frequency-domain specifications like input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc. obviates the need for knowing the specific T/H time-domain specifications, however, the table on the following page does supply typical values for those critical T/H performance specifications.

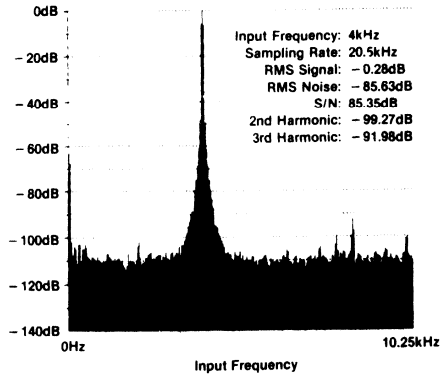
Note that the static errors (gain error, track-mode offset error, and pedestal) of the T/H function add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D-converter offset error. However, when the A/D offset is functionally laser trimmed, it is done with the whole device sampling at a 20kHz rate and the T/H is in the hold mode whenever trimming is actually performed. Consequently, all error sources are compensated for. All static errors on MN6290/6291 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

Typical T/H Performance Specifications	
Gain Error Gain Linearity Error	± 0.01% ± 0.001%FSR
Track Mode Output Offset Error Pedestal	± 0.5mV ± 0.5mV
Acquisition Time: 10V step to ± 0.003% 20V step to ± 0.003%	5μsec 6μsec
Track-Hold Transient Settling (to ± 1mV)	250nsec
Slew Rate Full Power Bandwidth	± 4V/μsec 50kHz
Effective Aperture Delay Time Aperture Jitter	– 25nsec 0.5nsec
Droop Rate Hold-Mode Feedthrough Attenuation	± 0.05μV/μsec – 86dB

FREQUENCY-DOMAIN TESTING — MN6290/6291 is specified and tested statically in the traditional manner (linearity, accuracy, offset error, current drains, etc.) and dynamically in the frequency domain. In the dynamic tests, MN6290/6291 is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics – 100dB) is used to generate a pure, full-scale, 10kHz sine wave that MN6290/6291 samples and digitizes at a 20.5kHz rate. These conditions (signal period = 100μsec, sampling interval = 48.8μsec) approach the Nyquist sampling limit (at least 2 samples per signal cycle; sampling frequency greater than 2 times signal frequency). A total of 512 sample-and-convert operations are performed, and the digital output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are read from the spectrum. A functional block diagram of the test setup appears below, and a sample spectrum appears above.



Frequency-Domain Testing of A/D Converters

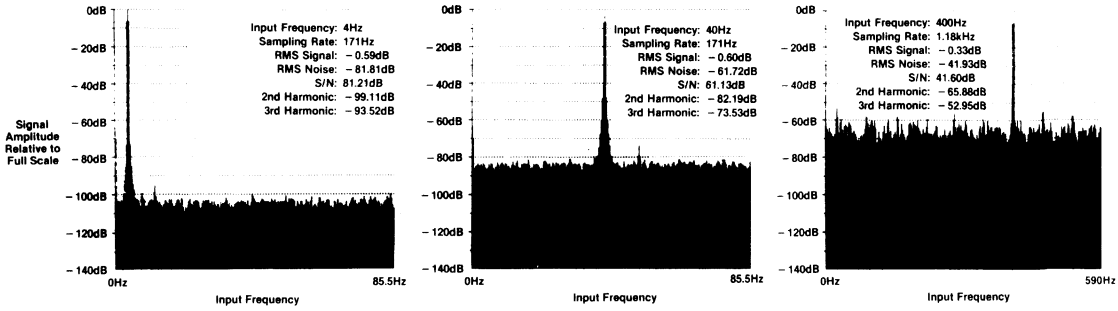


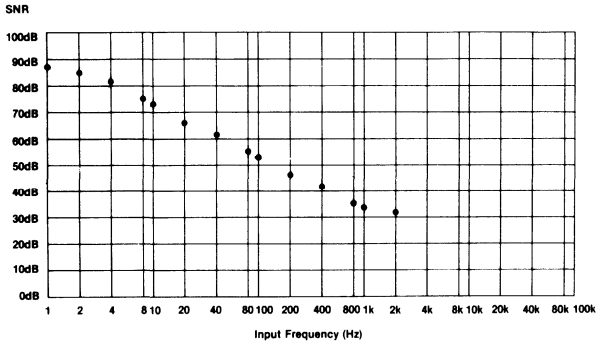
The spectrum above is the real portion (imaginary portions of spectra are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate (10.25kHz in this case). The horizontal axis is divided into 256 frequency bins, each with a width of 40.04Hz. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). The sample spectrum above is the result of averaging 10 512-point FFT's run on data taken from an MN6290 operating on its bipolar input range (± 5V) with a full-scale input sine wave ($v(t) = 5\sin\omega t$) at a frequency of 4kHz. In the spectrum, the full-scale input signal appears at 4kHz at a level of – 0.28dB. Full-scale rms signals do not appear at – 3dB levels because our FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the MN6290 combined with that of the signal generator and test fixture. A second harmonic, if it were either present in the input signal or created by the MN6290, would appear at 8kHz. If a third harmonic were present, it would be aliased back into the spectrum and appear at 8.5kHz. Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level to the strongest harmonic or spurious (nonharmonic) signal in the spectrum. In the sample spectrum above, the strongest harmonic is the third. It appears at a level of – 92.26dB, and the signal to harmonics ratio is equal to 91.98dB. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to the rms noise. For the above spectrum, the normalized rms signal level is – 0.28dB; the rms noise level is – 85.63dB; and the SNR is 85.35dB.

The term "noise" is generally used to describe what remains in the output spectrum after all fundamental, harmonic, d.c., and outstanding spurious components have been removed. It generally appears across all frequency bins at some relatively flat level sometimes referred to as the "noise floor". The rms noise, as described above, represents the broadband noise that would appear superimposed on the sinusoidal input signal if that signal were perfectly recreated from the stored digital output data. Virtually all the noise in the output spectrum is created either by the act of digitizing or by the A/D converter itself.

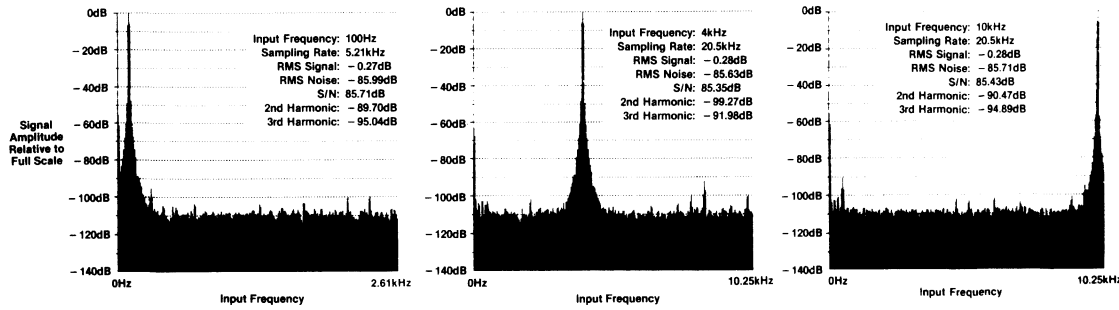
Effective Resolution v.s. Input Frequency
MN5290, 40μsec, 16-Bit A/D

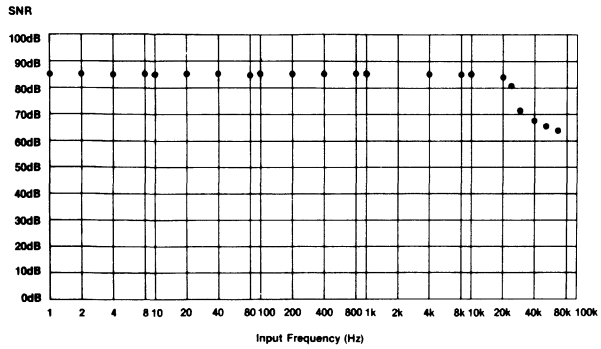




The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN5290 type 16-bit A/D converter without a companion T/H amplifier. The input signal frequencies are respectively 4Hz, 40Hz, and 400Hz. The A/D's conversion time is approximately 40μsec, and the sampling rates are respectively 171Hz, 171Hz, and 1.18kHz. The accompanying plot shows the rapid (6dB/octave) degradation of SNR (effective resolution) with increasing input frequency when SA type A/D converters are used to digitize dynamically changing input signals without the aid of a T/H amplifier.

Effective Resolution v.s. Input Frequency
MN6290, 20kHz, 16-Bit, Sampling A/D





The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN6290 16-bit sampling A/D. The input signal frequencies are respectively 100Hz, 4kHz, and 10kHz, and the sample/convert rates are respectively 5.21kHz, 20.5kHz, and 20.5kHz. The accompanying plot shows that MN6290's internal T/H amplifier enables the device to maintain near ideal SNR independent of increasing input frequencies. The aperture jitter of the T/H is small enough to maintain SNR for undersampled input frequencies, i.e., for frequencies greater than 10kHz.

In a simple, first- order analysis, the noise in the output spectrum of an A/D converter can be traced to three sources. All three of these noise sources have the potential to manifest themselves as quasi-random relative-accuracy errors in any single A/D conversion of a static signal and subsequently, the potential to manifest themselves as broadband noise in a series of conversions of a dynamically changing signal. Two of these noise sources (quantization noise and converter noise) are effectively constant and do not change with input-signal frequency. The third (aperture noise) usually varies linearly as a function of input-signal frequency, basically doubling whenever input frequency doubles.

Digitizing an analog signal quantizes it or "rounds it off". Digitizing or quantizing an analog signal with a 16-bit A/D effectively "rounds off" the signal to one of 65,536 possible discrete levels. This rounding off produces an inherent accuracy error in that the digital output no longer **exactly** represents the analog input. If one has an ideal A/D converter with all other accuracy-error sources driven to zero, the actual value of rounding-off error or quantization error can be as small as zero or as large as ± ½LSB from conversion to conversion. In a single conversion of a static input signal, quantization error is simply an accuracy error. It is impossible for a given conversion of an unknown signal to be more accurate than ± ½LSB. In a series of conversions of a dynamically changing signal, actual instantaneous quantization error varies from sample to sample and manifests itself as broadband noise. In the output spectrum, this noise limits the theoretically achievable signal-to-noise ratio to the following:

$$\text{Ideal SNR} = (6.02n + 1.76)\text{dB}$$

n = number of bits

For an ideal 16-bit A/D, the theoretical noise floor in a 512-point FFT occurs around − 122dB, and the theoretical SNR is 98dB. For an ideal 14-bit A/D and a 512-point FFT, the numbers are − 110dB and 86dB respectively.

The second type of single-conversion accuracy error that manifests itself as broadband noise in the output spectrum results from the actual noise of the A/D converter. This "converter noise" is frequently referred to as "transition noise" and manifests itself, among other ways, by allowing certain fixed, static, input signals to produce either of two adjacent output codes from one conversion to the next. In most A/D converters, the transition from one given digital output code to the next (or vice versa) does not always occur at exactly the same analog input voltage. The "transition voltage" varies from conversion to conversion, and this "transition noise" (the band of adjacent-code uncertainty) is normally on the order of ± 1/10 to ± 1/3 LSB. It is caused by broadband noise and timing jitter in the A/D's constituent components (especially its comparator and reference circuit). In a single given A/D conversion, transition noise adds (or subtracts) to the device's static differential linearity error. Again, this phenomenon will manifest itself as an accuracy error in any single conversion and as noise in any series of conversions of a changing input signal.

This second noise component should be thought of simply as the "converter noise". Recall that quantization noise is a result of the digitizing process, and it limits SNR to some theoretical value. Its effect is independent of the type or kind of A/D converter used. Converter noise is a function of how "noisy" a selected A/D converter may be, and it reduces actual measured SNR's to a level something below ideal. Hence MN6290/6291 K and T models guarantee 84dB and not 86dB initial room-temperature SNR.

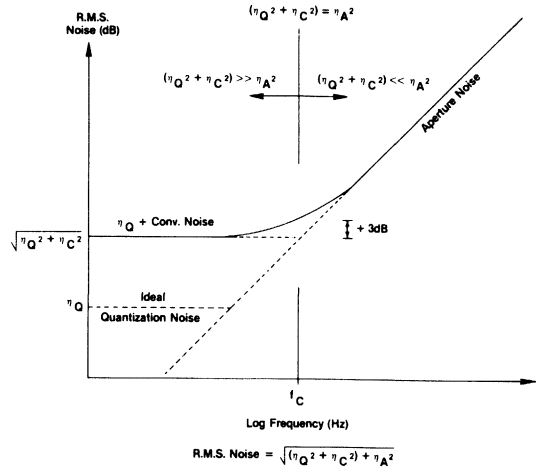
The third component of A/D converter noise derives from the fact that SA type A/D converters (without companion T/H amplifiers) cannot accurately convert dynamically changing input signals. Because of the nature of the technique of successive approximations, it is imperative that A/D's using this technique maintain a stable input signal during their conversion (aperture) time. Slew rates in excess of (± ½LSB) / (conversion time) can cause accuracy errors in any individual conversion. In a series of conversions of a sinusoidal signal, the slew rate varies from sample to sample, and the consequent aperture (slew-rate) errors manifest themselves as broadband noise.

This third component of A/D noise is effectively eliminated by MN6290/6291's internal T/H. The T/H's ability to instantaneously freeze the slewing input signal (limited only by the T/H's aperture jitter) and hold it constant results in the A/D seeing a series of d.c. signals and not the sinusoid itself. MN6290/6291's ability to maintain SNR over its full input bandwidth (up to the "Nyquist frequency" or ½ the sampling rate) is the result of the T/H's ability to limit the overall noise to the quantization noise plus the noise inherent in the A/D.

The plots on the previous page demonstrate that an A/D without a companion T/H is effectively incapable of accurately converting analog input signals above some critical frequency (slew rate) and that the A/D's SNR or "effective resolution" deteriorates at approximately 6dB/octave above that frequency. Basically, the A/D's quantization and converter noise remain constant while its aperture noise doubles each time the input frequency doubles.

MN6290/6291's internal T/H effectively eliminates aperture noise allowing the A/D to maintain "low-frequency SNR" as the actual input frequency increases.

The plot below graphically illustrates the principles we have been discussing and focuses on A/D converter noise, not on SNR. Earlier, we discussed quantization noise (η_Q), converter noise (η_C) and slew rate or aperture noise (η_A) and how each individually contributes to broadband noise in an A/D's output spectrum. The plot below illustrates the relationship of the three noise components to each other as input signal frequency increases. If each of the three noise components is expressed in r.m.s. terms, the total r.m.s. noise (η_T) of the A/D converter will be the square root of the sum of the squares of its respective noise components. The vertical axis of the plot is the r.m.s. value of the A/D converter's total noise expressed in dB. The horizontal axis is the frequency of the A/D's analog input signal plotted on a logarithmic scale.



At very low (approaching d.c.) input frequencies, aperture noise effectively makes no contribution, and the total noise is equal to the r.m.s. summation of quantization noise and converter noise. As explained earlier, this initial noise level is greater than that solely attributable to theoretical quantization noise and is a constant term in the total r.m.s. noise equation shown below.

η_Q = Quantization Noise

η_C = Converter Noise

η_A = Aperture Noise (slew-rate noise)

$$\eta_{Total\ (r.m.s.)} = \sqrt{\eta_{Q\ (r.m.s.)}^2 + \eta_{C\ (r.m.s.)}^2 + \eta_{A\ (r.m.s.)}^2}$$

$$\eta_T = \sqrt{(\eta_Q^2 + \eta_C^2) + \eta_A^2}$$

Constant Term

Frequency Dependent Term

As the input frequency increases, aperture noise begins to come into play. At some critical frequency (f_C), the contribution made by aperture noise will be equal to that of quantization plus converter noise, and the total noise will have risen 3dB above its initial value (SNR drops 3dB). Aperture noise increases 6dB for every octave increase in input frequency and eventually overwhelms the other noise components which have essentially remained constant. If one maintains a constant input level while increasing the input signal frequency through many decades, the plot of the A/D's SNR vs. input frequency should look like the inverse of the noise plot shown on the previous page. This is demonstrated in the actual plots of SNR vs. frequency for the MN5290 shown previously.

ORDERING INFORMATION

Part Number	Input Voltage Range		Specified Temperature Range	No Missing Codes	Integral Linearity	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics
	Unipolar	Bipolar							
MN6290J	0 to + 10V	± 5V	0°C to + 70°C	13 Bits	± 0.006%FSR	20kHz	10kHz	80dB	– 85dB
MN6290K	0 to + 10V	± 5V	0°C to + 70°C	14 Bits	± 0.003%FSR	20kHz	10kHz	84dB	– 88dB
MN6290S	0 to + 10V	± 5V	– 55°C to + 125°C	13 Bits	± 0.006%FSR	20kHz	10kHz	80dB	– 85dB
MN6290S/B	0 to + 10V	± 5V	– 55°C to + 125°C	13 Bits	± 0.006%FSR	20kHz	10kHz	80dB	– 85dB
MN6290T	0 to + 10V	± 5V	– 55°C to + 125°C	14 Bits	± 0.003%FSR	20kHz	10kHz	84dB	– 88dB
MN6290T/B	0 to + 10V	± 5V	– 55°C to + 125°C	14 Bits	± 0.003%FSR	20kHz	10kHz	84dB	– 88dB
MN6291J	N.A.	± 10V	0°C to + 70°C	13 Bits	± 0.006%FSR	20kHz	10kHz	80dB	– 85dB
MN6291K	N.A.	± 10V	0°C to + 70°C	14 Bits	± 0.003%FSR	20kHz	10kHz	84dB	– 88dB
MN6291S	N.A.	± 10V	– 55°C to + 125°C	13 Bits	± 0.006%FSR	20kHz	10kHz	80dB	– 85dB
MN6291S/B	N.A.	± 10V	– 55°C to + 125°C	13 Bits	± 0.006%FSR	20kHz	10kHz	80dB	– 85dB
MN6291T	N.A.	± 10V	– 55°C to + 125°C	14 Bits	± 0.003%FSR	20kHz	10kHz	84dB	– 88dB
MN6291T/B	N.A.	± 10V	– 55°C to + 125°C	14 Bits	± 0.003%FSR	20kHz	10kHz	84dB	– 88dB

Contact factory for availability of CH device types.

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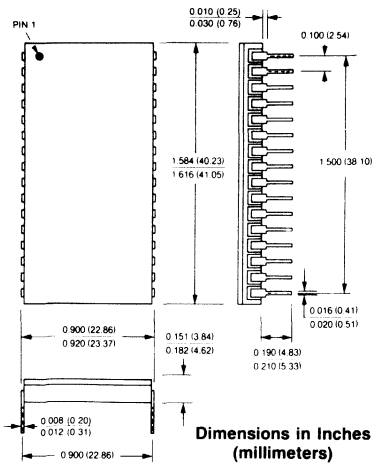
MN6295
MN6296

LOW-DISTORTION, 50kHz
16-Bit, SAMPLING
A/D CONVERTERS

FEATURES

- **50kHz Sampling Rate With Internal T/H Amplifier**
- **25kHz Full-Power Input Bandwidth**
- **84dB Signal-to-Noise Ratio Over Full Bandwidth**
- **−88dB Harmonics Over Full Bandwidth**
- **FFT Testing**
- **Serial and Parallel Outputs**
- **1.3 Watts Power Consumption**
- **32-Pin Side-Brazed DIP**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

32 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN6295/6296 Family of 50kHz, 16-bit, sampling A/D converters offers an outstanding combination of resolving power, sampling rate, low noise and low harmonic distortion. These SA type A/D's are packaged in small, side-brazed, 32-pin, triple-wide DIP's and have internal track-hold (T/H) amplifiers that enable them to accurately sample and digitize 25kHz full-scale input signals at rates up to 50kHz. The package, including the internal T/H, is smaller than that of most stand-alone 16-bit A/D's. Each device is fully FFT (Fast Fourier Transform) tested using contemporary DSP technology and guarantees up to 84dB signal-to-noise ratio (SNR, rms-to-rms) and up to −88dB harmonics and spurious noise.

MN6295 (10V input span) and MN6296 (20V input span) are configured in a manner that makes their internal T/H completely user transparent. A 2.5kΩ input resistor isolates the T/H from its signal source, and the T/H's operational mode is internally controlled by the A/D's status line. Users need only supply start-convert pulses at the desired sampling rate. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's. This type of configuration and testing eliminates the need for potentially confusing and misleading T/H specifications like aperture delay, aperture jitter, charge injection, etc., and also eliminates frustrating attempts to translate data-converter time-domain specifications into frequency-domain performance.

The MN6295/6296 Family offers 4 electrical performance grades (J,K,S and T part-number suffixes) and 2 operating temperature ranges (0°C to +70°C and −55°C to +125°C.

April 1990

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MN6295 MN6296 50kHz SAMPLING 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6295J, K; MN6296J, K	0°C to +70°C
MN6295S, S/B, T, T/B	−55°C to +125°C
MN6296S, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 28)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 21)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 30)	0 to +7 Volts
Digital Inputs (Pins 31, 32)	0 to +5.5 Volts
Analog Inputs (Pins 24, 25)	±15 Volts
Analog Ground (Pin 22) to Digital Ground (Pin 19)	±1 Volt
Ref. Out (Pin 23) Short Circuit Duration	Continuous to Ground

ORDERING INFORMATION

PART NUMBER — **MN6295T/B CH**

- Select MN6295 or MN6296.
- Select suffix J, K, S or T for desired performance and specified temperature range.
- Add "/B" to "S" or "T" models for Environmental Stress Screening.
- Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: MN6295		0 to +10, ±5		Volts
MN6296		±10		Volts
Input Impedance (Note 17): Resistance		2.5		kΩ
Capacitance		50		pF
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 2): Unipolar Ranges		CSB		
Bipolar Ranges		COB		
Logic Levels: Logic "1" ($I_{source} \leq 320\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 3.2mA$)			+0.4	Volts
INTERNAL REFERENCE				
Reference Output (Pin 23): Voltage	+9.9	+10	+10.1	Volts
Drift		±15		ppm/°C
Output Current (Notes 3, 17)			1	mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc Supply	±14.5	±15	±15.5	Volts
+Vdd Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection (Note 14): +Vcc Supply		±0.003	±0.02	%FSR/%Supply
−Vcc Supply		±0.003	±0.02	%FSR/%Supply
+Vdd Supply		±0.001	±0.01	%FSR/%Supply
Current Drains: +Vcc Supply		+42	+55	mA
−Vcc Supply		−30	−40	mA
+Vdd Supply		+48	+60	mA
Power Consumption		1320	1725	mW

PERFORMANCE SPECIFICATIONS (Typical T_A = +25°C, ±V_{CC} = ±15V, +Vdd = +5V unless otherwise indicated)

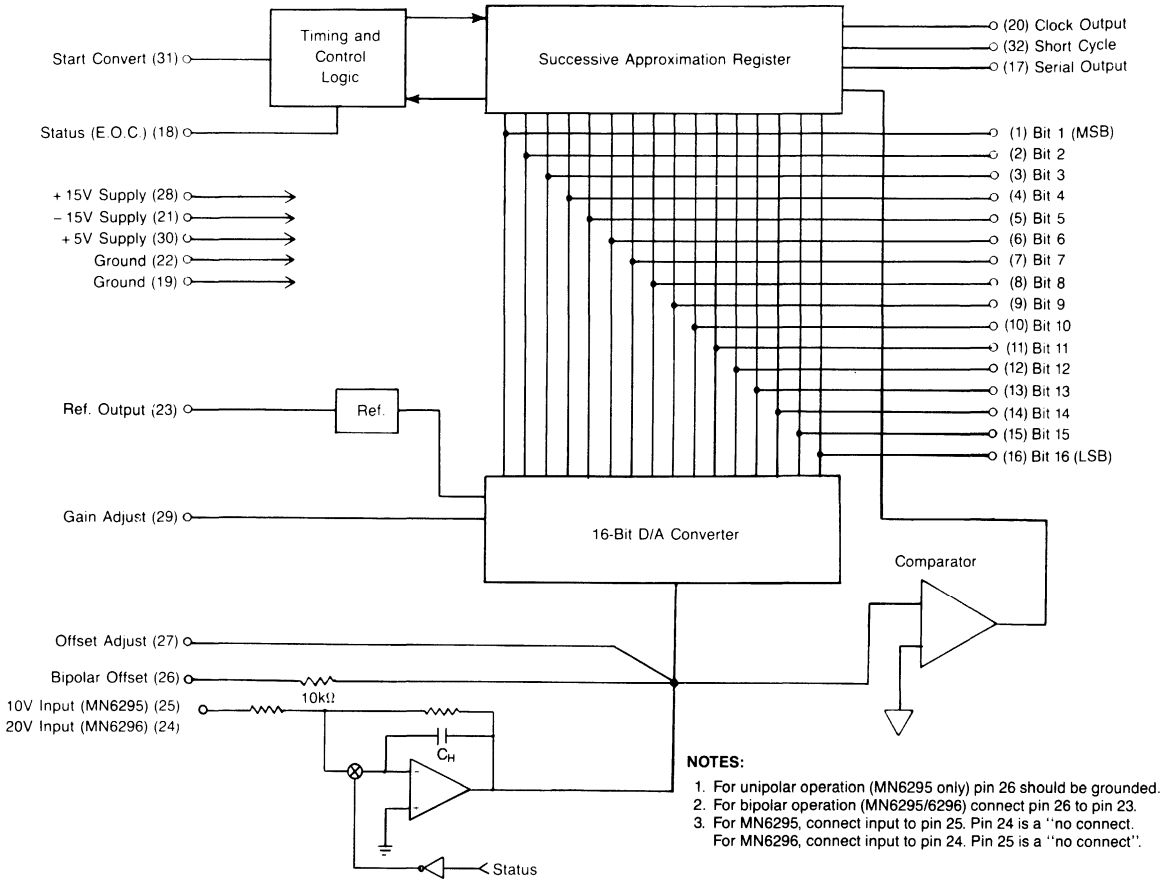
DYNAMIC CHARACTERISTICS	MN6295J MN6296J	MN6295K MN6296K	MN6295S MN6296S	MN6295T MN6296T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	50	50	50	50	kHz
Maximum A/D Conversion Time (Note 5)	16	16	16	16	μsec
Signal-to-Noise Ratio (SNR, Note 6):					
Initial (+25°C) (Minimum)	80	84	80	84	dB
T_{min} to T_{max} (Minimum, Note 7)	78	82	78	82	dB
Harmonics and Spurious Noise (Note 8):					
Initial (+25°C) (Minimum)	−85	−88	−85	−88	dB
T_{min} to T_{max} (Minimum, Note 7)	−82	−85	−82	−85	dB
Input Signal Full-Scale Bandwidth (Minimum, Note 9)	25	25	25	25	kHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C) (Max. Note 16)	±0.006	±0.003	±0.006	±0.003	%FSR
T_{min} to T_{max} (Maximum, Note 7)	±0.012	±0.006	±0.012	±0.006	%FSR
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	13	14	13	14	Bits
T_{min} to T_{max} (Note 7)	13	14	13	14	Bits
Unipolar Offset Error (Notes 10, 11):					
Initial (+25°C) (Maximum)	±0.05	±0.05	±0.05	±0.05	%FSR
Drift (Maximum)	±15	±7.5	±15	±7.5	ppm of FSR/°C
Max Error T_{min} to T_{max} (Note 7, 15)	±0.12	±0.084	±0.2	±0.125	%FSR
Bipolar Zero Error (Notes 10, 12):					
Initial (+25°C) (Maximum)	±0.075	±0.05	±0.075	±0.05	%FSR
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
Max Error T_{min} to T_{max} (Note 7, 15)	±0.15	±0.1	±0.225	±0.15	%FSR
Full Scale Accuracy Error (Notes 10, 13):					
Initial (+25°C) (Maximum)	±0.2	±0.1	±0.2	±0.1	%FSR
Drift (Maximum)	±30	±20	±30	±20	ppm of FSR/°C
Max Error T_{min} to T_{max} (Note 7, 15)	±0.35	±0.2	±0.5	±0.3	%FSR

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. CSB=complementary straight binary.
   COB=complementary offset binary.
   See table of transition voltages in section labeled Digital Output Coding.
3. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 23 connected to pin 26), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 50kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at rates of 55kHz or higher.
5. Whenever Status (pin 18) is low (logic "0"), the internal T/H is in the track mode, and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0dB) at any frequency up to 25kHz.
7. MN6295J, K and MN6296J, K are fully specified for 0°C to +70°C operation. MN6295S, S/B, T, T/B and MN6296S, S/B, T, T/B are fully specified for −55°C to +125°C operation.
8. This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
9. This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 50kHz rate.
10. Adjustable to zero with external potentiometer.
11. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6295 on its unipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
12. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1000 0000 0000 0000 to 0111 1111 1111 1111 when operating the MN6295/6296 on a bipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
13. Full scale accuracy specifications apply at negative full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
15. Listed maximum error-over-temperature specifications for unipolar offset, bipolar zero and full scale accuracy correspond to the combination of maximum room-temperature errors and worst case drift conditions to describe the worst case error that might be encountered over the entire specified temperature range.
16. ±0.006%FSR is equivalent to ±½LSB for 13 bits and is equal to ±0.6mV for a device with a 10V full scale range (0 to −10V or ±5V input range). ±0.003%FSR is equivalent to ±½LSB for 14 bits and is equal to ±0.3mV for a device with a 10V full scale range.
17. These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



NOTES:

1. For unipolar operation (MN6295 only) pin 26 should be grounded.
2. For bipolar operation (MN6295/6296) connect pin 26 to pin 23.
3. For MN6295, connect input to pin 25. Pin 24 is a "no connect.
   For MN6296, connect input to pin 24. Pin 25 is a "no connect".

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — MN6295 and MN6296 are 16-bit, sampling, A/D converters. Each contains a 16-bit successive-approximation type A/D and a companion track-hold (T/H) amplifier. The T/H's enable MN6295 and MN6296 to accurately and repetitively sample and digitize dynamically changing input signals in both traditional data-acquisition and comtemporary DSP-type applications.

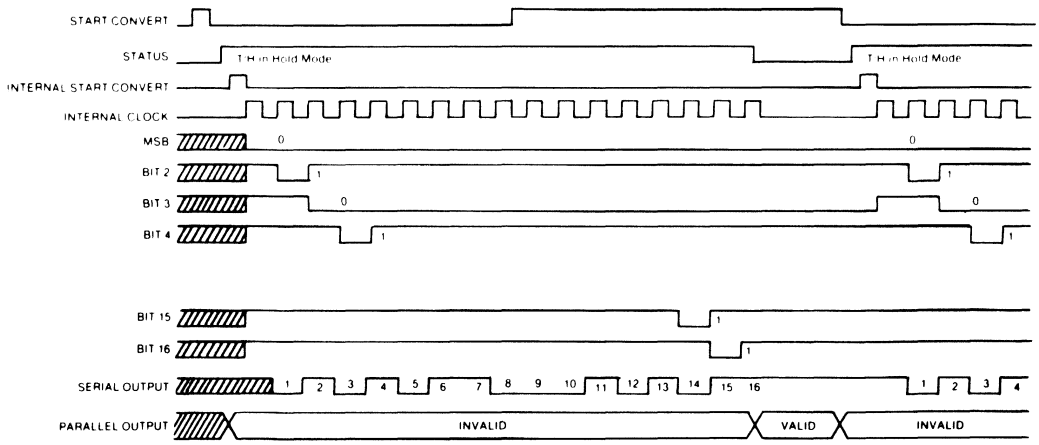
Successive approximation (SA) type A/D converters, when operated without the aid of T/H amplifiers, are severely limited in their ability to accurately convert changing analog input signals. The traditional rule of thumb for gauging such performance is that the A/D's are incapable of accurately converting signals that are slewing faster than (±½LSB)/(conversion time). For a 14-bit A/D with an input range of ±10V and a conversion time of 16μsec, this corresponds to an input slew-rate limit of ±38μV/μsec. If one wishes to express the slew-rate limit as a bandwidth for a full-scale input sinusoid, it corresponds to 0.61Hz.

The proliferating use of A/D converters in DSP applications has resulted in significantly greater demands on A/D's to be able to convert dynamic signals, particularly sinusoids. More and more frequently, T/H amplifiers are used with A/D's to enable them to accomplish this task.

MN6295/6296 are extremely user friendly. They have been configured in a manner that virtually eliminates all of the problems encountered when mating T/H's and successive approximation A/D's and driving the pair from real-world signal sources. The T/H is truly transparent. A 2.5kΩ input resistor isolates it from the external signal source, and its output is internally connected directly to the input of the A/D converter. The output current, impedance and transient-response characteristics of the T/H have been optimized for driving the 16-bit SA A/D. More importantly, the critical dynamic characteristics of the T/H (aperture delay, aperture jitter, small and large signal bandwidths, droop rate, etc.) have been similarly optimized. Most importantly, the critical inter-device timing relationships (T/H mode control, transient decay time, etc.) are internally controlled by MN6295/6296's timing and control circuitry. All that users need to provide externally is the start convert pulse.

The falling edge of the start convert pulse activates MN6295/6296's internal timing circuitry. Immediately, the T/H (which has been in the track or signal-acquisition mode up until this time) is driven into the hold mode, instantaneously "freezing" the value of the analog input signal. Simultaneously, MN6295/6296's status output (also called "End of Conversion" or E.O.C.) is set to a logic "1", indicating that the T/H is now in hold; that an A/D conversion is now in progress;

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits) (Note 6)		15	16	μsec
Internal Clock Frequency (Notes 4, 8)	110	1.07	1.19	MHz
Start Convert Pulse Width (Notes 2, 7)	40			nsec
Delay Falling Edge of Start to (Note 8): Status="1" Clock Output="1"		30 350		nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20		50	nsec
Delay LSB Valid to Falling Edge of Status (Notes 3, 8)	20	40		nsec

TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command can be either a positive or negative pulse at least 10nsec wide. Conversions are initiated on the falling edge of the Start Convert command.
3. Data will be valid 20nsec prior to the falling edge of Status (E.O.C.).
4. The internal clock is enabled and the conversion commences following an internal delay which allows for T/H switching and settling.
5. When the converter is initially "powered up" it may come on at any point in the conversion cycle.
6. Conversion time is defined as the width of the Status (E.O.C.) pulse.
7. The minimum time between falling edges of the Start Convert command is 20μsec.
8. These parameters are listed for reference only and are not tested.

and that the parallel output data (from the previous conversion) is no longer valid. MN6295/6296's internal timing logic now provides approximately 350nsec of delay to permit the track-to-hold switching transient at the output of the T/H to decay. Subsequently, the internal clock is started, and the 16-bit A/D conversion of the held signal proceeds.

The value of the hold capacitor used in MN6295/6296's internal T/H has been selected so that T/H output droop, even over temperature, it not significant (greater than ± ½LSB) during the A/D's conversion time. Similarly, the offset and pedestal voltages, as well as the gain error, of the T/H do not contribute to the overall accuracy of the sampling A/D because they are effectively nulled out during our active laser trimming of the A/D converter.

At the completion of the A/D conversion, MN6295/6296's internal control logic turns off the internal clock; drops the status output back to a logic "0"; and commands the T/H back into the track mode to acquire a new input signal. Status going low signifies that the conversion is complete and that the parallel output data is valid. A 20nsec delay has been added between the finalization of the LSB and the falling edge of status. This ensures that all output bits are valid when status falls and permits the use of this trailing edge to clock data into output latches. Output data remains valid until the falling edge of the next start convert pulse.

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracies from MN6295/6296. The unit's two ground pins (pin 19 and 22) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If the grounds must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between the analog ground (pin 22) and digital ground (pin 19) as close to the unit as possible. Wide conductor runs should be employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Bipolar Offset (pin 26), Analog Input (pins 24,25), Offset Adjust (pin 27) and Gain Adjust (pin 29) are particularly noise susceptable. Care should be taken to avoid long runs or runs close to digital lines when utilizing these inputs. Input signal lines should be as short as possible. In bipolar operation, where Bipolar Offset (pin 26) is connected to Reference Output (pin 23), a short jumper should be used. For unipolar operation (MN6295 only) pin 26 should be grounded. For external gain or offset adjustment, the series resistor(s) should be located as close to Offset Adjust (pin 27) or Gain Adjust (pin 29) as possible. A 0.01μF capacitor should be connected between Gain Adjust (pin 29) and Analog Ground as close to the package as possible.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN6295/6296. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used.

If short-cycling is not used, the Short-Cycle pin (pin 32) must be connected to +5V (pin 30).

THE INTERNAL T/H AMPLIFIER

As stated in the Description of Operation, MN6295/6296's internal T/H amplifier is transparent to the user. The T/H's output is connected directly to the A/D's input and its operational mode is controlled by the Timing and Control Logic (see Block Diagram). The user is not required to supply additional support timing circuits sometimes necessary when mating an A/D with its companion T/H. Additionally, MN6295/6296 users need not concern themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6295/6296 and are, in fact, impossible to directly test because the T/H's output and control lines are not accessable at the device pins. Frequency-domain specifications like input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc. obviates the need for knowing the specific T/H time-domain specifications, however, the following table does supply typical values for those critical T/H performance specifications.

Note that the static errors (gain error, track-mode offset error and pedestal) of the T/H function add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D converter offset error. However, when the A/D offset is functionally laser trimmed, it is done with the whole device sampling at a 50kHz rate and the T/H is in the hold mode whenever trimming is actually performed. Consequently, all error sources are compensated for. All static errors on MN6295/6296 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

Typical T/H Performance Specifications	
Gain Error	±0.01%
Gain Linearity Error	±0.001%FSR
Track Mode Output Offset Error	±0.5mV
Pedestal	±0.5mV
Acquisition Time: 10V step to ±0.003%	2.5μsec
20V step to ±0.003%	3μsec
Track-Hold Transient Settling (to ±1mV)	250nsec
Slew Rate	±30V/μsec
Full Power Bandwidth	500kHz
Effective Aperture Delay Time	−25nsec
Aperture Jitter	0.4nsec
Droop Rate	±0.05μV/μsec
Hold-Mode Feedthrough Attenuation	−86dB

PARALLEL OUTPUTS—During the successive approximation process the weight of each bit is compared to the value of the analog input voltage. The converter is reset to MSB-0111 1111 1111 1111-LSB by the rising edge of the first clock pulse. Subsequent rising clock edges set the bit previously tested to its final state and brings the next bit to be tested to a logic "0". This process continues until all bits have been tested and Status returns to a logic "0". Valid parallel output data can only be latched at the end of the sample/conversion cycle.

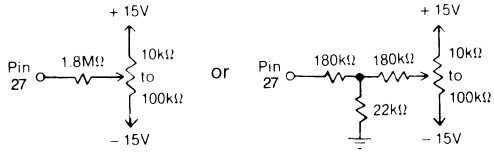
The LSB bit is valid 20nsec prior to the falling edge of Status (E.O.C.), therefore, this edge may be used to latch parallel output data. While the converter is idling (Status is "0"), the parallel output data from the most recent conversion remains valid until the start of the next conversion cycle.

SERIAL OUTPUT—Serial output data is provided only during the conversion process and is in a NRZ (non-return-to-zero) format. The data is coded the same as parallel output data and is synchronous with the internal clock. Each serial output bit is valid 20nsec after the rising clock edge (serial output data lags parallel output by one clock cycle, see timing diagram) and can be strobed into a shift register by rising edges of the internal clock.

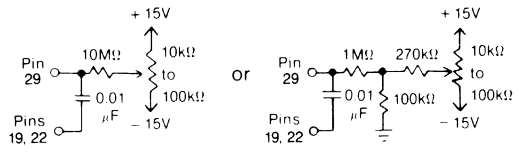
OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS—Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, Offset Adjust (pin 27) should be left open and a 0.01μF capacitor should be connected from Gain Adjust (pin 29) to Ground.

ZERO ADJUSTMENT—Connect the zero adjust potentiometer as shown below. For unipolar (MN6295 only), apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off.

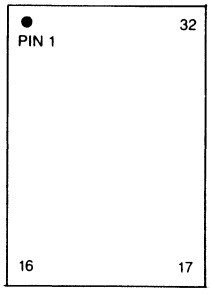
For bipolar ranges (MN6295 and MN6296), apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "flickering."



GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off. A 0.01μf capacitor should be connected from Gain Adjust (pin 29) to Ground.



PIN DESIGNATIONS



1	Bit 1 (MSB)	32	Short Cycle
2	Bit 2	31	Start Convert
3	Bit 3	30	+5V Supply (+Vdd)
4	Bit 4	29	Gain Adjust
5	Bit 5	28	+15V Supply (+Vcc)
6	Bit 6	27	Offset Adjust
7	Bit 7	26	Bipolar Offset
8	Bit 8	25	10V Input (MN6295; N.C. MN6296)
9	Bit 9	24	20V Input (MN6296; N.C. MN6295)
10	Bit 10	23	Reference Output (+10V)
11	Bit 11	22	Ground
12	Bit 12	21	−15V Supply (−Vcc)
13	Bit 13	20	Clock Output
14	Bit 14	19	Ground
15	Bit 15	18	Status
16	Bit 16 (LSB)	17	Serial Output

DIGITAL OUTPUT CODING

Analog Input			Digital Output	
0 to −10V	±5V	±10V	MSB	LSB
0	+F.S.		0000 0000 0000 0000	
−½LSB	+F.S. − ½LSB		0000 0000 0000 000ø*	
−½F.S. + ³⁄₂LSB	+³⁄₂LSB		0111 1111 1111 111ø*	
−½F.S. + ½LSB	+½LSB		øøøø øøøø øøøø øøøø*	
−½F.S. − ½LSB	−½LSB		1000 0000 0000 000ø*	
−F.S. + ³⁄₂LSB	−F.S. + ³⁄₂LSB		1111 1111 1111 111ø*	
−F.S.	−F.S.		1111 1111 1111 1111	

CODING NOTES:

1. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV. 1LSB for 14 Bits = 610.4μV.
2. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV. 1LSB for 14 Bits = 1.22mV.
3. For unipolar ranges, the coding is straight binary.
4. For bipolar ranges, the coding if offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN6295/MN6296 continuously converting, the output bits indicated as ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the ±10V range, the transition from output code 0000 0000 0000 0000 to output code 0000 0000 0000 0001 (or vice versa) will ideally occur at an input of +9.999847V (+F.S. −½LSB). Subsequently, any voltage greater than +9.999847V will give a digital output of all "0's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of +0.000153 volts. The 1111 1111 1111 1110 to 1111 1111 1111 1111 transition will occur at −9.999542V. An input more negative than this level will give all "1's."

INPUT RANGE SELECTION

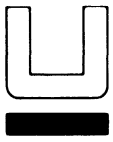
Part Number	Range	Connect Pin 26 to Pin
6295	0 to −10V	Ground
6295	±5V	23
6296	±10V	23

ORDERING INFORMATION

Part Number	Input Voltage Range		Specified Temperature Range	No Missing Codes	Integral Linearity (3)	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics
	Unipolar	Bipolar							
MN6295J	0 to −10V	±5V	0°C to +70°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6295K	0 to −10V	±5V	0°C to +70°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6295S	0 to −10V	±5V	−55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6295S/B (1)	0 to −10V	±5V	−55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6295S/B CH(2)	0 to −10V	±5V	−55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6295T	0 to −10V	±5V	−55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6295T/B (1)	0 to −10V	±5V	−55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6295T/B CH(2)	0 to −10V	±5V	−55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6296J	N.A.	±10V	0°C to +70°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6296K	N.A.	±10V	0°C to +70°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6296S	N.A.	±10V	−55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6296S/B (1)	N.A.	±10V	−55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6296S/B CH(2)	N.A.	±10V	−55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	−85dB
MN6296T	N.A.	±10V	−55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6296T/B (1)	N.A.	±10V	−55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB
MN6296T/B CH(2)	N.A.	±10V	−55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	−88dB

Notes:

1. Includes Environmental Stress Screening.
2. Contact factory for availability of CH device types.
3. ±0.006%FSR is equivalent to ±½LSB for 13 bits.
   ±0.003%FSR is equivalent to ±½LSB for 14 bits.



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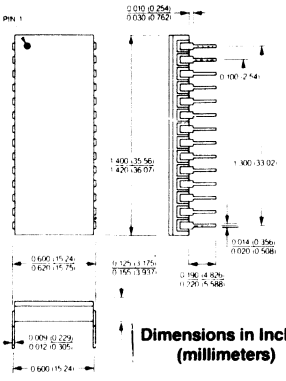
MN6400

50kHz, 16-Bit
SELF-CALIBRATING
SAMPLING A/D CONVERTER

FEATURES

- **Self-Calibrating A/D Provides True 16-bit Performance**
- **50kHz Sampling Rate with Inherent T/H Function**
- **16-Bit No-Missing-Codes Guaranteed Over Full Operating Temperature Range**
- **Complete Contains:**
  - **T/H Function**
  - **Analog Input Buffer**
  - **Reference**
  - **Timing and Control Logic**
  - **μP Interface**
  - **Parallel Data Bus Driver**
- **±1LSB Integral Linearity**
- **88dB SNR, −98dB Harmonics**
- **740mW Maximum Power Consumption**
- **Fully specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

28 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN6400 is a complete self-calibrating, 16-bit, 50kHz Sampling A/D converter. Each Sampling A/D contains an inherent T/H function, analog input buffer amplifier, reference, timing and control logic circuitry, microprocessor interface and parallel data bus driver making it the most complete device of its kind. These Sampling A/D converters are packaged in small, 28-pin, side-brazed, double-wide DIPs. The inherent T/H function allows these devices to accurately sample and digitize dynamically changing analog input signals at rates up to 50kHz. The package, including all of the functions, is smaller than that of most stand-alone 16-bit A/Ds. Each device is fully tested using contemporary FFT (Fast Fourier Transform) technology and guarantees frequency-domain performance — no more guesswork in converting time-domain specifications (linearity, accuracy, etc.) into frequency-domain performance.

The MN6400 offers four analog input voltage ranges (0 to +5V, 0 to +10V, ±5V and ±10V) whose Bipolar and Unipolar operation is digitally controlled. These devices may be operated from the internal clock, or for critical sampling applications, these devices may be operated from a low-jitter crystal clock circuit. Serial output data is provided synchronized to the serial clock output. The internal parallel data bus driver with its 3-state outputs enables the MN6400 to connect directly to system data buses without loading concerns.

The MN6400 offers users four electrical performance grades (J,K,S and T models) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C) In addition, S and T models are available with environmental stress screening. Contact factory for availability of fully compliant MIL-H-38534 devices.

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MN6400 50kHz 16-Bit SELF-CALIBRATING SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6400 J,K	0°C to +70°C
MN6400 S,T	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 15)	0 to +16.5 Volts
−15V Supply (−V_{CC}, Pin 14)	0 to −16.5 Volts
+5V Supply (+V_{DD}, Pin 21)	−0.3 to +6.0 Volts
Digital Inputs:	
(Pins 10, 11, 12, 13, 22, 23, 24)	−0.3 to +V_{DD} +0.3V
Analog Inputs: (Pins 17, 18)	±V_{CC}

ORDERING INFORMATION

PART NUMBER **MN6400T/B CH**

Select suffix J, K, S or T for desired performance and specified temperature range.
Add "/B" suffix to "S" or "T" models for Environmental Stress Screening.
Add "CH" to "S/B" and "T/B" models for MIL-H-38534 compliant devices.

DESIGN SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V unless otherwise specified) (Note 10)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V Input		0 to +5		Volts
		−5 to +5		Volts
10V Input		0 to +10		Volts
		−10 to +10		Volts
Input Impedance: 5V Input		5		kΩ
10V Input		10		kΩ
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			±10	μA
Logic "0" (V_{IL} = +0.4V)			±10	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{OH} = +6.0mA)	+3.9	+4.3		Volts
Logic "0" (I_{OL} = −6.0mA)		+0.16	+0.26	Volts
3-State Leakage Current			±10	μA
INTERNAL REFERENCE				
Reference Output: Voltage (Note 11)	+4.45	+4.5	+4.55	Volts
Drift		±3	±10	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supply	±11.4	±15	±16.5	Volts
+V_{DD} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection: +V_{CC} Supply		±.0001	±.001	%FS/%VS
−V_{CC} Supply		±.0001	±.001	%FS/%VS
+V_{DD} Supply		±.0001	±.001	%FS/%VS
Current Drains: +V_{CC} Supply		+5	+10	mA
−V_{CC} Supply		−20	−31	mA
+V_{DD} Supply		+14	+25	mA
Power Consumption		445	740	mW

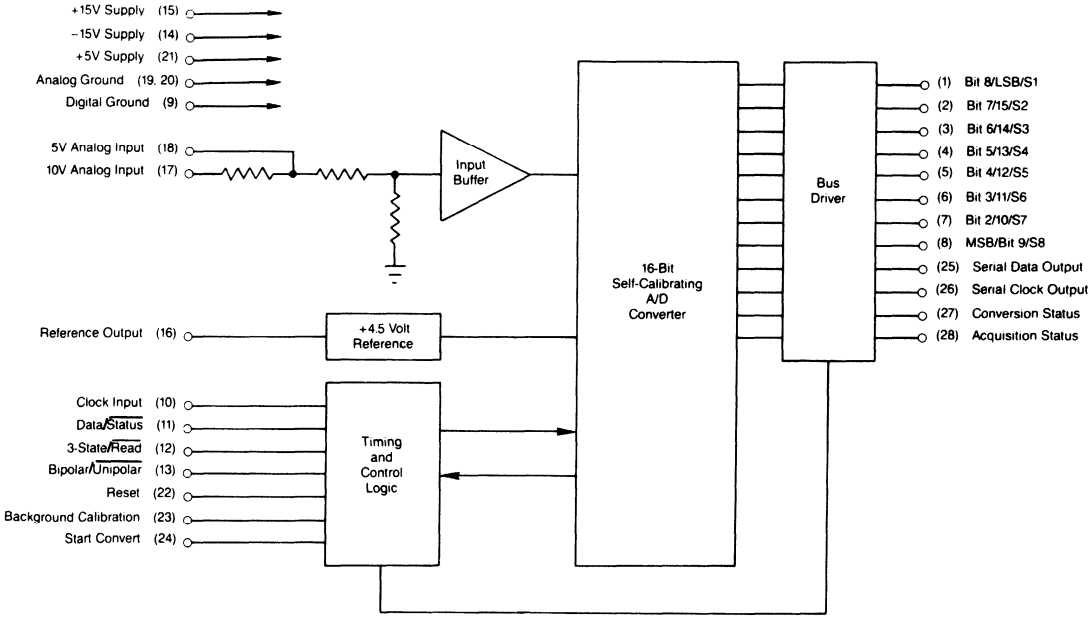
SPECIFICATION NOTES:

1. External Master Clock frequency set to 4MHz, synchronous sampling mode and background calibration disabled.
2. Specification listed applies after calibration at any temperature within the specified temperature range.
3. Specification listed applies over the specified temperature range after initial calibration at 25°C.
4. Specification listed applies after calibration at 25°C.
5. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6400 on a unipolar range.
6. Bipolar zero error is defined as the difference between the ideal and actual input voltage at which the digital output changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6400 on a bipolar range.
7. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors. Full scale absolute accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scales for bipolar input ranges. Full scale absolute accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0001 to 0000 0000 0000 0000 transition for bipolar input ranges.
8. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full scale analog input sine wave (0dB) at the specified frequencies.
9. This parameter represents the peak-to-peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
10. External Master Clock frequency set to 4MHz and operated in the synchronous sampling mode.
11. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with an 0.1μF capacitor. Reference must not be used for applications circuits without buffering.

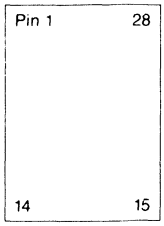
PERFORMANCE SPECIFICATIONS (Typical at +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V unless otherwise indicated) (Note 1)

STATIC CHARACTERISTICS	MN6400J	MN6400K	MN6400S	MN6400T	UNITS
Integral Linearity Error (Max) (Note 2)	±0.0015	±0.0015	±0.0015	±0.0015	%FSR
Integral Linearity Error (Max) (Note 3)	±0.0022	±0.0015	±0.0022	±0.0015	%FSR
Minimum Resolution for Which No Missing Codes is Guaranteed (Note 3)	16	16	16	16	Bits
Unipolar Offset Error (Notes 4, 5)					
Initial (Maximum)	±0.03	±0.02	±0.03	±0.02	%FSR
Drift (Maximum)	±4	±2.5	±4	±2.5	ppm of FSR/°C
Bipolar Zero Error (Notes 4, 6)					
Initial (Maximum)	±0.03	±0.02	±0.03	±0.02	%FSR
Drift (Maximum)	±4	±2.5	±4	±2.5	ppm of FSR/°C
Full Scale Accuracy Error (Notes 4, 7)					
Initial (Maximum)	±0.1	±.05	±0.1	±.05	%FSR
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
DYNAMIC CHARACTERISTICS					
Minimum Guaranteed Sampling Rate	50	50	50	50	kHz
Maximum A/D Conversion Time	16.25	16.25	16.25	16.25	μsec
Signal-to-Noise Ratio (Notes 3, 8):					
Initial (+25°C): 1kHz Full Scale Input (Minimum)	85	88	85	88	dB
12kHz Full Scale Input (Minimum)	81	84	81	84	dB
T_{min} to T_{max}: 1kHz Full Scale Input (Minimum)	83	85	83	85	dB
12kHz Full Scale Input (Minimum)	79	82	79	82	dB
Harmonics and Spurious Noise (Notes 3, 9):					
Initial (+25°C): 1kHz Full Scale Input (Maximum)	−96	−98	−96	−98	dB
12kHz Full Scale Input (Maximum)	−90	−92	−90	−92	dB
T_{min} to T_{max}: 1kHz Full Scale Input (Maximum)	−94	−96	−94	−96	dB
12kHz Full Scale Input (Maximum)	−88	−90	−88	−90	dB

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Bit 8 /Bit 16 (LSB) or S1	28	Acquisition Status
2	Bit 7 /Bit 15 or S2	27	Conversion Status
3	Bit 6 /Bit 14 or S3	26	Serial Clock Output
4	Bit 5 /Bit 13 or S4	25	Serial Data Output
5	Bit 4 /Bit 12 or S5	24	Start Convert
6	Bit 3 /Bit 11 or S6	23	Background Calibration
7	Bit 2 /Bit 10 or S7	22	Reset
8	Bit 1 (MSB)/Bit 9 or S8	21	+5V Supply ($+V_{DD}$)
9	Digital Ground	20	Analog Ground
10	Clock Input	19	Analog Ground
11	Data/$\overline{\text{Status}}$	18	5V Analog Input
12	3-State/$\overline{\text{Read}}$	17	10V Analog Input
13	Bipolar/$\overline{\text{Unipolar}}$	16	Reference Output (+4.5V)
14	−15V/−12V Supply ($-V_{CC}$)	15	+15V/+12V Supply ($+V_{CC}$)

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN6400 is a 16-bit Sampling A/D converter containing an inherent, user-transparent T/H function and features self-calibration, μP-interface logic and an 8-bit parallel data bus driver. Self-calibration and the inherent T/H function enable the MN6400 to accurately sample and digitize dynamically changing analog input signals at a 50kHz throughput rate.

The MN6400 is designed to operate from ±12 or ±15V and +5V power supplies and an external or internally generated Master Clock. After power-up, the MN6400 must be reset by bringing Reset (pin 22) high for a minimum of 100nsec. Bringing Reset high clears the internal logic circuitry while returning Reset low initiates a full calibration cycle. Full calibration cycles require 1,441,020 Master Clock cycles (360.255msec with external 4MHz Master Clock applied). Conversion Status (pin 27) is high during calibration and returns low when complete.

After calibration, conversions can be initiated by the falling edge of Start Convert. The signal applied to Start Convert (pin 24) must remain low for a minimum of one Master Clock cycle plus 50nsec. This translates into 300nsec with the use of an external 4MHz clock. Start Convert must return high prior to the end of the conversion cycle (65 clock cycles, 16.25μsec with 4MHz clock) to allow sufficient time for the next sample to be acquired.

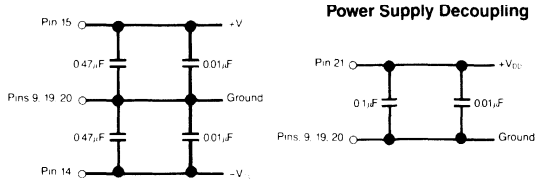
With the conversion complete, output data and converter status information may be read using various combinations of input control lines. Both serial and parallel data are available. Serial data is available at Serial Data Output (pin 25) and is syncronous and valid with the rising edges of Serial Data Clock Output (pin 26). Serial data is presented MSB first, and is only available during the conversion cycle. Parallel data is available in two 8-bit bytes. Once a conversion is complete and Data/$\overline{\text{Status}}$ (pin 11) is set high, parallel output data is read by bringing 3-State/$\overline{\text{Read}}$ low. MSB-byte data (MSB-bit 8) is first to be presented to data output lines (pins 1-8). Toggling 3-State/$\overline{\text{Read}}$ (that is, to bring it high and then low again) presents LSB-byte data. Output data lines are in the high-impedance state when 3-State/$\overline{\text{Read}}$ is high.

In addition to conversion data, device status information can also be accessed via the 8-bit data lines (pins 1-8). Status information is presented when Data/$\overline{\text{Status}}$ is set low. A detailed description of the types of status information which is provided and the pin locations of this information appear in the section labeled Parallel Output Pin Description - Status Information.

POWER SUPPLIES AND LAYOUT — The MN6400 is powered from standard supply voltages of +12/15V (pin 15), −12/15V (pin 14) and +5V (pin 21). The analog ground (pins 19,20) and digital ground (pin 9) are separated to minimize analog and digital circuit interaction. The analog ground is internally used as a reference point, therefore it should be used as the system analog ground reference point. Care must be taken to reduce the system noise to a level below the MN6400's high-resolution conversion capability.

It is recommended that the power supplies be decoupled in the following manner. The +12/15V and −12/15V supplies should be bypassed with a 0.01 μF capacitor in parallel with a 0.47 μF capacitor to analog ground. The +5V supply, which powers both analog and digital internal circuitry, should be bypassed with a 0.1 μF capacitor in parallel with a 0.01 μF capacitor to analog ground. The optimum value decoupling capacitors to use may vary depending on the users system noise characteristics.

Power Supply Decoupling



DEVICE CALIBRATION — The MN6400 features two user-controlled self-calibration modes of operation. Self-calibration insures optimum performance at any temperature and at any time throughout the lifetime of the device. Self-calibration also eliminates the need for additional external circuitry to maintain operation of the device within specification.

The first mode of calibration is called reset, and its initiation is controlled with Reset (pin 22). A reset calibration must be performed after the device is powered-up, and can be repeated optionally after the device reaches its operating temperature. The required initial reset is initiated by strobing the Reset pin high for a minimum of 100 nsec. When Reset is brought high, internal logic clears. When Reset returns low, a single full calibration lasting 1,441,020 master clock cycles begins (360.255 msec w/ 4 MHz clock). During reset the Conversion Status (pin 27) output will be in a high state, and will fall low upon completion of calibration.

The reset mode of calibration can be initiated by either hardware using a power-up reset circuit or by software in microprocessor control applications. Care must be taken to avoid an inadvertent reset brought about by bringing 3-State/Read (12), Data/Status (pin 11) and Start Convert (pin 24) low simultaneously.

The second mode of calibration is called background calibration, which is activated by either tying Background Calibration (pin 23) to digital ground or bringing Background Calibration and 3-State/Read (pin 12) both low. This mode differs from reset calibration in that a fractional portion of the total calibration time is added to the end of each conversion. After 72,051 conversions, the calibration cycle is complete. The conversion time of the device when background calibration is active is extended by 20 master clock cycles (5μsec w/4 MHz clock). Except for the decrease in throughput rate, the background calibration mode is transparent to the user.

MASTER CLOCK — The MN6400 operates from a master clock that can be supplied externally or generated internally depending upon the signal applied to Clock Input (pin 10). A logic low on this pin will activate the 2 MHz minimum internal clock. Optionally, the user can supply a TTL or CMOS system clock with a maximum frequency of 4MHz (100kHz minimum) to the Clock Input. All device timing characteristics scale to the master clock frequency. The internal oscillator exhibits relatively high jitter compared to crystal oscillators, which may affect performance in some sampling applications.

INITIATING CONVERSIONS — A falling edge on the Start Convert (pin 24) digital input will set the device into the hold mode and initiate a conversion cycle. The Start Convert input must remain low for a minimum of one master clock cycle plus 50 nsec (300 nsec w/4 MHz clock). It must return high before the minimum conversion time of 65 clock cycles (16.25μsec w/4 MHz clock) to allow sufficient time for acquisition of the next sample.

T/H ACQUISITION — The MN6400 is a sampling A/D converter, therefore it requires a finite amount of time to accurately acquire an analog input signal before performing a conversion. At the completion of a conversion, signalled by the falling of Conversion Status (pin 27), the device automatically enters the acquisition mode and begins to track the analog input. A minimum acquisition time of six master clock cycles plus 2.25μsec (3.75μsec w/4 MHz clock) is required to acquire the input signal. When sufficient time has elapsed after a conversion for the acquisition of the input signal, the Acquisition Status (pin 28) output will fall low. It returns high on initiation of a new conversion cycle. When driving the MN6400 from a high source impedance, the necessary acquisition time should be extended to allow for the resultant increase in the input settling time constant.

The MN6400's acquisition circuitry operates from a delayed and divided down internal clock frequency of 1/4 times the master clock. If sampling is not synchronized to this internal clock, a sample will be synchronously taken but may not be converted until up to four master clock cycles later (1μsec w/ 4 MHz clock). In other words, when Start Convert goes low and is not synchronous with the internal clock, a maximum of four master clock cycles may occur before Conversion Status goes high. This asynchronous uncertainty adds these four master clock cycles plus 235 nsec of internal clock delay (1.235μsec w/4 MHz clock) to the conversion time.

When performing an asynchronous sampling operation, the device can operate at 69 master clock cycles plus 235 nsec for conversion and six master clock cycles plus 2.25 μsec for acquisition for a total of 75 master clock cycles plus 2.485μsec (21.235μsec w/4 MHz clock). This corresponds to a 47.1 kHz maximum throughput rate. Although the sample is asynchronously converted, the sample itself is taken synchronously upon the falling edge of Start Convert. This is particularly important to users in DSP applications.

To synchronize the sampling operation to the internal clock, the Acquisition Status (pin 28) output can be connected to the Start Convert (pin 24) input. The Acquisition Status output is synchronized to the internal clock, thereby eliminating the sampling uncertainty and enabling device operation at 65 master clock cycles for conversion and 15 master clock cycles for acquisition for a total of 80 master clock cycles (20μsec w/4 MHz clock). This corresponds to a 50kHz maximum throughput rate.

ANALOG INPUTS — The MN6400 can be operated in four user-selectable input voltage range configurations. They are 0 to +5V, ±5V, 0 to +10V and ± 10V. The 5V Analog Input (pin 18) is used for 5V full scale analog inputs, and the 10V Analog Input (pin 17) is used for 10V full scale analog inputs. Selection of a unipolar or bipolar input transfer function is made with the Bipolar/Unipolar digital input (pin 13). A logic high on this pin selects a bipolar transfer function of analog input voltage between −Full Scale and +Full Scale. A logic low on this pin selects a unipolar transfer function of analog input voltages between 0V and +Full Scale.

The unipolar voltage ranges are digitally represented at the output in Straight Binary format. An all zero's output corresponds to 0V at the input, and an all ones output corresponds to +FS range voltage at the input. The bipolar voltage ranges produce digital outputs in Offset Binary format. An all zeros output corresponds to an analog input voltage of −Full Scale Range.

The MN6400 contains an input buffer configured to condition the analog input signal for optimum acquisition and conversion performance. Additional signal-conditioning circuitry meeting 16 bit performance levels can be used to drive the analog inputs.

REFERENCE OUTPUT — The MN6400 contains an internal +4.5V low drift precision reference. This reference voltage appears at Reference Output (pin 16) to allow for the attachment of a 0.1μF capacitor in parallel with a 10μF tantalum capacitor. These capacitors are required to allow the reference to exhibit a low output impedance throughout the frequency range of device operation. The optimum value for these capacitors will vary depending on the master clock frequency being used.

It is recommended not to use the Reference Output pin for any additional circuitry requirements. If absolutely necessary, the Reference Output can be buffered and used to fulfill additional circuitry requirements.

DIGITAL OUTPUTS — The MN6400 supplies converted data and device status information on outputs capable of driving system bus connections directly. The device presents both parallel data in an 8-bit MSB/LSB byte format and serial data with serial clock output. In addition to digital output data, device status information can be read via the parallel data bit outputs.

The information present on the 8-bit bus is controlled by the state of Data/Status (pin 11). When high, converted data can be read on the bus.

When low, the status register can be read on the bus. Converted data appears on the bus in parallel MSB/LSB byte format. A read operation is executed by bringing the 3-State/Read (pin 12) input low. The first read operation following a conversion will bring the bus out of the 3-state condition and present the eight MSBs (MSB on pin 8 through bit 8 on pin 1). On the second read operation following a conversion, executed by bringing 3-State/Read back high and then low again, the eight LSBs will be presented (Bit 9 on pin 8 through LSB on pin 1). On subsequent reads before the next conversion is complete, the MSB/LSB byte will toggle. Data is valid after a delay of 100 nsec from the falling edge of Conversion Status, and remains valid until the next Conversion Status falling edge.

PARALLEL OUTPUT PIN DESCRIPTION

PIN#	MSB BYTE	LSB BYTE	STATUS BIT	STATUS INFORMATION
1	Bit 8	LSB	S1	Same as Conversion Status (pin 27).
2	Bit 7	Bit 15	S2	Reserved for factory use.
3	Bit 6	Bit 14	S3	LSB/$\overline{\text{MSB}}$ byte indicates which data byte will appear on next read operation.
4	Bit 5	Bit 13	S4	Same as Acquisition Status (pin 28)
5	Bit 4	Bit 12	S5	Reserved for factory use.
6	Bit 3	Bit 11	S6	Tracking — high when device is tracking the input.
7	Bit 2	Bit 10	S7	Converting — high when the device is converting the input.
8	MSB	Bit 9	S8	Calibrating — high when the device is calibrating.

Device status information can be read on the bus whenever Data/$\overline{\text{Status}}$ is low. Status bit pin locations and definitions appear under the section labeled Parallel Output Pin Description.

Converted data is available in Serial format (MSB first) at the Serial Data Output (pin 25). Serial data is present at the output when it is determined during conversion. Serial data is valid and can be latched with the rising edge of Serial Clock Output (pin 26).

The Conversion Status (pin 27) and Acquisition Status (pin 28) outputs provide the user with device status information detailed in the Pin Description Section. Conversion Status will remain low for four master clock cycles if 3-State/$\overline{\text{Read}}$ is held low. These status outputs along with the serial data and clock output are not 3-stateable, but have direct bus-driver output capability.

PIN DESCRIPTION

POWER SUPPLY CONNECTIONS

Pin Designation	Function
+15V/+12V Supply (+V_{CC}, Pin 15)	Positive analog power supply. Devices will operate from nominal +12V or +15V supplies.
−15V/−12V Supply (−V_{CC}, Pin 14)	Negative analog power supply. Devices will operate from nominal −12V or −15V supplies.
+5V Supply (+V_{DD}, Pin 21)	Positive digital and analog power supply. Device operates from nominal +5V.

ANALOG INPUTS

Pin Designation	Function
10V Analog Input (Pin 17)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +10V analog input signals. When in Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±10V analog input signals.
5V Analog Input (Pin 18)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +5V analog input signals. When in the Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±5V analog input signals.

ANALOG OUTPUTS

Pin Designation	Function
Reference Output (Pin 16)	Provides reference voltage of +4.5V to be bypassed to Analog Ground with an external 10μF tantalum capacitor in parallel with a 0.1μF ceramic disk capacitor. Use of this reference in additional circuit applications requires the use of an external, low-input-current buffer amplifier.

DIGITAL OUTPUTS

Pin Designation	Function
Parallel Data Outputs (Pins 1-8)	3-stated output byte offers converted data in MSB-byte, LSB-byte format or status register information (S1-S8). Data Output is controlled by 3-State/$\overline{\text{Read}}$ input and is dependent on state of Data/$\overline{\text{Status}}$. See Digital Output section for a detailed description of data output pins.
Serial Data Output (Pin 25)	Presents serial output data valid on the rising edge of Serial Clock Output (pin 26). Data is available only during conversion, and is presented MSB first.
Serial Clock Output (Pin 26)	Provides clock edges to facilitate latching of serial output data.
Conversion Status (Pin 27)	Indicates A/D Converter status. When high (Logic "1"), the A/D is busy in a conversion or calibration cycle. Returns high on first read cycle or the beginning of new conversion cycle.
Acquisition Status (Pin 28)	Indicates the status of the inherent T/H function. When high (Logic "1"), the device is acquiring and tracking the analog input signal. Acquisition Status returns low indicating that sufficient time has elapsed since the last conversion and a new conversion can be initiated. The device continues to track until a conversion is initiated.

DIGITAL INPUTS

Pin Designation	Function
Clock Input (Pin 10)	Connect external Master Clock signal (TTL or CMOS level @ 4MHz maximum) or tie to digital ground to activate the internal clock.
Data/Status (Pin 11)	Selects the type of information presented to digital output pins 1-8 during the read operation. When high (Logic "1"), convertered output data is presented to parallel output pins 1-8; when low (Logic "0"), status register is presented to digital outputs.
3-State/Read (Pin 12)	Selects state of digital data output pins 1-8. When high (Logic "1"), data is disabled and parallel output bits are in high-impedance state. When low (Logic "0"), converted data (Data/Status, pin 11=Logic "1") or status information (Data/Status, pin 11=Logic "0") is presented to output pins 1-8. Converted output data is presented in two 8-bit bytes. The first read cycle (initiated when 3-State/Read =Logic "0") after a conversion is complete enables the MSB data byte. Toggling 3-State/Read (that is bringing it high and then low again) enables the LSB data byte. The MSB and LSB data bytes will toggle on subsequent read operations. Additionally, falling edges latch the state of Background Calibration.

Pin Designation	Function
Bipolar/$\overline{\text{Unipolar}}$ (Pin 13)	Selects either unipolar or bipolar operation. When high (Logic "1"), the analog input range is bipolar (−Full Scale to +Full Scale). When low (Logic "0"), the analog input range is unipolar (0V to +Full Scale). The analog input voltage pins select the desired full scale range.
Reset (Pin 22)	Controls the device clear and calibration cycle initiation. When brought high, the internal logic is cleared. When returned low (after being high for 100nsec minimum) a full device calibration cycle is initiated.
Background Calibration (Pin 23)	Controls the device active calibration mode. When latched low by the falling edge of 3-State/$\overline{\text{Read}}$, the device interleaves conversions and calibration cycles. Full calibration cycle extends over 72,051 conversions at the expense of extended conversion time.
Start Convert (Pin 24)	The falling edge of Start Convert initiates the conversion cycle. Start Convert must remain low for at least one Master Clock cycle plus 50nsec.

MN6400

DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+F.S.	+F.S.	1111 1111 1111 1111
+F.S. −3/2LSB	+F.S. −3/2LSB	1111 1111 1111 111Ø*
+1/2F.S. +1/2LSB	+1/2LSB	1000 0000 0000 000Ø*
+1/2F.S. −1/2LSB	−1/2LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+1/2F.S. −3/2LSB	−3/2LSB	0111 1111 1111 111Ø*
+1/2LSB	−F.S. +1/2LSB	0000 0000 0000 000Ø*
0	−F.S.	0000 0000 0000 0000

CODING NOTES:

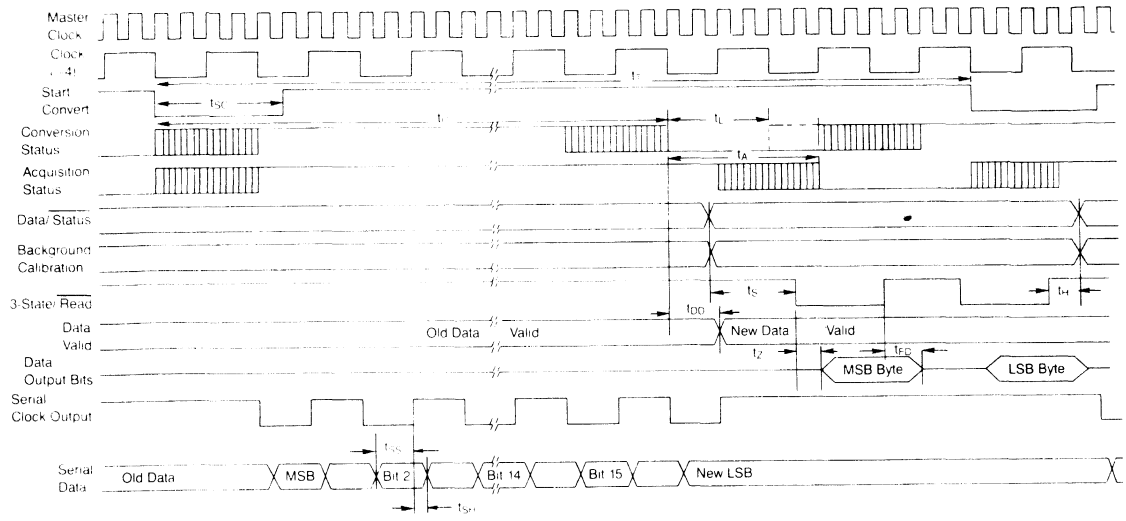
1. For 5 Volt FSR, 1LSB for 16 Bits =76.3μV.
2. For 10 Volt FSR, 1LSB for 16 Bits =152.6μV.
3. For 20 Volt FSR, 1LSB for 16 Bits =305.2μV.
4. For unipolar ranges, the coding is straight binary.
5. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transition indicated. Ideally, with the MN6400 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE			
	0 to +5V	0 to +10V	±5V	±10V
Connect Pin 18 to	Analog Input	Open	Analog Input	Open
Connect Pin 17 to	Open	Analog Input	Open	Analog Input
Connect Pin 13 to Logic	"0"	"0"	"1"	"1"

TIMING DIAGRAM



Notes: 1. Clock (÷4) signal not available. For reference only.
2. Asynchronous mode shown. In synchronous mode, timing uncertainty (, four Master Clock Cycles) is eliminated.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}, $\pm V_{CC} = \pm 15V$, $+V_{DD} = +5V$, $C_L = 50pF$)

PARAMETER	MIN	TYP	MAX	UNITS
Master Clock Frequency (f_{CLK}):				
Internal	2			MHz
External	0.1		4	MHz
Start Convert Pulse Width (t_{SC}) (Note 1)	$1/f_{CLK} + 0.05$		t_C	μsec
Conversion Time (t_C) (Note 1)	$65/f_{CLK}$		$69/f_{CLK} + 0.235$	μsec
Acquisition Time (t_A) (Note 1)			$6/f_{CLK} + 2.25$	μsec
Throughput Time (t_T): (Note 1)				
Synchronous Sampling			$80/f_{CLK}$	μsec
Asynchronous Sampling			$75/f_{CLK} + 2.485$	μsec
Set Up Times (t_S):				
Background Calibration, Data/Status to 3-State/Read Low	20	10		nsec
Hold Times (t_H):				
3-State/Read High to Background Calibration, Data/Status Invalid	50	30		nsec
Data Delay Time (t_{DD})		40	100	nsec
Data Access Time (t_Z):				
3-State/Read Low to Data Valid		80	150	nsec
Output Float Delay (t_{FD}):				
3-State/Read High to Output High Z		80	150	nsec
Set Up Times (t_{SS}):				
Serial Data to Serial Clock Output Rising Edge (Note 1)	$2/f_{CLK} - 0.05$	$2/f_{CLK}$		μsec
Hold Time (t_{SH}):				
Serial Clock Output Rising Edge to Serial Data (Note 1)	$2/f_{CLK} - 0.1$	$2/f_{CLK}$		μsec

Notes. 1. Formulas in the table are for f_{CLK} expressed in MHz.

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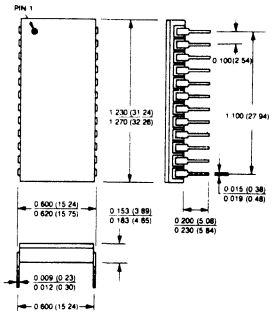
MN6405

50kHz, 16-Bit
SELF-CALIBRATING
SAMPLING A/D CONVERTER

FEATURES

- Self-Calibrating A/D provides True 16-bit Performance
- 50kHz Sampling Rate with Inherent T/H Function
- 16-Bit No-Missing-Codes Guaranteed Over Full Operating Temperature Range
- Complete - Contains:
  - T/H Function
  - Analog Input Buffer
  - Reference
  - Timing and Control Logic
  - μP Interface
- ±1LSB Integral Linearity
- 88dB SNR, −98dB Harmonics
- 740mW Maximum Power Consumption
- Fully specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

24 PIN SIDE-BRAZED DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

The MN6405 is a complete self-calibrating, 16-bit, 50kHz Sampling A/D converter. Each Sampling A/D contains an inherent T/H function, analog input buffer amplifier, reference, timing and control logic circuitry, and microprocessor interface, making it the most complete device of its kind. These Sampling A/D converters are packaged in small, 24-pin, side-brazed, double-wide DIPs. The inherent T/H function allows these devices to accurately sample and digitize dynamically changing analog input signals at rates up to 50kHz. The package, including all of the functions, is smaller than that of most stand-alone 16-bit A/Ds. Each device is fully tested using contemporary FFT (Fast Fourier Transform) technology and guarantees frequency-domain performance — no more guesswork in converting time-domain specifications (linearity, accuracy, etc.) into frequency-domain performance.

The MN6405 offers four analog input voltage ranges (0 to +5V, 0 to +10V, ±5V and ±10V) whose Bipolar and Unipolar operation is digitally controlled. These devices may be operated from the internal clock, or for critical sampling applications, these devices may be operated from a low-jitter crystal clock circuit. Serial output data is provided synchronized to the serial clock output. The device's 3-state outputs enable the MN6405 to connect directly to system data buses.

The MN6405 offers users four electrical performance grades (J,K,S and T models) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C). In addition, S and T models are available with environmental stress screening. Contact factory for availability of fully compliant MIL-H-38534 devices.

MICRO NETWORKS
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MN6405 50kHz 16-Bit SELF-CALIBRATING SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6405 J,K	0°C to +70°C
MN6405 S,T	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 13)	0 to +16.5 Volts
−15V Supply (−V_{CC}, Pin 12)	0 to −16.5 Volts
+5V Supply (+V_{DD}, Pin 20)	−0.3 to +6.0 Volts
Digital Inputs:	
(Pins 9, 10, 18, 19, 21, 22)	−0.3 to +V_{DD} +0.3V
Analog Inputs: 5V (Pin 16)	± V_{CC}
10V (Pin 15)	± V_{CC}

ORDERING INFORMATION

PART NUMBER — MN6405T/B CH

Select suffix J, K, S or T for desired performance and specified temperature range.

Add "/B" suffix to "S" or "T" models for Environmental Stress Screening.

Add "CH" to "S/B" and "T/B" models for MIL-H-38534 compliant devices.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V unless otherwise specified) (Note 10)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V Input		0 to +5		Volts
		−5 to +5		Volts
10V Input		0 to +10		Volts
		−10 to +10		Volts
Input Impedance: 5V Input		5		kΩ
10V Input		10		kΩ
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			±10	μA
Logic "0" (V_{IL} = +0.4V)			±10	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{IH} = −40μA)	+2.4			Volts
Logic "0" (I_{IL} = +1.6mA)			+0.4	Volts
3-State Leakage Current			±10	μA
INTERNAL REFERENCE				
Reference Output: Voltage (Note 11)	+4.45	+4.5	+4.55	Volts
Drift		±3	±10	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supply	±11.4	±15	±16.5	Volts
+V_{DD} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection: +V_{CC} Supply		±.0001	±.001	%FS/%VS
−V_{CC} Supply		±.0001	±.001	%FS/%VS
+V_{DD} Supply		±.0001	±.001	%FS/%VS
Current Drains: +V_{CC} Supply		+5	+10	mA
−V_{CC} Supply		−20	−31	mA
+V_{DD} Supply		+14	+25	mA
Power Consumption		445	740	mW

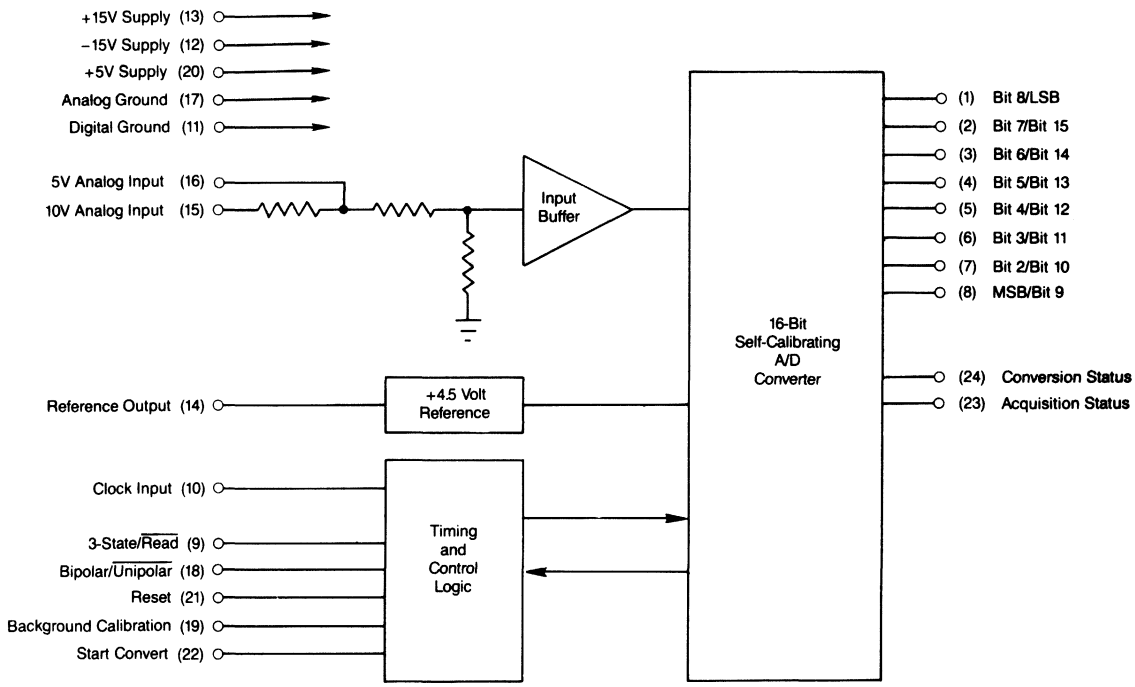
SPECIFICATION NOTES:

1. External Master Clock frequency set to 4MHz, synchronous sampling mode and background calibration disabled.
2. Specification listed applies after calibration at any temperature within the specified temperature range.
3. Specification listed applies over the specified temperature range after initial calibration at 25°C.
4. Specification listed applies after calibration at 25°C.
5. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6405 on a unipolar range.
6. Bipolar zero error is defined as the difference between the ideal and actual input voltage at which the digital output changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6405 on a bipolar range.
7. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale absolute accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scales for bipolar input ranges. Full scale absolute accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0001 to 0000 0000 0000 0000 transition for bipolar input ranges.
8. This parameter represents the rms-to-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full scale analog input sine wave (0dB) at the specified frequencies.
9. This parameter represents the peak-to-peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
10. External Master Clock frequency set to 4MHz and operated in the synchronous sampling mode.
11. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with an 0.1μF capacitor. Reference must not be used for applications circuits without buffering.
12. This parameter's specification limits for bipolar range, 5V input.

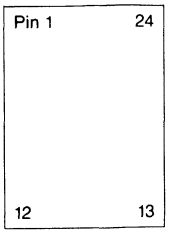
PERFORMANCE SPECIFICATIONS (Typical at +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V unless otherwise indicated) (Note 1)

STATIC CHARACTERISTICS	MN6405J	MN6405K	MN6405S	MN6405T	UNITS
Integral Linearity Error (Max) (Note 2)	±0.0015	±0.0015	±0.0015	±0.0015	%FSR
Integral Linearity Error (Max) (Note 3)	±0.0022	±0.0015	±0.0022	±0.0015	%FSR
Minimum Resolution for Which No Missing Codes is Guaranteed (Note 3)	16	16	16	16	Bits
Unipolar Offset Error (Notes 4, 5)					
Initial (Maximum)	±0.03	±0.02	±0.03	±0.02	%FSR
Drift (Maximum)	±4	±2.5	±4	±2.5	ppm of FSR/°C
Bipolar Zero Error (Notes 4, 6)					
Initial (Maximum)	±0.03	±0.02	±0.03	±0.02	%FSR
Drift (Maximum)	±4	±2.5	±4	±2.5	ppm of FSR/°C
Full Scale Accuracy Error (Notes 4, 7)					
Initial (Maximum)	±0.1	±.05	±0.1	±.05	%FSR
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
DYNAMIC CHARACTERISTICS					
Minimum Guaranteed Sampling Rate	50	50	50	50	kHz
Maximum A/D Conversion Time	16.25	16.25	16.25	16.25	μsec
Signal-to-Noise Ratio (Notes 3, 8, 12):					
Initial (+25°C): 1kHz Full Scale Input	85	88	85	88	dB
12kHz Full Scale Input	81	84	81	84	dB
T_{min} to T_{max}: 1kHz Full Scale Input	83	85	83	85	dB
12kHz Full Scale Input	79	82	79	82	dB
Harmonics and Spurious Noise (Notes 3, 9, 12):					
Initial (+25°C): 1kHz Full Scale Input	−96	−98	−96	−98	dB
12kHz Full Scale Input	−90	−92	−90	−92	dB
T_{min} to T_{max}: 1kHz Full Scale Input	−94	−96	−94	−96	dB
12kHz Full Scale Input	−88	−90	−88	−90	dB

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Bit 8 /LSB
2 Bit 7 /Bit 15
3 Bit 6 /Bit 14
4 Bit 5 /Bit 13
5 Bit 4 /Bit 12
6 Bit 3 /Bit 11
7 Bit 2 /Bit 10
8 MSB/Bit 9
9 3-State/$\overline{\text{Read}}$
10 Clock Input
11 Digital Ground
12 −15V/−12V Supply ($-V_{CC}$)
13 +15V/+12V Supply ($+V_{CC}$)
24 Conversion Status
23 Acquisition Status
22 Start Convert
21 Reset
20 +5V Supply ($+V_{DD}$)
19 Background Calibration
18 Bipolar/$\overline{\text{Unipolar}}$
17 Analog Ground
16 5V Analog Input
15 10V Analog Input
14 Reference Output (+4.5V)

APPLICATION INFORMATION

DESCRIPTION OF OPERATION — The MN6405 is a 16-bit Sampling A/D converter containing an inherent, user-transparent T/H function and features self-calibration and μP-interface logic. Self-calibration and the inherent T/H function enable the MN6405 to accurately sample and digitize dynamically changing analog input signals at a 50kHz throughput rate.

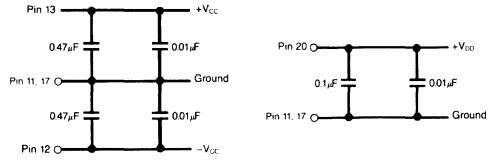
The MN6405 is designed to operate from ±12 or ±15V and +5V power supplies and an external or internally generated Master Clock. After power-up, the MN6405 must be reset by bringing Reset (pin 21) high for a minimum of 100nsec. Bringing Reset high clears the internal logic circuitry while returning Reset low initiates a full calibration cycle. Full calibration cycles require 1,441,020 Master Clock cycles (360.255msec with external 4MHz Master Clock applied). Conversion Status (pin 24) is high during calibration and returns low when complete.

After calibration, conversions can be initiated by the falling edge of Start Convert. The signal applied to Start Convert (pin 22) must remain low for a minimum of one Master Clock cycle plus 50nsec. This translates into 300nsec with the use of an external 4MHz clock. Start Convert must return high prior to the end of the conversion cycle (65 clock cycles, 16.25μsec with 4MHz clock) to allow sufficient acquisition time for the next sample to be converted.

With the conversion complete, output data may be read using various combinations of input control lines. Parallel data is available in two 8-bit bytes. Once a conversion is complete, parallel output data is read by bringing 3-State/$\overline{\text{Read}}$ low. MSB-byte data (MSB-bit 8) is first to be presented to data output lines (pins 1-8). Toggling 3-State/$\overline{\text{Read}}$ (that is, to bring it high and then low again) presents LSB-byte data. Output data lines are in the high-impedance state when 3-State/$\overline{\text{Read}}$ is high.

POWER SUPPLIES AND LAYOUT — The MN6405 is powered from standard supply voltages of +12/15V (pin 13), −12/15V (pin 12) and +5V (pin 20). The analog ground (pin 17) and digital ground (pin 11) are separated to minimize analog and digital circuit interaction. The analog ground is internally used as a reference point, therefore it should be used as the system analog ground reference point. Care must be taken to reduce the system noise to a level below the MN6405's high-resolution conversion capability.

It is recommended that the power supplies be decoupled in the following manner. The +12/15V and −12/15V supplies should be bypassed with a 0.01 μF capacitor in parallel with a 0.47 μF capacitor to analog ground. The +5V supply, which powers both analog and digital internal circuitry, should be bypassed with a 0.1 μF capacitor in parallel with a 0.01 μF capacitor to analog ground. The optimum value decoupling capacitors to use may vary depending on the user's system noise characteristics.



DEVICE CALIBRATION — The MN6405 features two user-controlled self-calibration modes of operation. Self-calibration insures optimum performance at any temperature and at any time throughout the lifetime of the device. Self-calibration also eliminates the need for additional external circuitry to maintain operation of the device within specification.

The first mode of calibration is called reset, and its initiation is controlled with Reset (pin 21). A reset calibration must be performed after the device is powered-up, and can be repeated optionally after the device reaches its operating temperature. The required initial reset is initiated by strobing the Reset pin high for a minimum of 100 nsec. When Reset is brought high, internal logic clears. When Reset returns low, a single full calibration lasting 1,441,020 master clock cycles begins (360.255 msec w/ 4 MHz clock). During reset the Conversion Status (pin 24) output will be in a high state, and will fall low upon completion of calibration.

The reset mode of calibration can be initiated by either hardware using a power-up reset circuit or by software in microprocessor control applications.

The second mode of calibration is called background calibration, which is activated by either tying Background Calibration (pin 19) to digital ground or bringing Background Calibration and 3-State/$\overline{\text{Read}}$ (pin 9) both low. This mode differs from reset calibration in that a fractional portion of the total calibration time is added to the end of each conversion. After 72,051 conversions, the calibration cycle is complete. The conversion time of the device when background calibration is active is extended by 20 master clock cycles (5μsec w/4 MHz clock). Except for the decrease in throughput rate, the background calibration mode is transparent to the user.

MASTER CLOCK — The MN6405 operates from a master clock that can be supplied externally or generated internally depending upon the signal applied to Clock Input (pin 10). A logic low on this pin will activate the 2 MHz minimum internal clock. Optionally, the user can supply a TTL or CMOS system clock with a maximum frequency of 4MHz (100kHz minimum) to the Clock Input. All device timing characteristics scale to the master clock frequency. The internal oscillator exhibits relatively high jitter compared to crystal oscillators, which may affect performance in some sampling applications.

INITIATING CONVERSIONS — A falling edge on the Start Convert (pin 22) digital input will set the device into the hold mode and initiate a conversion cycle. The Start Convert input must remain low for a minimum of one master clock cycle plus 50 nsec (300 nsec w/4 MHz clock). It must return high before the minimum conversion time of 65 clock cycles (16.25μsec w/4 MHz clock) to allow sufficient time for acquisition of the next sample.

T/H ACQUISITION — The MN6405 is a sampling A/D converter, therefore it requires a finite amount of time to accurately acquire an analog input signal before performing a conversion. At the completion of a conversion, signalled by the falling of Conversion Status (pin 24), the device automatically enters the acquisition mode and begins to track the analog input. A minimum acquisition time of six master clock cycles plus 2.25μsec (3.75μsec w/4 MHz clock) is required to acquire the input signal. When sufficient time has elapsed after a conversion for the acquisition of the input signal, the Acquisition Status (pin 23) output will fall low. It returns high on initiation of a new conversion cycle. When driving the MN6405 from a high source impedance, the necessary acquisition time should be extended to allow for the resultant increase in the input settling time constant.

The MN6405's acquisition circuitry operates from a delayed and divided down internal clock frequency of ¼ times the master clock. If sampling is not synchronized to this internal clock, a sample will be synchronously taken but may not be converted until up to four master clock cycles later (1μsec w/ 4 MHz clock). In other words, when Start Convert goes low and is not synchronous with the internal clock, a maximum of four master clock cycles may occur before Conversion Status goes high. This asynchronous uncertainty adds these four master clock cycles plus 235 nsec of internal clock delay (1.235μsec w/4 MHz clock) to the conversion time.

When performing an asynchronous sampling operation, the device can operate at 69 master clock cycles plus 235 nsec for conversion and six master clock cycles plus 2.25 μsec for acquisition for a total of 75 master clock cycles plus 2.485μsec (21.235μsec w/4 MHz clock). This corresponds to a 47.1 kHz maximum throughput rate. Although the sample is asynchronously converted, the sample itself is taken synchronously upon the falling edge of Start Convert. This is particularly important to users in DSP applications.

To synchronize the sampling operation to the internal clock, the Acquisition Status (pin 23) output can be connected to the Start Convert (pin 22) input. The Acquisition Status output is synchronized to the internal clock, thereby eliminating the sampling uncertainty and enabling device operation at 65 master clock cycles for conversion and 15 master clock cycles for acquisition for a total of 80 master clock cycles (20μsec w/4 MHz clock). This corresponds to a 50kHz maximum throughput rate.

ANALOG INPUTS — The MN6405 can be operated in four user-selectable input voltage range configurations. They are 0 to +5V, ±5V, 0 to +10V and ± 10V. The 5V Analog Input (pin 16) is used for 5V full scale analog inputs, and the 10V Analog Input (pin 15) is used for 10V full scale analog inputs. Selection of a unipolar or bipolar input transfer function is made with the Bipolar/$\overline{\text{Unipolar}}$ digital input (pin 18). A logic high on this pin selects a bipolar transfer function of analog input voltage between –Full Scale and +Full Scale. A logic low on this pin selects a unipolar transfer function of analog input voltages between 0V and +Full Scale.

The unipolar voltage ranges are digitally represented at the output in Straight Binary format. An all zero's output corresponds to 0V at the input, and an all ones output corresponds to +FS range voltage at the input. The bipolar voltage ranges produce digital outputs in Offset Binary format. An all zeros output corresponds to an analog input voltage of –Full Scale Range.

The MN6405 contains an input buffer configured to condition the analog input signal for optimum acquisition and conversion performance. Additional signal-conditioning circuitry meeting 16 bit performance levels can be used to drive the analog inputs.

REFERENCE OUTPUT — The MN6405 contains an internal +4.5V low drift precision reference. This reference voltage appears at Reference Output (pin 14) to allow for the attachment of a 0.1μF capacitor in parallel with a 10μF tantalum capacitor. These capacitors are required to allow the reference to exhibit a low output impedance throughout the frequency range of device operation. The optimum value for these capacitors will vary depending on the master clock frequency being used.

It is recommended not to use the Reference Output pin for any additional circuitry requirements. If absolutely necessary, the Reference Output can be buffered and used to fulfill additional circuitry requirements.

DIGITAL OUTPUTS — The MN6405 supplies converted parallel data in an 8-bit MSB/LSB byte format. Converted data appears on the bus in parallel MSB/LSB byte format. A read operation is executed by bringing the 3-State/$\overline{\text{Read}}$ (pin 9) input low. The first read operation following a conversion will bring the bus out of the 3-state condition and present the eight MSBs (MSBs on pin 8 through bit 8 on pin 1). On the second read operation following a conversion, executed by bringing 3-State/$\overline{\text{Read}}$ back high and then low again, the eight LSBs will be presented (Bit 9 on pin 8 through LSB on pin 1). On subsequent reads before the next conversion is complete, the MSB/LSB byte will toggle. Data is valid after a delay of 100 nsec from the falling edge of Conversion Status, and remains valid until the next Conversion Status falling edge.

The Conversion Status (pin 24) and Acquisition Status (pin 23) outputs provide the user with device status information detailed in the Pin Description Section. Conversion Status will remain low for four master clock cycles if 3-State/$\overline{\text{Read}}$ is held low. These status outputs and clock output are not 3-stateable.

PIN DESCRIPTION

POWER SUPPLY CONNECTIONS

Pin Designation	Function
+15V/+12V Supply ($+V_{CC}$, Pin 13)	Positive analog power supply. Devices will operate from nominal +12V or +15V supplies.
−15V/−12V Supply ($-V_{CC}$, Pin 12)	Negative analog power supply. Devices will operate from nominal −12V or −15V supplies.
+5V Supply ($+V_{DD}$, Pin 20)	Positive digital and analog power supply. Device operates from nominal +5V.

ANALOG INPUTS

Pin Designation	Function
10V Analog Input (Pin 15)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +10V analog input signals. When in Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±10V analog input signals.
5V Analog Input (Pin 16)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +5V analog input signals. When in the Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±5V analog input signals.

ANALOG OUTPUTS

Pin Designation	Function
Reference Output (Pin 14)	Provides reference voltage of +4.5V to be bypassed to Analog Ground with an external 10μF tantalum capacitor in parallel with a 0.1μF ceramic disk capacitor. Use of this reference in additional circuit applications requires the use of an external, low-input-current buffer amplifier.

DIGITAL OUTPUTS

Pin Designation	Function
Parallel Data Outputs (Pins 1-8)	3-stated output byte offers converted data in MSB-byte, LSB-byte format. $\overline{\text{Data}}$ Output is controlled by 3-State/$\overline{\text{Read}}$ input.
Conversion Status (Pin 24)	Indicates A/D Converter status. When high (Logic "1"), the A/D is busy in a conversion or calibration cycle. Returns high on first read cycle or the beginning of new conversion cycle.
Acquisition Status (Pin 23)	Indicates the status of the inherent T/H function. When high (Logic "1"), the device is acquiring and tracking the analog input signal. Acquisition Status returns low indicating that sufficient time has elapsed since the last conversion and a new conversion can be initiated. The device continues to track until a conversion is initiated.

ITAL INPUTS

n Designation	Function
ock Input (Pin 10)	Connect external Master Clock signal (TTL or CMOS level @ 4MHz maximum) or tie to digital ground to activate the internal clock.
State/$\overline{\text{Read}}$ (Pin 9)	Selects state of digital data output pins 1-8. When high (Logic "1"), data is disabled and parallel output bits are in high-impedance state. When low (Logic "0"), converted data is presented to output pins 1-8. Converted output data is presented in two 8-bit bytes. The first read cycle (initiated when 3-State/$\overline{\text{Read}}$ =Logic "0") after a conversion is complete enables the MSB data byte. Toggling 3-State/$\overline{\text{Read}}$ (that is, bringing it high and then low again) enables the LSB data byte. The MSB and LSB data bytes will toggle on subsequent read operations. Additionally, falling edges latch the state of Background Calibration.

Pin Designation	Function
Bipolar/$\overline{\text{Unipolar}}$ (Pin 18)	Selects either unipolar or bipolar operation. When high (Logic "1"), the analog input range is bipolar (−Full Scale to +Full Scale). When low (Logic "0"), the analog input range is unipolar (0V to +Full Scale). The analog input voltage pins select the desired full scale range.
Reset (Pin 21)	Controls the device clear and calibration cycle initiation. When brought high, the internal logic is cleared. When returned low (after being high for 100nsec minimum) a full device calibration cycle is initiated.
Background Calibration (Pin 19)	Controls the device active calibration mode. When latched low by the falling edge of 3-State/$\overline{\text{Read}}$, the device interleaves conversions and calibration cycles. Full calibration cycle extends over 72,051 conversions at the expense of extended conversion time.
Start Convert (Pin 22)	The falling edge of Start Convert initiates the conversion cycle. Start Convert must remain low for at least one Master Clock cycle plus 50nsec.

MN6405

ITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+F.S.	+F.S.	1111 1111 1111 1111
+F.S. −3/2LSB	+F.S. −3/2LSB	1111 1111 1111 111Ø*
+1/2F.S. +1/2LSB	+1/2LSB	1000 0000 0000 000Ø*
+1/2F.S. −1/2LSB	−1/2LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+1/2F.S. −3/2LSB	−3/2LSB	0111 1111 1111 111Ø*
+1/2LSB	−F.S. +1/2LSB	0000 0000 0000 000Ø*
0	−F.S.	0000 0000 0000 0000

ING NOTES:

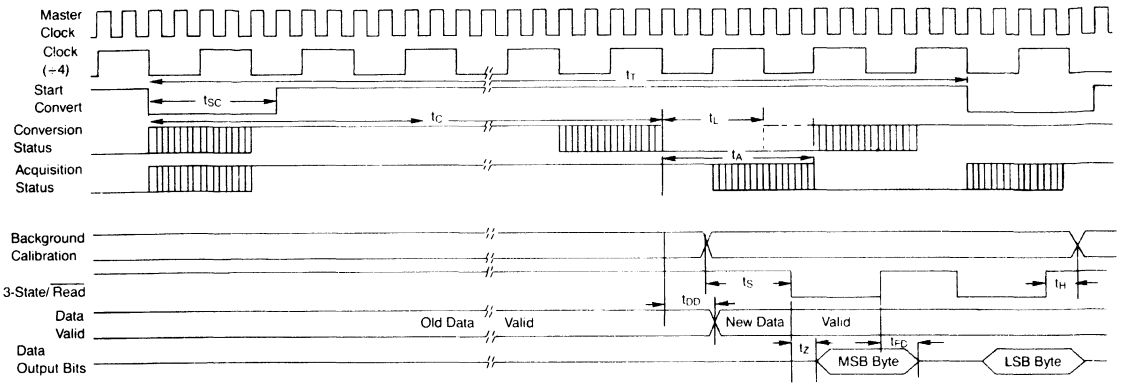
- 5 Volt FSR, 1LSB for 16 Bits =76.3μV.
- 10 Volt FSR, 1LSB for 16 Bits =152.6μV.
- 20 Volt FSR, 1LSB for 16 Bits =305.6μV.
- unipolar ranges, the coding is straight binary.
- bipolar ranges, the coding is offset binary.

og voltages listed are the theoretical values for the transition indicated. Ideally, with IN6405 continuously converting, the output bits indicated as Ø will change from a) a "0" or vice versa as the input voltage passes through the level indicated.

PUT RANGE SELECTION

I CONNECTIONS	ANALOG INPUT VOLTAGE RANGE			
	0 to +5V	0 to +10V	±5V	±10V
nnect Pin 16 to	Analog Input	Open	Analog Input	Open
nnect Pin 15 to	Open	Analog Input	Open	Analog Input
nnect Pin 18 to Logic	"0"	"0"	"1"	"1"

TIMING DIAGRAM



Note: 1. Clock (÷4) signal not available, for reference only.
2. Asynchronous mode shown. In synchronous mode, timing uncertainty (, four Master Clock Cycles) is eliminated.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}, $\pm V_{CC} = \pm 15V$, $+V_{DD} = +5V$, $C_L = 50pF$)

PARAMETER	MIN	TYP	MAX	UNITS
Master Clock Frequency (f_{CLK}): Internal External	 2 0.1		 4	 MHz MHz
Start Convert Pulse Width (t_{SC}) (Note 1)	$1/f_{CLK} + 0.050$		t_C	μsec
Conversion Time (t_C) (Note 1)	$65/f_{CLK}$		$69/f_{CLK} + 0.235$	μsec
Acquisition Time (t_A) (Note 1)			$6/f_{CLK} + 2.25$	μsec
Throughput Time (t_T): (Note 1) Synchronous Sampling Asynchronous Sampling			 $80/f_{CLK}$ $75/f_{CLK} + 2.485$	 μsec μsec
Set Up Times (t_S): Background Calibration to 3-State/$\overline{\text{Read}}$ Low	20	10		nsec
Hold Times (t_H): 3-State/$\overline{\text{Read}}$ High to Background Calibration	50	30		nsec
Data Delay Time (t_{DD})		40	100	nsec
Data Access Time (t_Z): 3-State/$\overline{\text{Read}}$ Low to Data Valid		80	150	nsec
Output Float Delay (t_{FD}): 3-State/$\overline{\text{Read}}$ High to Output High Z		80	150	nsec

Notes: 1. Formulas in the table are for f_{CLK} expressed in MHz.

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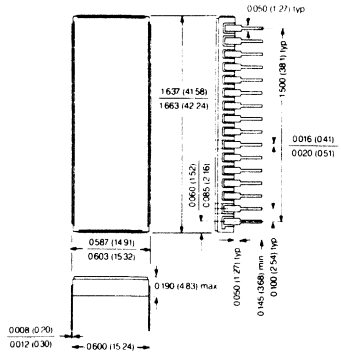
MN6450

47kHz, 16-Bit
SELF-CALIBRATING
SAMPLING A/D CONVERTER

FEATURES

- **Self-Calibrating A/D Provides True 16-Bit Performance**
- **47kHz Sampling Rate with Inherent T/H Function**
- **16-Bit No-Missing-Codes Guaranteed Over Full Operating Temperature Range**
- **Complete - Contains:**
  - **T/H Function**
  - **Analog Input Buffer**
  - **Reference**
  - **μP Interface**
  - **Full 16-Bit Parallel Output**
  - **Output Bus Driver**
- **±1LSB Integral Linearity**
- **88dB SNR, −98dB Harmonics**
- **740mW Maximum Power Consumption**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

32-PIN SIDE-BRAZED DIP



DESCRIPTION

The MN6450 is a complete 16-bit sampling A/D converter capable of converting analog signals into digital words at a 47kHz rate. Each device contains an inherent sampling function, analog input buffer amplifier, reference, microprocessor interface and a 16-bit-wide parallel data bus driver.

The inherent sampling function associated with the A/D converter's architecture allows changing input signals (up to 12kHz) to be digitized without the need for an external T/H amplifier. Self-calibration accounts for the device's ±0.0015%FSR integral linearity and 16-bit no-missing-code performance. In addition to static performance characteristics, the MN6450 is also specified for dynamic applications with frequency domain specifications including 88dB signal-to-noise ratio and -98dB harmonics.

The MN6450 is packaged in a small 32-pin, hermetically sealed, double-wide, side-brazed DIP package. Designers can select from four electrical grades (J,K,S and T) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C). In addition, S and T models are available environmentally stress screened or fully compliant with MIL-H-38534. Contact factory for availability of "CH" types.

APPLICATIONS

Test and Measurement	Weights and Measures
P.C.-Based Data Acquisition	Robotics and Motion Control
Geophysical/Seismic	Fire and Control Systems
Systems ATE	Analyzers

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MN6450 47kHz 16-Bit SELF-CALIBRATING SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	–55°C to +125°C
Specified Temperature Range	
MN6450J, K	0°C to +70°C
MN6450S, T	–55°C to +125°C
Storage Temperature Range	–65°C to 150°C
+15V Supply (+V_{CC}, Pin 17)	0 to +16.5 Volts
–15V Supply (-V_{CC}, Pin 20)	0 to -16.5 Volts
+5V Supply (+V_{DD}, Pin 32)	–0.3 to +6 Volts
Digital Inputs (Pins 18, 19, 25, 26, 27, 28, 29)	–0.3 to +V_{DD} + 0.3V
Analog Inputs: 5V (Pin 22)	±V_{CC}
10V (Pin 21)	±V_{CC}

ORDERING INFORMANTION

PART NUMBER — MN6450T/B CH

Select suffix J, K, S or T for desired performance and specified temperature range.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS (T_A = +25°C, ± V_{CC} = ± 15V, +V_{DD} = +5V unless otherwise specified) (Note 10)

ANALOG INPUTS		MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges:	5V Input		0 to +5		Volts
			–5 to +5		Volts
	10V Input		0 to +10		Volts
			–10 to +10		Volts
Input Impedance:	5V Input		5		kΩ
	10V Input		10		kΩ
DIGITAL INPUTS					
Logic Levels:	Logic "1"	+2.0			Volts
	Logic "0"			+0.8	Volts
Logic Currents:	Logic "1" (V_{IH} = +2.4V)			±10	µA
	Logic "0" (V_{IL} = +0.4V)			±10	µA
DIGITAL OUTPUTS					
Logic Levels (Note 12):	Logic "1" (I_{OH} = –6.0mA)	+3.9			Volts
	Logic "0" (I_{OL} = +6.0mA)			+0.26	Volts
Logic Levels (Note 13):	Logic "1" (I_{OH} = 40µA)	+2.4			Volts
	Logic "0" (I_{OL} = 1.6mA)			+0.4	Volts
3-State Leakage Current				±10	µA
INTERNAL REFERENCE					
Reference Output:	Voltage (Note 11)	+4.45	+4.5	+4.55	Volts
	Drift		±3	±10	ppm/°C
POWER SUPPLY REQUIREMENTS					
Power Supply Range:	±V_{CC} Supply	±11.4	±15	±16.5	Volts
	+V_{DD} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection:	+V_{CC} Supply		±.0001	±.001	%FS/%VS
	–V_{CC} Supply		±.0001	±.001	%FS/%VS
	+V_{DD} Supply		±.0001	±.001	%FS/%VS
Current Drains:	+V_{CC} Supply		+5	+10	mA
	–V_{CC} Supply		–20	–31	mA
	+V_{DD} Supply		+14	+25	mA
Power Consumption			445	740	mW

SPECIFICATION NOTES:

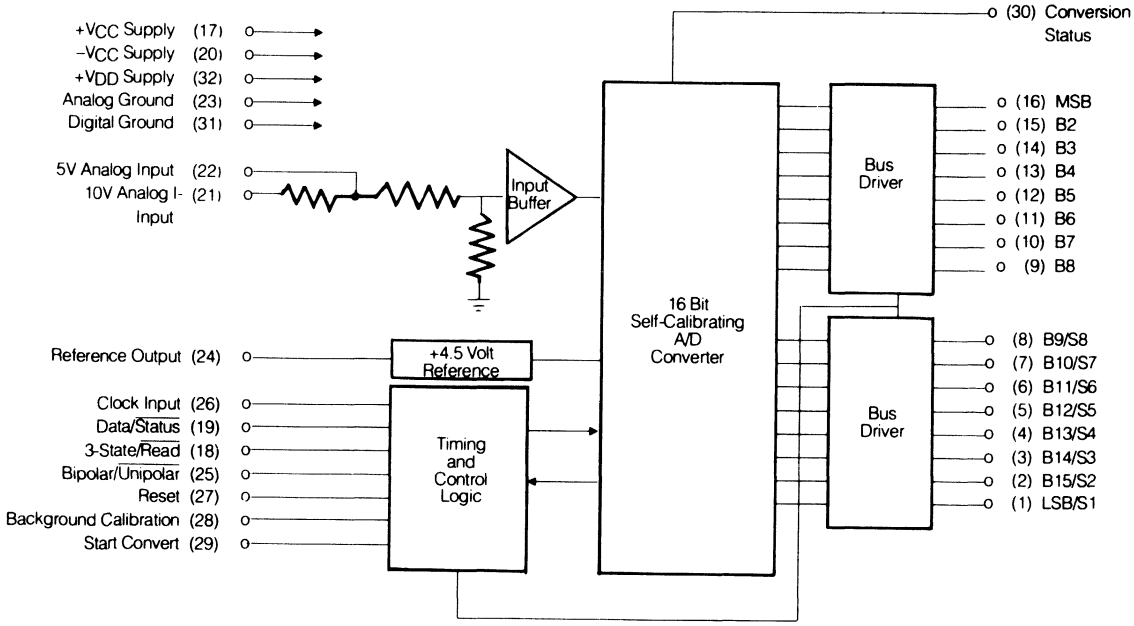
1. External Master Clock frequency set to 4MHz and background calibration disabled.
2. Specification listed applies after calibration at any temperature within the specified temperature range.
3. Specification listed applies over the specified temperature range after initial calibration at 25°C.
4. Specification listed applies after calibration at 25°C.
5. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6450 on a unipolar range.
6. Bipolar zero error is defined as the difference between the ideal and actual input voltage at which the digital output changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6450 on a bipolar range.
7. Full scale absolute accuracy error includes offset, gain linearity, noise and all other errors. Full scale absolute accuracy specifications apply at postive full scale for unipolar input ranges and at both positive and negative full scales for bipolar input ranges. Full scale absolute accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0001 to 0000 0000 0000 0000 transition for bipolar input ranges.
8. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full scale analog input sine wave (0dB) at the specified frequencies.
9. This parameter represents the peak-to-peak non-fundamental component (harmonic or spurious, inband or out-of-band) in the output spectrum.
10. External Master Clock frequency set to 4MHz.
11. Reference output is to be bypassed to Analog Ground with a 10µF capacitor in parallel with an 0.1µF capacitor. Reference must not be used for applications circuits without buffering.
12. For all digital outputs except Conversion Status.
13. Specification for Conversion Status Only.

PERFORMANCE SPECIFICATIONS (Typical at +25°C, $\pm V_{CC}$=±15V, $+V_{DD}$=+5V unless otherwise indicated)(Note 1)

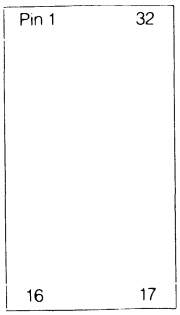
STATIC CHARACTERISTICS	MN6450J	MN6450K	MN6450S	MN6450T	UNITS
Integral Linearity Error (Max) (Note2)	±0.0015	±0.0015	±0.0015	±0.0015	%FSR
Integral Linearity Error (Max) (Note 3)	±0.0022	±0.0015	±0.0022	±0.0015	%FSR
Minimum Resolution for Which No Missing Codes is Guaranteed (Note 3)	16	16	16	16	Bits
Unipolar Offset Error (Notes 4, 5)					
Initial (Maximum)	±0.03	±0.02	±0.03	±0.02	%FSR
Drift (Maximum)	±4	±2.5	±4	±2.5	ppm of FSR/°C
Bipolar Zero Error (Notes 4, 6)					
Initial (Maximum)	±0.03	±0.02	±0.03	±0.02	%FSR
Drift (Maximum)	±4	±2.5	±4	±2.5	ppm of FSR/°C
Full Scale Accuracy Error s (Notes 4, 7)					
Initial (Maximum)	±0.1	±.05	±0.1	±.05	%FSR
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
DYNAMIC CHARACTERISTICS					
Minimum Guaranteed Sampling Rate	47	47	47	47	kHz
Maximum A/D Conversion Time	16.25	16.25	16.25	16.25	µsec
Signal-to-Noise Ratio (Notes 3, 8):					
Initial (+25°C): 1kHz Full Scale Input	85	88	85	88	dB
12kHz Full Scale Input	81	84	81	84	dB
T_{min} to T_{max}: 1kHz Full Scale Input	83	85	83	85	dB
12kHz Full Scale Input	79	82	79	82	dB
Harmonics and Spurious Noise (Notes 3,9):					
Initial (+25°C): 1kHz Full Scale Input	-96	-98	-96	-98	dB
12kHz Full Scale Input	-90	-92	-90	-92	dB
T_{min} to T_{max}: 1kHz Full Scale Input	-94	-96	-94	-96	dB
12kHz Full Scale Input	-88	-90	-88	-90	dB

MN6450

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Bit 16 (LSB)
2 Bit 15
3 Bit 14
4 Bit 13
5 Bit 12
6 Bit 11
7 Bit 10
8 Bit 9
9 Bit 8
10 Bit 7
11 Bit 6
12 Bit 5
13 Bit 4
14 Bit 3
15 Bit 2
16 Bit 1 (MSB)

32 +5V Supply ($+V_{DD}$)
31 Digital Ground
30 Conversion Status
29 Start Convert
28 Background Calibration
27 Reset
26 Clock Input
25 Bipolar/Unipolar
24 Reference Output
23 Analog Ground
22 5V Analog Input
21 10V Analog Input
20 −15V Supply ($-V_{CC}$)
19 Data/Status
18 3-State/Read
17 +15V Supply ($+V_{CC}$)

APPLICATION INFORMATION

DESCRIPTION OF OPERATION – The MN6450 is a 16-bit, Sampling A/D converter containing an inherent, user-transparent T/H function and features self-calibration and microprocessor interface logic. Self-calibration and the inherent T/H function enable the MN6450 to accurately sample and digitize dynamically changing analog input signals at a 47kHz throughput rate.

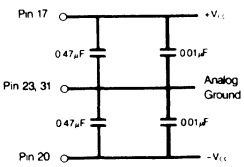
The MN6450 is designed to operate from standard ±12 or ±15V and +5V power supplies and an internal or externally generated Master Clock. After initial power-up, the device must be reset by bringing Reset (pin 27) high for a minimum of 100nsec. Bringing Reset high clears the internal logic circuitry while returning Reset low initiates a full calibration cycle. Full calibration cycles require 1,441,020 Master Clock cycles (360.255msec with an externally applied 4MHz Master Clock). Conversion Status (pin 30) is high during calibration and returns low when calibration is complete.

After calibration, conversions can be initiated by the falling edge of Start Convert (pin 29). The signal applied to Start Convert must remain low for one Master Clock cycle plus 50nsec. This translates to 300nsec with the use of an external 4MHz clock. Start Convert must remain high prior to the end of the conversion cycle (65 clock cycles, 16.25µsec with a 4MHz external clock) to allow sufficient acquisition of the next analog signal to be converted.

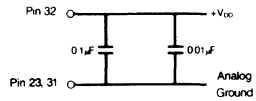
With the conversion complete, digital output data and device status information can be read using various combinations of the digital input control lines. Parallel data is available in a single 16-bit-wide word and is read by bringing 3-State/Read low. Output data lines are returned to the high-impedance state by bringing 3-State/Read high.

POWER SUPPLIES AND LAYOUT – The MN6450 is powered from standard +12/15V (pin 17), −12/15V (pin 20), and +5V (pin 32) supplies. The analog ground (pin 23) and digital ground (pin 31) pins are not connected together internal to the device to minimize analog and digital circuit interaction. The analog ground connection is used as a signal reference point, therefore it should be used as the system analog reference point. Care should be taken to reduce the system noise to a level below the MN6450's high-resolution conversion capability.

It is recommended, for most applications, that the power supplies to the MN6450 be decoupled in the following manner. The +12/15V and −12/15V supplies should be bypassed with a 0.01µF capacitor in parallel with a 0.47µF capacitor to analog ground. The +5V supply, which powers both analog and digital circuits, should be bypassed with a 0.1µF capacitor in parallel with a 0.01µF capacitor to analog ground. System noise characteristics will actually dictate the optimum combination of bypass capacitors.



Power Supply Decoupling



DEVICE CALIBRATION – The MN6450 features two user-controlled self-calibration modes of operation. Self-calibration insures optimum performance at any temperature and at any time throughout the lifetime of the device. Self-calibration also eliminates the need for additional external circuits to maintain operation of the device within specification.

The first mode of calibration is called reset, and its initiation is controlled via the Reset input (pin 27). The device must be reset after the application of power, and can be repeated at the user's option at any time thereafter to compensate for changes in temperature, etc. The required initial reset is initiated by bringing Reset (pin 27) high for a minimum of 100nsec. When Reset is brought high, all internal calibration logic is cleared. When reset is returned low, a single full calibration cycle lasting 1,441,020 master clock cycles begins (360.225msec with a 4MHz external master clock applied). During reset, the Conversion Status

output (pin 30) will be in a high state, and will fall low upon the completion of the calibration cycle.

The reset mode of calibration can be initiated either by hardware using a power-up reset circuit or by software in microprocessor controlled applications.

In the second mode of operation, calibration can be interleaved with the conversion process. In this mode of calibration the conversion cycle is extended by 20 master clock cycles to accommodate a portion of the calibration process. This mode of calibration is called Background Calibration and is initiated by bringing Background Calibration (pin 28) and 3-State/$\overline{\text{Read}}$ (pin 18) both low. This mode differs from Reset in that a fraction of the calibration process is accomplished at the end of each conversion. After 72,051 conversions, the calibration cycle is complete. Except for the increase in conversion time (and a proportionate decrease in throughput), the background calibration mode is transparent to the user.

MASTER CLOCK – The MN6450 operates from a master clock that can be supplied externally or generated internally depending upon the signal applied to Clock Input (pin 26). A logic low on this pin will activate the 2MHz minimum internal clock. Optionally, the user can supply a TTL or CMOS system clock with a maximum frequency of 4MHz (100kHz minimum) to the clock input. All device timing characteristics scale to the master clock frequency. The internal oscillator exhibits relatively high jitter when compared to crystal oscillators, which may have an adverse affect on performance in some sampling applications.

INITIATING CONVERSIONS – A falling edge on the start convert input will set the device into the hold mode and initiate a conversion cycle. The start convert signal must remain low for a minimum of one master clock cycle plus 50nsec (300nsec total for applications using an applied 4MHz external clock). It must return high before the minimum conversion time of 65 clock cycles (16.25µsec with an applied 4MHz external clock) to allow for sufficient time to acquire the next sample to be digitized.

T/H ACQUISITION – The MN6450 is a sampling A/D converter, therefore it requires a finite amount of time to accurately acquire an analog input signal before performing an A/D conversion. At the end of a conversion cycle, signalled by the falling of Conversion Status (pin 30), the device automatically enters the acquisition mode and begins to track the analog input signal. A minimum of six master clock cycles plus 2.25µsec (3.75µsec with an applied 4MHz external clock) is required to acquire the input signal. When driving the MN6450 from a high impedance, it may be necessary to extend the amount of time allowed for the increase in the input settling time constant.

The MN6450's acquisition circuitry operates from a delayed and divided down internal clock frequency of 1/4 times the Master Clock. If sampling is not synchronized to this internal clock, a sample will be synchronously taken but may not be converted until up to four master clock cycles later (1µsec with an applied 4MHz Master Clock). In other words, when Start Convert is brought low asynchronously with respect to the generated internal master clock a maximum of four clock cycles could pass before Conversion Status returns high and the conversion begins. This asynchronous uncertainty in effect adds these four master clock cycles plus 235nsec of internal clock delay (1.235µsec with applied 4MHz Master Clock) to the conversion time.

When operating the MN6450 in an asynchronous application, the conversion cycle will require 69 master clock cycles plus 235nsec while signal acquisition requires six master clock cycles plus 2.25µsec for a total of 75 master clock cycles plus 2.485µsec (21.325µsec with applied 4MHz Master Clock). This corresponds to a maximum throughput rate of 47.1kHz. Although the sample is converted asynchronously, it is important to note for DSP applications that the sample itself was taken synchronously with the falling edge of Start Convert.

ANALOG INPUTS – The MN6450 can be operated in four user-selectable input voltage range configurations. They are 0 to +5V, ±5V, 0 to +10V and ±10V. The 5V analog input (pin 22) is used for 5V full scale analog inputs (0 to +5V and ±5V) while the 10V input (pin 21) is used for 10V full scale inputs (0 to 10V and ±10V). Selection of either bipolar or unipolar operation is controlled via digital input control line Bipolar/$\overline{\text{Unipolar}}$ (pin 25). A logic "1" on this pin selects a bipolar transfer function while a logic "0" applied to this pin selects a unipolar transfer function.

The unipolar ranges are digitally represented at the digital outputs in Straight Binary format. An all 0's output correspond to 0V applied at the input to the device. Likewise, an all 1's output corresponds to +FS applied to the device input. Bipolar ranges are digitally represented at the digital outputs in Offset Binary format. All 0's at the digital output corresponds to an analog input of –FS while all 1's at the digital output corresponds to +FS.

The MN6450 contains an analog input buffer amplifier configured to condition the analog input signal for optimum acquisition and conversion performance. Additional signal conditioning circuitry meeting 16-bit performance levels can be used to drive the analog input to the device.

REFERENCE OUTPUT – The MN6450 contains an internal +4.5V precision low-drift reference. This reference voltage appears a Reference Output (pin 24) to allow for the attachment of a 0.1µf capacitor in parallel with a 10µF tantalum capacitor. These capacitors are required to allow the reference to exhibit a low output impedance throughout the frequency range of device operation. The optimum value for these capacitors will vary depending on the Master Clock frequency being used.

It is recommended to not use the Reference Output to drive any additional circuit requirements. If absolutely necessary, the Reference Output can be buffered and used to fulfill additional circuit requirements.

DIGITAL OUTPUTS – The MN6450 supplies converted parallel output data in a 16-bit-wide format. Output data is read by bringing digital input 3-State/$\overline{\text{Read}}$ (pin 18) low after a conversion is complete. Data outputs are returned to the high-impedance state when 3-State/$\overline{\text{Read}}$ is returned high.

In addition to digital output data, device status information can be read via the parallel data output bits. The information present on the the 16-bit output bus is controlled via the Data/$\overline{\text{Status}}$ control line (pin 19). When high (logic 1), converted data is presented on digital output lines.

When low (logic 0), The Status Register can be read on bit 16 through bit 9 (pins 1-8). Output bit 1 through bit 8 remain in a high impedance state (pins 9-16). Status bit pin locations appear in the table labled Parallel Output Pin Description.

PARALLEL OUTPUT PIN DESCRIPTION

PIN #	DATA OUTPUT	STATUS BIT	STATUS INFORMATION
1	LSB	S1	Same as Conversion Status (pin 30).
2	Bit 15	S2	Reserved for factory use.
3	Bit 14	S3	Reserved for factory use.
4	Bit 13	S4	Acquisition Status – when low, indicates that sufficient time has been allowed for input signal acquisition.
5	Bit 12	S5	Reserved for factory use.
6	Bit 11	S6	Tracking—high when device is tracking analog input.
7	Bit 10	S7	Converting–high when device is converting analog input.
8	Bit 9	S8	Calibrating –high when device is calibrating.
9	Bit 8	Hi-Z	
10	Bit 7	Hi-Z	
11	Bit 6	Hi-Z	
12	Bit 5	Hi-Z	
13	Bit 4	Hi-Z	
14	Bit 3	Hi-Z	
15	Bit 2	Hi-Z	
16	MSB	Hi-Z	

PIN DESCRIPTION

POWER SUPPLY CONNECTIONS

Pin Designation	Function
+15V/+12V Supply (+V_{CC}, Pin 17)	Positive analog power supply. Devices will operate from nominal +12V or +15V supplies.
–15V/–12V Supply (–V_{CC}, Pin 20)	Negative analog power supply. Devices will operate from nominal –12V or –15V supplies.
+5V Supply (+V_{DD}, Pin 32)	Positive digital and analog power supply. Device operates from nominal +5V.

ANALOG INPUTS

Pin Designation	Function
10V Analog Input (Pin 21)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +10V analog input signals. When in Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±10V analog input signals.
5V Analog Input (Pin 22)	When in the Unipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "0"), accepts 0 to +5V analog input signals. When in the Bipolar mode (Bipolar/$\overline{\text{Unipolar}}$ is set to logic "1"), accepts ±5V analog input signals.

ANALOG OUTPUTS

Pin Designation	Function
Reference Output (Pin 24)	Provides reference voltage of +4.5V to be bypassed to Analog Ground with an external 10µF tantalum capacitor in parallel with an 0.1µF ceramic disk capacitor. Use of this reference in additional circuit applications requires the use of an external, low-input current buffer amplifier.

DIGITAL OUTPUTS

Pin Designation	Function
Parallel Data Outputs (Pins 1-16)	Output data is presented in a 16-bit parallel format and is 3-State controlled via the 3-State/$\overline{\text{Read}}$ input. In addition to output data, the device's status register may be read back on pin 1 through pin 8. Data Output is controlled by 3-State/$\overline{\text{Read}}$ and is dependent on Data/$\overline{\text{Status}}$.
Conversion Status (Pin 30)	Indicates A/D Converter status. When high (Logic "1"), the A/D is busy in a conversion or calibration cycle. Returns high on first read cycle or the beginning of new conversion cycle.

DIGITAL INPUTS

Pin Designation	Function
Clock Input (Pin 26)	Connect external Master Clock signal (TTL or CMOS level @ 4MHz maximum) or tie to digital ground to activate the internal clock.
Data/$\overline{\text{Status}}$ (Pin 19)	Selects the type of information presented to digital output pins 1-8 during the read operation. When high (Logic "1"), converted output data is presented to parallel output pins 1-16, when low (Logic "0"), status register is presented to digital outputs (Pins 1-8).
3-State/$\overline{\text{Read}}$ (Pin 18)	Selects state of digital data output pins 1-16. When high (Logic "1"), data is disabled and parallel output bits are in high-impedance state. When low (Logic "0"), converted data (Data/$\overline{\text{Status}}$ pin 19=Logic "1") or status information (Data/$\overline{\text{Status}}$, pin19=Logic "0") is presented to output pins 1-8. Converted output data is presented in one 16-bit word. Additionally, falling edges latch the state of Background Calibration.

Pin Designation	Function
Bipolar/$\overline{\text{Unipolar}}$ (Pin 25)	Selects either unipolar or bipolar operation. When high (Logic "1"), the analog input range is bipolar (-Full Scale to + Full Scale). When low (Logic "0"), the analog input range is unipolar (0V to +Full Scale). The analog input voltage pins selects the desired full scale range.
Reset (Pin 27)	Controls the device clear and calibration cycle initiation. When brought high, the internal logic is cleared. When returned low (after being high for 100nsec minimum) a full device calibration cycle is initiated.
Background Calibration (Pin 28)	Controls the device active calibration mode. When latched low by the falling edge of 3-State/$\overline{\text{Read}}$, the device interleaves conversions and calibration cycles. Full calibration cycle extends over 72,051 conversions at the expense of extended conversion time.
Start Convert (Pin 29)	The falling edge of Start Convert initiates the conversion cycle. Start Convert must remain low for at least one Master Clock cycle plus 50nsec.

DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT	
UNIPOLAR RANGES	BIPOLAR RANGES	MSB	LSB
+F.S.	+F.S.	1111 1111 1111 1111	
+F.S.-3/2LSB	+F.S.-3/2LSB	1111 1111 1111 111Ø*	
+1/2F.S.+1/2LSB	+1/2LSB	1000 0000 0000 000Ø*	
+1/2F.S.-1/2LSB	-1/2LSB	ØØØØ ØØØØ ØØØØ ØØØØ*	
+1/2F.S.-3/2LSB	-3/2LSB	0111 1111 1111 111Ø*	
+1/2LSB	-F.S.+1/2LSB	0000 0000 0000 000Ø*	
0	-F.S.	0000 0000 0000 0000	

CODING NOTES:

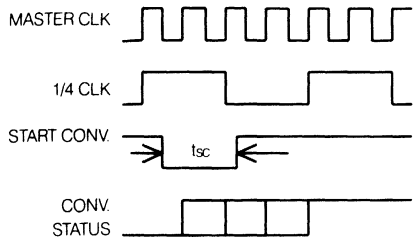
1. For 5 Volt FSR, 1LSB for 16 Bits =76.3μV.
2. For 10 Volt FSR, 1LSB for 16 Bits = 152.6μV.
3. For 20 Volt FSR, 1LSB for 16 Bits =305.6μV.
4. For unipolar ranges, the coding is straight binary.
5. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transition indicated. Ideally, with the MN6450 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

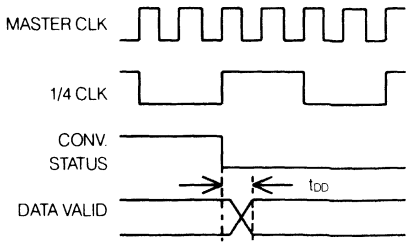
INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE			
	0 to +5V	0 to +10V	±5V	±10V
Connect Pin 22 to	Analog Input	Open	Analog Input	Open
Connect Pin 21 to	Open	Analog Input	Open	Analog Input
Connect Pin 25 to Logic	"0"	"0"	"1"	"1"

INITIATING A CONVERSION:



END OF CONVERSION:



NOTES:

1. 1/4 CLK is shown for reference only. It is generated internally by the device and is used to synchronize all other signals. It is not available as an output.
2. The uncertainty at the rising edge of CONVERSION STATUS is due to the unknown phase relation between START CONV. and 1/4 CLK. CONVERSION STATUS will go high on the first rising edge of 1/4 CLK which occurs after START CONVERT has been recognized as a low. This delay is a maximum of 4 MASTER CLK cycles.
3. The width of CONVERSION STATUS="1" will always be a maximum of 65 MASTER CLK cycles plus 235 nsec regardless of the uncertainty at the rising edge.
4. Although CONVERSION STATUS may not go high for up to 4 MASTER CLK cycles after START CONVERT goes low, the analog input will be held at the value present when START CONVERT goes low.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}, $\pm V_{CC}$, = ± 15V, $+V_{DD}$ = +5V, CL=50pF)

PARAMETER	MIN	TYP	MAX	UNITS
Master Clock Frequency (f_{CLK}) Internal External	 2 0.1		 4	 MHz MHz
Start Convert Pulse Width (t_{SC})	$1/f_{CLK}$ +0.05		t_C	µsec
Conversion Time	$65/f_{CLK}$		$69/f_{CLK}$ +0.235	µsec
Acquisition Time			$6/f_{CLK}$ +2.25	µsec
Throughput Time Asynchronous Sampling			$75/f_{CLK}$ +2.485	µsec
Set Up Times Background Calibration, Data/$\overline{\text{Status}}$ to 3-State/$\overline{\text{Read}}$ Low	20	10		nsec
Hold Times 3-State/$\overline{\text{Read}}$ High to Background Calibration, Data/$\overline{\text{Status}}$ Invalid	50	30		nsec
Data Delay Time (t_{DD})		40	100	nsec
Data Access Time 3-State/$\overline{\text{Read}}$ Low to Data Valid		80	150	nsec
Output Float Delay 3-State/$\overline{\text{Read}}$ High to Output High Z		80	150	nsec

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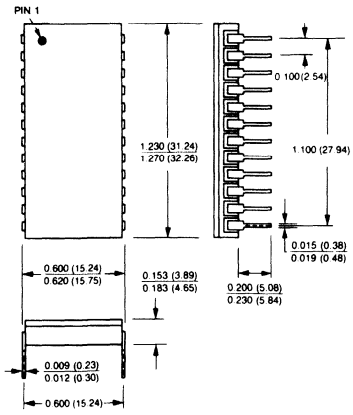
MN6500

16-Bit, 100kHz SAMPLING A/D CONVERTER

FEATURES

- 16-Bit No-Missing Codes
- 100kHz Sampling Rate
- Self Calibration
- Inherent T/H Function
- Serial Output Port
- Small 24-Pin DIP
- Low Power
- Sleep Mode
- Four User-Selectable Input Ranges
- Serial Data Clock Output
- ±12 to 15V, +5V Supplies
- Optional Environmental Stress Screening

24-PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN6500 is a 16-bit, 100kHz Sampling A/D converter complete with internal reference, inherent sampling function and analog input amplifier. Self-calibration ensures ±0.0015%FSR integral linearity error and 16-bits no-missing-codes over the specified temperature range. Output data is provided in a serial format during the conversion or can be clocked from the device upon completing the conversion. Each device is fully tested using contemporary FFT (Fast Fourier Transform) technology guaranteeing frequency-domain performance.

The MN6500 offers four analog input ranges (0 to +5V, 0 to +10V, ±5V and ±10V) whose bipolar and unipolar operation is digitally controlled. Serial output data is provided via the serial output port and can be user configured to allow maximum system flexibility. Serial output clock is also provided to facilitate reading output data.

Packaged in a small 24-pin hermetically-sealed DIP package, the MN6500 only consumes 685mW when operating. While in the sleep mode, power consumption is reduced to 200mW. The MN6500 offers designers four electrical grades (J, K, S, and T) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C). In addition, S and T models are available with Environmental Stress Screening. Contact the factory for availability of fully compliant MIL-H-38534 devices.

APPLICATIONS

Test and Measurement

Weights and Measures

P.C. Based Data Acquisition

Robotics and Motion Control

Geophysical and Seismic

Fire and Control Systems

System ATE

Analyzers

This data sheet contains preliminary information regarding the MN6500. Please contact the factory for up-to-date performance and product information.

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MN6500 100kHz 16-Bit, SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN6500J, K	0°C to +70°C
MN6500S, T	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 23)	0 to +16.5 Volts
−15V Supply (−V_{CC}, Pin 24)	0 to −16.5 Volts
+5V Supply (+V_{DD}, Pin 3)	−0.3 to +6 Volts
Digital Inputs (Pins 5, 6, 8, 9, 12, 15, 16, 17)	−0.5 to +5.5 Volts
Analog Inputs (Pins 18, 19)	±V_{CC}

ORDERING INFORMATION

PART NUMBER — **MN6500 T/B CH**

Select J, K, S or T for desired performance and temperature range.

Add "/B" to "S" and "T" models for Environmental Stress Screening

Add "CH" to "S/B" and "T/B" models for MIL-H-38534 compliant devices.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS ALL UNITS (Typical at T_A = +25°C, ± V_{CC} = ±15V, +V_{DD} = +5V, f_{CLK} = 8MHz (external) unless otherwise indicated) (Note 1)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V		0 to +5, ± 5		Volts
10V		0 to +10, ± 10		Volts
Input Impedance: 5V Input		5		kΩ
10V Input		10		kΩ
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			± 10	μA
Logic "0" (V_{IL} = +0.4V)			± 10	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (V_{OH} = −100uA)	+2.4			Volts
Logic "0" (V_{OL} = +1.6mA)			+0.4	Volts
INTERNAL REFERENCE				
Reference Output: Voltage (Note 2)	+4.45	+4.5	+4.55	Volts
Drift (Note 2)		± 3	± 10	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ± V_{CC} Supply	± 11.4	± 15	± 16.5	Volts
+ V_{DD} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection: ± V_{CC} Supply		± 0.001	± 0.01	%FSR/%VS
+ V_{DD} Supply		± 0.001	± 0.01	%FSR/%VS
Current Drains: +V_{CC} Supply		+27		mA
−V_{CC} Supply		−7		mA
+V_{DD} Supply		+35		mA
Power Consumption		685		mW

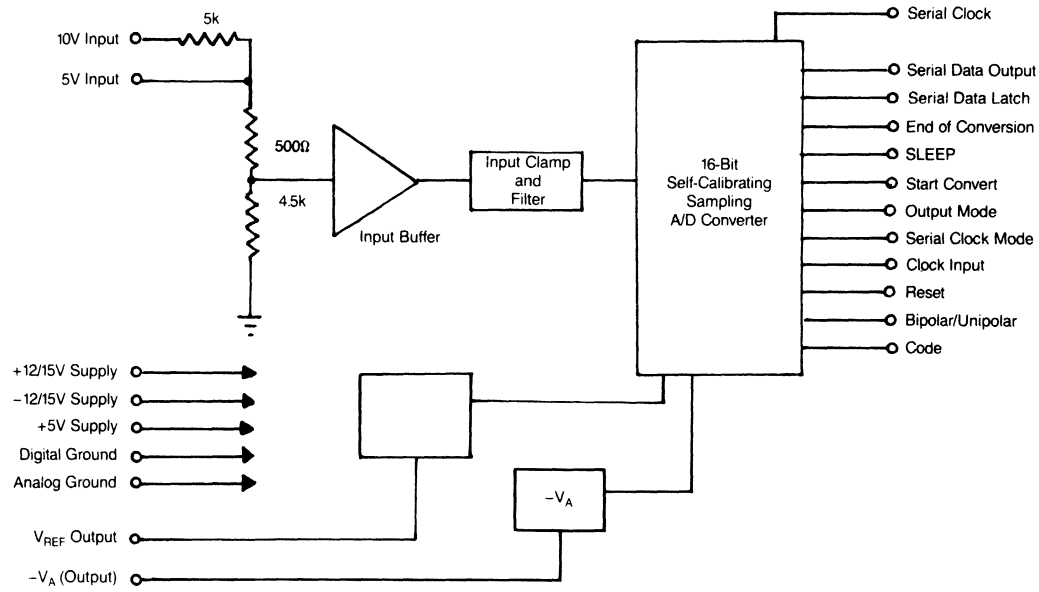
SPECIFICATION NOTES:

1. Specifications apply after calibration following power-up at +25°C.
2. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with a 0.1μF capacitor. Reference must not be used for applications circuitry without buffering.
3. Specification listed applies after calibration at any temperature with specified temperature range.
4. Specification listed applies over the specified temperaure range after initial calibration at 25°C.

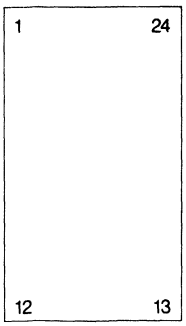
PERFORMANCE CHARACTERISTICS (Typical at T_A = +25°C, ±V_{CC} = +15, +V_{DD} = +5V, f_{CLK} = 8MHz (external) unless otherwise indicated)

STATIC CHARACTERISTICS	MN6500J	MN6500K	MN6500S	MN6500T	UNITS
Integral Linearity Error (Note 3)	±0.0015	±0.0015	±0.0015	±0.0015	%FSR
Integral Linearity Error (Note 4)	±0.0022	±0.0015	±0.0022	±0.0015	%FSR
No Missing Codes	16	16	16	16	Bits
Unipolar Offset Error: Initial	±0.03	±0.02	±0.03	±0.02	%FSR
Drift	±4	±2	±4	±2	ppm of FSR/°C
Bipolar Zero Error: Initial	±0.03	±0.02	±0.03	±0.02	%FSR
Drift	±4	±2	±4	±2	ppm of FSR/°C
Full Scale Accuracy Error: Initial	±0.1	±0.05	±0.1	±0.05	%FSR
Drift	±15	±10	±15	±10	ppm of FSR/°C
DYNAMIC CHARACTERISTIC					
Minimum Sampling Rate	100	100	100	100	kHz
Maximum A/D Conversion Time	8.12	8.12	8.12	8.12	μsec
Signal-to-(Noise+Distortion): f_{AIN} = 1kHz	85	88	85	88	dB
f_{AIN} = 24kHz	81	84	81	84	dB
Harmonics and Spurious Noise: f_{AIN} = 1kHz	−96	−98	−96	−98	dB
f_{AIN} = 24kHz	−94	−96	−94	−96	dB

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Analog Ground
2 Analog Ground
3 +V_A Supply (+5V Analog)
4 Reference Output
5 Serial Clock Mode Input
6 Sleep Input
7 End of Conversion (E.O.C.)
8 Reset
9 Clock Input
10 Digital Ground
11 Serial Data Latch
12 Start Convert
13 Serial Clock
14 Serial Data Output
15 Code Input
16 Data Output Mode Input
17 Bipolar/$\overline{\text{Unipolar}}$
18 10V Analog Input
19 5V Analog Input
20 Analog Ground
21 −V_A Supply (−5V Output)
22 −V_A Supply (−5V Output)
23 +V_{CC} Supply (+15V)
24 −v_{CC} Supply (−15V)

APPLICATIONS INFORMATION

LAYOUT AND GROUNDING CONSIDERATIONS — The MN6500 is powered from standard supply voltages of ± 12/15V and +5V. Analog and digital ground pins are not connected internal to the MN6500. These grounds should be tied together as close to the unit as possible, and connected to system analog ground, preferably through a large, low-impedance ground plane beneath the package. As with all high-resolution, high-speed systems, careful consideration must be given to layout. Analog runs should be isolated from digital lines and power supplies should be decoupled to systems analog ground at the device pins. It is recommended that the +12/15V and −12/15V supply pins be bypassed with a 0.01μF capacitor in parallel with a 0.47μF capacitor to the system analog ground plane.. The +5V supply pin should be bypassed with a 0.1μF capacitor in parallel with a 0.01μF capacitor to the system analog ground plane.

REFERENCE OUTPUT — The MN6500 contains an internal +4.5V low-drift, precision reference. This reference voltage appears at Reference Output to allow for external attachment of a 0.01μF capacitor in parallel with a 10μF tantalum capacitor. These capacitors allow the reference to exhibit low output impedance throughout the frequency range of device operation. The optimum value of these capacitors will vary with the frequency of the Master Clock applied. It is recommended that the Reference Output not be used for any additional system requirements. However, if absolutely necessary, the MN6500 reference output can be buffered for use in additional system applications.

A −5V analog supply is created internal to the MN6500 and brought out to pins 21 and 22 for bypassing. It is recommended that thses pins be bypassed with 0.01μF capacitor in parallel with a 0.47μF capacitor.

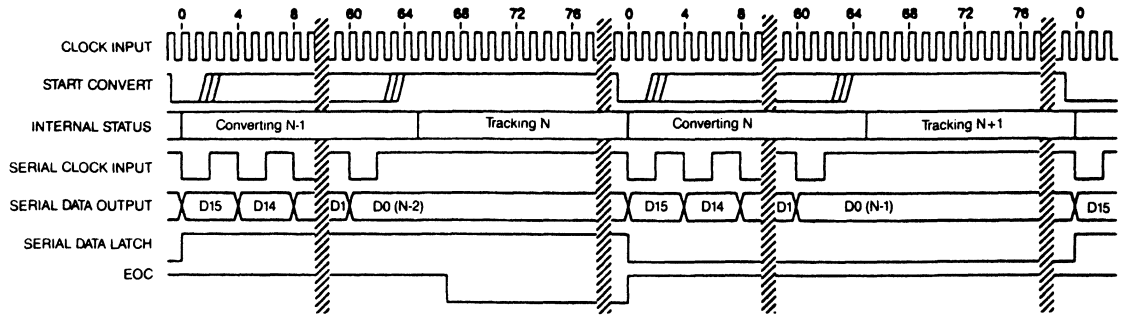
DESCRIPTION OF OPERATION — The MN6500 is a self-calibrating, 100kHz, 16-bit Sampling A/D converter featuring a user-configurable serial data output port. The MN6500 operates from an applied Master Clock and various applied digital input signals. Upon power-up, the MN6500 must be calibrated by resetting the device. The MN6500 features digital control of unipolar or bipolar operation and an output clock for latching valid serial output data.

DIGITAL OUTPUT CODING

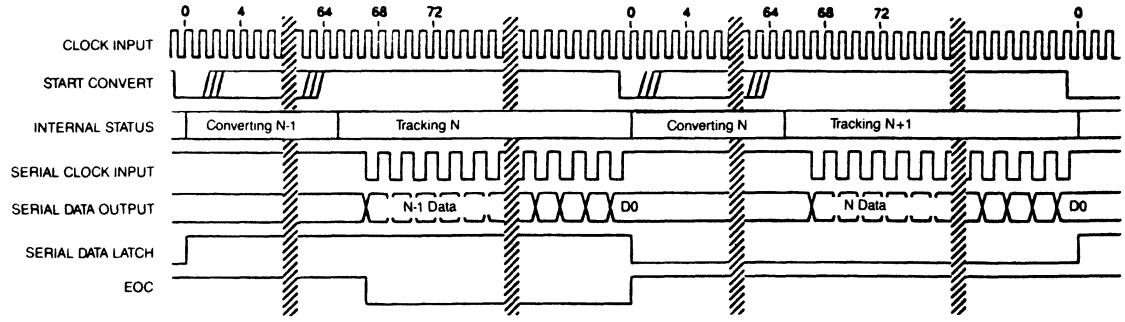
ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGEES	MSB LSB
+F.S.	+F.S.	1111 1111 1111 1111
+F.S. −3/2LSB	+F.S.−3/2LSB	1111 1111 1111 111Ø *
+1/2F.S.+1/2LSB	+1/2LSB	1000 0000 0000 000Ø *
+1/2F.S.−1/2LSB	−1/2LSB	ØØØØ ØØØØ ØØØØ ØØØØ *
+1/2F.S.−3/2LSB	−3/2LSB	0111 1111 1111 111Ø *
+1/2LSB	−F.S.+1/2LSB	0000 0000 0000 000Ø *
0	−F.S.	0000 0000 0000 0000

* Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN6500 continuously converting, the output bits indicated as Ø will change from a logic "1" to a logic "0" or visa versa as the input signal passes through the level indicated.

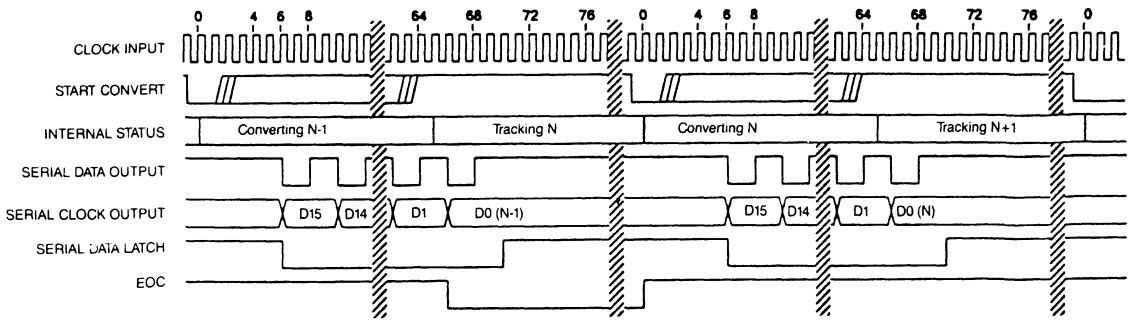
MODE A: PIPELINED DATA TRANSMISSION



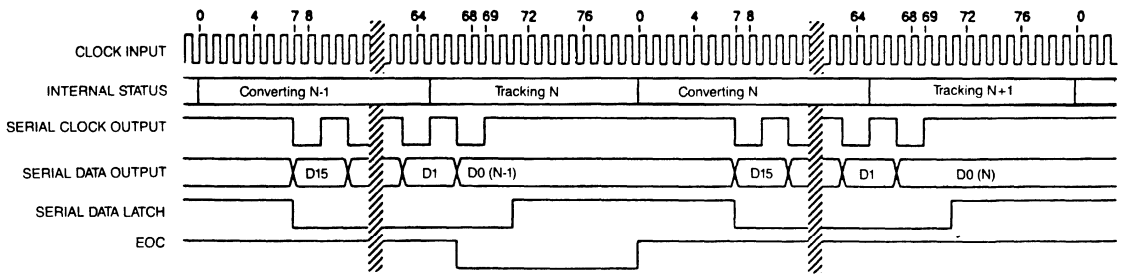
MODE B: REGISTERED BURST TRANSMISSION



MODE C: SYNCHRONOUS SELF-CLOCKING



MODE D: FREE RUN



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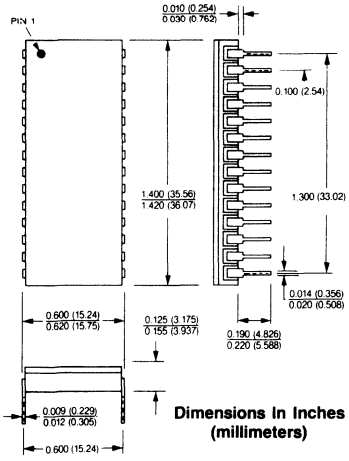
MN6774

100kHz, SAMPLING
12-Bit A/D
CONVERTER

FEATURES

- **100kHz Sampling Rate with Internal T/H Amplifier**
- **50kHz Full-Power Input Bandwidth**
- **70dB Signal-to-Noise Ratio Over Full Bandwidth**
- **Full 8 or 16-Bit μP Interface: CS, CE, R/C, A_0, 12/8, 150nsec Bus Access Time**
- **Industry-Standard MN774 Package and Pinout**
- **895mW Maximum Power**
- **Full Specified 0°C to +70°C (J and K Models) or −55°C to +125μC (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

28-Pin Side Brazed Dip



Dimensions in Inches (millimeters)

DESCRIPTION

The MN6774 is a high-speed (9μsec), μP interfaced (CS, CE, A_0, 12/8, 3-state buffer), 12-bit, successive-approximation type A/D converter with an internal track-hold (T/H) amplifier. The T/H is completely user-transparent and operates totally under the control of the A/D converter. The T/H amplifier enables the A/D to accurately sample and digitize full-scale input signals with frequency components up to 50kHz at sampling rates up to 100kHz. FFT (Fast Fourier Transform) testing using contemporary DSP technology enables these devices to specify and guarantee true dynamic performance characteristics like signal-to-noise ratio (70dB, rms-to-rms), harmonic distortion (−80dB), spurious noise (−80dB) and input-signal full-power bandwidth (50kHz). The need for confusing T/H specifications like aperture delay, aperture jitter, charge injection, etc. has been eliminated.

A/D converters with this configuration and specification techniques are ideally suited for dynamic-digitizing applications in the fields of digital spectrum analysis, voice recognition, vibration analysis, signature recognition and others. The MN6774 is completely self contained with internal T/H, reference, clock, 3-state buffer, and decoding logic and need only be clocked at the desired sampling rates.

The MN6774 is packaged in a small, low-profile, 28-pin, side-brazed, ceramic DIP and has the industry-standard MN574A/674A/774 pinout. Devices are fully specified for 0°C to +70°C (J and K models) or −55°C to +125°C (S and T models) operation.

For military/aerospace or harsh environment commercial/industrial applications, S and T models are available with environmental stress screening. Contact factory for availability of fully compliant MIL-H-38534 devices.

May 1990

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MN6774 100kHz SAMPLING 12-Bit A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6774J, K	0°C to +70°C
MN6774S, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+Vdd +0.5) Volts
Analog Inputs: (Pins 10, 12, 13, 14)	±15 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref. Out (Pin 8) Short Circuit Duration	Continuous to Ground

ORDERING INFORMATION

PART NUMBER — MN6774T/B CH

Select suffix J,K,S or T for desired performance and specified temperature range.

Add "/B" suffix to "S" or "T" models for Environmental Stress Screening.

Add "CH" to "S/B" and "T/B" models for MIL-H-38534 compliant devices.

Contact factory for availability of "CH" devices.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to −10, ±5, ±10		Volts
Input Impedance (Note 16)		3		kΩ
DIGITAL INPUTS CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Loading ($\overline{CS}$, CE, A_0, 12/$\overline{8}$): Logic Currents		±1	±5	μA
Input Capacitance (Note 16)		5		pF
Loading (RI$\overline{C}$): Logic "1" (V_{IH} = +2.4V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−0.4	mA
DIGITAL OUTPUTS DB0-DB11, STS				
Output Coding (Note 2): Unipolar Ranges		CSB		
Bipolar Ranges		COB		
Logic Levels: Logic "1" ($I_{source} \leq 320\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 1.6mA$)			+0.4	Volts
Leakage (DB0-DB11) in High-Z State		±1	±10	μA
Output Capacitance (Note 16)		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10	+10.1	Volts
Drift (Note 16)		±10		ppm/°C
Output Current (Notes 3, 16)			1	mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc Supplies	±14.5	±15	±15.5	Volts
+Vdd Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection (Note 14): +Vcc Supply		±0.01	±0.02	%FSR/%Supply
−Vcc Supply		±0.01	±0.02	%FSR/%Supply
+Vdd Supply		±0.005	±0.01	%FSR/%Supply
Current Drains: +Vcc Supply		+16	+20	mA
−Vcc Supply		−21	−28	mA
+Vdd Supply		+25	−35	mA
Power Consumption		680	895	mW

ORDERING INFORMATION

Part Number	Specified Temperature Range	No Missing Codes	Integral Linearity	Minimum Sampling Rate	Minimum Full Power Bandwidth	SNR	Harmonics
MN6774J	0°C to +70°C	11 Bits	±1LSB	100kHz	50kHz	68dB	−77dB
MN6774K	0°C to +70°C	12 Bits	±½LSB	100kHz	50kHz	70dB	−80dB
MN6774S	−55°C to +125°C	11 Bits	±1LSB	100kHz	50kHz	68dB	−77dB
MN6774S/B (1)	−55°C to +125°C	11 Bits	±1LSB	100kHz	50kHz	68dB	−77dB
MN6774S/B CH (2)	−55°C to +125°C	11 Bits	±1LSB	100kHz	50kHz	68dB	−77dB
MN6774T	−55°C to +125°C	12 Bits	±½LSB	100kHz	50kHz	70dB	−80dB
MN6774T/B (1)	−55°C to +125°C	12 Bits	±½LSB	100kHz	50kHz	70dB	−80dB
MN6774T/B CH (2)	−55°C to +125°C	12 Bits	±½LSB	100kHz	50kHz	70dB	−80dB

1. Includes environmental stress screening.
2. MIL-STD-883, Method 5008 compliant.

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

DYNAMIC CHARACTERISTICS	MN6774J	MN6774K	MN6774S	MN6774T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	100	100	100	100	kHz
Maximum A/D Conversion Time (Note 5)	9	9	9	9	μsec
Signal-to-Noise Ratio (SNR, Note 6):					
Initial (+25°C) (Minimum)	68	70	68	70	dB
T_{min} to T_{max} (Minimum, Note 7)	66	68	66	68	dB
Harmonics and Spurious Noise (Note 8):					
Initial (+25°C) (Minimum)	−77	−80	−77	−80	dB
T_{min} to T_{max} (Minimum, Note 7)	−74	−77	−74	−77	dB
Input Signal Full-Scale Bandwidth (Minimum, Note 9)	50	50	50	50	kHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C) (Maximum)	±1	±½	±1	±½	LSB
T_{min} to T_{max} (Maximum, Note 7)	±1	±½	±1	±1	LSB
Resolution for Which No Missing					
Codes is Guaranteed: Initial (+25°C)	11	12	11	12	Bits
T_{min} to T_{max} (Note 7)	11	12	11	12	Bits
Unipolar Offset Error (Notes 10, 11):					
Initial (+25°C) (Maximum)	±2	±2	±2	±2	LSB
Drift (Maximum)	±10	±5	±10	±5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Notes 7, 15)	±2	±1	±4	±2	LSB
Bipolar Zero Error (Notes 10, 12):					
Initial (+25°C) (Maximum)	±4	±4	±4	±4	LSB
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
Maximum Change to T_{min} to T_{max} (Notes 7, 15)	±3	±2	±6	±4	LSB
Full Scale Accuracy Error (Notes 10, 13):					
Initial (+25°C) (Maximum)	±0.2	±0.1	±0.2	±0.1	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.4	±0.2	±0.7	±0.4	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.2	±0.1	±0.5	±0.3	%FSR
Drift (Maximum)	±50	±25	±50	±25	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±10	±5	±20	±10	LSB

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. See table of transition voltages in section labeled Digital Output Coding.
3. If the internal reference is used to drive an external load, the load should not change during a conversion.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 100kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at higher rates.
5. Whenever Status (pin 28) is low (logic "0"), the internal T/H is in the track mode, and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0dB) at any frequency up to 50kHz.
7. MN6774J, K is fully specified for 0°C to +70°C operation. MN6774S, T is fully specified for −55°C to +125°C operation.
8. This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
9. This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 100kHz rate.
10. Adjustable to zero with external potentiometer.
11. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN6774 on its unipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
12. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN6774 on a bipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding. Listed specs assume fixed 50Ω resistors between Ref Out (pin 8) and Ref In (pin 10) and between Ref Out (pin 8) and Bipolar Offset (pin 12).
13. Full scale accuracy specifications apply at negative full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 to 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB above the nominal negative full scale voltage. The latter ideally occurs ½LSB below the nominal positive full scale voltage. See Digital Output Coding. Listed specs assume fixed 50Ω resistors between Ref Out (pin 8) and Ref In (pin 10) and between Ref Out (pin 8) and Bipolar Offset (pin 12).
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
15. Listed maximum error-over-temperature specifications for unipolar offset, bipolar zero and full scale accuracy correspond to the maximum change from the intial value (+25°C) to the value at T_{min} or T_{max}.
16. These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

CAUTION: These devices are sensitive to electronic discharge.
Proper I.C. handling procedures should be followed.

DESCRIPTION OF OPERATION

The MN6774 is a complete 12-bit Sampling A/D converter. It utilizes the successive approximation conversion technique and contains all required function blocks — successive approximation register (SAR), D/A converter, comparator, clock, reference and T/H amplifier — internal to its package. Internal logic circuitry controls the operational mode of the T/H amplifier. No additional "glue" logic chips are required.

The MN6774 mates directly to most popular 8, 16 and 32-bit microprocessors and contains all the necessary address decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most applications, the MN6774 will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete A/D conversion function. The completeness of this device makes it most convenient to think of the MN6774 as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating the MN6774 under microprocessor control (it also functions as a stand-alone A/D) consists, in most applications, of a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D and involves a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN6774's Status Output (also called Busy Line or End of Conversion (E.O.C.) Line) rises to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Output to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Output or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

If the MN6774 is operated with 12-bit or wider microprocessors, all 12 output bits can be 3-state enabled simultaneously, permitting data collection with a single read operation. If the MN6774 is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's), in a left justified format, with 4 trailing "0's".

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN6774. It is critically important that the MN6774's power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitors should be connected directly from pin 1 to pin 15 (Digital Ground), and the $+V_{CC}$ and $-V_{CC}$ supplies should be decoupled directly to pin 9 (Analog Ground). A suitable decoupling capacitor pair is usually a relatively large tantalum (1 – 10μF) in parallel with a smaller (0.01 – 1.0μF) ceramic disc.

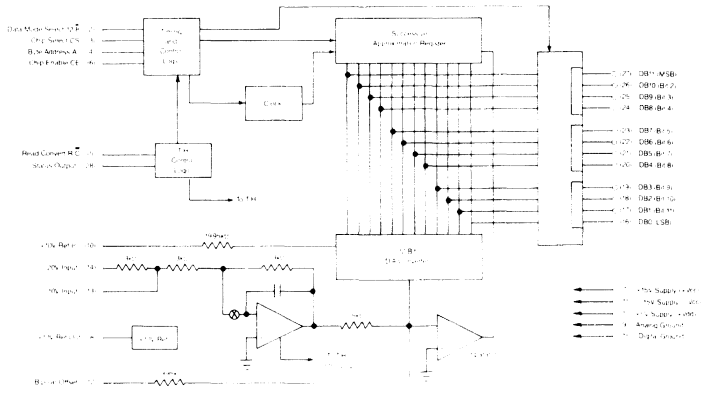
Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN6774 and associated analog input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the MN6774 as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to the MN6774. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for the MN6774's internal reference. It should be connected as close as possible to the analog input signal reference point.

PIN DESIGNATIONS

1	+5V Supply (+Vdd)	28	Status Output
2	Data Mode Select 12/$\overline{8}$	27	DB11 (MSB)
3	Chip Select $\overline{CS}$	26	DB10 (Bit 2)
4	Byte Address A_0	25	DB9 (Bit 3)
5	Read/Convert R/$\overline{C}$	24	DB8 (Bit 4)
6	Chip Enable CE	23	DB7 (Bit 5)
7	+15V Supply (+Vcc)	22	DB6 (Bit 6)
8	+10V Ref Out	21	DB5 (Bit 7)
9	Analog Ground	20	DB4 (Bit 8)
10	+10V Ref In	19	DB3 (Bit 9)
11	–15V Supply (–Vcc)	18	DB2 (Bit 10)
12	Bipolar Offset	17	DB1 (Bit 11)
13	10V Input	16	DB0 (LSB)
14	20V Input	15	Digital Ground

BLOCK DIAGRAM



CONTROL FUNCTIONS — Operating the MN6774 under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN6774 control-line functions. Table 2 is the MN6774 Truth Table.

Unless Chip Enable (CE, pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$ and A_0) will have no effect on MN6774 operation. When CE and $\overline{CS}$ are both asserted, a falling edge applied to R/$\overline{C}$ (Read/Convert, pin 5) initiates a convert operation (R/$\overline{C}$ = "↓").

When initiating a conversion, the signal applied to A_0 (Byte Address/Short Cycle, pin 4) determines whether a 12-bit conversion is initiated (A_0 = "0") or an 8-bit conversion is initiated (A_0 = "1"). It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "↓" and A_0 = "1" or "0" that initiates a convert operation. The actual conversion is initiated by the falling edge of R/$\overline{C}$ as shown in the Truth Table and as described in the section labeled Timing — Initiating Conversions. When initiating conversions, the 12/$\overline{8}$ line is a "don't care".

When reading digital output data from the MN6774, CE and $\overline{CS}$ must be asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine the format of output data. Data will be valid when status is a Logic "0". If the 12/$\overline{8}$ line is a "1", all 12 output data bits will be accessed simultaneously when data is read.

If the 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit bytes as detailed in the section labeled Timing — Reading Output Data. In this situation, A_0 = "0" will result in the 8 MSB's being accessed, and A_0 = "1" will result in the 4 LSB's and 4 trailing zeros being accessed. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled. The 4 LSB's then effectively present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23. See the section labeled Hardwiring to 8-Bit Data Buses.

Table 1: MN6774 Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	1→0 edge must be used to initiate a conversion. Must be high ("1") to read output data.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits) (Note 5)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enalble the MSB's or LSB's as determined by the A_0 line.

Table 2: MN6774 Truth Table

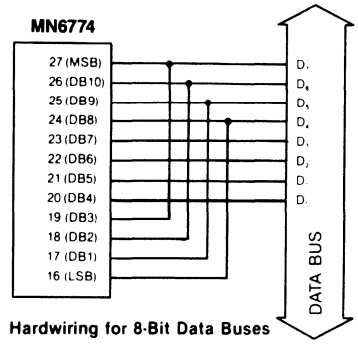
CONTROL INPUTS					MN6774 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1 and TABLE 2 NOTES:

1. "1" indicates TTL logic high (+2.0V minimum).
2. "0" indicates TTL logic zero (+0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicates logic transitions (edges).
5. Some vendors 774's required the 12/$\overline{8}$ line to be hard wired to either +5V (pin 1) or 0V (pin 15). The MN6774 may be hard wired as such or driven with normal TTL signals.
6. Output data format is as follows:

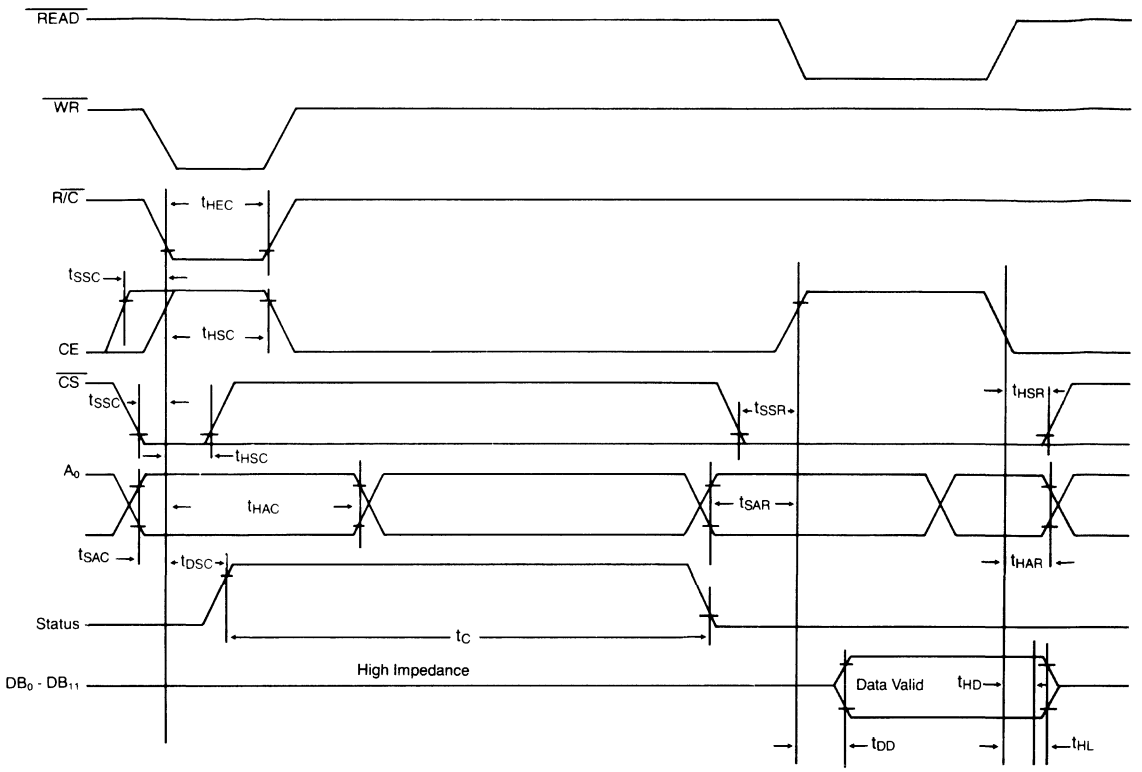
MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

HARDWIRING TO 8-BIT DATA BUSES — For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN6774 output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".



Hardwiring for 8-Bit Data Buses

TIMING DIAGRAM — FULL MICROPROCESSOR CONTROL



Initiating Conversion **Read Data Cycle**

TIMING — INITIATING CONVERSIONS — It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="1→0" and A_0="1" (initiate an 8-bit conversion) or A_0="0" (initiate a 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion is initiated by the falling edge of R/$\overline{C}$. CE and $\overline{CS}$ must be asserted and stable concurrently with the falling edge of R/$\overline{C}$. Because the MN6774's control logic latches the A_0 signal upon conversion initiation, the A_0 line should be stable immediately prior to the falling edge of R/$\overline{C}$.

The diagram below illustrates the initiation of a conversion and subsequent read cycle. When connected to and under micro processor control, conversions are initiated when the MN6774's CE input is high while R/$\overline{C}$ is brought low by $\overline{WR}$. In this application, CE, R/$\overline{C}$ are brought high while $\overline{CS}$ is low and A_0 is set to its chosen state prior to the falling edge of R/$\overline{C}$. Once a conversion has begun, additional convert commands will be ignored until the ongoing conversion is complete.

TIMING — RETRIEVING DATA — In the example below, data is enabled when $\overline{READ}$ is brought low, which in turn, brings CE high. This in combination with CE low and 12/$\overline{8}$="1" enables all twelve output bits to be read simultaneously. If the 12/$\overline{8}$ line is "0", output data will be formatted for an 8-bit bus. The 8 MSB's will become valid when the above conditions are met with A_0="0"; while the 8 LSB's (4 data bits plus 4 trailing "0's") will become valid whenever A_0="1". If 12/$\overline{8}$="1", A_0 is a "don't care." If an 8-bit conversion is performed and all 12 output data bits are read, bit 9 (DB3) will be a "1", and bits 10-12 (DB2-DB0) will be "0's".

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid 300nsec (typ) before the falling edge of Status. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TLL/CMOS compatible and may be actively driven.

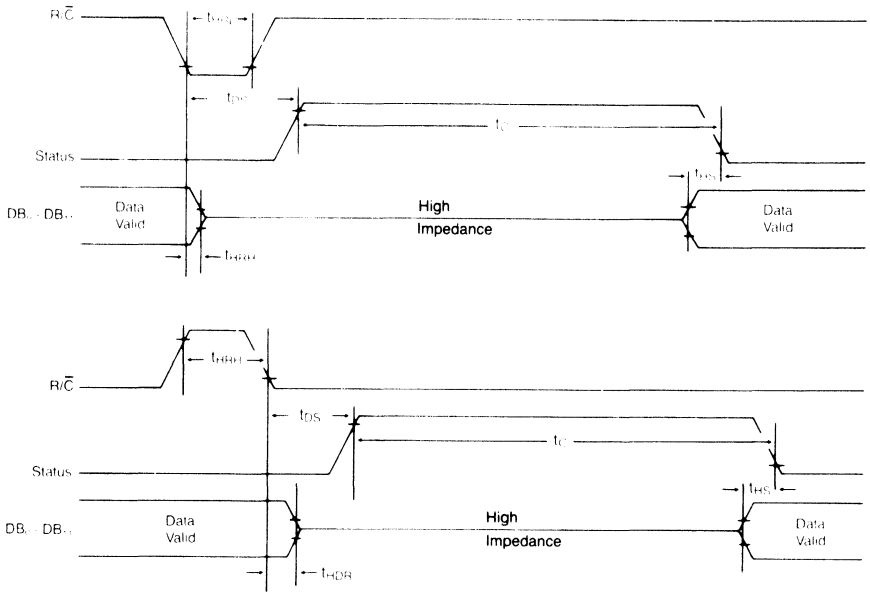
CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	Status Delay from R/$\overline{C}$		60	250	nsec
t_{HEC}	R/$\overline{C}$ Pulse Width	50	30		nsec
t_{SSC}	CE and $\overline{CS}$ Setup	0			nsec
t_{HSC}	CE and $\overline{CS}$ Hold Time	50	20		nsec
t_{SAC}	A_0 to R/$\overline{C}$ Setup	0			nsec
t_{HAC}	A_0 Valid During R/$\overline{C}$ Low	50	20		nsec
t_C	Conversion Time (+25°C)				
	8-Bit Cycle		5	5.3	μsec
	12-Bit Cycle		7.5	8	μsec

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time from CE		75	150	nsec
t_{HD}	Data Valid After CE Low	25	35		nsec
t_{HL}	Output Float Delay		100	150	nsec
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		nsec
t_{SAR}	A_0 to CE Setup	50	25		nsec
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			nsec
t_{HAR}	A_0 Valid After CE Low	50			nsec

TIMING DIAGRAM — STAND ALONE OPERATION



TAND-ALONE OPERATION

e MN6774 can be used in a "stand-alone" mode in systems ving dedicated input ports and not requiring full bus interface pability. In this mode, CE and 12/8 are tied to logic "1" (they ıy be hard-wired to +5V), $\overline{CS}$ and A_0 are tied to logic "0" (they ıy be grounded), and the conversion is controlled by R/$\overline{C}$. A ıversion is initiated whenever R/$\overline{C}$ is brought low (assuming a ıversion is not already in progress), and all 12 bits of the three-te output buffers are enabled when Status returns low indicating ıversion complete).

is gives rise to two possible modes of operation; conversions can initiated with either positive or negative R/$\overline{C}$ pulses. The timing ıgram details operation with a negative or positive start pulse. In ıer case, the outputs are forced into the high-impedance state esponse to the falling edge of R/$\overline{C}$ and return to valid logic levels ər the conversion cycle is completed.

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			nsec
t_{DS}	STS Delay from R/$\overline{C}$			200	nsec
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			nsec
t_{HS}	STS Delay After Data Valid		150	375	nsec
t_{HRH}	High R/$\overline{C}$ Pulse Width	50			nsec

IGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)			DIGITAL OUTPUT		
0 to −10V	±5V	±10V	MSB		LSB
−10.0000	−5.0000	−10.0000	1111	1111	1111
− 9.9963	−4.9963	− 9.9927	1111	1111	111Ø*
− 5.0012	−0.0012	− 0.0024	1000	0000	000Ø*
− 4.9988	+0.0012	+ 0.0024	0000	0000	000Ø*
− 4.9963	+0.0037	+ 0.0073	0111	1111	111Ø*
− 0.0012	+4.9988	+ 9.9976	0000	0000	000Ø*
0.0000	+5.0000	+10.0000	0000	0000	0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary.
2. For bipolar input ranges, output coding is complementary offset binary.
3. For 0 to −10V or ±5V input ranges, 1 LSB for 12 bits=2.44mV. 1 LSB for 11 bits=4.88mV.
4. For ±10V input range, 1 LSB for 12 bits=4.88mV. 1 LSB for 11 bits=9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN6774 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.9976 volts. Subsequently, any input voltage more positive than +9.9976 volts will give a digital output of all "0's." The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of +0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at −9.9927 volts. An input more negative than −9.9927 volts will give all "1's".

UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating modes are shown below. If the 0 to −10V input range is to be used, apply the analog input to pin 13. If gain adjustment is not used, replace trim pot R_2 with a fixed, 50Ω ± 1%, metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, the actual transition will occur within ± 2 LSB's of its ideal value (−½LSB). For the 10V range, 1 LSB=2.44mV. To offset adjust, apply an analog input equal to −½LSB and, with the MN6774 continuously converting, adjust the offset potentiometer "up" until the digital output is all "0's" and then adjust "down" until the LSB "flickers" between "0" and "1".

Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's above the nominal minus full scale of the selected input range. This corresponds to −9.9963V for the −10V unipolar input range. Gain trimming is accomplished by applying this voltage and adjusting the gain potentiometer "down" until the digital outputs are all "1's" and then adjusting "up" until the LSB "flickers" between "1" and "0".

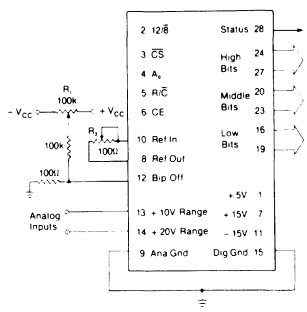
If a 10.24V (1 LSB=2.5mV) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor and a 200Ω trim pot inserted in series with the analog input to pin 13. Offset trimming proceeds as described above. Gain trimming is now accomplished with the new pots. If one is not gain trimming and wishes to use fixed-value resistors, the value is 120Ω. MN6774's input impedance is laser trimmed to a typical accuracy of ± 2%.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating modes are shown below. If the ± 5V input range is to be used, apply the analog input to pin 13. If the ± 10V range is used, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trim pots R_1 and R_2 should be replaced with fixed, 50Ω ± 1%, metal-film resistors to meet all published specifications.

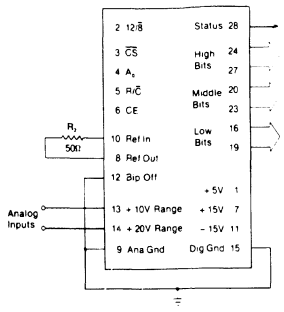
Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition should occur ½LSB above zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the positive full scale point. The procedure is to apply an analog input equal to +FS−½LSB (+4.9988V for the ± 5V range, +9.9976V for the ± 10V range) and adjust the bipolar offset trim pot "up" until the digital output is all "0's". Then adjust "down" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's above the nominal negative full scale value of the selected input range. This corresponds to −4.9963V and −9.9927V respectively for the ± 5V and ± 10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "down" until the digital outputs are all "1's" and then adjusting "up" until the LSB "flickers" between "1" and "0".

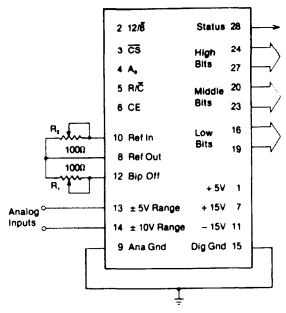
MN6774 unipolar operation with trim adjustment.



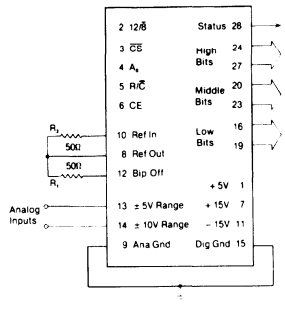
MN6774 unipolar operation without trim adjustment.



MN6774 bipolar operation with trim adjustment.



MN6774 bipolar operation without trim adjustment.



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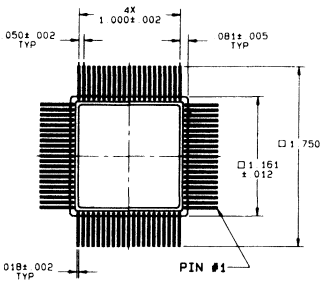
MICRO NETWORKS

MN6900

8-Bit, 500MHz
SAMPLING A/D CONVERTER

FEATURES

- **500MHz Effective Conversion Rate**
- **7.0 Effective Bits at 250MHz Input**
- **50Ω input**
- **±1/2 LSB Integral Linearity Error**
- **$<10^{-15}$ Metastable States**
- **±270mV Input Signal Range**
- **Dual Interleaved Output Data Paths**
- **Reference Sense Inputs for Precision Reference Voltage Setting**
- **+5V, -5.2V Power Supplies**
- **Latched ECL Compatible Outputs**
- **84 Pin Strip-Line Ceramic Package**
- **7.5W Power Dissipation**



DESCRIPTION

The MN6900 is a high speed, 8-bit, fully parallel Analog to Digital converter with strobed comparators, latched outputs and internal Track-Hold amplifier. Dual monolithic converters, driven by the track-hold, operate on opposite clock edges (time interleaved). Sampling rates of 500MHz allow accurate digitizing of analog signals from DC to 250MHz.

Innovative design of the internal T/H gives exceptionally wide input bandwidths of 1.2GHz and aperture jitter of <2pS. These two features combine to give effective bits performance of 7.0 at an input signal frequency of 250MHz. Special comparator output design and decoding minimizes metastable states and out-of-sequence codes.

APPLICATIONS

High Energy Physics
Radar/Sonar
Communications
Medical Electronics

ORDERING INFORMATION

Model Number	Speed	Resolution	Package
MN6900	500MHz	8-bit, T/H	Ceramic 84-pin Quad
MN6900EVB	500MHz	8-bit, T/H	Evaluation Board

THERMAL CHARACTERISTICS

Thermal Resistance Junction-to-Case ($R_{\theta JC}$)	5°C/W
Thermal Resistance Junction-to-Ambient ($R_{\theta JA}$, 200 Lineal Ft/min)	12°C/W
with heat sink ($R_{\theta JA}$, 400 Lineal Ft/min)	9°C/W

MICRO NETWORKS
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MN6900 8 Bit 500MHz SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Negative (V_{EE})	-7 to 0V	Clock Input Voltage (V_{IH}, V_{IL})	-2.3 to 0V
Supply Voltage, Positive (V_{CC})	0 to +7V	DIV10 Input Voltage (V_{IH}, V_{IL})	V_{EE} to 0V
Supply Voltage, Difference (V_{CC}-V_{EE})	12V	Output Current, $I_O$max (T_J <100°C)	14mA
Analog Input Voltage (V_{AIN})	±2V	(100<T_J<125°C)	12mA
Reference Voltage (VA_{RT}, VB_{RT})	-0.3 to ±1.5V	Storage Temperature (T_{STG})	-55 to +150°C
Reference Voltage (VA_{RB}, VB_{RB})	-1.5 to ±0.3V	Operating Temperature, Junction (T_{OPR})	-15 to +125°C
		Lead Temperature (solder <10sec) (T_S)	+250°C

V_{EE}=-5.2V, V_{CC}=+5V, R_L=100Ω to -2V, V_{RT}=1.02V, V_{RB}=-1.02V, T_A=25°C unless otherwise noted.

ANALOG INPUTS	**MIN**	**TYP**	**MAX**	**UNITS**
Input Voltage Range: Differential		±270		mV
Single-Ended		±270		mV
Input Offset Voltage	-17		+32	mV
Input Resistance	49		51	Ω
Full-Power Bandwidth (Note 1)		1.2		GHz
Common Mode Rejection Ratio (V_{INCM} = ±0.5V)		45		dB
REFERENCE INPUTS				
Reference Voltages (Note 2) V_{RT},V_{RB}			1.2	V
Reference String Resistance	100		175	Ω
DIGITAL INPUTS				
Logic Levels: Logic "1"				
±CLK	-1.13		-0.81	V
±TRK1	-0.05		+0.05	V
Logic "0"				
±CLK	-1.95		-1.48	V
±TRK1	-0.5		-0.35	V
Logic Currents:				
Logic "1", DIV10	1.2		3	mA
Input Bias Current, PH_{ADJ}	-50		40	µA
Clock Input:				
Pulse Width High (Note 5)	0.9		2.5	nsec
Pulse Width Low (Note 5)	0.9		2.5	nsec
Bias Current			50	µA
Input Capacitance		6		pF
DIGITAL OUTPUTS				
Logic Levels: Logic "1"				
ADATA, BDATA	-0.95		-0.7	V
±DCLK	-0.95		-0.7	V
Logic "0"				
ADATA, BDATA	-1.85		-1.6	V
±DCLK	-1.3		-1.0	V
V_{OH}-V_{OL}, (+DCLK)-(-DCLK)	280		440	mV
TRANSFER CHARACTERISTICS				
Integral Linearity Error			±0.5	LSB
Differential Linearity Error			±0.5	LSB
DYNAMIC PERFORMANCE				
Maximum Conversion Rate	500			MHz
Aperture Width		270		psec
Aperture Jitter		2		psec
AC LINEARITY (Note 3)				
Dynamic Linearity (Effective Bits)				
f_{AIN} = 10MHz		7.6		Bits
f_{AIN} = 125MHz		7.1		Bits
f_{AIN} = 250MHz		7.0		Bits
Signal-to-Error Ratio (Note 4)				
f_{AIN} = 100MHz		45		dB
POWER SUPPLIES				
Power Supply Range: +V_{CC}	4.75		5.25	V
-V_{EE}	-5.46		-4.94	V
Power Supply Rejection Ratio: +V_{CC}		49		dB
-V_{EE}		66		dB
Power Supply Current Drains: +V_{CC}		765	1065	mA
-V_{EE}		750	935	mA

SPECIFICATION NOTES:

1. Full Power Bandwidth is the input frequency at which the reconstructed output amplitude drops 3dB with respect to a low frequency output.
2. V_{RT} must always be more positive than V_{RB}.
3. Measured at a 500MHz sample rate with analog input equal to 95% of full-scale.
4. Calculated from effective bits performance.
5. Guaranteed but not tested.

PIN DESCRIPTION FOR 84 PIN PACKAGE

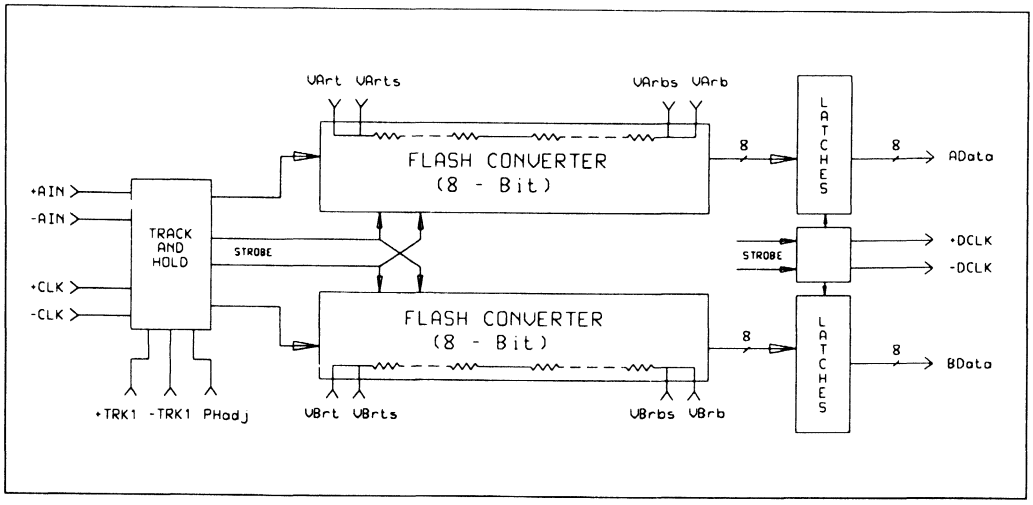
Pin #	Symbol	Comments
72,73 75,76	+AIN -AIN	These are the Analog inputs, input impedance = 50Ω to ground. Full scale linear input range =±270mV approx. It is recommended that inputs +AIN, -AIN, be driven differentially for best high frequency performance.
1	PAD	Internal connection, leave pin open
2,62 3,61	+CLK -CLK	+CLK and -CLK are the differential clock inputs. They can be driven from ECL with the following considerations: Internally pin 2 and pin 62 are the ends of a 50 ohm transmission line. Pin 3 and pin 61 are connected in a similar manner. Either end of these can be driven with the other end terminated with 50 ohms to -2V.
6,58	+TRK1	Phasing inputs, see application section.
5,59	TRK1	Phasing inputs, see application section.
47 45 44 42 41 39 38 36	A0 A1 A2 A3 A4 A5 A6 A7	A0 through A7, and B0 through B7 are the AData and BData outputs. A0 and B0 are designated as the LSBs, A7 and B7 the MSBs. AData and BData outputs conform to ECL logic swings over a limited temperature range and will drive 100 Ohm transmission lines. Terminate with 100 Ohms to -2V (120 Ohm for T_j>100°C). See Figures 1-3 for timing information.
17 19 20 22 23 25 26 28	B0 B1 B2 B3 B4 B5 B6 B7	See A0 through A7 above. See Figures 1-3 for timing information.
29	SUB	Circuit Substrate contact. This pin **MUST** be connected to V_{EE}.
33 31	+DCLK -DCLK	Differential clock output (+DCLK, -DCLK). Used to time and phase following circuitry. Outputs A0 through A7 are valid after the rising edge of +DCLK. B0 through B7 output data are valid after the falling edge of +DCLK (see Figure 1 for output timing information).
35	DIV10	Divide by 10 mode pin. Leave open for normal operation. Selects divide by 10 mode when grounded.
16,48,63	NC	No internal connections to these pins.
52	TP1	Internal connection, leave pin open
53	TP2	Internal connection, leave pin open
12	TP3	Internal connection, leave pin open
11	TP4	Internal connection, leave pin open
65	TP5	Internal connection, leave pin open
66	TP6	Internal connection, leave pin open

Pin #	Symbol	Comments
83	PH_{ADJ}	Phase adjustment for T/H. Normally connected to ground. A phase adjustment of approx. ±18pS can be made by varying this pin's bias point to optimize interleaving between sides A and B (see Note 1).
81	VCCT	Positive supply connection for internal node. Connect this pin to VCC.
50	VART	"A" side positive reference voltage top input (see Note 2).
51	VARTS	"A" side positive reference voltage top sense (see Note 2).
55	VARB	"A" side negative reference voltage bottom input (see Note 2).
54	VARBS	"A" side negative reference voltage bottom sense (see Note 2).
14	VBRT	"B" side positive reference voltage top input (see Note 2).
13	VBRTS	"B" side positive reference voltage top sense (see Note 2).
9	VBRB	"B" side negative reference voltage bottom input (see Note 2).
10	VBRBS	"B" side negative reference voltage bottom sense (see Note 2).
4,7,15,49	GND	Power Supply Ground. Connect all pins.
57,60,64,67		
70,71,74,77		
78,79,82,84		
18,24,27,30		
34,37,40,46		
8,21,43,56	VCC	Positive power supply, +5V nominal.
32,69,80	VEE	Negative power supply, -5.2V nominal.

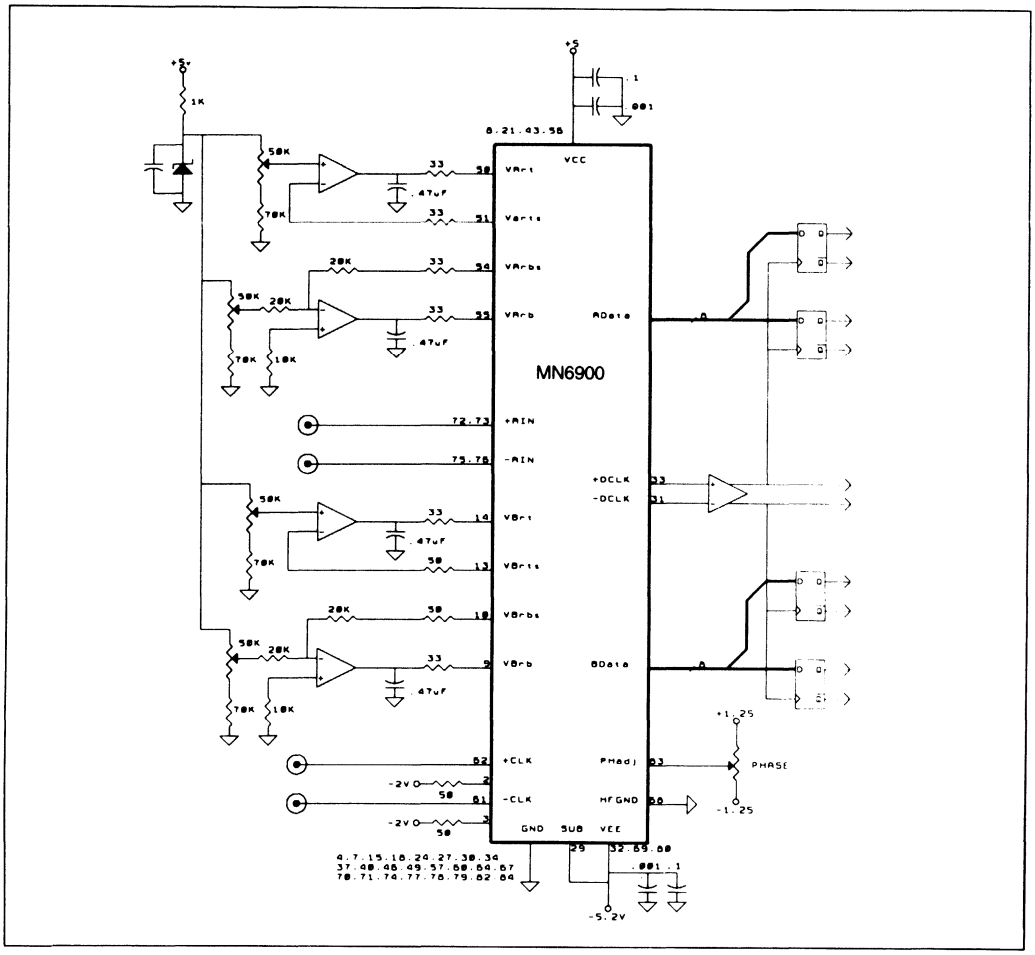
Note 1: Good results are obtained by connecting the PH_{ADJ} input to ground. Improved performance can be achieved by applying a voltage between ±1.25V to this input. The point in time that the "A" T/H bridge samples relative to the time that the "B" T/H bridge samples can be varied through a ±18pS typ. range.

Note 2: VART, VARB, VBRT, and VBRB should be adjusted separately from a well bypassed reference circuit to ensure proper amplitude and offset matching. The sense connection to each of these terminals allows precision setting of the reference voltage. The reference ladder is similar for both networks (check electrical section for values). Any noise on these terminals will severely reduce overall performance.

FUNCTIONAL DIAGRAM



TYPICAL CONNECTION DIAGRAM



DEFINITION OF TERMS

EFFECTIVE BITS

Dynamic accuracy of the MN6900 is expressed in effective bits. Effective bits is a measure of the signal to error ratio of an analog to digital conversion. Effective bits is expressed as the number of bits of an ideal, but lower resolution, A/D conversion with the same signal to error ratio. That is, the quantization error of the ideal converter equals the total error of the device. In addition to the ideal quantization error, other sources of error include all DC and AC non-linearities, clock and aperture jitter, missing output codes, and noise. Noise on references and supplies also degrades effective bits performance.

Effective bits is calculated from a digital record taken from the A/D under test. The input to the A/D is a sine wave filtered with an anti-aliasing filter to remove any harmonic content. The digital record taken from this signal is compared against a mathematically generated sine wave. DC offsets, phase and amplitudes of the mathematical model are adjusted until a best fit sine wave is found. After subtracting this sine wave from the digital record the residual error remains. The rms value of the error is applied in the following equation to yield the A/D converter's effective bits.

$$EB = N - \mathrm{Log}_2\left(\frac{\text{measured rms error}}{\text{ideal rms error}}\right)$$

'N' is the resolution of the converter. In this case N = 8.

It is important to note at which frequency the measurement was made. The worst case error for any device will be at the converter's maximum clock rate with the analog input near the Nyquist rate (1/2 the input clock rate).

APERTURE WIDTH AND JITTER

Aperture width and aperture jitter are performance indicators of the A/D converter. Each of these parameters will greatly affect the A/D's high frequency accuracy (see Figure 4). Aperture width is defined as the time that the track-and-hold circuit takes to disconnect the hold capacitor from the input circuit (i.e., to turn off the sampling bridge and put the T/H in its hold mode). Aperture jitter is defined as the uncertainty of the actual start point of the aperture width.

METASTABLE STATES

In a typical A/D converter, metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any of the 255 input comparators. The output code resulting from this input voltage can have a large error and could result in a false full or zero scale output. Through innovative circuit design, Micro Networks has reduced the magnitude of this type of error in the MN6900 to less than one LSB, and reduced the probability of this occurring to less than one error every 10^{15} clock cycles. If the MN6900 were operated at 500 MHz, 24 hours per day, this would translate to one metastable state error every 50 days.

INTEGRAL LINEARITY ERROR

Integral Linearity Error (ILE) is the difference between the measured input voltage and the calculated input voltage for that output code. The calculated input voltage is determined from a straight line least squares fit for all transitions. ILE is expressed in terms of an LSB size.

$$LSB = \frac{1}{\text{slope of least squares fit line}}$$

$$ILE(LSB) = \frac{V_{MEAS} - V_{CAL}}{LSB}$$

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the difference between the measured LSB step and an ideal LSB step size between adjacent code transitions. DLE is expressed in LSBs and is calculated using the following equation:

$$DLE(LSB) = \frac{(V_{MEAS} - (V_{MEAS\text{-}1})) - LSB}{LSB}$$

$V_{MEAS\text{-}1}$ is the measured value of the previous code.

A DLE error specification of <1 LSB guarantees that there are no missing codes and the transfer function is monotonic.

APPLICATION NOTES

POWER SUPPLIES/GROUNDS

A +5V supply as well as a -5.2 V supply is needed for proper operation. Bypassing of the VEE and VCC supply pins to GND should be done with a good quality 0.1 µF and 0.001 µF ceramic capacitor located as close to the package as possible.

CLK AND DCLK.

All clock signals, input and output, are differential. The input clocks, +CLK and -CLK, are the primary timing signals for the MN6900, and are fed to the internal circuitry from one of two input groups, pins (2,3) or pins (62,61), through a 50 Ω transmission line. One set of +CLK, -CLK inputs should be driven and the other pair terminated by 50 Ω to -2 V. Either set of inputs can be used as the driven inputs (input lines are balanced) for ease of circuit connection. A minimum pulse width t_{pwi} is required for the input clocks, +CLK, -CLK, to ensure proper operation (see timing Figures 1 through 3).

To ensure optimum performance and repeatable results, a low phase noise clock source should be used for +CLK and -CLK. Phase noise from the input clock source will reduce the converter's effective bits performance and cause inconsistent results. The clock supplied to the MN6900 is internally divided by two, reshaped, and buffered. This divided clock becomes the internal signal used as strobes for the converters.

+DCLK, -DCLK are output clock signals derived from the input clocks and are used for external timing of the data outputs AData and BData (AData is valid on the rising edge of +DCLK, and BData is valid on the falling edge). They are fixed at one half the rate of the input clocks in divide by '1' mode. The MN6900 is specified to work at a maximum input clock frequency of 500 MHz (see Table 1).

DATA FLOW

The MN6900 contains an internal Track and Hold (T/H) amplifier that samples the analog input voltage for the A/D to convert. The T/H is split into two sections which operate on opposite clock edges. The input clock, +CLK, is conditioned by the T/H and fed to the A/D section. The output clock +DCLK, used for output data timing, will be divided by 2 or 10 from the input clock +CLK (see Table 1). The differential inputs, +AIN and -AIN, are tracked continuously between data samples. When a negative internal strobe edge is sensed, the T/H goes into the hold mode (see Figure 4). When the internal strobe is in the low state, the just acquired sample is presented to the A/D converter's input comparators. Internal processing of the sampled data takes an additional 15 clock cycles before it is available at the outputs AData and BData. For timing see Figures 1 through 3.

INPUT CLOCK PHASING

The clock edge that AData and BData operate from is undetermined at power up. If the converter is desired to work off a specific input clock edge, the following procedure using +TRK1 and -TRK1 must be implemented.

+TRK1 and -TRK1 are differential ECL inputs that are used in addition to the normal input clock (+CLK) to set phasing of the data. A signal at one half of the input clock rate with the proper set up and hold time (setup and hold typically 300 ps) is applied to these inputs. By applying a logic "1" to +TRK1 ("0" to -TRK1) before the negative transition of +CLK, side AData is chosen. If BData is desired at the negative edge of +CLK, then a logic "0" must be applied ("1" to -TRK1) instead. In this manner, several MN6900 converters can be interleaved to obtain faster effective sampling rates.

TRACK-AND-HOLD

As with all A/D converters, if the input waveform is changing rapidly at the time of conversion the Effective Bits (EB) and Signal to Error Ratio (SER) will decrease. To avoid this problem a Track-and-Hold (T/H) circuit was added internally to the MN6900. The T/H increases attainable effective bits performance, and allows capture of analog data more accurately at high conversion rates.

The T/H provides two additional circuit functions for the MN6900. First, its nominal voltage gain of four (4) reduces the input driving signal to 270 mV (±135 mV differentially, normal conversion range assuming a ±1.02 V reference). Secondly, the T/H provides a differential 50 Ω low VSWR input allowing easy interfacing to this converter. Although the normal operating range is 270 mV, it can be operated with up to ±500 mV on each input with respect to ground. This extended input level would include the analog signal and any DC common mode voltage.

To obtain full scale digital output with differential input drive, a nominal 270 mV must be applied between +AIN and -AIN. That is, +AIN = +135 mV and -AIN= -135 mV (when no DC offset is applied). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero scale digital output code, with differential drive, occurs when +AIN = -135 mV and -AIN = +135 mV. The output of the converter stays at all ones (full scale) or all zeros (zero scale) when over or under ranged, respectively. Table 2 shows these relationships in a tabular form.

Single ended operation can be handled simply by applying a DC offset to, or by leaving open, one of the analog inputs (both +AIN and -AIN are terminated internally with 50 Ω to analog ground). Then drive one input with a ±270 mV + offset to obtain either full or zero scale digital output. If a DC common mode offset is to be applied, the total voltage swing allowed is ±500 mV (analog signal plus offset with respect to ground).

INPUT REFERENCE LADDER

The A/D converter's reference ladder is a Kelvin sensed resistor string used to set the LSB size and dynamic operating range of the converter. Normally, the top and bottom of this string are driven with an op-amp circuit.

The buffer amplifier circuit used to drive the top and bottom inputs will need to supply approximately 21 mA due to a resistor string impedance of 100 Ω minimum. A reference voltage of ±1.02 V is normally applied to inputs VA_{RT}, VB_{RT} and VA_{RB}, VB_{RB}. These references control the comparators' input windows and can be adjusted up to ±1.2 V to accommodate extended input requirements (accuracy specifications are guaranteed with references of ±1.02 V). The reference inputs VA_{RTS}, VA_{RBS}, VB_{RTS}, and VB_{RBS} allow Kelvin sensing of the applied voltages for precision setting of the resistor chain.

Any noise on the reference pins will directly affect the code uncertainty and degrade the effective bits performance of the A/D.

TABLE 1 — OUTPUT MODE CONTROL

DIV10	DCLK*	Description
		(Divide by 1 mode)
OPEN	250 MHz	AData and BData valid on opposite DCLK edges (AData on rise, BData on fall).
		(Divide by 10 mode)
GND	50 MHz	AData and BData valid on opposite DCLK edges (AData on rise, BData on fall). Data sampled at input CLK rate but 4 out of every 5 samples discarded.

* Input clocks (+CLK, -CLK) = 500 MHz for all above combinations.
In all modes the output clock +DCLK will be a 50% duty cycle signal.

TABLE 2 — INPUT VOLTAGE RANGE

Input	+AIN**	-AIN**	Output Code MSB to LSB	
	+135 mV	-135 mV	1 1 1 1 1 1 1 1	full scale
Differential	0	0	1 0 0 0 0 0 0 0	mid scale
	-135 mV	+135 mV	0 0 0 0 0 0 0 0	zero scale
	+270 mV	0	1 1 1 1 1 1 1 1	full scale
Single Ended	0	0	1 0 0 0 0 0 0 0	mid scale
	-270 mV	0	0 0 0 0 0 0 0 0	zero scale

** An offset V_{10}, as specified in the DC electrical parameters, will be present at the input. Compensate for this offset by adjusting the reference voltage. Offsets may be different between side A and side B.

APPLICATION NOTES

DIV10

When DIV10 is grounded it enables the divide by 10 circuitry. The output data and clock rates are reduced by a factor of 10 with respect to the input clock. The output clock duty cycle remains at 50% and the clock to output data phasing remains the same. In this mode four out of every five sampled input values are discarded. When left open this input will be pulled low by internal circuitry and the converter will function in its fastest mode. This pin is left open for normal operation.

PHASE ADJUST

PH_{ADJ} is normally connected to ground, but can be adjusted from a variable supply of ±1.25 V. This control affects the point in time that one half of the converter samples the input signal relative to the other half. An adjustment range of ±18 ps typically, is made available for optimization of converter performance.

If PH_{ADJ} is not grounded, care should be taken to bypass it properly since any noise on this pin will reduce system performance.

INTERLEAVING

PH_{ADJ} is used only to adjust timing between the clock and data as stated above. Reference inputs must be adjusted to compensate for amplitude and offset differences.

Figure 1. **Output Timing: DIV10 = OPEN**

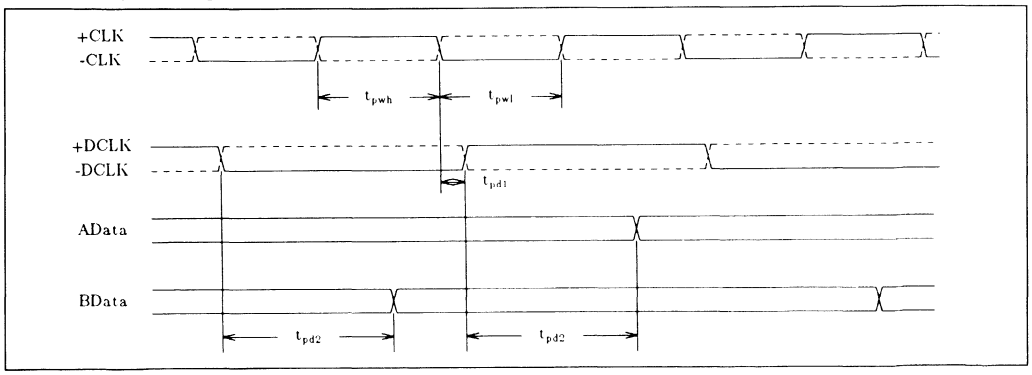
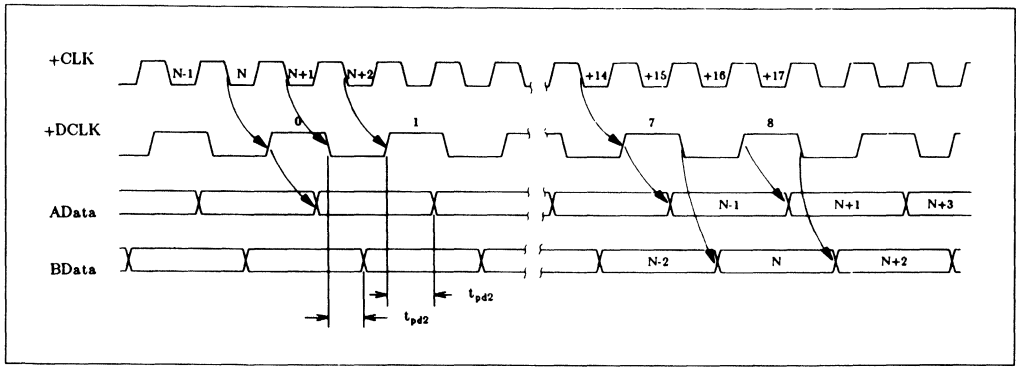
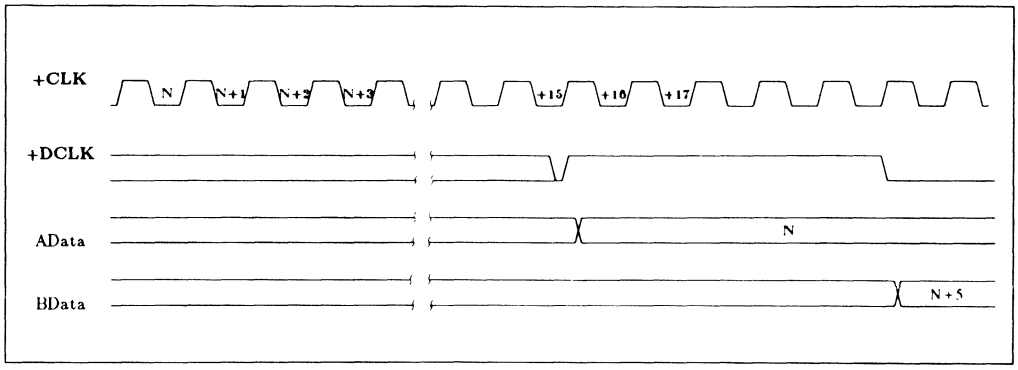


Figure 2. **Output Timing: Clock to Data, Fast Mode DIV10 = OPEN**



Data arbitrary on start up for side A or B unless TRK1 is used.

Figure 3. **Output Timing: Divide by 10 Mode (DIV10 = GND)**



Data arbitrary on start up for side A or B unless TRK1 is used.

Figure 4. **T/H Aperture Timing**

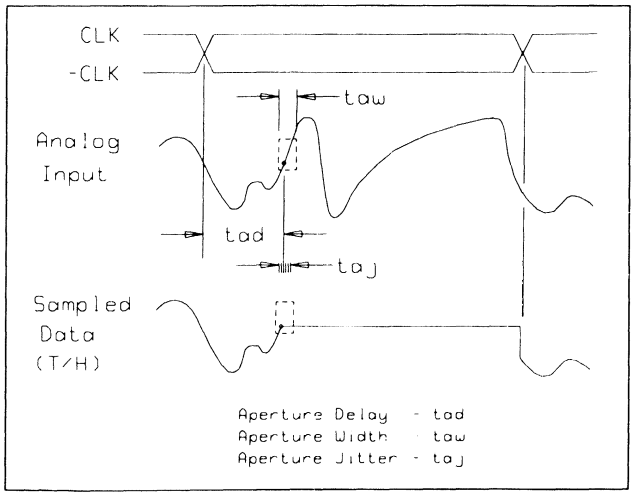


Figure 5.

Integral Linearity Error (LSB's) vs Output Code

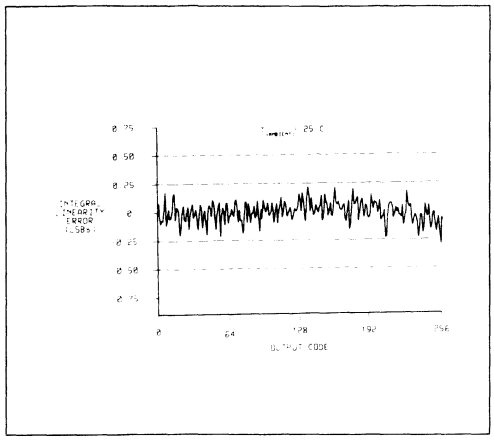


Figure 6.

Differential Linearity Error (LSB's) vs Output Code

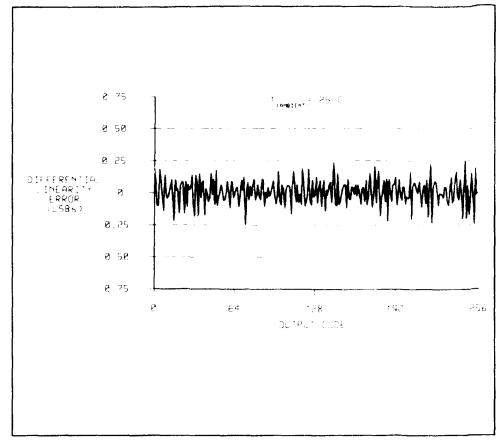


Figure 7. FFT.

F_{CLK} = 500 MHz, F_{AIN} = 251.4462 MHz, SER = -44.5 dB, Noise Floor = -67.3 dB, Spurious = -58.2 dB

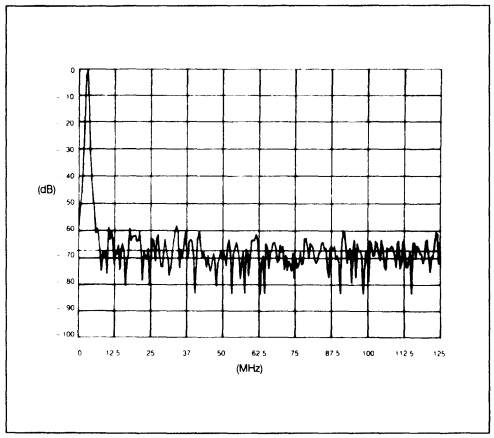


Figure 8. FFT.

F_{CLK} = 250 MHz, F_{AIN} = 10.4462 MHz, SER = -47.2 dB, Noise Floor = -70.5 dB, Spurious = -61.8 dB

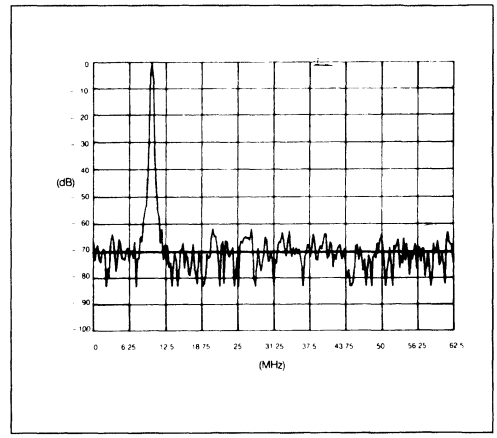


Figure 9. **Effective Bits vs Frequency (F_{AIN})**
F_{CLK} = 500 MHz, V_{IN} = 95% FS

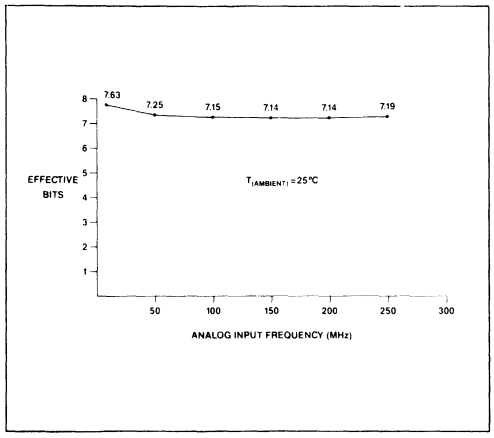
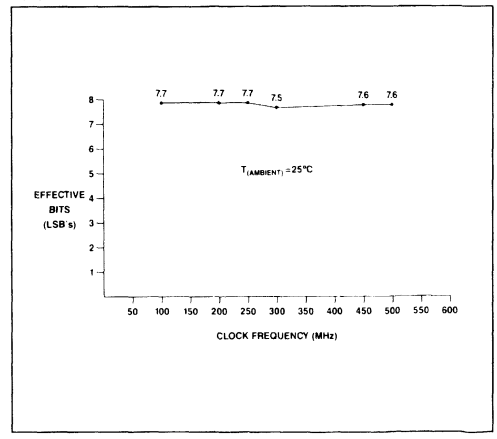
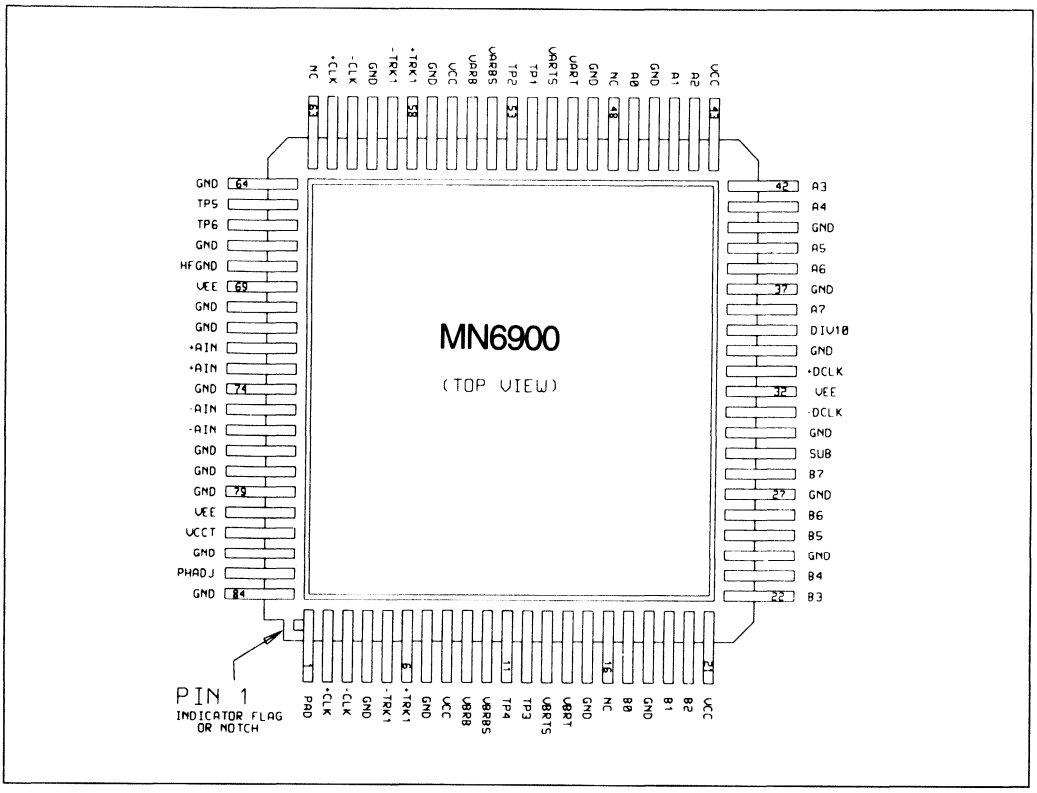
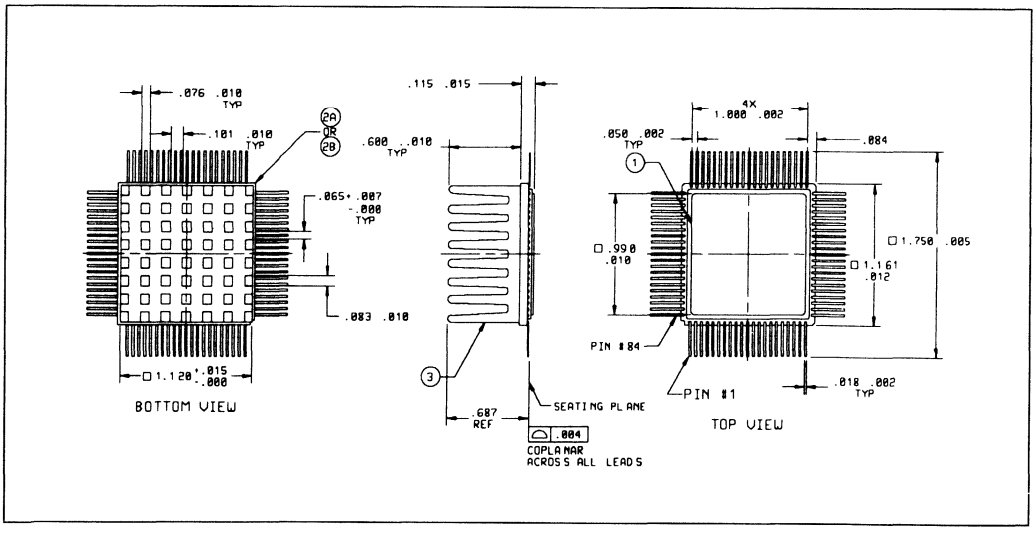


Figure 10. **Effective Bits vs Frequency (F_{CLK})**
F_{AIN} = 10.4462 MHz, V_{IN} = 95% FS




MN6900
(TOP VIEW)
PIN 1
INDICATOR FLAG
OR NOTCH
NC
•CLK
-CLK
GND
-TRK1
•TRK1
GND
VCC
VARB
VARBS
TP2
TP1
VARTS
VART
GND
NC
A0
GND
A1
A2
VCC
GND
TPS
TP6
GND
HFGND
VEE
GND
GND
•AIN
•AIN
GND
-AIN
-AIN
GND
GND
GND
VEE
VCCT
GND
PHADJ
GND
A3
A4
GND
A5
A6
GND
A7
DIV10
GND
•DCLK
VEE
-DCLK
GND
SUB
B7
GND
B6
B5
GND
B4
B3
PAD
•CLK
-CLK
GND
-TRK1
•TRK1
GND
VCC
VARB
VARBS
TP4
TP3
VARTS
VART
GND
NC
B0
GND
B1
B2
VCC


.076 .010
TYP
.101 .010
TYP
2A
OR
2B
.600 .010
TYP
.065+.007
-.000
TYP
.083 .010
□1.120+.015
-.000
BOTTOM VIEW
.115 .015
3
.687
REF
SEATING PLANE
.004
COPLANAR
ACROSS ALL LEADS
4X
1.000 .002
.050 .002
TYP
1
.884
□.990
.010
□1.161
.012
□1.750 .005
PIN #84
PIN #1
.018 .002
TYP
TOP VIEW



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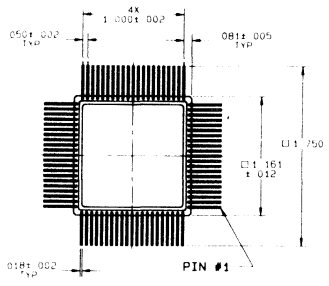
MICRO NETWORKS

MN6901

8-Bit, 250MHz
SAMPLING A/D CONVERTER

FEATURES

- **250MHz Effective Conversion Rate**
- **6.8 Effective Bits at 125MHz Input**
- **50Ω input**
- **<±1/2 LSB Integral Linearity Error**
- **<10^{-15} Metastable States**
- **Dual Output Data Paths**
- **On Chip 8 to 16 Demux, Selectable**
- **±270mV Input Signal Range**
- **Reference Sense Inputs for Precision Reference Voltage Setting**
- **+5V, -5.2V Power Supplies**
- **Latched ECL Compatible Outputs**
- **84 Pin Strip-Line Ceramic Package**
- **5W Power Dissipation**



DESCRIPTION

The MN6901 is a high speed, 8-bit, fully parallel Analog to Digital converter with strobed comparators, latched outputs and internal Track-Hold amplifier. A sampling rate of 250MHz allows accurate digitizing of analog signals from DC to 125MHz.

Innovative design of the internal T/H achieves input signal bandwidths of 1.2GHz and aperture jitter of <2pS. These two features combine to give effective bits performance of 6.8 at 125MHz. In addition, special comparator output decoding minimizes false codes.

Dual output data paths provide several data output modes for easy interfacing. These modes include two identical fast outputs, or an 8:16 demultiplexer to reduce output data rates to one-half the clock rate.

APPLICATIONS

High Energy Physics
Radar/Sonar
High Speed Image Processing
Communications
Medical Electronics
Instrumentation

ORDERING INFORMATION

Model No.	Speed	Resolution	Package
MN6901	250MHz	8-bit, T/H	Ceramic 84-pin Quad
MN6901EVB	250MHz	8-bit, T/H	Evaluation Board

THERMAL CHARACTERISTICS

Thermal Resistance Junction-to-Case ($R_{\theta JC}$)	5°C/W
Thermal Resistance Junction-to-Ambient ($R_{\theta JA}$, 200 Lineal ft/min)	12°C/W

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

February 1991
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MN6901 8 Bit 250MHz SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Negative (V_{EE})	-7 to 0V	Digital Input Voltage (V_{IH}, V_{IL})	-2.3 to 0V
Supply Voltage, Positive (V_{CC})	0 to +7V	Data Output Current (I_{OMAX})	-33mA
Supply Voltage, Difference (V_{CC}-V_{EE})	12V	DCLK Output Current (I_{OMAX})	-43mA
Analog Input Voltage (V_{AIN})	±2V	Storage Temperature (T_{STG})	-55 to +150°C
Reference Voltage (VA_{RT})	-0.3 to +1.5V	Operating Temperature, Junction (T_{OPR})	-15 to +125°C
Reference Voltage (VA_{RB})	-1.5 to +0.3V	Lead Temperature (solder <10sec) (T_S)	+250°C

V_{EE}=-5.2V, V_{CC}=+5V, R_L=50Ω to -2V, V_{RT}=1.02V V_{RB}=-1.02V, T_A=25°C unless otherwise noted.

	MIN	TYP	MAX	UNITS
ANALOG INPUTS				
Input Voltage Range: Differential		±270		mV
Single-Ended		±270		mV
Input Offset Voltage	-17		+32	mV
Input Resistance	49		51	Ω
Full-Power Bandwidth (Note 1)		1.2		GHz
Common Mode Rejection Ratio (V_{INCM} = ±0.5V)		45		dB
REFERENCE INPUTS				
Reference Voltages (Note 2) V_{RT},V_{RB}			±1.4	V
Reference String Resistance	100		150	Ω
DIGITAL INPUTS				
Logic Levels: Logic "1"	-1.13		-0.81	V
Logic "0"	-1.95		-1.48	V
Logic Currents: Logic "1" (V_{IH}=-0.8V)				
DIV, MOD, A=B	-5		20	µA
CLK (no termination)	0		75	µA
Logic "0" (V_{IL}=-1.8V)				
DIV, MOD, A=B	-5		20	µA
CLK (no termination)	0		75	µA
Clock Input:				
Pulse Width High (Note 5)	1.9			nsec
Pulse Width Low (Note 5)	1.9		5	nsec
Input Capacitance		6		pF
DIGITAL OUTPUTS				
Logic Levels: Logic "1"	-1.02		-0.7	V
Logic "0"	-1.95		-1.6	V
TRANSFER CHARACTERISTICS				
Integral Linearity Error			±0.5	LSB
Differential Linearity Error			±0.5	LSB
DYNAMIC PERFORMANCE				
Maximum Conversion Rate	250			MHz
Aperture Width		270		psec
Aperture Jitter		2		psec
AC LINEARITY (Note 3)				
Dynamic Linearity (Effective Bits)				
f_{AIN} = 10MHz		7.4		Bits
f_{AIN} = 50MHz		7.1		Bits
f_{AIN} = 125MHz		6.8		Bits
Signal-to-Error Ratio (Note 4)				
f_{AIN} = 50MHz		45		dB
POWER SUPPLIES				
Power Supply Range: +V_{CC}	4.75		5.25	V
-V_{EE}	-5.46		-4.94	V
Power Supply Rejection Ratio: +V_{CC}		49		dB
-V_{EE}		66		dB
Power Supply Current Drains: +V_{CC}		464	670	mA
-V_{EE}		560	750	mA

SPECIFICATION NOTES:

1. Full Power Bandwidth is the input frequency at which the reconstructed output amplitude drops 3dB with respect to a low frequency output.
2. +V_{RT} must always be more positive than -V_{RB}.
3. Measured at a 250MHz sample rate with an analog input equal to 95% of full-scale.
4. Calculated from effective bits performance.
5. Guaranteed but not tested.

PIN DESCRIPTION FOR 84 PIN PACKAGE

Pin #	Symbol	Comments
72,73 75,76	+AIN -AIN	These are the Analog inputs, input impedance = 50Ω to ground. Full scale linear input range ±270mV approx. It is recommended that inputs +AIN, -AIN, be driven differentially for best high frequency performance.
1	PAD	Internal connection, leave pin open.
2,62 3,61	CLK $\overline{CLK}$	CLK and $\overline{CLK}$ are the differential clock inputs. They can be driven from standard 10KH ECL with the following considerations: Internally pin 2 and pin 62 are the ends of a 50 Ohm transmission line. Pin 3 and pin 61 are connected in a similar manner. Either end of these can be driven with the other end terminated with 50 Ohms to -2V.
45	A0	AData output pins.
42 39 36 26	A1 A2 A3 A4	A0 through A7, and B0 through B7 are the AData and BData outputs. A0 and B0 are designated as the LSBs, A7 and B7 the MSBs. AData and BData outputs conform to ECL logic swings over standard 10KH temperature ranges and will drive 50 Ohm transmission lines.
23 20 17	A5 A6 A7	Terminate with 50 Ohms to -2V. See Figures 1-4 for timing information.
47 44 41 38 28 25 22 19	B0 B1 B2 B3 B4 B5 B6 B7	BData output pins. (See AData above)
29	SUB	Circuit substrate contact. This pin **MUST** be connected to V_{EE}.
14	DCLK	Differential clock output (DCLK, $\overline{DCLK}$). Used to synchronize following circuitry. Outputs A0 through A7 and B0 through B7 are valid t_{pd2} after the rising edge of DCLK (see Figures 1 through 4 for timing information).
13	$\overline{DCLK}$	Differential clock output (complement of DCLK, see above).
68	TP1	Internal connection. This pin **MUST** be connected to GND.
66	TP2	Internal node. Do not connect.
65	TP3	Internal node. Do not connect.
50	VA_{RT}	Positive reference voltage input (see Note 1).
51	VA_{RTS}	Positive reference voltage sense (see Note 1).
53	VA_{CT}	Reference bias resistor centertap (see Note 2).
52	VA_{CTS}	Reference bias resistor centertap sense (see Note 2).
55	VA_{RB}	Negative reference voltage input (see Note 1).
54	VA_{RBS}	Negative reference voltage sense (see Note 1).
11	DIV	Divide enable pin. Tied high for normal operation. Allows selection of either divide by 2 mode or divide by 5 mode. See Table 1.
12	MOD	Sets clock division modulus for divide by 2 or 5 mode. See Table 1.
16	A=B	Sets AData equal to BData when asserted ('A=B' = 1). See Table 1.

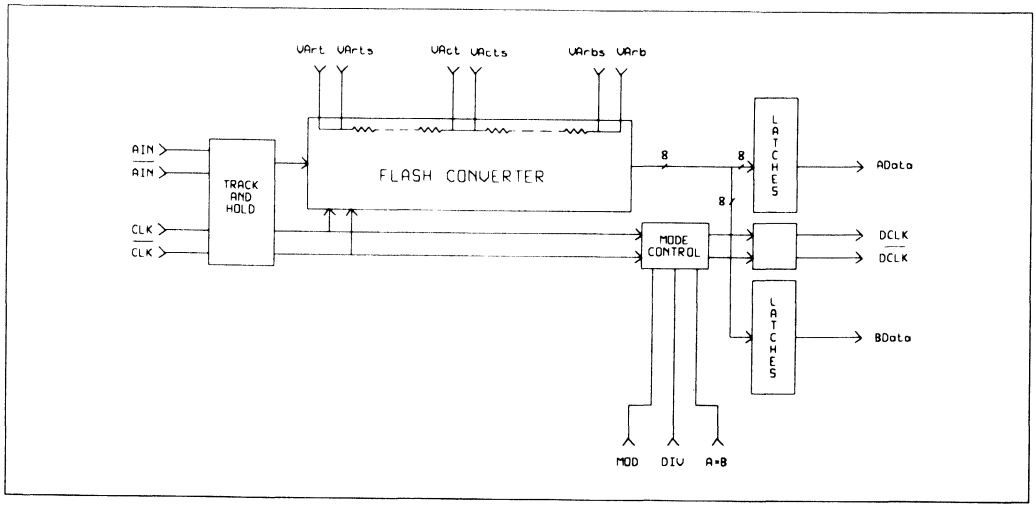
Pin #	Symbol	Comments
4,7,15,49, 57,60,64,67, 70,71,74,77, 78,79,82,84	GND	Power Supply Ground. Connect all pins (GND, DGND) see Note 3.
18,24,27, 30,34,40,46	DGND	Power supply ground. Connect all pins (GND, DGND) see Note 3.
8,21,43,56	VCC	Positive power supply, +5V nom.
32,69,80	VEE	Negative power supply, -5.2V nom.
5,6,9,10,31,33, 35,48,58,59, 63,81,83	NC	No internal connections to these pins.

Note 1: Reference bias supply - Use a separate high quality supply for these pins. Careful bypassing of these pins to achieve noise-free operation of the reference supplies contributes directly to achieving the high accuracy of the A/D.

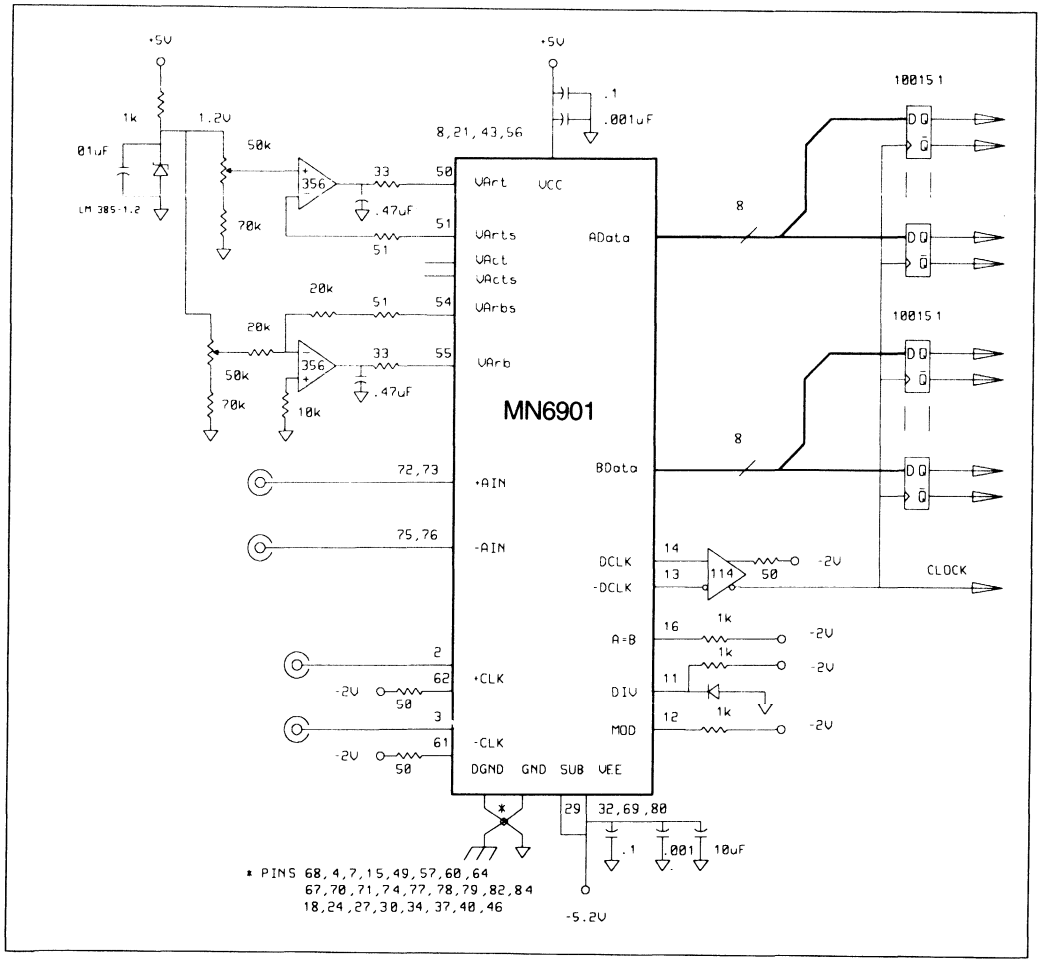
Note 2: The centertap connection of the A/D is normally left open. It can be driven with a bias voltage but care should be taken as outlined in Note 1.

Note 3: It is recommended that a multilayer circuit board be used with the MN6901 with a separate layer dedicated to ground. The GND and DGND connections should be made to separate areas in this ground plane (separated by at least 1/4 inch) and connected at only one location on the board (see typical connection diagram).

FUNCTIONAL DIAGRAM



TYPICAL CONNECTION DIAGRAM



DEFINITION OF TERMS

EFFECTIVE BITS

Dynamic accuracy of the MN6901 is expressed in effective bits. Effective bits is a measure of the signal to error ratio of an analog to digital conversion. Effective bits is expressed as the number of bits of an ideal, but lower resolution, A/D conversion with the same signal to error ratio. That is, the quantization error of the ideal converter equals the total error of the device. In addition to the ideal quantization error, other sources of error include all DC and AC non-linearities, clock and aperture jitter, missing output codes, and noise. Noise on references and supplies also degrades effective bits performance.

Effective bits is calculated from a digital record taken from the A/D under test. The input to the A/D is a sine wave filtered with an anti-aliasing filter to remove any harmonic content. The digital record taken from this signal is compared against a mathematically generated sine wave. DC offsets, phase and amplitude of the mathematical model are adjusted until a best fit sine wave is found. After subtracting this sine wave from the digital record the residual error remains. The rms value of the error is applied in the following equation to yield the A/D converter's effective bits.

$$\text{Eff. Bits} = N - \text{Log}_2\left(\frac{\text{measured rms error}}{\text{ideal rms error}}\right)$$

'N' is the resolution of the converter. In this case N = 8.

It is important to note at which frequency the measurement was made. The worst case error for any device will be at the converter's maximum clock rate with the analog input near the Nyquist rate (1/2 the input clock rate).

APERTURE WIDTH AND JITTER

Aperture width, and aperture jitter are performance indicators of the A/D converter. Each of these parameters will greatly affect the A/D's high frequency accuracy (see Figure 5). Aperture width is defined as the time that the track-and-hold circuit takes to disconnect the hold capacitor from the input circuit (i.e., to turn off the sampling bridge and put the T/H in its hold mode). Aperture jitter is defined as the uncertainty of the actual start point of the aperture width.

METASTABLE STATES

In a typical A/D converter, metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The output code resulting from this input voltage can have a large error and could result in a false full or zero scale output. Through innovative circuit design, Micro Networks has reduced the magnitude of this type of error in the MN6901 to one LSB, and reduced the probability of this occurring to less than one error every 10^{15} clock cycles. If the MN6901 were operated at 250 MHz, 24 hours per day, this would translate to one metastable state error every 50 days.

INTEGRAL LINEARITY ERROR

Integral Linearity Error (ILE) is the difference between the measured input voltage and the calculated input voltage for that output code. The calculated input voltage is determined from a straight line least squares fit for all transitions. ILE is expressed in terms of an LSB size.

$$\text{LSB} = \frac{1}{\text{slope of least squares fit line}}$$

$$\text{ILE (LSB)} = \frac{V_{MEAS} - V_{CAL}}{\text{LSB}}$$

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the difference between the measured LSB step and an ideal LSB step size between adjacent code transitions. DLE is expressed in LSBs and is calculated using the following equation:

$$\text{DLE (LSB)} = \frac{(V_{MEAS} - (V_{MEAS\,-1})) - \text{LSB}}{\text{LSB}}$$

$V_{MEAS\,-1}$ is the measured value of the previous code

A DLE error specification of <1 LSB guarantees that there are no missing codes and the transfer function is monotonic.

APPLICATION NOTES

POWER SUPPLIES/GROUNDS

The MN6901 is designed with separate analog and digital ground connections to isolate high current digital noise spikes. The high current digital ground is identified as DGND and is connected to the collector of the output emitter follower transistors. The low current ground connection is GND which is a combination of the analog ground and the low current decode section ground. The DGND and GND ground connections should be at the same DC level, and should be connected at only one location on the board. This will provide better noise immunity and allow the realization of this device's high accuracy.

The +5V supply as well as a -5.2V supply is needed for proper operation. Bypassing of the VEE and VCC supply pins to GND should be done with good quality 0.1uF and 0.001uF ceramic capacitors located as close to the package as possible.

CLK AND DCLK.

All clock signals, input and output, are differential. The input clocks, CLK and $\overline{CLK}$, are the primary timing signals for the MN6901, and are fed to the internal circuitry from one of two input groups, pins (2,3) or pins (62,61), through a 50 Ω transmission line. One set of CLK, $\overline{CLK}$ inputs should be driven and the other pair terminated by 50 Ω to -2V. Either set of inputs can be used as the driven inputs (input lines are balanced) for ease of circuit connection. A minimum pulse width t_{pwi} is required for the input clocks, CLK, $\overline{CLK}$, to ensure proper operation (see timing Figures 1 through 4).

To ensure optimum performance and repeatable results, a low phase jitter clock source should be used for CLK and $\overline{CLK}$. Phase jitter from the input clock source will reduce the converter's *effective bits* performance and cause inconsistent results.

DCLK, $\overline{DCLK}$ are output clock signals derived from the input clocks and are used for external timing of the data outputs AData and BData. The MN6901 is characterized to work with maximum input clock frequencies of 250MHz (see Table 1).

DATA FLOW

The MN6901 contains an internal Track and Hold (T/H) amplifier that stores the analog input voltage for the A/D to convert. The differential inputs, +AIN and -AIN, are tracked continuously between data samples. When a negative CLK is applied, the T/H enters the hold mode (see Figure 5). When CLK reaches the low state, the just acquired sample is presented to the A/D converter's input comparators. Internal processing of the sampled data takes additional clock cycles before it is available at the outputs AData or BData. All output data is timed from the output clocks, DCLK and $\overline{DCLK}$ (see Figures 1 through 4).

TRACK-AND-HOLD

As with all A/D converters, if the input waveform is changing rapidly at the time of conversion, the Effective Bits (EB) and Signal to Error Ratio (SER) will decrease. To avoid this problem, a Track-and-Hold (T/H) circuit was added internally to the MN6901. The T/H increases attainable effective bits performance and allows capture of analog data more accurately at high conversion rates.

The internal T/H circuit provides two important circuit functions for the MN6901. First, its nominal voltage gain of four (4) reduces the input driving signal to 270 mV (±135 mV differentially, normal conversion range assuming a ±1.02V reference). Secondly, the T/H provides a differential 50 Ω input allowing easy interfacing to this converter. Although the normal operating range is 270 mV, it can be operated with up to ±500 mV on each input with respect to ground. This extended input level includes the analog signal and any DC common mode voltage.

To obtain full scale digital output with differential input drive, a nominal 270 mV must be applied between +AIN and -AIN. That is, +AIN = +135 mV and -AIN = -135 mV (when no DC offset is applied). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero scale digital output code, with differential drive, occurs when +AIN = -135 mV and -AIN = +135 mV. The output of the converter stays at all ones (full scale) or all zeros (zero scale) when over or under ranged, respectively. Table 2 shows these relationships in a tabular form.

Single ended operation can be handled simply by applying a DC offset to, or by leaving open, one of the analog inputs (both +AIN and -AIN are terminated internally with 50 Ω to analog ground). Then drive one input with a ±270 mV + offset to obtain either full or zero scale digital output. If a DC common mode offset is to be applied, the total voltage swing allowed is ±500 mV (analog signal plus offset with respect to ground).

INPUT REFERENCE RESISTOR

The A/D converter's reference resistor is a Kelvin sensed, center tapped resistor string used to set the LSB size and dynamic operating range of the converter. Normally, the top and bottom of this string are driven with an op-amp, and the center tap left open. However, driving the center tap is an effective way to modify the output coding to provide a user defined bi-linear response. The buffer amplifier used to drive the top and bottom inputs will need to supply approximately 21 mA due to the resistor string impedance of 100 Ω minimum. A reference voltage of ±1.02V is normally applied to inputs VA_{RT} and VA_{RB}. This reference controls the comparators' input windows and can be adjusted up to ±1.4V to accommodate extended input requirements (accuracy specifications are guaranteed with references of ±1.02V). The reference inputs VA_{RTS}, VA_{RBS}, VA_{CTS} allow Kelvin sensing of the applied voltages for precise setting of the resistor chain.

An R-C network at the A/D converter's reference terminals is needed for optimum operation. This network consists of a 33 Ω resistor connected in series with the op-amp output that drives the reference. A 0.47uF capacitor must be connected near the resistor at the output of the op-amp (see typical connection diagram). This resistor and capacitor combination should be located within 0.5 inches of the MN6901 package. Any noise on these pins will directly affect the code uncertainty and degrade the effective bits performance of the A/D.

OUTPUT MODE CONTROL

DIV, MOD, and A=B are input pins that determine the operating mode of the two output data paths. Six options are available, but the normal operating configuration (8:16 demux mode) is set by 1 0 0 on the DIV, MOD, and A=B inputs, respectively (see Tabel 1). This will give the most recent sample at AData with the older data on BData; both outputs are synchronous and are at half the input clock rate. As with any ECL input, proper level setting (1 or 0) is necessary. To terminate these inputs use a 1kΩ or less resistor to -2V or the Thevinin resistor combination from DGND to -5.2V. When using a diode pull-up to tie an input in the "high" state, it is recommended that the diode be biased "on" with a pull-down resistor to avoid input voltage excursions close to ground. These inputs are compatible with standard ECL 10KH logic levels over temperature.

TABLE 1 — OUTPUT MODE CONTROL

DIV	MOD	A=B	DCLK*	Description
				(Divide by 1 mode)
0	X	0	250 MHz	Data appears on AData only. BData port inactive (see Figure 3).
0	X	1	250 MHz	AData identical to BData (see Figure 3).
				(Divide by 2 mode)
1	0	0	125 MHz	8:16 demux mode. AData and BData ports are active. BData carries older sample and AData carries most recent sample (see Figure 4).
1	0	1	125 MHz	AData and BData ports are active, both carry identical sampled data. Alternate samples are taken but discarded.
				(Divide by 5 mode)
1	1	0	50 MHz	AData port updates data on 5th input CLK. BData port inactive. Other 4 sampled data points are discarded.
1	1	1	50 MHz	AData and BData ports are both active with identical data. Data is updated on output ports every 5th input clock (CLK). The other 4 samples are discarded.

* Input clocks (CLK, $\overline{CLK}$) = 250 MHz for all above combinations.

In divide by 2 or 5 mode the output clock DCLK will always be a 50% duty cycle signal. In divide by 1 mode DCLK will have the same duty cycle as CLK.

TABLE 2 — INPUT VOLTAGE RANGE

Input	+AIN**	-AIN**	Output Code MSB to LSB	
	+135 mV	-135 mV	1 1 1 1 1 1 1 1	full scale
Differential	0	0	1 0 0 0 0 0 0 0	mid scale
	-135 mV	+135 mV	0 0 0 0 0 0 0 0	zero scale
	+270 mV	0	1 1 1 1 1 1 1 1	full scale
Single Ended	0	0	1 0 0 0 0 0 0 0	mid scale
	-270 mV	0	0 0 0 0 0 0 0 0	zero scale

** An offset V_{10}, as specified in the DC electrical parameters, will be present at the input. Compensate for this offset by either adjusting the reference voltage, VA_{Rt}, VA_{Rb}, or introduce an offset voltage in one of the input terminals +AIN or -AIN.

Figure 1. **Output Timing: Divide by 1 (fast mode)**

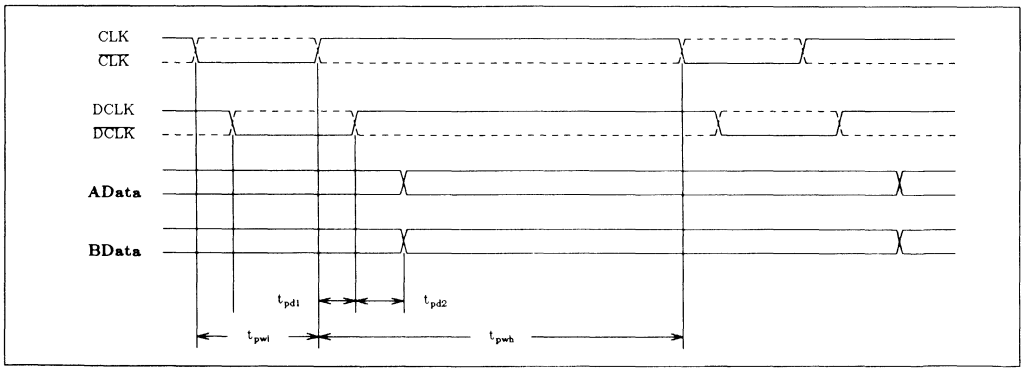
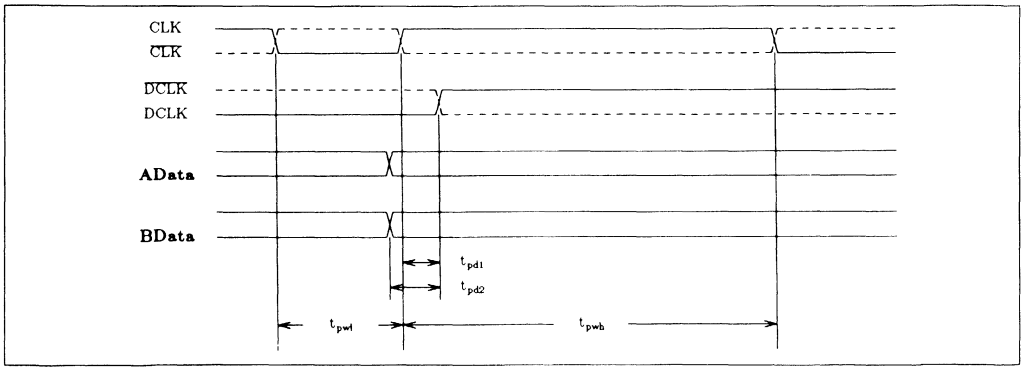


Figure 2. **Output Timing: Divide by 2 or 5 mode (DIV =1)**



Note: In the divide by 2 mode DCLK will be at 1/2 the CLK rate. When in the divide by 5 mode there will be one DCLK pulse for every 5 CLK clock pulses.

Figure 3. **Output Timing: Clock to Data, Divide by 1 (fast mode DIV=0)**

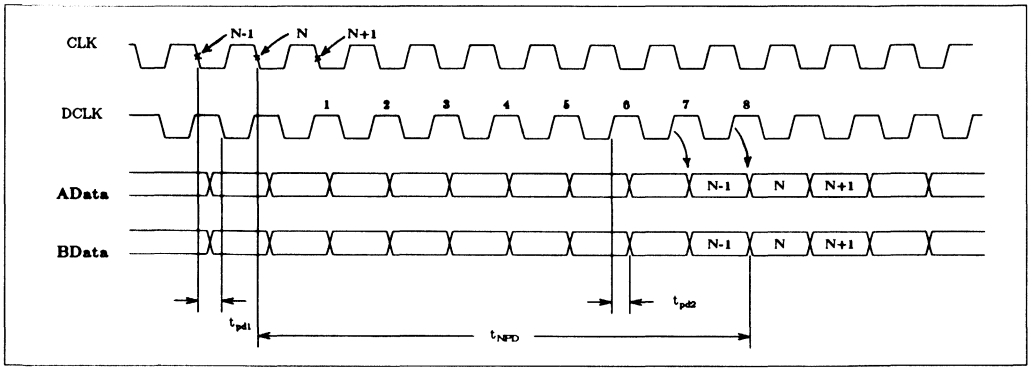
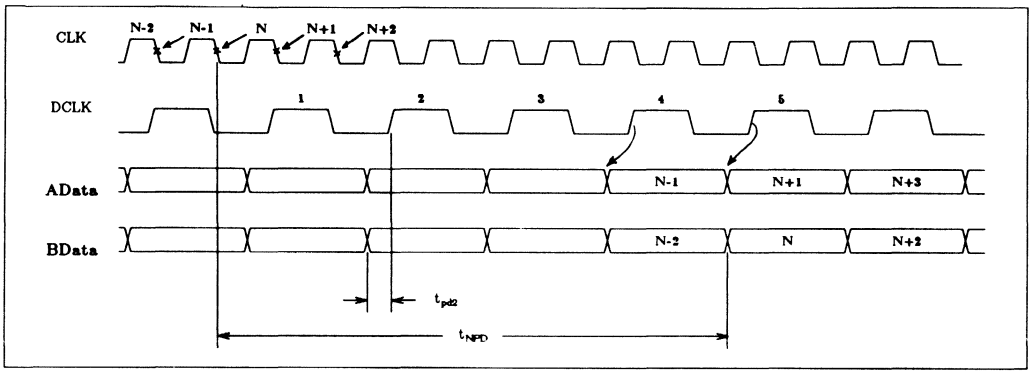
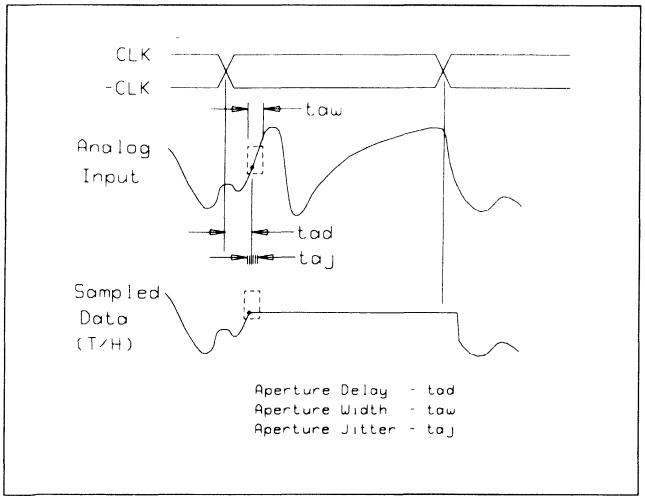


Figure 4. **Output Timing: Divide by 2 mode (DIV=1)**



Note: Sampling occurs on the falling edge of CLK. Data appearing at AData and BData is updated on the rising edge of DCLK (plus tpd_2).

Figure 5. **T/H Aperture Timing**



MN6901

Figure 6.

Integral Linearity Error (LSB's) vs Output Code

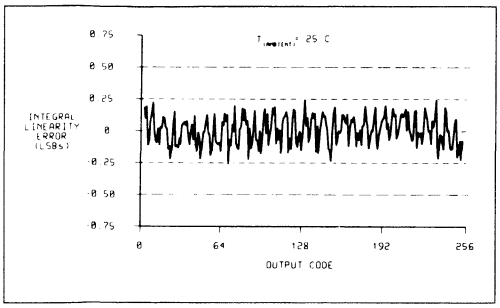


Figure 7.

Differential Linearity Error (LSB's) vs Output Code

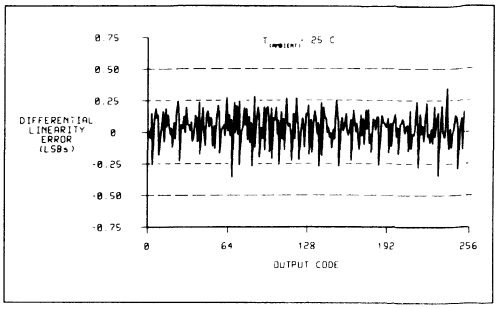


Figure 8. FFT.

F_{CLK} = 250 MHz, F_{AIN} = 120.4462 MHz

SER = -42.3 dB, Noise floor = -65.4 dB

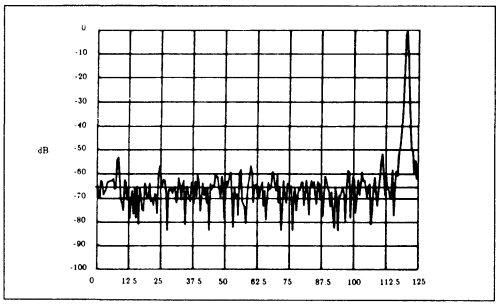


Figure 9. FFT.

F_{CLK} = 250 MHz, F_{AIN} = 10.4462 MHz

SER = -45.87 dB, Noise floor = -68.5 dB

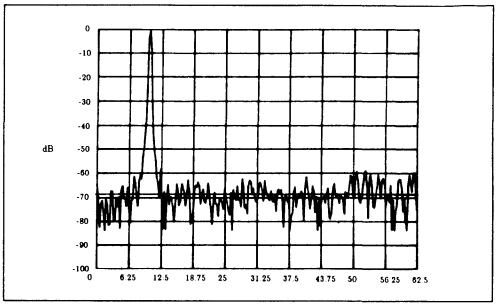


Figure 10. **Effective Bits vs Frequency (F_{AIN})**

F_{CLK} = 250 MHz, V_{IN} = 95% FS

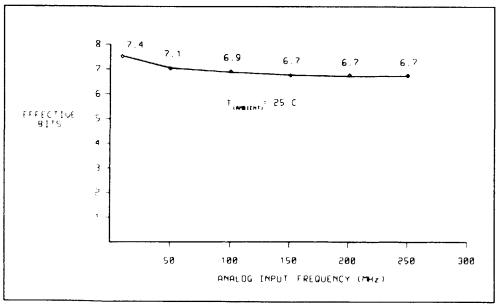


Figure 11. **Effective Bits vs Frequency (F_{CLK})**

F_{AIN} = 10.4 MHz, V_{IN} = 95% FS

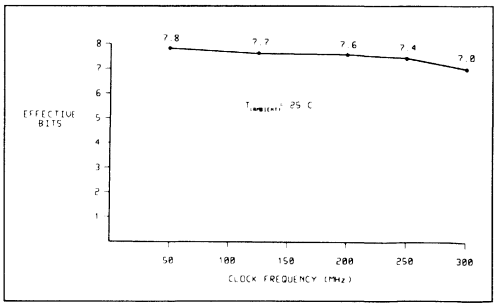


Figure 12. **Effective Bits vs Frequency (F_{AIN})**

T_C = 80°C, F_{CLK} = 250 MHz, V_{IN} = 95% FS

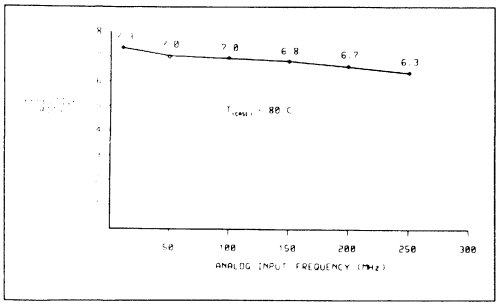


Figure 13. **Effective Bits vs Frequency (F_{AIN})**

T_C = -15°C, F_{CLK} = 250 MHz, V_{IN} = 95% FS

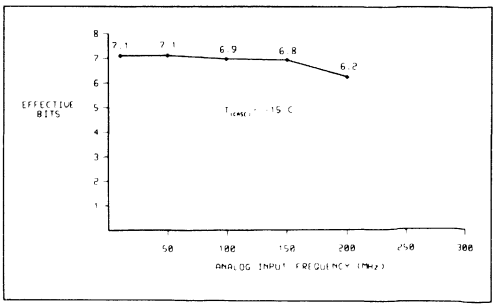


Figure 14. **CLK, DCLK, $\overline{\text{DCLK}}$, F_{CLK} = 250 MHz**
Divide by one mode.,
Vertical = 500mV/div, Horizontal = 1ns/div

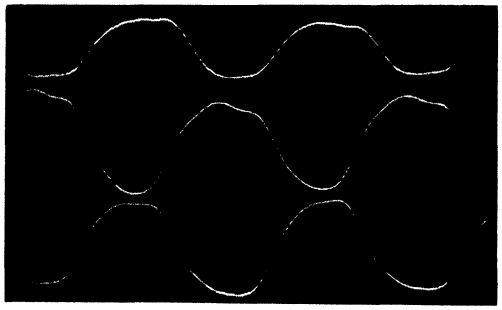


Figure 15. **DCLK, t_r = 710 ps**
Vertical = 200mV/div, Horizontal = 500 ps/div

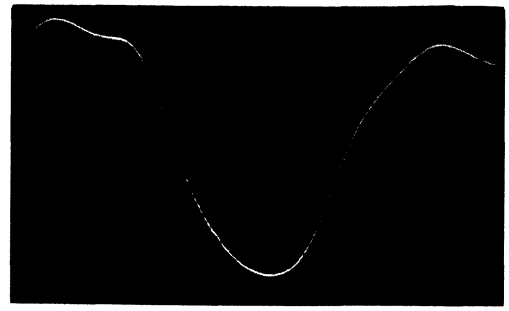
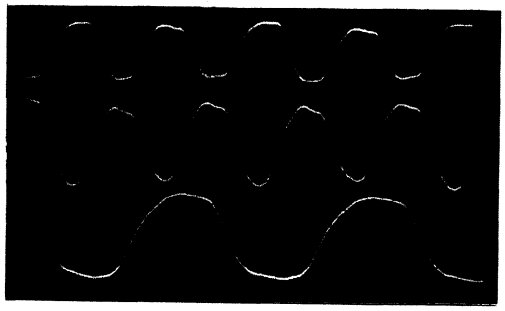
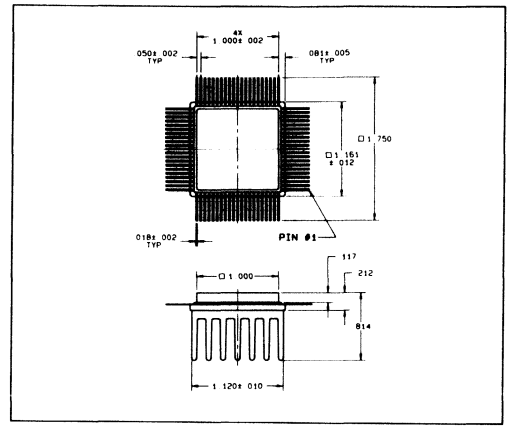
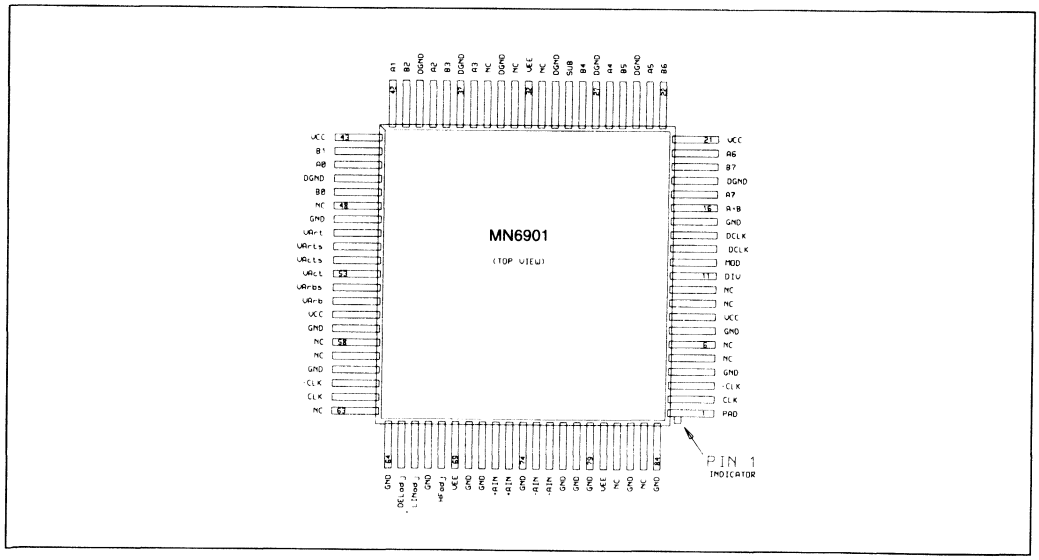


Figure 16. **CLK, DCLK, AData, F_{CLK} = 250 MHz**
Divide by one mode
Vertical = 500 mV/div, Horizontal = 2ns/div







MN6901



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Analog-to-Digital Converters

Analog-to-Digital Converters

Since its inception, Micro Networks has continually contributed to advancing the leading edge of DIP-packaged, high-speed, high-resolution A/D conversion technology. As detailed in the History section at the beginning of this catalog, we lay claim to a long list of industry firsts. Recent years have seen the introduction of a 16-bit, 17μsec extended-temperature range A/D (MN5295/5296), a 12-bit, 400nsec A/D converter (MN5249), and many 12 and 16-bit sampling A/D converters (MN6249, MN6400, MN6405).

The four products listed below are the first in a series of high-speed 6 and 8-bit CMOS monolithic Flash A/D converters. The MN5902 and MN5908 are 8-bit, 20MHz and 15MHz devices. Two 6-bit devices, the MN5906 and MN5909, convert at an impressive 50MHz and 100MHz and consume less than 200mW of power.

Micro Networks is a recognized leading supplier of high-speed, high-resolution A/D converters for military/aerospace applications, and we currently supply products to more than 50 missile, aircraft and satellite programs. Most of our A/D converters are available specified for extended temperature range operation, in hermetically sealed packages. Additionally, these devices are available with optional Environmental Stress Screening (H/B models) or compliant with MIL-H-38534 requirements. Our complete line of high-performance A/D converters is complimented by a complete line of compatible, high-performance track-hold (T/H) amplifiers (see Section 8), and we also offer a growing line of sampling A/D converters (see Section 5).

MN5902
MN5908

8-Bit
CMOS Flash A/D
Converters

FEATURES

- 20MHz (MN5902)
  15MHz (MN5908)
- Single +5V Supply Operation
- Low Harmonic Distortion
- 3-State Outputs
- Easy Cascading to 9 Bits
- Low 350mW Power Consumption
- Small 24-Pin DIP
- −55°C to +125°C Operating Temperature Range
- Optional Environmental Stress Screening

MN5906

6-Bit, 50MHz
CMOS Flash A/D
Converter

FEATURES

- 6-Bit Resolution Plus Overflow Bit
- 50MHz Typical Conversion Rate
- Single +5V Operation
- Low Input Capacitance
- Low Power (190mW, typ.)
- Small 18-Pin Ceramic or Plastic DIP
- 3-State Outputs
- Optional Environmental Stress Screening

MN5909

6-Bit, 100MHz
CMOS Flash A/D
Converter

FEATURES

- 6-Bit Resolution Plus Overflow Bit
- 100MHz Typical Conversion Rate
- Single +5V Operation
- Low Input Capacitance
- Low Power (200mW, Typical)
- Externally-Strobed, Auto-Zeroed Comparators
- Small 20-Pin Ceramic or Plastic DIP
- 3-State Outputs
- Optional Environmental Stress Screening

Analog-to-Digital Converters

Resolution	Model Number	Maximum Conversion Time (μsec) (1)	Internal Clock	Specified Temperature Range (°C)	Maximum Linearity Error (%FSR)	Guaranteed No Missing Codes Over Temperature	Power (mW)	DIP Package (Pins)	Hi-Rel Option	DESC SMD 5962-	Page No.
16-Bits	MN5295 MN5296	17	Yes	0 to +70 −55 to +125	±0.003 ±0.006	Yes (2) Yes (3)	945	32	Yes	8956901	6-135
	MN5290 MN5291	40	Yes (2)	0 to +70 −55 to +125	±0.003 ±0.006	Yes (2) Yes (3)	810	32	Yes	8956301	6-127
	MN5284 Series	50	Yes	0 to +70	±0.003	Yes (4)	255	32	No	N.A.	6-119
12-Bits	MN5249	0.4	Note 6	0 to +70 −55 to +125	±0.024	Yes	2820	40	Yes	Note 5	6-109
	MN5245 MN5246	0.85	Note 6	0 to +70 −55 to +125	±0.024	Yes	2635	40	Yes	89595 01-03	6-99
	MN5240	5	Yes	0 to +70 −55 to +125	±0.012	Yes	1400	32	Yes	Note 5	6-93
	MN774	8	Yes	0 to +70 −55 to +125	±0.012	Yes	325	28	Yes	Note 5	6-39
	ADC84	8	Yes	0 to +70 −25 to +85	±0.012	Yes	975	32	No	N.A.	6-11
	ADC85	8	Yes	0 to +70 −25 to +85	±0.012	Yes	975	32	No	N.A.	6-11
	ADC87	8	Yes	−25 to +85 −55 to +125	±0.012	Yes	1110	32	Yes	8850802	6-17
	MN5210 Series	13	No	0 to +70 −55 to +125	±0.012	Yes	845	24	Yes	89584 01-07	6-85
	MN674A	15	Yes	0 to +70 −55 to +125	±0.012	Yes	325	28	Yes	Note 5	6-31
	ADC80	25	Yes	−25 to +85	±0.012	Yes	593	32	No	N.A.	6-5
	MN574A	25	Yes	0 to +70 −55 to +125	±0.012	Yes	325	28	Yes	8512702	6-23
	MN5200 Series	50	No	0 to +70 −55 to +125	±0.012	Yes	845	24	Yes	89583 01-07	6-77
	MN5250 Series	175	No	0 to +70 −55 to +125	±0.012	Yes	56	24	Yes	Note 5	6-115
8-Bits	MN5902	0.050 20MHz	Note 6	0 to +70 −55 to +125	±0.4	Yes	350	24	Yes	Note 5	6-149
	MN5908	0.067 15MHz	Note 6	0 to +70 −55 to +125	±0.4	Yes	350	24	Yes	Note 5	6-177
	MN5825	1	Yes	0 to +70 −55 to +125	±0.2	Yes	925	24	Yes	Note 5	6-143
	MN5101 MN5100	0.9 1.5	No	0 to +70 −55 to +125	±0.2	Yes	1125	24	Yes	Note 5	6-51
	MN5160	2	No	0 to +70 −55 to +125	±0.2	Yes	890	24	Yes	Note 5	6-71
	MN5130 Series	2.5	No	0 to +70 −55 to +125	±0.2	Yes	680	18	Yes	Note 5	6-57
	MN5140 Series	2.5	No	0 to +70 −55 to +125	±0.2	Yes	680	18	Yes	Note 5	6-57
	MN5150	2.5	No	0 to +70 −55 to +125	±0.2	Yes	680	24	Yes	Note 5	6-65
	MN5120 Series	6	No	0 to +70 −55 to +125	±0.2	Yes	680	18	Yes	Note 5	6-57
	MN5065 MN5066	100	No	0 to +70 −55 to +125	±0.2	Yes	53	18	Yes	Note 5	6-47

Continued on next page.

Analog-to-Digital Converters (continued from previous page)

Resolution	Model Number	Maximum Conversion Time (μsec) (1)	Internal Clock	Specified Temperature Range (°C)	Maximum Linearity Error (%FSR)	Guaranteed No Missing Codes Over Temperature	Power (mW)	DIP Package (Pins)	Hi-Rel Option	DESC SMD 5962-	Page No.
6-Bits	MN5909	0.010 100MHz	Note 6	0 to +70	±1.6	Yes	200	20	Note 7	Note 5	6-185
	MN5903 MN5903A	0.014 70MHz	Note 6	0 to +70 −25 to +85 −55 to +125	±1.4	Yes	693	16	Yes	Note 5	6-157
	MN5904 MN5905	0.014 70MHz	Note 6	0 to +70 −25 to +85 −55 to +125	±1.4	Yes	536	16	No	N.A.	6-163
	MN5906	0.020 50MHz	Note 6	0 to +70 −55 to +125	±1.6	Yes	190	18	Note 7	Note 5	6-169

NOTES:

1. For models with an external clock, the table shows the minimum conversion time that will result in specified accuracy. For units with internal clock, maximum conversion time is listed.
2. No missing codes for 14 bits guaranteed over temperature.
3. No missing codes for 13 bits guaranteed over temperature.
4. No missing codes for 15 bits guaranteed over temperature.
5. Contact factory for information regarding DESC SMD's for these device types.
6. The conversion technique does not require a clock.
7. Contact the factory for availability information.

✓ Indicates New Product.

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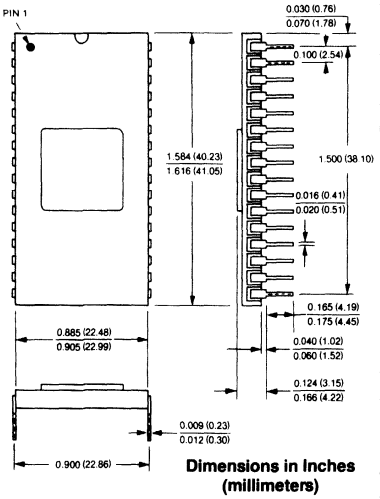
ADC80

LOW-COST, MONOLITHIC
10 and 12-Bit
A/D CONVERTERS

FEATURES

- **Low-Cost Single-Chip Design**
- **Complete with Internal Clock, Comparator and Reference**
- **−25°C to +85°C Operation**
- **± ½ LSB Linearity and No Missing Codes Guaranteed**
- **Maximum Conversion Time: 25μsec 12 Bits 22μsec 10 Bits**
- **5 User-Selectable Input Voltage Ranges**
- **Serial and Parallel Outputs**
- **±12V to ±15V Supplies**
- **705mW Maximum Power Consumption**
- **Standard 32-Pin Hermetic DIP**
- **Multisourced**

32 PIN SIDE BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

Micro Networks ADC80 is a complete, single-chip, 12-bit, successive approximation A/D converter that includes on-chip clock, reference and comparator. 12-bit units (add "-12" suffix to part number) perform a complete conversion in 25μsec. Devices specified for 10-bit performance (add "-10" suffix to part number) perform a short-cycled 10-bit conversion in 22μsec. Both are packaged in standard, 32-pin, side-brazed ceramic dual-in-lines, and both guarantee ± ½ LSB integral linearity and "no missing codes" for their respective resolutions.

These TTL-compatible A/D's feature internal input scaling resistors that provide 5 user-selectable input ranges (0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V). Functionally trimmed thin-film resistors ensure that all published accuracy and linearity specifications are met without the need for additional external adjustments. User-optional gain and offset adjust points are provided, however, for critical applications requiring the highest accuracies. Units may be driven from the internal clock or from an external system clock, and short cycling may be used to reduce conversion times for applications in which fewer than 12 bits are required. Output data is complementary binary coded and appears in both serial and parallel formats.

Low cost, multisource availability and guaranteed performance have made the ADC80 the designer's choice for most 10 or 12-bit commercial and industrial applications. Devices operate from ±12V to ±15V supplies and also require a +5V logic supply. Power consumption is 705mW maximum, and unlike earlier hybrid versions of this device, a +5V analog supply is no longer required. Similarly, the "Z" suffix on the part number is no longer required for ±12V operation as all devices now operate from either ±12V or ±15V supplies.

Model	Integral Linearity (%FSR)	No Missing Codes	Power Supplies
ADC80-12	±0.012	12 Bits	±12V/±15V, +5V
ADC80-10	±0.049	10 Bits	±12V/±15V, +5V

April 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

ADC80 LOW-COST MONOLITHIC 10 and 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+V_{CC}, Pin 17)	−0.5 to +18 Volts
Negative Supply (−V_{CC}, Pin 25)	+0.5 to −18 Volts
Logic Supply (+V_{dd}, Pin 9)	−0.5 to +7 Volts
Analog Inputs (Pins 13 and 14)	±16.5 Volts
Digital Inputs (Pins 18, 19, 20 and 21)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— **ADC80-12**

Select "-10" for guaranteed 10-bit performance or "-12" for guaranteed 12-bit performance.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±12V or ±15V +Vdd = +5V unless otherwise indicated) (Note 1)

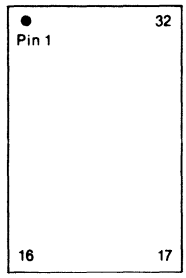
ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 0 to +10 ±2.5, ±5, ±10		Volts Volts
Input Impedance: 0 to +5V, ±2.5V 0 to +10V, ±5V ±10V		2.5 5 10		kΩ kΩ kΩ
DIGITAL INPUTS (Note 2)				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.7V) Logic "0" (V_{IL} = +0.4V)			+20 −20	μA μA
TRANSFER CHARACTERISTICS (Note 4)				
Integral Linearity Error (Note 5): "-12" Devices "-10" Devices		±0.006 ±0.024	±0.012 ±0.049	%FSR %FSR
Integral Linearity Drift		±1	±3	ppm of FSR/°C
Differential Linearity Error (Note 5): "-12" Devices "-10" Devices		±1/2 ±1/2		LSB LSB
Differential Linearity Drift: "-12" Devices "-10" Devices		±2 ±5		ppm of FSR/°C ppm of FSR/°C
No Missing Codes Guaranteed −25°C to +85°C: "-12" Devices "-10" Devices	 12 10			 Bits Bits
Unipolar Offset Error (Notes 6, 7): Initial (+25°C) Drift		±0.05 ±3	±0.2	%FSR ppm of FSR/°C
Bipolar Offset Error (Notes 6, 8): Initial (+25°C) Drift		±0.1 ±7	±0.3 ±15	%FSR ppm of FSR/°C
Gain Error (Notes 6, 9): Initial (+25°C) Drift		±0.1 ±15	±0.3 ±30	% ppm of FSR/°C
DIGITAL OUTPUTS (Note 3)				
Output Coding (Note 10): Unipolar Ranges Bipolar Ranges		CSB COB, CTC		
Logic Levels: Logic "1" ($I_{SOURCE} \leq 80\mu A$) Logic "0" ($I_{SINK} \leq 3.2mA$)	+2.4		 +0.4	Volts Volts
REFERENCE OUTPUT				
Internal Reference: Voltage Accuracy Tempco External Current		+6.3 ±1 ±10	 200	Volts % ppm/°C μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 11): "-12" Devices "-10" Devices		22 19	25 22	μsec μsec
Internal Clock Frequency		556		kHz
Start Convert Positive Pulse Width (Note 11)	0.1		20	μsec

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: $+V_{CC}$ Supply	+11.4	+15	+16.5	Volts
$-V_{CC}$ Supply	−11.4	−15	−16.5	Volts
$+V_{dd}$ Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection: $+V_{CC}$ Supply		±0.003		%FSR/%Supply
$-V_{CC}$ Supply		±0.003		%FSR/% Supply
$+V_{dd}$ Supply		±0.002		%FSR/% Supply
Current Drains: $+V_{CC}$ Supply		+8.5	+11	mA
$-V_{CC}$ Supply		−21	−24	mA
$+V_{dd}$ Supply		+30	+36	mA
Power Consumption		593	705	mW

SPECIFICATION NOTES:

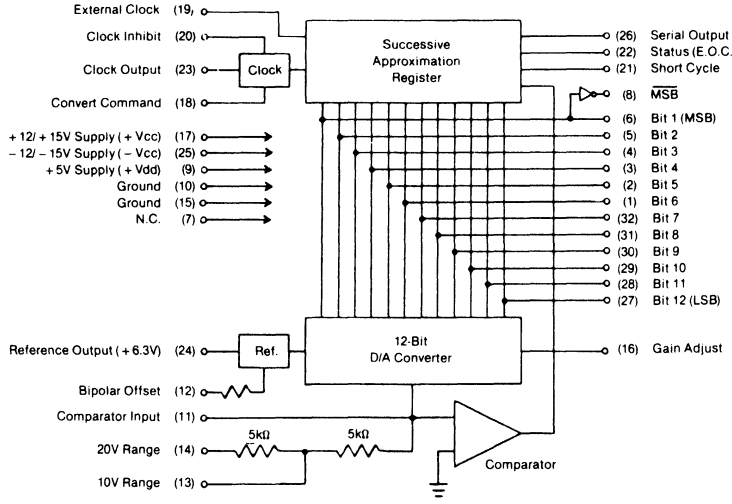
1. Unless otherwise indicated, all specifications apply for both 10-bit and 12-bit versions.
2. Digital inputs include Start Convert, External Clock Input, Clock Inhibit and Short Cycle.
3. Digital outputs include Parallel Data, Serial Data, Status and Clock Output.
4. FSR = full scale range. A unit connected for ±10V operation has a 20V FSR. A unit connected for 0 to +10V or ±5V operation has a 10V FSR etc.
5. For a 12-bit converter, 1LSB = 0.024% FSR and ±0.012% FSR = ± ½LSB. For a 10-bit converter, 1LSB = 0.098% FSR and ±0.049% FSR = ± ½LSB. ADC80 "-10" and "-12" devices both have 12 output data bits. "-12" devices guarantee true 12-bit performance while "-10" devices guarantee the equivalent of 10-bit performance.
6. Initial offset and gain errors are adjustable to zero with optional external potentiometers.
7. Unipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition occurs when operating on a unipolar input range.
8. Bipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition occurs when operating on a bipolar input range.
9. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
10. CSB = complementary straight binary. COB = complementary offset binary. CTC = complementary two's complement. CTC coding is achieved using the $\overline{MSB}$ output. Coding applies for both serial and parallel outputs. CTC coding not available for serial output.
11. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Conversion is initiated on the rising edge of the Start Convert command. Listed conversion times apply for internal clock. See Timing Diagram.

PIN DESIGNATIONS



1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB)
7	N.C.	26	Serial Output
8	Bit 1 ($\overline{MSB}$)	25	−12/−15V Supply (−V_{CC})
9	+5V Supply (+V_{dd})	24	Reference Output (+6.3V)
10	Ground	23	Clock Output
11	Comparator Input	22	Status (E.O.C.)
12	Bipolar Offset	21	Short Cycle
13	10V Range	20	Clock Inhibit
14	20V Range	19	External Clock
15	Ground	18	Convert Command
16	Gain Adjust	17	+12/+15V Supply (+V_{CC})

BLOCK DIAGRAM

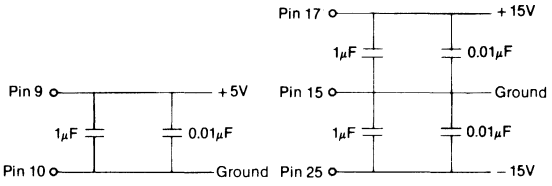


APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the ADC80. The units' two ground pins (pins 15 and 10) are not connected to each other internally and must be tied together as close to the package as possible, preferably to a large analog ground plane underneath the package. If these commons must be run separately, a non-polarized 0.01μF to 0.1μF bypass capacitor should be connected between pins 10 and 15 as close to the unit as possible and wide conductor runs employed.

Coupling between the analog inputs and digital signals should be minimized to avoid noise pickup. Pin 11, the high impedance input to the internal comparator, is particularly susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing the comparator input. In bipolar operation, where pin 11 is connected to pin 12, a short jumper should be used, and for external offset adjustment, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the ADC80. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be connected as shown below. An additional 0.01μF ceramic bypass capacitor should be located close to the package connecting Gain Adjust (pin 16) to ground.



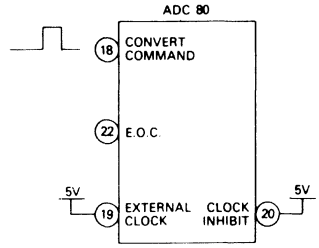
END OF CONVERSION—During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of the clock pulse "h + 1". Therefore, a complete conversion requires 13 clock pulses with the Status (E.O.C.) output dropping from logic "1" to logic "0" shortly after the falling edge of the 13th clock pulse. Parallel data is valid and ready to be read when Status falls. This allows direct use of Status for latching parallel data.

CLOCK OUTPUT—The internal 556kHz clock is brought out (pin 23) and will drive up to two standard TTL loads. The internal clock is stopped at the end of each conversion and remains low until a new conversion is initiated.

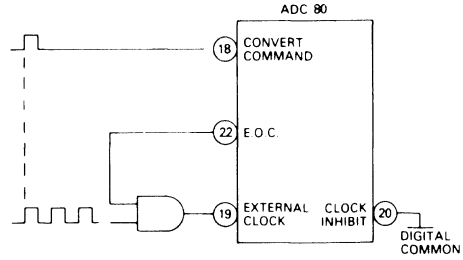
SERIAL DATA OUTPUT—Serial data is available (pin 26) in non-return-to-zero format. Timing for the serial output is shown on the Timing Diagram.

REFERENCE OUTPUT—The internal 6.3V reference (pin 24) will drive loads up to 30k ohms, however it is recommended that this output be buffered before use.

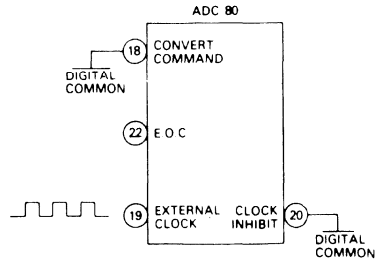
NORMAL OPERATION—For normal operation, a positive input pulse (100nsec minimum, 20μsec maximum pulse width) is applied to the Convert Command input as shown. The rising edge of the Convert Command will start the internal clock and initiate conversion. The Convert Command input must return low before the E.O.C. output returns low indicating the end of the conversion period. The External Clock and Clock Inhibit inputs must be tied high for normal operation.



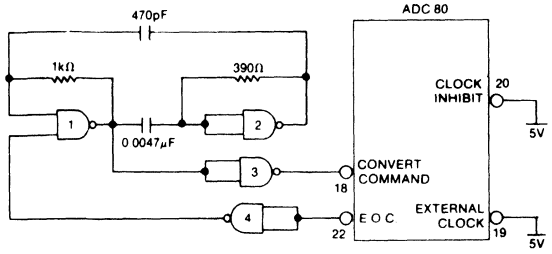
OPERATION WITH EXTERNAL CLOCK—The external clock is connected and gated as shown. The Convert Command input must be synchronized with the external clock signal and the Clock Inhibit input tied low, for proper operation.



CONTINUOUS CONVERSION WITH EXTERNAL CLOCK—For continuous conversion of the input signal, the Convert Command and Clock Inhibit inputs are tied low and an external clock applied to the Clock Input. The converter will then continuously convert, reset and initiate new conversions. The converter will be reset on the 13th clock pulse, and the subsequent conversion will be initiated by the 14th clock pulse. The output data will be valid when E.O.C. goes low and will remain valid until E.O.C. returns high.



CONTINUOUS CONVERSION WITH INTERNAL CLOCK—For continuous conversion of the input signal, the Clock Inhibit and External Clock pins are tied high. The conversion is initiated by the 14th clock pulse and the internal clock runs continuously. The oscillator formed by gates 1 and 2 insures that the conversion will start when logic power is turned on.



SHORT CYCLE FEATURE—The ADC80 may be operated at faster speeds if resolution of less than 12 bits is required. Connections for Short Cycle (pin 21) are shown in the following table:

RESOLUTION (BITS)	12	10	8
Connect Pin 21 to	Pin 9	Pin 28	Pin 30
Maximum Conversion Time Internal Clock (μsec) (Note 1)	25	22	18
Maximum nonlinearity at +25°C (% of FSR)	±0.012 (Note 2)	±0.048	±0.20

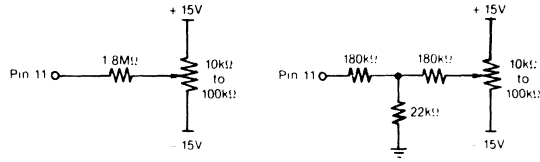
NOTES: (1) Max. conversion time to maintain ± ½ LSB linearity error.
(2) ADC80-12 model only.

INPUT VOLTAGE CONNECTIONS—The analog input voltage ranges of the ADC80 are user selectable by external pin connections as shown in the adjacent table.

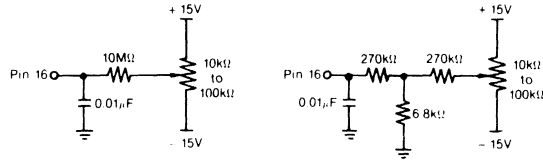
INPUT SIGNAL	CONNECT INPUT SIGNAL TO PIN	CONNECT PIN 12 TO PIN	CONNECT PIN 14 TO PIN
±10V	14	11	Input Sig.
±5V	13	11	Open
±2.5V	13	11	Pin 11
0 to +5V	13	15	Pin 11
0 to +10V	13	15	Open

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 11 should be connected as described in the Input Voltage Connections section, and pin 16 should be left open.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition is idealy supposed to occur (see Output Coding Table). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply the input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off.



DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Outputs
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB LSB
+5.0000	+10.0000	+2.5000	+5.0000	+10.0000	0000 0000 0000
+4.9982	+9.9963	+2.4982	+4.9963	+9.9927	0000 0000 000Ø*
+2.5006	+5.0012	+0.0006	+0.0012	+0.0024	0111 1111 111Ø*
+2.4994	+4.9988	−0.0006	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+2.4982	+4.9963	−0.0018	−0.0037	−0.0073	1000 0000 000Ø*
+0.0006	+0.0012	−2.4994	−4.9988	−9.9976	1111 1111 111Ø*
0.0000	0.0000	−2.5000	−5.0000	−10.0000	1111 1111 1111

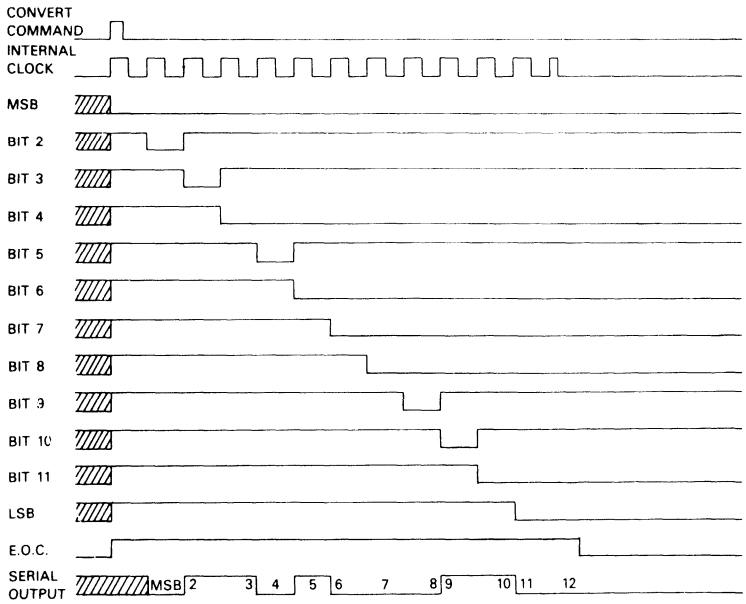
DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary.
2. For bipolar input ranges, output coding is complementary offset binary or complementary two's complement if $\overline{MSB}$ output is used.
3. For 0 to +5V or ±2.5V input ranges, 1LSB for 12 bits = 1.22mV. 1LSB for 10 bits = 4.88mV.
4. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 10 bits = 9.77mV.
5. For 0 to +20V or ±10V input ranges, 1LSB for 12 bits = 4.88mV. 1LSB for 10 bits = 19.53mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADC80-12 operating on its ±10V input range, the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9976 Volts. Subsequently, any input voltage more negative than −9.9976 Volts will give a digital output of all "1's". The transition from digital output 0111 1111 1111 to 1000 0000 0000 will ideally occur at an input of −0.024 Volts, and the 0000 0000 0000 to 0000 0000 0001 transition should occur at +9.9927 Volts. An input more positive than +9.9927 Volts will give all "0's".

TIMING DIAGRAM



DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time: 12-Bits		22	25	μsec
10-Bits		19	22	μsec
Clock Delay from Convert Command		153		nsec
Clock Period		1.81		μsec
Clock Pulse Width (High)		0.87		μsec
Status Delay from Convert Command		186		nsec
All Bits Reset Delay from Convert Command		141		nsec
Data Valid Time from Clock Pulse High		−15		nsec

MICRO NETWORKS

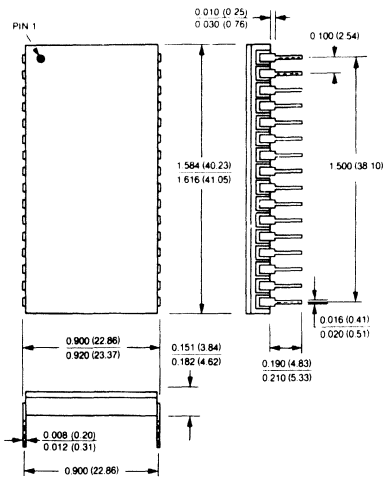
ADC84
ADC85

HIGH-SPEED, 12-Bit
A/D CONVERTERS

FEATURES

- **Fast Conversion Times:**
  8μsec max. for 12 Bits
  5μsec max. for 10 Bits
- **± ½ LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Complete:**
  Internal Reference
  Internal Clock
  User-Optional Input Buffer
- **Versatile:**
  5 Input Voltage Ranges
  Serial and Parallel Outputs
  4 Output Coding Formats
  Short-Cycle Capability
  Variable Clock
- **Small 32-Pin DIP**

32 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

ADC84 and ADC85 are high-speed, 12-bit, successive approximation analog-to-digital converters. Each is complete with internal reference, clock and input buffer amplifier and is extremely versatile offering 5 user-selectable input ranges, short cycling capability, parallel and serial outputs, a status output for easy interfacing in microprocessor-based applications, and an internal clock with the option of using an external clock.

Models are available in both 10 and 12 bit linearities for either 0°C to +70°C or −25°C to +85°C operation. No clock adjusting is necessary to achieve the guaranteed 8μsec maximum conversion time (for 12 bits), and "no missing codes" is guaranteed over temperature.

The Micro Networks ADC84 and ADC85 series of 12-bit A/D converters are direct pin-for-pin replacements for industry-standard ADC84 and ADC85 converters and offer faster conversion times, lower power consumption and guaranteed "no missing codes".

ADC84 and ADC85 series devices are excellent choices for high-speed applications in commercial/industrial OEM designs. They are particularly well suited for high-speed, multichannel, simultaneous sampling or sequential, data acquisition systems.

For example, ADC84 or ADC85 can be combined with an MN376 high-speed T/H amplifier and an industry-standard 508 type CMOS multiplexer to create a multichannel DAS with a scan rate greater than 100,000 channels/sec. In DSP-type applications, ADC84 or ADC85 can be configured with MN376 to create a 100kHz-plus digitizer with a 50kHz input bandwidth that will typically produce signal-to-noise ratios greater than 70dB with harmonics more than 80dB down.

Model Number	Linearity Error (%FSR)	Specification Temp. Range	Gain Drift (ppm/°C)
ADC84-10	±0.048	0°C to +70°C	±30
ADC84-12	±0.012	0°C to +70°C	±30
ADC85C-10	±0.048	0°C to +70°C	±40
ADC85C-12	±0.012	0°C to +70°C	±25
ADC85-10	±0.048	−25°C to +85°C	±20
ADC85-12	±0.012	−25°C to +85°C	±15

April 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

ADC84 ADC85 HIGH-SPEED 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
ADC84-10, ADC84-12	0°C to +70°C
ADC85C-10, ADC85C-12	0°C to +70°C
ADC85-10, ADC85-12	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 28)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 31)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 16)	−0.5 to +7 Volts
Digital Inputs (Pins 14, 21)	−0.5 to +5.5 Volts
Analog Inputs (Pins 24, 25)	±25 Volts
Buffer Input (Pin 30)	±15 Volts

ORDERING INFORMATION

PART NUMBER **ADC8XX-XX**
Select ADC84, ADC85C or ADC85 for desired performance and specified temperature range.
Select -10 or -12 for desired resolution and linearity error.

SPECIFICATIONS ALL UNITS (Typical at T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 13)

MODEL	ADC84 -10	ADC84 -12	ADC85C -10	ADC85C -12	ADC85 -10	ADC85 -12	UNITS
ANALOG INPUTS							
Input Voltage Ranges: Unipolar	0 to +5, 0 to +10		•		•		Volts
Bipolar	±2.5, ±5, ±10		•		•		Volts
Input Impedance (Direct Input) (Note 1):							
0 to +5V, ±2.5V	2.5		•		•		kΩ
0 to +10V, ±5V	5		•		•		kΩ
±10V	10		•		•		kΩ
Buffer Amplifier: Impedance (min)	100		•		•		MΩ
Bias Current (Note 1)	±50		•		•		nA
Settling Time to ±0.01% for 20V Step (Notes 1, 2)	2		•		•		μsec
DIGITAL INPUTS (Start, Short Cycle)							
Logic Levels: Logic "1" (min)	+2.0		•		•		Volts
Logic "0" (max)	+0.8		•		•		Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)	+40		•		•		μA
Logic "0" (V_{IL} = +0.4V)	−1.6		•		•		mA
TRANSFER CHARACTERISTICS (Note 3)							
Resolution	10	12	10	12	10	12	Bits
Linearity Error (max)	±0.048	±0.012	±0.048	±0.012	±0.048	±0.012	%FSR
Differential Linearity Error	±½	±½	•	•	•	•	LSB
Temperature Range for No Missing Codes	0 to +70	0 to +70	0 to +70	0 to +70	−25 to +85	−25 to +85	°C
Unipolar Offset Error (Notes 5, 9): Initial	±0.05	±0.05	•	•	•	•	%FSR
Drift (Note 4)	±3	±3	•	•	•	•	(Note 14)
Bipolar Offset Error (Notes 6, 9): Initial	±0.1	±0.1	•	•	•	•	%FSR
Drift (Note 4)	±15	±15	±20	±12	±10	±7	(Note 14)
Gain Error (Notes 7, 9): Initial	±0.1	±0.1	•	•	•	•	%
Drift (Note 4) (max)	±30	±30	±40	±25	±20	±15	ppm/°C
DIGITAL OUTPUTS							
Output Coding (Note 10):							
Parallel Outputs: Unipolar	CSB		•		•		
Bipolar	COB, CTC		•		•		
Serial Output (Note 11): Unipolar	CSB		•		•		
Bipolar	COB		•		•		
Logic Levels All Outputs:							
Logic "1" ($I_{source} \leq 80\mu A$) (min)	+2.4		•		•		Volts
Logic "0" ($I_{sink} \leq 3.2mA$) (max)	+0.4		•		•		Volts
REFERENCE OUTPUT							
Internal Reference (Note 1):							
Voltage	+6.3		•		•		Volts
Tempco (max)	±20		±10		±10		ppm/°C
External Current (max)	200		•		•		μA

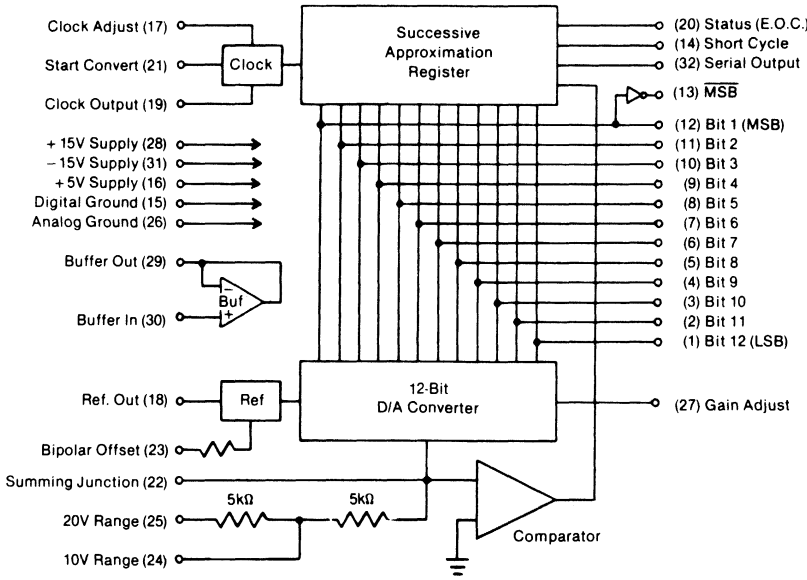
MODEL	ADC84 -10	ADC84 -12	ADC85C -10	ADC85C -12	ADC85 -10	ADC85 -12	UNITS
DYNAMIC CHARACTERISTICS							
Conversion Time (Note 8) (max)	5	8	5	8	5	8	μsec
Internal Clock Frequency (Note 1)	2	1.5	2	1.5	2	1.5	MHz
Start Convert Pulse Width (Note 1) (min)	50		•		•		nsec
POWER SUPPLIES							
Power Supply Range: + 15V Supply	+ 14.5 to + 15.5		•		•		Volts
− 15V Supply	− 14.5 to − 15.5		•		•		Volts
+ 5V Supply	+ 4.75 to + 5.25		•		•		Volts
Power Supply Rejection (Notes 3, 12): + 15V Supply	± 0.004		•		•		(Note 15)
− 15V Supply	± 0.004		•		•		(Note 15)
+ 5V Supply	± 0.001		•		•		(Note 15)
Current Drain: + 15V Supply	+ 20		•		•		mA
− 15V Supply	− 25		•		•		mA
+ 5V Supply	+ 60		•		•		mA
Power Consumption	975		•		•		mW

SPECIFICATION NOTES:

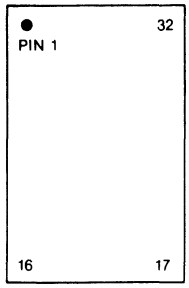
1. These parameters are listed for reference only and are not tested.
2. Buffer settling time is added to conversion time when calculating system throughput when using the internal buffer. See section labeled Internal Buffer Amplifier.
3. FSR = full scale range. A unit connected for a 0 to + 5V or ± 2.5V input range has a 5V FSR. A unit connected for a 0 to + 10V or ± 5V input range has a 10V FSR, etc.. 1LSB for 12 bits is equivalent to 0.024% FSR. 1LSB for 10 bits is equivalent to 0.098% FSR.
4. Listed specification applies over the 0°C to + 70°C temperature range for ADC84-10, -12 and ADC85C-10, -12. Listed specification applies over the − 25°C to + 85°C temperature range for ADC85-10, -12.
5. Unipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition occurs when operating on a unipolar input range.
6. Bipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition occurs when operating on a bipolar input range.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
8. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 2 (bit 11) to pin 14 (Short Cycle) for 10-bit conversions. See Timing Diagram.
9. Initial error is adjustable to zero.
10. CSB = complementary straight binary. COB = complementary offset binary. CTC = complementary two's complement.
11. Serial data is in non-return-to-zero (NRZ) format and is coded in CSB and COB.
12. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0001 to 0000 0000 0000 output transitions occur versus a change in power-supply voltage.
13. " • " indicates that specification is the same as for ADC84.
14. ppm of FSR/°C
15. %FSR/% Supply

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



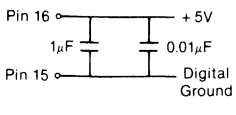
1 Bit 12 (LSB)
2 Bit 11
3 Bit 10
4 Bit 9
5 Bit 8
6 Bit 7
7 Bit 6
8 Bit 5
9 Bit 4
10 Bit 3
11 Bit 2
12 Bit 1 (MSB)
13 $\overline{\text{MSB}}$
14 Short Cycle
15 Digital Ground
16 +5V Supply (+Vdd)
32 Serial Output
31 −15V Supply (−Vcc)
30 Buffer Input
29 Buffer Output
28 +15V Supply (+Vcc)
27 Gain Adjust
26 Analog Ground
25 20V Range
24 10V Range
23 Bipolar Offset
22 Summing Junction
21 Start Convert
20 Status (E.O.C.)
19 Clock Output
18 Reference Output (+6.3V)
17 Clock Adjust

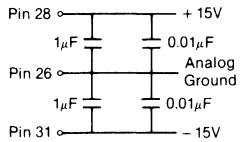
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies. Analog and digital grounds (pins 15 and 26) are not connected to each other internally and must be tied together as close to the package as possible, preferably through a large analog ground plane underneath the package. If these commons must be run separately, a nonpolarized, 0.01 to 0.1μF bypass capacitor should be connected between pins 15 and 26 as close to the package as possible and wide conductor runs should be used.

Coupling between the analog inputs and digital signals should be minimized to reduce noise pickup. The Summing Junction (pin 22) is the direct input to the internal comparator and is particularly noise susceptible. In bipolar operation, where pin 22 is connected to pin 23, a short jumper should be used, and when external offset adjustment is employed, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the device package. For optimum results, 1μF capacitors paralleled by 0.01μF ceramic capacitors should be connected as shown in the diagrams below. An additional 0.01μF ceramic bypass capacitor should be located close to the package connecting the gain adjust point (pin 27) to analog ground.





For normal 12-bit operation using the internal clock, Clock Adjust (pin 17) must be connected to Digital Ground (pin 15) and Short Cycle (pin 14) should be connected to +5V (pin 16).

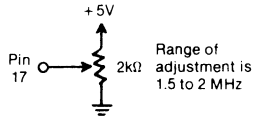
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

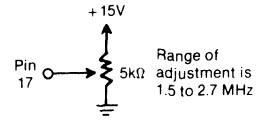
STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit of any conversion will not be valid until a maximum of 120nsec after the Status output has gone low.

SHORT CYCLING—For applications requiring less than 12 bits resolution, these converters can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. The connections shown below both increase the clock rate and truncate the converter to provide the minimum conversion time for a given resolution.

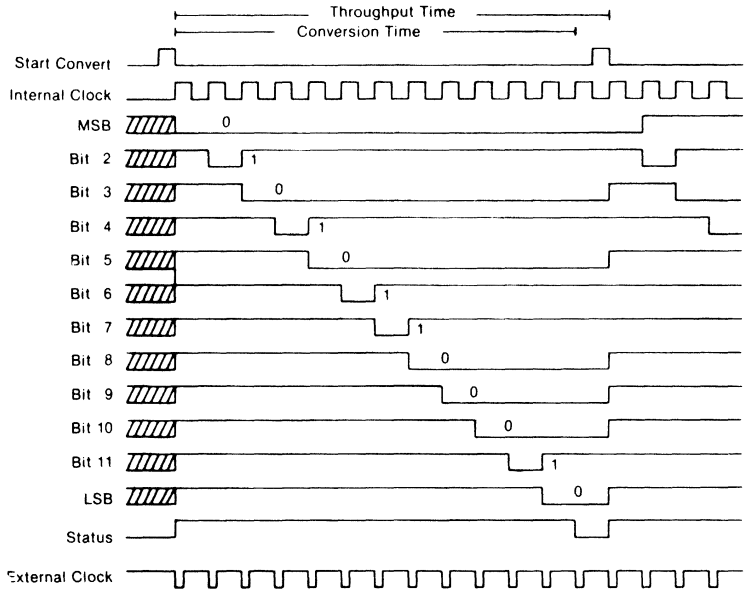
Resolution (Bits)	12	10	8
Connect Pin 17 to Pin	15	16	28
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μsec)	8	5	3
Clock Speed (MHz)	1.5	2	2.7

CLOCK RATE—The internal clock is preset to approximately 1.5 MHz and can be adjusted over a range of 1.5 to 2.7 MHz. To adjust the internal clock, a multiturn pot (TCR of 100ppm/°C or less) is connected to pin 17 as shown in the diagrams below.





'IMING DIAGRAM



MING DIAGRAM NOTES:

Conversion time is defined as the width of the Status pulse.
The Start Convert command must be at least 50nsec wide and must remain low during conversion.
The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
The delay from the falling edge of the Start Convert signal to Status actually rising to a "1" may be 100nsec.
Parallel data will be valid 120nsec after the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
The delay from clock to serial data valid will be a maximum of 140nsec from a rising internal clock edge or a maximum of 200nsec from a falling external clock edge.
7. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock section.
8. Once a conversion has begun, a second start pulse will not reset the converter. See Start Convert section.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

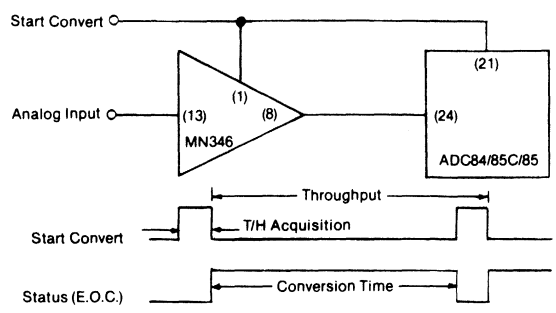
ADC84/85

(TERNAL CLOCK—An external clock may be connected to e Start Convert input. This external clock must consist of gative going pulses 100 to 200nsec wide and must be at a ver frequency than the internal clock. In this mode of operan, the converter will provide a continuous string of conversns each of which begins on the first falling edge of the exnal clock after Status (E.O.C.) has gone low.

TERNAL BUFFER AMPLIFIER—Both the ADC84 and)C85 provide user-optional internal buffer amplifiers. Use these buffer amplifiers provides an input impedance eater than 100MΩ allowing the A/D's to be driven from high pedance sources or directly from an analog multiplexer. nen using the optional buffer amplifier, a 2μsec delay must provided to allow the amplifier to settle prior to triggering Start Convert input. If the buffer amplifier is not required, input should be connected to analog ground to avoid introcing noise into the converter.

ING A TRACK/HOLD AMPLIFIER WITH AN ADC84/85C/85
When using a track-hold (T/H) amplifier with an C84/85C/85, the T/H can be driven directly (or inverted) from A/D's Start Convert signal. When the Start is high prior to beginning of a conversion, the T/H can be in the tracking signal acquisition mode. The falling edge of the start signal iates the conversion and simultaneously commands the T/H into the hold mode. The MSB output will be set to its final value one internal clock period later (approximately 0.67μsec), and the sample-to-hold transient of the chosen T/H should have settled to within ±0.01%FSR of its final value by that time. The width of the start convert pulse may have to be lengthened to accommodate the acquisition time spec of the chosen T/H.

MN346 - ADC84/85C/85

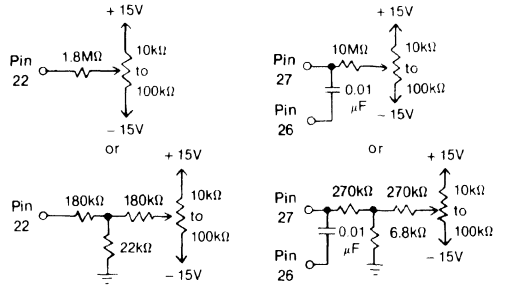


Throughput Rate	100kHz
T/H Acquisition Time	2μsec
A/D Conversion Time	8μsec

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 22 should be connected as described in the Input Range Selection section and a 0.01μF capacitor should be connected from pin 27 to pin 26.

OFFSET ADJUSTMENTS—Connect the offset potentiometer as shown and apply the input voltage at which the 1111 1111 1110 to 1111 1111 1111 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off. A 0.01μF capacitor should be connected from Gain Adjust (pin 27) to Analog Ground (pin 26).



Offset Adjust **Gain Adjust**

INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FOR NORMAL INPUT					
Input Impedance (kΩ)	2.5	5	2.5	5	10
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	Input Signal
Connect Pin 30 to Pin	26	26	26	26	26
Connect Input to Pin	24	24	24	24	25
FOR BUFFERED INPUT					
Input Impedance (MΩ)	100	100	100	100	100
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	29
Connect Pin 29 to Pin	24	24	24	24	25
Connect Input to Pin	30	30	30	30	30

DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Outputs
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB LSB
+5.0000	+10.0000	+2.5000	+5.0000	+10.0000	0000 0000 0000
+4.9982	+9.9963	+2.4982	+4.9963	+9.9927	0000 0000 000Ø*
+2.5006	+5.0012	+0.0006	+0.0012	+0.0024	0111 1111 111Ø*
+2.4994	+4.9988	−0.0006	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+2.4982	+4.9963	−0.0018	−0.0037	−0.0073	1000 0000 000Ø*
+0.0006	+0.0012	−2.4994	−4.9988	−9.9976	1111 1111 111Ø*
0.0000	0.0000	−2.5000	−5.0000	−10.0000	1111 1111 1111

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary (CSB).
2. For bipolar input ranges, output coding is complementary offset binary (COB).
3. For bipolar input ranges, complementary two's complement coding (CTC) can be obtained by using the complement of the most significant bit MSB. $\overline{\text{MSB}}$ is available on pin 13. See Pin Designations.
4. For 0 to +5V or ±2.5V input ranges, 1LSB for 12 bits = 1.22mV. 1LSB for 10 bits = 4.88mV.
5. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 10 bits = 9.77mV.
6. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 10 bits = 19.5mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADC85-12 operating on its ±10V input range, the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9976 volts (−Full Scale + ½LSB). Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input voltage of −0.0024 volts (−½LSB) and the 0000 0000 0001 to 0000 0000 0000 transition should occur at +9.9927 volts (+Full Scale −⅜LSB). An input more positive than +9.9927 volts will give all "0's".

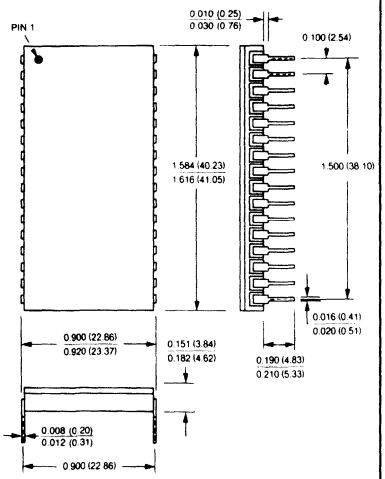
MICRO NETWORKS

ADC87

12-Bit, 8μsec
MILITARY
A/D CONVERTER

FEATURES

- **Fully Guaranteed −55°C to +125°C Operation**
- **8μsec Max Conversion Time**
- **Complete/Versatile A/D Function:**
  - **Internal or External Clock**
  - **Internal Reference**
  - **User-Optional Input Buffer**
  - **Serial and Parallel Outputs**
  - **Short-Cycle Pin**
- **No Missing Codes Guaranteed Over Temperature**
- **Low Drift: Gain ±20ppm/°C Max Offset ±5ppm/°C Max**
- **Pin-Compatible ADC84/85**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**



Dimensions in Inches (millimeters)

DESCRIPTION

The Micro Networks ADC87 is a high-performance, 12-bit, successive approximation, A/D converter in a hermetically sealed, ceramic, 32-pin dual-in-line package. It is pin-compatible with industry-standard ADC85 type 12-bit A/D converters and is the first device of this type to offer fully guaranteed performance specifications over the full -55°C to +125°C operating temperature range. It also guarantees an 8μsec max conversion time compared to the 10μsec of other devices in its class. ADC87 linearity is guaranteed better than ±½LSB, and no missing codes is guaranteed over temperature. Max gain drift is a low ±20ppm/°C; max offset drift a low ±5ppm of FSR/°C.

ADC87 is extremely versatile. It has its own reference and internal clock; yet it can run from an external clock. There are 5 user-selectable input ranges, serial and parallel outputs, a short-cycle pin, a user-optional high-impedance input buffer and pins for optional offset and gain adjustments.

For military aerospace or harsh-environment commercial/industrial applications, ADC87H/B CH is fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

ADC87 is ideally suited for fast data digitizing in military/aerospace applications. Its rugged, hermetically sealed, ceramic package has outstanding thermal characteristics and can withstand the harshest environments.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

December 1991
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ADC87 12-Bit 8μsec A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
ADC87	−25°C to +85°C
ADC87H, ADC87H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 28)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 31)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 16)	−0.5 to +7 Volts
Digital Inputs (Pins 14, 21)	−0.5 to +5.5 Volts
Analog Inputs: Direct (Pins 24, 25)	±25 Volts
Buffer (Pin 30)	±15 Volts

ORDERING INFORMATION

PART NUMBER ADC87H/B CH

- Standard part is specified for −25°C to +85°C operation.
- Add "H" for specified −55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +5, 0 to +10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Direct Input Impedance (Note 1): 0 to +5V, ±2.5V		2.5		kΩ
0 to +10V, ±5V		5		kΩ
±10V		10		kΩ
Buffer Amplifier (Note 2): Gain Accuracy		±0.01		%
Input Impedance (Note 1)	10^{10}	10^{12}		Ω
Input Bias Current (Note 1)		±2	±7	nA
Offset Voltage		±4	±10	mV
Settling Time (20V Step to ±0.01%FSR)		3		μsec
DIGITAL INPUTS (Start Convert, Short Cycle)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+80	μA
Logic "0" (V_{IL} = +0.4V)			−3.2	mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 4)		±½	±1	LSB
Differential Linearity Error		±½		LSB
Differential Linearity Drift (Notes 1, 4)		±2		ppm of FSR/°C
Guaranteed Temperature Range for No Missing Codes:				
ADC87	−25		+85	°C
ADC87H, ADC87H/B	−55		+125	°C
Unipolar Offset Error (Notes 5, 6): Initial (+25°C)		±0.1	±0.2	%FSR
Drift (Note 4)		±3	±5	ppm of FSR/°C
Bipolar Zero Error (Notes 5, 7): Initial (+25°C)		±0.1	±0.25	%FSR
Drift (Note 4)		±5	±10	ppm of FSR/°C
Gain Error (Notes 5, 8): Initial (+25°C)		±0.1	±0.25	%
Drift (Note 4)		±10	±20	ppm/°C
DIGITAL OUTPUTS (Parallel, Serial, Clock, Status)				
Output Coding (Note 9): Unipolar Ranges		CSB		
Bipolar Ranges		COB, CTC		
Logic Levels: Logic "1" ($I_{SOURCE} \leq 320\mu A$)	+2.4			Volts
Logic "0" ($I_{SINK} \leq 3.2mA$)			+0.4	Volts
REFERENCE OUTPUT				
Internal Reference: Voltage		+6.3		Volts
Accuracy (Note 1)		±5		%
Tempco		±5	±10	ppm/°C
External Current			200	μA

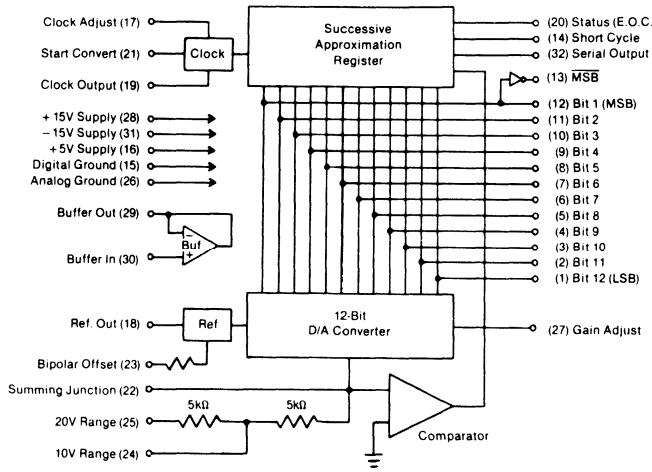
DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (Note 10)		7	8	μsec
Internal Clock Frequency (Note 1)	1.5	1.7		MHz
Start Convert Pulse Width (Note 1)	50			nsec
Delay Falling Edge of Start Convert to Status="1" (Note 1)		50	100	nsec
Delay Falling Edge of Status to LSB Valid (Note 1)		25	120	nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		75	140	nsec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.5	+15	+15.5	Volts
−15V Supply	−14.5	−15	−15.5	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Note 11): +15V Supply		±0.01	±0.02	%FSR/%Supply
−15V Supply		±0.01	±0.02	%FSR/%Supply
+5V Supply		±0.005	±0.01	%FSR/%Supply
Current Drain: +15V Supply		+27	+35	mA
−15V Supply		−27	−35	mA
+5V Supply		+60	+75	mA
Power Consumption		1110	1425	mW

SPECIFICATION NOTES:

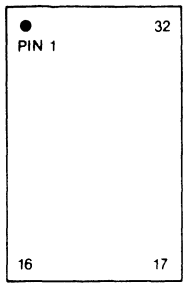
1. These parameters are listed for reference only and are not tested.
2. When using the internal buffer amplifier, buffer settling time must be added to conversion time when calculating system throughput. See section labled Internal Buffer Amplifier.
3. FSR = full scale range. A unit connected for a 0 to +5V or ±2.5V input range has a 5V FSR. A unit connected for a 0 to +10V or ±5V input range has a 10V FSR, etc. 1 LSB for 12 bits is equivalent to 0.024%FSR.
4. Listed specification applies over the −25°C to +85°C temperature range for ADC87. Listed specification applies over the −55°C to +125°C temperature range for ADC87H and ADC87H/B.
5. Initial error is adjustable to zero.
6. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 when operating the ADC87 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
7. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the ADC87 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
8. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
9. CSB = complementary straight binary. COB = complementary offset binary. CTC = complementary two's complement. See table of transition voltages in section labeled Digital Output Coding.
10. Conversion is initiated on the falling edge of the start convert command, and conversion time is defined as the width of status (E.O.C.). Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 2 (Bit 11) to pin 14 (Short Cycle) for 10-bit conversions. See Timing Diagram.
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



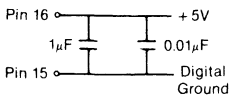
1 Bit 12 (LSB)
2 Bit 11
3 Bit 10
4 Bit 9
5 Bit 8
6 Bit 7
7 Bit 6
8 Bit 5
9 Bit 4
10 Bit 3
11 Bit 2
12 Bit 1 (MSB)
13 $\overline{\text{MSB}}$
14 Short Cycle
15 Digital Ground
16 +5V Supply (+Vdd)
32 Serial Output
31 −15V Supply (−Vcc)
30 Buffer Input
29 Buffer Output
28 +15V Supply (+Vcc)
27 Gain Adjust
26 Analog Ground
25 20V Range
24 10V Range
23 Bipolar Offset
22 Summing Junction
21 Start Convert
20 Status (E.O.C.)
19 Clock Output
18 Reference Output (+6.3V)
17 Clock Adjust

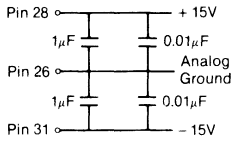
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies. Analog and digital grounds (pins 15 and 26) are not connected to each other internally and must be tied together as close to the package as possible, preferably through a large analog ground plane underneath the package. If these commons must be run separately, a nonpolarized, 0.01 to 0.1μF bypass capacitor should be connected between pins 15 and 26 as close to the package as possible and wide conductor runs should be used.

Coupling between the analog inputs and digital signals should be minimized to reduce noise pickup. The Summing Junction (pin 22) is the direct input to the internal comparator and is particularly noise susceptible. In bipolar operation, where pin 22 is connected to pin 23, a short jumper should be used, and when external offset adjustment is employed, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the device package. For optimum results, 1μF capacitors paralleled by 0.01μF ceramic capacitors should be connected as shown in the diagrams below. An additional 0.01μF ceramic bypass capacitor should be located close to the package connecting the gain adjust point (pin 27) to analog ground.





For normal 12-bit operation using the internal clock, Clock Adjust (pin 17) must be connected to Digital Ground (pin 15) and Short Cycle (pin 14) should be connected to +5V (pin 16).

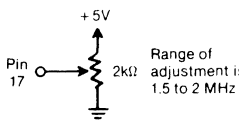
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

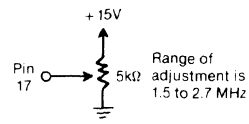
STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit of any conversion will not be valid until a maximum of 120nsec after the Status output has gone low.

SHORT CYCLING—For applications requiring less than 12 bits resolution, these converters can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. The connections shown below both increase the clock rate and truncate the converter to provide the minimum conversion time for a given resolution.

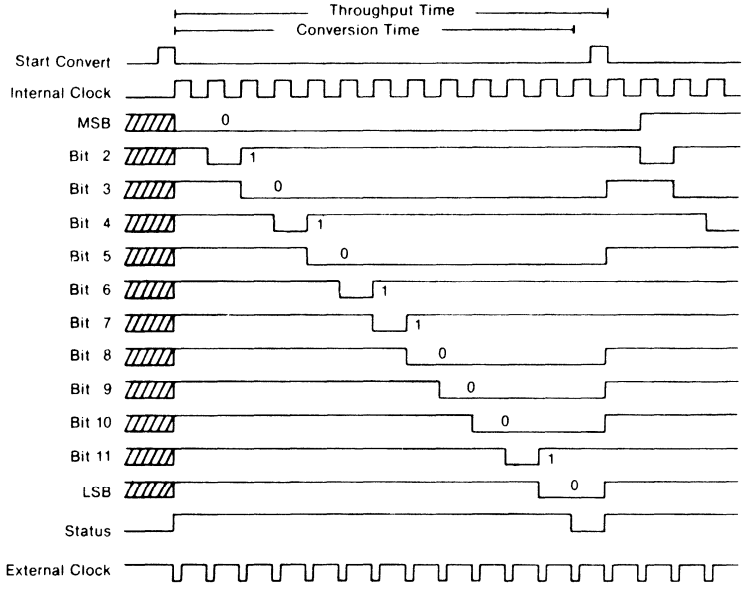
Resolution (Bits)	12	10	8
Connect Pin 17 to Pin	15	16	28
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μsec)	8	5	3
Clock Speed (MHz)	1.5	2	2.7

CLOCK RATE—The internal clock is preset to approximately 1.5 MHz and can be adjusted over a range of 1.5 to 2.7 MHz. To adjust the internal clock, a multiturn pot (TCR of 100ppm/°C or less) is connected to pin 17 as shown in the diagrams below.





TIMING DIAGRAM



TIMING DIAGRAM NOTES:

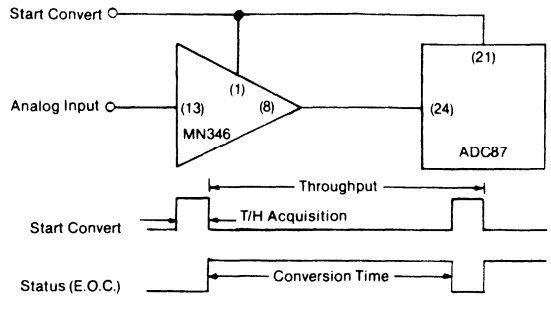
1. Conversion time is defined as the width of the Status pulse.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. The delay from the falling edge of the Start Convert signal to Status actually rising to a "1" may be 100nsec.
5. Parallel data will be valid 120nsec after the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
6. The delay from clock to serial data valid will be a maximum of 140nsec from a rising internal clock edge or a maximum of 200nsec from a falling external clock edge.
7. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock section.
8. Once a conversion has begun, a second start pulse will not reset the converter. See Start Convert section.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. In this mode of operation, the converter will provide a continuous string of conversions each of which begins on the first falling edge of the external clock after Status (E.O.C.) has gone low.

INTERNAL BUFFER AMPLIFIER—ADC87 provides a user-optional internal buffer amplifier. Use of this buffer amplifier provides an input impedance greater than 100MΩ allowing the A/D to be driven from high impedance sources or directly from an analog multiplexer. When using the optional buffer amplifier, a 2μsec delay must be provided to allow the amplifier to settle prior to triggering the Start Convert input. If the buffer amplifier is not required, its input should be connected to analog ground to avoid introducing noise into the converter.

USING A TRACK/HOLD AMPLIFIER WITH AN ADC87—When using a track-hold (T/H) amplifier with an ADC87, the T/H can be driven directly (or inverted) from the A/D's Start Convert signal. When the Start is high prior to the beginning of a conversion, the T/H can be in the tracking or signal acquisition mode. The falling edge of the start signal initiates the conversion and simultaneously commands the T/H into the hold mode. The MSB output will be set to its final value one internal clock period later (approximately 0.67μsec), and the sample-to-hold transient of the chosen T/H should have settled to within ±0.01%FSR of its final value by that time. The width of the start convert pulse may have to be lengthened to accommodate the acquisition time spec of the chosen T/H.

MN346 - ADC87

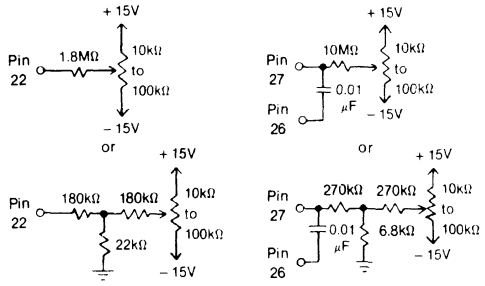


Throughput Rate	100kHz
T/H Acquisition Time	2μsec
A/D Conversion Time	8μsec

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 22 should be connected as described in the Input Range Selection section and a 0.01μF capacitor should be connected from pin 27 to pin 26.

OFFSET ADJUSTMENTS—Connect the offset potentiometer as shown and apply the input voltage at which the 1111 1111 1110 to 1111 1111 1111 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off. A 0.01μF capacitor should be connected from Gain Adjust (pin 27) to Analog Ground (pin 26).



Offset Adjust **Gain Adjust**

INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FOR NORMAL INPUT					
Input Impedance (kΩ)	2.5	5	2.5	5	10
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	Input Signal
Connect Pin 30 to Pin	26	26	26	26	26
Connect Input to Pin	24	24	24	24	25
FOR BUFFERED INPUT					
Input Impedance (MΩ)	100	100	100	100	100
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	29
Connect Pin 29 to Pin	24	24	24	24	25
Connect Input to Pin	30	30	30	30	30

DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Outputs
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB LSB
+5.0000	+10.0000	+2.5000	+5.0000	+10.0000	0000 0000 0000
+4.9982	+9.9963	+2.4982	+4.9963	+9.9927	0000 0000 000Ø*
+2.5006	+5.0012	+0.0006	+0.0012	+0.0024	0111 1111 111Ø*
+2.4994	+4.9988	−0.0006	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+2.4982	+4.9963	−0.0018	−0.0037	−0.0073	1000 0000 000Ø*
+0.0006	+0.0012	−2.4994	−4.9988	−9.9976	1111 1111 111Ø*
0.0000	0.0000	−2.5000	−5.0000	−10.0000	1111 1111 1111

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary (CSB).
2. For bipolar input ranges, output coding is complementary offset binary (COB).
3. For bipolar input ranges, complementary two's complement coding (CTC) can be obtained by using the complement of the most significant bit MSB. $\overline{MSB}$ is available on pin 13. See Pin Designations.
4. For 0 to +5V or ±2.5V input ranges, 1LSB for 12 bits = 1.22mV. 1LSB for 10 bits = 4.88mV.
5. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 10 bits = 9.77mV.
6. For ±10V input range. 1LSB for 12 bits = 4.88mV. 1LSB for 10 bits = 19.5mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADC87 operating on its ±10V input range, the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9976 volts (−Full Scale +½LSB). Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input voltage of −0.0024 volts (−½LSB) and the 0000 0000 0001 to 0000 0000 0000 transition should occur at +9.9927 volts (+Full Scale −$^3/_2$LSB). An input more positive than +9.9927 volts will give all "0's".

MICRO NETWORKS

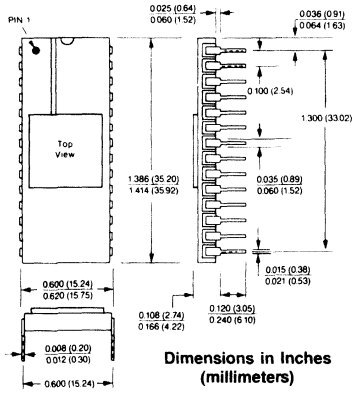
MN574A

μP-COMPATIBLE
25μsec, 12-Bit
A/D CONVERTER

FEATURES

- **Low Cost**
- **Complete, 25μsec, 12-Bit A/D Converter with Internal:**
  - **Clock**
  - **Reference**
  - **Control Logic**
- **HI-574A and AD574A Pin and Function Compatible**
- **Full 8 or 16-Bit μP Interface:**
  - **Three-State Output Buffer**
  - **Chip Select, Address Decode**
  - **Read/Write Control**
- **No Missing Codes Guaranteed Over Temperature**
- **Operation with ±12V or ±15V Supplies**
- **28-Pin DIP, 450mW Max Power**
- **Full Mil Operation −55°C to +125°C**

28-PIN CERAMIC DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN574A is a complete, low-cost, 12-bit, successive-approximation A/D with internal buried-zener reference (+10V), clock, and control logic. MN574A is packaged in a 28-pin DIP and contains all the interface logic necessary to directly mate to most popular 8 and 16-bit microprocessors. MN574A's 3-state output buffer connects directly to the μP's data bus and can be read either as one 12-bit word or as two 8-bit bytes. Chip select, chip enable, address decode (short cycle), and read/write (read/convert) control inputs enable MN574A to connect directly to system address bus and control lines and operate totally under processor control.

MN574A's combination of bipolar and CMOS technologies represents the latest advances in 574A/674A evolution, and all problems associated with earlier models from other manufacturers have been solved. These devices are truly TTL compatible over all temperature ranges, and they are not prone to CMOS latch-up at power-on. Their internal clock has minimal drift, and conversion time is guaranteed over all temperature ranges. Bus access time is guaranteed not to exceed 150nsec, and the A_0 line may be toggled freely with no fear of output-data overlap thanks to break-before-make action on the output buffer. At 450mW max, power consumption is almost half that of competing devices.

MN574A is ideal for most military/aerospace and industrial, general-purpose, data-acquisition applications. The device is multi-sourced and available in 5 different electrical grades fully specified for either 0°C to +70°C or −55°C to +125°C operation. Each device guarantees integral linearity and no missing codes as summarized below. Add "/B" to either the S or T grade units for environmental stress screening.

Model	Temperature Range	Linearity Error Max (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})
MN574AJ	0°C to +70°C	±1LSB	11 Bits
MN574AK	0°C to +70°C	±½LSB	12 Bits
MN574AL	0°C to +70°C	±½LSB	12 Bits
MN574AS	−55°C to +125°C	±1LSB	11 Bits
MN574AS/B*	−55°C to +125°C	±1LSB	11 Bits
MN574AT	−55°C to +125°C	±1LSB	12 Bits
MN574AT/B*	−55°C to +125°C	±1LSB	12 Bits

*Includes environmental stress screening

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MN574A μP-COMPATIBLE, 25μsec, 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN574AJ, K, L	0°C to +70°C
MN574AS, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+Vdd + 0.5) Volts
Analog Inputs: Pins 10, 12 and 13	±16.5 Volts
Pin 14	±24 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref. Out (Pin 8) Short Circuit Duration	Continuous to Ground Momentary to ±Vcc

ORDERING INFORMATION

PART NUMBER — MN574AX/B

Select suffix J, K, L, S or T for desired performance and specified temperature range.

Add "/B" suffix to S or T models for environmental stress screening.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	4.7	5	5.3	kΩ
0 to +20V, ±10V	9.4	10	10.6	kΩ
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8 (Note 2)				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Currents	−5	±0.1	+5	μA
Input Capacitance		5		pF
DIGITAL OUTPUTS DB0-DB11, STS (Note 2)				
Output Coding (Note 3): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 500\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 1.6mA$)			+0.4	Volts
Leakage (DB0-DB11) in High-Z State	−5	±0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10.0	+10.1	Volts
Drift		±10		ppm/°C
Output Source Current (Note 4)	2.0			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc	±11.4		±16.5	Volts
+Vdd	+4.5	+5	+5.5	Volts
Power Supply Rejection (See Performance Specifications)				
Current Drains: +Vcc Supply		+3.5	+5	mA
−Vcc Supply		−15	−20	mA
+Vdd Supply		+9	+15	mA
Power Consumption (±Vcc = ±15V)		325	450	mW
DYNAMIC CHARACTERISTICS				
Conversion Time (Notes 1, 2, 5): 8-Bit Cycle:	10	13	17	μsec
12-Bit Cycle:	15	20	25	μsec

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. Listed specifications guaranteed over each device's full specified temperature range as determined by part number suffix.
3. See table of transition voltages in section labeled Output Coding.
4. The internal reference can be used to drive an external load, and it is capable of supplying up to 2mA over and above the requirements of the reference-in and bipolar-offset resistors. The external load should not vary during a conversion. The reference output does not require a buffer when operating with either ±15V or ±12V supplies.
5. If a conversion is started with A_0 (pin 4) low, a full 12-bit conversion cycle is initiated. If A_0 is high, a shorter 8-bit conversion is initiated. Conversion time is defined as the width of the Status Output pulse. See the Timing sections for more details.
6. MN574AJ, K, L are fully specified for 0°C to +70°C operation. MN574AS, T, are fully specified for −55°C to +125°C operation.
7. Adjustable to zero with external potentiometer.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN574A on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Listed maximum change specifications (temperature coefficients) for unipolar offset, bipolar offset and full scale calibration error correspond to the maximum change from the initial value (+25°C) to the value at T_{min} or T_{max}.

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated)

MODEL	574AJ	574AK	574AL	574AS	574AT	UNITS
Integral Linearity Error: Initial (+25°C) (Max)	±1	±½	±½	±1	±½	LSB
T_{min} to T_{max} (Max, Note 6)	±1	±½	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	11	12	12	11	12	Bits
T_{min} to T_{max} (Note 6)	11	12	12	11	12	Bits
Unipolar Offset Error (Notes 7, 8):						
Initial (+25°C) (Max)	±2	±1	±1	±2	±1	LSB
Drift (Max)	±10	±5	±5	±5	±2.5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±2	±1	LSB
Bipolar Offset Error (Notes 7, 10):						
Initial (+25°C) (Max)	±4	±4	±2	±4	±4	LSB
Drift (Max)	±10	±5	±5	±10	±5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±4	±2	LSB
Full Scale Calibration Error (Notes 7, 11):						
Initial (+25°C) (Max)	±0.25	±0.25	±0.25	±0.25	±0.25	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.47	±0.37	±0.3	±0.75	±0.5	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.22	±0.12	±0.05	±0.5	±0.25	%FSR
Drift (Max)	±50	±27	±10	±50	±25	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±9	±5	±2	±20	±10	LSB
Power Supply Rejection (Note 12)						
+13.5V ≤ +Vcc ≤ +16.5V or +11.4V ≤ +Vcc ≤ +12.6V	±2	±1	±1	±2	±1	LSB
−16.5V ≤ −Vcc ≤ −13.5V or −12.6V ≤ −Vcc ≤ −11.4V	±2	±1	±1	±2	±1	LSB
+4.5V ≤ +Vdd ≤ +5.5V	±½	±½	±½	±½	±½	LSB

Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN574A on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.

Listed specs assume a fixed 50Ω resistor between Ref Out (pin 8) and Ref In (pin 10) and a fixed 50Ω resistor between Ref Out (pin 8) and Bipolar Offset (pin 12, bipolar configurations) or Bipolar Offset grounded (unipolar configurations). Full scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. Ideally, this digital output transition should occur at an analog voltage 1½LSB's below the nominal full scale voltage. See Digital Output Coding.

12. Listed spec is the max change in full scale calibration accuracy as supplies are varied over the range indicated.

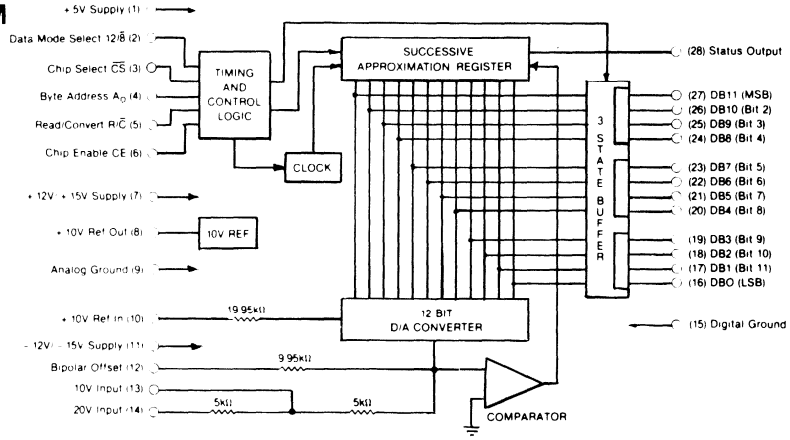
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

ORDERING INFORMATION

Part Number	Specified Temperature Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	No Missing Codes Over Temp.	Max. Offset Drift (2)	Max. Full Scale Drift (2)	Max. Power (mW)
MN574AJ	0°C to +70°C	±1	±1	11 Bits	±10	±50	450
MN574AK	0°C to +70°C	±½	±½	12 Bits	±5	±27	450
MN574AL	0°C to +70°C	±½	±½	12 Bits	±5	±10	450
MN574AS	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN574AS/B (3)	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN574AT	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450
MN574AT/B (3)	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450

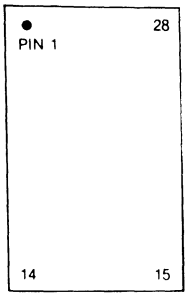
Maximum error expressed in LSB's for 12 bits. 2. Expressed in ppm of FSR/°C. 3. Includes environmental stress screening.

BLOCK DIAGRAM



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

PIN DESIGNATIONS



(1)	+ 5V Supply (+ V_{dd})	(28)	Status Output
(2)	Data Mode Select 12/$\overline{8}$	(27)	DB11 (MSB)
(3)	Chip Select $\overline{CS}$	(26)	DB10 (Bit 2)
(4)	Byte Address A_0	(25)	DB9 (Bit 3)
(5)	Read/Convert R/$\overline{C}$	(24)	DB8 (Bit 4)
(6)	Chip Enable CE	(23)	DB7 (Bit 5)
(7)	+ 12V/+ 15V Supply (+ V_{CC})	(22)	DB6 (Bit 6)
(8)	+ 10V Ref Out	(21)	DB5 (Bit 7)
(9)	Analog Ground	(20)	DB4 (Bit 8)
(10)	+ 10V Ref In	(19)	DB3 (Bit 9)
(11)	− 12V/− 15V Supply (− V_{CC})	(18)	DB2 (Bit 10)
(12)	Bipolar Offset	(17)	DB1 (Bit 11)
(13)	10V Input	(16)	DB0 (LSB)
(14)	20V Input	(15)	Digital Ground

DESCRIPTION OF OPERATION

The MN574A is a complete 12-bit A/D converter. It utilizes the successive approximation conversion technique and contains all required function blocks — successive approximation register (SAR), D/A converter, comparator, clock and reference — internal to its package. The MN574A mates directly to most popular 8, 16 and 32-bit microprocessors and contains all the necessary address decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most applications, the MN574A will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete A/D conversion function. The completeness of this device makes it most convenient to think of the MN574A as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating the MN574A under microprocessor control (it also functions as a stand-alone A/D) consists, in most applications, of a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D and involves a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN574A's Status Output (also called Busy Line or End of Conversion (E.O.C.) Line) rises to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Output to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Output or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

If the MN574A is operated with 12-bit or wider microprocessors, all 12 output bits can be 3-state enabled simultaneously, permitting data collection with a single read operation. If the MN574A is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's), in a left justified format, with 4 trailing "0's".

APPLICATIONS INFORMATION

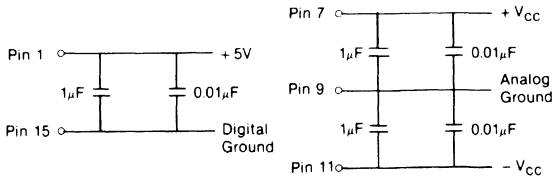
LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN574A. It is critically important that the MN574A's power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitors should be connected directly from pin 1 to pin 15 (Digital Ground), and the $+V_{CC}$ and $-V_{CC}$ supplies should be decoupled directly to pin 9 (Analog Ground). A suitable decoupling capacitor pair is usually a relatively large tantalum (1 – 10μF) in parallel with a smaller (0.01 – 1.0μF) ceramic disc.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN574A and associated analog input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the MN574A as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to the MN574A. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for the MN574A's internal reference. It should be connected as close as possible to the analog input signal reference point.

POWER SUPPLY DECOUPLING



CONTROL FUNCTIONS — Operating the MN574A under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN574A control-line functions. Table 2 is the MN574A Truth Table.

Unless Chip Enable (CE, pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$ and A_0) will have no effect on MN574A operation. When CE and $\overline{CS}$ are

Table 1: MN574A Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0→1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1→0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1→0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0→1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits) (Note 5)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

)th asserted, the signal applied to R/$\overline{C}$ (Read/Convert, pin 5) deter-
ines whether a data read (R/$\overline{C}$="1") or a convert operation
l/$\overline{C}$="0") is initiated.

'hen initiating a conversion, the signal applied to A_0 (Byte Ad-
ess/Short Cycle, pin 4) determines whether a 12-bit conversion
initiated (A_0="0") or an 8-bit conversion is initiated (A_0="1"). It
the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" or
)" that initiates a convert operation. The actual conversion can
: initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the
ling edge of R/$\overline{C}$ as shown in the Truth Table and as described
the section labeled Timing — Initiating Conversions. When
tiating conversions, the 12/$\overline{8}$ line is a "don't care".

hen reading digital output data from the MN574A, CE and $\overline{CS}$ must
asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine
: format of output data. Logic "1" applied to the R/$\overline{C}$ line will initiate
tual output data access. If the 12/$\overline{8}$ line is a "1", all 12 output data
s will be accessed simultaneously when the R/$\overline{C}$ line goes from
'0" to a "1".

he 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit
es as detailed in the section labeled Timing — Reading Output
ta. In this situation, A_0="0" will result in the 8 MSB's being ac-
ssed, and A_0="1" will result in the 4 LSB's and 4 trailing zeros
ng accessed. In this mode, only the 8 upper bits or the 4 lower
; can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled. The 4 LSB's then effectively present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23. See the section labeled Hardwiring to 8-Bit Data Buses.

Table 2: MN574A Truth Table

CONTROL INPUTS					MN574A OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (+2.0V minimum).
2. "0" indicates TTL logic zero (+0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicate logic transitions (edges).
5. Some vendors 574A's required the 12/$\overline{8}$ line to be hard wired to either +5V (pin 1) or 0V (pin 15). The MN574A may be hard wired as such or driven with normal TTL signals.
6. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

TIMING — INITIATING CONVERSIONS — It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" (initiate 8-bit conversion) or A_0="0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may change simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60nsec). If it is desired that a particular one of these three inputs be responsible for starting the conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input.

Because the MN574A's control logic latches the A_0 signal upon conversion initiation, the A_0 line should be stable immediately prior to whichever of the above transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a read operation were occurring, and the result could be system

bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.

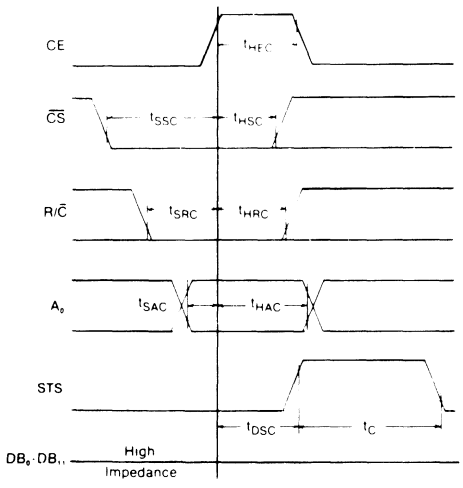
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE becoming a "1". This sequence can be accomplished in a number of ways including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent) and generating a CE 0→1 transition using the system clock. In this example, $\overline{CS}$ should be a "0" 50nsec prior to the CE transition (t_{SSC} =50nsec min), R/$\overline{C}$ should be a "0" 50nsec prior to the CE transition (t_{SRC} =50nsec min), and A_0 should be stable 0nsec prior to the CE transition (t_{SAC} =0nsec min). The minimum pulse width for CE="1" is 50nsec (t_{HEC} =50nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50nsec while CE="1" (t_{HSC} and t_{HRC} =50nsec min) to effectively initiate the conversion. Similarly, A_0 must be valid for at least 50nsec (t_{HAC} =50nsec min) while CE is high to effectively initiate the conversion. The Status Line rises to a "1" no later than 200nsec after the rising edge of CE (t_{DSC} =200nsec max). Once Status="1", additional convert commands will be ignored until ongoing conversion is complete.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status Output="1"), the MN574A's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates that the conversion is done, the combination of CE="1", $\overline{CS}$="0", and R/$\overline{C}$="1" is used to activate the buffer and read the digital output data. If the above combination of control signals is met and the 12/$\overline{8}$ line has a "1" applied, all twelve output bits will become valid simultaneously. If the 12/$\overline{8}$ line has a "0" applied, output data will be formatted for an 8-bit data bus. The 8 MSB's will become valid when the above conditions are met with A_0="0"; while the 8 LSB's (4 data bits and 4 trailing "0's") will become valid whenever A_0="1". If 12/$\overline{8}$="1", A_0 is a "don't care". If an 8-bit conversion is performed and all 12 output data bits are read, bit 9 (DB3) will be a "1", and bits 10-12 (DB2-DB0) will be "0's". Data access can be initiated by either the rising edge of CE or the falling edge of $\overline{CS}$.

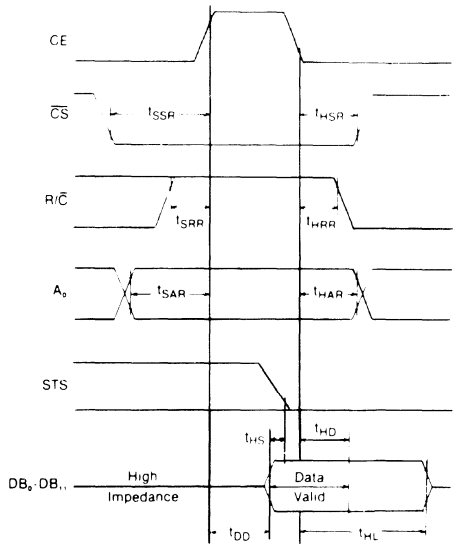
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50nsec prior to CE (t_{SSR} =50nsec min, t_{SAR} =50nsec min). R/$\overline{C}$ can become valid the same time as CE (t_{SRR} =0nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid typically 400nsec before the falling edge of Status as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TLL/CMOS compatible and may be actively driven.



Convert Start Timing



Read Cycle Timing

MN574A TIMING SPECIFICATIONS:

CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	50	20		ns
t_C	Conversion Time				
	8-Bit Cycle	10	13	17	µs
	12-Bit Cycle	15	20	25	µs

MN574A TIMING SPECIFICATIONS:

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE Low	50			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns

UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating modes are shown below. If the 0 to +10V input range is to be used, apply the analog input to pin 13. If the 0 to +20V range is used, apply the analog input to pin 14. If gain adjustment is not used, replace trim pot R_2 with a fixed, 50Ω ± 1%, metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, the actual transition will occur within specified limits of its ideal value (+½ LSB). For the 10V range, 1 LSB=2.44mV. For the 20V range, 1 LSB=4.88mV. To offset adjust, apply an analog input equal to +½LSB and, with the MN574A continuously converting, adjust the offset potentiometer "down" until the digital output is all "0's" and then adjust "up" until the LSB "flickers" between "0" and "1".

Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½LSB's below the nominal full scale of the selected input range. This corresponds to +9.9963V and +19.9927V respectively for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer "up" until the digital outputs are all "1's" and then adjusting down until the LSB "flickers" between "1" and "0".

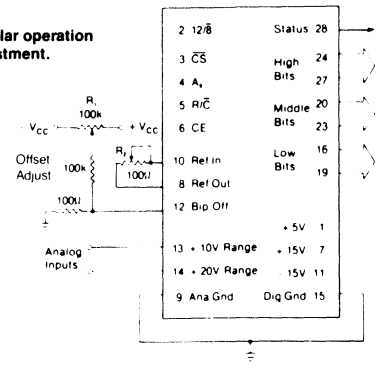
If a 10.24V (1 LSB=2.5mV) or a 20.48V (1 LSB=5mV) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor and a 200Ω trim pot (500Ω for 20.48V) inserted in series with the analog input to pin 13 (pin 14 for 20.48V). Offset trimming proceeds as described above. Gain trimming is now accomplished with the new pots. If one is not gain trimming and wishes to use fixed-value resistors, the values are 120Ω and 240Ω, respectively. MN574A's input impedance is laser trimmed to a typical accuracy of ±2%.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating modes are shown below. If the ±5V input range is to be used, apply the analog input to pin 13. If the ±10V range is used, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trim pots R_1 and R_2 should be replaced with fixed, 50Ω ±1%, metal-film resistors to meet all published specifications.

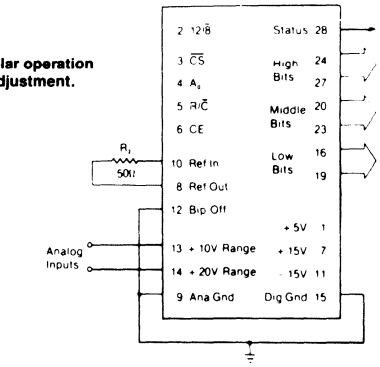
Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition should occur ½ LSB below zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the minus full scale point. The procedure is to apply an analog input equal to −FS+½ LSB (−4.9988V for the ±5V range, −9.9976V for the ±10V range) and adjust the bipolar offset trim pot "down" until the digital output is all "0's". Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal positive full scale value of the selected input range. This corresponds to +4.9963V and +9.9927V respectively for the ±5V and ±10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "up" until the digital outputs are all "1's" and then adjusting "down" until the LSB "flickers" between "1" and "0".

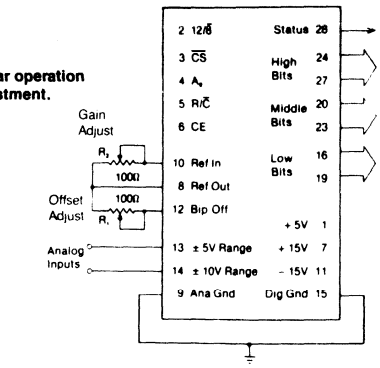
MN574A unipolar operation with trim adjustment.



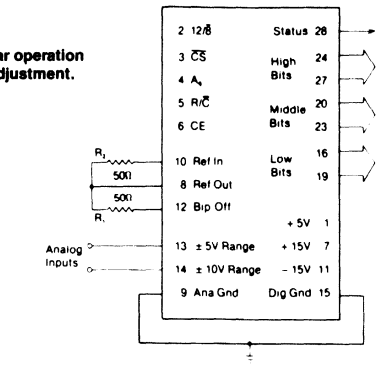
MN574A unipolar operation without trim adjustment.



MN574A bipolar operation with trim adjustment.

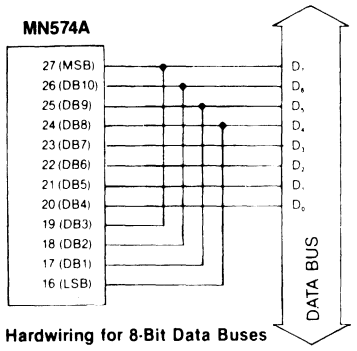


MN574A bipolar operation without trim adjustment.



HARDWIRING TO 8-BIT DATA BUSES — For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN574A output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".

	D_7	D_8	D_5	D_4	D_3	D_2	D_1	D_0
High Byte ($A_0 = 0$)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte ($A_0 = 1$)	DB3	DB2	DB1	DB0	0	0	0	0

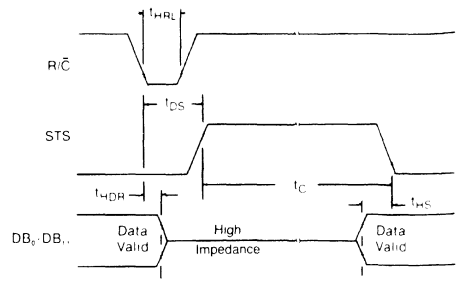


Hardwiring for 8-Bit Data Buses

STAND-ALONE OPERATION

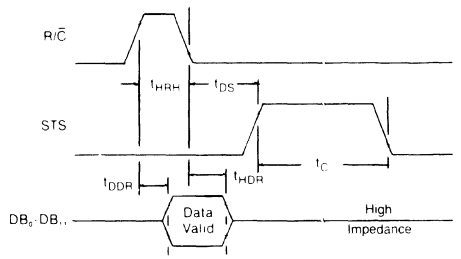
The MN574A can be used in a "stand-alone" mode in systems having dedicated input ports and not requiring full bus interface capability. In this mode, $\overline{CE}$ and 12/$\overline{8}$ are tied to logic "1" (they may be hard-wired to +5V), $\overline{CS}$ and A_0 are tied to logic "0" (they may be grounded), and the conversion is controlled by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low (assuming a conversion is not already in progress), and all 12 bits of the three-state output buffers are enabled whenever R/$\overline{C}$ is brought high (assuming Status has already gone low indicating conversion complete).

This gives rise to two possible modes of operation; conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. The first timing diagram to the right details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The Status Output goes high 200ns after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 1000nsec after data is valid (t_{HS}). In this mode, output data is available "most of the time" and becomes invalid only during a conversion.



Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion

The timing diagram below details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible "most of the time" and becomes valid only when R/$\overline{C}$ is brought high.



High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to + 10V	0 to + 20V	± 5V	± 10V	MSB LSB
+ 10.0000	+ 20.0000	+ 5.0000	+ 10.0000	1111 1111 1111
+ 9.9963	+ 19.9927	+ 4.9963	+ 9.9927	1111 1111 111Ø*
+ 5.0012	+ 10.0024	+ 0.0012	+ 0.0024	1000 0000 000Ø*
+ 4.9988	+ 9.9976	− 0.0012	− 0.0024	ØØØØ ØØØØ ØØØØ*
+ 4.9963	+ 9.9927	− 0.0037	− 0.0073	0111 1111 111Ø*
+ 0.0012	+ 0 0024	− 4.9988	− 9.9976	0000 0000 000Ø*
0.0000	0.0000	− 5.0000	− 10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to + 10V or ± 5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For 0 to + 20V or ± 10V input ranges, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN574A operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of − 9.9976 volts. Subsequently, any input voltage more negative than − 9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of − 0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at + 9.9927 volts. An input more positive than + 9.9927 volts will give all "1's".

MICRO NETWORKS

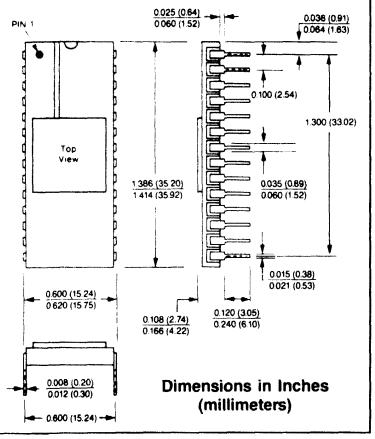
MN674A

μP-COMPATIBLE
15μsec, 12-Bit
A/D CONVERTER

FEATURES

- **Complete, 15μsec, 12-Bit A/D Converter with Internal:**
  - **Clock**
  - **Reference**
  - **Control Logic**
- **HI-674A and AD674A Pin and Function Compatible**
- **Full 8 or 16-Bit μP Interface:**
  - **Three-State Output Buffer**
  - **Chip Select, Address Decode**
  - **Read/Write Control**
- **±½LSB Linearity Guaranteed −55°C to +125°C (U Model)**
- **No Missing Codes Guaranteed Over Temperature**
- **Operation with ±12V or ±15V Supplies**
- **28-Pin DIP, 450mW Max Power**
- **Full Mil Operation −55°C to +125°C**

28-PIN CERAMIC DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN674A is a faster version (15μsec max conversion time) of the industry-standard MN574A microprocessor-interfaced, 12-bit A/D converter. It is a complete, successive-approximation A/D with internal buried-zener reference (+10V), clock, and control logic. MN674A is packaged in a 28-pin DIP and contains all the interface logic necessary to directly mate to most popular 8 and 16-bit microprocessors. The 3-state output buffer connects directly to the μP's data bus and can be read either as one 12-bit word or as two 8-bit bytes. Chip select, chip enable, address decode (short cycle), and read/write (read/convert) control inputs enable MN674A to connect directly to system address bus and control lines and operate totally under processor control.

MN674A's combination of bipolar and CMOS technologies represents the latest advances in 574A/674A evolution, and all problems associated with previous models from other manufacturers have been solved. These devices are truly TTL compatible over all temperature ranges, and they are not prone to CMOS latch-up at power-on. Their internal clock has minimal drift, and conversion time is guaranteed over all temperature ranges. Bus access time is guaranteed not to exceed 150nsec, and the A_0 line may be toggled freely with no fear of output-data overlap thanks to break-before-make action on the output buffer. At 450mW max, power consumption is almost half that of competing devices.

MN674A is ideal for most military/aerospace and industrial, general-purpose, data-acquisition applications. The device is available in 5 different electrical grades fully specified for either 0°C to +70°C or −55°C to +125°C operation. Each device guarantees integral linearity and no missing codes as summarized below. Add "/B" to either the S or T grade units for environmental stress screening.

Model	Temperature Range	Linearity Error Max (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})
MN674AJ	0°C to +70°C	±1LSB	11 Bits
MN674AK	0°C to +70°C	±½LSB	12 Bits
MN674AL	0°C to +70°C	±½LSB	12 Bits
MN674AS	−55°C to +125°C	±1LSB	11 Bits
MN674AS/B*	−55°C to +125°C	±1LSB	11 Bits
MN674AT	−55°C to +125°C	±1LSB	12 Bits
MN674AT/B*	−55°C to +125°C	±1LSB	12 Bits

*Includes environmental stress screening.

MICRO NETWORKS
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MN674A μP-COMPATIBLE 15μsec 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN674AJ, K, L	0°C to +70°C
MN674AS, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+Vdd + 0.5) Volts
Analog Inputs: Pins 10, 12 and 13	±16.5 Volts
Pin 14	±24 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref. Out (Pin 8) Short Circuit Duration	Continuous to Ground Momentary to ±Vcc

ORDERING INFORMATION

PART NUMBER — MN674AX/B

Select suffix J, K, L, S or T for desired performance and specified temperature range.

Add "/B" suffix to S or T models for environmental stress screening.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	4.7	5	5.3	kΩ
0 to +20V, ±10V	9.4	10	10.6	kΩ
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8 (Note 2)				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Currents	−5	±0.1	+5	μA
Input Capacitance		5		pF
DIGITAL OUTPUTS DB0-DB11, STS (Note 2)				
Output Coding (Note 3): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 500\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 1.6mA$)			+0.4	Volts
Leakage (DB0-DB11) in High-Z State	−5	±0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10.0	+10.1	Volts
Drift		±10		ppm/°C
Output Source Current (Note 4)	2.0			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc	±11.4		±16.5	Volts
+Vdd	+4.5	+5	+5.5	Volts
Power Supply Rejection (See Performance Specifications)				
Current Drains: +Vcc Supply		+3.5	+5	mA
−Vcc Supply		−15	−20	mA
+Vdd Supply		+9	+15	mA
Power Consumption (±Vcc = ±15V)		325	450	mW
DYNAMIC CHARACTERISTICS				
Conversion Time (Notes 1, 2, 5): 8-Bit Cycle	6	8	10	μsec
12-Bit Cycle	9	12	15	μsec

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. Listed specifications guaranteed over each device's full operating temperature range as determined by part number suffix.
3. See table of transition voltages in section labeled Output Coding.
4. The internal reference can be used to drive an external load, and it is capable of supplying up to 2mA over and above the requirements of the reference-in and bipolar-offset resistors. The external load should not vary during a conversion. The reference output does not require a buffer when operating with ±12V supplies.
5. If a conversion is started with A_0 (pin 4) low, a full 12-bit conversion cycle is initiated. If A_0 is high, a shorter 8-bit conversion is initiated. Conversion time is defined as the width of the Status Output pulse. See the Timing sections for more details.
6. MN674AJ, AK, AL are fully specified for 0°C to +70°C operation. MN674AS, AT are fully specified for −55°C to +125°C operation.
7. Adjustable to zero with external potentiometer.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN674A on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Listed maximum change specifications (temperature coefficients) for unipolar offset, bipolar offset and full scale calibration error correspond to the maximum change from the initial value (+25°C) to the value at T_{min} or T_{max}.
10. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN674A on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
11. Listed specs assume a fixed 50Ω resistor between Ref Out (pin 8) and Ref In (pin 10). Full scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. Ideally, this digital output transition should occur at an analog voltage 1½LSB's below the nominal full scale voltage. See Digital Output Coding.
12. Listed spec is the max change in full scale calibration accuracy as supplies are varied over the range indicated.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PERFORMANCE SPECIFICATIONS (Typical at $T_A = +25°C$, $\pm Vcc = \pm 12V$ or $\pm 15V$, $+Vdd = +5V$ unless otherwise indicated)

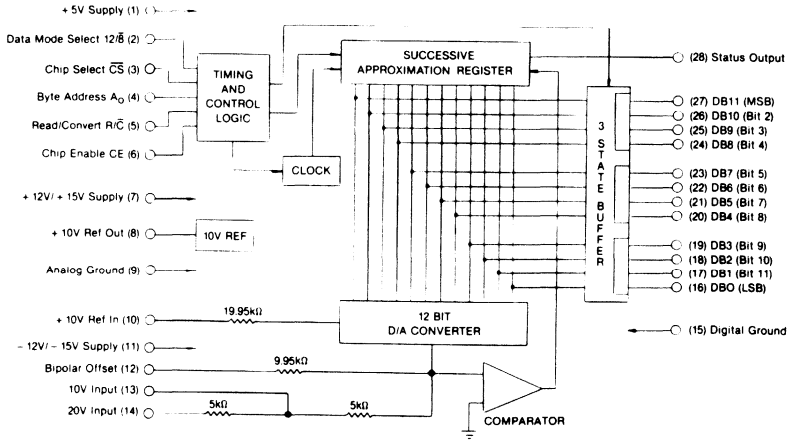
MODEL	674AJ	674AK	674AL	674AS	674AT	UNITS
Integral Linearity Error: Initial (+25°C) (Max)	±1	±½	±½	±1	±½	LSB
T_{min} to T_{max} (Max, Note 6)	±1	±½	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	11	12	12	11	12	Bits
T_{min} to T_{max} (Note 6)	11	12	12	11	12	Bits
Unipolar Offset Error (Notes 7, 8):						
Initial (+25°C) (Max)	±2	±2	±2	±2	±2	LSB
Drift (Max)	±10	±5	±5	±5	±2.5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±2	±1	LSB
Bipolar Offset Error (Notes 7, 10):						
Initial (+25°C) (Max)	±10	±4	±4	±10	±4	LSB
Drift (Max)	±10	±5	±5	±10	±5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±4	±2	LSB
Full Scale Calibration Error (Notes 7, 11):						
Initial (+25°C) (Max)	±0.25	±0.25	±0.25	±0.25	±0.25	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.47	±0.37	±0.3	±0.75	±0.5	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.22	±0.12	±0.05	±0.5	±0.25	%FSR
Drift (Max)	±50	±27	±10	±50	±25	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±9	±5	±2	±20	±10	LSB
Power Supply Rejection (Note 12)						
$+13.5V \le +Vcc \le +16.5V$ or $+11.4V \le +Vcc \le +12.6V$	±2	±1	±1	±2	±1	LSB
$-16.5V \le -Vcc \le -13.5V$ or $-12.6V \le -Vcc \le -11.4V$	±2	±1	±1	±2	±1	LSB
$+4.5V \le +Vdd \le +5.5V$	±½	±½	±½	±½	±½	LSB

ORDERING INFORMATION

Part Number	Specified Temperature Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	No Missing Codes Over Temp.	Max. Offset Drift (2)	Max. Full Scale Drift (2)	Max. Power (mW)
MN674AJ	0°C to +70°C	±1	±1	11 Bits	±10	±50	450
MN674AK	0°C to +70°C	±½	±½	12 Bits	±5	±27	450
MN674AL	0°C to +70°C	±½	±½	12 Bits	±5	±10	450
MN674AS	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN674AS/B (3)	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN674AT	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450
MN674AT/B (3)	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450

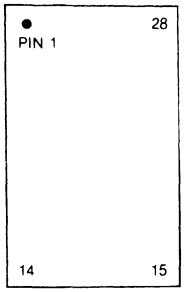
Maximum error expressed in LSB's for 12 bits.
Expressed in ppm of FSR/°C.
Includes environmental stress screening.

BLOCK DIAGRAM



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

PIN DESIGNATIONS



(1)	+5V Supply (+ V_{dd})	(28)	Status Output
(2)	Data Mode Select 12/$\overline{8}$	(27)	DB11 (MSB)
(3)	Chip Select $\overline{CS}$	(26)	DB10 (Bit 2)
(4)	Byte Address A_0	(25)	DB9 (Bit 3)
(5)	Read/Convert R/$\overline{C}$	(24)	DB8 (Bit 4)
(6)	Chip Enable CE	(23)	DB7 (Bit 5)
(7)	+12V/+15V Supply (+ V_{CC})	(22)	DB6 (Bit 6)
(8)	+10V Ref Out	(21)	DB5 (Bit 7)
(9)	Analog Ground	(20)	DB4 (Bit 8)
(10)	+10V Ref In	(19)	DB3 (Bit 9)
(11)	−12V/−15V Supply (− V_{CC})	(18)	DB2 (Bit 10)
(12)	Bipolar Offset	(17)	DB1 (Bit 11)
(13)	10V Input	(16)	DB0 (LSB)
(14)	20V Input	(15)	Digital Ground

DESCRIPTION OF OPERATION

The MN674A is a complete 12-bit A/D converter. It utilizes the successive approximation conversion technique and contains all required function blocks — successive approximation register (SAR), D/A converter, comparator, clock and reference — internal to its package. The MN674A mates directly to most popular 8, 16 and 32-bit microprocessors and contains all the necessary address decoding logic, control logic and 3-state output buffering to operate completely under processor control. In most applications, the MN674A will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete A/D conversion function. The completeness of this device makes it most convenient to think of the MN674A as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating the MN674A under microprocessor control (it also functions as a stand-alone A/D) consists, in most applications, of a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D and involves a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN674A's Status Output (also called Busy Line or End of Conversion (E.O.C.) Line) rises to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Output to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Output or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

If the MN674A is operated with 12-bit or wider microprocessors, all 12 output bits can be 3-state enabled simultaneously, permitting data collection with a single read operation. If the MN674A is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's), in a left justified format, with 4 trailing "0's".

APPLICATIONS INFORMATION

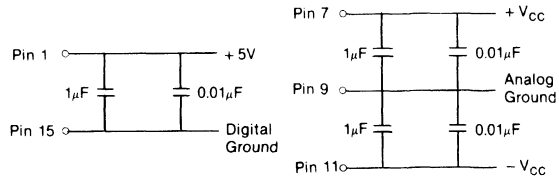
LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN674A. It is critically important that the MN674A's power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitors should be connected directly from pin 1 to pin 15 (Digital Ground), and the $+V_{CC}$ and $-V_{CC}$ supplies should be decoupled directly to pin 9 (Analog Ground). A suitable decoupling capacitor pair is usually a relatively large tantalum (1 − 10μF) in parallel with a smaller (0.01 − 1.0μF) ceramic disc.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN674A and associated analog input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the MN674A as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to the MN674A. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for the MN674A's internal reference. It should be connected as close as possible to the analog input signal reference point.

POWER SUPPLY DECOUPLING



CONTROL FUNCTIONS — Operating the MN674A under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN674A control-line functions. Table 2 is the MN674A Truth Table.

Unless Chip Enable (CE, pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$ and A_0) will have no effect on MN67[illegible]peration. When CE and $\overline{CS}$ are

Table 1: MN674A Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0→1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1→0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1→0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0→1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits) (Note 5)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

)th asserted, the signal applied to R/$\overline{C}$ (Read/Convert, pin 5) deter-ines whether a data read (R/$\overline{C}$="1") or a convert operation /$\overline{C}$="0") is initiated.

'hen initiating a conversion, the signal applied to A_0 (Byte Ad-ess/Short Cycle, pin 4) determines whether a 12-bit conversion initiated (A_0="0") or an 8-bit conversion is initiated (A_0="1"). It the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" or)" that initiates a convert operation. The actual conversion can ı initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the ling edge of R/$\overline{C}$ as shown in the Truth Table and as described the section labeled Timing — Initiating Conversions. When tiating conversions, the 12/$\overline{8}$ line is a "don't care".

hen reading digital output data from the MN674A, CE and $\overline{CS}$ must asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine ɜ format of output data. Logic "1" applied to the R/$\overline{C}$ line will initiate tual output data access. If the 12/$\overline{8}$ line is a "1", all 12 output data s will be accessed simultaneously when the R/$\overline{C}$ line goes from "0" to a "1".

he 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit tes as detailed in the section labeled Timing — Reading Output ta. In this situation, A_0="0" will result in the 8 MSB's being ac-ssed, and A_0="1" will result in the 4 LSB's and 4 trailing zeros ing accessed. In this mode, only the 8 upper bits or the 4 lower s can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled. The 4 LSB's then effectively present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23. See the section labeled Hardwiring to 8-Bit Data Buses.

Table 2: MN674A Truth Table

CONTROL INPUTS					MN674A OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (+2.0V minimum).
2. "0" indicates TTL logic zero (+0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicate logic transitions (edges).
5. Some vendors 674's required the 12/$\overline{8}$ line to be hard wired to either +5V (pin 1) or 0V (pin 15). The MN674A may be hard wired as such or driven with normal TTL signals.
6. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

TIMING — INITIATING CONVERSIONS — It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" (initiate 8-bit conversion) or A_0="0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may change simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60nsec). If it is desired that a particular one of these three inputs be responsible for starting the conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input.

Because the MN674A's control logic latches the A_0 signal upon conversion initiation, the A_0 line should be stable immediately prior to whichever of the above transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a read operation were occurring, and the result could be system

bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.

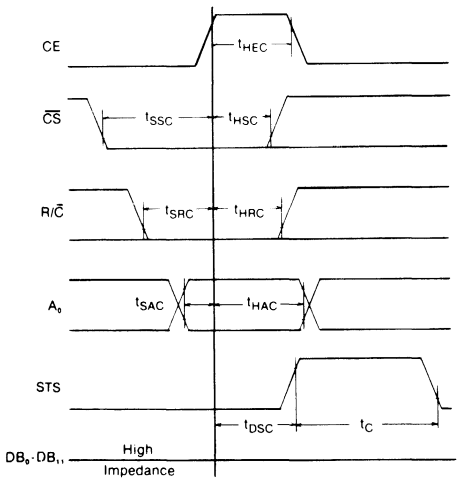
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE becoming a "1". This sequence can be accomplished in a number of ways including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent) and generating a CE 0→1 transition using the system clock. In this example, $\overline{CS}$ should be a "0" 50nsec prior to the CE transition (t_{SSC} =50nsec min), R/$\overline{C}$ should be a "0" 50nsec prior to the CE transition (t_{SRC} =50nsec min), and A_0 should be stable 0nsec prior to the CE transition (t_{SAC} =0nsec min). The minimum pulse width for CE="1" is 50nsec (t_{HEC} =50nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50nsec while CE="1" (t_{HSC} and t_{HRC} =50nsec min) to effectively initiate the conversion. Similarly, A_0 must be valid for at least 50nsec (t_{HAC} =50nsec min) while CE is high to effectively initiate the conversion. The Status Line rises to a "1" no later than 200nsec after the rising edge of CE (t_{DSC} =200nsec max). Once Status="1", additional convert commands will be ignored until ongoing conversion is complete.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status Output="1"), the MN674A's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates that the conversion is done, the combination of CE="1", $\overline{CS}$="0", and R/$\overline{C}$="1" is used to activate the buffer and read the digital output data. If the above combination of control signals is met and the 12/$\overline{8}$ line has a "1" applied, all twelve output bits will become valid simultaneously. If the 12/$\overline{8}$ line has a "0" applied, output data will be formatted for an 8-bit data bus. The 8 MSB's will become valid when the above conditions are met with A_0="0"; while the 8 LSB's (4 data bits and 4 trailing "0's") will become valid whenever A_0="1". If 12/$\overline{8}$="1", A_0 is a "don't care". If an 8-bit conversion is performed and all 12 output data bits are read, bit 9 (DB3) will be a "1", and bits 10-12 (DB2-DB0) will be "0's". Data access can be initiated by either the rising edge of CE or the falling edge of $\overline{CS}$.

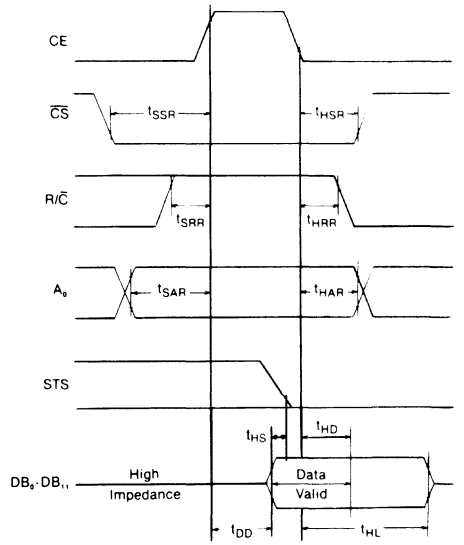
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50nsec prior to CE (t_{SSR} =50nsec min, t_{SAR} =50nsec min). R/$\overline{C}$ can become valid the same time as CE (t_{SRR} =0nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid typically 300nsec before the falling edge of Status as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TLL/CMOS compatible and may be actively driven.



Convert Start Timing



Read Cycle Timing

MN674A TIMING SPECIFICATIONS:

CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	50	20		ns
t_C	Conversion Time (Over Temp.)				
	8-Bit Cycle	6	8	10	μs
	12-Bit Cycle	9	12	15	μs

MN674A TIMING SPECIFICATIONS:

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE Low	50			ns
t_{HS}	STS Delay After Data Valid	100	300	600	ns

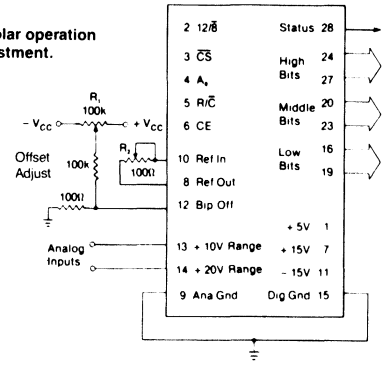
UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating modes are shown below. If the 0 to +10V input range is to be used, apply the analog input to pin 13. If the 0 to +20V range is used, apply the analog input to pin 14. If gain adjustment is not used, replace trim pot R_2 with a fixed, 50Ω ± 1%, metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, the actual transition will occur within ±2 LSB's of its ideal value (+½ LSB). For the 10V range, 1 LSB=2.44mV. For the 20V range, 1 LSB=4.88mV. To offset adjust, apply an analog input equal to +½ LSB and, with the MN674A continuously converting, adjust the offset potentiometer "down" until the digital output is all "0's" and then adjust "up" until the LSB "flickers" between "0" and "1".

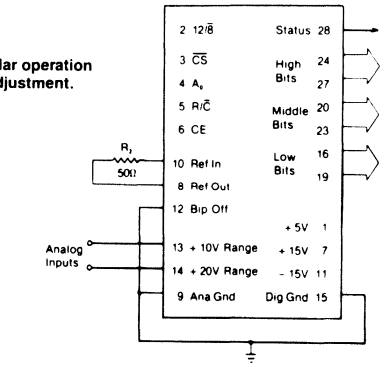
Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal full scale of the selected input range. This corresponds to +9.9963V and +19.9927V respectively for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer "up" until the digital outputs are all "1's" and then adjusting down until the LSB "flickers" between "1" and "0".

If a 10.24V (1 LSB=2.5mV) or a 20.48V (1 LSB=5mV) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor and a 200Ω trim pot (500Ω for 20.48V) inserted in series with the analog input to pin 13 (pin 14 for 20.48V). Offset trimming proceeds as described above. Gain trimming is now accomplished with the new pots. If one is not gain trimming and wishes to use fixed-value resistors, the values are 120Ω and 240Ω, respectively. MN674A's input impedance is laser trimmed to a typical accuracy of ±2%.

MN674A unipolar operation with trim adjustment.



MN674A unipolar operation without trim adjustment.

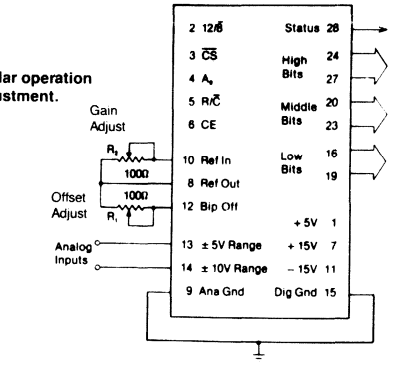


BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating modes are shown below. If the ±5V input range is to be used, apply the analog input to pin 13. If the ±10V range is used, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trim pots R_1 and R_2 should be replaced with fixed, 50Ω ±1%, metal-film resistors to meet all published specifications.

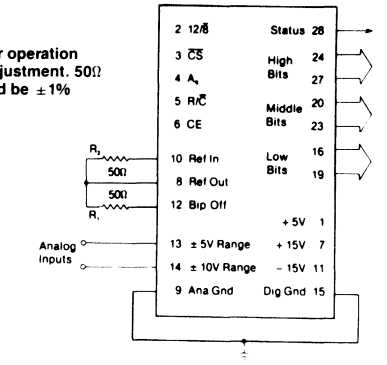
Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition should occur ½ LSB below zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the minus full scale point. The procedure is to apply an analog input equal to −FS+½ LSB (−4.9988V for the ±5V range, −9.9976V for the ±10V range) and adjust the bipolar offset trim pot "down" until the digital output is all "0's". Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal positive full scale value of the selected input range. This corresponds to +4.9963V and +9.9927V respectively for the ±5V and ±10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "up" until the digital outputs are all "1's" and then adjusting "down" until the LSB "flickers" between "1" and "0".

MN674A bipolar operation with trim adjustment.

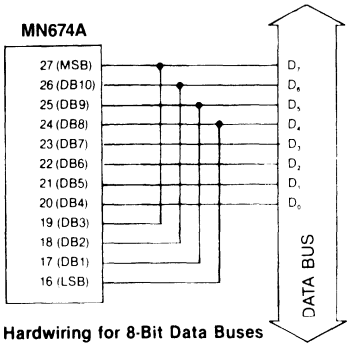


MN674A bipolar operation without trim adjustment. 50Ω resistors should be ±1% metal film.



HARDWIRING TO 8-BIT DATA BUSES — For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN674A output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte ($A_0 = 0$)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte ($A_0 = 1$)	DB3	DB2	DB1	DB0	0	0	0	0

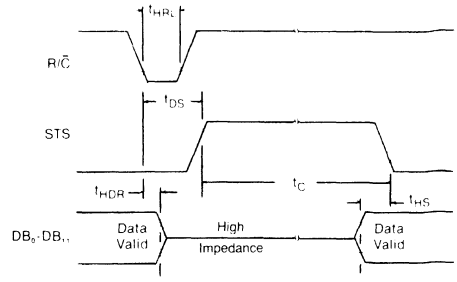


Hardwiring for 8-Bit Data Buses

STAND-ALONE OPERATION

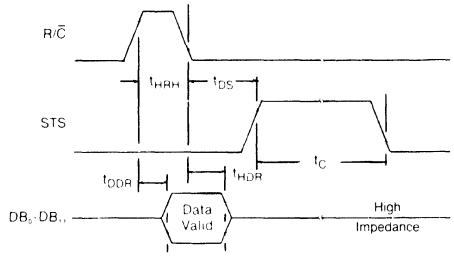
The MN674A can be used in a "stand-alone" mode in systems having dedicated input ports and not requiring full bus interface capability. In this mode, $\overline{CE}$ and 12/$\overline{8}$ are tied to logic "1" (they may be hard-wired to +5V), $\overline{CS}$ and A_0 are tied to logic "0" (they may be grounded), and the conversion is controlled by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low (assuming a conversion is not already in progress), and all 12 bits of the three-state output buffers are enabled whenever R/$\overline{C}$ is brought high (assuming Status has already gone low indicating conversion complete).

This gives rise to two possible modes of operation; conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. The timing diagram below details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The Status Output goes high 200ns after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 1000nsec after data is valid (t_{HS}). In this mode, output data is available "most of the time" and becomes invalid only during a conversion.



Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion

The timing diagram below details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible "most of the time" and becomes valid only when R/$\overline{C}$ is brought high.



High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to + 10V	0 to + 20V	± 5V	± 10V	MSB LSB
+ 10.0000	+ 20.0000	+ 5.0000	+ 10.0000	1111 1111 1111
+ 9.9963	+ 19.9927	+ 4.9963	+ 9.9927	1111 1111 111Ø*
+ 5.0012	+ 10.0024	+ 0.0012	+ 0.0024	1000 0000 000Ø*
+ 4.9988	+ 9.9976	− 0.0012	− 0.0024	ØØØØ ØØØØ ØØØØ*
+ 4.9963	+ 9.9927	− 0.0037	− 0.0073	0111 1111 111Ø*
+ 0.0012	+ 0.0024	− 4.9988	− 9.9976	0000 0000 000Ø*
0.0000	0.0000	− 5.0000	− 10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to + 10V or ± 5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For 0 to + 20V or ± 10V input ranges, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN674A operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of − 9.9976 volts. Subsequently, any input voltage more negative than − 9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of − 0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at + 9.9927 volts. An input more positive than + 9.9927 volts will give all "1's".

MICRO NETWORKS

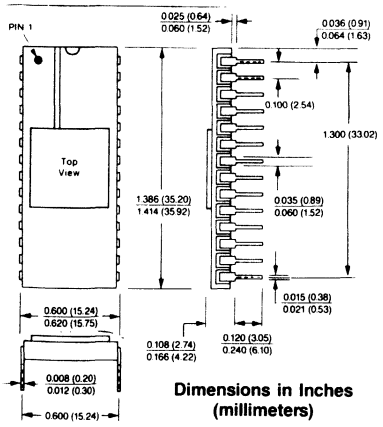
MN774

μP-COMPATIBLE
8μsec, 12-Bit
A/D CONVERTER

FEATURES

- **Complete, 8μsec, 12-Bit A/D Converter with Internal:**
  - **Clock**
  - **Reference**
  - **Control Logic**
- **HI-774A Pin and Function Compatible:**
  - **Faster (9μsec over Temp.)**
  - **Lower Power (450mW max)**
- **Full 8 or 16-Bit μP Interface:**
  - **Three-State Output Buffer**
  - **Chip Select, Address Decode**
  - **Read/Write Control**
- **±½LSB Linearity Guaranteed −55°C to +125°C (U Model)**
- **100kHz Sampling Rate with MN376 T/H Amplifier**
- **Operation with ±12V or ±15V Supplies**
- **28-Pin DIP**
- **Full Mil Operation −55°C to +125°C**

28-PIN CERAMIC DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN774 is the fastest device (8μsec) in Micro Networks MN574A/674A/774 Family of μP-interfaced, 12-bit ADC's. Like other devices in the Family, MN774 is a complete A/D with internal buried-zener reference (+10V), clock, and control logic. It is packaged in a 28-pin DIP that contains all the interface logic necessary to directly mate to most 8 and 16-bit μP's. Chip select, chip enable, address decode and read/write control inputs enable MN774 to connect directly to system address bus and control lines. The 3-state output buffer connects directly to the μP's data bus and can be read either as one 12-bit word or as two 8-bit bytes.

MN774 combines monolithic bipolar technology for its precision analog functions with CMOS technology for its high-speed logic functions. Its clock-oscillator circuit benefits from a current-controlled architecture that not only enables us to make a faster device but one whose conversion time is guaranteed over temperature (8.5μsec max 0°C to +70°C; 9μsec max −55°C to +125°C). Not only is the MN774 faster than competing devices, it consumes significantly less power (450mW max).

MN774 may be combined with a fast T/H such as MN376 (200nsec max acquisition time) to configure an impressive, fully μP controlled, sampling A/D capable of accurately digitizing full-scale signals at rates up to 100kHz. Such a configuration typically achieves signal-to-noise ratios (SNR's) of 72dB with harmonics down more than −80dB while digitizing signals with full-power bandwidths up to 500kHz.

MN774 is ideal for most military/aerospace and industrial, high-speed, data-acquisition applications. The device is available in 5 different electrical grades that guarantee integral linearity and no missing codes as summarized below.

Model	Temperature Range	Linearity Error Max (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})
MN774J	0°C to +70°C	±1LSB	11 Bits
MN774K	0°C to +70°C	±½LSB	12 Bits
MN774L	0°C to +70°C	±½LSB	12 Bits
MN774S	−55°C to +125°C	±1LSB	11 Bits
MN774S/B*	−55°C to +125°C	±1LSB	11 Bits
MN774T	−55°C to +125°C	±1LSB	12 Bits
MN774T/B*	−55°C to +125°C	±1LSB	12 Bits

*Includes environmental stress screening.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

December 1991
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MN774 μP-COMPATIBLE, 8μsec, 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN774J, K, L	0°C to +70°C
MN774S, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+Vdd + 0.5) Volts
Analog Inputs: Pins 10, 12 and 13	±16.5 Volts
Pin 14	±24 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref. Out (Pin 8) Short Circuit Duration	Continuous to Ground Momentary to ±Vcc

ORDERING INFORMATION

PART NUMBER — **MN774X/B**

Select suffix J, K, L, S or T for desired performance and specified temperature range.

Add "/B" suffix to S or T models for environmental stress screening.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	4.7	5	5.3	kΩ
0 to +20V, ±10V	9.4	10	10.6	kΩ
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8 (Note 2)				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Currents	−5	±0.1	+5	μA
Input Capacitance		5		pF
DIGITAL OUTPUTS DB0-DB11, STS (Note 2)				
Output Coding (Note 3): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 500\mu A$)	+2.4			Volts
Logic "0" ($I_{sink} \leq 1.6mA$)			+0.4	Volts
Leakage (DB0-DB11) in High-Z State	−5	±0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10.0	+10.1	Volts
Drift		±10		ppm/°C
Output Source Current (Note 4)	2.0			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc	±11.4		±16.5	Volts
+Vdd	+4.5	+5	+5.5	Volts
Power Supply Rejection (See Performance Specifications)				
Current Drains: +Vcc Supply		+3.5	+5	mA
−Vcc Supply		−15	−20	mA
+Vdd Supply		+9	+15	mA
Power Consumption (±Vcc = ±15V)		325	450	mW
DYNAMIC CHARACTERISTICS				
Conversion Time (Notes 1, 5): 8-Bit Cycle: +25°C		5	5.3	μsec
0°C to +70°C			5.7	μsec
−55°C to +125°C			6	μsec
12-Bit Cycle: +25°C		7.5	8	μsec
0°C to +70°C			8.5	μsec
−55°C to +125°C			9	μsec

SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. Listed specifications guaranteed over each device's full operating temperature range as determined by part number suffix.
3. See table of transition voltages in section labeled Output Coding.
4. The internal reference can be used to drive an external load, and it is capable of supplying up to 2mA over and above the requirements of the reference-in and bipolar-offset resistors. The external load should not vary during a conversion. The reference output does not require a buffer when operating with ±12V supplies.
5. If a conversion is started with A_0 (pin 4) low, a full 12-bit conversion cycle is initiated. If A_0 is high, a shorter 8-bit conversion is initiated. Conversion time is defined as the width of the S'atus Output pulse. See the Timing sections for more details.
6. MN774J, K, L are fully specified for 0°C to +70°C operation. MN774S, T are fully specified for −55°C to +125°C operation.
7. Adjustable to zero with external potentiometer.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN774 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Listed maximum change specifications (temperature coefficients) for unipolar offset, bipolar offset and full scale calibration error correspond to the maximum change from the initial value (+25°C) to the value at T_{min} or T_{max}.

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, ±Vcc = ±12V or ±15V, +Vdd = +5V unless otherwise indicated)

MODEL	774J	774K	774L	774S	774T	UNITS
Integral Linearity Error: Initial (+25°C) (Max)	±1	±½	±½	±1	±½	LSB
T_{min} to T_{max} (Max, Note 6)	±1	±½	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	11	12	12	11	12	Bits
T_{min} to T_{max} (Note 6)	11	12	12	11	12	Bits
Unipolar Offset Error (Notes 7, 8):						
Initial (+25°C) (Max)	±2	±2	±2	±2	±2	LSB
Drift (Max)	±10	±5	±5	±5	±2.5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±2	±1	LSB
Bipolar Offset Error (Notes 7, 10):						
Initial (+25°C) (Max)	±10	±4	±4	±10	±4	LSB
Drift (Max)	±10	±5	±5	±10	±5	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±2	±1	±1	±4	±2	LSB
Full Scale Calibration Error (Notes 7, 11):						
Initial (+25°C) (Max)	±0.25	±0.25	±0.25	±0.25	±0.25	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.47	±0.37	±0.3	±0.75	±0.5	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.22	±0.12	±0.05	±0.5	±0.25	%FSR
Drift (Max)	±50	±27	±10	±50	±25	ppm of FSR/°C
Max Change to T_{min} or T_{max} (Note 9)	±9	±5	±2	±20	±10	LSB
Power Supply Rejection (Note 12)						
+13.5V ≤ +Vcc ≤ +16.5V or +11.4V ≤ +Vcc ≤ +12.6V	±2	±1	±1	±2	±1	LSB
−16.5V ≤ −Vcc ≤ −13.5V or −12.6V ≤ −Vcc ≤ −11.4V	±2	±1	±1	±2	±1	LSB
+4.5V ≤ +Vdd ≤ +5.5V	±½	±½	±½	±½	±½	LSB

10. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN774 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
11. Listed specs assume a fixed 50Ω resistor between Ref Out (pin 8) and Ref In (pin 10) and a fixed 50Ω resistor between Ref Out (pin 8) and Bipolar Offset (pin 12, bipolar configurations) or Bipolar Offset grounded (unipolar configurations). Full scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. Ideally, this digital output transition should occur at an analog voltage 1½LSB's below the nominal full scale voltage. See Digital Output Coding.
12. Listed spec is the max change in full scale calibration accuracy as supplies are varied over the range indicated.

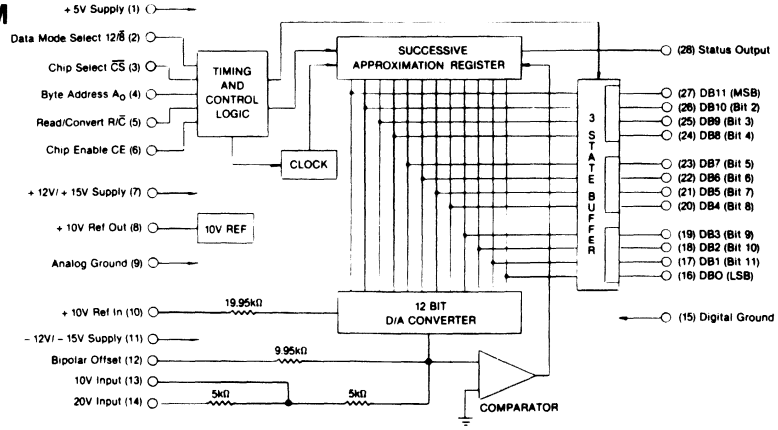
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

ORDERING INFORMATION

Part Number	Specified Temperature Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	No Missing Codes Over Temp.	Max. Offset Drift (2)	Max. Full Scale Drift (2)	Max. Power (mW)
MN774J	0°C to +70°C	±1	±1	11 Bits	±10	±50	450
MN774K	0°C to +70°C	±½	±½	12 Bits	±5	±27	450
MN774L	0°C to +70°C	±½	±½	12 Bits	±5	±10	450
MN774S	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN774S/B (3)	−55°C to +125°C	±1	±1	11 Bits	±5	±50	450
MN774T	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450
MN774T/B (3)	−55°C to +125°C	±½	±1	12 Bits	±2.5	±25	450

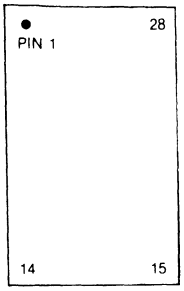
1. Maximum error expressed in LSB's for 12 bits. 2. Expressed in ppm of FSR/°C. 3. Includes environmental stress screening.

BLOCK DIAGRAM



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

PIN DESIGNATIONS



(1)	+ 5V Supply (+ V_{dd})	(28)	Status Output
(2)	Data Mode Select 12/$\overline{8}$	(27)	DB11 (MSB)
(3)	Chip Select $\overline{CS}$	(26)	DB10 (Bit 2)
(4)	Byte Address A_0	(25)	DB9 (Bit 3)
(5)	Read/Convert R/$\overline{C}$	(24)	DB8 (Bit 4)
(6)	Chip Enable CE	(23)	DB7 (Bit 5)
(7)	+ 12V/ + 15V Supply (+ V_{CC})	(22)	DB6 (Bit 6)
(8)	+ 10V Ref Out	(21)	DB5 (Bit 7)
(9)	Analog Ground	(20)	DB4 (Bit 8)
(10)	+ 10V Ref In	(19)	DB3 (Bit 9)
(11)	− 12V/ − 15V Supply (− V_{CC})	(18)	DB2 (Bit 10)
(12)	Bipolar Offset	(17)	DB1 (Bit 11)
(13)	10V Input	(16)	DB0 (LSB)
(14)	20V Input	(15)	Digital Ground

DESCRIPTION OF OPERATION

The MN774 is a complete 12-bit A/D converter. It utilizes the successive approximation conversion technique and contains all required function blocks — successive approximation register (SAR), D/A converter, comparator, clock and reference — internal to its package. The MN774 mates directly to most popular 8, 16 and 32-bit microprocessors and contains all the necessary address decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most applications, the MN774 will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete A/D conversion function. The completeness of this device makes it most convenient to think of the MN774 as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating the MN774 under microprocessor control (it also functions as a stand-alone A/D) consists, in most applications, of a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D and involves a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN774's Status Output (also called Busy Line or End of Conversion (E.O.C.) Line) rises to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Output to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Output or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

If the MN774 is operated with 12-bit or wider microprocessors, all 12 output bits can be 3-state enabled simultaneously, permitting data collection with a single read operation. If the MN774 is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's), in a left justified format, with 4 trailing "0's".

APPLICATIONS INFORMATION

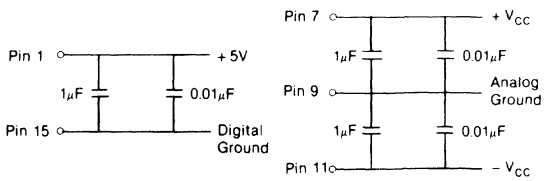
LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN774. It is critically important that the MN774's power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitors should be connected directly from pin 1 to pin 15 (Digital Ground), and the +V_{CC} and −V_{CC} supplies should be decoupled directly to pin 9 (Analog Ground). A suitable decoupling capacitor pair is usually a relatively large tantalum (1 − 10μF) in parallel with a smaller (0.01 − 1.0μF) ceramic disc.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN774 and associated analog input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the MN774 as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to the MN774. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for the MN774's internal reference. It should be connected as close as possible to the analog input signal reference point.

POWER SUPPLY DECOUPLING



CONTROL FUNCTIONS — Operating the MN774 under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN774 control-line functions. Table 2 is the MN774 Truth Table.

Unless Chip Enable (CE, pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$ and A_0) will have no effect on MN774 operation. When CE and $\overline{CS}$ are

Table 1: MN774 Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0→1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1→0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1→0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0→1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits) (Note 5)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

both asserted, the signal applied to R/$\overline{C}$ (Read/Convert, pin 5) determines whether a data read (R/$\overline{C}$="1") or a convert operation (R/$\overline{C}$="0") is initiated.

When initiating a conversion, the signal applied to A_0 (Byte Address/Short Cycle, pin 4) determines whether a 12-bit conversion is initiated (A_0="0") or an 8-bit conversion is initiated (A_0="1"). It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" or "0" that initiates a convert operation. The actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$ as shown in the Truth Table and as described in the section labeled Timing — Initiating Conversions. When initiating conversions, the 12/$\overline{8}$ line is a "don't care".

When reading digital output data from the MN774, CE and $\overline{CS}$ must be asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine the format of output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is a "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line goes from a "0" to a "1".

If the 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit bytes as detailed in the section labeled Timing — Reading Output Data. In this situation, A_0="0" will result in the 8 MSB's being accessed, and A_0="1" will result in the 4 LSB's and 4 trailing zeros being accessed. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled. The 4 LSB's then effectively present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23. See the section labeled Hardwiring to 8-Bit Data Buses.

Table 2: MN774 Truth Table

CONTROL INPUTS					MN774 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (+2.0V minimum).
2. "0" indicates TTL logic zero (+0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicate logic transitions (edges).
5. Some vendors 774's required the 12/$\overline{8}$ line to be hard wired to either +5V (pin 1) or 0V (pin 15). The MN774 may be hard wired as such or driven with normal TTL signals.
6. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

TIMING — INITIATING CONVERSIONS — It is the combination of CE="1", $\overline{CS}$="0", R/$\overline{C}$="0" and A_0="1" (initiate 8-bit conversion) or A_0="0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may change simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60nsec). If it is desired that a particular one of these three inputs be responsible for starting the conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input.

Because the MN774's control logic latches the A_0 signal upon conversion initiation, the A_0 line should be stable immediately prior to whichever of the above transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a read operation were occurring, and the result could be system

bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.

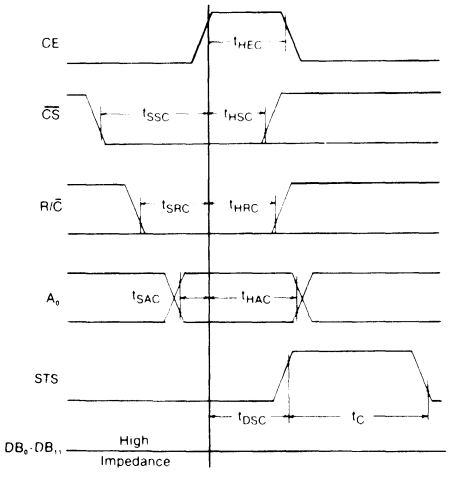
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE becoming a "1". This sequence can be accomplished in a number of ways including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent) and generating a CE 0→1 transition using the system clock. In this example, $\overline{CS}$ should be a "0" 50nsec prior to the CE transition (t_{SSC} =50nsec min), R/$\overline{C}$ should be a "0" 50nsec prior to the CE transition (t_{SRC} =50nsec min), and A_0 should be stable 0nsec prior to the CE transition (t_{SAC} =0nsec min). The minimum pulse width for CE="1" is 50nsec (t_{HEC} =50nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50nsec while CE="1" (t_{HSC} and t_{HRC} =50nsec min) to effectively initiate the conversion. Similarly, A_0 must be valid for at least 50nsec (t_{HAC} =50nsec min) while CE is high to effectively initiate the conversion. The Status Line rises to a "1" no later than 200nsec after the rising edge of CE (t_{DSC} =200nsec max). Once Status="1", additional convert commands will be ignored until ongoing conversion is complete.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status Output="1"), the MN774's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates that the conversion is done, the combination of CE="1", $\overline{CS}$="0", and R/$\overline{C}$="1" is used to activate the buffer and read the digital output data. If the above combination of control signals is met and the 12/$\overline{8}$ line has a "1" applied, all twelve output bits will become valid simultaneously. If the 12/$\overline{8}$ line has a "0" applied, output data will be formatted for an 8-bit data bus. The 8 MSB's will become valid when the above conditions are met with A_0="0"; while the 8 LSB's (4 data bits and 4 trailing "0's") will become valid whenever A_0="1". If 12/$\overline{8}$="1", A_0 is a "don't care". If an 8-bit conversion is performed and all 12 output data bits are read, bit 9 (DB3) will be a "1", and bits 10-12 (DB2-DB0) will be "0's". Data access can be initiated by either the rising edge of CE or the falling edge of $\overline{CS}$.

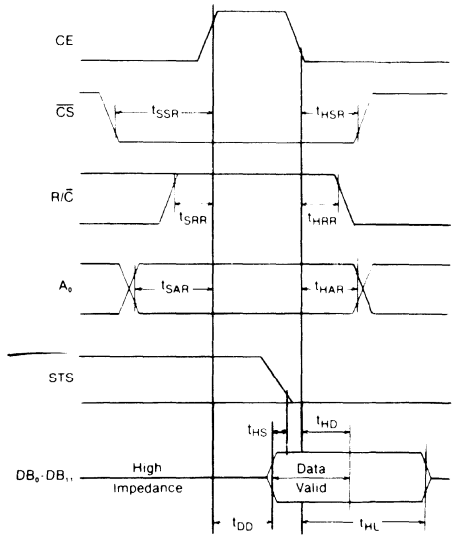
Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50nsec prior to CE (t_{SSR} =50nsec min, t_{SAR} =50nsec min). R/$\overline{C}$ can become valid the same time as CE (t_{SRR} =0nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid typically 150nsec before the falling edge of Status as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TLL/CMOS compatible and may be actively driven.



Convert Start Timing



Read Cycle Timing

MN774 TIMING SPECIFICATIONS:

CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	50	20		ns
t_C	Conversion Time (+25°C)				
	8-Bit Cycle		5	5.3	μs
	12-Bit Cycle		7.5	8	μs

MN774 TIMING SPECIFICATIONS:

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE Low	50			ns
t_{HS}	STS Delay After Data Valid		150	375	ns

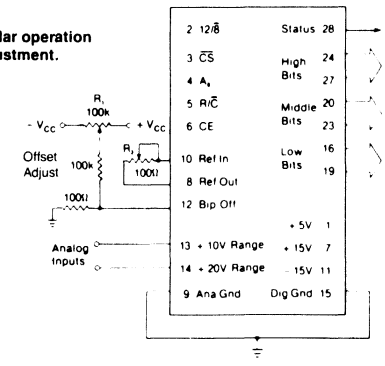
UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating modes are shown below. If the 0 to +10V input range is to be used, apply the analog input to pin 13. If the 0 to +20V range is used, apply the analog input to pin 14. If gain adjustment is not used, replace trim pot R_2 with a fixed, 50Ω ± 1%, metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, the actual transition will occur within ±2 LSB's of its ideal value (+½ LSB). For the 10V range, 1 LSB=2.44mV. For the 20V range, 1 LSB=4.88mV. To offset adjust, apply an analog input equal to +½ LSB and, with the MN774 continuously converting, adjust the offset potentiometer "down" until the digital output is all "0's" and then adjust "up" until the LSB "flickers" between "0" and "1".

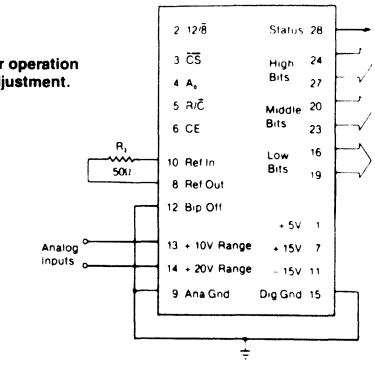
Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal full scale of the selected input range. This corresponds to +9.9963V and +19.9927V respectively for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer "up" until the digital outputs are all "1's" and then adjusting down until the LSB "flickers" between "1" and "0".

If a 10.24V (1 LSB=2.5mV) or a 20.48V (1 LSB=5mV) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor and a 200Ω trim pot (500Ω for 20.48V) inserted in series with the analog input to pin 13 (pin 14 for 20.48V). Offset trimming proceeds as described above. Gain trimming is now accomplished with the new pots. If one is not gain trimming and wishes to use fixed-value resistors, the values are 120Ω and 240Ω, respectively. MN774's input impedance is laser trimmed to a typical accuracy of ±2%.

MN774 unipolar operation with trim adjustment.



MN774 unipolar operation without trim adjustment.

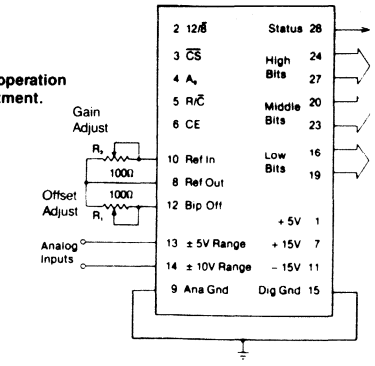


BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating modes are shown below. If the ±5V input range is to be used, apply the analog input to pin 13. If the ±10V range is used, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trim pots R_1 and R_2 should be replaced with fixed, 50Ω ±1%, metal-film resistors to meet all published specifications.

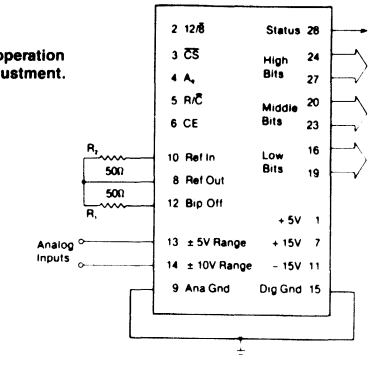
Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition should occur ½ LSB below zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the minus full scale point. The procedure is to apply an analog input equal to −FS+½ LSB (−4.9988V for the ±5V range, −9.9976V for the ±10V range) and adjust the bipolar offset trim pot "down" until the digital output is all "0's". Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal positive full scale value of the selected input range. This corresponds to +4.9963V and +9.9927V respectively for the ±5V and ±10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "up" until the digital outputs are all "1's" and then adjusting "down" until the LSB "flickers" between "1" and "0".

MN774 bipolar operation with trim adjustment.

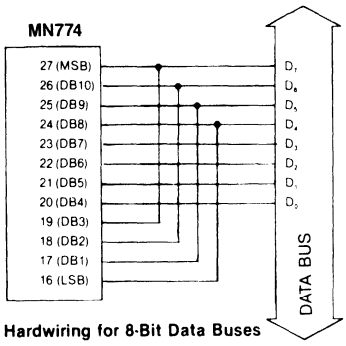


MN774 bipolar operation without trim adjustment.



HARDWIRING TO 8-BIT DATA BUSES — For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN774 output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte ($A_0 = 0$)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte ($A_0 = 1$)	DB3	DB2	DB1	DB0	0	0	0	0

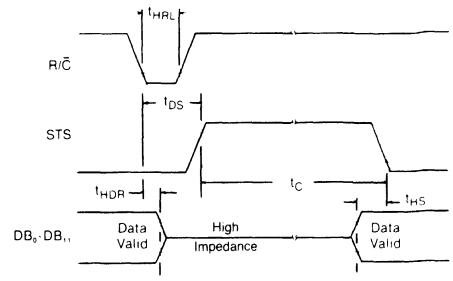


Hardwiring for 8-Bit Data Buses

STAND-ALONE OPERATION

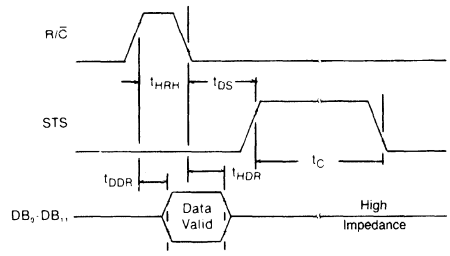
The MN774 can be used in a "stand-alone" mode in systems having dedicated input ports and not requiring full bus interface capability. In this mode, $\overline{CE}$ and 12/$\overline{8}$ are tied to logic "1" (they may be hardwired to +5V), $\overline{CS}$ and A_0 are tied to logic "0" (they may be grounded), and the conversion is controlled by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low (assuming a conversion is not already in progress), and all 12 bits of the three-state output buffers are enabled whenever R/$\overline{C}$ is brought high (assuming Status has already gone low indicating conversion complete).

This gives rise to two possible modes of operation; conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. The timing diagram below details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The Status Output goes high 200ns after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 375nsec after data is valid (t_{HS}). In this mode, output data is available "most of the time" and becomes invalid only during a conversion.



Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion

The timing diagram below details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible "most of the time" and becomes valid only when R/$\overline{C}$ is brought high.



High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid		150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to + 10V	0 to + 20V	± 5V	± 10V	MSB LSB
+ 10.0000	+ 20.0000	+ 5.0000	+ 10.0000	1111 1111 1111
+ 9.9963	+ 19.9927	+ 4.9963	+ 9.9927	1111 1111 111Ø*
+ 5.0012	+ 10.0024	+ 0.0012	+ 0.0024	1000 0000 000Ø*
+ 4.9988	+ 9.9976	− 0.0012	− 0.0024	ØØØØ ØØØØ ØØØØ*
+ 4.9963	+ 9.9927	− 0.0037	− 0.0073	0111 1111 111Ø*
+ 0.0012	+ 0.0024	− 4.9988	− 9.9976	0000 0000 000Ø*
0.0000	0.0000	− 5.0000	− 10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to + 10V or ± 5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For 0 to + 20V or ± 10V input ranges, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN774 operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of − 9.9976 volts. Subsequently, any input voltage more negative than − 9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of − 0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at + 9.9927 volts. An input more positive than + 9.9927 volts will give all "1's".

MICRO NETWORKS

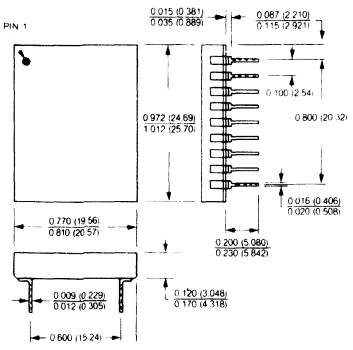
MN5065
MN5066

LOW-POWER, 8-Bit
A/D CONVERTERS

FEATURES

- **Low Power 84mW Maximum**
- **Single +12V Supply**
- **Small 18-Pin DIP**
- **CMOS/TTL Compatible**
- **Adjustment-Free No Gain and Offset Adjustment Necessary**
- **Full Mil Operation −55°C to +125°C**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5065 and MN5066 are extremely low-power, 8-bit, successive approximation analog-to-digital converters that may be operated from a single +12 Volt power supply. These converters are designed with CMOS logic and have power consumptions less than 84mW maximum. The MN5065 has a ±5V input range; the MN5066 has a 0 to +10V input range. Both devices are housed in small, convenient, 18-pin dual-in-line packages.

These A/D's are complete with internal reference and are actively laser trimmed as complete units eliminating the need for external adjusting potentiometers. Performance features include the following: ±½LSB linearity and "no missing codes" guaranteed over the entire operating temperature range, 100μsec conversion time, and ±2 LSB maximum absolute accuracy error over the entire operating temperature range.

MN5065 and MN5066 may be procured for operation over either the 0°C to +70°C or the −55°C to +125°C ("H" models) temperature range. For military/aerospace or harsh-environment commercial/industrial applications, MN5065H/B and MN5066H/B are available with optional Environmental Stress Screening.

MN5065 and MN5066 are excellent choices for remote battery-operated instrumentation, for portable test equipment, and for oceanographic and seismologic monitoring equipment. In these applications, adjustment-free operation and maximum specifications guaranteed over temperature assure field interchangeability without recalibration.

May 1988

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324 Clark St., Worcester, MA 01606 (508) 852-5400

MN5065 MN5066 LOW-POWER 8-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
Power Supplies (Pins 15, 18)	−0.5 to +16 Volts
Analog Inputs (Pin 9)	±15 Volts
Digital Inputs (Pins 12, 17)	−0.5 to + Logic Supply

ORDERING INFORMATION

PART NUMBER — MN5065H/B

Select MN5065 or MN5066 Model.
Standard part is specified for 0°C to +70°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" to "H" devices for Environmental Stress Screening.

SPECIFICATIONS (T_A = +25°C, Vdd = Vcc = 12V unless otherwise specified).

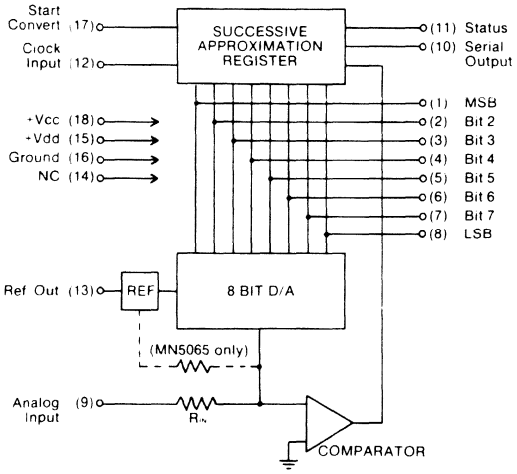
ANALOG INPUTS	+Vdd	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: MN5065			−5 to +5		Volts
MN5066			0 to +10		Volts
Input Impedance			50		KΩ
DIGITAL INPUTS					
Logic Levels (Note 1): Logic "1"	+ 5V	3.5			Volts
	+12V	8.4			Volts
Logic "0"	+ 5V			1.5	Volts
	+12V			3.5	Volts
Loading: Input Current			10		pA
Input Capacitance (Vin=0V)			5		pF
Start Convert Input: Pulse Width	+ 5V	750			nSec
	+12V	250			nSec
Setup Time Start High to Clock	+ 5V	300			nSec
	+12V	150			nSec
Clock Input: Frequency (Note 2)				85	KHz
Positive Pulse Width (Note 3)	+ 5V	600			nSec
	+12V	300			nSec
Rise and Fall Times (Note 3)	+ 5V			15	μSec
	+12V			4	μSec
TRANSFER CHARACTERISTICS					
Linearity Error (Note 4): +25°C			±¼	±½	LSB
0°C to +70°C			±¼	±½	LSB
−55°C to +125°C ("H" Models)				±½	LSB
Differential Linearity Error			±½		LSB
No Missing Codes		Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 5, 6):					
+25°C			±½	±1	LSB
0°C to +70°C			±1	±2	LSB
−55°C to +125°C ("H" Models)				±2	LSB
Zero Error (Notes 5, 6): +25°C			±¼	±½	LSB
0°C to +70°C			±½	±1	LSB
−55°C to +125°C ("H" Models)				±1	LSB
Gain Error (Note 5)			± 0.1		%
Gain Drift			±20		ppm/°C
DYNAMIC CHARACTERISTICS					
Conversion Time (Note 2)				100	μSec
Analog Input Settling Time (Note 8)			1.5		μSec
DIGITAL OUTPUTS					
Logic Coding (Note 9): MN5065		Complementary Offset Binary			
MN5066		Complementary Straight Binary			
Logic Levels (Note 1): Logic "1"	+ 5V	4.95			Volts
	+12V	11.95			Volts
Logic "0"	+ 5V			0.05	Volts
	+12V			0.05	Volts
Output Drive Capability:					
Parallel Outputs: Logic "1" (V_{OH}=2.5V)	+ 5V	−0.2	−1.7		mA
(V_{OH}=11V)	+12V	−0.2	−2.0		mA
Logic "0" (V_{OL}=0.4V)	+ 5V	+0.4	+1.6		mA
(V_{OL}=0.5V)	+12V	+1.0	+4.0		mA
Serial and Status Outputs: Logic "1" (V_{OH}=2.5V)	+ 5V	−0.2	−1.7		mA
(V_{OH}=11V)	+12V	−0.2	−2.0		mA
Logic "0" (V_{OL}=0.4V)	+ 5V	+0.2	+0.8		mA
(V_{OL}=0.5V)	+12V	+0.5	+2.0		mA

REFERENCE OUTPUT	+Vdd	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage			+ 6.3		Volts
Accuracy			± 5.		%
Tempco of Drift			±15.		ppm/°C
Ext. Current Without Buffering				10	μA
POWER SUPPLY REQUIRMENTS					
Power Supply Range: +Vcc (Pin 18)		+11.64	+12.00	+12.36	Volts
+Vdd (Pin 15)		+ 4.75		+12.36	Volts
Power Supply Rejection (Note 10):			± 0.01	± 0.04	%FSR/%Vs
Current Drain: +Vcc (Pin 18)			4.3	5.5	mA
+Vdd (Pin 15)	+ 5V		0.05	0.2	mA
	+12V		0.1	1.5	mA
Power Consumption (Vcc=12V)	+ 5V		52	67	mW
	+12V		53	84	mW

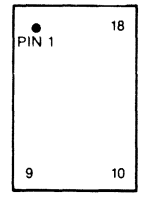
SPECIFICATION NOTES:

1. The +Vdd Logic Supply (Pin 15) can be at any voltage between +5V (low power TTL compatibility) and +12V (CMOS compatibility).
2. Conversion Time is defined as the width of the Converter's STATUS (E.O.C.) pulse. See Timing Diagram. For the MN5065 and the MN5066, a 100 μSec conversion time corresponds to an external clock frequency of 85KHz. Micro Networks guarantees linearity and absolute accuracy at and below this clock frequency.
3. The clock may be asymmetrical, and it may ramp up and down as long as it meets minimum pulse width and maximum rise and fall time requirements.
4. Micro Networks tests and guarantees maximum linearity error at room temperature and at the high and low extremes of the specified operating temperature range.
5. See the tutorial section of the Micro Networks Product Guide and Applications Manual for an explanation of how Micro Networks defines Full Scall Absolute Accuracy, Zero, and Gain Errors. For the MN5065 and MN5066 we 100% test Full Scale Absolute Accuracy and Zero Error at room temperature and at the high and low extreme of the specified operating temperature range.
6. 1 LSB for an 8 bit converter corresponds to 0.39% FSR. See Note 7.
7. FSR stands for Full Scale Range and is equal to the peak to peak input voltage of the converter. For both the MN5065 and MN5066, FSR = 10V, and 1 LSB = 39mV.
8. Analog Input Settling Time is the time required for the input circuitry to settle to within ±½ LSB for a 10V step in input signal.
9. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
10. PSRR is tested over a range of ±3% with Vcc = Vdd = + 12V.

BLOCK DIAGRAM



PIN DESIGNATIONS

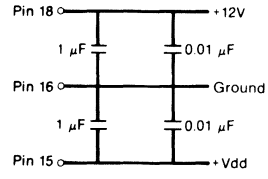


Pin 1 Bit 1 (MSB)	Pin 18 +Vcc Power Supply
Pin 2 Bit 2	Pin 17 Start Convert
Pin 3 Bit 3	Pin 16 Ground
Pin 4 Bit 4	Pin 15 +Vdd Logic Supply
Pin 5 Bit 5	Pin 14 N/C
Pin 6 Bit 6	Pin 13 Ref. Output (+6.3V)
Pin 7 Bit 7	Pin 12 Clock Input
Pin 8 Bit 8 (LSB)	Pin 11 Status (E.O.C.)
Pin 9 Analog Input	Pin 10 Serial Output

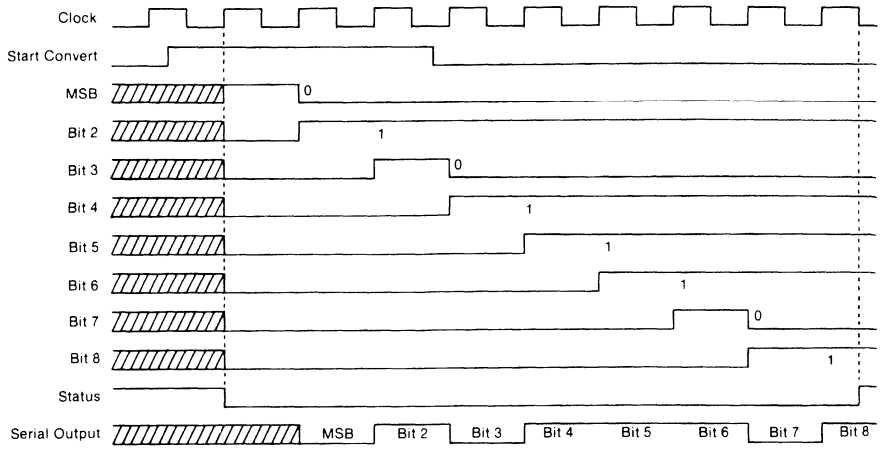
APPLICATIONS INFORMATION

The digital circuitry used in the MN5065 and MN5066 is CMOS. The standard precautionary measures for handling CMOS should be followed.

Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5065 and MN5066. The units' GROUND (Pin 16) should be connected to system analog ground, preferably through a large ground plane beneath the package. Power supplies should be decoupled with tantalum or electolytic capacitors located as close to the units as possible. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01 μF ceramic capacitors should be used as shown in the diagram below.



TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 1101 which corresponds to +6.328V on the 0 to +10V (MN5066) input range. See Output Coding.
2. Conversion Time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "1", all other bits = "0", STATUS = "0") by holding the START CONVERT high during a low to high clock transition; the START CONVERT must be high for a minimum of 300 nSec prior to the clock transition. Output bits, starting with the MSB, will be set to their final values on succeeding clock edges. The START CONVERT input does not have to return low for the conversion to continue.
4. The START CONVERT may be brought high at any time during a conversion to reset and begin converting again.
5. The delay between the resetting clock edge and the STATUS actually dropping to a "0" is 750 nSec maximum.
6. The STATUS (E.O.C.) output will rise to a "1" 750 nSec (maximum) after the first falling clock edge after the determination of LSB. STATUS will remain high until the converter is reset. Parallel output data is valid as long as STATUS is a "1".
7. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
8. For continuous conversion, connect the STATUS output pin (Pin 11) to the START CONVERT input (Pin 17). When the converter is initially "powered up", it may come on at any point in the conversion cycle.

OUTPUT CODING

The key points along an A/D converter's analog input/digital output transfer function are the transition voltages, the input voltages at which the digital outputs change from one state to the next. These are the points manufacturers look for when testing A/D accuracy and linearity. To test the Full Scale Absolute Accuracy of the MN5066, for example, we find the input voltage at which the digital outputs just change from 0000 0000 to 0000 0001. To test the Zero Error, we find the input voltage at which the digital outputs just change from 1111 1111 to 1111 1110. These and other transition voltages are listed below.

ANALOG INPUT (DC VOLTS)		DIGITAL OUTPUT
MN5065	MN5066	MSB LSB
+ 5.000	+10.000	0000 0000
+ 4.961	+ 9.961	0000 000Ø*
+ 0.039	+ 5.039	0111 111Ø
0.000	+ 5.000	0000 0000*
− 0.039	+ 4.961	1000 000Ø*
− 4.961	+ 0.039	1111 111Ø*
− 5.000	0.000	1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5065 (±5V analog input range) the transition from digital output 1111 1111 to 1111 1110 (or vice versa) will ideally occur at an input voltage of −4.961 volts. Subsequently, any input voltage more negative than −4.961 volts will give a digital output of all "1's". The transition from digital output 1000 0000 to 0111 1111 (or vice versa) will ideally occur at an input of zero volts, and the 0000 0000 to 0000 0001 (or vice versa) transition should occur at +4.961 volts. An input greater than +4.961 volts will give all "0's".

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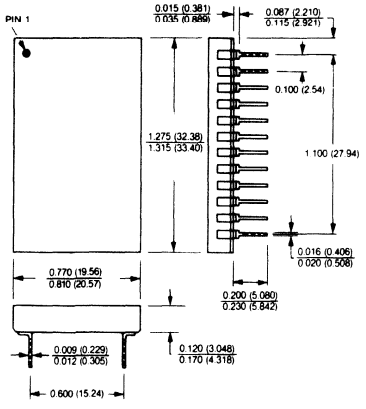
MN5100
MN5101

HIGH-SPEED
8-Bit A/D CONVERTERS

FEATURES

- **High Conversion Speed**
  900nsec MN5101
  1.5μsec MN5100
- **Small 24-Pin DIP**
- **±1/2LSB Linearity and No Missing Codes Over Temperature**
- **Parallel and Serial Outputs**
- **Adjustment-free No Gain or Offset Adjustments Necessary**
- **Fully Specified 0°C to +70°C (MN5100/5101) or −55°C to +125°C (MN5100/5101H or H/B)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5100 and MN5101 are very high-speed, 8-bit, successive approximation A/D converters. MN5100 guarantees a 1.5μsec conversion time, and MN5101 guarantees a 900nsec conversion time. Containing an internal reference and requiring only an external clock, these devices are much easier to use than other 8-bit A/D's in their speed class. Both devices are functionally laser trimmed and complement their speed performance with excellent linearity (±½ LSB max) and accuracy (±½ LSB max) specifications.These specifications are achieved without the need for external adjusting potentiometers and are guaranteed over the full specified temperature range. MN5100 and MN5101 are a simple solution to high-speed, low-resolution, digitizing requirements in single or multi-channel systems.

MN5100 and MN5101 are packaged in standard, 24-pin, double-wide, hermetically sealed, ceramic DIP's. Both devices are TTL compatible; have a low-drift, −6.3V internal reference; and offer 7 user-selectable input voltage ranges. Supply requirements are ±15V and +5V, and power consumption is 1550mW maximum.

Units are available and fully specified for 0°C to +70°C (MN5100 and MN5101) or −55°C to +125°C (MN5100H, H/B and MN5101H, H/B) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN5100H/B CH and MN5101H/B CH are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

Part Number	Conversion Time	Specified Temperature Range
MN5100	1.5μsec	0°C to +70°C
MN5100H	1.5μsec	−55°C to +125°C
MN5100H	1.5μsec	−55°C to +125°C
MN5100H/B CH	1.5μsec	−55°C to +125°C
MN5101	900nsec	0°C to +70°C
MN5101H	900nsec	−55°C to +125°C
MN5101H/B	900nsec	−55°C to +125°C
MN5101H/B CH	900nsec	−55°C to +125°C

MN5100/01

March 1988

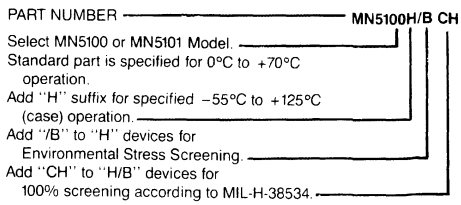
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MN5100 MN5101 HIGH-SPEED, 8-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN5100, MN5101	0°C to +70°C
MN5100H, MN5100H/B	−55°C to +125°C (case)
MN5101H, MN5101H/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 16)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 13)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 6)	−0.5 to +7 Volts
Analog Inputs (Pins 11, 12)	±25 Volts
Digital Inputs (Pins 23, 24)	−0.5 to +5.5 Volts

ORDERING INFORMATION



SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Positive		0 to +5, 0 to +10		Volts
Unipolar Negative		0 to −5, 0 to −10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Input Impedance (Notes 2, 3): 5V FSR		1.5		kΩ
10V FSR		3		kΩ
20V FSR		6		kΩ
DIGITAL INPUTS (Start, Clock)				
Logic Levels All Inputs: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Start: Logic "1" (V_{IH} = +2.4V)			+80	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
Clock: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Linearity Error (Note 4): Initial (+25° C)		±¼	±½	LSB
Over Temperature (Note 5)		±¼	±½	LSB
Full Scale Absolute Accuracy Error (Notes 4, 6):				
Initial (+25° C)		±¼	±½	LSB
0°C to +70°C		±½	±1	LSB
−55°C to +125°C		±1	±2	LSB
Unipolar Offset Error (Notes 4, 7):				
Initial (+25°C)		±¼	±½	LSB
0°C to +70°C		±½	±1	LSB
−55°C to +125°C		±1	±2	LSB
Bipolar Zero Error (Notes 4, 8):				
Initial (+25°C)		±¼	±½	LSB
0°C to +70°C		±½	±1	LSB
−55°C to +125°C		±1	±2	LSB
DIGITAL OUTPUTS				
Output Coding (Note 9): Unipolar Ranges		CSB		
Bipolar Ranges		COB		
Logic Levels All Outputs: Logic "1" (Isource ≤ 80μA)	+2.4			Volts
Logic "0" (Isink ≤ 3.2mA)			+0.4	Volts
REFERENCE OUTPUT				
Internal Reference (Note 2): Voltage		−6.3		Volts
Accuracy		±10		%
Tempco		±10		ppm/°C
External Current			200	μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 10): MN5100			1.5	μsec
MN5101			900	nsec
External Clock Frequency (Note 2): MN5100			5.33	MHz
MN5101			8.88	MHz
Clock Pulse Width (Note 2): High	20			nsec
Low	50			nsec
Setup Time Start Low to Clock (Note 2)	20			nsec

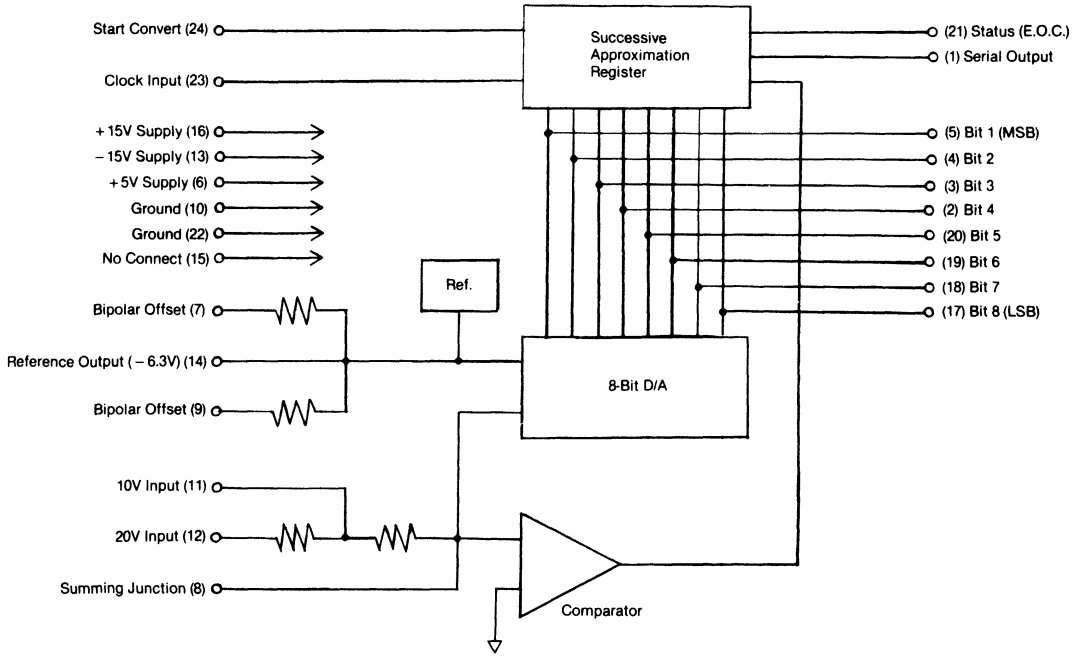
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
+5V Supply	+4.75	+5.00	+5.25	Volts
Power Supply Rejection (Notes 3, 11): +15V Supply		± 0.01		%FSR/%Supply
−15V Supply		± 0.03		%FSR/%Supply
+5V Supply		± 0.01		%FSR/%Supply
Current Drain: +15V Supply		+25	+35	mA
−15V Supply		−25	−35	mA
+5V Supply		+75	+100	mA
Power Consumption		1125	1550	mW

SPECIFICATION NOTES:

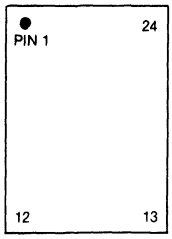
1. Listed specifications apply for all part numbers unless specifically indicated.
2. These parameters are listed for reference and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for ± 10V operation has a 20V FSR. A unit connected for 0 to + 10V, 0 to − 10V or ± 5V operation has a 10V FSR. A unit connected for 0 to + 5V, 0 to − 5V, or ± 2.5V operation has a 5V FSR.
4. 1 LSB for 8 bits in 20V FSR is 78mV.
   1 LSB for 8 bits in 10V FSR is 39mV.
   1 LSB for 8 bits in 5V FSR is 19.5mV.
5. Listed specifications apply over the 0°C to + 70°C temperature range for standard products, and over the − 55°C to + 125°C (case) range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale accuracy specifications apply at positive full scale for unipolar positive input ranges, at negative full scale for unipolar negative input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 for unipolar positive and bipolar input ranges. Additionally, it describes the accuracy of the 1111 1111 to 1111 1110 transition for unipolar negative and bipolar input ranges. The former transition ideally occurs at an input voltage 1 LSB below the nominal positive full scale voltage. The latter ideally occurs 1 LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 to 1111 1110 when operating MN5100/5101 on a unipolar positive range (0 to + 5V, 0 to + 10V) or from 0000 0000 to 0000 0001 when operating on a unipolar negative range (0 to − 5V or 0 to − 10V). The ideal value at which this transition should occur is + 1 LSB for unipolar positive ranges and − 1 LSB for unipolar negative ranges. See Digital Output Coding.
8. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating the MN5100/5101 on a bipolar range. The ideal value at which this transition should occur is 0 volts. See Digital Output Coding.
9. CSB = complementary straight binary. COB = complementary offset binary.
10. Conversion time is defined as the width of Status (E.O.C.).
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0000 to 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Serial Output	24	Start Convert
2	Bit 4	23	Clock Input
3	Bit 3	22	Ground
4	Bit 2	21	Status (E.O.C.)
5	Bit 1 (MSB)	20	Bit 5
6	+5V Supply (+Vdd)	19	Bit 6
7	Bipolar Offset	18	Bit 7
8	Summing Junction	17	Bit 8 (LSB)
9	Bipolar Offset	16	+15V Supply (+Vcc)
10	Ground	15	N.C.
11	10V Input	14	Reference Output (−6.3V)
12	20V Input	13	−15V Supply (−Vcc)

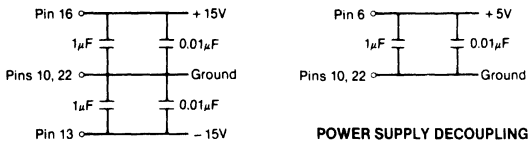
APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 24) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 21) is set to logic "1" (See Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the Status output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5100 Series converters. The units' two ground pins (pins 10 and 22) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.0[illegible]μF bypass capacitor should be connected between pins 10 and 22 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converter. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

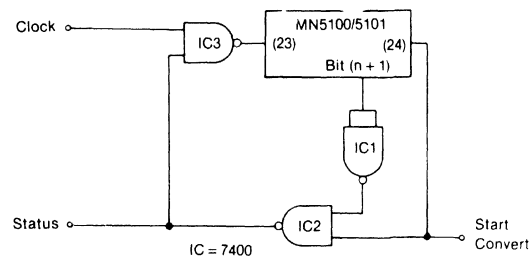


POWER SUPPLY DECOUPLING

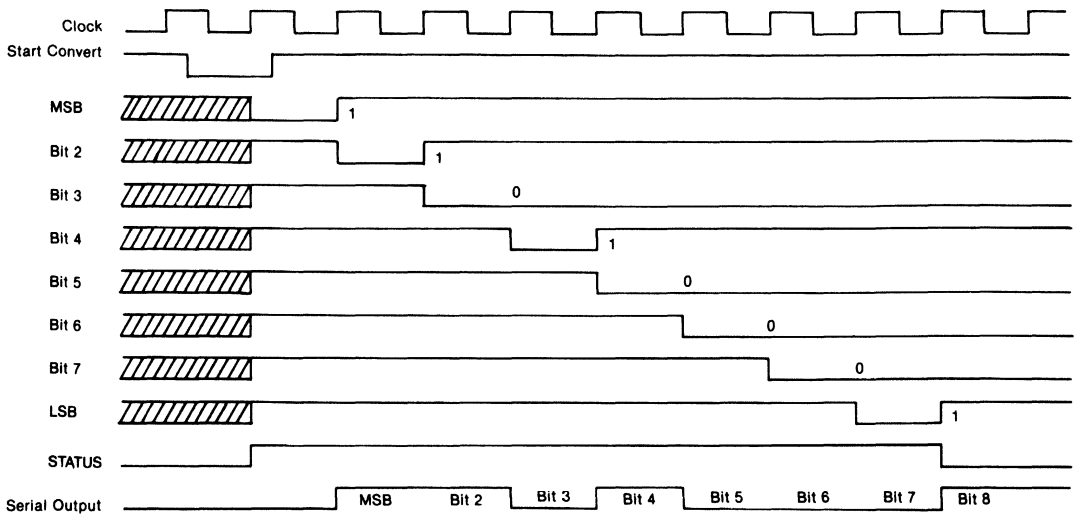
CONTINUOUS CONVERTING—The MN5100 Series A/D converters can be made to continuously convert by tying the Status output (pin 21) to the Start Convert input (pin 24). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output.

SHORT CYCLING—For applications requiring less than 8-bits resolution, the MN5100 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.

SHORT CYCLING SINGLE CONVERSION



TIMING DIAGRAM



TIMING DIAGRAM NOTES:

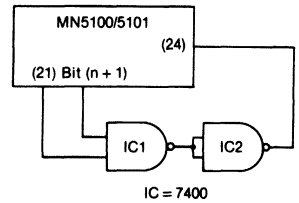
. Operation shown is for the digital word 1101 0001 which corresponds to −8.164V on the 0 to −10V input range. See Output Coding.
. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 20 nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the Start has returned high.
. The delay between the resetting clock edge and Status actually rising to a "1" is 50nsec maximum.
. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 50nsec (maximum) after the Status (E.O.C.) output has returned low. Parallel output data will remain valid and the Status output low until another conversion is initiated.
8. For continuous conversion, connect the Status output (pin 21) to the Start Convert input (pin 24). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

Assuming a conversion is already in progress, bit (n + 1) will go low as bit n is being set (see Timing Diagram). Since the Start Convert signal is high at this time, Status (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, Start Convert is brought low driving Status high and gating on the clock. The first rising clock edge the converter sees with Start Convert low will reset the converter bringing bit (n + 1) high again. Now Status will remain high as Start Convert is brought back high allowing the conversion to continue. Therefore, in this configuration, Status and Start Convert function normally, i.e., the same as Status and Start Convert for a converter not being short cycled.

SHORT CYCLING AND CONTINUOUS CONVERTING—A previous section described how continuous converting for n-bits could be accomplished by simply tying the Status output back to the Start Convert input. To continuously convert n bits, one simply has to tie the bit (n + 1) output back to the Start Convert input. The bit (n + 1) output acts like a status when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be voided by making the Start Convert input the AND function of bit (n + 1) and the Status output.

If one is already using the circuit described in the section labeled Short Cycling, one can short cycle and continuously convert by making the Start Convert input the AND function of Status (IC2) and Status (pin 21) outputs.

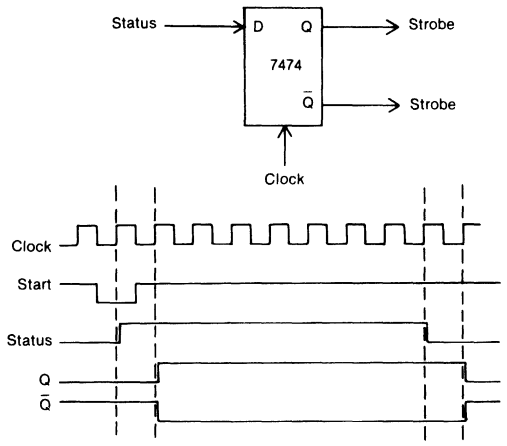
SHORT CYCLING CONTINUOUS CONVERTING



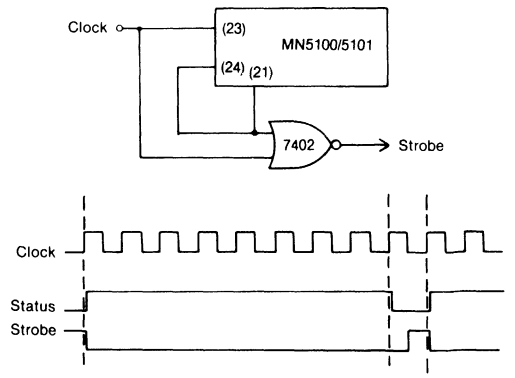
STATUS OUTPUT—The Status or End Of Conversion (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 50nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple

gate delays can be employed or the Status can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after Status changes.

LATCHING OUTPUT DATA



LATCHING DATA CONTINUOUS CONVERSIONS



If continuously converting, the Status (E.O.C.) output can be NORed with the converter clock, as shown above, to produce a positive strobe pulse ½ period wide, ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range						
	0 to −5V	0 to −10V	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect Input to Pin	11	11	11	11	11	11	12
Connect Pin 8 to Pin	12	Open	7, 9,12	7, 9	9,12	9	9
Connect Pin 7 to Pin	Ground	Ground	8, 9,12	8, 9	Ground	Ground	Ground
Connect Pin 9 to Pin	Ground	Ground	7, 8,12	7, 8	8,12	8	8
Input Impedance (kΩ)	1.5	3	1.5	3	1.5	3	6

DIGITAL OUTPUT CODING

Analog Input Voltage Range							Digital Outputs	
0 to −5V	0 to −10V	0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB	LSB
0.000	0.000	+5.000	+10.000	+2.500	+5.000	+10.000	0000	0000
−0.019	−0.039	+4.981	+9.961	+2.481	+4.961	+9.922	0000	000Ø
−2.481	−4.961	+2.519	+5.039	+0.019	+0.039	+0.078	0111	111Ø
−2.500	−5.000	+2.500	+5.000	0.000	0.000	0.000	ØØØØ	ØØØØ
−2.519	−5.039	+2.481	+4.961	−0.019	−0.039	−0.078	1000	000Ø
−4.981	−9.961	+0.019	+0.039	−2.481	−4.961	−9.922	1111	111Ø
−5.000	−10.000	0.000	0.000	−2.500	−5.000	−10.000	1111	1111

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +5V, 0 to −5V or ±2.5V input ranges, 1 LSB for 8 bits = 19.5mV.
4. For 0 to +10V, 0 to −10Vor ±5V input ranges, 1 LSB for 8 bits = 39mV.
5. For ±10V input range, 1 LSB for 8 bits = 78mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5100 operating on its ±10V input range, the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.922 volts. Subsequently, any input voltage more positive than +9.922 volts will give a digital output of all "0's". The transition from digital output 1000 0000 to 0111 1111 will ideally occur at an input of 0.000 volts, and the 1111 1111 to 1111 1110 transition should occur at −9.922 volts. An input more negative than −9.922 volts will give all "1's".

MICRO NETWORKS

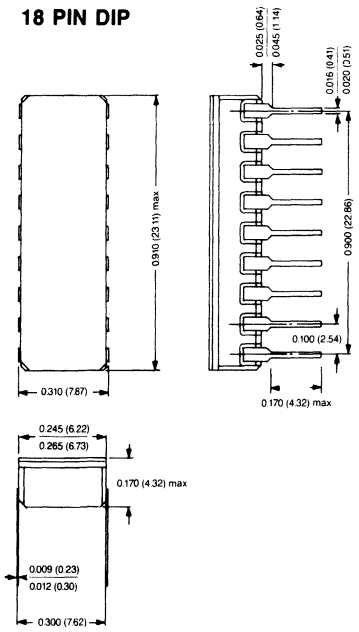
MN5120 Series
MN5130 Series
MN5140 Series

8-Bit A/D CONVERTERS

FEATURES

- **2.5μsec Maximum Conversion Time (MN5130, MN5140)**
- **Small 18-pin DIP**
- **±1/2 LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5120, MN5130 and MN5140 Series are a family of 8-bit, high-speed, successive approximation analog-to-digital converters in small, 18-pin, hermetically sealed dual-in-line packages. All devices incorporate our own thin-film resistor networks and are functionally laser trimmed as complete devices to meet all published specifications without external adjustments.

Each Series offers analog input ranges of 0 to +10V, 0 to −10V, ±5V and ±10V. MN5120 Series devices complete a conversion in 6μsec. MN5130 and MN5140 Series devices complete a conversion in 2.5μsec. The MN5120 and MN5130 Series devices operate from ±15V supplies. MN5140 devices operate from ±12V supplies. All units require a +5V logic supply.

These A/D's are fully specified and tested for linearity and accuracy at room temperature and at both the high and low extremes of the specified operating temperature range. Devices may be ordered for either 0°C to +70°C or −55°C to +125°C ("H" models) operation, and all guarantee ±1/2 LSB linearity over their entire operating temperature range. Full scale absolute accuracy is guaranteed to be better than ±1 LSB at +25°C and better than ±2LSBs over temperature. For military/aerospace or harsh-environment commercial/industrial application, "H/B CH" are fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

Low cost, 8-bit resolution and high conversion speeds make MN5120, MN5130 and MN5140 Series A/D's excellent choices for digitizing data in microprocessor-based systems for industrial-control and monitoring applications. Adjustment-free operation, accuracy and linearity specs guaranteed from −55°C to +125°C, and optional MIL-H-38534 screening make them excellent choices for military/aerospace and avionics applications.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

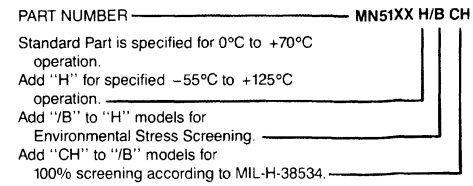
January 1992
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MN5120 MN5130 MN5140 SERIES 8-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
Positive Supply (+Vcc, Pin 1)	+18 Volts
Negative Supply (−Vcc, Pin 18)	−18 Volts
Logic Supply (+Vdd, Pin 12)	−0.5 to +7 Volts
Analog Input (Pin 2)	±15 Volts
Digital Inputs (Pins 8, 10)	−0.5 to +5.5 Volts

ORDERING INFORMATION



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated)

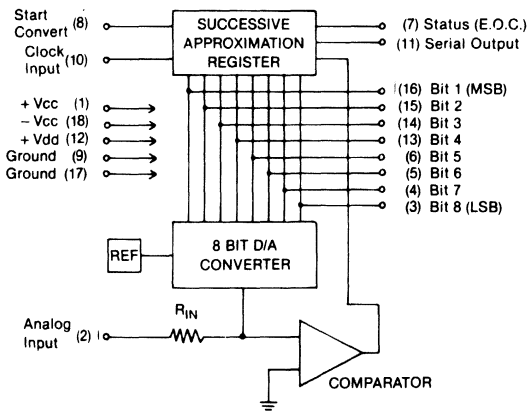
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: MN5120, MN5130, MN5140		0 to −10		Volts
MN5121, MN5131, MN5141		−5 to +5		Volts
MN5122, MN5132, MN5142		−10 to +10		Volts
MN5123, MN5133, MN5143		0 to +10		Volts
Input Impedance: MN5120, MN5130, MN5140		5		KΩ
MN5121, MN5131, MN5141		5		KΩ
MN5122, MN5132, MN5142		10		KΩ
MN5123, MN5133, MN5143		5		KΩ
DIGITAL INPUTS (ALL UNITS)				
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.8	Volts
Clock Input (Note 1): Pulse Width High	25			nSec
Pulse Width Low	50			nSec
Loading (Note 2)			1	TTL Load
Frequency (Note 3): MN5120 Series			1.33	MHz
MN5130 Series			3.2	MHz
MN5140 Series			3.2	MHz
Start Convert Input: Loading High (Note 2)			2	TTL Loads
Loading Low (Note 2)			1	TTL Load
Setup Time Start Low to Clock (Note 4)	20			nSec
DIGITAL OUTPUTS (ALL UNITS)				
Logic Levels: Logic "1"	2.4	3.6		Volts
Logic "0"		0.2	0.4	Volts
Output Coding (Note 5): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Output Drive Capability, All Outputs (Note 2): Logic "1"	11			TTL Loads
Logic "0"	5			TTL Loads
TRANSFER CHARACTERISTICS (ALL UNITS)				
Linearity Error (Note 6): 0°C to +70°C		±¼	±½	LSB
−55°C to +125°C ("H" Models)			±½	LSB
Differential Linearity Error		±½		LSB
No Missing Codes		Guaranteed Over Temperature		
Full Scale Absolute Accuracy Error (Notes 7, 8):				
+25°C		±½	±1	LSB
−55°C to +125°C (Note 10)		±1	±2	LSB
Zero Error (Notes 7, 8): +25°C		±¼	±1	LSB
−55°C to +125°C (Note 10)		±½	±1	LSB
Unipolar Offset Error, 0 to +10V Range (Notes 7, 8):				
+25°C		±¼	±1	LSB
−55°C to +125°C (Note 10)		±½	±1	LSB
Unipolar Offset Error, 0 to −10V Range (Notes 7, 8):				
+25°C		±½	±1	LSB
−55°C to +125°C (Note 10)		±1	±2	LSB
Bipolar Offset Error, ±5V and ±10V Ranges (Notes 7, 8):				
+25°C		±½	±1	LSB
−55°C to +125°C (Note 10)		±1	±2	LSB
Offset Drift (Note 9): 0 to +10V Range		±1		ppm of FSR/°C
0 to −10V Range		±10		ppm of FSR/°C
±5V and ±10V Ranges		±10		ppm of FSR/°C
Gain Error (Note 7)		±0.1		%
Gain Drift		±20		ppm/°C

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (Note 3): MN5120 Series MN5130 Series MN5140 Series			6 2.5 2.5	μSec μSec μSec
POWER SUPPLY REQUIREMENTS (ALL UNITS)				
Power Supply Range (Note 11): ± Vcc + Vdd	± 11 + 4.75	 + 5.00	± 17 + 5.25	Volts Volts
Power Supply Rejection (Note 11): + Vcc – Vcc		± 0.02 ± 0.01		%FSR/%Vs %FSR/%Vs
Current Drain (Note 11): + Vcc – Vcc + Vdd		12 – 10 70	16 – 18 100	mA mA mA
Power Consumption (All Units)		680	1010	mW

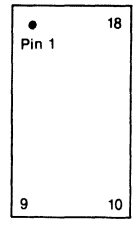
SPECIFICATION NOTES:

1. The clock may be asymmetrical with minimum positive or negative pulse width. See Note 3.
2. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
3. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) output pulse. See Timing Diagram. For the MN5120 series, the maximum conversion time of 6 μSec corresponds to an external clock frequency of 1.33 MHz. For the MN5130 and MN5140 series, the maximum conversion time of 2.5 μSec corresponds to an external clock frequency of 3.2 MHz. Micro Networks guarantees Absolute Accuracy and Linearity at and below these clock frequencies.
4. In order to reset the converter, START CONVERT must be brought low at least 20 nSec prior to a low to high clock transition. See Timing Diagram.
5. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding (page 8) and Timing Diagram.
6. Micro Networks tests and guarantees maximum linearity error at room temperature and at both extremes of the specified operating temperature range.
7. See Absolute Accuracy section below for explanation of how Micro Networks tests and specifies Absolute Accuracy, Offset, Gain and Zero Errors.
8. 1 LSB for an 8 bit converter corresponds to ± 0.39%FSR. See Note 9.
9. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ± 10V input range, FSR is 20 volts, and 1 LSB is equal to 78 mV. For the 0 to ± 10V and ± 5V ranges, FSR is 10 volts, and 1 LSB is equal to 39 mV.
10. For Commercial Models, this specification applies over the 0°C to + 70°C range. See Ordering Information.
11. For the MN5120 and MN5130 Series the positive and negative power supply (+ Vcc and – Vcc) requirements are + 15V and – 15V. For the MN5140 series the + Vcc and – Vcc requirements are + 12V and – 12V. All units will operate over a ± Vcc range of ± 11V to ± 17V with reduced accuracy, and all units require a + 5V logic supply (+ Vdd).

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Positive Supply (+ Vcc)	18	Negative Supply (– Vcc)
2	Analog Input	17	Ground
3	Bit 8 (LSB)	16	Bit 1 (MSB)
4	Bit 7	15	Bit 2
5	Bit 6	14	Bit 3
6	Bit 5	13	Bit 4
7	Status (E.O.C.)	12	+ 5V Supply (+ Vdd)
8	Start Convert	11	Serial Output
9	Ground	10	Clock Input

ABSOLUTE ACCURACY ERROR

A given digital output code is valid for a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated in the next column where portions of the theoretical analog input/digital output transfer function of the MN5122, MN5132, and MN5142 A/D converters (±10V input range) are sketched.

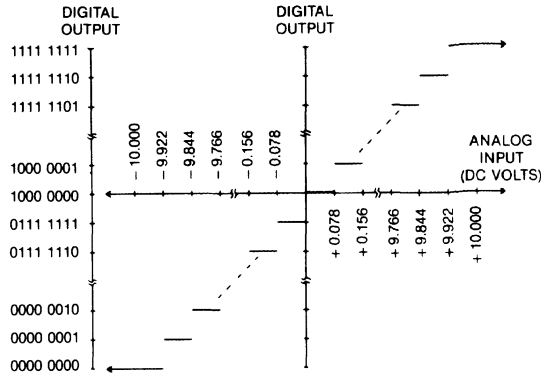
Notice that, ideally, any analog input between zero and +0.078V (1 LSB = 0.078 volts) will give a digital output of 1000 0000. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 1000 0000 digital code corresponds to analog inputs of +0.039V ±0.039V (+0.039V ± ½ LSB). The ± ½ LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error and its magnitude can be reduced only by going to higher resolution converters.

It is difficult and time consuming to measure the center of a quantization level (the +0.039 volts in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted*, analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR (see Note 9 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors.

For the MN5120/30/40 A/D Converters, we test Absolute Accuracy Error at both endpoints of unipolar input ranges and at both endpoints and the midpoint of bipolar input ranges. These tests are performed at room temperature and at the high and low extremes of the specified operating temperature range. The specifications appear in the table as the Full Scale Absolute Accuracy and Zero Errors.

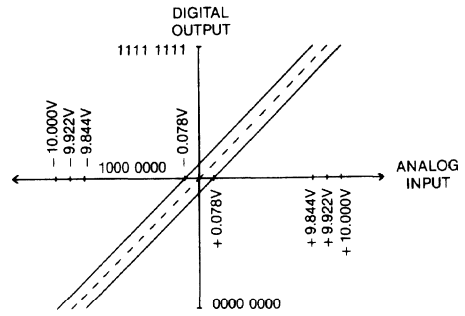
EXAMPLE: Return to the ideal analog input/digital output transfer function of the MN5122, MN5132, and MN5142 sketched above. Notice that the digital output data should change from 0000 0000 to 0000 0001 when the input voltage increases from −10.000V to −9.922V. It should change from 0000 0001 back to 0000 0000 as the input voltage is decreased from some more positive voltage to −9.922V. This voltage, −9.922V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "0". The 0111 1111 to 1000 0000 transition (the major transition) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "1", is ideally +9.922V.

For the MN5122H, MN5132H, and MN5142H (±10V input range, −55°C to +125°C operation), Micro Networks measures the three transition voltages just discussed at −55°C, +25°C, and +125°C. We guarantee that the positive and negative full scale LSB transition voltages will be within ±1 LSB (±78mV) of their ideal values at +25°C and within ±2 LSB's (±156mV)of their ideal values over the entire −55°C to +125°C operating temperature range. This is our Full Scale Absolute Accuracy Error specification. We also guarantee that the major transition voltage will be within ±1 LSB (±78mV) of its ideal value (zero volts) over the entire −55°C to +125°C operating temperature range. This is our Zero Error specification.

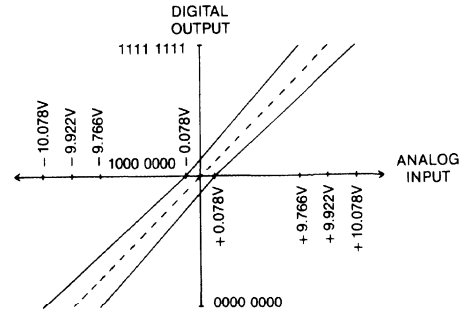


These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5122H, MN5132H, and MN5124H, that the actual transfer function will be ± ½ LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at −55°C and +125°C.

For temperatures intermediate to +25°C and −55°C or +125°C, maximum absolute accuracy errors can be interpolated. At +75°C, for example, Full Scale Absolute Accuracy Error will be ±1.5 LSB's.



ABSOLUTE ACCURACY +25°C



ABSOLUTE ACCURACY −55°C, +125°C

Unipolar and Bipolar Offset Errors are both Absolute Accuracy Errors. Their definitions differ with respect to where along the converter's analog input/digital output transfer function the errors are to be measured, i.e., different analog errors are measured at different digital output code transitions.

OFFSET ERROR—Space does not permit a theoretical discussion of the definitions and origins of Offset Error. Suffice it to say that for the MN5120, MN5130, and MN5140 Series A/D's, Offset Error is the difference between the ideal and the actual input voltages at which the 0000 0000 to 0000 0001 output transition takes place. It is the Absolute Accuracy Error measured for the 0000 0000 to 0000 0001 transition. For the MN5123, MN5133, and MN5143 converters (0 to +10V input range), Unipolar Offset Error is the same as Zero Error, and it indicates how accurate the converters will be when the analog input is around zero volts. For the MN5120, MN5130, and MN5140 converters (0 to −10V input range), Unipolar Offset Error is equivalent to Full Scale Absolute Accuracy Error, and it indicates how accurate the converters will be around −10 volts. For the bipolar converters (±5V and ±10V input ranges), Bipolar Offset Error is also equivalent to Full Scale Absolute Accuracy Error, and it indicates how accurate the converters will be around their negative full scale input points.

It is redundant to specify Offset Errors after specifying Full Scale Absolute Accuracy and Zero Errors the way Micro Networks does. We have provided the Offset Error specs to simplify comparing the MN5120, MN5130, and MN5140 Series to other 8 bit A/D's. Be sure you clearly understand each manufacturer's specification definitions before you compare converters solely on a data sheet basis.

GAIN ERROR—Gain Error is the difference between the ideal and the measured values of a converter's Full Scale Range (minus 2 LSB); it is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 1111 1110 to 1111 1111 transition minus that measured for the 0000 0000 to 0000 0001 transition.

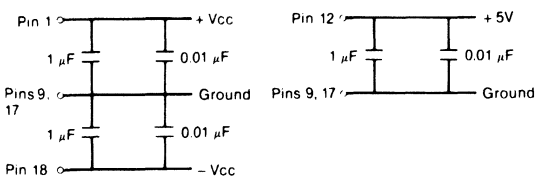
See the Converter Tutorial Section of the Micro Networks Applications Manual and Product Guide for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5120, MN5130, and MN5140 Series converters. The units' two GROUND pins (pins 9 and 17) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 9 and 17 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

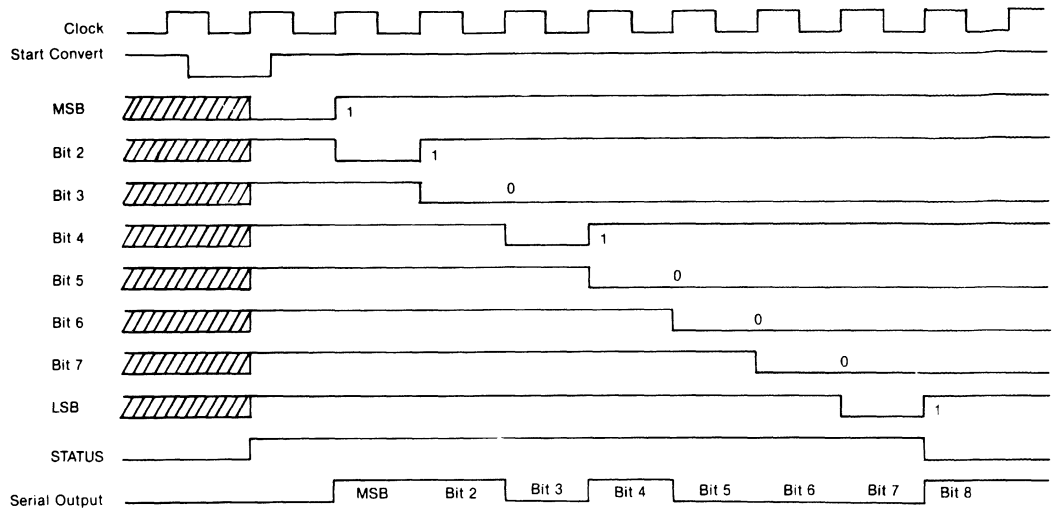
POWER SUPPLY DECOUPLING



DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's START CONVERT (Pin 8) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the STATUS output (Pin 7) is set to logic "1" (See Timing Diagram). The START CONVERT must now be brought high again for the conversion to continue. If the START is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the START has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the STATUS output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

TIMING DIAGRAM



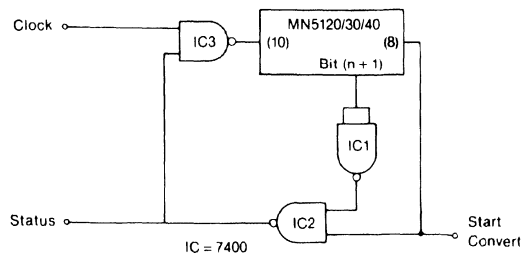
TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0001 which corresponds to 8.164V on the 0 to +10V (MN5123/33/43) input range. See Output Coding.
2. Conversion Time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 20 nSec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 50 nSec maximum.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 50 nSec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated.
8. For continuous conversion, connect the STATUS output pin (Pin 7) to the START CONVERT input (Pin 8). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

CONTINUOUS CONVERTING—The MN5120/30/40 Series A/D converters can be made to continuously convert by tying the STATUS output (Pin 7) to the START CONVERT input (Pin 8). In this configuration, STATUS (START CONVERT) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing STATUS (START CONVERT) high again. The MSB will be set on the next rising clock edge. The result is that the STATUS will go low for approximately one clock period following each conversion. Please read the section describing the STATUS output. See page 7 for continuous conversions while short cycling.

SHORT CYCLING — For applications requiring less than 8 bits resolution, the MN5120/30/40 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.

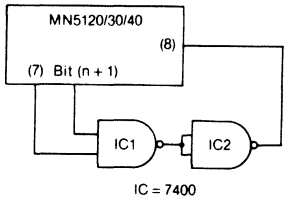
SHORT CYCLING SINGLE CONVERSION



Assuming a conversion is already in progess, bit (n + 1) will go low as bit n is being set (see Timing Diagram). Since the START CONVERT signal is high at this time, STATUS (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, START CONVERT is brought low driving STATUS high and gating on the clock. The first rising clock edge the converter sees with START CONVERT low will reset the converter bringing bit (n + 1) high again. Now STATUS will remain high as START CONVERT is brought back high allowing the conversion to continue. Therefore, in this configuration, STATUS and START CONVERT function normally, i.e., the same as STATUS and START CONVERT for a converter not being short cycled.

SHORT CYCLING AND CONTINUOUS CONVERTING — A previous section described how continuous converting for 8 bits could be accomplished by simply tying the STATUS output back to the START CONVERT input. To continuously convert at n bits, one simply has to tie the bit (n + 1) output back to the START CONVERT input. The bit (n + 1) output acts like a STATUS when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be avoided by making the START CONVERT input the AND function of bit (n + 1) and the STATUS output.

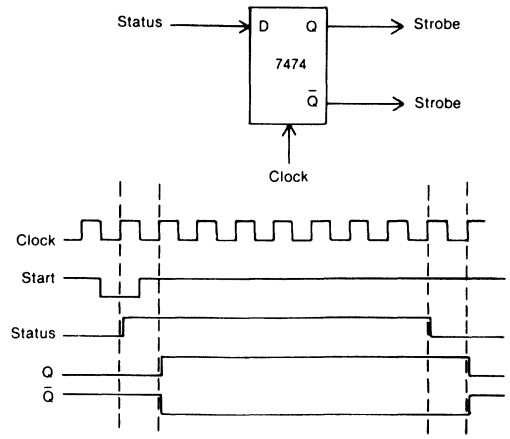
SHORT CYCLING CONTINUOUS CONVERTING



If one is already using the circuit described in the section labeled SHORT CYCLING, one can short cycle and continuously convert by making the START CONVERT input the AND function of STATUS (IC2) and STATUS (pin 7) outputs.

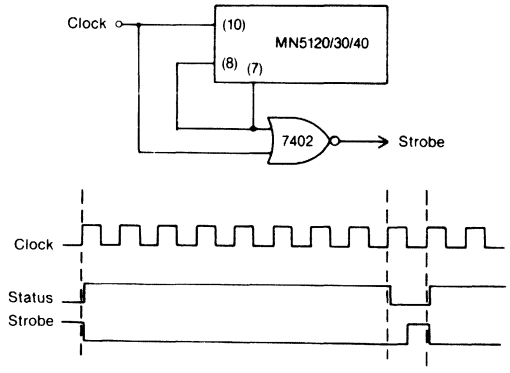
STATUS OUTPUT—The STATUS or END OF CONVERSION (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 50 nSec after STATUS has returned low. Therefore, an adequate delay must be provided if STATUS is to be used to strobe latches to hold output data. Simple gate delays can be employed or the STATUS can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after STATUS changes.

LATCHING OUTPUT DATA



If continuously converting, the STATUS (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse ½ period wide, ½ period after the STATUS output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

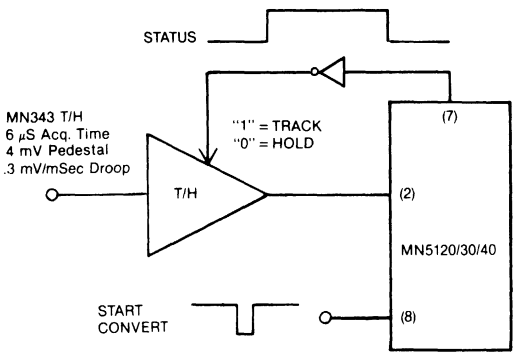
LATCHING DATA CONTINUOUS CONVERSIONS



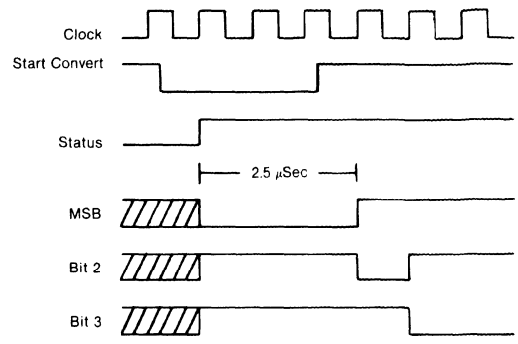
USING A TRACK AND HOLD AMP WITH MN5120/30/40 A/D's —The error that results when trying to convert moving analog signals with a successive approximation A/D can be as great as the amount the analog signal changes during a single A/D conversion time. If this error is unacceptable, a Track and Hold (T/H) or Sample and Hold (S/H) amplifier can be placed between the analog signal source and the A/D converter. A careful error analysis will be necessary to determine if the T/H is actually reducing and not increasing overall error. T/H parameters such as aperture uncertainty, gain accuracy, pedestal error and droop rate will have to be contended with (see the tutorial section of the Micro Networks' Applications Manual and Product Guide for a complete discussion of T/H parameters).

Normally, the T/H can be controlled directly by the A/D's STATUS output. Typical connections are shown on the next page. The STATUS output changes from a "0" to a "1" when the converter is reset. This drives the T/H from the track to the hold mode. At the end of conversion, STATUS returns to a "0" restoring the T/H to the track mode.

DRIVING A TRACK AND HOLD



Recall that if the START CONVERT pulse is brought high immediately after the converter has been reset, the MSB will be finalized one clock period later (see Timing Diagram). Care should be taken to ensure that aperture delay time and track-to-hold settling time do not contribute errors. If necessary, the width of the START CONVERT pulse can be increased to allow more time between the T/H being commanded into the hold mode (STATUS = "1") and the MSB being set. Recall that output bits do not begin to get set until after the START CONVERT has returned high. The example below shows a 2.25 μSec delay to allow for track to hold settling. Clock frequency = 1.33 MHz; 1 period = 0.75 μSec.



INPUT VOLTAGE AND OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT	
MN5120,30,40 0 to −10V	**MN5121,31,41 ±5V**	**MN5122,32,42 ±10V**	**MN5123,33,43 0 to +10V**	**MSB**	**LSB**
0.000	+5.000	+10.000	+10.000	1111	1111
−0.039	+4.961	+9.922	+9.961	1111	111ϕ*
−4.961	+0.039	+0.078	+5.039	1000	000ϕ*
−5.000	0.000	0.000	+5.000	ϕϕϕϕ	ϕϕϕϕ*
−5.039	−0.039	−0.078	+4.961	0111	111ϕ*
−9.961	−4.961	−9.922	+0.039	0000	000ϕ*
−10.000	−5.000	−10.000	0.000	0000	0000

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as ϕ will change from "1" to a "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages.

EXAMPLE: For an MN5122 (±10V analog input range) the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.922 volts. Subsequently, any input voltage more negative than −9.922 volts will give a digital output of all "0's". The transition from digital output 0111 1111 to 1000 0000 will ideally occur at an input of zero volts, and the 1111 1110 to 1111 1111 transition should occur at +9.922 volts. An input greater than +9.922 volts will give all "1's".

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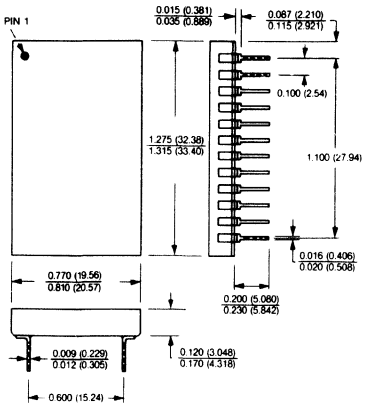
MN5150

HIGH-SPEED
8-Bit A/D CONVERTER
with 3-STATE OUTPUTS

FEATURES

- **Fast 2.5μsec Conversion Time**
- **3-State Output Buffer**
- **±1/2LSB Linearity and No Missing Codes Over Temperature**
- **Adjustment-Free No Gain or Offset Adjustments Necessary**
- **Fully Specified 0°C to +70°C (MN5150) or −55°C to +125°C (MN5150H and MN5150H/B)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5150 is a high-speed, 8-bit, successive approximation analog-to-digital converter with a three-state output buffer for easy interfacing to microprocessor and microcomputer data buses. Other performance features include a 2.5μsec maximum conversion time, ±½LSB linearity and "no missing codes" guaranteed over the entire operating temperature range, and ±1LSB unadjusted absolute accuracy. Convenience features include hermetic dual-in-line packaging, 7 user-selectable input ranges, and thanks to the stability of our own laser-trimmed thin-film resistor networks, the absence of external gain and offset adjusting potentiometers.

Units are available for either 0°C to +70°C or −55°C to +125°C operation with performance fully specified and guaranteed over the entire operating temperature range. High reliability processing, screening and qualification according to Method 5008 of MIL-STD-883 are available for military/aerospace applications.

Units are available for either 0°C to +70°C or −55°C to +125°C operation with performance fully specified and guaranteed over the entire operating temperature range. High-reliability processing, screening and qualification according to MIL-H-38534 are available for military/aerospace applications.

MN5150's 3-state output buffer simplifies interfacing to microprocessor and microcomputer data buses. In memory-mapped applications, MN5150 looks like a RAM location with a 2.5μsec access time. It should be considered for high-speed industrial monitoring and automatic test equipment. Optional MIL-H-38534 screening, hermetic packaging, and fully guaranteed performance from −55°C to +125°C make MN5150H/B CH an excellent choice for fast military data digitizing applications.

Part Number	Temperature Range for Guaranteed No Missing Codes	
MN5150	8 Bits	0°C to +70°C
MN5150H	8 Bits	−55°C to +125°C
MN5150H/B	8 Bits	−55°C to +125°C
MN5150H/B CH	8 Bits	−55°C to +125°C

March 1988

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MN5150 HIGH-SPEED 8-Bit A/D with 3-STATE BUFFER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5150	0°C to +70°C
MN5150H, MN5150H/B	−55°C to +125°C
Storage Temperature	−65°C to +150°C
+15V Supply (+Vcc, Pin 16)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 13)	+0.5 to −18 Volts
+5V Supply (+Vdd, Pin 6)	−0.5 to +7 Volts
Analog Input (Pins 11, 12)	±20 Volts
Digital Inputs (Pins 15, 23, 24)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN5150H/B CH

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, $\pm V_{cc}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Negative		0 to −5, 0 to −10		Volts
Unipolar Positive		0 to +5, 0 to +10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Input Impedance (Note 2): 0 to −5V, 0 to +5V, ±2.5V		2.5		kΩ
0 to −10V, 0 to +10V, ±5V		5		kΩ
±10V		10		kΩ
DIGITAL INPUTS (Start, Clock, $\overline{OE}$)				
Logic Levels: Start, Clock: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
$\overline{OE}$: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
Logic Currents: Start: Logic "1" (V_{IH} = +2.4V)			+80	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
Clock: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
$\overline{OE}$: Logic "1" (V_{IH} = +5.0V)			±10	μA
Logic "0" (V_{IL} = 0.0V)			±10	μA
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature		±¼	±½	LSB
Temperature Range for Guaranteed No Missing Codes:				
MN5150	0		+70	°C
MN5150H, MN5150H/B	−55		+125	°C
Full Scale Absolute Accuracy Error (Notes 4, 6):				
Initial (+25°C)		±½	±1	LSB
Over Temperature (Note 5)		±1	±2	LSB
Unipolar Offset Error (Notes 4, 7): Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 5)		±½	±1	LSB
Bipolar Zero Error (Notes 4, 8): Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 5)		±½	±1	LSB
DIGITAL OUTPUTS (Parallel, Serial, Status)				
Output Coding (Note 9): Unipolar Ranges		SB		
Bipolar Ranges		OB		
Logic Levels:				
Parallel Outputs: Logic "1" ($I_{source} \leq 1.6$mA)	+2.4			Volts
Logic "0" ($I_{sink} \leq 1.6$mA)			+0.4	Volts
Status, Serial Outputs: Logic "1" ($I_{source} \leq 400\mu$A	+2.4			Volts
Logic "0" ($I_{sink} \leq 8$mA)			+0.4	Volts
Leakage (Parallel Outputs) in High-Z State (Note 2)		±20		μA
REFERENCE OUTPUT				
Internal Reference (Note 2): Voltage		+6.3		Volts
Accuracy		±10		%
Tempco		±10		ppm/°C
External Current			200	μA

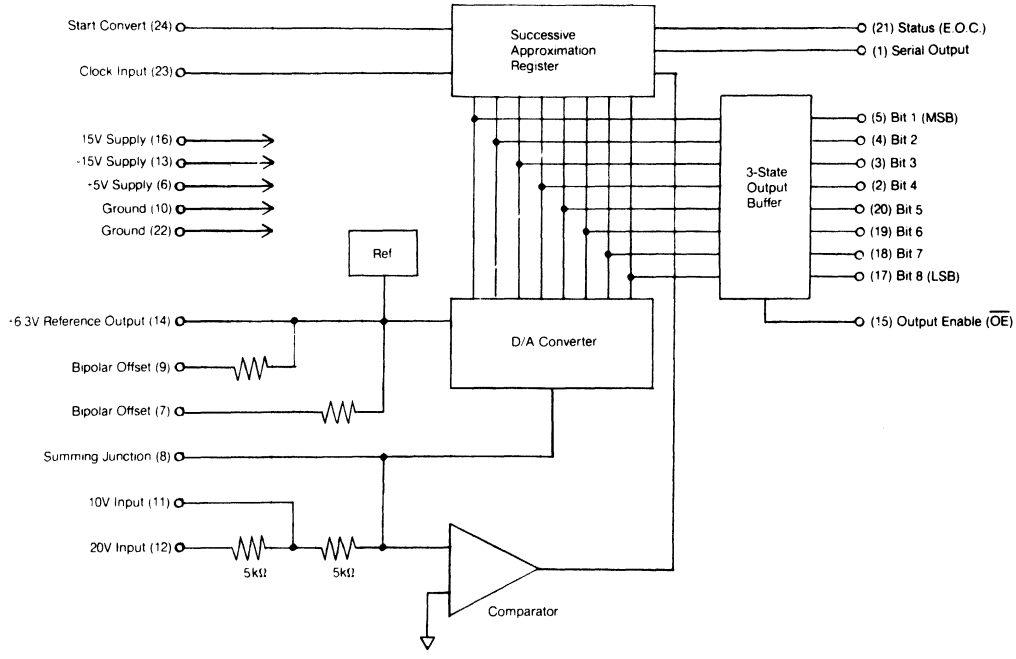
DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (Note 10)			2.5	μsec
External Clock Frequency			3.2	MHz
Clock Pulse Width (Note 2): High	25			nsec
Low	50			nsec
Setup Time Start Low to Clock (Note 2)	20			nsec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Notes 2,3,11): +15V Supply		±0.03		%FSR/%Supply
−15V Supply		±0.01	-	%FSR/%Supply
Current Drain: +15V Supply		+12	+16	mA
−15V Supply		−10	−18	mA
+5V Supply		+70	+101	mA
Power Consumption		680	1015	mW

SPECIFICATION NOTES:

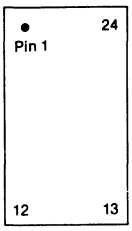
1. Listed specifications apply for all part numbers unless specifically indicated.
2. These parameters are listed for reference and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for ±10V operation has a 20V FSR. A unit connected for 0 to +10V, 0 to −10V or ±5V operation has a 10V FSR. A unit connected for 0 to +5V, 0 to −5V or ±2.5V operation has a 5V FSR.
4. 1LSB for 8 bits in 20V FSR is 78mV.
   1LSB for 8 bits in 10V FSR is 39mV.
   1LSB for 8 bits in 5V FSR is 19.5mV.
5. Listed specifications apply over the 0°C to +70°C temperature range for standard products and over the −55°C to +125°C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale accuracy specifications apply at positive full scale for unipolar positive input ranges, at negative full scale for unipolar negative input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 to 1111 1110 for unipolar positive and bipolar input ranges. Additionally it describes the accuracy of the 0000 0000 to 0000 0001 transition for unipolar negative and bipolar input ranges. The former transition ideally occurs at an input voltage 1 LSB below the nominal positive full scale voltage. The latter ideally occurs 1 LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 when operating MN5150 on a unipolar postive range. The ideal value at which this transition should occur is +1 LSB. When operating MN5150 on a unipolar negative range, unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1110 to 1111 1111. The ideal value at which this transition should occur is −1 LSB. See Digital Output Coding.
8. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating the MN5150 on a bipolar range. The ideal value at which this transition should occur is 0 Volts. See Digital Output Coding.
9. SB = straight binary. OB = offset binary.
10. Conversion time is defined as the width of Status (E.O.C.).
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0000 to 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Serial Output
2 Bit 4
3 Bit 3
4 Bit 2
5 Bit 1 (MSB)
6 +5V Supply (+Vdd)
7 Bipolar Offset
8 Summing Junction
9 Bipolar Offset
10 Ground
11 10V Input
12 20V Input
24 Start Convert
23 Clock Input
22 Ground
21 Status (E.O.C.)
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8 (LSB)
16 +15V Supply (+Vcc)
15 Output Enable ($\overline{OE}$)
14 Reference Output (+6.3V)
13 −15V Supply (−Vcc)

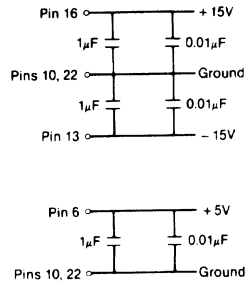
APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 24) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 21) is set to logic "1" (See Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the Status output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off. At this point, output data may be read by bringing Output Enable ($\overline{OE}$, pin 15) low. Output data will be valid 120nsec. maximum after Output Enable is low. Output data bits are returned to the high-impedance state by bringing Output Enable high.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5150. The unit's two ground pins (pins 10 and 22) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 10 and 22 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converter. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

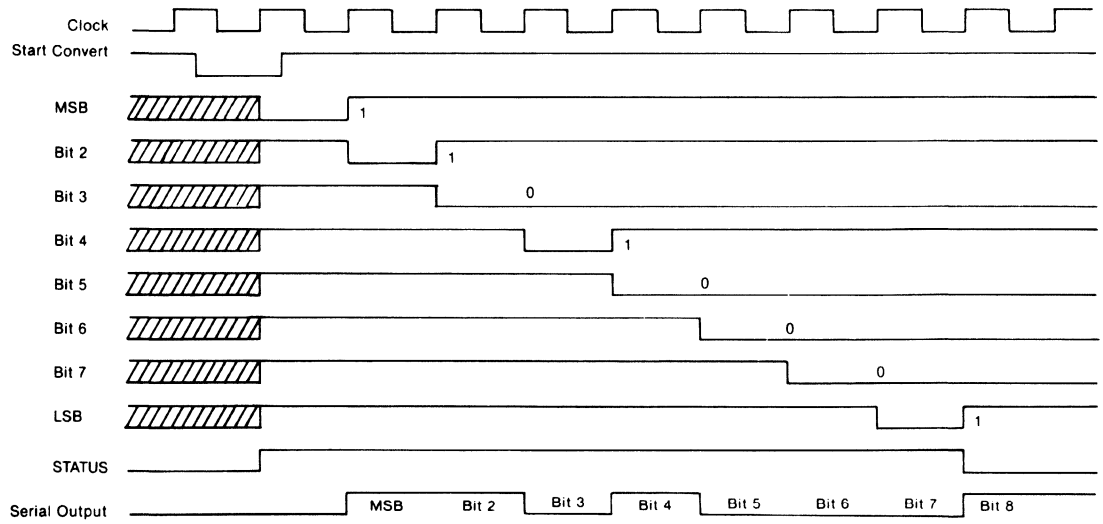


POWER SUPPLY DECOUPLING

CONTINUOUS CONVERTING—MN5150 A/D converter can be made to continuously convert by tying the Status output (pin 21) to the Start Convert input (pin 24). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output.

STATUS OUTPUT—Status or End of Conversion (E.O.C., pin 21) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 100nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple gate delays can be employed or the Status can be connected to the input of a D flip flop whose clock input is the same as the converter clock. In this situation, the Q output will change one clock period after Status changes.

TIMING DIAGRAM

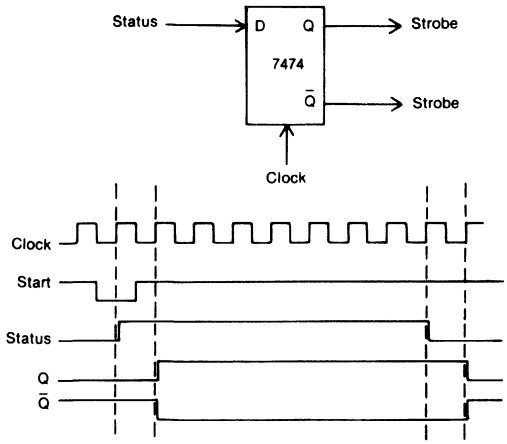


TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0001 which corresponds to 8.164V on the 0 to +10V input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 20nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the Start has returned high.
4. The delay between the resetting clock edge and Status actually rising to a "1" is 50nsec maximum.
5. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 100nsec (maximum) after the Status (E.O.C.) output has returned low. Parallel output data will remain valid and the Status output low until another conversion is initiated.
8. Parallel output data can be enabled by bringing Output Enable ($\overline{OE}$, pin 15) low. Parallel output bits can be returned to the high-impedance state by setting output enable high.
9. For continuous conversion, connect the Status output (pin 21) to the Start Convert Input (pin 24). See section on Continuous Converting.
10. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

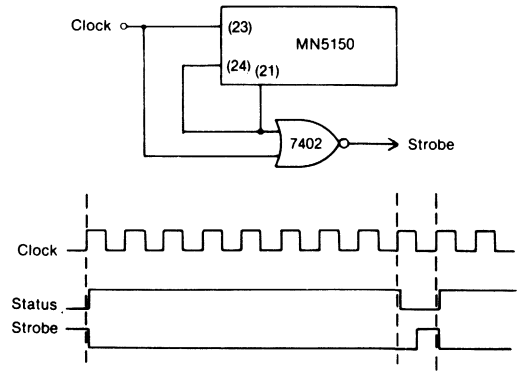
MN5150

LATCHING OUTPUT DATA

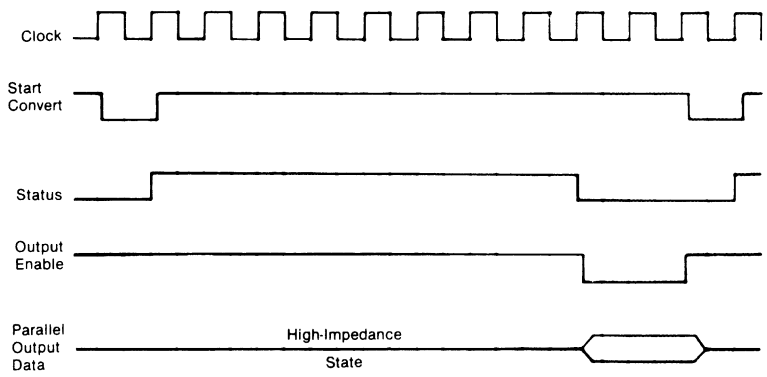


If continuously converting, the Status (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a postive strobe pulse ½ period wide, ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

LATCHING DATA CONTINUOUS CONVERSIONS



OUTPUT ENABLE—Output Enable ($\overline{OE}$, pin 15) controls the state of the parallel outputs. When a conversion is complete, valid parallel output data may be enabled by bringing Output Enable low. Data will be available 120nsec maximum after Output Enable is low. Output data is returned to the high-impedance state by bringing Output Enable high. See diagram below.



INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range						
	0 to +5V	0 to +10V	±2.5V	±5V	±10V	0 to −5V	0 to −10V
Connect Input to Pin	11	11	11	11	12	11	11
Connect Pin 7 to Pin	Ground	Ground	Ground	Ground	Ground	8,9,12	9
Connect Pin 8 to Pin	12	Open	9,12	9	9	7,9,12	7,9
Connect Pin 9 to Pin	Ground	Ground	8,12	8	8	7,8,12	7,8
Input Impedance (kΩ)	2.5	5	2.5	5	10	2.5	5

DIGITAL OUTPUT CODING

Analog Input Voltage Range							Digital Output	
0 to +5V	0 to +10V	±2.5V	±5V	±10V	0 to −5V	0 to −10V	MSB	LSB
+5.000	+10.000	+2.500	+5.000	+10.000	0.000	0.000	1111	1111
+4.981	+9.961	+2.481	+4.961	+9.922	−0.019	−0.039	1111	111Ø*
+2.519	+5.039	+0.019	+0.039	+0.078	−2.481	−4.961	1000	000Ø*
+2.500	+5.000	0.000	0.000	0.000	−2.500	−5.000	ØØØØ	ØØØØ*
+2.481	+4.961	−0.019	−0.039	−0.078	−2.519	−5.039	0111	111Ø*
+0.019	+0.039	−2.481	−4.961	−9.922	−4.981	−9.961	0000	000Ø*
0.000	0.000	−2.500	−5.000	−10.000	−5.000	−10.000	0000	0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +5V, 0 to −5V or ±2.5V ranges, 1LSB for 8 bits = 19.5mV.
4. For 0 to +10V, 0 to −10V or +5V input ranges, 1LSB for 8 bits = 39mV.
5. For ±10V input range, 1LSB for 8 bits = 78mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5150 operating on its ±10V input range, the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.961 volts. Subsequently, any input voltage more negative than −9.961 volts will give a digital output of all "0's". The transition from digital output 1000 0000 to 0111 1111 will ideally occur at an input of 0.000 volts, and the 1111 1111 to 1111 1110 transition should occur at +9.961 volts. An input more positive than +9.961 volts will all give all "1's".

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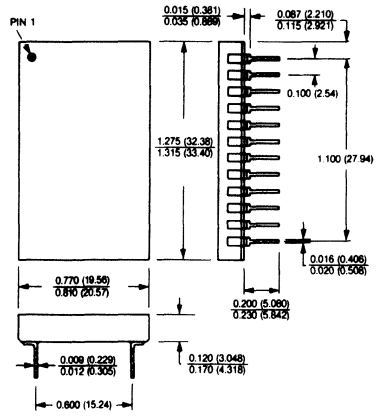
MN5160

HIGH-SPEED
8-Bit A/D CONVERTER
with LATCHED, 3-STATE OUTPUTS

FEATURES

- **Fast 2.0μsec Conversion Time**
- **Latched, 3-State Output Buffer**
- **±1/2LSB Linearity and No Missing Codes Over Temperature**
- **Adjustment-Free No Gain or Offset Adjustments Necessary**
- **Fully Specified 0°C to +70°C (MN5160) or −55°C to +125°C (MN5160H and MN5160H/B)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5160 is a high-speed, 8-bit, successive approximation A/D converter with an onboard, latched, 3-state output buffer for easy data bus interfacing. Fast (2μsec maximum) conversion time, ± ½ LSB linearity, ±1 LSB absolute accuracy and "no missing codes" guaranteed over the entire operating temperature range make the MN5160 an excellent choice for industrial or military, high-speed, single or multi-channel data acquisition systems in monitoring or automatic test equipment. In very high-speed applications, the latched, 3-state output buffer provides a significant advantage over unlatched A/D's in that it allows valid parallel output data from the previous conversion to be held and read during an ongoing conversion.

MN5160 is packaged in a 24-pin, double-wide, hermetically sealed DIP and features 5 user-selectable input ranges. The stability of our Micro Networks laser-trimmed thin-film resistor networks allows MN5160 to operate without external gain and offset adjustments and maintain full accuracy and linearity over temperature.

Units are available and fully specified for 0°C to +70°C (MN5160) or −55°C to +125°C (MN5160H and MN5160H/B) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN5160H/B is available with Environmental Stress Screening, while MN5160H/B CH is screened in accordance with MIL-H-38534. Contact factory for availability of "CH" device types.

Part Number	Temperature Range for Guaranteed No Missing Codes	
MN5160	8 Bits	0°C to +70°C
MN5160H	8 Bits	−55°C to +125°C
MN5160H/B	8 Bits	−55°C to +125°C
MN5160H/B CH	8 Bits	−55°C to +125°C

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January 1992
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MN5160 HIGH-SPEED 8-Bit A/D CONVERTER with LATCHED 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5160	0°C to +70°C
MN5160H, MN5160H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 16)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 13)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 6)	−0.5 to +7 Volts
Analog Inputs (Pins 11, 12)	±20 Volts
Digital Inputs (Pins 7, 15, 23, 24)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN5160 H/B CH

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.
Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +5, 0 to +10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Input Impedance (Note 2): 0 to +5V, ±2.5V		2.5		kΩ
0 to +10V, ±5V		5		kΩ
±10V		10		kΩ
DIGITAL INPUTS (Start, Clock, Latch, $\overline{OE}$)				
Logic Levels All Inputs: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Start: Logic "1" (V_{IH} = +2.4V)			+80	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
Clock, Latch, $\overline{OE}$: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Linearity Error (Note 4): Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 5)		±¼	±½	LSB
Temperature Range for Guaranteed No Missing Codes (Note 5):				
MN5160	0		+70	°C
MN5160H, MN5160H/B	−55		+125	°C
Full Scale Absolute Accuracy Error (Notes 4, 6):				
Initial (+25°C)		±½	±1	LSB
Over Temperature (Note 5)		±1	±2	LSB
Unipolar Offset Error (Notes 4, 7):				
Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 5)		±½	±1	LSB
Bipolar Zero Error (Notes 4, 8):				
Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 5)		±½	±1	LSB
DIGITAL OUTPUTS (Parallel, Serial, Status)				
Output Coding (Note 9): Unipolar Ranges		SB		
Bipolar Ranges		OB		
Logic Levels All Outputs: Logic "1" (Isource ≤ 400μA)	+2.4			Volts
Logic "0" (Isink ≤ 8 mA)			+0.4	Volts
Leakage (Parallel Outputs) in High - Z State (Note 2)		±20		μA
REFERENCE OUTPUT				
Internal Reference (Note 2): Voltage		+6.3		Volts
Accuracy		±10		%
Tempco		±10		ppm/°C
External Current			200	μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 10)			2.0	μsec
External Clock Frequency			4	MHz
Clock Pulse Width (Note 2): High	20			nsec
Low	50			nsec
Setup Time Start Low to Clock (Note 2)	20			nsec
Latch Enable Pulse Width (Note 2)	50			nsec
Delay From Output Enable to Data Valid (Note 2)			50	nsec

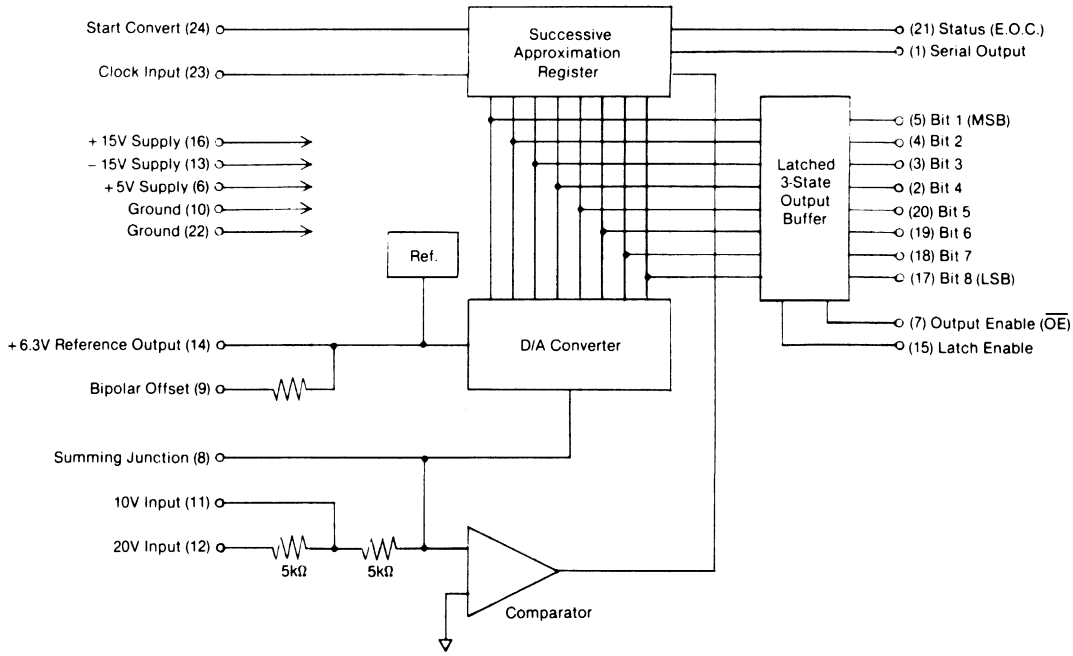
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Notes 3, 11): +15V Supply		± 0.03	± 0.06	%FSR/%Supply
−15V Supply		± 0.01	± 0.02	%FSR/%Supply
Current Drain: +15V Supply		+16	+22	mA
−15V Supply		−10	−18	mA
+5V Supply		+100	+140	mA
Power Consumption		890	1300	mW

SPECIFICATION NOTES:

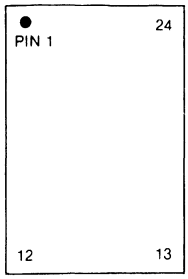
1. Listed specifications apply for all part numbers unless specifically indicated.
2. These parameters are listed for reference and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for ± 10V operation has a 20V FSR. A unit connected for 0 to + 10V, ± 5V operation has a 10V FSR. A unit connected for 0 to + 5V, ± 2.5V operation has a 5V FSR.
4. 1 LSB for 8 bits in 20V FSR is 78mV.
   1 LSB for 8 bits in 10V FSR is 39mV.
   1 LSB for 8 bits in 5V FSR is 19.5mV.
5. Listed specifications apply over the 0 °C to + 70 °C temperature range for standard products, and over the − 55 °C to + 125 °C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input range. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 to 1111 1110 for unipolar and bipolar input ranges. Additionally it describes the accuracy of the 0000 0000 to 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB below the nominal positive full scale voltage. The latter ideally occurs + ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 when operating MN5160 on a unipolar range. The ideal value at which this transition should occur is + ½LSB. See Digital Output Coding.
8. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating the MN5160 on a bipolar range. The ideal value at which this transition should occur is − ½LSB. See Digital Output Coding.
9. SB = straight binary. OB = offset binary.
10. Conversion time is defined as the width of Status (E.O.C.).
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0000 to 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Serial Output
2 Bit 4
3 Bit 3
4 Bit 2
5 Bit 1 (MSB)
6 +5V Supply (+Vdd)
7 Output Enable ($\overline{OE}$)
8 Summing Junction
9 Bipolar Offset
10 Ground
11 10V Input
12 20V Input
24 Start Convert
23 Clock Input
22 Ground
21 Status (E.O.C.)
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8 (LSB)
16 +15V Supply (+Vcc)
15 Latch Enable
14 Reference Output (+6.3V)
13 −15V Supply (−Vcc)

APPLICATIONS INFORMATION

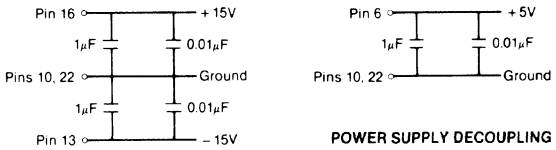
DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 24) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 21) is set to logic "1" (See Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the Status output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

As you recall, digital output bits are reset to 0111 1111 at the beginning of the successive approximation conversion process and that valid parallel output data can only be read between conversions. MN5160's Latch Enable (pin 15) and Output Enable (pin 7) allow data from a prior conversion to be latched and read while the next conversion is in progress. If desired, valid output data may be latched by applying a "0" to "1" edge to Latch Enable (pin 15). If this is done, output data from the just completed conversion will be latched in MN5160's 3-state output latch. Once latched, output data may be read by bringing Output Enable ($\overline{OE}$, pin 7) low. Output data will be valid 50nsec maximum after Output Enable is low. Output data bits are returned to the high-impedance state by bringing Output Enable high.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5160. The unit's two ground pins (pins 10 and 22) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 10 and 22 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

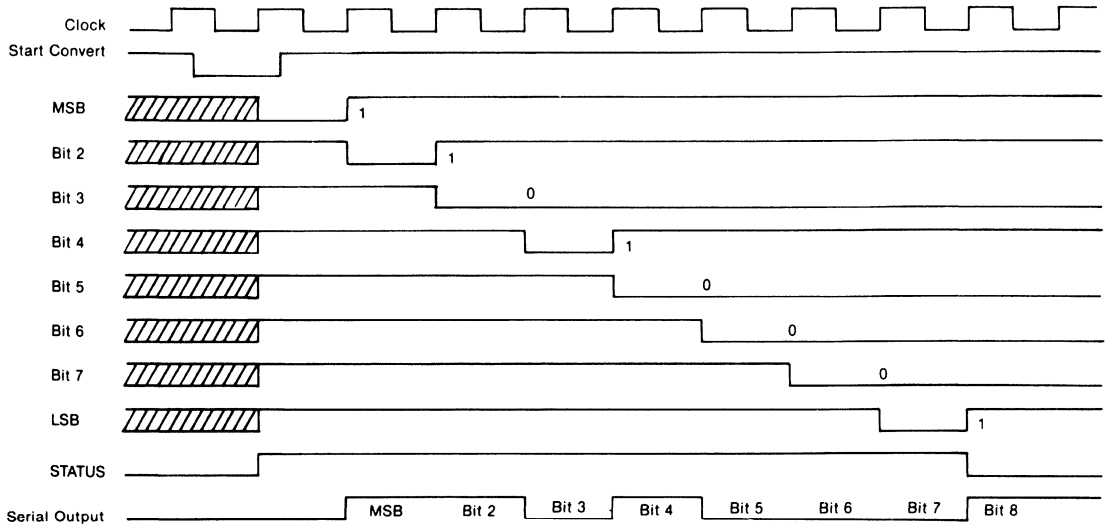


POWER SUPPLY DECOUPLING

CONTINUOUS CONVERTING—The MN5160 A/D converters can be made to continuously convert by tying the Status output (pin 21) to the Start Convert input (pin 24). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output.

STATUS OUTPUT—The Status or End Of Conversion (E.O.C., pin 21) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 100nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple gate delays can be employed or the Status can be made the input of a D flip flop whose clock input is the same as the converter clock. In this situation, the Q output will change one clock period after Status changes.

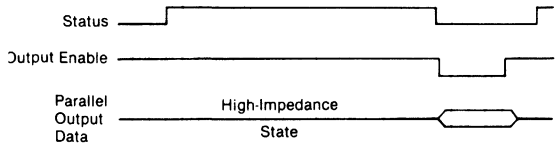
TIMING DIAGRAM



TIMING DIAGRAM NOTES:

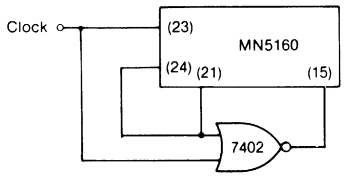
1. Operation shown is for the digital word 1101 0001 which corresponds to 8.164V on the 0 to +10V input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 20nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after Start has returned high.
4. The delay between the resetting clock edge and Status actually rising to a "1" is 50nsec maximum.
5. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 100nsec (maximum) after the Status (E.O.C.) output has returned low. Parallel output data will remain valid and the Status output low until another conversion is initiated.
8. Parallel output data can be latched at the end of a conversion by a "0" to "1" edge applied to Latch Enable (pin 15).
9. Parallel output data can be enabled by bringing Output Enable ($\overline{OE}$, pin 7) low. Parallel output bits can be returned to the high impedance state by setting Output Enable high.
10. For continuous conversion, connect the Status output (pin 21) to the Start Convert input (pin 24). See section on Continuous Conversion.
11. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

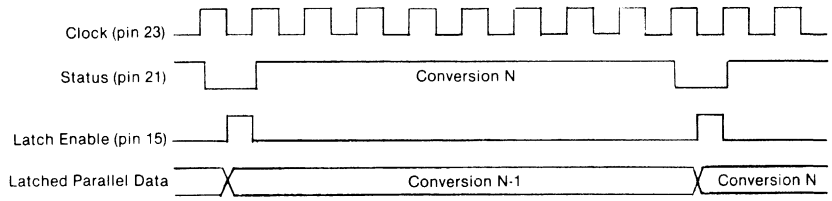
OUTPUT ENABLE—Output Enable ($\overline{OE}$, pin 7) controls the state of the parallel outputs. When a conversion is complete, valid parallel output data may be enabled by bringing Output Enable low. Data will be available 50nsec maximum after Output Enable is low. Output data is returned to the high-impedance state by bringing Output Enable high. See diagram below.



LATCH ENABLE—Valid parallel output data can be latched in MN5160's output buffer by the rising edge ("0" to "1" transition) of Latch Enable input (pin 15). When continuously converting, data from the previous conversion can be latched and read during a subsequent conversion. The Status (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse ½ period wide, ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion. Once latched, output data can be enabled and read by bringing Output Enable ($\overline{OE}$, pin 7) low.

LATCHING DATA CONTINUOUS CONVERSIONS





INPUT RANGE SELECTION

Connect	Analog Input Voltage Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Input to Pin	11	11	11	11	12
Pin 8 to Pin	12	Open	12,9	9	9
Pin 9 to Pin	Ground	Ground	8	8	8
Input Impedance	2.5kΩ	5kΩ	2.5kΩ	5kΩ	10kΩ

DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Output	
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB	LSB
+5.000	+10.000	+2.500	+5.000	+10.000	1111	1111
+4.981	+9.961	+2.481	+4.961	+9.922	1111	111Ø*
+2.519	+5.039	+0.019	+0.039	+0.078	1000	000Ø*
+2.500	+5.000	0.000	0.000	0.000	ØØØØ	ØØØØ*
+2.481	+4.961	−0.019	−0.039	−0.078	0111	111Ø*
+0.019	+0.039	−2.481	−4.961	−9.922	0000	000Ø*
0.000	0.000	−2.500	−5.000	−10.000	0000	0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +5V or ±2.5V input ranges, 1LSB for 8 bits = 19.5mV.
4. For 0 to +10V or ±5V input ranges, 1LSB for 8 bits = 39mV.
5. For ±10V input range, 1LSB for 8 bits = 78mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5160 operating on its ±10V input range, the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.961 volts. Subsequently, any input voltage more negative than −9.961 volts will give a digital output of all "0's". The transition from digital output 1000 0000 to 0111 1111 will ideally occur at an input of −0.039 volts, and the 1111 1111 to 1111 1110 transition should occur at +9.883 volts. An input more positive than +9.883 volts will give all "1's."

MICRO NETWORKS

MN5200 Series

50μsec, 12-Bit
MILITARY
A/D CONVERTERS

*FEATURES

- **50μsec Maximum Conversion Time**
- **±1/2LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Small 24-Pin DIP**
- **±1LSB Zero Error**
- **±2LSB Absolute Accuracy**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

DESCRIPTION

MN5200 Series devices are 12-bit, successive approximation A/D converters in industry-standard, 24-pin, dual-in-line packages. Functional laser trimming of our own nichrome thin-film resistor networks results in adjustment-free devices that are extremely accurate and highly stable.
Zero error, for example, is guaranteed to be better than ±0.025% FSR (±1 LSB) at +25°C and better than ±0.05% FSR (±2 LSB) over the entire operating temperature range. All units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature.

These A/D converters are available in a number of input voltage ranges. For each range, the user has the option of specifying a model complete with internal reference or, for improved overall accuracy, a model which uses an external reference. In all cases, ±½LSB linearity and 12-bit "no missing codes" are guaranteed over the entire operating temperature range.

All models of the MN5200 Series may be procured for operation over the full −55°C to +125°C military temperature range ("H" models) or the 0°C to +70°C commercial temperature range. For military/aerospace or harsh-environment commercial/industrial applications "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

The MN5200 Series (50μsec conversion time) and MN5210 Series (13μsec conversion time) are the industry's most widely accepted 12-bit A/D's for military/aerospace applications. These devices are presently designed into more than 50 military/aerospace programs. Their small size, low power consumption and adjustment-free operation make them excellent selections for compact, highly reliable systems. New applications will be found wherever size, speed, power and temperature considerations are paramount.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

January 1992
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MN5200 SERIES 50μsec 12-Bit MILITARY A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	-55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
Positive Supply (Pin 15)	+18 Volts
Negative Supply (Pin 13)	-18 Volts
Logic Supply (Pin 2)	-0.5 to +7 Volts
Analog Input (Pin 14)	±25 Volts
Digital Inputs (Pins 1, 24)	-0.5 to +5.5 Volts
Digital Outputs	Logic Supply
Ref. Input (MN5203, 04, 05)	0 to -15 Volts

ORDERING INFORMATION

PART NUMBER — MN520X H/B CH

- Select Model Number (MN5200, MN5201 etc.)
- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified -55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and ±5V, for Ext. Ref. Models V_{Ref} = -10.000V, unless otherwise specified).

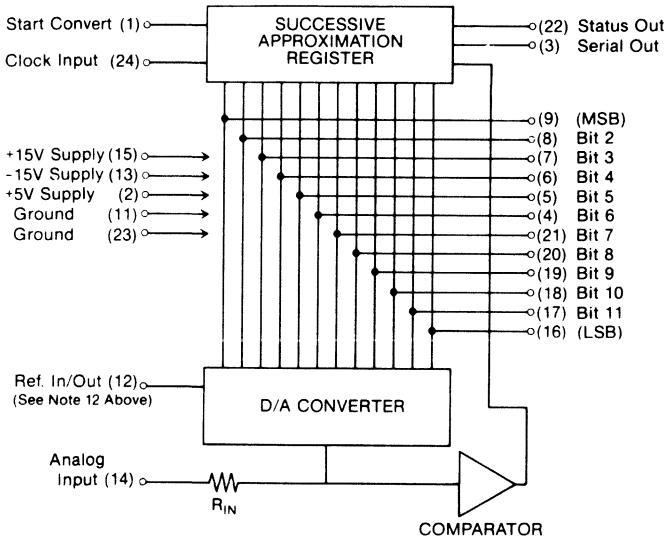
ANALOG INPUTS	MODEL NUMBER (Internal Ref.) MN5200 MN5201 MN5202 MN5206		MODEL NUMBER (External Ref.) MN5203 MN5204 MN5205		
Input Range (Input Impedance) (Note 1): 0 to -10V (5KΩ); -5V to +5V (5KΩ); -10V to +10V (10KΩ); 0 to +10V (5KΩ)					
TRANSFER CHARACTERISTICS	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNITS**
Linearity Error (Notes 2, 3): +25°C	±¼	±½	±¼	±½	LSB
0°C to +70°C	±¼	±½	±¼	±½	LSB
-55°C to +125°C ("H" Models)		±½		±½	LSB
Differential Linearity Error	±½		±½		LSB
No Missing Codes	Guaranteed Over Temperature				
Full Scale Absolute Accuracy Error (Notes 4, 5) +25°C	± 0.25	± 0.05	± 0.025	± 0.05	%FSR
0°C to +70°C	± 0.2	± 0.4	± 0.05	± 0.1	%FSR
-55°C to +125°C ("H" Models)		± 0.4		± 0.1	%FSR
Zero Error (Notes 4, 5): +25°C	± 0.01	± 0.025	± 0.01	± 0.025	%FSR
0°C to +70°C	± 0.025	± 0.05	± 0.025	± 0.05	%FSR
-55°C to +125°C ("H" Models)		± 0.05		± 0.05	%FSR
Gain Error (Note 5)	± 0.025		± 0.025		%
Gain Drift	± 10		± 3		ppm/°C
Conversion Time (Note 6)		50		50	μSec
POWER SUPPLIES					
Power Supply Range: ±15V Supplies		± 3		± 3	%
+5V Supply		± 5		± 5	%
Power Supply Rejection (Note 7): +15V Supply	± 0.005	± 0.02	± 0.005	± 0.02	%FSR/% Vs
-15V Supply	± 0.01	± 0.05	± 0.005	± 0.02	%FSR/% Vs
Current Drain: +15V Supply	23	28	23	28	mA
-15V Supply	-25	-35	-25	-35	mA
+5V Supply	25	42	25	42	mA
-10V Reference (MN5203, 04, 05)			-1.5	-2	mA

DIGITAL INPUTS (ALL UNITS)	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.7	Volts
Clock Input (Note 8): Pulse Width High	125			nSec
Pulse Width Low	175			nSec
Loading High (V_{in} = 2.4V)		2	20	μA
Loading Low (V_{in} = 0.3V)		-0.25	-0.4	mA
Frequency (Note 6)			240	KHz
Start Convert Input: Loading High (V_{in} = 2.4V)		4	40	μA
Loading Low (V_{in} = 0.3V)		-0.25	-0.4	mA
Setup Time Start Low to Clock (Note 9)	25			nSec
DIGITAL OUTPUTS (ALL UNITS)				
Logic Coding (Note 10): Unipolar Ranges	Complementary Straight Binary			
Bipolar Ranges	Complementary Offset Binary			
Logic Levels: Logic "1"	2.4	3.6		Volts
Logic "0"		0.15	0.3	Volts
Output Drive Capability, All Outputs (Note 11): Logic "1"	8			TTL Loads
Logic "0"	2			TTL Loads
REFERENCE INPUT/OUTPUT (Note 12)				
Internal Reference: Voltage		-6.3		Volts
Accuracy		±2		%
Tempco of Drift		±5		ppm/°C
Max. External Current (Without Buffering)			100	μA
External Reference: Voltage		-10.000		Volts
Loading			- 2	mA

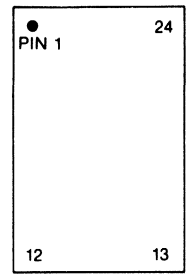
SPECIFICATION NOTES:

1. Consult factory for other available input voltage ranges.
2. Micro Networks tests and guarantees maximum linearity error at room temperature and at both the high and low extremes of the specified operating temperature range.
3. 1 LSB for a 12 bit converter corresponds to 0.024%FSR. See Note 4.
4. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ±10V input range, FSR is 20 volts, and 1 LSB is equal to 4.88 mV. For the 0 to +10V, 0 to -10V, and ±5V ranges, FSR is 10 volts, and 1 LSB is equal to 2.44 mV.
5. See Absolute Accuracy section below for an explanation of how Micro Networks tests and specifies Full Scale Absolute Accuracy, Gain, and Zero Errors.
6. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. See Timing Diagram. For the MN5200 Series, a 50 μSec conversion time corresponds to an external clock frequency of 240 kHz. Micro Networks guarantees Linearity and Absolute Accuracy at and below this clock frequency.
7. Micro Networks tests and guarantees Power Supply Rejection over the ±15V ±3% range.
8. The clock may be asymmetrical with minimum positive or negative pulse width. See Note 6.
9. In order to reset the converter, START CONVERT must be brought low at least 25 nSec prior to a low to high clock transition. See Timing Diagram.
10. CSB = Complementary Straight Binary
    COB = Complementary Offset Binary
    Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
11. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
12. MN5200, MN5201, MN5202, and MN5206 have an internal -6.3V reference. MN5203, MN5204, and MN5205 require an external -10.000V reference.

BLOCK DIAGRAM



PIN DESIGNATIONS

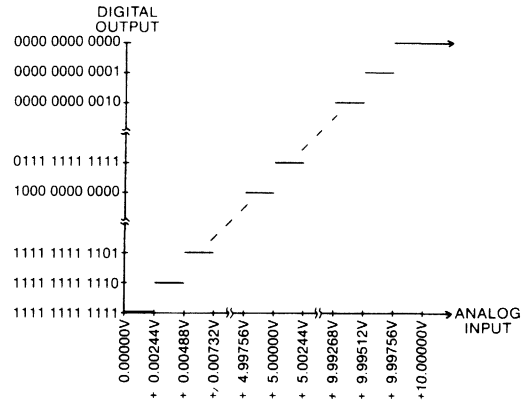


Pin 1	Start Convert	Pin 24	Clock Input
Pin 2	+5V Supply	Pin 23	Ground
Pin 3	Serial Output	Pin 22	Status (E.O.C.)
Pin 4	Bit 6	Pin 21	Bit 7
Pin 5	Bit 5	Pin 20	Bit 8
Pin 6	Bit 4	Pin 19	Bit 9
Pin 7	Bit 3	Pin 18	Bit 10
Pin 8	Bit 2	Pin 17	Bit 11
Pin 9	Bit 1 (MSB)	Pin 16	Bit 12 (LSB)
Pin 10	N/C	Pin 15	+15V Supply
Pin 11	Ground	Pin 14	Analog Input
Pin 12	Ref. Out (-6.3V) Ref. In (-10.0V)	Pin 13	-15V Supply

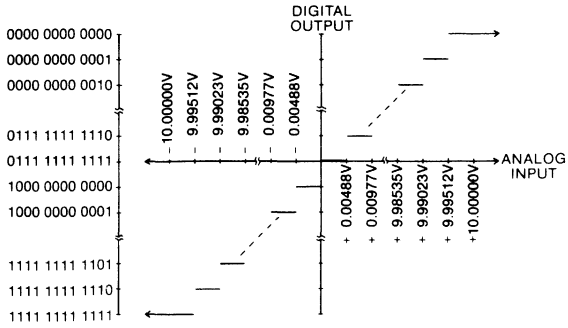
ABSOLUTE ACCURACY ERROR

A given digital output code is valid for a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated in the next column and on the following page where portions of the theoretical analog input/digital output transfer functions of the MN5206 (0 to +10V input range) and the MN5202 (±10V input range) are sketched.

Notice that, for the MN5206, any analog input between +0.00244 volts (1 LSB = 2.44 mV) and +0.00488 volts will give a digital output of 1111 1111 1110. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 1111 1111 1110 digital code corresponds to analog inputs of +3.66 mV ±1.22 mV which can be written as +3.66 mV ±1/2 LSB. The ±1/2 LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error and its magnitude can be reduced only by going to higher resolution converters.



MN5206 TRANSFER FUNCTION



MN5202 TRANSFER FUNCTION

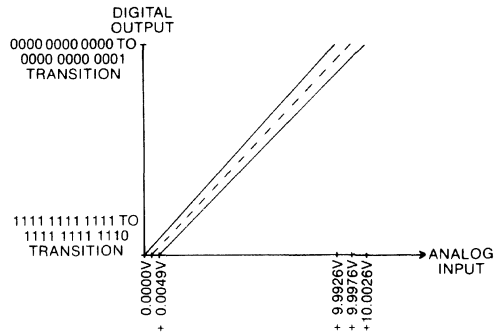
It is difficult and time consuming to measure the center of a quantization level (the +0.00366 volts in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted,* analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR (see Note 4 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors.

For the MN5200 Series A/D converters, Micro Networks tests Absolute Accuracy Error at both endpoints of unipolar input ranges and at both endpoints and the midpoint of bipolar input ranges. These tests are performed at room temperature and at both the high and low extremes of the specified operating temperature range. The specifications appear in the table as the Full Scale Absolute Accuracy and Zero Errors.

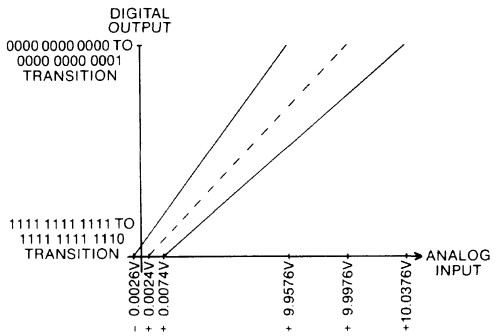
EXAMPLE MN5206: Return to the ideal analog input/digital output transfer function of the MN5206 sketched on page 3. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from 0V to +2.44 mV. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to +2.44 mV. This voltage, +2.44 mV is the zero transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1'. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9976V.

For the MN5206H (0 to +10V input range, -55°C to +125°C operation), Micro Networks tests linearity and the accuracy of the two transition voltages just discussed at -55°C, +25°C, and +125°C. We guarantee that the transfer function will be ±1/2 LSB linear at all temperatures and that the zero transition will be within ±0.025%FSR (±2.5 mV) of its ideal value (+2.44 mV) at +25°C and within ±0.05%FSR (±5 mV) of its ideal value at -55°C and at +125°C. This is our Zero Error specification. We guarantee that the positive full scale LSB transition voltage will be within ±0.05%FSR (±5 mV) of its ideal value (+9.9976V) at +25°C and within ±0.4%FSR (±40 mV) of its ideal value at -55°C and +125°C. This is our Full Scale Absolute Acuracy Error specification.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5206H, that the actual transfer function will be ±1/2 LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at -55°C and +125°C.



MN5206 ABSOLUTE ACCURACY +25°C



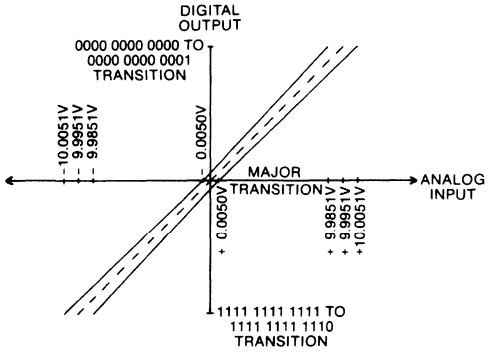
MN5206H ABSOLUTE ACCURACY -55°C AND +125°C

EXAMPLE MN5202: Return to the ideal analog input/digital output transfer function of the MN5202 sketched above. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from -10.000V to -9.9951V. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to -9.9951V. This voltage, -9.9951V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The 1000 0000 0000 to 0111 1111 1111 transition (called the "major transition" because all the bits change) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9951V.

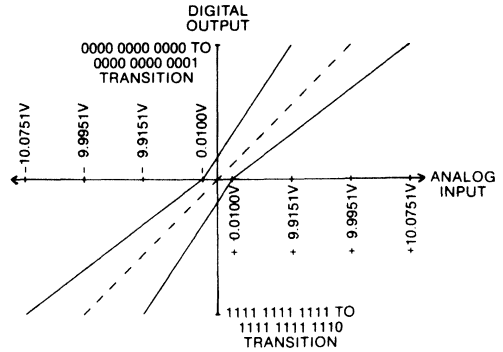
For the MN5202H (±10V input range, -55°C to +125°C operation), Micro Networks tests linearity and the accuracy of the three transition voltages just discussed at -55°C, +25°C, and +125°C. We guarantee that the transfer function will be ±1/2 LSB linear at all temperatures and that the positive and negative full scale LSB transition voltages will be within ±0.05%FSR (±10 mV) of their ideal values (+9.9951V and -9.9951V) at +25°C and within ±0.4%FSR (±80 mV) of their ideal values at -55°C and +125°C. This is our Full Scale

Absolute Accuracy Error specification. We also guarantee that the major transition voltage will be within ±0.025%FSR (±5 mV) of its ideal value (zero volts) at +25°C and within ±0.05%FSR (±10 mV) of its ideal value over the entire -55°C to +125°C operating temperature range. This is our Zero Error specification.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5202H, that the actual transfer function will be ±1/2 LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at -55°C and +125°C.



MN5202 ABSOLUTE ACCURACY +25°C

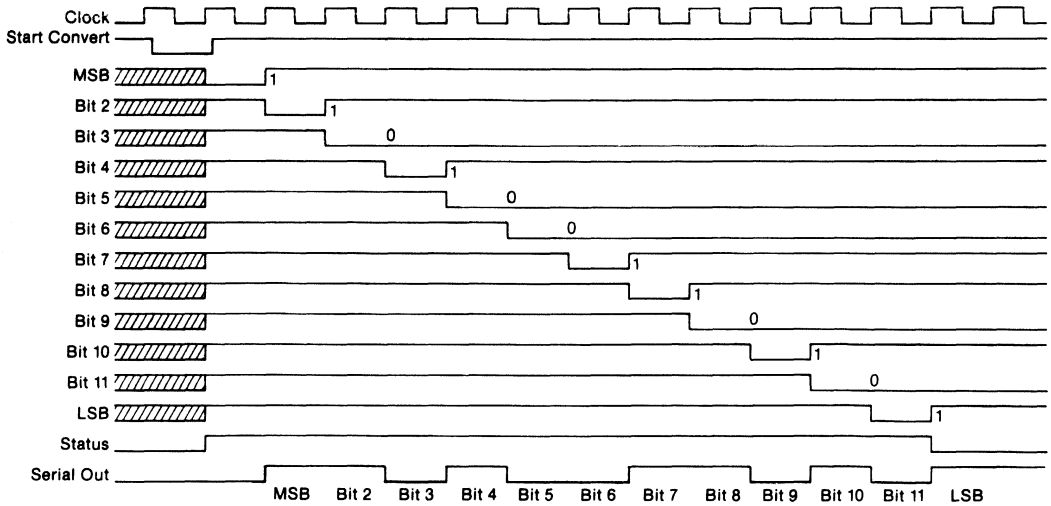


MN5202H ABSOLUTE ACCURACY -55°C AND +125°C

Because Micro Networks tests and guarantees ±1/2 LSB linearity at all temperatures, the Absolute Accuracy of any transition voltage can be interpolated from the Full Scale Absolute Accuracy and Zero Error specifications. Example: at +25°C, the 1000 0000 0000 to 0111 1111 1111 transition of the MN5206 will occur within ±0.0375%FSR (±3.75 mV) of its ideal value (+5.000V). For temperatures intermediate to +25°C and -55°C or +125°C, maximum Full Scale Absolute Accuracy and Zero Errors can also be interpolated. At +75°C, for example, Full Scale Absolute Accuracy Error will be ±0.225%FSR.

We have not specified Unipolar and Bipolar Offset Errors for the MN5200 Series. We feel that Offset is a confusing

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0011 0101 which corresponds to 1.7432V on the 0 to +10V input range (MN5206). See Output Coding.
2. Conversion time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nSec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 120 nSec maximum.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 30 nSec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated.
8. For continuous conversion, connect the STATUS output (Pin 22) to the START CONVERT input (Pin 1). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

specification and choose not to use it. Offset Errors for the MN5200 Series will always be equivalent to either our Full Scale Absolute Accuracy or Zero Errors and we prefer these specifications because of their simplicity. Be sure you clearly understand each manufacturer's converter specification definitions before you compare converters solely on a data sheet basis.

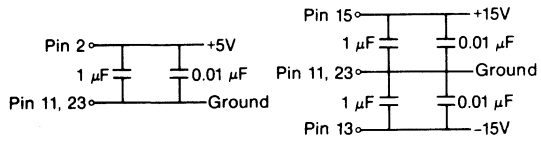
GAIN ERROR—Gain Error is the difference between the ideal and the measured values of a converter's Full Scale Range (minus 2 LSB); it is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 0000 0000 0000 to 0000 0000 0001 transition minus that measured for the 1111 1111 1111 to 1111 1111 1110 transition.

See the Converter Tutorial Section of the Micro Networks' Applications Manual and Product Guide for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5200 Series converters. The units' two GROUND pins (Pins 11 and 23) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between Pins 11 and 23 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.



POWER SUPPLY DECOUPLING

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's START CONVERT (Pin 1) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the STATUS output (Pin 22) is set to logic "1" (see Timing Diagram). The START CONVERT must now be brought high again for the conversion to continue. If the START is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the START has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 12) also drops the STATUS OUTPUT to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

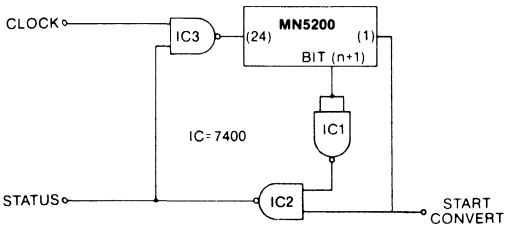
CONTINUOUS CONVERTING — The MN5200 Series A/D converters can be made to continuously convert by tying the STATUS output (Pin 22) to the START CONVERT input (Pin 1). In this configuration, STATUS (START CONVERT) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing STATUS (START CONVERT) high again. The MSB will be set on the next rising clock edge. The result is that the STATUS will go low for approximately one clock period following each conversion. Please read the section describing the STATUS output. See below for continuous conversions while short cycling.

DIGITAL OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT
MN5200, 5203	MN5201, 5204	MN5202, 5205	MN5206	MSB LSB
0.0000V	+5.0000V	+10.0000V	+10.0000V	0000 0000 0000
- 0.0024V	+4.9976V	+ 9.9951V	+ 9.9976V	0000 0000 0000*
- 4.9976V	+0.0024V	+ 0.0049V	+ 5.0024V	0111 1111 1110*
- 5.0000V	0.0000V	0.0000V	+ 5.0000V	0000 0000 0000*
- 5.0024V	-0.0024V	- 0.0049V	+ 4.9976V	1000 0000 0000*
- 9.9976V	-4.9976V	- 9.9951V	+ 0.0024V	1111 1111 1110*
-10.0000V	- 5.0000V	-10.0000V	0.0000V	1111 1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as 0 will change from "1" to "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages.
EXAMPLE: For an MN5202/05 (±10V analog input range) the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.9951 volts. Subsequently, any input voltage more positive than +9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at −9.9951 volts. An input more negative than −9.9951 volts will give all "1's".

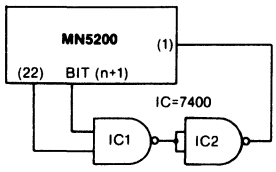
SHORT CYCLING—For applications requiring less than 12 bits resolution, the MN5200 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.



SHORT CYCLING SINGLE CONVERSIONS

Assuming a conversion is already in progress, bit (n+1) will go low as bit n is being set (see Timing Diagram). Since the START CONVERT signal is high at this time, STATUS (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, START CONVERT is brought low driving STATUS high and gating on the clock. The first rising clock edge the converter sees with START CONVERT low will reset the converter bringing bit (n+1) high again. Now STATUS will remain high as START CONVERT is brought back high allowing the conversion to continue. Therefore, in this configuration, STATUS and START CONVERT function normally, i.e., the same as STATUS and START CONVERT for a converter not being short cycled.

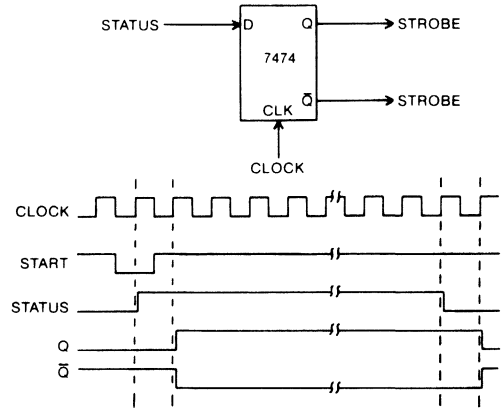
SHORT CYCLING AND CONTINUOUS CONVERTING—A previous section described how continuous converting for 12 bits could be accomplished by simply tying the STATUS output back to the START CONVERT input. To continuously convert at n bits, one simply has to tie the bit (n+1) output back to the START CONVERT input. The bit (n+1) output acts like a STATUS when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n+1) comes on as a "1" and the conversion process comes on at bit (n+2). This situation can be avoided by making the START CONVERT input the AND function of bit (n+1) and the STATUS output.



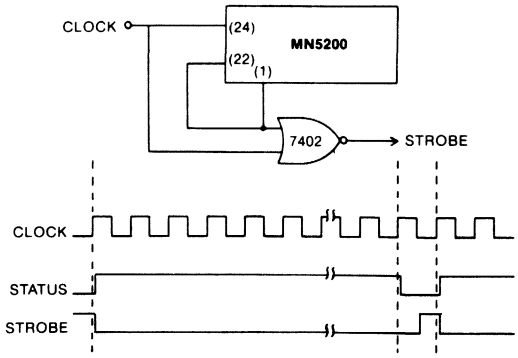
SHORT CYCLING CONTINUOUS CONVERTING

If one is already using the circuit described in the section labeled SHORT CYCLING, one can short cycle and continuously convert by making the START CONVERT input the AND function of STATUS (IC2) and STATUS (pin 7) outputs.

STATUS OUTPUT—The STATUS or END OF CONVERSION (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 30 nSec after STATUS has returned low. Therefore, an adequate delay must be provided if STATUS is to be used to strobe latches to hold output data. Simple gate delays can be employed or the STATUS can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after STATUS changes.



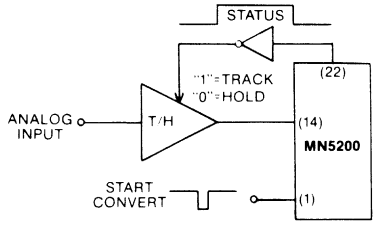
If continuously converting the STATUS (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse 1/2 period wide, 1/2 period after the STATUS output has gone low. The rising edge of this pulse can be used to latch data after each conversion.



USING A TRACK AND HOLD AMP WITH MN5200 SERIES A/D's—The error that results when trying to convert moving analog signals with a successive approximation A/D can be as great as the amount the analog signal changes during a single A/D conversion time. If this error is unacceptable, a Track and Hold (T/H) or Sample and Hold (S/H) amplifier can be placed between the analog signal source and the A/D converter. A careful error analysis will be necessary to determine if the T/H is actually reducing and not increasing overall error. T/H parameters such as aperture uncertainty, gain accuracy, pedestal error and droop rate will have to be contended with (see the tutorial section of the Micro Networks'

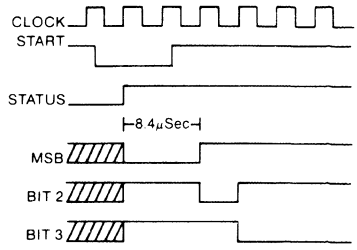
Applications Manual and Product Guide for a complete discussion of T/H parameters).

Normally, the T/H can be controlled directly by the A/D's STATUS output. Typical connections are shown below for Micro Networks' MN343 (10 μSec acquisition time to ±0.01%) and MN346 (1.6 μSec acquisiton time to ±0.01%) Track and Hold Amplifiers. The STATUS output changes form a "0" to a "1" when the converter is reset. This drives the T/H from the track to the hold mode. At the end of conversion, STATUS returns to a "0" restoring the T/H to the track mode.

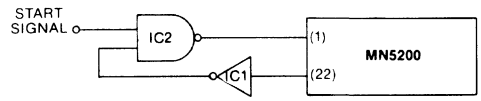


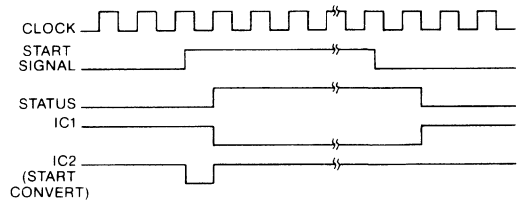
MN343		MN346
10 μSec	Acquisition Time	1.6 μSec
60 nSec	Aperature Delay	30 nSec
3 mV	Pedestal Error	2 mV
0.1 mV/mSec	Droop Rate	0.1 mV/mSec
1.5 μSec	Track to Hold Settling	150 nSec

Recall that if the START CONVERT pulse is brought high immediately after the converter has been reset, the MSB will be finalized one clock period later (see Timing Diagram). Care should be taken to ensure aperture delay time and track-to-hold settling time do not contribute errors. If necessary, the width of the START CONVERT pulse can be increased to allow more time between the T/H being commanded into the hold mode (STATUS = "1") and the MSB being set. Recall that output bits do not begin to get set until after the START CONVERT has returned high. The example below shows a 8.4 μSec delay to allow for track to hold settling. Clock frequency = 240 kHz; 1 period = 4.2 μSec.

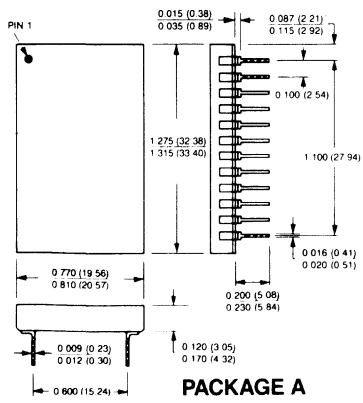


TRIGGERING WITH A POSITIVE EDGE—If it is inconvenient to generate a negative going START CONVERT PULSE of the proper width, MN5200 Series A/D's can be made to start converting on a positive going edge by employing the circuit shown below. Assuming the previous conversion is done and the Start Signal is low, the STATUS output will be low, the output of IC1 will be high, and the output of IC2 will be high. A rising edge as a Start Signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. Resetting brings the STATUS high; IC1 goes low; the start Signal is still high so the output of IC2 goes high allowing the conversion to continue immediately. The Start Signal has only to be brought back down before the conversion is completed.





24 PIN DIP

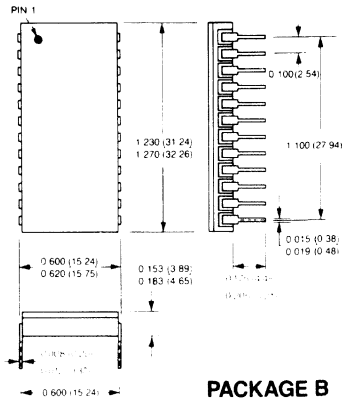


PACKAGE A

24-PIN DIP
Dimensions in Inches
(millimeters)

Note: MN5200 and MN5203 utilize package A.

MN5201, MN5202, MN5204, MN5205, and MN5206 utilize package B.



PACKAGE B

MICRO NETWORKS

MN5210 Series

13μsec, 12-Bit
MILITARY A/D CONVERTERS

FEATURES

- **13μsec Maximum Conversion Time**
- **±1/2LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Small 24-Pin DIP**
- **±1LSB Zero Error**
- **±2LSB Absolute Accuracy**
- **Low Power**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

DESCRIPTION

MN5210 Series devices are high-speed, 12-bit, successive approximation A/D converters in industry-standard, 24-pin dual-in-line packages. Conversion time is 13μsec max, and all specifications are met with a 1MHz clock. Functional laser trimming of our own nichrome thin-film resistor networks results in adjustment-free devices that are extremely accurate and highly stable. Zero error, for example, is guaranteed to be better than ±0.025% FSR (±1 LSB) at +25°C and better than ±0.05% FSR (±2 LSB) over the entire operating temperature range. All units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature.

These A/D converters are available in a number of input voltage ranges. For each range, the user has the option of specifying a model complete with internal reference or, for improved overall accuracy, a model which uses an external reference. In all cases, ±½LSB linearity and 12-bit "no missing codes" are guaranteed over the entire operating temperature range.

All models of the MN5210 Series may be procured for operation over the full −55°C to +125°C military temperature range ("H" models) or the 0°C to +70°C commercial temperature range. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

The MN5210 Series (13μsec conversion time) and MN5200 Series (50μsec conversion time) are the industry's most widely accepted 12-bit A/D's for military/aerospace applications. These devices are presently designed into more than 50 military/aerospace programs. Their small size, low power consumption and adjustment-free operation make them excellent selections for compact, highly reliable systems. New applications will be found wherever size, speed, power and temperature considerations are paramount.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

January 1992
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MN5210 SERIES 13μsec 12-Bit MILITARY A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	-55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
Positive Supply (Pin 15)	+18 Volts
Negative Supply (Pin 13)	-18 Volts
Logic Supply (Pin 2)	-0.5 to +7 Volts
Analog Input (Pin 14)	±25 Volts
Digital Inputs (Pins 1, 24)	-0.5 to +5.5 Volts
Digital Outputs	Logic Supply
Ref. Input (MN5213, 14, 15)	0 to -15 Volts

ORDERING INFORMATION

PART NUMBER ——— MN521X H/B CH

- Select Model Number (MN5210, 5211, etc.)
- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified -55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A=25°C, Supply Voltages ±15V and +5V, for Ext. Ref. Models V_{Ref}=-10.000V, unless otherwise specified).

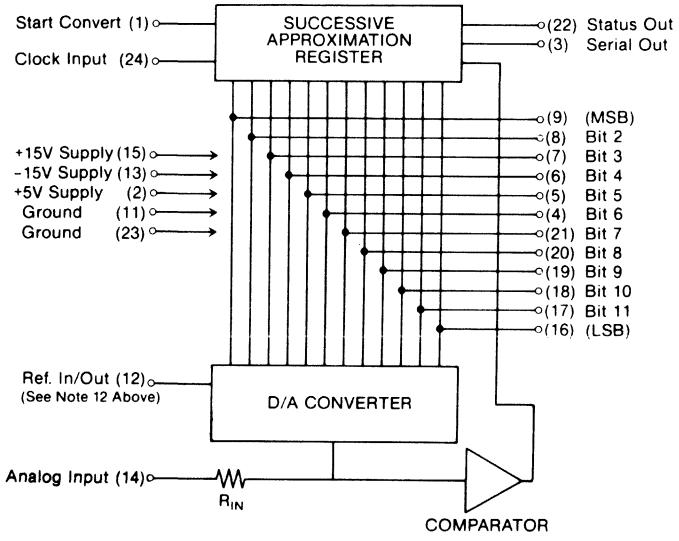
ANALOG INPUTS	MODEL NUMBER (Internal Ref.) MN5210 MN5211 MN5212 MN5216		MODEL NUMBER (External Ref.) MN5213 MN5214 MN5215		
Input Range (Input Impedance) (Note 1): 0 to -10V (5KΩ); -5V to +5V (5KΩ); -10V to +10V (10KΩ); 0 to +10V (5KΩ)					
TRANSFER CHARACTERISTICS	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNITS**
Linearity Error (Notes 2, 3): +25°C	±¼	±½	±¼	±½	LSB
0°C to +70°C	±¼	±½	±¼	±½	LSB
-55°C to +125°C ("H" Models)		±½		±½	LSB
Differential Linearity Error	±½		±½		LSB
No Missing Codes	Guaranteed Over Temperature				
Full Scale Absolute Accuracy Error (Notes 4, 5) +25°C	± 0.025	± 0.05	± 0.025	± 0.05	%FSR
0°C to +70°C	± 0.2	± 0.4	± 0.05	± 0.1	%FSR
-55°C to +125°C ("H" Models)		± 0.4		± 0.1	%FSR
Zero Error (Notes 4, 5): +25°C	± 0.01	± 0.025	± 0.01	± 0.025	%FSR
0°C to +70°C	± 0.025	± 0.05	± 0.025	± 0.05	%FSR
-55°C to +125°C ("H" Models)		± 0.05		± 0.05	%FSR
Gain Error (Note 5)	± 0.025		± 0.025		%
Gain Drift	± 10		± 3		ppm/°C
Conversion Time (Note 6)		13		13	μSec
POWER SUPPLIES					
Power Supply Range: ±15V Supplies		± 3		± 3	%
+5V Supply		± 5		± 5	%
Power Supply Rejection (Note 7): +15V Supply	± 0.005	± 0.02	± 0.005	± 0.02	%FSR/% Vs
-15V Supply	± 0.01	± 0.05	± 0.005	± 0.02	%FSR/% Vs
Current Drain: +15V Supply	23	28	23	28	mA
-15V Supply	-25	-35	-25	-35	mA
+5V Supply	25	42	25	42	mA
-10V Reference (MN5203, 04, 05)			-1.5	-2	mA

DIGITAL INPUTS (ALL UNITS)	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.7	Volts
Clock Input (Note 8): Pulse Width High	125			nSec
Pulse Width Low	175			nSec
Loading High (V_{in}=2.4V)		2	20	μA
Loading Low (V_{in}=0.3V)		-0.25	-0.4	mA
Frequency (Note 6)			1	MHz
Start Convert Input: Loading High (V_{in}=2.4V)		4	40	μA
Loading Low (V_{in}=0.3V)		-0.25	-0.4	mA
Setup Time Start Low to Clock (Note 9)	25			nSec
DIGITAL OUTPUTS (ALL UNITS)				
Logic Coding (Note 10): Unipolar Ranges	Complementary Straight Binary			
Bipolar Ranges	Complementary Offset Binary			
Logic Levels: Logic "1"	2.4	3.6		Volts
Logic "0"		0.15	0.3	Volts
Output Drive Capability, All Outputs (Note 11): Logic "1"	8			TTL Loads
Logic "0"	2			TTL Loads
REFERENCE INPUT/OUTPUT (Note 12)				
Internal Reference: Voltage		-6.3		Volts
Accuracy		±2		%
Tempco of Drift		±5		ppm/°C
Max. External Current (Without Buffering)			100	μA
External Reference: Voltage		-10.000		Volts
Loading			- 2	mA

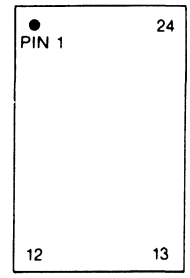
SPECIFICATION NOTES:

1. Consult factory for other available input voltage ranges.
2. Micro Networks tests and guarantees maximum linearity error at room temperature and at both the high and low extremes of the specified operating temperature range.
3. 1 LSB for a 12 bit converter corresponds to 0.024%FSR. See Note 4.
4. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ±10V input range, FSR is 20 volts, and 1 LSB is equal to 4.88 mV. For the 0 to +10V, 0 to -10V, and ±5V ranges, FSR is 10 volts, and 1 LSB is equal to 2.44 mV.
5. See Absolute Accuracy section below for an explanation of how Micro Networks tests and specifies Full Scale Absolute Accuracy, Gain, and Zero Errors.
6. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse (see Timing Diagram). Micro Networks guarantees MN5210 Series converters will meet all specs with clock frequencies up to 1 MHz. A 1 MHz clock gives a STATUS pulse that is 12 μSec wide. The 13 μSec spec reflects the fact that unless careful timing precautions are taken, it will usually take 13 clock periods to update digital output data.
7. Micro Networks tests and guarantees Power Supply Rejection over the ±15V ±3% range.
8. The clock may be asymmetrical with minimum positive or negative pulse width. See Note 6.
9. In order to reset the converter, START CONVERT must be brought low at least 25 nSec prior to a low to high clock transition. See Timing Diagram.
10. CSB = Complementary Straight Binary
    COB = Complementary Offset Binary
    Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
11. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
12. MN5210, MN5211, MN5212, and MN5216 have an internal -6.3V reference. MN5213, MN5214, and MN5215 require an external -10.000V reference.

BLOCK DIAGRAM



PIN DESIGNATIONS

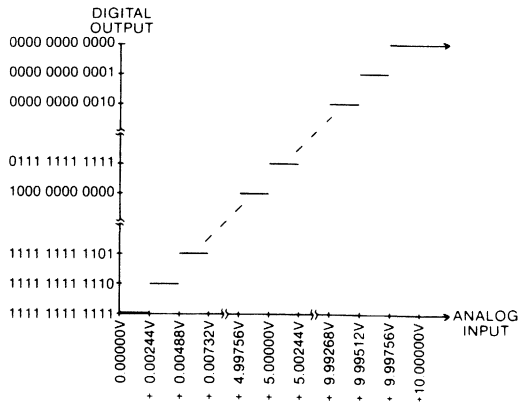


Pin 1	Start Convert	Pin 24	Clock Input
Pin 2	+5V Supply	Pin 23	Ground
Pin 3	Serial Output	Pin 22	Status (E.O.C.)
Pin 4	Bit 6	Pin 21	Bit 7
Pin 5	Bit 5	Pin 20	Bit 8
Pin 6	Bit 4	Pin 19	Bit 9
Pin 7	Bit 3	Pin 18	Bit 10
Pin 8	Bit 2	Pin 17	Bit 11
Pin 9	Bit 1 (MSB)	Pin 16	Bit 12 (LSB)
Pin 10	2.2 μF to +15V	Pin 15	+15V Supply
Pin 11	Ground	Pin 14	Analog Input
Pin 12	Ref. Out (-6.3V) Ref. In (-10.0V)	Pin 13	-15V Supply

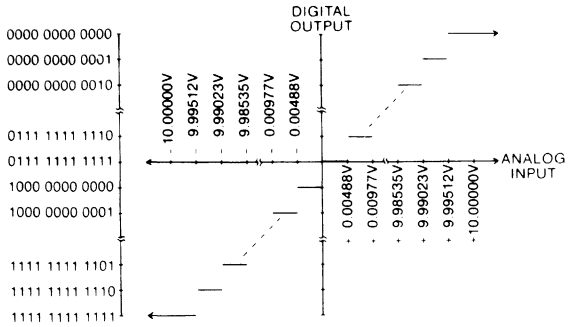
ABSOLUTE ACCURACY ERROR

A given digital output code is valid for a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated in the next column and on the following page where portions of the theoretical analog input/digital output transfer functions of the MN5216 (0 to +10V input range) and the MN5212 (±10V input range) are sketched.

Notice that, for the MN5216, any analog input between +0.00244 volts (1 LSB = 2.44 mV) and +0.00488 volts will give a digital output of 1111 1111 1110. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 1111 1111 1110 digital code corresponds to analog inputs of +3.66 mV ±1.22 mV which can be written as +3.66 mV ±1/2 LSB. The ±1/2 LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error and its magnitude can be reduced only by going to higher resolution converters.



MN5216 TRANSFER FUNCTION



MN5212 TRANSFER FUNCTION

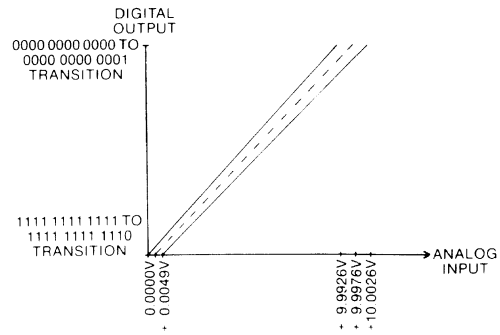
It is difficult and time consuming to measure the center of a quantization level (the +0.00366 volts in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted,* analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR (see Note 4 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors.

For the MN5210 Series A/D converters, Micro Networks tests Absolute Accuracy Error at both endpoints of unipolar input ranges and at both endpoints and the midpoint of bipolar input ranges. These tests are performed at room temperature and at both the high and low extremes of the specified operating temperature range. The specifications appear in the table as the Full Scale Absolute Accuracy and Zero Errors.

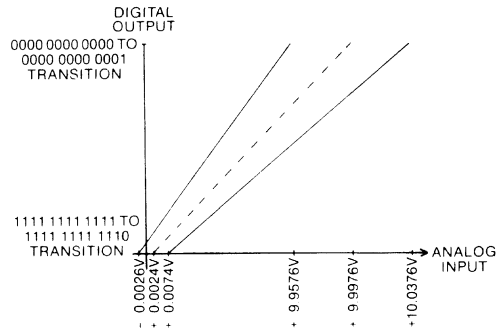
EXAMPLE MN5216: Return to the ideal analog input/digital output transfer function of the MN5216 sketched on page 3. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from 0V to +2.44 mV. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to +2.44 mV. This voltage, +2.44 mV is the zero transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9976V.

For the MN5216H (0 to +10V input range, -55°C to +125°C operation), Micro Networks tests linearity and the accuracy of the two transition voltages just discussed at -55°C, +25°C, and +125°C. We guarantee that the transfer function will be ±1/2 LSB linear at all temperatures and that the zero transition will be within ±0.025%FSR (±2.5 mV) of its ideal value (+2.44 mV) at +25°C and within ±0.05%FSR (±5 mV) of its ideal value at -55°C and at +125°C. This is our Zero Error specification. We guarantee that the positive full scale LSB transition voltage will be within ±0.05%FSR (±5 mV) of its ideal value (+9.9976V) at +25°C and within ±0.4%FSR (±40 mV) of its ideal value at -55°C and +125°C. This is our Full Scale Absolute Acuracy Error specification.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5216H, that the actual transfer function will be ±1/2 LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at -55°C and +125°C.



MN5216 ABSOLUTE ACCURACY +25°C



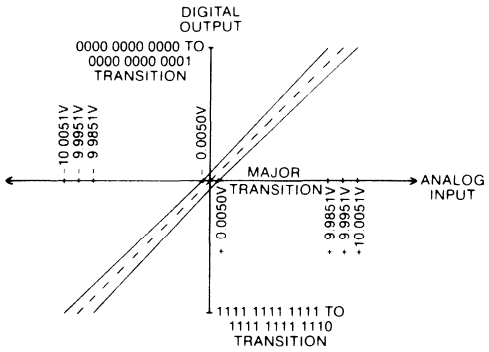
MN5216H ABSOLUTE ACCURACY -55°C AND +125°C

EXAMPLE MN5212: Return to the ideal analog input/digital output transfer function of the MN5212 sketched above. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from -10.000V to -9.9951V. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to -9.9951V. This voltage, -9.9951V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The 1000 0000 0000 to 0111 1111 1111 transition (called the "major transition" because all the bits change) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9951V.

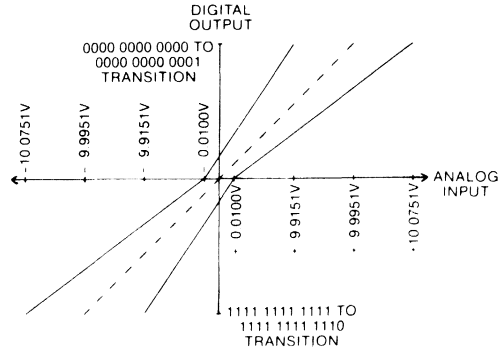
For the MN5212H (±10V input range, -55°C to +125°C operation), Micro Networks tests linearity and the accuracy of the three transition voltages just discussed at -55°C, +25°C, and +125°C. We guarantee that the transfer function will be ±1/2 LSB linear at all temperatures and that the positive and negative full scale LSB transition voltages will be within ±0.05%FSR (±10 mV) of their ideal values (+9.9951V and -9.9951V) at +25°C and within ±0.4%FSR (±80 mV) of their ideal values at -55°C and +125°C. This is our Full Scale

Absolute Accuracy Error specification. We also guarantee that the major transition voltage will be within ±0.025%FSR (±5 mV) of its ideal value (zero volts) at +25°C and within ±0.05%FSR (±10 mV) of its ideal value over the entire -55°C to +125°C operating temperature range. This is our Zero Error specification.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5212H, that the actual transfer function will be ±1/2 LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at -55°C and +125°C.



MN5212 ABSOLUTE ACCURACY +25°C

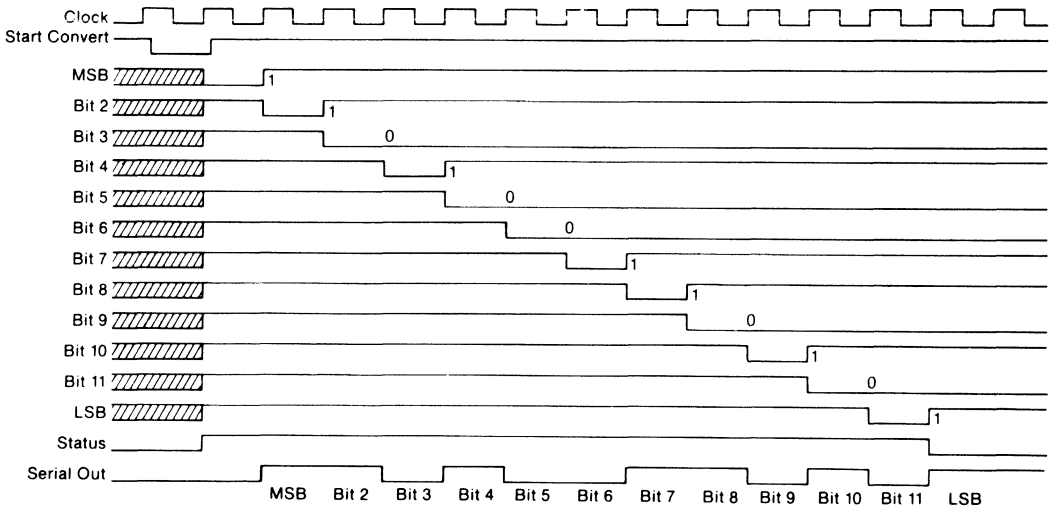


MN5212H ABSOLUTE ACCURACY -55°C AND +125°C

Because Micro Networks tests and guarantees ±1/2 LSB linearity at all temperatures, the Absolute Accuracy of any transition voltage can be interpolated from the Full Scale Absolute Accuracy and Zero Error specifications. Example: at +25°C, the 1000 0000 0000 to 0111 1111 1111 transition of the MN5216 will occur within ±0.0375%FSR (±3.75 mV) of its ideal value (+5.000V). For temperatures intermediate to +25°C and -55°C or +125°C, maximum Full Scale Absolute Accuracy and Zero Errors can also be interpolated. At +75°C, for example, Full Scale Absolute Accuracy Error will be ±0.225%FSR.

We have not specified Unipolar and Bipolar Offset Errors for the MN5210 Series. We feel that Offset is a confusing

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0011 0101 which corresponds to 1.7432V on the 0 to +10V input range (MN5216). See Output Coding.
2. Conversion time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nSec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 120 nSec maximum.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 30 nSec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated.
8. For continuous conversion, connect the STATUS output (Pin 22) to the START CONVERT input (Pin 1). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

specification and choose not to use it. Offset Errors for the MN5210 Series will always be equivalent to either our Full Scale Absolute Accuracy or Zero Errors and we prefer these specifications because of their simplicity. Be sure you clearly understand each manufacturer's converter specification definitions before you compare converters solely on a data sheet basis.

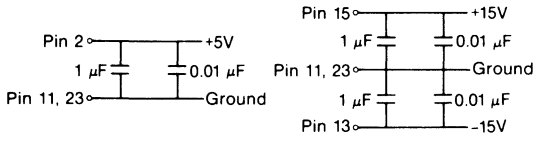
GAIN ERROR—*Gain Error is the difference* between the ideal and the measured values of a converter's Full Scale Range (minus 2 LSB); it is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 0000 0000 0000 to 0000 0000 0001 transition minus that measured for the 1111 1111 1111 to 1111 1111 1110 transition.

See the Converter Tutorial Section of the Micro Networks' Applications Manual and Product Guide for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5210 Series converters. A 2.2μF (25V) non-polarized capacitor must be connected between Pin 10 and +15V. The units' two GROUND pins (Pins 11 and 23) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between Pins 11 and 23 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.



POWER SUPPLY DECOUPLING

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's START CONVERT (Pin 1) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the STATUS output (Pin 22) is set to logic "1" (see Timing Diagram). The START CONVERT must now be brought high again for the conversion to continue. If the START is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the START has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 12) also drops the STATUS OUTPUT to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

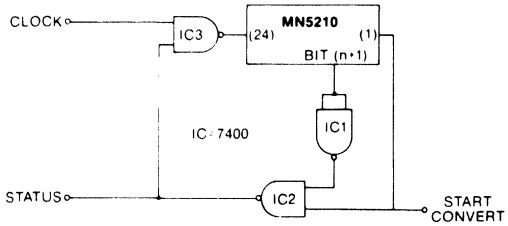
CONTINUOUS CONVERTING — The MN5210 Series A/D converters can be made to continuously convert by tying the STATUS output (Pin 22) to the START CONVERT input (Pin 1). In this configuration, STATUS (START CONVERT) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing STATUS (START CONVERT) high again. The MSB will be set on the next rising clock edge. The result is that the STATUS will go low for approximately one clock period following each conversion. Please read the section describing the STATUS output. See below for continuous conversions while short cycling.

DIGITAL OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT
MN5210, 5213	MN5211, 5214	MN5212, 5215	MN5216	MSB LSB
0.0000V - 0.0024V	+5.0000V +4.9976V	+10.0000V + 9.9951V	+10.0000V + 9.9976V	0000 0000 0000 0000 0000 0000*
- 4.9976V - 5.0000V - 5.0024V	+0.0024V 0.0000V -0.0024V	+ 0.0049V 0.0000V - 0.0049V	+ 5.0024V + 5.0000V + 4.9976V	0111 1111 1110* 0000 0000 0000* 1000 0000 0000*
- 9.9976V -10.0000V	-4.9976V - 5.0000V	- 9.9951V -10.0000V	+ 0.0024V 0.0000V	1111 1111 1110* 1111 1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as 0 will change from "1" to "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages.
EXAMPLE: For an MN5212/15 (±10V analog input range) the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.9951 volts. Subsequently, any input voltage more positive than +9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at −9.9951 volts. An input more negative than −9.9951 volts will give all "1's".

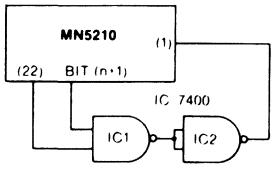
SHORT CYCLING—For applications requiring less than 12 bits resolution, the MN5210 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.



SHORT CYCLING SINGLE CONVERSIONS

Assuming a conversion is already in progress, bit (n+1) will go low as bit n is being set (see Timing Diagram). Since the START CONVERT signal is high at this time, STATUS (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, START CONVERT is brought low driving STATUS high and gating on the clock. The first rising clock edge the converter sees with START CONVERT low will reset the converter bringing bit (n+1) high again. Now STATUS will remain high as START CONVERT is brought back high allowing the conversion to continue. Therefore, in this configuration, STATUS and START CONVERT function normally, i.e., the same as STATUS and START CONVERT for a converter not being short cycled.

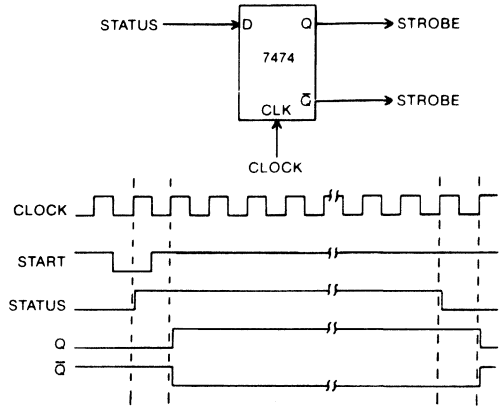
SHORT CYCLING AND CONTINUOUS CONVERTING—A previous section described how continuous converting for 12 bits could be accomplished by simply tying the STATUS output back to the START CONVERT input. To continuously convert at n bits, one simply has to tie the bit (n+1) output back to the START CONVERT input. The bit (n+1) output acts like a STATUS when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n+1) comes on as a "1" and the conversion process comes on at bit (n+2). This situation can be avoided by making the START CONVERT input the AND function of bit (n+1) and the STATUS output.



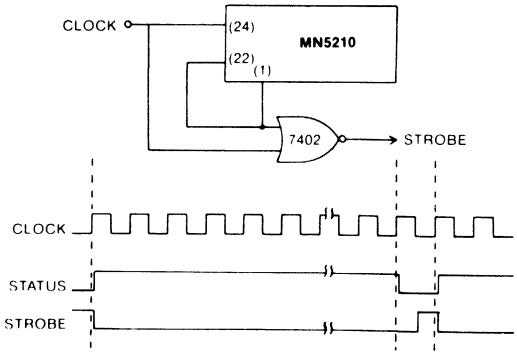
SHORT CYCLING CONTINUOUS CONVERTING

If one is already using the circuit described in the section labeled SHORT CYCLING, one can short cycle and continuously convert by making the START CONVERT input the AND function of STATUS (IC2) and STATUS (pin 7) outputs.

STATUS OUTPUT—The STATUS or END OF CONVERSION (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 30 nSec after STATUS has returned low. Therefore, an adequate delay must be provided if STATUS is to be used to strobe latches to hold output data. Simple gate delays can be employed or the STATUS can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after STATUS changes.



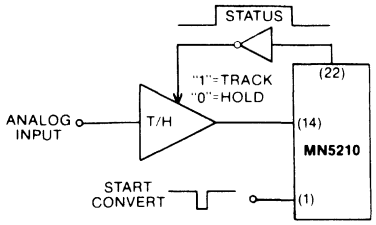
If continuously converting the STATUS (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse 1/2 period wide, 1/2 period after the STATUS output has gone low. The rising edge of this pulse can be used to latch data after each conversion.



USING A TRACK AND HOLD AMP WITH MN5210 SERIES A/D's—The error that results when trying to convert moving analog signals with a successive approximation A/D can be as great as the amount the analog signal changes during a single A/D conversion time. If this error is unacceptable, a Track and Hold (T/H) or Sample and Hold (S/H) amplifier can be placed between the analog signal source and the A/D converter. A careful error analysis will be necessary to determine if the T/H is actually reducing and not increasing overall error. T/H parameters such as aperture uncertainty, gain accuracy, pedestal error and droop rate will have to be contended with (see the tutorial section of the Micro Networks'

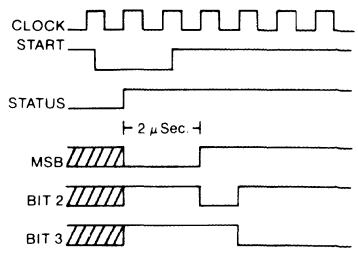
Applications Manual and Product Guide for a complete discussion of T/H parameters).

Normally, the T/H can be controlled directly by the A/D's STATUS output. Typical connections are shown below for Micro Networks' MN343 (10 μSec acquisition time to ±0.01%) and MN346 (1.6 μSec acquisiton time to ±0.01%) Track and Hold Amplifiers. The STATUS output changes form a "0" to a "1" when the converter is reset. This drives the T/H from the track to the hold mode. At the end of conversion, STATUS returns to a "0" restoring the T/H to the track mode.

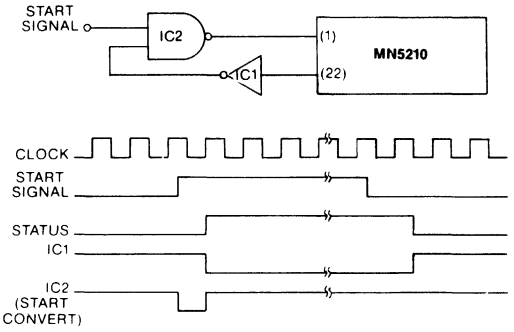


MN343		MN346
10 μSec	Acquisition Time	1.6 μSec
60 nSec	Aperature Delay	30 nSec
3 mV	Pedestal Error	2 mV
0.1 mV/mSec	Droop Rate	0.1 mV/mSec
1.5 μSec	Track to Hold Settling	150 nSec

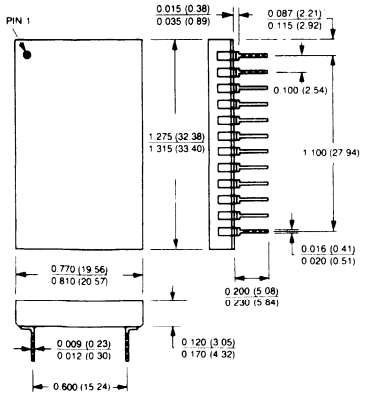
Recall that if the START CONVERT pulse is brought high immediately after the converter has been reset, the MSB will be finalized one clock period later (see Timing Diagram). Care should be taken to ensure aperture delay time and track-to-hold settling time do not contribute errors. If necessary, the width of the START CONVERT pulse can be increased to allow more time between the T/H being commanded into the hold mode (STATUS = "1") and the MSB being set. Recall that output bits do not begin to get set until after the START CONVERT has returned high. The example below shows a 2μSec delay to allow for track to hold settling. Clock frequency = 1 MHz; 1 period = 1 μSec.



TRIGGERING WITH A POSITIVE EDGE—If it is inconvenient to generate a negative going START CONVERT PULSE of the proper width, MN5210 Series A/D's can be made to start converting on a positive going edge by employing the circuit shown below. Assuming the previous conversion is done and the Start Signal is low, the STATUS output will be low, the output of IC1 will be high, and the output of IC2 will be high. A rising edge as a Start Signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. Resetting brings the STATUS high; IC1 goes low; the start Signal is still high so the output of IC2 goes high allowing the conversion to continue immediately. The Start Signal has only to be brought back down before the conversion is completed.



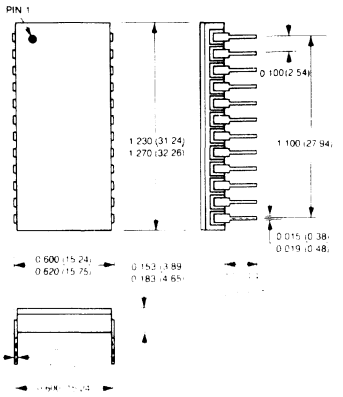
PACKAGING



PACKAGE A

24-PIN DIP
Dimensions in Inches
(millimeters)

Note: MN5210 and MN5213 utilize package A.
MN5211, MN5212, MN5214, MN5215, and MN5216 utilize package B.



PACKAGE B

MICRO NETWORKS

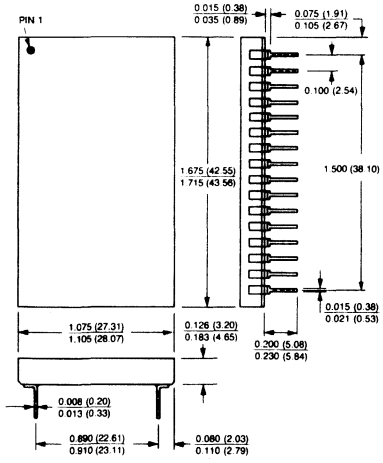
MN5240

10 and 12-Bit
HIGH-SPEED
A/D CONVERTERS

FEATURES

- **Fast Conversion Times:**
  5μsec Max for 12 Bits
  4.2μsec Max for 10 Bits
- **Complete A/D Function:**
  Internal Clock
  Internal Reference
  Input Buffer
  Short-Cycle Pin
- **No Clock Adjusting Necessary**
- **Small 32-Pin DIP**
- **5 User-Selectable Input Ranges**
- **0°C to +70°C or −55°C to +85°C Operation**

32 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5240 is a high-speed, successive approximation analog-to-digital converter that offers versatility and excellent overall performance at moderate cost. Models are available in either 10 or 12-bit linearities for either 0°C to +70°C or −55°C to +85°C operation. Conversion time is 5μsec max for 12-bit models and 4.2μsec max for 10-bit models. These conversion times are guaranteed using the internal clock, and no clock adjusting is necessary.

Features of MN5240 include convenient, hermetic dual-in-line packaging, 5-user selectable analog input ranges, short cycling capability and the choice of internal or external clock. Also included are both serial and parallel data outputs and a status output for easy interfacing in microprocessor-based applications. For military/aerospace applications, the MN5240F/B is available with Environmental Stress Screening.

Micro Networks MN5240 is pin compatible with ADC84 and ADC85 Series A/D Converters and can be used to upgrade performance and improve throughput in existing designs employing those devices. For new designs, MN5240 is being used in high-speed data acquisition systems, in automatic test equipment and in ECM equipment. For data acquisition systems applications, MN5240 can be used with Micro Networks MN7130 Multiplexed Track-Hold Amplifier to configure a 16-channel data acquisition system with a 58,000 channels/sec throughput rate in only two dual-in-line packages.

Part Number	Specified Temperature Range	No Missing Codes Over Temperature	Maximum Conversion Time
MN5240	0°C to +70°C	12 Bits	5μsec
MN5240F	−55°C to +85°C	12 Bits	5μsec
MN5240F/B	−55°C to +85°C	12 Bits	5μsec
MN5240-10	0°C to +70°C	10 Bits	4.2μsec
MN5240-10F	−55°C to +85°C	10 Bits	4.2μsec
MN5240-10F/B	−55°C to +85°C	10 Bits	4.2μsec

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

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MN5240 10 and 12-Bit HIGH-SPEED A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5240, MN5240-10	0°C to +70°C
MN5240F, F/B; MN5240-10F, F/B	−55°C to +85°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 28)	0 to +18 Volts
Negative Supply (−Vcc, Pin 31)	0 to −18 Volts
Logic Supply (+Vdd, Pin 16)	0 to +7 Volts
Analog Inputs: Direct (Pins 24, 25)	±25 Volts
Buffer (Pin 30)	±15 Volts
Digital Inputs (Pins 14, 21)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — **MN5240 F/B**

Standard part is specified for 0°C to +70°C operation.

Add "F" suffix for specified −55°C to +85°C operation.

Add "/B" suffix to "F" models for Environmental Stress Screening.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +5, 0 to +10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Input Impedance (Direct) (Note 1): 0 to +5V, ±2.5V		2.5		kΩ
0 to +10V, ±5V		5		kΩ
±10V		10		kΩ
Buffer Amplifier (Note 1): Input Impedance	100			MΩ
Input Bias Current		50		nA
Settling Time to 0.01% for 20V Step (Note 2)		2		μsec
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
TRANSFER CHARACTERISTICS (Note 3)				
Resolution		12		Bits
Linearity Error (Note 13): Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 4)		±¼	±½	LSB
Temperature Range for Guaranteed No Missing Codes (Note 13):				
MN5240, MN5240-10	0		+70	°C
MN5240F, F/B; MN5240-10F, F/B	−55		+85	°C
Unipolar Zero Error (Notes 5, 6): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 4)		±0.07	±0.12	%FSR
Bipolar Zero Error (Notes 5, 7): Initial (+25°C)		±0.1	±0.2	%FSR
Over Temperature (Note 4)		±0.15	±0.25	%FSR
Full Scale Absolute Accuracy Error (Notes 5, 8):				
Unipolar: Initial (+25°C)		±0.1	±0.3	%FSR
Over Temperature (Note 4)		±0.2	±0.4	%FSR
Bipolar: Initial (+25°C)		±0.15	±0.4	%FSR
Over Temperature (Note 4)		±0.2	±0.5	%FSR
DIGITAL OUTPUTS				
Output Coding (Note 9): Parallel Outputs: Unipolar		CSB		
Bipolar		COB, CTC		
Serial Outputs (Note 10): Unipolar		CSB		
Bipolar		COB		
Logic Levels All Outputs: Logic "1" ($I_{SOURCE} \leq 40\mu A$)	+2.4			Volts
Logic "0" ($I_{SINK} \leq 3.2mA$)			+0.4	Volts
REFERENCE OUTPUT				
Internal Reference (Note 1): Voltage		+6.3		Volts
Tempco		±10		ppm/°C
External Current			200	μA
DYNAMIC CHARACTERISTICS				
Conversion Time (12-bits, Note 11)			5	μsec
Internal Clock Frequency (Note 1)	2.4			MHz
Start Convert Pulse Width (Note 1)	50			nsec

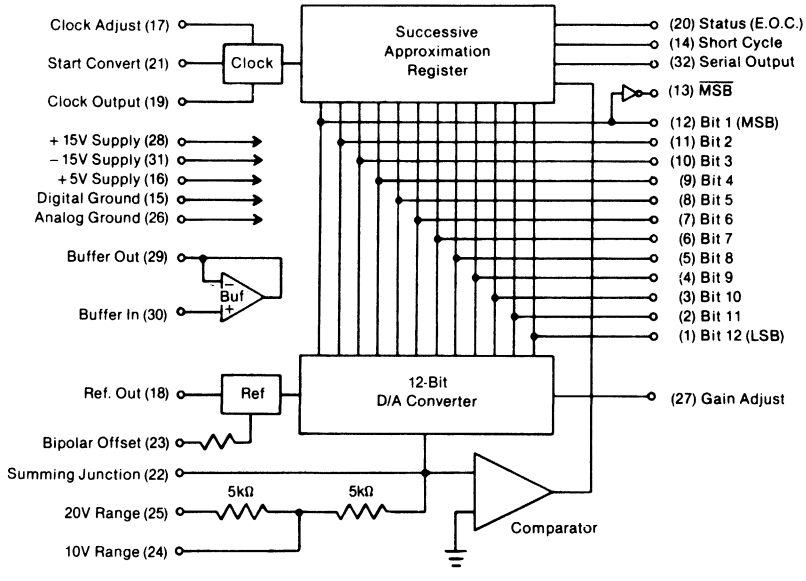
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Ranges: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Notes 1, 12): +15V Supply		±0.004		%FSR/%Supply
−15V Supply		±0.004		%FSR/%Supply
+5V Supply		±0.001		%FSR/%Supply
Current Drain: +15V Supply		+30	+45	mA
−15V Supply		−40	−60	mA
+5V Supply		+70	+105	mA
Power Consumption		1400	2100	mW

SPECIFICATION NOTES:

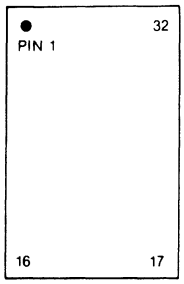
1. These parameters are listed for reference only and are not tested.
2. Buffer settling time is added to conversion time when calculating system throughput when using the internal buffer. See section labeled Internal Buffer Amplifier.
3. FSR=full scale range. A unit connected for a 0 to +5V or ±2.5V input range has a 5V FSR. A unit connected for a 0 to +10V or ±5V input input range has a 10V FSR, etc.. 1LSB for 12 bits is equivalent to 0.024% FSR. 1LSB for 10 bits is equivalent to 0.098% FSR.
4. Listed specification applies over the 0°C to +70°C temperature range for MN5240 and MN5240-10. Listed specification applies over the −55°C to +85°C temperature range for MN5240F, F/B and MN5240-10F, F/B.
5. Initial zero and absolute accuracy errors are adjustable to zero with the use of external potentiometers.
6. Unipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1110 to 1111 1111 1111 transition occurs when operating on a unipolar input range. See Digital Output Coding table.
7. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs when operating on a bipolar input range. See Digital Output Coding table.
8. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0001 to 0000 0000 0000 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 1111 1111 1110 to 1111 1111 1111 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1LSB below the nominal positive full scale voltage. The latter ideally occurs 1LSB above the nominal negative full scale voltage. See Digital Output Coding.
9. CSB=complementary straight binary. COB=complementary offset binary. CTC=complementary two's complement.
10. Serial data is in non-return-to-zero (NRZ) format and is coded in CSB and COB.
11. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 2 (bit 11) to pin 14 (Short Cycle) for 10-bit conversions. See Timing Diagram.
12. Power Supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0001 to 0000 0000 0000 output transitions occur versus a change in power-supply voltage.
13. MN5240, F and F/B guarantee ±½LSB linearity error and no missing codes for 12-bit resolution. MN5240-10, F and F/B guarantee ±½LSB linearity error and no missing codes for 10-bit resolution.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



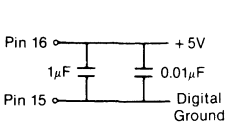
1 Bit 12 (LSB)
2 Bit 11
3 Bit 10
4 Bit 9
5 Bit 8
6 Bit 7
7 Bit 6
8 Bit 5
9 Bit 4
10 Bit 3
11 Bit 2
12 Bit 1 (MSB)
13 $\overline{\text{MSB}}$
14 Short Cycle
15 Digital Ground
16 +5V Supply (+Vdd)
32 Serial Output
31 −15V Supply (−Vcc)
30 Buffer Input
29 Buffer Output
28 +15V Supply (+Vcc)
27 Gain Adjust
26 Analog Ground
25 20V Range
24 10V Range
23 Bipolar Offset
22 Summing Junction
21 Start Convert
20 Status (E.O.C.)
19 Clock Output
18 Reference Output (+6.3V)
17 Clock Adjust

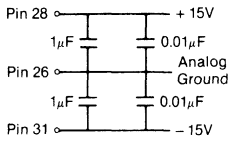
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies. Analog and digital grounds (pins 15 and 26) are not connected to each other internally and must be tied together as close to the package as possible, preferably through a large analog ground plane underneath the package. If these commons must be run separately, a non-polarized, 0.01 to 0.1μF bypass capacitor should be connected between pins 15 and 26 as close to the package as possible and wide conductor runs should be used.

Coupling between the analog inputs and digital signals should be minimized to reduce noise pickup. The Summing Junction (pin 22) is the direct input to the internal comparator, and is particularly noise susceptible. In bipolar operation, where pin 22 is connected to pin 23, a short jumper should be used, and when external offset adjustment is employed, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the device package. For optimum results, 1μF capacitors paralleled by 0.01μF ceramic capacitors should be connected as shown in the diagrams below. An additional 0.01μF ceramic bypass capacitor should be located close to the package connecting the gain adjust point (pin 27) to analog ground.





For normal 12-bit operation using the internal clock, Clock Adjust (pin 17) and Short Cycle (pin 14) should be connected to +5V (pin 16).

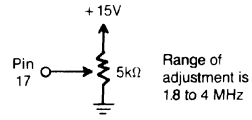
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit of any conversion will not be valid until a maximum of 120nsec after the Status output has gone low.

SHORT CYCLING—For applications requiring less than 12 bits resolution, these converters can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. The connections shown below truncate the converter to provide the minimum conversion time for a given resolution.

Resolution (Bits)	12	10	8
Connect Pin 17 to Pin	16	16	16
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μsec)	5	4.2	3.3
Clock Speed (MHz)	2.4	2.4	2.4

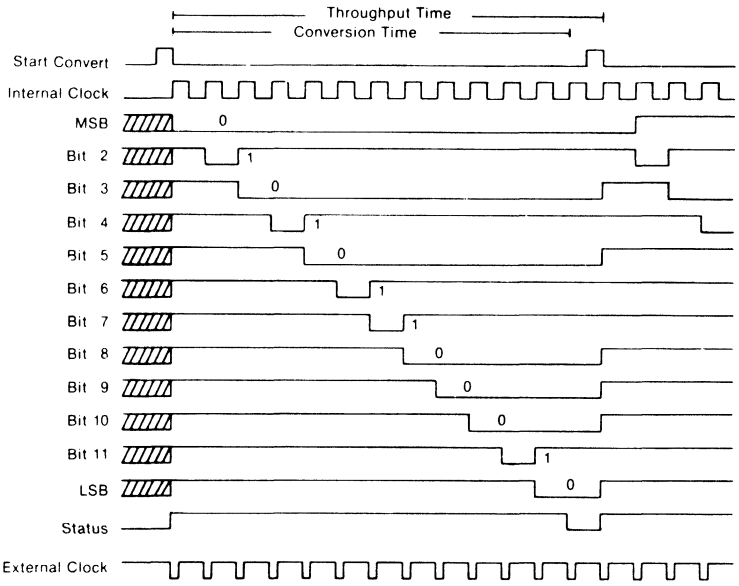
CLOCK RATE—The internal clock is preset to approximately 2.4MHz and can be adjusted over a range of 1.8 to 4 MHz. To adjust the internal clock, a multiturn pot (TCR of 100ppm/°C or less) is connected to pin 17 as shown in the diagram below.



EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. In this mode of operation, the converter will provide a continuous string of conversions each of which begins on the first falling edge of the external clock after Status (E.O.C.) has gone low.

INTERNAL BUFFER AMPLIFIER—MN5240 provides a user-optional internal buffer amplifier. Use of this buffer amplifier provides an input impedance greater than 100MΩ allowing the A/D to be driven from high impedance sources or directly from an analog multiplexer. When using the optional buffer amplifier, a 2μsec delay must be provided to allow the amplifier to settle prior to triggering the Start Convert input. If the buffer amplifier is not required, its input should be connected to analog ground to avoid introducing noise into the converter.

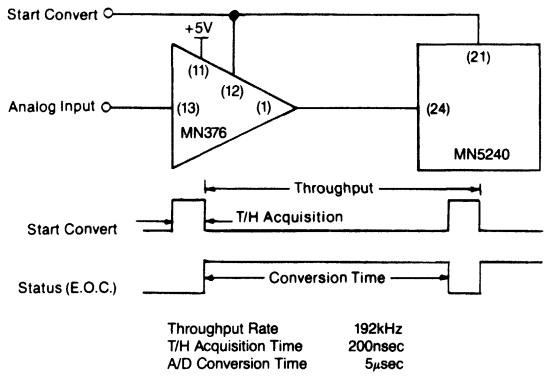
TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Conversion time is defined as the width of the Status pulse.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. The delay from the falling edge of the Start Convert signal to Status actually rising to a "1" may be 100nsec.
5. Parallel data will be valid 120nsec after the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
6. The delay from clock to serial data valid will be a maximum of 140nsec from a rising internal clock edge or a maximum of 200nsec from a falling external clock edge.
7. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock section.
8. Once a conversion has begun, a second start pulse will not reset the converter. See Start Convert section.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

USING A TRACK/HOLD AMPLIFIER WITH MN5240—When using a track-hold (T/H) amplifier with MN5240, the T/H can be driven directly (or inverted) from the A/D's Start Convert signal. When the Start is high prior to the beginning of a conversion, the T/H can be in the tracking or signal acquisition mode. The falling edge of the start signal initiates the conversion and simultaneously commands the T/H into the hold mode. The MSB output will be set to its final value one internal clock period later (approximately 0.42μsec), and the track-to-hold transient of the chosen T/H should have settled to within ±0.01%FSR of its final value by that time. The width of the start convert pulse may have to be lengthened to accommodate the acquisition time spec of the chosen T/H or to allow valid output data to be latched.

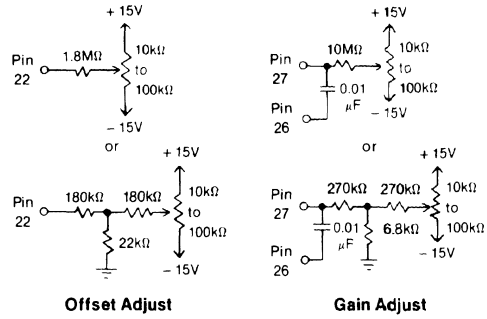


Throughput Rate	192kHz
T/H Acquisition Time	200nsec
A/D Conversion Time	5μsec

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 22 should be connected as described in the Input Range Selection section and a 0.01μF capacitor should be connected from pin 27 to pin 26.

OFFSET ADJUSTMENTS—Connect the offset potentiometer as shown and apply the input voltage at which the 1111 1111 1110 to 1111 1111 1111 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off. A 0.01μF capacitor should be connected from Gain Adjust (pin 27) to Analog Ground (pin 26).



Offset Adjust **Gain Adjust**

INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
FOR NORMAL INPUT					
Input Impedance (kΩ)	2.5	5	2.5	5	10
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	Input Signal
Connect Pin 30 to Pin	26	26	26	26	26
Connect Input to Pin	24	24	24	24	25
FOR BUFFERED INPUT					
Input Impedance (MΩ)	100	100	100	100	100
Connect Pin 23 to Pin	26	26	22	22	22
Connect Pin 25 to Pin	22	Open	22	Open	29
Connect Pin 29 to Pin	24	24	24	24	25
Connect Input to Pin	30	30	30	30	30

DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Outputs
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB LSB
+5.0000	+10.0000	+2.5000	+5.0000	+10.0000	0000 0000 0000
+4.9988	+9.9976	+2.4988	+4.9976	+9.9951	0000 0000 000Ø*
+2.5012	+5.0024	+0.0012	+0.0024	+0.0049	0111 1111 111Ø*
+2.5000	+5.0000	0.0000	0.0000	0.0000	ØØØØ ØØØØ ØØØØ*
+2.4988	+4.9976	-0.0012	-0.0024	-0.0049	1000 0000 000Ø*
+0.0012	+0.0024	-2.4988	-4.9976	-9.9951	1111 1111 111Ø*
0.0000	0.0000	-2.5000	-5.0000	-10.0000	1111 1111 1111

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary (CSB).
2. For bipolar input ranges, output coding is complementary offset binary (COB).
3. For bipolar input ranges, complementary two's complement coding (CTC) can be obtained by using the complement of the most significant bit. $\overline{\text{MSB}}$ is available on pin 13. See Pin Designations.
4. For 0 to +5V or ±2.5V input ranges. 1LSB for 12 bits=1.22mV. 1LSB for 10 bits=4.88mV.
5. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits=2.44mV. 1LSB for 10 bits =9.77mV.
6. For ±10V input range, 1LSB for 12 bits=4.88mV. 1LSB for 10 bits=19.5mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For a MN5240 operating on its ±10V range, the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of -9.9951V (-Full Scale +1LSB). Subsequently, any input voltage more negative than -9.9951V will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input voltage of 0V and the 0000 0000 0001 to 0000 0000 0000 transition should occur at +9.9951V (+Full Scale -1LSB). An input more positive than +9.9951V will give all "0's".

MICRO NETWORKS

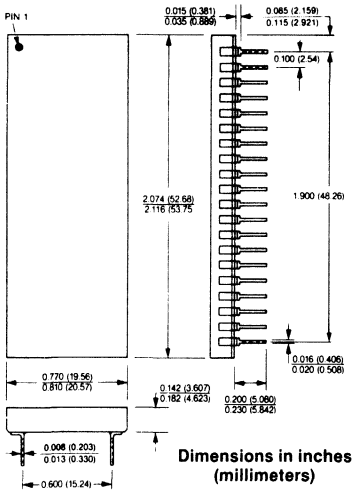
MN5245
MN5246

1.1 MHz, 12-Bit
A/D CONVERTERS

FEATURES

- 850nsec Maximum Conversion Time
- Guaranteed 1.1MHz Conversion Rate
- 1MHz Sampling Rate When used with MN376 T/H Amplifier
- Multisourced
- Small 40-Pin DIP
- No Missing Codes Guaranteed Over Temperature
- TTL Compatible
- 3-State Output Buffer (MN5245A, MN5246A)
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

40 PIN DIP



Dimensions in inches (millimeters)

DESCRIPTION

MN5245, MN5245A, MN5246 and MN5246A are 850nsec, 12-bit, A/D converters that guarantee 1.1MHz conversion rates. When used with MN376 High-Speed T/H Amplifiers, these A/D's can be configured to form bonafide, 1MHz, sample-and-convert systems that can digitize full-scale (5V) input signals with bandwidths up to 500kHz. These systems typically achieve signal-to-noise ratios of 70dB with harmonics down more than −80dB while digitizing 500kHz signals at the Nyquist rate.

Packaged in standard, 40-pin, hermetically sealed, ceramic dual-in-lines, MN5245 and MN5246 A/D converters offer an outstanding combination of resolution, speed, size and cost. These TTL compatible devices achieve their sub-1usec conversion speed using the digitally corrected subranging (serial-parallel) A/D conversion technique. Recent advances in monolithic flash A/D converters and improvements in digital error correcting techniques have enabled us to reduce chip count over previous designs while improving performance.

MN5245 has a 0 to +5V analog input range; while MN5246 has a ±2.5V analog input range. "A" versions of each device contain internal 3-state output buffers to facilitate microprocessor interfacing. All models guarantee ±0.024% FSR integral linearity and "no missing codes" for 12 bits over their entire specified temperature ranges.

MN5245 and MN5246 are ideal design solutions for high-speed digitizing applications in which speed, accuracy, size and reliability are paramount considerations. Typical applications include spectrum, vibration, waveform and transient analyzers; radar, sonar and video digitizers; medical imaging equipment; digital filters; and multiplexed or simultaneous-sampling data-acquisition systems.

MN5245 and MN5246 are manufactured in Micro Networks MIL-STD-1772 qualified hybrid facility, and for military/aerospace and harsh-environment industrial applications, they are available 100% screened to MIL-H-38534.

MICRO NETWORKS
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January 1992
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MN5245 MN5246 1MHz 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125° C (case)
Specified Temperature Range:	
MN5245, 45A, 46, 46A	0°C to +70°C (case)
MN5245E, 45AE, 46E, 46AE	−25°C to +85°C (case)
MN5245H, 45AH, 46H, 46AH	−55°C to +125°C (case)
MN5245H/B, 45AH/B, 46H/B, 46AH/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 9)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 3)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pins 15, 22, 39)	−0.5 to +7 Volts
Digital Inputs (Pins 36 and 37)	−0.5 to +5.5 Volts
Analog Input (Pin 1): MN5245, MN5245A	−1 to +6 Volts
MN5246, MN5246A	−3.5 to +3.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5245A H/B CH

- Select MN5245 or MN5246.
- Add "A" suffix for optional 3-state output buffer.
- Standard Part is specified for 0°C to +70°C operation.
- Add "E" suffix for specified −25°C to +85°C (case) operation.
- Add "H" suffix for specified −55°C to +125°C (case) operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: MN5245, MN5245A		0 to +5		Volts
MN5246, MN5246A		−2.5 to +2.5		Volts
Input Impedance (Note 11)		2/10		kΩ/pF
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0		+5.0	Volts
Logic "0"	0		+0.8	Volts
Loading (Note 2): Start Convert Input			1	LS TTL Load
Data Enable Input (MN5245A, MN5246A)			1	LS TTL Load
TRANSFER CHARACTERISTICS (Note 3)				
Integral Linearity Error: Initial (+25°C)		±½	±1	LSB
Over Temperature		±½	±1	LSB
12-Bit No Missing Codes		Guaranteed Over Temperature		
Full Scale Absolute Accuracy Error (Note 4): Initial (+25°C)		±0.05	±0.15	%FSR
Over Temperature		±0.1	±0.3	%FSR
Unipolar Offset Error (MN5245, MN5245A; Note 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature		±0.1	±0.15	%FSR
Drift		±10	±20	ppm of FSR/°C
Bipolar Zero Error (MN5246, MN5246A; Note 6): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature		±0.1	±0.2	%FSR
Drift		±10	±25	ppm of FSR/°C
Gain Error (Note 7): Initial (+25°C)		±0.05	±0.1	%
Over Temperature		±0.1	±0.3	%
Drift		±15	±40	ppm/°C
DIGITAL OUTPUTS				
Output Coding (Note 8): MN5245, MN5245A		Straight Binary		
MN5246, MN5246A		Offset Binary		
Output Logic Levels (Note 12): Logic "1" ($I_{SOURCE} \leq 100\mu A$)	+2.7			Volts
Logic "0" ($I_{SINK} \leq 2mA$)			+0.5	Volts
Leakage (Bit 1-Bit 12) in High-Z State (MN5245A, MN5246A):				
Logic "1" (V_{OH} = +2.7V)			+10	μA
Logic "0" (V_{OL} = +0.4V)			−10	μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 9)		825	850	nsec
Conversion Rate (Note 9)	1.1			MHz
Start Convert Pulse Width (Notes 10, 11)	50			nsec
Delay Falling Edge of Start to Status = "1" (Note 11)		45		nsec
Delay Falling Edge of Start to Previous Output Data Invalid (Note 11)		750		nsec
Delay Falling Edge of Start to Falling Edge of T/H Control		750	780	nsec
Delay Falling Edge of Status to Output Data Valid (Note 11)			0	nsec
Delay Falling Edge of Enable to Output Data Valid (Note 11)			50	nsec
REFERENCE OUTPUT				
Internal Reference (Note 11): Voltage		+5.000		Volts
Accuracy		±2		%
Drift		±10		ppm/°C
External Current		5		μA

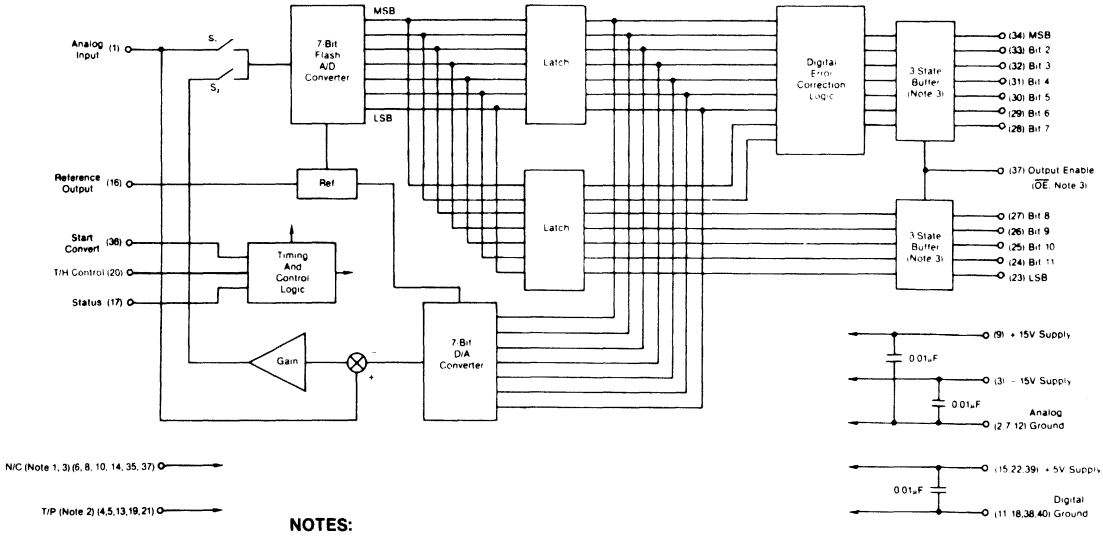
POWER SUPPLY REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15	+15.43	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Note 13): +15V Supply	−50			dB
−15V Supply	−50			dB
+5V Supply	−50			dB
Current Drain: +15V Supply		+41	+50	mA
−15V Supply		−83	−90	mA
+5V Supply		+150	+165	mA
Power Consumption		2635	2925	mW

SPECIFICATION NOTES:

1. Unless otherwise indicated, listed specifications apply for all MN5245, MN5245A, MN5246 and MN5246A models. Drift specifications apply over each device's specified temperature range as selected by part number suffix.
2. One LS TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.4mA with a logic "0" applied.
3. FSR = Full Scale Range. For both the MN5245 and MN5246, FSR = 5 volts. For a 12-bit converter, 1LSB = 0.024% FSR.
4. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 to 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
5. Unipolar offset error is defined for the MN5245 and MN5245A as the difference between the actual and ideal input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition occurs. The ideal value at which this transition should occur is + ½LSB. See Digital Output Coding.
6. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs for the MN5246 and MN5246A. The ideal value at which this transition should occur is − ½LSB. See Digital Output Coding.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000. Initial gain error is adjustable to zero with an external potentiometer.
8. See Output Coding table for details.
9. Conversion time is defined as the width of the converter's Status output pulse. The combination of 50nsec Start Convert pulses and 850nsec Status pulses permits minimum 1.1MHz conversion rates. See Timing Diagram.
10. Actual conversion process is initiated on the falling edge of the Start Convert signal. See Timing diagram.
11. These parameters are listed for reference only and are not tested.
12. Digital outputs include Data Bits (pins 23-34), Status (pin 17), and T/H control (pin 20). Specified drive capability is the equivalent of 5 LS TTL loads minimum.
13. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

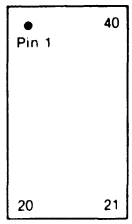
BLOCK DIAGRAM



NOTES:

1. "No Connects" (N/C) are not connected to internal circuitry.
2. "Test Points" (T/P) are connected to internal circuitry and should not be connected to externally.
3. 3-state output buffers included only in "A" models. For standard MN5245 and MN5246, pin 37 is a N/C.

PIN DESIGNATIONS



1	Analog Input	40	Digital Ground
2	Analog Ground	39	+ 5V Supply
3	– 15V Supply	38	Digital Ground
4	Test Point	37	N/C ($\overline{OE}$)
5	Test Point	36	Start Convert
6	N/C	35	N/C
7	Analog Ground	34	Bit 1 (MSB)
8	N/C	33	Bit 2
9	+ 15V Supply	32	Bit 3
10	N/C	31	Bit 4
11	Digital Ground	30	Bit 5
12	Analog Ground	29	Bit 6
13	Test Point	28	Bit 7
14	N/C	27	Bit 8
15	+ 5V Supply	26	Bit 9
16	Reference Output	25	Bit 10
17	Status (E.O.C.)	24	Bit 11
18	Digital Ground	23	Bit 12 (LSB)
19	Test Point	22	+ 5V Supply
20	T/H Control	21	Test Point

NOTES:

1. "No Connects" (N/C) are not connected to internal circuitry.
2. "Test Points" (T/P) are connected to internal circuitry and should not be connected to externally.
3. 3-state output buffers included only in "A" models. For standard MN5245 and MN5246, pin 37 is a N/C.

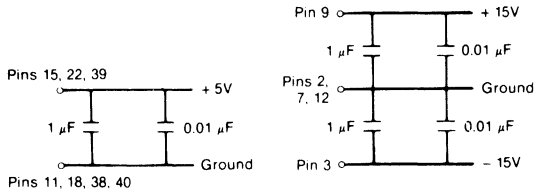
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and performance from the MN5245 and MN5246. Analog Ground pins (pins 2, 7, and 12) are not connected internally to Digital Ground pins (pins 11, 18, 38 and 40). All ground pins should be tied together as close to the unit as possible and connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

A 0.1μF capacitor should be connected from Reference Output (pin 16) to system analog ground.

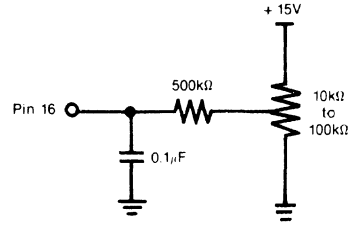


POWER SUPPLY DECOUPLING

STATUS OUTPUT/DATA VALID — The Status or End of Conversion (E.O.C.) output is set to logic "1" by the falling edge of the Start Convert; remains high during the conversion; and is set to a logic "0" by the rising edge of the T/H Control output, signaling that the conversion is complete. Digital output data is valid on the falling edge of Status and remains valid until the next falling edge of T/H Control (approximately 750nsec after Start Convert goes low initiating the next conversion). It is important to note that the falling edge of the T/H Control indicates the end of the "analog-processing" portion of the A/D conversion and the beginning of the "digital-processing" portion. Output data becomes **invalid** on the falling edge of the T/H Control signal, and it is not recommended that this edge be used to clock data away from the MN5245/46. When making successive conversions, any of the edges occuring during the beginning of the data-valid period (fall of Status, falling edge of the next Start Convert, rising edge of Status, etc.) are better suited for this purpose. Also, output data can be enabled (MN5245A/MN5246A) during this data-valid period by bringing Output Enable ($\overline{OE}$, pin 37) low. The delay from the falling edge of Output Enable to output data valid is 50nsec maximum.

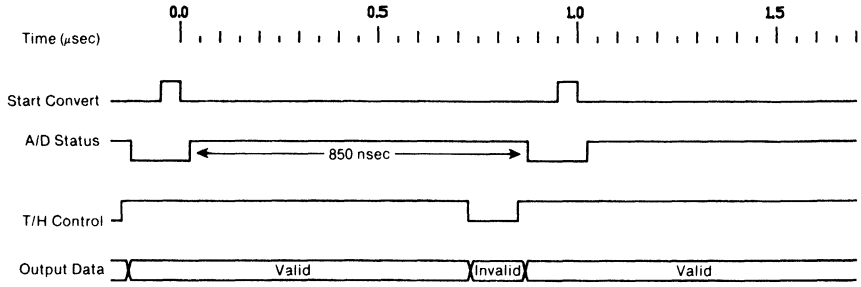
REFERENCE IN/OUT, GAIN ADJUST—Pin 16 on MN5245/MN5246 type A/D converters serves a unique function. The devices' internal + 5V ± 2% reference is brought out at this point and can be used to drive external loads. If used for this purpose, pin 16 should be buffered with a FET-input device as drawing more than 5μA from the internal reference will affect MN5245/MN5246 accuracy and linearity. Pin 16 can also be used as a Reference In Point if it is necessary to operate MN5245/MN5246 from an external reference. An application requiring an external reference might be one in which it is necessary to have a number of devices operate from the same reference to track each other in changing temperatures. The applied reference should be + 5V ± 250mV.

Pin 16 also functions as the gain-adjust point for MN5245/MN5246 A/D converters. Gain adjustment is accomplished using a 10kΩ to 100kΩ trimming potentiometer and a 500kΩ series resistor as shown below. The series resistor can be ± 20% carbon composition or better. The multiturn potentiometer should have a TCR of 100ppm/°C or less to minimize drift with temperature. Gain adjusting is normally accomplished by applying the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition is ideally supposed to take place and adjusting the pot until the transition is observed.



Gain Adjust Range = ± 0.2% FSR

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. Minimum Start Convert pulse width is 50nsec, and Start Convert must remain low during conversion.
2. Status rises to a "1" typically 45nsec after the falling edge of Start Convert.
3. Digital output data from the previous conversion is valid typically 750nsec after the falling edge of Start and 705nsec after the rising edge of Status.
4. Digital output data is valid on the falling edge of Status.
5. For MN5245A or MN5246A, output data becomes valid a maximum of 50nsec after Output Enable (pin 37) is brought low.
6. The falling edge of T/H Control occurs 780nsec maximum after the falling edge of Start Convert.

DIGITAL OUTPUT CODING

Analog Input		Digital Output
MN5245, MN5245A	MN5246, MN5246A	MSB LSB
+5.0000	+2.5000	1111 1111 1111
+4.9982	+2.4982	1111 1111 111Ø*
+2.5006	+0.0006	1000 0000 000Ø*
+2.4994	−0.0006	ØØØØ ØØØØ ØØØØ*
+2.4982	−0.0018	0111 1111 111Ø*
+0.0006	−2.4994	0000 0000 000Ø*
0.0000	−2.5000	0000 0000 0000

NOTES

1. For a 12-bit converter with a 5 volt FSR, 1LSB = 1.22mV.
2. Coding is straight binary for the unipolar 5V range and offset binary for the bipolar 2.5V range.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the MN5245 or MN5245A, the transition from output code 1111 1111 1111 to output code 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of +4.9982V (+F.S. − 1½LSB). Subsequently, any voltage greater than +4.9982V will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 (or vice versa) will ideally occur at an input of +2.4994V. The 0000 0000 0000 to 0000 0000 0001 transition will occur at +0.0006V. An input more negative than this level will give all "0's".

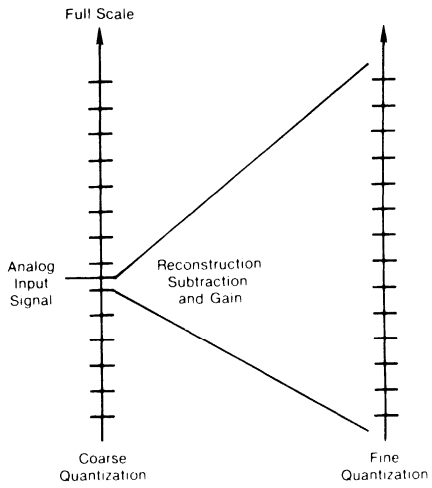
DESCRIPTION OF OPERATION — MN5245 and MN5246 are multi-stage (two-step) A/D converters. They employ the Micro Networks Serial-Parallel conversion technique (sometimes referred to as the subranging technique) with digital error correction. The technique uses two 7-bit flash A/D converters (actually a single 7-bit flash coverter is used twice) in a configuration that yields a resolution (12 bits) that is beyond the practical limits of what can be achieved in a single "high-resolution" flash coverter. The technique trades off speed against resolution and, in the case of MN5245/MN5246, against size, as putting the device in a single DIP package necessitates additional considerations.

As shown in the block diagram, the main function blocks in MN5245/MN5246 type A/D's may be partitioned into analog functions (including input switching network (S_1 and S_2); 7-bit, high-speed, flash-type A/D converter; precision, 7-bit, high-speed D/A converter; high-speed difference amplifier with gain; precision reference; and timing circuits) and digital functions (including 2 sets of latches; the digital-error-correction logic; and the 3-state output buffers). The circuit functions in the following manner.

The falling edge of the Start Convert command (50nsec minimum pulse width): drives the Status output to a logic "1" (approximate 45nsec delay) indicating that a conversion is in process; switches S_1 on and S_2 off connecting the analog input signal directly to the 7-bit flash converter; and initiates a series of timing pulses that will control the assorted operations of the converter during the conversion cycle. At this point, digital output data from the previous conversion is still valid, and it remains so until approximately 750nsec after the falling edge of Start.

After a period of time allowing the flash-converter input circuitry to settle, the first internally generated timing pulse initiates a flash conversion and subsequently latches the 7-bit output into the first latch. The input signal has now been coarsely quantized into $2^7 = 128$ levels and the result, after being stored in the first latch, is simultaneously directed to the 7-bit D/A converter which reconstructs the signal into an analog equivalent.

This digitized and subsequently reconstructed signal is subtracted from the original analog input yielding the difference between the first 7-bit conversion and the input signal. As depicted below, the difference signal is then amplified and itself digitized by being fed back into the 7-bit flash converter via the closing of S_2 and the opening of S_1. The result of this conversion is now latched into the second latch.



One of the tradeoffs that enable MN5245 and MN5246 to be built in DIP's was the decision to use a single 7-bit flash converter and cycle through it twice rather than use 2 flash A/D's. Had 2 A/D's been used, the amplified difference signal would be routed to the second A/D at this point, liberating the first A/D to begin a new conversion cycle and eliminating the S_1S_2 switching network and its associated settling times.

Returning to the conversion process, one might conclude that digitizing the amplified difference signal would constitute the end of a conversion as the 5 most significant bits (MSB's) from the second 7-bit conversion could simply be added to the 7 bits from the first conversion to give a full, accurate, 12-bit output. However, the realities of implementing the conversion technique make such an obvious conclusion a wrong one.

The major sources of error in the technique occur in the first 7-bit conversion and result from the fact that such a conversion is only 7, or at most, 8-bits accurate. Twelve-bit accuracy would be required at this point in order for one to simply add output bits together to get an accurate result. Such 7-bit resolution, 12-bit accurate flash converters do not exist, and if they did, would probably be considerably slower than required to make a 850nsec 12-bit conversion. The problem is overcome using the technique of digital error correction. In this technique, the first 7-bit A/D conversion is allowed to have errors (as long as they are within some known bounded range), and these errors are corrected for in the later portion of the conversion cycle. The process proceeds as follows: Recall that if the 7-bit converter had 12-bit accuracy one would only need 5 bits from the second conversion to produce a 12-bit result. By digitizing the difference signal to a level that is four times greater than theoretically required (7 bits compared to 5 bits) and comparing the result to theoretically anticipated limits, one can deduce what the inaccuracies were in the first 7-bit conversion. This is what MN5245/MN5246's digital-error-correction circuitry accomplishes. Using combinatorial logic and lookup tables, the error-correction circuitry assesses the 2 most significant bits of the digitized difference signal; decides how accurate the first 7-bit conversion was; and adds or subtracts bits to or from the first 7-bit output as necessary. Once the first 7 bits have been corrected, they are simply added to the 5 remaining bits of the second conversion to produce the full 12-bit output. This is why in the Block Diagram, the two MSB's from the second latch are routed to the digital-error-correction logic and the 5 LSB's are directed to the output.

It should be obvious, following the above discussion, that MN5245/MN5246 A/D's normally require the use of track-hold amplifiers (T/H's) to hold the input signal relatively constant during the first conversion and the subsequent subtraction, gain and second digitization cycles. The output droop rate of the track-hold should be slow enough so the held signal does not change more than $\pm$ ½LSB ($\pm$0.61mV) during the conversion period. Micro Networks MN375 and MN376 both do the job well. A consideration that may enable designers to improve throughput when using MN5245 and MN5246 with T/H's is that an accurate input signal is no longer required after the second 7-bit A/D conversion has been made. During the interval between that conversion and the point at which Status drops to a "0" indicating that the conversion is complete, the digital-error-correction logic is performing its function and the analog input circuitry is dormant. This period is called converter "slack time" and is typically 100nsec for MN5245/MN5246 devices. The T/H amplifier can be put back into its tracking (signal acquisition) mode at this point rather than waiting until the falling edge of Status by utilizing the T/H control output (pin 20) described on the following pages.

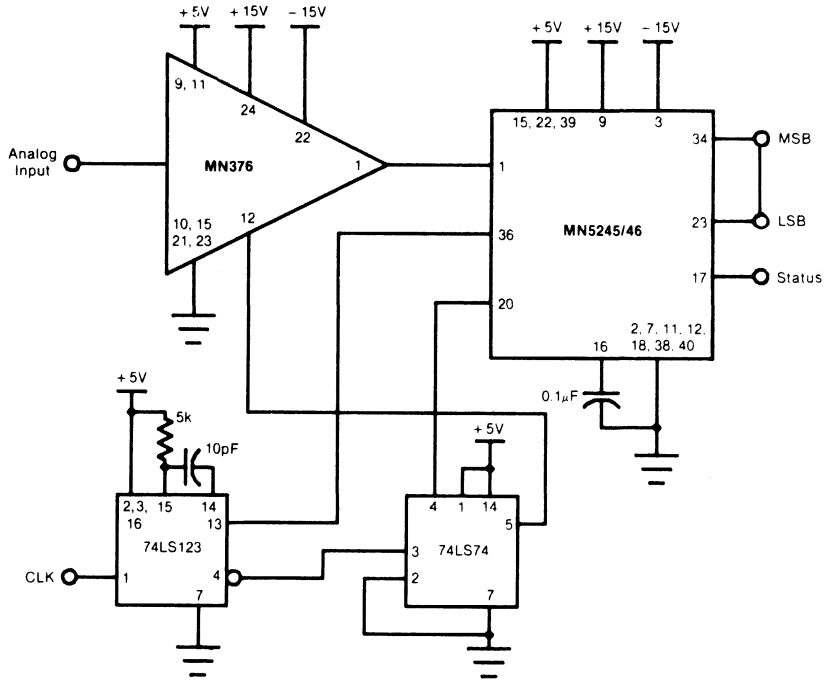
MN5245/5246 — MN376 1MHz Sampling System

A/D converters that utilize the subranging (serial-parallel) conversion architecture may be relatively limited in their ability to accurately convert rapidly changing dynamic input signals. In other words, these high-throughput digitizers often have analog input bandwidth limitations. In situations in which both high-throughput and high-bandwidth digitizing is required, a track-hold (T/H) amplifier can be used to overcome the A/D's inherent limitations. The T/H has the ability to quickly capture rapidly changing analog signals and hold them constant while the A/D performs its conversion. The MN376 High Speed T/H Amplifier (200nsec maximum acquisition time) has been designed specifically for this type of usage with MN5245/46. The following application information describes how to configure MN376 and MN5245/46 to create a T/H-A/D pair that is capable of sampling and digitizing at rates in excess of 1MHz and has a full-power input bandwidth greater than 500kHz. Interconnect and timing diagrams are shown below, and the basics of the application are applicable to most high-speed T/H-A/D combinations.

The T/H Control pulse provided on pin 20 of the MN5245/46 is the key to this application. The falling edge of this output signals the end of the "analog-processing" portion of the A/D conversion and consequently, the end of the requirement for a constant-value analog input signal. Immediately thereafter, the T/H can be removed from its "hold" state and permitted to acquire a new input sample, i.e., the T/H can be put into the acquisition (track) mode. The T/H Control line remains low for approximately 100nsec (during the "digital-processing" portion of the conversion) and then returns high triggering the fall of the A/D's Status output. The falling edge of Status signals the end of the conversion and the validity of digital output data (see Description of Operation if necessary). At the beginning of the next conversion, the T/H is driven from the track (signal-acquisition) mode to the hold mode "freezing" the input signal permitting an accurate conversion to proceed.

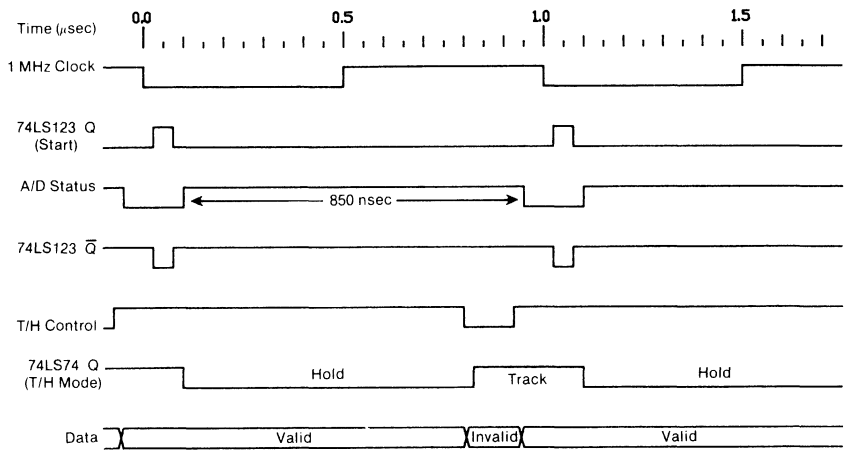
Maximum throughput is achieved in this application because the T/H is driven into the acquisition mode for its next sample prior to the completion of the ongoing A/D conversion and remains in the acquisition mode while the A/D is being "set up" for its next conversion. This "overlapping" allows every nanosecond to be utilized.

APPLICATION SCHEMATIC



MN5245/46

APPLICATION TIMING DIAGRAM



As previously stated, the MN376-MN5245/46 T/H-A/D combination is capable of sampling and digitizing at rates in excess of 1MHz, with the actual rate determined by the frequency of the externally applied clock. See interconnect and timing diagrams. The falling edge of the external clock triggers the 74LS123 one-shot, and the clock can have any duty cycle as long as it has a minimum positive pulse width of 50nsec to accommodate the setup-time requirement of the one-shot. The Q output of the one shot provides a 50nsec start-convert signal to the MN5245/46; while the rising edge of the $\overline{Q}$ output simultaneously resets the 74LS74 flip-flop. The Q output of the flip-flop controls the operational mode of the T/H (utilizing the T/H's $\overline{hold}$ input), and at the beginning of a sample/convert cycle, the flip-flop output going to a logic "0" drives the T/H into the hold mode. This "freezes" (holds) the input signal that the T/H has been acquiring/tracking up until this time.

It is unnecessary to have the 74LS123 one-shot in this application if the externally applied clock can be made to be a series of 50nsec-wide positive pulses occurring at a 1MHz rate. In other words, if the clock can be made to look like the output of the one-shot in our timing diagram, it is unnecessary to have the one-shot. The clock can drive the MN5245/46 directly, and it can be inverted to drive the 74LS74.

The falling edge of the MN5245/46's applied start-convert signal (the Q output of the one-shot) initiates the A/D conversion process and drives the converter's status line high. The "first-pass" conversion of MN5245/46's internal 7-bit flash A/D does not occur until approximately 190nsec after the falling edge of the start-convert signal. This delay allows time for the T/H's track-to-hold output transient to fully settle before the 7-bit flash makes it first conversion. The MN376 specifies a maximum transient settling time (to ± 1mV) of 100nsec. The T/H remains in the hold mode while the A/D conversion continues, and the T/H's excellent output-droop performance guarantees that the A/D's input will not change more than 5μV during the conversion window. At approximately 700nsec into the conversion, the T/H Control line (pin 20) goes low signaling the end of the analog-processing portion of the conversion. This action asynchronously sets the flip-flop output to a logic "1", which in turn drives the MN376 T/H back into the signal-acquisition (track) mode. Approximately 100nsec later, the rising edge of the pin 20 signal triggers the fall of the Status line indicating that the conversion is complete and that output data is now valid. The Status pulse is guaranteed not be wider than 850nsec, and neither the rising edge of the T/H Control signal (pin 20) nor the falling edge of the Status signal (pin 17) will affect the operational mode of the T/H. It remains in the track mode through both events.

When making repetitive conversions, the T/H Control signal permits the MN376 to acquire and track new samples of the input signal during the "slack time" of the present conversion. When the T/H Control signal is used in this manner in a 1MHz application, a minimum of 240nsec is allocated for the MN376 acquisition-time requirements. This more than accommodates the MN376's maximum acquisition time of 200nsec (10V step acquired to ± 1mV or 5V step acquired to ± ½mV).

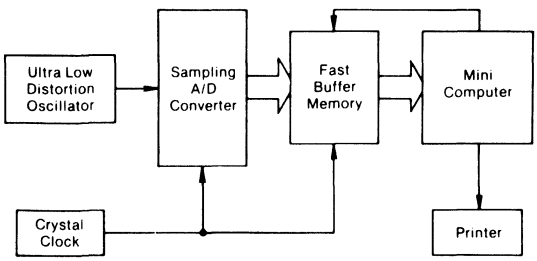
MN5245/5246 has a latched output, and output data from a conversion typically remains valid into the next conversion for 750nsec beyond the falling edge of the next start-convert signal. Output data becomes **invalid** on the falling edge of the T/H Control signal, and it is not recommended that this edge be used to clock data away from MN5245/46. Any of the edges occurring during the beginning of the data-valid period (clock edge, one-shot outputs, rising edge of Status, etc.) are better suited for this purpose.

This T/H-A/D pair is guaranteed to meet all its performance specs while running at a 1MHz sampling rate. The slew rate (300V/μsec), full-power bandwidth and aperture jitter (±25psec) of the T/H are good enough to accurately track and sample full-scale (5V), 500kHz, input signals. Consequently, this T/H-A/D pair can accurately sample and digitize (at a 1MHz rate) full-scale input signals with frequency content (bandwidths) up to 500kHz.

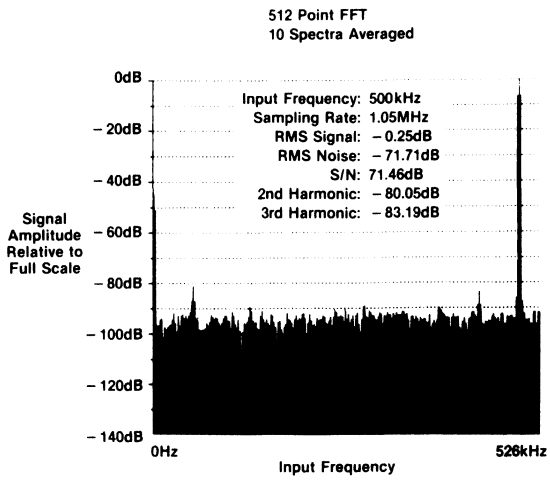
This means that the Nyquist criterion of sampling 2 times per peroid (sample/digitizing rate equal to at least 2 times the signal frequency) is satisfied, and the MN5245/46 pair is truly a Nyquist A/D converter. Evaluating it as such is no longer a difficult task.

The availability of low-cost, p.c. based, digital-signal-processing (D.S.P.) technology has made it relatively easy to now perform dynamic, frequency-domain evaluations of sampling A/D converters. Prior to this, it was virtually impossible to review the listed specifications for A/D converters and/or T/H amplifiers and make a valid determination of the true dynamic capabilities of either device. This inconclusiveness was due primarily to the fact that virtually all traditional A/D converter specs (integral linearity, differential linearity, accuracy, gain, etc.) are tested statically and cannot necessarily be extrapolated to dynamic situations. It was also due to the fact that appropriate dynamic T/H specs either were similarly static (linearity); did not exist (harmonic distortion); or were too difficult to understand (aperture jitter).

In the dynamic tests that we now perform at Micro Networks, the MN376-MN5256/46 T/H-A/D combination is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics −90dB) is used to generate a pure, full-scale, 500kHz sine wave that MN376-MN5245/46 samples and digitizes at a 1MHz rate. These conditions (signal period = 2μsec, sampling interval = 1μsec) achieve the Nyquist sampling criterion (at least 2 samples per signal cycle). A total of 512 sample-and-convert operations are performed, and the digital-output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are made from the spectrum. A functional block diagram of the test setup and a sample spectrum appear below.



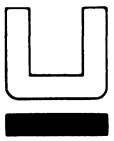
Frequency-Domain Testing of A/D Converters



The spectrum above is the real portion (imaginary portions of spectra are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate (526kHz in this case). The horizontal axis is divided into 256 frequency bins, each with a width of 2.05kHz. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). The sample spectrum above is the result of averaging 10 512-point FFT's run on data taken from an MN376-MN5246 operating on its ±2.5V bipolar input range with a full scale input sine wave (v(t) = 2.5sinwt) at a frequency of 500kHz. In the spectrum, the full-scale input signal appears at 500kHz at a level of −0.25dB. Full-scale r.m.s. signals do not appear at −3dB levels because our FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the MN376-MN5246 combined with that of the signal generator and test fixture. A second harmonic distortion component is aliased back into the spectrum and appears at 52kHz at a level of −80.30dB (−80.05dB relative to the signal level). The third harmonic is also aliased into the spectrum and appears at 448kHz at a level of −83.44dB (−83.19dB relative to the signal level). The fourth and fifth harmonics, if they were present, would occur at 104kHz and 396kHz respectively, however, due to their small amplitudes they are buried in the broadband noise.

Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level ot the strongest harmonic or spurious (nonharmonic) signal in the spectrum. In the sample spectrum above, the strongest harmonic is the second. It appears at a level of −80.30dB, and the signal to harmonics ratio is equal to −80.05dB. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to rms noise. For the above spectrum, the normalized rms signal level is −0.25dB; the rms noise level is −71.71dB; and the SNR is 71.46dB.



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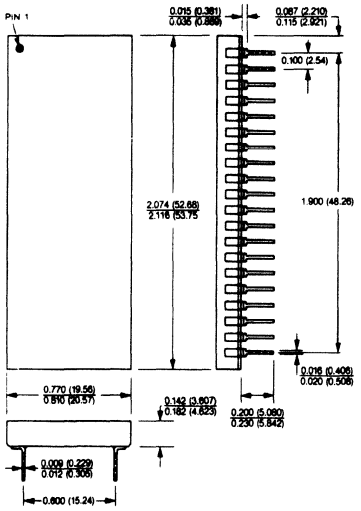
MN5249

400nsec, 12-Bit
A/D CONVERTER

FEATURES

- 400nsec Maximum Conversion Time
- Guaranteed 2.5MHz Conversion Rate
- 2MHz Sampling Rate When Used with MN376 T/H Amplifier
- No Missing Codes Guaranteed Ov Temperature
- Small 40-Pin DIP
- ±2.5 Watt Power Consumption
- TTL Compatible
- 3-State Output Buffer
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

40 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5249 is a 400nsec, 12-bit A/D converter that guarantees 2.5MHz conversion rates. When used with MN376 high-speed T/H amplifiers, these A/D's can be configured to form bonafide, 2MHz, sample-and-convert systems that can digitize full-scale (5V) input signals with bandwidths up to 1MHz. These systems typically achieve signal-to-noise ratios of 70dB with harmonics down more than −80dB while digitizing 1MHz signals at the Nyquist rate.

Packaged in a standard, 40-pin, double-wide, hermetically sealed, ceramic dual-in-line, MN5249 offers an outstanding combination of resolution, speed, size and cost. This TTL compatible device achieves its sub-500nsec conversion speed using the digitally corrected subranging (serial-parallel) A/D conversion technique. Recent advances in monolithic flash A/D converters and monolithic DAC's and improvements in digital error correcting techniques have enabled us to reduce chip count over previous designs while improving performance.

MN5249 has a ±2.5V input range and a user-optional, 3-state output buffer to facilitate μP interfacing. A "T/H Control" output line is provided with all the necessary delays for direct T/H control. All models guarantee ±0.024% FSR integral linearity and "no missing codes" for 12 bits over their entire specified temperature range.

MN5249 is an ideal design solution for high-speed digitizing applications in which speed, accuracy, size and reliability are paramount considerations. Typical applications include spectrum, vibration, waveform and transient analyzers; radar, sonar and video digitizers; medical imaging equipment; digital filters; and multiplexed or simultaneous-sampling data acquisition systems.

The MN5249H/B is available with Environmental Stress Screening while the MN5249H/B CH is screened in accordance with MIL-H-38534. Contact the factory for availability of CH device types.

April 1989

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324 Clark St., Worcester, MA 01606 (508) 852-5400

MN5249 400nsec 12-Bit A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN5249	0°C to +70°C (case)
MN5249E, MN5249E/B	−25°C to +85°C (case)
MN5249H, MN5249H/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 17)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 25)	+0.5 to −18 Volts
+5V Supply (+Vdd, Pins 5,29,40)	−0.5 to +7 Volts
−5.2V Supply (−Vdd, Pin 14)	0 to −7 Volts
Digital Inputs (Pins 7, 12)	−0.5 to +5.5 Volts
Analog Input (Pin 22)	−3.5 to +3.5 Volts

ORDERING INFORMATION

PART NUMBER ——— **MN5249 H/B CH**

Standard Part is specified for 0°C to +70°C operation.
Add "E" suffix for specified −25°C to +85°C (case) operation.
Add "H" suffix for specified −55°C to +125°C (case) operation.
Add "/B" to "H" devices for Environmental Stress Screening.
Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.
Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V, −Vdd = −5.2V unless otherwise indicated)

ANALOG INPUTS	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range		±2.5		Volts
Input Impedance (Note 1)		500//10		Ω//pF
DIGITAL INPUTS (Start Convert, OE)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.7)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−0.4	mA
TRANSFER CHARACTERISTICS (Note 2)				
Integral Linearity Error: Initial (+25°C)		±½	±1	LSB
Over Temperature (Note 3)		±½	±1	LSB
12-Bit No Missing Codes		Guaranteed Over Temperature		
Full Scale Absolute Accuracy Error (Note 4): Initial (+25°C)		±0.05	±0.15	%FSR
Over Temperature (Note 3)		±0.1	±0.3	%FSR
Bipolar Zero Error (Note 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 3)		±0.1	±0.2	%FSR
Drift (Note 3)		±10	±25	ppm of FSR/°C
Gain Error (Note 6): Initial (+25°C)		±0.05	±0.1	%
Over Temperature (Note 3)		±0.1	±0.3	%
Drift (Note 3)		±20	±40	ppm/°C
DIGITAL OUTPUTS (Parallel, OR/UR, T/H Control, Status, $\overline{MSB}$)				
Output Coding (Note 7)		Offset Binary		
Output Logic Levels: Logic "1" ($I_{SOURCE} \leq 100\mu A$)	+2.7			Volts
Logic "0" ($I_{SINK} \leq 2mA$)			+0.5	Volts
Leakage (Bit 1 – Bit 12) in High-Z State: Logic "1" (V_{OH} = +2.7V)			+10	μA
Logic "0" (V_{OL} = +0.4V)			−10	μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 8)		375	400	nsec
Conversion Rate (Note 8)	2.5	2.7		MHz
Start Convert Pulse Width (Notes 1, 9)	50			nsec
Delay Falling Edge of Start to Status = "1" (Note 1)		45		nsec
Delay Falling Edge of Start to Previous Output Data Invalid (Note 1)		280		nsec
Delay Falling Edge of Start to Falling Edge of T/H Control		280	300	nsec
Delay Falling Edge of Status to Output Data Valid (Note 1)			0	nsec
Delay Falling Edge of Enable to Output Data Valid (Note 1)			50	nsec
REFERENCE OUTPUT				
Internal Reference (Note 1): Voltage		+5		Volts
Accuracy		±2		%
Drift		±10		ppm/°C
External Current		5		μA

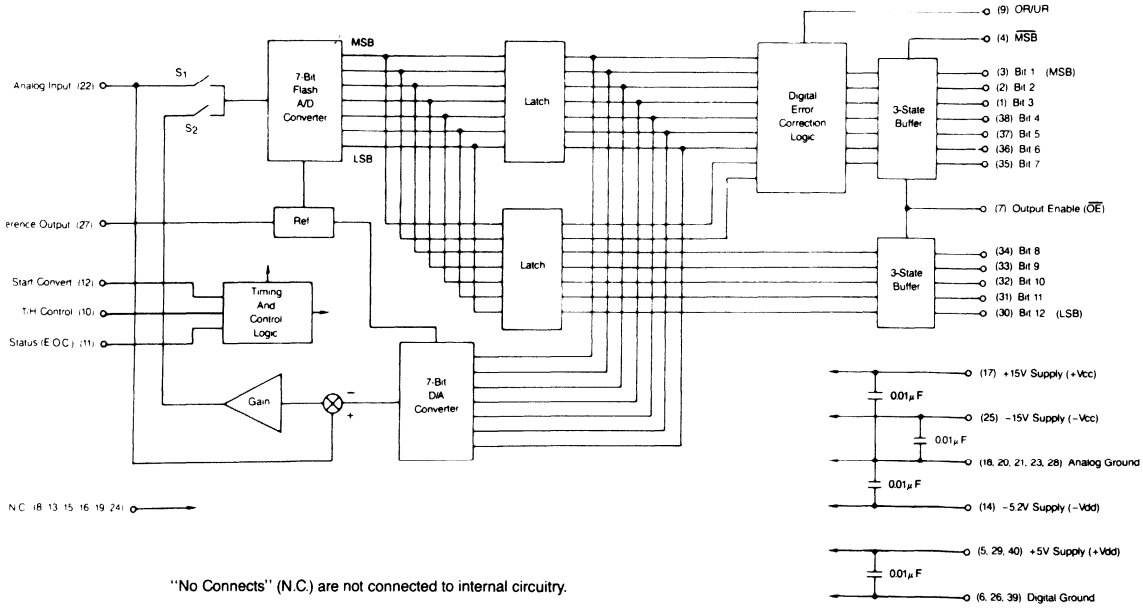
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
−5.2V Supply	−5	−5.2	−5.4	Volts
Power Supply Rejection (Note 10): +15V Supply	−50	−72		dB
−15V Supply	−50	−66		dB
+5V Supply	−50	−68		dB
−5.2V Supply	−50	−57		dB
Current Drain: +15V Supply		+40	+50	mA
−15V Supply		−64	−75	mA
+5V Supply		+200	+250	mA
−5.2V Supply		−50	+60	mA
Power Consumption		2.82	3.44	Watts

PECIFICATION NOTES:

1. These parameters are listed for reference only and are not tested.
2. FSR=full scale range, and for the MN5249, FSR=5 Volts. For a 12-bit converter, 1LSB=0.024% FSR.
3. Listed specifications apply over the 0°C to +70°C (case) temperature range for standard product; over the −25°C to +85°C (case) temperature range for MN5249E and MN5249E/B; and over the −55°C to +125°C (case) temperature range for MN5249H and MN5249H/B.
4. Full scale accuracy specifications apply at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 and from 0000 0000 0000 to 0000 0000 0001. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
5. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
6. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000. Initial gain error is adjustable to zero with an external potentiometer.
7. See Output Coding table for details.
8. Conversion time is measured from the falling edge of Start Convert to the falling edge of Status (E.O.C.). See Timing Diagram.
9. The rising edge of Start Convert resets internal timing circuits ensuring that the first conversion after "powerup" produces valid output data. The falling edge of Start Convert actually initiates the conversion process.
10. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

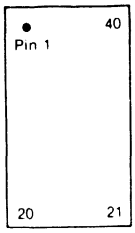
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

LOCK DIAGRAM



"No Connects" (N.C.) are not connected to internal circuitry.

PIN DESIGNATIONS



1	Bit 3	40	+5V Supply (+Vdd)
2	Bit 2	39	Digital Ground
3	Bit 1 (MSB)	38	Bit 4
4	$\overline{\text{MSB}}$	37	Bit 5
5	+5V Supply (+Vdd)	36	Bit 6
6	Digital Ground	35	Bit 7
7	Output Enable ($\overline{\text{OE}}$)	34	Bit 8
8	N.C.	33	Bit 9
9	Over/Underrange (OR/UR)	32	Bit 10
10	T/H Control	31	Bit 11
11	Status (E.O.C.)	30	Bit 12 (LSB)
12	Start Convert	29	+5V Supply (+Vdd)
13	N.C.	28	Analog Ground
14	−5.2V Supply (−Vdd)	27	Reference Output (+5V)
15	N.C.	26	Digital Ground
16	N.C.	25	−15V Supply (−Vcc)
17	+15V Supply (+Vcc)	24	N.C.
18	Analog Ground	23	Analog Ground
19	N.C.	22	Analog Input
20	Analog Ground	21	Analog Ground

NOTES:

1. "No Connects" (N.C.) are not connected to internal circuitry.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—MN5249 is a multistage (two-step) A/D converter. It employs the Micro Networks Serial-Parallel conversion technique (sometimes referred to as the subranging technique) with digital error correction. The technique uses two 7-bit flash A/D converters (actually a single 7-bit flash converter is used twice) in a configuration that yields a resolution (12 bits) that is beyond the practical limits of what can be achieved in a single high-resolution flash converter. The technique trades off speed against resolution, and in the case of MN5249 against size, as putting the device in a single DIP package necessitates additional considerations. For a detailed discussion of the Serial-Parallel conversion technique and digital error correction, please refer to the MN5245/5246 data sheet.

Start Convert must be a positive pulse with a minimum pulse width of 50nsec (100nsec maximum if continuously converting at maximum conversion rate) and must remain low during the conversion. The rising edge of Start Convert resets the timing logic ensuring that all timing pulses are set to the proper state and that the first conversion following "power on" produces valid digital output data. The falling edge of Start Convert initiates the conversion setting T/H Control and Status (E.O.C.) to logic "1's". The T/H Control remains a logic "1" for 300nsec maximum after the falling edge of Start Convert and returns to a logic "0" signaling that the "analog-processing" portion of the conversion is complete and that a constant-value analog input signal is no longer required. Status remains a logic "1" for 400nsec maximum after the falling edge of Start Convert. Status returning low, signifies that the conversion process is complete and that parallel output data is valid.

The T/H Control signal enables designers to achieve maximum sampling rates from T/H-A/D pairs (MN376-MN5249 for example) by allowing the T/H to acquire the next analog voltage to be converted during the digital error correction process rather than waiting until the fall of Status.

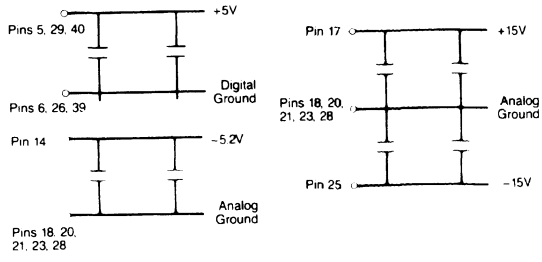
Valid parallel output data is available on the falling edge of Status and remains valid during the next conversion for 280nsec (typ) after the next falling edge of Start Convert. See Timing Diagram. This allows the use of rising and falling edges of either Start Convert or Status for latching output data.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and performance from the MN5249. Analog Ground (pins 18, 20, 21, 23, 28) is not connected internally to Digital Ground (pins 6, 26, 39). All ground pins should be tied together as close to the unit as possible and connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

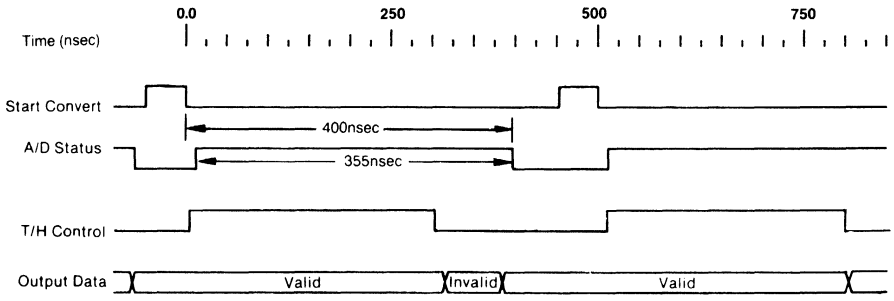
Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

A 0.1μF capacitor should be connected from Reference Output (pin 27) to system analog ground.



POWER SUPPLY DECOUPLING

TIMING DIAGRAM

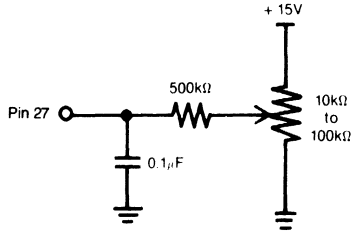


TIMING DIAGRAM NOTES:

1. Minimum start convert pulse width is 50nsec. The rising edge of start convert resets internal timing circuits ensuring that T/H Control (pin 10) is set to a logic "0" and that the first conversion made upon "powerup" is valid. The falling edge of Start Convert initiates the conversion, and Start Convert must remain low for 350nsec minimum. See section labeled Start Convert.
2. Status rises to a "1" typically 45nsec after the falling edge of Start Convert.
3. Conversion time is defined as the time from the falling edge of Start Convert to the falling edge of Status and is specified as 400nsec maximum.
4. Digital output data from the previous conversion remains valid typically 280nsec after the falling edge of Start and 235nsec after the rising edge of Status.
5. Digital output data is valid on the falling edge of Status.
6. Output data is enabled and becomes valid a maximum of 50nsec after Output Enable ($\overline{OE}$, pin 7) is brought low. See section labeled Output Enable.
7. The falling edge of T/H Control occurs 300nsec maximum after the falling edge of Start Convert. See section labeled Start Convert.

REFERENCE IN/OUT, GAIN ADJUST—Pin 27 on MN5249 serves a unique function. The device's internal +5V ±2% reference is brought out at this point and can be used to drive external loads. If used for this purpose, pin 27 should be buffered with a FET-input device as drawing more than 5μA from the internal reference will affect MN5249 accuracy and linearity. Pin 27 can also be used as a Reference In point if it is necessary to operate MN5249 from an external reference. An application requiring an external reference might be one in which it is necessary to have a number of devices operate from the same reference in order to track each other in changing temperatures. The applied reference should be +5V ±250mV.

Pin 27 also functions as the gain-adjust point for MN5249. Gain adjustment is accomplished using a 10kΩ to 100kΩ trimming potentiometer and a 500kΩ series resistor as shown below. The series resistor can be ±20% carbon composition or better. The multiturn potentiometer should have a TCR of 100ppm/°C or less to minimize drift with temperature. Gain adjusting is normally accomplished by applying the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition is ideally supposed to take place and adjusting the pot until the transition is observed.



Gain Adjust Range = ±0.2% FSR

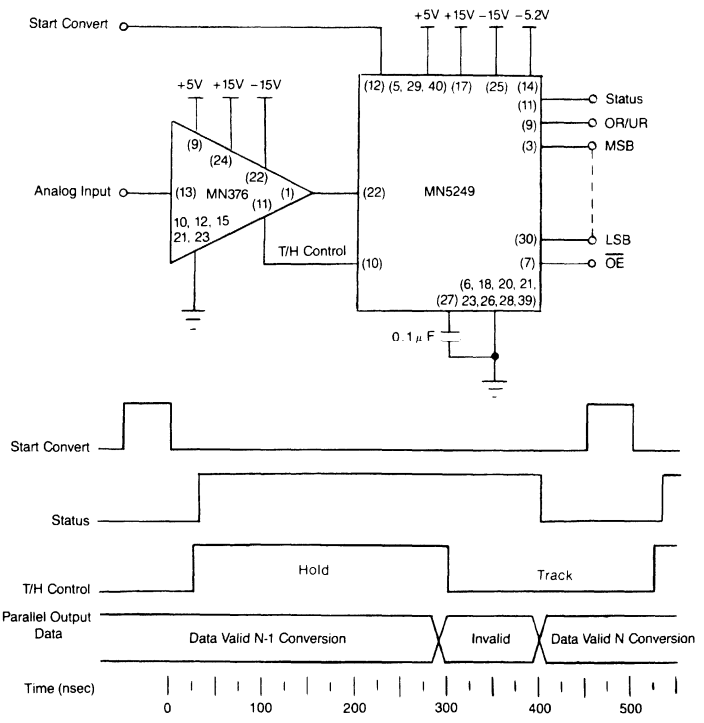
OVERRANGE/UNDERRANGE—An overrange/underrange output (OR/UR, pin 9) is provided and will be set to a logic "1" if an over or underrange condition exists. An input voltage 1 LSB more positive than the voltage at which the 1111 1111 1110 to 1111 1111 1111 transition occurs will set the OR/UR output to a logic "1" and parallel output bits will remain at all "1's". Similarly, an input voltage 1 LSB more negative than the voltage at which the 0000 0000 0001 to 0000 0000 0000 transition occurs will set the OR/UR output to a logic "1" and parallel output bits will remain at all "0's."

STATUS OUTPUT/DATA VALID—The Status or End of Conversion (E.O.C., pin 11) is set to a logic "1" by the falling edge of Start Convert; remains high during the conversion; and is set to a logic "0" when the conversion is complete. Digital output data is valid on the falling edge of Status and remains valid 280nsec after Start Convert goes low initiating the next conversion. When making successive conversions, any of the edges occurring during the beginning of the data-valid period (fall of Status, falling edge of the next Start Convert, rising edge of Status, etc.) are best suited for this purpose. Also, output data can be enabled during this data-valid period by bringing Output Enable ($\overline{OE}$, pin 7) low. The delay from the falling edge of $\overline{OE}$ to output data enabled is 50nsec maximum.

TRACK/HOLD CONTROL—The Track/Hold Control (T/H Control, pin 10) output is provided so that designers can achieve maximum throughput without additional glue chips when using a track-hold amplifier with MN5249. This output signal is set to a logic "1" by the falling edge of Start Convert and remains high during the "analog-processing" portion of the A/D's conversion cycle. It drops back low when the "digital-processing" portion of the conversion cycle commences, signaling that it is no longer necessary to maintain a stable analog input. Use of this signal allows a companion T/H amplifier to acquire and track the next analog input signal to be converted during the "digital-processing" portion of the present conversion. T/H Control remains low until the falling edge of the next Start Convert signal.

The diagram below shows the MN376, high-speed T/H amplifier and the MN5249 configured as a 2MHz, 12-bit sampling system. Maximum throughput is achieved because the MN376's T/H Command input is driven directly by the MN5249's T/H Control output.

MN376-MN5249 2MHz Sampling System



DIGITAL OUTPUT CODING

Analog Input	Digital Output
MN5249	MSB LSB
+2.5000	1111 1111 1111
+2.4982	1111 1111 111Ø*
+0.0006	1000 0000 000Ø*
−0.0006	ØØØØ ØØØØ ØØØØ*
−0.0018	0111 1111 111Ø*
−2.4994	0000 0000 000Ø*
−2.5000	0000 0000 0000

NOTES:

1. For a 12-bit converter with a 5 Volt FSR, 1LSB=1.22mV.
2. Coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

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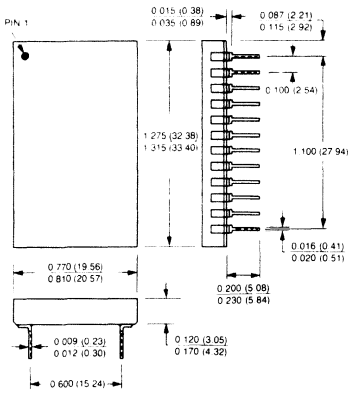
MN5250 Series

LOW-POWER
CMOS, 12-Bit
A/D CONVERTERS

FEATURES

- Low Power
  80mW Maximum
- Small 24-Pin DIP
- Linearity and
  No Missing Codes
  Guaranteed Over
  Temperature
- ±0.1% FSR Absolute Accuracy
- Totally Adjustment Free
  No Full-Scale or Zero
  Adjustments Necessary
- Full Mil Operation
  −55°C to +125°C
- MIL-H-38534 Screening
  Optional. MIL-STD-1772
  Qualified Facility

24 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN5250 Series devices are extremely low-power, 12-bit, successive approximation A/D converters in industry-standard, 24-pin, ceramic, dual-in-line packages. Power consumption is 80mW maximum.

Combining the advantages of highly stable thin-film resistors, functional laser trimming and hermetic packaging, the MN5250 Series offers designers the ultimate in convenience for high-resolution, low-power analog-to-digital conversion. All devices are supplied complete with internal reference, and no external trimming components or adjustments are necessary to meet published specifications.

Four input voltage rages are offered, and all units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature. All models of the MN5250 Series may be procured for operation over the full −55°C to +125°C military temperature range ("H" models) or the 0°C to +70°C commercial temperature range. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

The MN5250 Series is the ideal choice for designs requiring high resolution and low power consumption. Their small size, low power consumption and adjustment-free operation make them excellent selections for compact, highly reliable systems. Typical applications include remote-site seismological monitoring, precision portable instruments and high-accuracy industrial instrumentation.

May 1988

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MN5250 SERIES LOW-POWER CMOS 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
+12V Supply (Pin 15)	+18 Volts
−12V Supply (Pin 13)	−18 Volts
Logic Supply (+Vdd, Pin 2)	−0.5 to+16 Volts
Analog Input (Pin 14)	±25 Volts
Digital Inputs (Pins 1, 24)	−0.5 to +Vdd

ORDERING INFORMATION

PART NUMBER — MN525X H /B CH

Select MN5250, MN5251, MN5252, or MN5253.
Standard Part is specified for 0°C to +70°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" to "H" devices for Environmental Stress Screening.
Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±12V and +5V, unless otherwise specified).

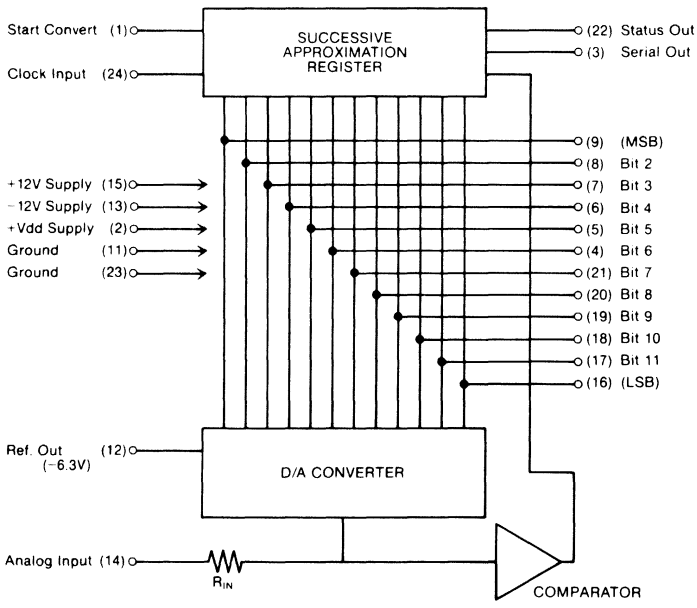
ANALOG INPUTS	+Vdd	MIN.	TYP.	MAX.	UNITS
Input Voltage Range (Input Impedance): MN5250 (50KΩ)			0 to −10		Volts
MN5251 (50KΩ)			− 5 to + 5		Volts
MN5252 (100KΩ)			−10 to +10		Volts
MN5253 (50KΩ)			0 to +10		Volts
DIGITAL INPUTS					
Logic Levels (Note 1): Logic "1"	+ 5V	3.5			Volts
	+12V	8.4			Volts
Logic "0"	+ 5V			1.5	Volts
	+12V			3.5	Volts
Loading: Input Current			10		pA
Input Capacitance (V_{IN}=0V)			5		pF
Start Convert Input: Pulse Width	+ 5V	750			nSec
	+12V	250			nSec
Setup Time Start High to Clock	+ 5V	300			nSec
	+12V	150			nSec
Clock Input: Frequency (Note 2)				71	KHz
Positive Pulse Width (Note 3)	+ 5V	600			nSec
	+12V	300			nSec
Rise and Fall Times (Note 3)	+ 5V			15	μSec
	+12V			4	μSec
TRANSFER CHARACTERISTICS					
Linearity Error (Note 4): +25°C			±¼	±½	LSB
0°C to +70°C			±¼	±½	LSB
−55°C to +125°C ("H" Models)			±½	±1	LSB
Differential Linearity Error			±½		LSB
No Missing Codes (0°C to +70°C)			Guaranteed		
Full Scale Absolute Accuracy Error (Notes 5, 6):					
+25°C			± 0.05	± 0.1	%FSR
0°C to +70°C			± 0.2	± 0.5	%FSR
−55°C to +125°C ("H" Models)			± 0.3	± 0.6	%FSR
Zero Error (Notes 5, 6): +25°C			± 0.01		%FSR
0°C to +70°C			± 0.04	± 0.1	%FSR
−55°C to +125°C ("H" Models)			± 0.05	± 0.1	%FSR
Gain Error (Note 5)			± 0.05		%
Gain Drift			±20		ppm/°C
DYNAMIC CHARACTERISTICS					
Conversion Time (Note 2)				175	μSec
Analog Input Settling Time (Note 8)			2		μSec
DIGITAL OUTPUTS					
Logic Coding (Note 9): Unipolar Ranges		Complementary Straight Binary			
Bipolar Ranges		Complementary Offset Binary			
Logic Levels (Note 1): Logic "1"	+ 5V	4.95			Volts
	+12V	11.95			Volts
Logic "0"	+ 5V			0.01	Volts
	+12V			0.05	Volts
Output Drive Current, All Outputs:					
Logic "1" (V_{OH}=2.5V)	+ 5V	0.2	1.7		mA
(V_{OH}=11V)	+12V	0.3	1.0		mA
Logic "0" (V_{OL}=0.4V)	+ 5V	0.1	0.6		mA
(V_{OL}=1.5V)	+12V	1.0	4.0		mA

REFERENCE OUTPUT	+Vdd	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage			− 6.3		Volts
Accuracy			± 5.		%
Tempco of Drift			±15.		ppm/°C
Ext. Current Without Buffering				10	μA
POWER SUPPLY REQUIREMENTS					
Power Supply Range (Note 10): +12V Supply		+11.64	+12.00	+12.36	Volts
−12V Supply		−11.64	−12.00	−12.36	Volts
+ 5V Supply		+ 4.75	+ 5.00	+12.36	Volts
Power Supply Rejection: +12V Supply			± 0.003		%FSR/%Vs
−12V Supply			± 0.03		%FSR/%Vs
+ 5V Supply			± 0.0003		%FSR/%Vs
Current Drain: +12V Supply			2.4	3.5	mA
−12V Supply			− 2.0	− 2.7	mA
+ 5V Supply			0.5	1.0	mA
Power Consumption			56	80	mW

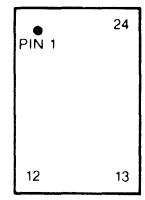
SPECIFICATION NOTES:

1. The +Vdd Logic Suppy (Pin 2) can be at any voltage between +5V (low power TTL compatibility) and +12V (CMOS compatibility).
2. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. See Timing Diagram. For MN5250 Series A/D's, a 175 μSec conversion time corresponds to an external clock frequency of 71 KHz. Micro Networks guarantees linearity and absolute accuracy at and below this clock frequency.
3. The clock may be asymmetrical, and it may ramp up and down as long as it meets minimum pulse width and maximum rise and fall time requirements.
4. Micro Networks tests and guarantees maximum linearity error at room temperature and at the high and low extremes of the specified operating temperature range.
5. See the tutorial section of the Micro Networks' Product Guide and Applications Manual for an explanation of how Micro Networks defines Full Scale Absolute Accuracy, Zero, and Gain Errors. For MN5250 Series A/D's we 100% test Full Scale Absolute Accuracy Error and Zero Error at room temperature and at the high and low extremes of the specified operating temperature range.
6. 1 LSB for a 12 bit converter corresponds to 0.024%FSR. See Note 7.
7. FSR stands for Full Scale Range and is equal to the peak to peak input voltage of the selected converter. For the MN5250, MN5251, and MN5253, FSR = 10V, and 1 LSB = 2.44mV. For the MN5252, FSR = 20V, and 1LSB = 4.88mV.
8. Analog Input Settling Time is the time required for the input circuitry to settle to within ±½ LSB for a 10V step in input signal.
9. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
10. The recommended range for the ±12V supplies is ±3%. Units will operate over a range of ±10V to ±14V with reduced accuracy.

BLOCK DIAGRAM



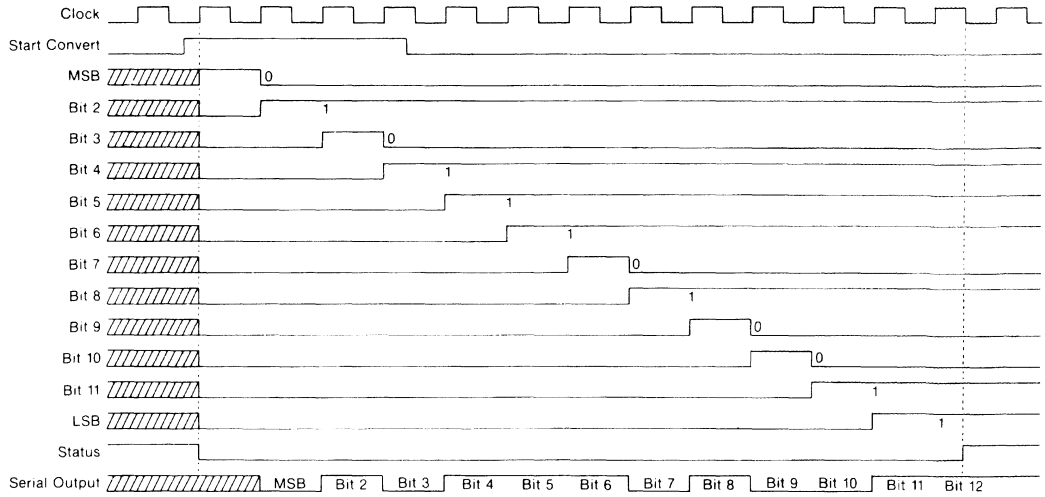
PIN DESIGNATIONS



Pin 1. Start Convert
Pin 2. Logic Supply (+Vdd)
Pin 3. Serial Output
Pin 4. Bit 6
Pin 5. Bit 5
Pin 6. Bit 4
Pin 7. Bit 3
Pin 8. Bit 2
Pin 9. Bit 1 (MSB)
Pin 10. N/C
Pin 11. Ground
Pin 12. Ref. Out (−6.3V)

Pin 13. −12V Supply
Pin 14. Analog Input
Pin 15. +12V Supply
Pin 16. Bit 12 (LSB)
Pin 17. Bit 11
Pin 18. Bit 10
Pin 19. Bit 9
Pin 20. Bit 8
Pin 21. Bit 7
Pin 22. Status (E.O.C.)
Pin 23. Ground
Pin 24. Clock Input

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 1101 0011 which corresponds to 6.357V on the 0 to + 10V (MN5253) input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "1", all other bits = "0", Status = "0") by holding the Start Convert high during a low to high clock transition; the Start Convert must be high for a minimum of 300nsec prior to the clock transition. Output bits, starting with the MSB, will be set to their final values on succeeding clock edges. The Start Convert must return low prior to the falling edge of the fourth clock cycle after conversion commences.
4. The Start Convert may be brought high at any time during a conversion to reset and begin converting again.
5. The delay between the resetting clock edge and the Status actually dropping to a "0" is 750nsec maximum.
6. The Status (E.O.C.) output will rise to a "1" 750nsec (maximum) after the first falling clock edge after the determination of LSB. Status will remain high until the converter is reset. Parallel output data is valid as long as Status is a "1".
7. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
8. For continuous conversion, connect the Status output pin (pin 22) to the Start Convert input (Pin 1).
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

DIGITAL OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT
MN5250	MN5251	MN5252	MN5253	MSB LSB
0.0000V − 0.0024V	+ 5.0000V + 4.9976V	+10.0000V + 9.9951V	+10.0000V + 9.9976V	0000 0000 0000 0000 0000 0000*
− 4.9976V − 5.0000V − 5.0024V	+ 0.0024V 0.0000V − 0.0024V	+ 0.0049V 0.0000V − 0.0049V	+ 5.0024V + 5.0000V + 4.9976V	0111 1111 1110* **0000 0000 0000*** 1000 0000 0000*
− 9.9976V −10.0000V	− 4.9976V − 5.0000V	− 9.9951V −10.0000V	+ 0.0024V 0.0000V	1111 1111 1110* 1111 1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as **0** will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

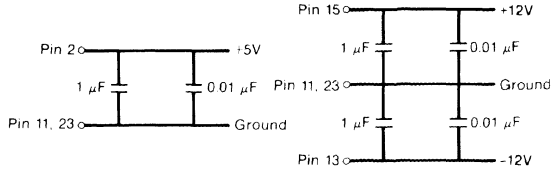
EXAMPLE: For an MN5252 (±10V analog input range) the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9951 volts. Subsequently, any input voltage more negative than −9.9951 volts will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 (or vice versa) will ideally occur at an input of zero volts, and the 0000 0000 0000 to 0000 0000 0001 (or vice versa) transition should occur at +9.9951 volts. An input greater than +9.9951 volts will give all "0's".

APPLICATIONS INFORMATION

The digital circuitry used in the MN5250 Series A/D's is CMOS. The standard precautionary measures for handling CMOS should be followed.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5250 Series converters. The units' two GROUND pins (Pins 11 and 23) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01 μF bypass capacitor should be connected between Pins 11 and 23 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagram below.



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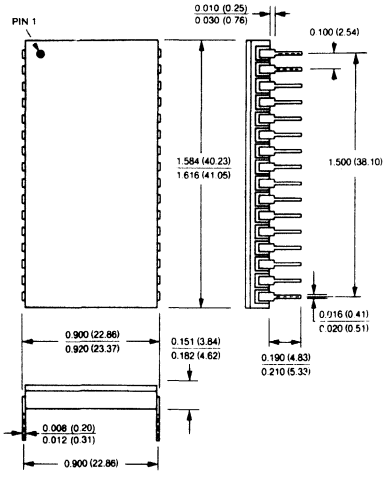
MN5284 Series

LOW-POWER
16-Bit
A/D CONVERTERS

FEATURES

- **16-Bit Resolution**
- **15-Bit No Missing Codes**
- **300mW Max Power Consumption**
- **50μsec Max Conversion Time**
- **Serial and Parallel Outputs**
- **True-TTL and 5V-CMOS Compatible**
- **Small 32-Pin Side-Brazed DIP**
- **$\pm$12V to $\pm$15V Power Supply Range**
- **8 User-Selectable Input Voltage Ranges**

32 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

An outstanding combination of resolution, speed, packaging, power consumption and price may make the MN5284 Series the best high-resolution A/D converters ever put in dual-in-line packages. Featuring 16-bit resolution and a maximum 50μsec conversion time, MN5284 Series A/D's are packaged in 32-pin, side-brazed, ceramic DIP's and have an impressively low 300mW maximum power consumption when operating from $\pm$15V and +5V supplies. $\pm$12V supplies may also be used.

These are successive approximation type A/D's fabricated in thin-film hybrid technology. Each employs a recently developed HCT CMOS successive approximation register and a proprietary, low-power, partially segmented, bipolar DAC that is inherently monotonic. "No missing codes" to the 15-bit level and true integral linearity to the 14-bit level are guaranteed over the device's entire 0°C to +70°C specified temperature range.

Each A/D is complete with internal reference and clock and is truely compatible with either TTL or 5V-CMOS logic families. Digital input currents are specified at $\pm$10μA max, and fanout is 2 standard TTL loads.

Originally designed for remote, lightweight, battery-operated data acquisition applications, MN5284 Series devices are extremely versatile. Their 50μsec max conversion time permits 167kHz data throughputs when used with Micro Networks MN373, High-Resolution Track-Hold Amplifier (10μsec max acquisition time to $\pm$0.003%, 300mW power consumption). Serial and parallel data outputs and optional CSB, COB and CTC output coding permit various data transmission and processing schemes, and devices may be short cycled to any resolution with a proportionately faster conversion time. Four part numbers in the Series offer the input voltage ranges shown below.

Part Number	Unipolar Input Range	Bipolar Input Range	LSB@ 14-Bits	LSB@ 16-Bits
MN5284	0 to −20V	$\pm$10V	1.22mV	305.2μV
MN5285	0 to −16.384V	$\pm$8.192V	1mV	250μV
MN5286	0 to −10V	$\pm$5V	0.61mV	152.6μV
MN5287	0 to −8.192V	$\pm$4.096V	0.5mV	125μV

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December 1991
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MN5284 SERIES LOW-POWER 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5284, 85, 86, 87	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 30)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 31)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 17)	−0.5 to +7 Volts
Analog Input (Pin 25)	Nominal ±5Volts
Digital Inputs (Pins 22, 24)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN528X
Select desired input voltage range. ———

SPECIFICATIONS (T_A = +25°C, ±V_{cc} = ±15V, +V_{dd} = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges (Note 1): Unipolar (MN5284, 85, 86, 87)		0 to −20, −16.384, −10, −8.192		Volts
Bipolar (MN5284, 85, 86, 87)		±10, ±8.192, ±5, ±4.096		Volts
Input Impedance: 0 to −20V, ±10V (MN5284)		20		kΩ
0 to −16.384V, ±8.192V (MN5285)		16.384		kΩ
0 to −10V, ±5V (MN5286)		10		kΩ
0 to −8.192V, ±4.096V (MN5287)		8.192		kΩ
DIGITAL INPUTS				
Logic Levels (Note 2): Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents (V_{IH} = +5V, V_{IL} = 0V, Note 2)			±10	μA
Start Convert Command Positive Pulse Width (Note 3)	1			μsec
TRANSFER CHARACTERISTICS (Note 4)				
Resolution		16		Bits
Integral Linearity Error (Note 5): Initial (+25°C)		±0.0015	±0.003	%FSR
Over Temperature (Note 6)			±0.003	%FSR
Differential Linearity Error: Initial (+25°C)		±0.0015	±0.003	%FSR
Over Temperature (Note 6)			±0.006	%FSR
Temperature Range for Guaranteed 15-Bit No Missing Codes MN5284, 85, 86, 87	0		+70	°C
Full Scale Absolute Accuracy Error (Note 7):				
Unipolar: Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 6)		±0.1	±0.2	%FSR
Bipolar: Initial (+25°C)		±0.05	±0.15	%FSR
Over Temperature (Note 6)		±0.1	±0.25	%FSR
Unipolar Offset Error (Notes 8, 9): Initial (+25°C)		±0.025	±0.1	%FSR
Over Temperature (Note 6)		±0.05	±0.15	%FSR
Drift		±2		ppm of FSR/°C
Bipolar Zero Error (Notes 8, 10): Initial (+25°C)		±0.05	±0.12	%FSR
Over Temperature (Note 6)		±0.1	±0.2	%FSR
Drift		±5		ppm of FSR/°C
Gain Error (Notes 8, 11): Initial (+25°C)		±0.05	±0.1	%
Over Temperature (Note 6)		±0.1	±0.2	%
Drift		±5	±15	ppm/°C
DIGITAL OUTPUTS				
Logic Levels (Note 2): Logic "1" ($I_{SOURCE} \leq 400\mu A$)	+3.5			Volts
Logic "0" ($I_{SINK} \leq 3.2mA$)			+0.4	Volts
Output Coding (Note 12): Unipolar Ranges		CSB		
Bipolar Ranges		COB, CTC		
REFERENCE OUTPUT				
Internal Reference: Voltage		−9.000		Volts
Accuracy		±0.025	±0.05	%
Tempco		±5		ppm/°C
External Current			1	mA

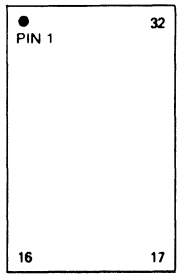
DYNAMIC CHARACTERISTICS (Note 13)	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits) (Note 14)		45	50	μsec
Internal Clock Frequency	320			kHz
Delay Falling Edge of Start to: Status = "1" Clock Output = "1"		75 40	150 80	nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		35	70	nsec
Delay LSB valid to Falling Edge of Status	40			nsec
POWER SUPPLIES				
Power Supply Range (Note 15): $\pm V_{cc}$ Supply $+V_{dd}$ Supply	±11.4 +4.75	± 15 + 5	± 16 + 5.25	Volts Volts
Power Supply Rejection: + Vcc Supply − Vcc Supply + Vdd Supply		± 0.001 ± 0.001 ± 0.001		%FSR/% Supply %FSR/% Supply %FSR/% Supply
Current Drains: + Vcc Supply − Vcc Supply + Vdd Supply		9 − 5 9		mA mA mA
Power Consumption (± Vcc = ± 15V)		255	300	mW

SPECIFICATION NOTES:

1. 0 to − 16.384V and ± 8.192V input ranges correspond to 1 LSB = 1mV for 14 bits or 1 LSB = ¼mV for 16 bits. 0 to − 8.192V and ± 4.096V input ranges correspond to 1 LSB = ½mV for 14 bits and 1 LSB = ⅛mV for 16 bits.
2. Digital portions of MN5284 Series A/D's are implemented with HCT CMOS logic and devices are true TTL and 5V CMOS compatible with specified logic levels and currents guaranteed over each devices entire specified temperature range.
3. Conversion is initiated on falling edge of Start Convert command; see timing diagram.
4. FSR = full scale range. A unit connected for 0 to + 10V or ± 5V operation has a 10V FSR. A ± 10V unit has a 20V FSR. A ± 8.192V unit has a 16.38V FSR etc. 1 LSB for 16 bits is equivalent to 0.00153%FSR, 1 LSB for 15 bits is equivalent to 0.00305%FSR.
5. ±0.003%FSR is equivalent to ± ½ LSB for 14 bits. ±0.0015%FSR is equivalent to ± ½ LSB for 15 bits.
6. Listed specifications apply over the 0°C to +70°C temperature range for standard products.
7. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. It refers to negative full scale accuracy for unipolar ranges and to both positive and negative full scale accuracies for bipolar ranges.
8. Initial offset and gain errors are adjustable to zero with optional external potentiometers or voltage output D/A converters.
9. Unipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 digital output code transition occurs when operating on a unipolar input range.
10. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 1000 0000 0000 0000 to 0111 1111 1111 1111 digital output code transition occurs when operating on a bipolar input range.
11. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from all 1111 1111 1111 1111 to 1111 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0000 0001 to 0000 0000 0000 0000.
12. CSB = complementary straight binary. COB = complementary offset binary. For bipolar ranges, complementary two's complement (CTC) coding is available if the MSB output is used.
13. Listed dynamic specifications are guaranteed over each device's entire specified temperature range.
14. Conversion time is defined as the width of the Status (End of conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 15 (Bit 15), for example, to pin 24 (Short Cycle) for 14-bit conversions.
15. For operation with $\pm V_{cc}$ supplies below ±12V, only 0 to -8.192V, ±8.192V, ±5V and ±4.096V input ranges should be used.

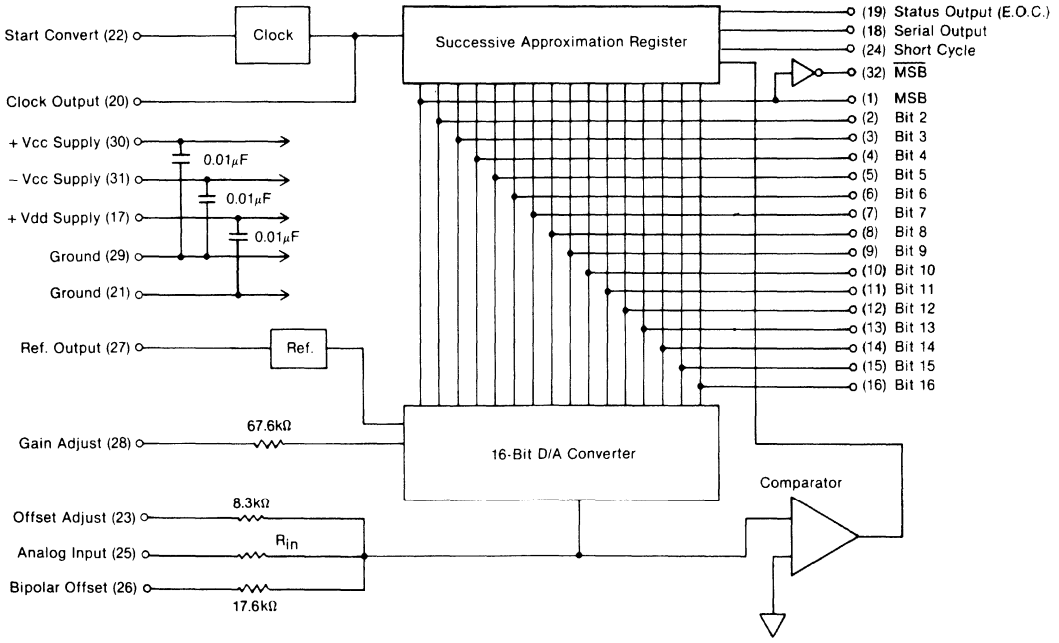
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	Bit 1 (MSB)	32	$\overline{\text{Bit 1 (MSB)}}$
2	Bit 2	31	− Vcc Supply (− 12V/ − 15V)
3	Bit 3	30	+ Vcc Supply (+ 12V/ + 15V)
4	Bit 4	29	Ground
5	Bit 5	28	Gain Adjust
6	Bit 6	27	Reference Output (− 9.0V)
7	Bit 7	26	Bipolar Offset
8	Bit 8	25	Analog Input
9	Bit 9	24	Short Cycle
10	Bit 10	23	Offset Adjust
11	Bit 11	22	Start Convert
12	Bit 12	21	Ground
13	Bit 13	20	Clock Output
14	Bit 14	19	Status Output (E.O.C.)
15	Bit 15	18	Serial Output
16	Bit 16 (LSB)	17	+ Vdd Supply (+ 5V)

BLOCK DIAGRAM



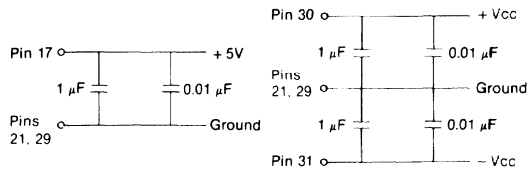
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified linearity and accuracy from MN5284 Series devices. It is critically important that power supplies be filtered, well-regulated, and free from high frequency noise. Use of noisy supplies can easily cause unstable output codes tc be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit or better accuracy unless great care is used in filtering any switching spikes present in the output.

MN5284's two ground pins (pins 21 and 29) are not connected to each other internal to the device. It is recommended, however, that the two pins be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large, low-impedance, analog ground plane beneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Power supply connections should be short and direct, and even though MN5284 has internal 0.01μF ceramic bypass capacitors, it is recommended that all power supplies be decoupled with additional high-frequency bypass capacitors to ground. For optimum performance and noise rejection, 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space. If the recommended ground-plane approach can not be used and separate p.c. card ground runs are used, the ± Vcc supplies should be decoupled to pin 29 and the + Vdd supply to pin 21.

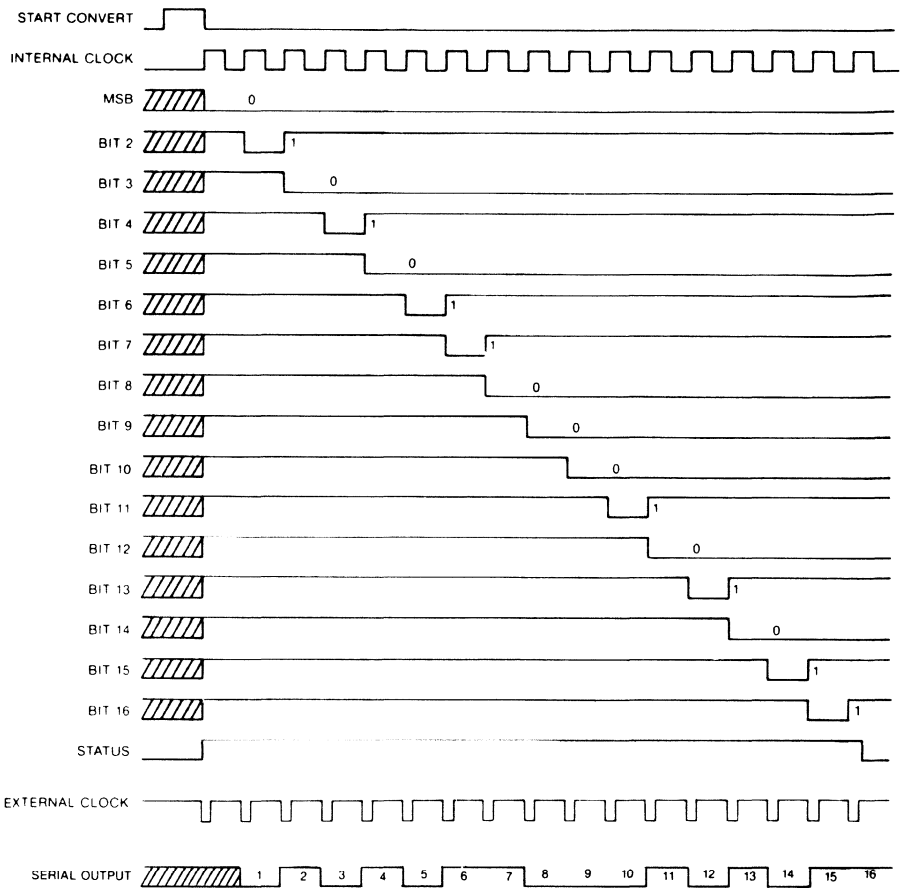
POWER SUPPLY DECOUPLING



Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 23 (Offset Adjust), 25 (Analog Input), 26 (Bipolar Offset), 27 (Reference Output), and 28 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing these pins. Input signal lines should be as short as possible. In bipolar operation, where pin 26 is connected to pin 27, a short jumper should be used. When using external offset and gain adjustments, the adjusting pots or voltage-output DAC's should be located as close to MN5284 as possible. If using optional gain adjust, an 0.01μF ceramic capacitor should be connected between pin 28 and analog ground as close to the package as possible. Similarly, if using the Reference Output (pin 27) to drive an external load or to operate MN5284 in a bipolar mode, an 0.01μF ceramic capacitor should be connected between pin 27 and analog ground.

If short-cycling is not used, the Short-Cycle pin (pin 24) must be connected to + 5V (pin 17).

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise specified)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits)		45	50	μsec
Internal Clock Frequency	320			kHz
Start Convert Positive Pulse Width	1			μsec
Delay Falling Edge of Start to: Status = "1" Clock Output = "1"		75 40	150 80	nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status)		35	70	nsec
Delay LSB valid to Falling Edge of Status	40			nsec

TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command must be at least 1μsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Output data will be valid 40nsec (minimum) prior to the falling edge of Status (E.O.C.) and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following Status going low at the end of the previous conversion. See External Clock.
6. Once a conversion has begun, a second start pulse will not reset the converter. See Start Convert.
7. When the converter is initially "powered up", it may come on at any point in the conversion cycle.
8. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 15 (Bit 15) to pin 24 (Short Cycle) for 14 bit conversions.

START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 1μsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

DESCRIPTION OF OPERATION — See Block Diagram. The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the analog-to-digital converter (A/D) and the digital drive for the A/D's internal digital-to-analog converter (D/A). The falling edge of a start convert pulse applied to pin 22 turns on the A/D's internal clock and resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status Output (pin 19) is set to logic "1" (see Timing Diagram). The Start Convert must now remain low for the conversion to continue.

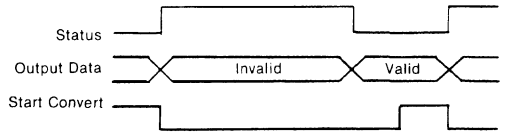
The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 16) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

SHORT CYCLING — For applications requiring less than 16 bits resolution, MN5284 Series A/D's can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle pin (pin 24). For example, to truncate at 14 bits, connect pin 15 (Bit 15) to pin 24; converting will stop and the Status output will go low after bit 14 has been set. Bit 14 (the LSB for a 14-bit conversion) will be valid approximately 40nsec prior to the falling edge of status.

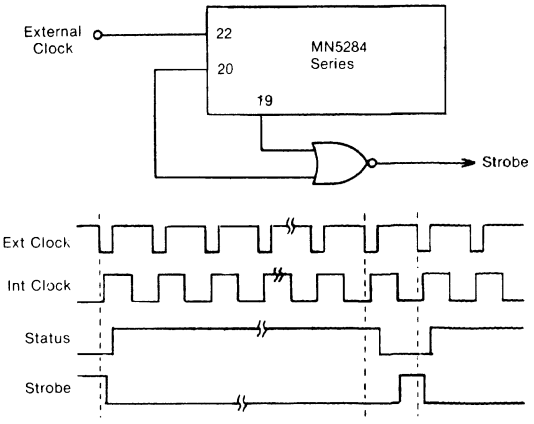
EXTERNAL CLOCK — An external clock may be connected to the Start Convert input. This external clock must consist of negative-going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever the Start Convert input is held high. When using an external clock, a Start Convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after the Status output has gone low signaling the end of the previous conversion. When continuously converting in this manner, the Status output will go low for one external clock period following the completion of each conversion.

SERIAL OUTPUT — Serial data is available only during the conversion process. Format is NRZ with the MSB occuring first. Serial data is coded the same as parallel output data, and it is synchronous with the internal clock as shown in the timing diagram. Each data bit becomes valid no longer than 70nsec after each rising clock edge and remains valid for the full clock period. Therefore, falling clock edges can be used to strobe serial data into output registers.

STATUS OUTPUT — The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. There is a minimum 40nsec delay between the point at which the LSB becomes valid (is set to its final value) and the status output falls to a "0". If an external latch is used to clock output data away from the MN5284, this 40nsec may or may not be long enough to satisfy the set-up time requirement of the latch. If it is not, additional delay will have to be generated. Simple gate delays can be employed or the latch can be controlled by the leading edge of the next start convert pulse. Recall that existing output data does not become invalid until the falling edge of the start pulse. See diagram below.



If continuously converting with an external clock, the Status output can be NORed with the internal clock output, as shown below, to produce a positive strobe pulse approximately ½ period wide, approximately ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion. Recall that the falling edges of the external clock pulses generate rising edges of the internal clock and that these two clocks appear 180 degrees out of phase. The delay from the rising edge of the internal clock to the rising edge of Status is typically 35nsec. See Timing Diagram and the section labeled External Clock.



INTERNAL REFERENCE — MN5284 Series devices contain an internal, low-drift −9V reference that is laser trimmed to an initial accuracy of ±0.05%. The reference is pinned out on pin 27 and can supply up to 1mA beyond the current required for bipolar operation (pin 27 connected to pin 26). If the external load is expected to vary during converter operation or if the internal reference is to be used to drive external circuitry at elevated temperatures, the reference output should be buffered externally.

DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
Unipolar Ranges	**Bipolar Ranges**	**MSB LSB**
0	+ F.S.	0000 0000 0000 0000
− 1 LSB	+ F.S. − 1 LSB	0000 0000 0000 000Ø*
− ½ F.S. + 1 LSB	+ 1 LSB	0111 1111 1111 111Ø*
− ½ F.S.	0	ØØØØ ØØØØ ØØØØ ØØØØ*
− ½ F.S. − 1 LSB	− 1 LSB	1000 0000 0000 000Ø*
− F.S. + 1 LSB	− F.S. + 1 LSB	1111 1111 1111 111Ø*
− F.S.	− F.S.	1111 1111 1111 1111

Part Number	Unipolar Input Range	Bipolar Input Range	LSB VALUE	
			16-Bits	**14-Bits**
MN5284	0 to − 20V	± 10V	305.2μV	1.22mV
MN5285	0 to − 16.384V	± 8.192V	250μV	1mV
MN5286	0 to − 10V	± 5V	152.6μV	0.61mV
MN5287	0 to − 8.192V	± 4.096V	125μV	0.5mV

CODING NOTES:

1. For unipolar ranges, the coding is complementary straight binary.
2. For bipolar ranges, the coding is complementary offset binary.
3. For bipolar ranges, if $\overline{\text{MSB}}$ is used instead of MSB, the coding will be complementary two's complement.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5284 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the ± 10V range, the transition from output code 0000 0000 0000 0000 to output code 0000 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of + 9.999695V (+ F.S. − 1 LSB). Subsequently, any voltage greater than + 9.999695V will give a digital output of all "0's". The transition from digital output 1000 0000 0000 0000 to 0111 1111 1111 1111 (or vice versa) will ideally occur at an input of zero volts. The 1111 1111 1111 1111 to 1111 1111 1111 1110 transition will occur at − 9.999695V. An input more negative than this level will give all "1's".

INPUT RANGE SELECTION — MN5284 Series A/D's have an internal, current-output, 16-bit D/A converter that is complementary coded and sources current at its output. Consequently, MN5284 Series A/D's are complementary coded and have unipolar input ranges that are negative (0 to − 20V, 0 to − 16.384V, etc.). Each device in the Series has one unipolar and one bipolar input voltage range. Unipolar ranges are selected by leaving pin 26 (Bipolar offset) open; bipolar ranges are selected by connecting pin 26 (Bipolar offset) to pin 7 (Reference Output).

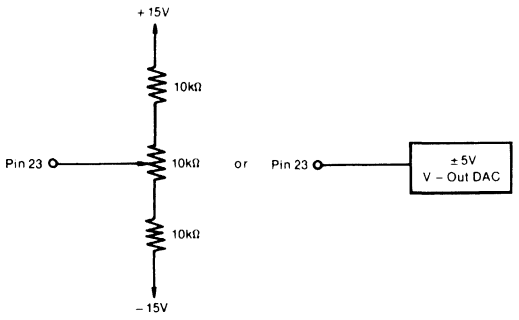
Making the bipolar-offset connection pulls a constant current from the comparator summing junction and has the effect of offsetting the device transfer function "upward" an amount equal to ½ of its full scale range (FSR). Recall that the traditional definition of unipolar offset error for a successive approximation A/D is the input-output accuracy error that occurs when the internal D/A is turned "off" or sourcing zero current (see the tutorial section of the Micro Networks catalog for details) and that for MN5284 type A/D's operating on their unipolar input range, this error occurs around zero volts (the all "0's" digital output). If one were performing optional unipolar offset adjustment, it would be done at this point. Note that making the bipolar-offset connection effectively moves this point "upward" to + ½FSR (equivalent to the positive full scale point on the bipolar input range). Now, at least according to traditional definitions, the point at which bipolar offset error occurs is the positive full scale point (still the all "0's" digital output), and if one were performing optional bipolar-offset adjustment, it would be done at this point.

To avoid potential confusion, Micro Networks does not specify bipolar offset error for MN5284 Series A/D's. We specify unipolar offset error and unipolar negative full scale accuracy (Full Scale Absolute Accuracy Error) for unipolar input ranges, and for bipolar input ranges, we specify positive and negative full scale accuracy as well as a bipolar zero error (around the zero-volt input point).

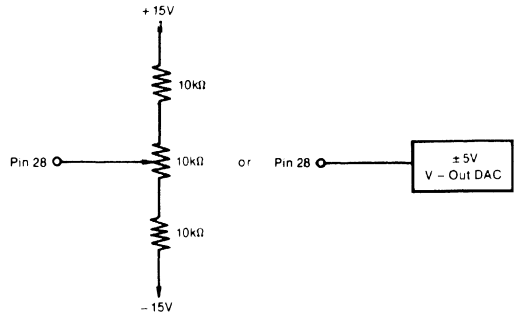
OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS — Initial offset and gain errors may be trimmed to zero using external potentiometers or voltage output DAC's as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, offset should be adjusted before gain. The gain and offset adjust points (pins 28 and 23) are purely resistive and are specifically designed to be driven with applied voltages ranging from + 5V to − 5V. Adjusting voltages can be generated by tying potentiometers to the supplies or, in microprocessor based applications, by using voltage output DAC's. If potentiometers are used, they should be r ,ultiturn devices with TCR's of 100ppm/°C or less. Fixed resistors can be ± 20% carbon composition or better. If these adjustments are not used, pin 23 should be left open and pin 28 should be decoupled to ground with a 0.01μF ceramic capacitor.

OFFSET ADJUSTMENT—Connect the offset potentiometer to pin 23 as shown. For unipolar ranges, apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "0" and the LSB "flickers" on and off. For bipolar ranges, apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur (see Digital Output Coding). While continuously converting, adjust the offset potentiometer until all the output bits are "flickering". The offset adjust sensitivity is approximately ±0.04%FSR/Volt, and the total range of offset adjust, using the applied voltages of ±5V, is ±0.2%FSR.

GAIN ADJUSTMENT — Connect the gain potentiometer to pin 28 as shown, and apply the input voltage at which the 1111 1111 1111 1111 to 1111 1111 1111 1110 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off. The gain-adjust sensitivity is approximately ±0.08%/Volt, and the total range of gain adjust, using applied voltages of ±5V, is ±0.4%.



OFFSET ADJUST



GAIN ADJUST

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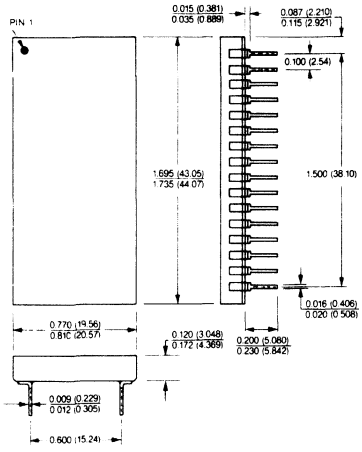
MN5290
MN5291

HIGH-RESOLUTION
EXTENDED-TEMPERATURE
A/D CONVERTERS

FEATURES

- 16-Bit Resolution
- 14-Bit Performance Guaranteed Over Temperature
- 40μsec Max Conversion Time
- ±0.003% FSR Maximum Linearity Error
- Serial and Parallel Outputs
- 6 User-Selectable Input Ranges
- 1080mW Max Power Consumption
- Standard 32-Pin DIP
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

32 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN5290 and MN5291 are high-performance, dual-in-line packaged, 40μsec, 16-bit A/D converters specifically designed for use in military/aerospace and industrial applications that demand fully guaranteed high-resolution performance over extended operating temperature ranges. These successive approximation A/D converters exploit the stability and tracking advantages of both SiCr and NiCr thin-film resistor technologies. Fully assembled devices are functionally laser trimmed before and after a proprietary resistor stabilization process that made MN5290 and MN5291 the industry's first 16-bit A/D's to fully guarantee performance from −55°C to +125°C. Recently, the Micro Networks MN5295/5296 (17μsec conversion time) have joined MN5290/5291 as the only true military 16-bit A/D's.

MN5290 and MN5291 are packaged in industry-standard, hermetically sealed, 32-pin, ceramic, dual-in-line packages. Each is complete with internal clock and reference and has 6 user-selectable input ranges. Output data is straight binary coded for unipolar input ranges and offset binary coded for bipolar input ranges and is available in both serial and parallel formats.

MN5290 and MN5291 are ideal for applications requiring true 14- and 13-bit performance over extended temperature ranges. Applications will be found in military instrumentation, ATE and servo systems and in industrial robotic position sensing systems. MN5290H/B and MN5291H/B are available with Environmental Stress Screening while MN5290H/B CH and MN5291H/B CH are screened in accordance with MIL-H-38534.

Model Number	Temperature Range for Guaranteed No Missing Codes	
MN5290	14 Bits	0°C to +70°C
MN5290E	14 Bits	−25°C to +85°C
MN5290H	14 Bits	−55°C to +125°C
MN5290H/B	14 Bits	−55°C to +125°C
MN5290H/B CH	14 Bits	−55°C to +125°C
MN5291	13 Bits	0°C to +70°C
MN5291E	13 Bits	−25°C to +85°C
MN5291H	13 Bits	−55°C to +125°C
MN5291H/B	13 Bits	−55°C to +125°C
MN5291H/B CH	13 Bits	−55°C to +125°C

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January 1992
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MN5290 MN5291 HIGH-RESOLUTION A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5290, MN5291	0°C to +70°C
MN5290E, MN5291E	−25°C to +85°C
MN5290H, H/B; MN5291H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 27)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 23)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pin 29)	0 to +7 Volts
Analog Inputs (Pins 8 and 9)	±22 Volts
Digital Inputs (Pins 30 and 32)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5290 H/B CH

- Select MN5290 or MN5291 model.
- Standard Part is specified for 0°C to +70°C operation.
- Add "E" suffix for specified −25°C to +85°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 1)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +5, 10, 20		Volts
Bipolar		±2.5, 5, 10		Volts
Input Impedance (Note 2): 0 to +5V, ±2.5V		2.5		kΩ
0 to +10V, ±5V		5		kΩ
±10V		10		kΩ
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
TRANSFER CHARACTERISTICS (Note 3)				
Resolution		16		Bits
Integral Linearity Error (Note 4): Initial (+25°C): MN5290		±0.0015	±0.003	%FSR
MN5291		±0.003	±0.006	%FSR
Over Temperature (Note 5): MN5290		±0.003	±0.006	%FSR
MN5291		±0.006	±0.012	%FSR
Differential Linearity Error (Note 4): MN5290		±0.003	±0.006	%FSR
MN5291		±0.006	±0.012	%FSR
Temperature Range for Guaranteed No Missing Codes				
MN5290 (14 bits), MN5291 (13 bits)	0		+70	°C
MN5290E (14 bits), MN5291E (13 bits)	−25		+85	°C
MN5290H (14 bits), MN5291H (13 bits)	−55		+125	°C
Full Scale Absolute Accuracy Error (Note 6):				
Unipolar: Initial (+25°C)		±0.075	±0.15	%FSR
Over Temperature (Note 5)		±0.15	±0.3	%FSR
Bipolar: Initial (+25°C)		±0.1	±0.2	%FSR
Over Temperature (Note 5)		±0.2	±0.4	%FSR
Unipolar Offset Error (Notes 7, 8): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 5)		±0.1	±0.2	%FSR
Drift		±5	±15	ppm of FSR/°C
Bipolar Zero Error (Notes 7, 9): Initial (+25°C)		±0.05	±0.12	%FSR
Over Temperature (Note 5)		±0.1	±0.2	%FSR
Drift		±5	±15	ppm of FSR/°C
Gain Error (Notes 7, 10): Initial (+25°C)		±0.05	±0.1	%
Over Temperature (Note 5)		±0.1	±0.2	%
Drift		±5	±20	ppm/°C
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 11): Unipolar Ranges		SB		
Bipolar Ranges		OB		
Logic Levels: Logic "1" ($I_{SOURCE} \leq 320\mu A$)	+2.4			Volts
Logic "0" ($I_{SINK} \leq 3.2mA$)			+0.4	Volts
REFERENCE OUTPUT				
Internal Reference: Voltage		+10.000		Volts
Accuracy		±0.025	±0.1	%
Tempco (Note 2)		±5		ppm/°C
External Current (Notes 2,12)			1	mA
DYNAMIC CHARACTERISTICS				
Conversion Time (14 Bits/16 Bits) (Note 13)		34/38	36/40	μsec

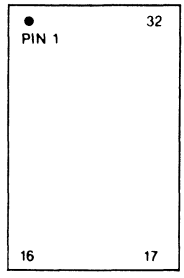
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: ±15V Supplies +5V Logic Supply	±14.55 +4.75	±15 +5	±15.45 +5.25	Volts Volts
Power Supply Rejection (Note 14): +15V Supply −15V Supply +5V Logic Supply		±0.005 ±0.005 ±0.001	±0.02 ±0.02 ±0.01	%FSR/%Supply %FSR/% Supply %FSR/% Supply
Current Drains: +15V Supply −15V Supply +5V Logic Supply		+30 −20 +12	+37 −29 +18	mA mA mA
Power Consumption		810	1080	mW

SPECIFICATION NOTES:

1. Listed specifications apply for all part numbers unless specifically indicated. Detailed timing specifications appear in the Timing sections of this data sheet.
2. These parameters are listed for reference only and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for 0 to +20V or ±10V operation has a 20V FSR. A unit connected for 0 to +10V or ±5V operation has a 10V FSR etc. 1 LSB for 16 bits is equivalent to 0.00153%FSR. 1 LSB for 14 bits is equivalent to 0.0061%FSR.
4. ±0.003%FSR is equivalent to ±½ LSB for 14 bits. ±0.006%FSR is equivalent to ±½ LSB for 13 bits.
5. Listed specifications apply over the 0°C to +70°C temperature range for standard products, over the −25°C to +85°C range for "E" products and over the −55°C to +125°C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Initial unipolar offset (bipolar zero) and gain errors are adjustable to zero with the use of external potentiometers.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN5290/5291 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN5290/5291 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
10. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 to the input voltage at which the output changes from 0000 0000 0000 0001 to 0000 0000 0000 0000.
11. SB = straight binary. OB = offset binary. See table of transition voltages in section labeled Digital Output Coding.
12. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 7 connected to pin 24), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
13. Conversion is initiated on the falling edge of the start convert command, and conversion time is defined as the width of the status (end of conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14-bit conversions. See Timing Diagram.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

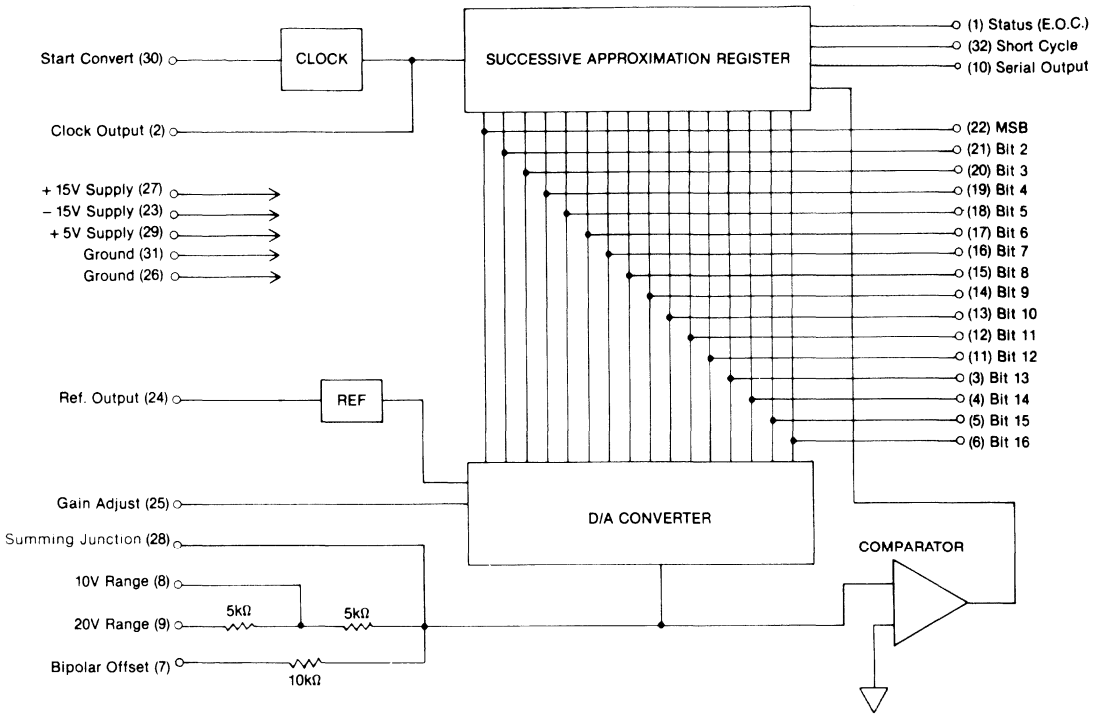
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	Status (E.O.C.)	32	Short Cycle
2	Clock Output	31	Ground
3	Bit 13	30	Start Convert
4	Bit 14	29	+5V Supply (+V_{dd})
5	Bit 15	28	Summing Junction
6	Bit 16 (LSB)	27	+15V Supply (+V_{cc})
7	Bipolar Offset	26	Ground
8	10V Input Range	25	Gain Adjust
9	20V Input Range	24	Reference Output (+10V)
10	Serial Output	23	−15V Supply (−V_{cc})
11	Bit 12	22	Bit 1 (MSB)
12	Bit 11	21	Bit 2
13	Bit 10	20	Bit 3
14	Bit 9	19	Bit 4
15	Bit 8	18	Bit 5
16	Bit 7	17	Bit 6

BLOCK DIAGRAM



APPLICATIONS INFORMATION

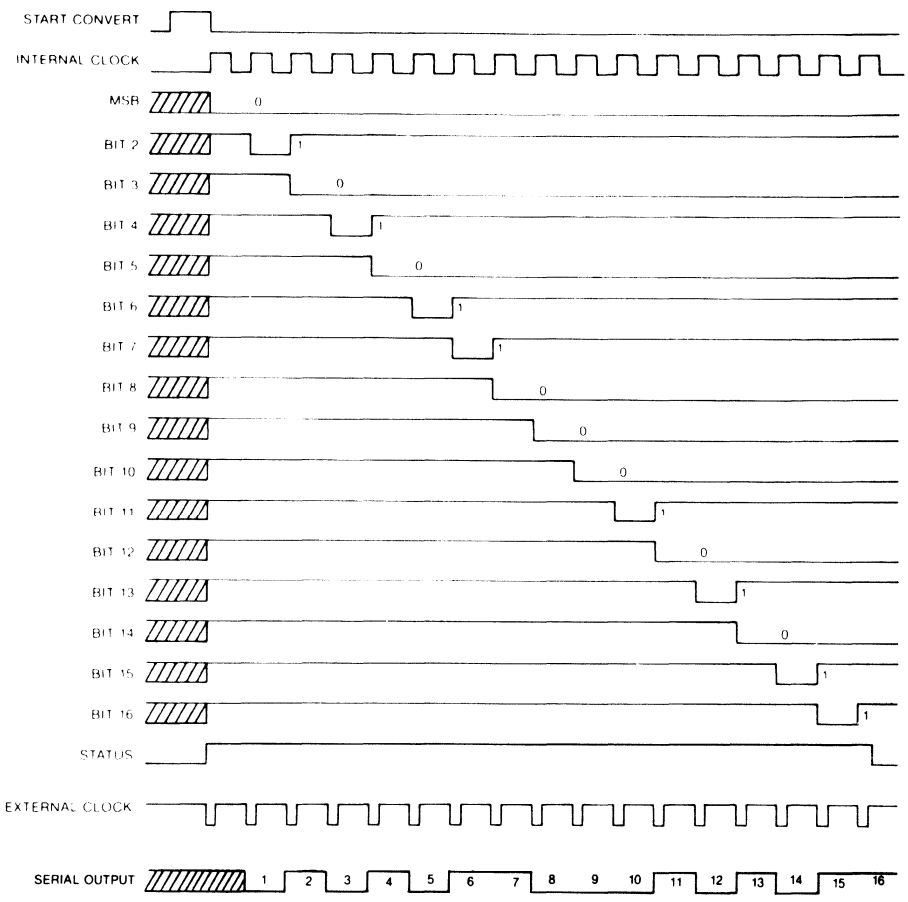
DESCRIPTION OF OPERATION—See Block Diagram. The successive approximation register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the analog-to-digital converter (A/D) and the digital drive for the A/D's internal digital-to-analog converter (D/A). The falling edge of a start convert pulse applied to pin 30 turns on the A/D's internal clock and resets the SAR. In this state, the output of the MSB flip flop is set to logic "0"; the outputs of the other bit flip flops are set to a logic "1"; and the Status (pin 1) is set to logic "1" (see Timing Diagram). The Start Convert must now remain low for the conversion to continue.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after Start Convert has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 16) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5290 and MN5291. The units' two ground pins (pins 26 and 31) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a nonpolarized 0.01μF ceramic bypass capacitor should be connected between pins 26 and 31 as close to the unit as possible and wide conductor runs employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 7 (Bipolar Offset), 8 and 9 (Analog Inputs), 28 (Summing Junction) and 25 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when using these inputs. Input signal lines should be as short as possible. In bipolar operation, where pin 7 is connected to pin 24, a short jumper should be used. If bipolar offsetting is not used, pin 7 should be grounded to pin 26. For external offset adjustment, the 1.8 megohm resistor should be located as close to pin 28 as possible. A 0.01μF ceramic capacitor should be connected between pin 25 and analog ground as close to the package as possible.

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise specified)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (14 Bits/16 Bits)		34/38	36/40	μsec
Internal Clock Frequency (Note 8)		420		kHz
Start Convert Positive Pulse Width (Note 8)	50			nsec
Delay Falling Edge of Start to (Note 8): Status = "1" Clock Output = "1"		50 20	80 50	nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20	120	200	nsec
Delay LSB Valid to Falling Edge of Status (Note 8)	20	60		nsec

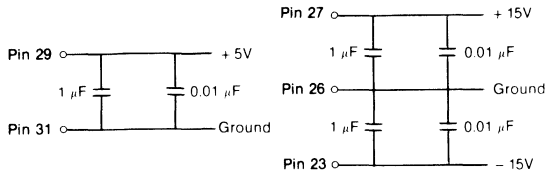
TIMING DIAGRAM NOTES

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Data will be valid 60nsec before the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock.
6. When the converter is initially "powered up", it may come on at any point in the conversion cycle.
7. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14 bit conversions.
8. These parameters are listed for reference only and are not tested.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN5290 and MN5291. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagram below.

If short cycling is not used, the Short Cycle pin (pin 32) must be connected to +5V (pin 29).

POWER SUPPLY DECOUPLING



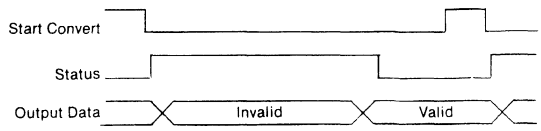
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

SHORT CYCLING—For applications requiring fewer than 16 bits of resolution, the MN5290 and MN5291 can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle pin (pin 32). For example, to truncate at 14 bits, connect pin 5 (Bit 15) to pin 32; converting will stop and Status will go low after bit 14 has been set. For any length conversion, the falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs.

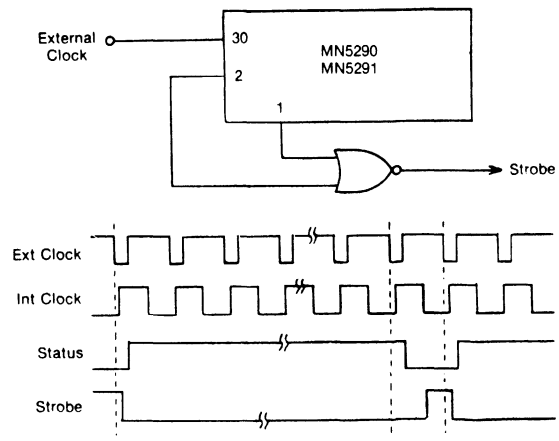
EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative-going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever Start Convert is held high. When using an external clock, a Start Convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after Status has gone low signaling the end of the previous conversion. When continuously converting in this manner, Status will go low for one external clock period following the completion of each conversion.

SERIAL OUTPUT—Serial data is available only during the conversion process. Format is NRZ with the MSB occurring first. Serial data is coded the same as parallel output data, and it is synchronous with the internal clock as shown in the Timing Diagram. Each data bit becomes valid typically 120nsec after each rising clock edge and remains valid for the full clock period. Therefore, falling clock edges can be used to strobe serial data into output registers.

STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. The falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs. If parallel data is to be latched into external registers, this delay should be long enough to accomodate the set-up time requirements of the latch such that Status can be used to strobe the latch. If the delay is not long enough, the Status can be delayed with gate delays or the latch can be strobed with the leading edge of the next start convert pulse. See diagram below.

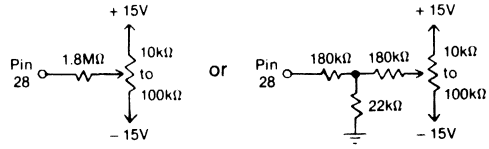


If continuously converting with an external clock, Status can be NORed with the internal clock, as shown below, to produce a positive strobe pulse approximately ½ period wide, approximately ½ period after Status has gone low. The rising edge of this pulse can be used to latch data after each conversion. Recall that the falling edges of the external clock pulses generate rising edges of the internal clock and that these two clocks appear 180 degrees out of phase. The delay from the rising edge of the internal clock to the rising edge of Status is typically 120nsec. See Timing Diagram and the section labeled External Clock.



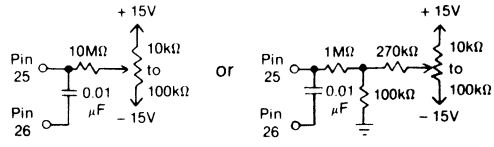
INTERNAL REFERENCE—The MN5290 and MN5291 contain an internal, low-drift 10V reference that is laser trimmed to an initial accuracy of ±0.1%. The reference is pinned out on pin 24 and can supply up to 1mA beyond the current required for bipolar operation (pin 24 connected to pin 7). If the external load is expected to vary during converter operation or if the internal reference is to be used to drive external circuitry at elevated temperatures, the reference output should be buffered externally.

OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS — Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 28 should be connected as described in the Range Selection section.



ZERO ADJUSTMENT—Connect the zero adjust potentiometer as shown. For unipolar ranges, apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off. For bipolar ranges, apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits "flicker" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off.



DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+ F.S.	+ F.S.	1111 1111 1111 1111
+ F.S. − ½ LSB	+ F.S. − ½ LSB	1111 1111 1111 111Ø*
+ ½ F.S. + ½ LSB	+ ½ LSB	1000 0000 0000 000Ø*
+ ½ F.S. − ½ LSB	− ½ LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+ ½ F.S. − ½ LSB	− ½ LSB	0111 1111 1111 111Ø*
+ ½ LSB	− F.S. + ½ LSB	0000 0000 0000 000Ø*
0	− F.S.	0000 0000 0000 0000

CODING NOTES:

1. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV, 1LSB for 14 Bits = 610.4μV.
2. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV, 1LSB for 14 Bits = 1.22mV.
3. For unipolar ranges, the coding is straight binary.
4. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5290/MN5291 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE					
	0 to + 5V	0 to + 10V	0 to + 20V	± 2.5V	± 5V	± 10V
Connect Pin 7 to Pin	26	26	26	24	24	24
Connect Pin 9 to Pin	28	Open	Input	28	Open	Input
Connect Pin 28 to Pin	9	Open	Open	9	Open	Open
Connect Input to Pin	8	8	9	8	8	9
Input Impedance (KΩ)	2.5	5	10	2.5	5	10

EXAMPLE. For the ± 10V range, the transition from output code 1111 1111 1111 1110 to output code 1111 1111 1111 1111 (or vice versa) will ideally occur at an input of + 9.999542V (+ F.S. − ½LSB). Subsequently, any voltage greater than + 9.999542V will give a digital output of all "1's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of − 0.000153 volts. The 0000 0000 0000 0000 to 0000 0000 0000 0001 transition will occur at − 9.999847V. An input more negative than this level will give all "0's."

USING TRACK-HOLD AMPLIFIERS WITH MN5290 AND MN5291 CONVERTERS

Successive approximation type A/D converters cannot accurately digitize analog signals whose slew rates produce amplitude changes (ΔV) greater than ± ½LSB during the A/D conversion time (Δt). If such signals are to be accurately digitized, a sample/hold (S/H) or track/hold (T/H) amplifier will be required in front of the A/D to hold input signals constant during the conversion period. For an MN5290 operating on its ± 10V input range and short cycled for 14-bit conversions, ½LSB (ΔV) is equivalent to 0.61mV, and the maximum conversion time (Δt) is 36μsec. Therefore, the analog-signal slew-rate limit beyond which an MN5290 requires a T/H is equal to $\Delta V/\Delta t = 0.61mV/36\mu sec = 16.94$ V/sec. If one prefers to think in terms of sinusoidal bandwidths, one concludes that a 36μsec, 14-bit A/D cannot accurately digitize a sinewave whose instantaneous slew rate exceeds 16.94V/sec. For a given sine wave $v(t) = A\sin\omega t$, the maximum slew rate will equal $\Delta V/\Delta t\ (max) = A\omega = 2\pi Af$. If A = 10V and $\Delta V/\Delta t\ (max) = 16.94V/sec$, then f(max) = 0.27Hz. In summary, the MN5290 or any similar successive approximation type A/D operated without a T/H (S/H) cannot be expected to accurately and linearly digitize a ± 10V sine wave with a frequency above 0.27Hz. The A/D will exhibit accuracy and linearity errors around the max slew rate point (zero crossing) of the sine wave. A properly selected T/H (S/H) in front of a given A/D converter will increase the permitted slew rate (bandwidth) by a factor equal to the ratio of the A/D conversion time divided by the T/H aperture jitter. The T/H may reduce system throughput, however, since T/H acquisition and transient settling times will have to be added to A/D conversion time to determine how often digital output data can be updated.

There are four major considerations when choosing a T/H to operate with the MN5290 or MN5291. The T/H must have an input/output linearity commensurate with that of the chosen A/D. The T/H must be capable of and clearly specify acquisition and track-to-hold transient settling times to ± 0.003% FSR (± ½LSB for MN5290 short-cycled to 14 bits) or to ± 0.006% FSR (± ½LSB for MN5291 short-cycled to 13 bits). The T/H's output droop in the hold mode must be low enough so the held signal does not change more than ± ½LSB during the A/D conversion time. For an MN5290 operating on its ± 10V range and short cycled to 14 bits, this droop limit is 0.61mV/36μsec = 16.94μV/μsec. For an MN5291 operating on its ± 10V range and short cycled to 13 bits, this droop limit is 1.22mV/34μsec = 36μV/μsec. Lastly, the T/H

feedthrough attenuation must be such that no more than ± ½LSB of changing input signal feeds through during the conversion period. For use with a 14-bit MN5290, the T/H should have at least 84dB of feedthrough attenuation at appropriate frequencies. For use with a 13-bit MN5291, the T/H should have at least 78dB of feedthrough attenuation.

When actually implementing the T/H-A/D connection, there are two important timing considerations. When commanded to the signal acquisition mode (track mode) the T/H must be given enough time to acquire a new signal to within ± ½LSB of final value, and when commanded back to the hold mode, the T/H must be given enough time to permit its output transient to settle to within ± ½LSB of final value before initiating a conversion. This second consideration is often overlooked. When a T/H or S/H is commanded from the signal acquisition mode to the hold mode, a transient (glitch) invariably occurs, and the transient should be allowed to decay sufficiently before an A/D conversion is initiated. The relevant T/H specification may be called Track to Hold Transient Settling Time, Transient Settling Time or simply Settling Time. It is important to recall that for most successive approximation type A/D converters, the MSB is not set to its final value until 1 full clock period after a conversion has been initiated, and the transient must have decayed before that time. In the MN5290 for example (see Timing Diagram), the MSB is not set to its final value until 1 full clock period (2.4μsec typical) after the falling edge of the start convert command. If the transient of the selected T/H decays to within ± ½LSB of the appropriate resolution in less than 2.4μsec, the falling edge of the convert command can be used to drive the T/H into the hold mode.

Figure 1 (below) shows just such a configuration. When the start command is high, the T/H is in the tracking (signal acquisition) mode. The falling edge of the start command puts the T/H into the hold mode and simultaneously initiates the conversion operation. The MSB is set to its final value 1 clock period later, and the switching transient of the selected T/H must decay sufficiently during that time. The duration of the start convert command must be long enough to accommodate the acquisition time of the chosen T/H.

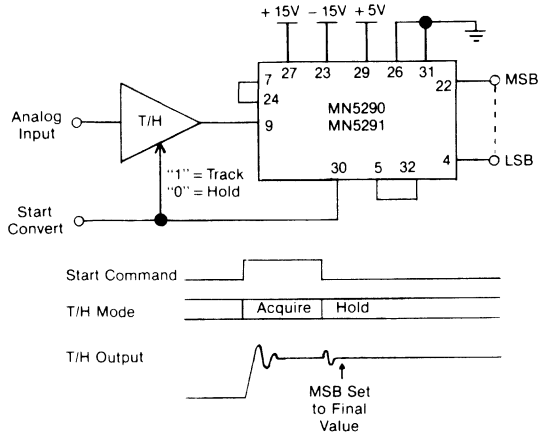


Figure 1. If controlling the T/H with the converter start pulse, the pulse must be wide enough to accomodate the acquisition time of the chosen T/H.

Another popular technique is to control the T/H's operation with the A/D converter's status line. This is demonstrated in Figure 2 below. For the MN5290 and MN5291, the status output is high during a conversion and drops low when a conversion is complete. The rising edge of status at the beginning of a conversion is used to command the T/H into the hold mode. As before, the T/H transient will have to decay before the A/D makes its MSB decision. The falling edge of status at the end of a conversion drives the T/H back into the track mode. The time between the falling edge of status and the falling edge of the next start convert pulse (the rising edge of the next status pulse) must be long enough to accomodate the acquisition time of the selected T/H.

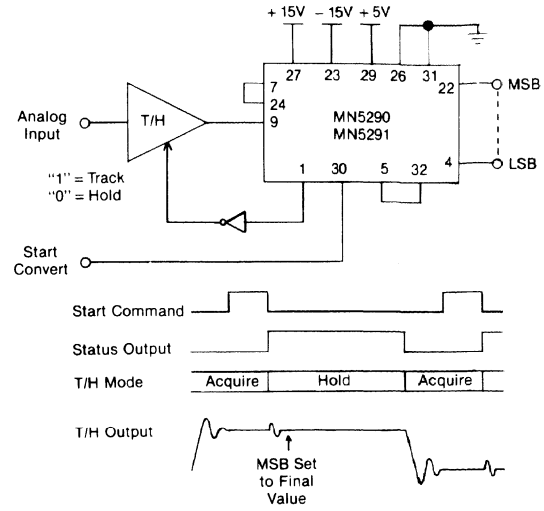


Figure 2. If controlling the T/H with the converter status output, the time between conversions must be long enough to accomodate the acquisition time of the chosen T/H.

If the MN5290 or MN5291 is to be operated in a continuously converting mode, there will not be enough time between conversions for most T/H's to acquire a new signal to the appropriate accuracy. In this situation, the falling edge of status at the end of each conversion can be used to fire a one-shot whose output can be both the start convert and T/H command signals. The duration of the one-shot must be long enough to accomodate the acquisition time of the chosen T/H.

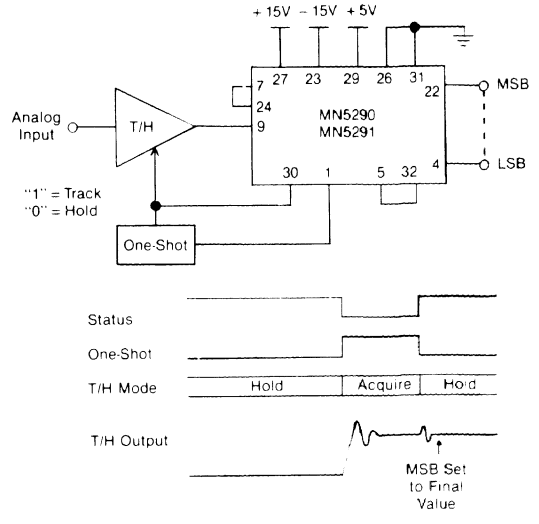


Figure 3. If continuously converting, a one-shot may be required to generate the start and T/H command pulses

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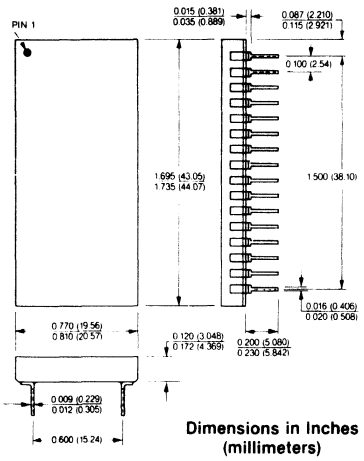
MN5295
MN5296

17μsec, 16-Bit
EXTENDED TEMPERATURE
A/D CONVERTERS

FEATURES

- 16-Bit Resolution
- 17μsec Max Conversion Time
- 14-Bit Performance Guaranteed Over Temperature (MN5295)
- ±0.003% FSR Maximum Linearity Error (MN5295)
- Serial and Parallel Outputs
- 6 User-Selectable Input Ranges
- 1.2 Watts Maximum Power Consumption
- Standard 32-Pin Double DIP
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

32 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

High resolution, high speed, small package and the ability to operate over extended temperatures (including −55°C to +125°C) are brought together in the MN5295 and MN5296. These TTL-compatible, 16-bit, DIP-packaged A/D converters guarantee 17μsec maximum conversion time (for 16 bits); 1.2 Watts maximum power consumption; and ±0.003%FSR maximum integral linearity error. Over temperature, MN5295 guarantees 14-bit "no missing codes", and MN5296 guarantees the same for 13-bits. Each device is packaged in a standard, 32-pin, double-wide, hermetic, ceramic DIP—not the triple-wide DIP's of most other 16-bit A/D's.

MN5295 and MN5296 are complete with internal clock and reference, and each has 6 user-selectable input voltage ranges. Output data is straight binary coded for unipolar input ranges and offset binary coded for bipolar input ranges and is available in both serial and parallel formats.

MN5295 and MN5296 16-bit A/D converters were specifically designed for use in military/aerospace and harsh-environment industrial applications that demand fully guaranteed, high-speed, high-resolution performance over extended operating temperature ranges. They are ideal for applications requiring true 14 (MN5295) or 13-bit (MN5296) performance over temperature. Applications will be found in military instrumentation, ATE, servo control systems and industrial robotic position sensing systems. MN5295 and MN5296H/B are available with Environmental Stress Screening while MN5295 H/B CH and MN5296 H/B CH are screened in accordance with MIL-H-38534. Contact factory for availability of "CH" device types.

Model Number	Temperature Range for Guaranteed No Missing Codes	
MN5295	14 Bits	0°C to +70°C
MN5295H	14 Bits	−55°C to +125°C
MN5295H/B	14 Bits	−55°C to +125°C
MN5295H/B CH	14 Bits	−55°C to +125°C
MN5296	13 Bits	0°C to +70°C
MN5296H	13 Bits	−55°C to +125°C
MN5296H/B	13 Bits	−55°C to +125°C
MN5296H/B CH	13 Bits	−55°C to +125°C

MICRO NETWORKS
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MN5295 MN5296 HIGH-SPEED 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5295, MN5296	0°C to +70°C
MN5295H, H/B, MN5296H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 27)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 23)	+0.5 to −18 Volts
+5V Supply (+Vdd, Pin 29)	0 to +7 Volts
Analog Inputs (Pins 8 and 9)	±22 Volts
Digital Inputs (Pins 30 and 32)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5295 H/B CH

- Select MN5295 or MN5296.
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 10, 20 ±2.5, 5, 10		Volts Volts
Input Impedance (Note 2): 0 to +5V, ±2.5V 0 to +10V, ±5V 0 to +20V, ±10V		2.5 5 10		kΩ kΩ kΩ
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			+40 −1.6	μA mA
TRANSFER CHARACTERISTICS (Note 3)				
Resolution		16		Bits
Integral Linearity Error (Note 4): Initial (+25°C): MN5295 MN5296 Over Temperature (Note 5): MN5295 MN5296		±0.0015 ±0.003 ±0.003 ±0.006	±0.003 ±0.006 ±0.006 ±0.012	%FSR %FSR %FSR %FSR
Differential Linearity Error (Note 4): MN5295 MN5296		±0.003 ±0.006	±0.006 ±0.012	%FSR %FSR
Temperature Range for Guaranteed No Missing Codes MN5295 (14 bits), MN5296 (13 bits) MN5295H (14 bits), MN5296H (13 bits)	 0 −55		 +70 +125	 °C °C
Full Scale Absolute Accuracy Error (Note 6): Unipolar: Initial (+25°C) Over Temperature (Note 5) Bipolar: Initial (+25°C) Over Temperature (Note 5)		 ±0.075 ±0.15 ±0.1 ±0.2	 ±0.15 ±0.3 ±0.2 ±0.4	 %FSR %FSR %FSR %FSR
Unipolar Offset Error (Notes 7, 8): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.1 ±0.2 ±15	%FSR %FSR ppm of FSR/°C
Bipolar Zero Error (Notes 7, 9): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.12 ±0.2 ±15	%FSR %FSR ppm of FSR/°C
Gain Error (Notes 7, 10): Initial (+25°C) Over Temperature (Note 5) Drift		±0.05 ±0.1 ±5	±0.1 ±0.2 ±20	% % ppm/°C
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 11): Unipolar Ranges Bipolar Ranges		SB OB		
Logic Levels: Logic "1" ($I_{source} \leq 320\mu A$) Logic "0" ($I_{sink} \leq 3.2mA$)	+2.4		 +0.4	Volts Volts
REFERENCE OUTPUT				
Internal Reference: Voltage Accuracy Tempco (Note 2) External Current (Notes 2, 12)		+10.000 ±0.025 ±5	 ±0.1 1	Volts % ppm/°C mA
DYNAMIC CHARACTERISTICS				
Conversion Time (14 Bits/16 Bits) (Note 13)		14/16	15/17	μsec

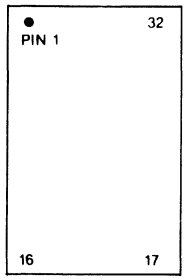
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: ±15V Supplies +5V Logic Supply	±14.55 +4.75	±15 +5	±15.45 +5.25	Volts Volts
Power Supply Rejection (Note 14): +15V Supply −15V Supply +5V Logic Supply		±0.005 ±0.005 ±0.001	±0.02 ±0.02 ±0.01	%FSR/% Supply %FSR/%Supply %FSR/% Supply
Current Drains: +15V Supply −15V Supply +5V Logic Supply		+35 −24 +12	+42 −32 +18	mA mA mA
Power Consumption		945	1200	mW

SPECIFICATION NOTES:

1. Listed specifications apply for all part numbers unless specifically indicated. Detailed timing specifications appear in the Timing sections of this data sheet.
2. These parameters are listed for reference only and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for 0 to +20V or ±10V operation has a 20V FSR. A unit connected for 0 to +10V or ±5V operation has a 10V FSR etc. 1 LSB for 16 bits is equivalent to 0.00153%FSR. 1 LSB for 14 bits is equivalent to 0.0061%FSR.
4. ±0.003%FSR is equivalent to ±½ LSB for 14 bits. ±0.006%FSR is equivalent to ±½ LSB for 13 bits.
5. Listed specifications apply over the 0°C to +70°C temperature range for standard products and over the −55°C to +125°C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Initial unipolar offset (bipolar zero) and gain errors are adjustable to zero with the use of external potentiometers.
8. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just chages from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN5295/5296 on a unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
9. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN5295/5296 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
10. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 1111 to 1111 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0000 0001 to 0000 0000 0000 0000.
11. SB = straight binary. OB = offset binary. See table of transition voltages in section labeled Digital Output Coding.
12. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 7 connected to pin 24), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
13. Conversion is initiated on the falling edge of the start convert command, and conversion time is defined as the width of the status (end of conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14-bit conversions. See Timing Diagram.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

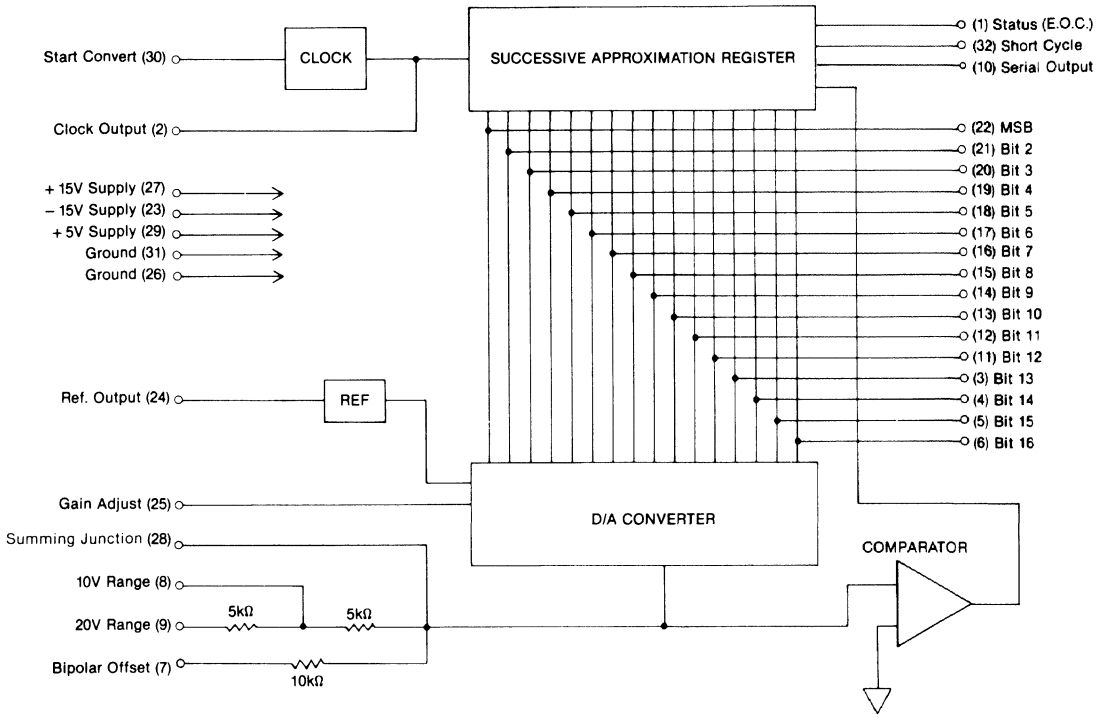
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	Status (E.O.C.)	32	Short Cycle
2	Clock Output	31	Ground
3	Bit 13	30	Start Convert
4	Bit 14	29	+5V Supply (+V_{dd})
5	Bit 15	28	Summing Junction
6	Bit 16 (LSB)	27	+15V Supply (+V_{cc})
7	Bipolar Offset	26	Ground
8	10V Input Range	25	Gain Adjust
9	20V Input Range	24	Reference Output (+10V)
10	Serial Output	23	−15V Supply (−V_{cc})
11	Bit 12	22	Bit 1 (MSB)
12	Bit 11	21	Bit 2
13	Bit 10	20	Bit 3
14	Bit 9	19	Bit 4
15	Bit 8	18	Bit 5
16	Bit 7	17	Bit 6

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—See Block Diagram. The successive approximation register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the analog-to-digital converter (A/D) and the digital drive for the A/D's internal digital-to-analog converter (D/A). The falling edge of a start convert pulse applied to pin 30 turns on the A/D's internal clock and resets the SAR. In this state, the output of the MSB flip flop is set to logic "0"; the outputs of the other bit flip flops are set to a logic "1"; and the Status (pin 1) is set to logic "1" (see Timing Diagram). The Start Convert must now remain low for the conversion to continue.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after Start Convert has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 16) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

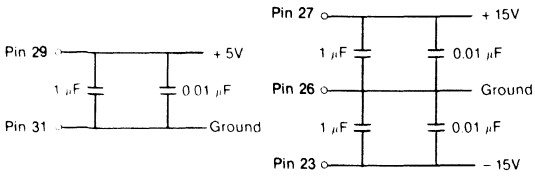
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5295 and MN5296. The units' two ground pins (pins 26 and 31) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a nonpolarized 0.01μF ceramic bypass capacitor should be connected between pins 26 and 31 as close to the unit as possible and wide conductor runs employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 7 (Bipolar Offset), 8 and 9 (Analog Inputs), 28 (Summing Junction) and 25 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when using these inputs. Input signal lines should be as short as possible. In bipolar operation, where pin 7 is connected to pin 24, a short jumper should be used. If bipolar offsetting is not used, pin 7 should be grounded to pin 26. For external offset adjustment, the 1.8 megohm resistor should be located as close to pin 28 as possible. A 0.01μF ceramic capacitor should be connected between pin 25 and analog ground as close to the package as possible.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN5295 and MN5296. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

If short cycling is not used, the Short Cycle pin (pin 32) must be connected to +5V (pin 29).

POWER SUPPLY DECOUPLING



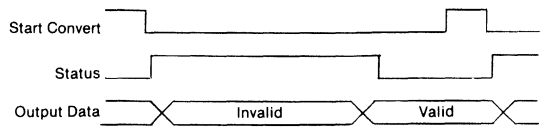
START CONVERT—The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec. The falling edge of the Start Convert signal resets the converter and turns on the internal clock. Status going low at the end of a conversion turns off the internal clock. If the Start Convert input is brought high after a conversion has been initiated, the internal clock will be disabled halting the conversion. If the Start Convert input is then brought low, the original conversion will continue with a possible error in the output bit that was about to be set when the internal clock was stopped.

SHORT CYCLING—For applications requiring fewer than 16 bits of resolution, the MN5295 and MN5296 can be truncated or short cycled at the desired number of bits with a proportionate decrease in conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle pin (pin 32). For example, to truncate at 14 bits, connect pin 5 (Bit 15) to pin 32; converting will stop and Status will go low after bit 14 has been set. For any length conversion, the falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs.

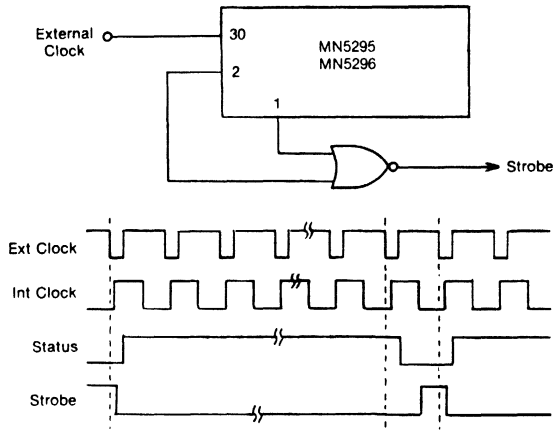
EXTERNAL CLOCK—An external clock may be connected to the Start Convert input. This external clock must consist of negative-going pulses 100 to 200nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 17 clock cycles. The internal clock will be disabled whenever Start Convert is held high. When using an external clock, a Start Convert command is unnecessary. The converter will begin to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after Status has gone low signaling the end of the previous conversion. When continuously converting in this manner, Status will go low for one external clock period following the completion of each conversion.

SERIAL OUTPUT—Serial data is available only during the conversion process. Format is NRZ with the MSB occurring first. Serial data is coded the same as parallel output data, and it is synchronous with the internal clock as shown in the Timing Diagram. Each data bit becomes valid typically 120nsec after each rising clock edge and remains valid for the full clock period. Therefore, falling clock edges can be used to strobe serial data into output registers.

STATUS OUTPUT—The Status or End of Conversion (E.O.C.) output will be set to a logic "1" by the falling edge of the Start Convert signal; will remain high during conversion; and will drop to a logic "0" when conversion is complete. The falling edge of Status is internally delayed a minimum of 20nsec to ensure that all parallel output data, including the LSB, is valid by the time the edge occurs. If parallel data is to be latched into external registers, this delay should be long enough to accomodate the set-up time requirements of the latch such that Status can be used to strobe the latch. If the delay is not long enough, the Status can be delayed with gate delays or the latch can be strobed with the leading edge of the next start convert pulse. See diagram below.

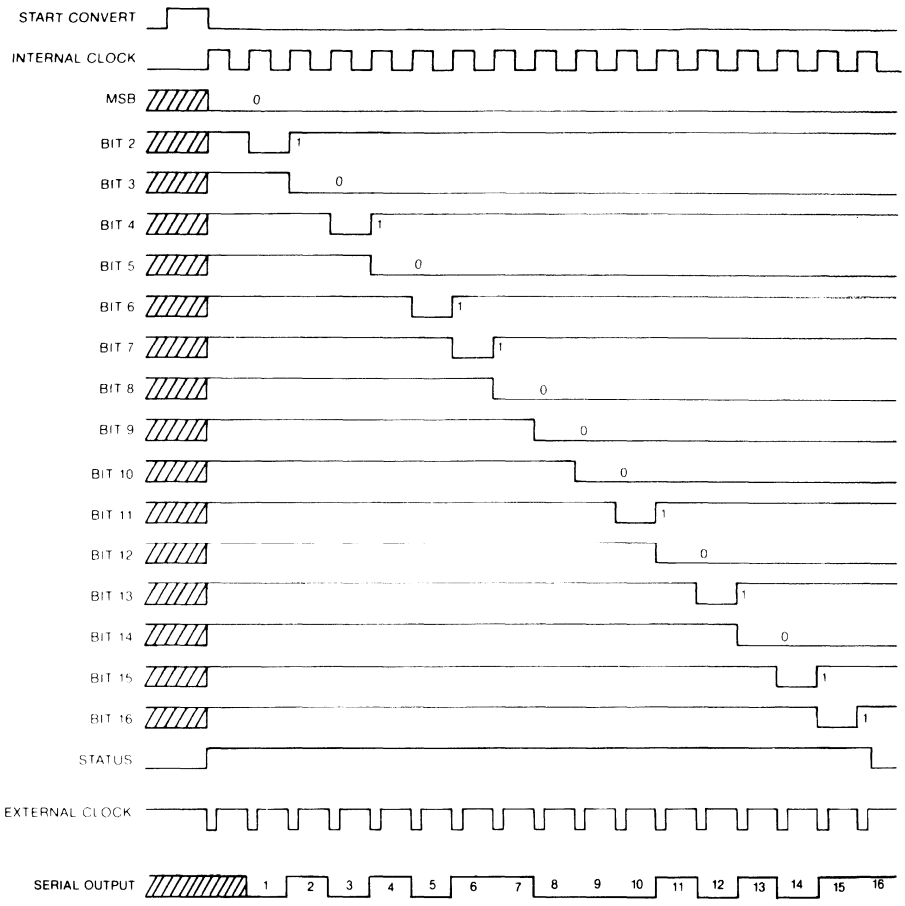


If continuously converting with an external clock, Status can be NORed with the internal clock, as shown below, to produce a positive strobe pulse approximately ½ period wide, approximately ½ period after Status has gone low. The rising edge of this pulse can be used to latch data after each conversion. Recall that the falling edges of the external clock pulses generate rising edges of the internal clock and that these two clocks appear 180 degrees out of phase. The delay from the rising edge of the internal clock to the rising edge of Status is typically 120nsec. See Timing Diagram and the section labeled External Clock.



INTERNAL REFERENCE—The MN5295 and MN5296 contain an internal, low-drift 10V reference that is laser trimmed to an initial accuracy of ±0.1%. The reference is pinned out on pin 24 and can supply up to 1mA beyond the current required for bipolar operation (pin 24 connected to pin 7). If the external load is expected to vary during converter operation or if the internal reference is to be used to drive external circuitry at elevated temperatures, the reference output should be buffered externally.

TIMING DIAGRAM



SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise specified)

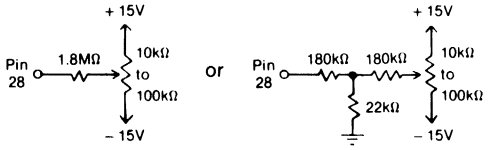
DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (14 Bits/16 Bits)		14/16	15/17	μsec
Internal Clock Frequency (Note 8)		1		MHz
Start Convert Positive Pulse Width (Note 8)	50			nsec
Delay Falling Edge of Start to (Note 8): Status = "1"		50	80	nsec
Clock Output = "1"		20	50	nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20	120	200	nsec
Delay LSB Valid to Falling Edge of Status (Note 8)	20	60		nsec

TIMING DIAGRAM NOTES

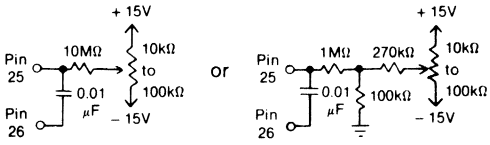
1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Data will be valid 60nsec before the Status (E.O.C.) output goes low and will remain valid until another conversion is initiated.
5. When using an external clock, the converter will continuously convert. Each conversion will be initiated by the falling edge of the first external clock pulse following E.O.C.'s going low at the end of the previous conversion. See External Clock.
6. When the converter is initially "powered up", it may come on at any point in the conversion cycle.
7. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Connect pin 5 (Bit 15) to pin 32 (Short Cycle) for 14 bit conversions.
8. These parameters are listed for reference only and are not tested.

)PTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS — ıitial zero and gain errors may be trimmed to zero using xternal potentiometers as shown in the following diagrams. ıdjustments should be made following warmup, and to avoid ıteraction, zero should be adjusted before gain. Fixed ɜsistors can be ±20% carbon composition or better. Multi-ɹrn potentiometers with TCR's of 100ppm/°C or less are rec-mmended to minimize drift with temperature. If these ad-ɹstments are not used, pin 28 should be connected as escribed in the Range Selection section.

ERO ADJUSTMENT—Connect the zero adjust potentiom-ter as shown. For unipolar ranges, apply the input voltage at /hich the 0000 0000 0000 0000 to 0000 0000 0000 0001 transi-on is ideally supposed to occur. While continuously convert-ıg, adjust the zero potentiometer until all bits are "0" and the SB "flickers" on and off. For bipolar ranges, apply the input oltage at which the 0111 1111 1111 1111 to 1000 0000 0000 000 transition is ideally supposed to occur. While continu-usly converting, adjust the zero potentiometer until all bits flicker" on and off.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off.



)IGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+ F.S.	+ F.S.	1111 1111 1111 1111
+ F.S. − ½ LSB	+ F.S. − ½ LSB	1111 1111 1111 111ø*
+ ½ F.S. + ½ LSB	+ ½ LSB	1000 0000 0000 000ø*
+ ½ F.S. − ½ LSB	− ½ LSB	øøøø øøøø øøøø øøøø*
+ ½ F.S. − ½ LSB	− ½ LSB	0111 1111 1111 111ø*
+ ½ LSB	− F.S. + ½ LSB	0000 0000 0000 000ø*
0	− F.S.	0000 0000 0000 0000

)DING NOTES:

. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV. 1LSB for 14 Bits = 610.4μV.
!. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV. 1LSB for 14 Bits = 1.22mV.
i. For unipolar ranges, the coding is straight binary.
·. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5295/MN5296 continuously converting, the output bits indicated as ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE					
	0 to + 5V	0 to + 10V	0 to + 20V	± 2.5V	± 5V	± 10V
Connect Pin 7 to Pin	26	26	26	24	24	24
Connect Pin 9 to Pin	28	Open	Input	28	Open	Input
Connect Pin 28 to Pin	9	Open	Open	9	Open	Open
Connect Input to Pin	8	8	9	8	8	9
Input Impedance (KΩ)	2.5	5	10	2.5	5	10

EXAMPLE: For the ± 10V range, the transition from output code 1111 1111 1111 1111 to output code 1111 1111 1111 1110 (or vice versa) will ideally occur at an input of + 9.999542V (+ F.S. − ½LSB). Subsequently, any voltage greater than + 9.999542V will give a digital output of all "1's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of − 0.000153 volts. The 0000 0000 0000 0000 to 0000 0000 0000 0001 transition will occur at − 9.999847V. An input more negative than this level will give all "0's."

)SING TRACK-HOLD AMPLIFIERS WITH /IN5295 AND MN5296 A/D CONVERTERS

ligh-speed, high-resolution, successive approximation type /D converters, such as MN5295/5296, are severely limited in ıeir ability to accurately convert dynamic input signals. tated differently, these high-resolution, high-throughput igitizers have limited analog input bandwidth capabilities. ı high-speed data-acquisition or digital-signal-processing)SP) applications in which high resolution, high throughput nd high input bandwidth are required, a track-hold (T/H) mplifier must be used to overcome the A/D's inherent band-ıidth limitations. The T/H has the ability to follow (track) the igh-speed input signal until it is time to convert it. When ommanded into the hold mode, the T/H instantaneously freezes" the input signal and holds it constant while the A/D erforms its conversion.

he MN374 High-Speed, High-Resolution T/H Amplifier has een designed specifically as a companion T/H for MN5295/ 296 A/D's. A typical application is described below. Please ɜe the MN5290/5291 data sheet for a general discussion of nportant factors to consider when selecting a T/H for use ith higher resolution A/D's.

For slower speed A/D converters, the most popular technique used to control the T/H's operation is to drive the T/H directly with the A/D's status line. For virtually all high-resolution A/D's in use today, including MN5295/5296, this technique does *not* work because the T/H's track-to-hold transients will not reliably settle fast enough. The application described below is a much more cautious way to control the T/H-A/D timing because it uses a timed one-shot to delay the start of the A/D conversion. The circuit allocates a predetermined amount of time for the track-to-hold transient to fully settle before initiating the A/D conversion. After the conversion has been completed, the circuit immediately drives the T/H back into the track mode.

The principles discussed below are general and can be used for virtually any T/H-A/D combination. The system is run by an externally applied clock whose frequency determines the overall sampling/digitizing rate. Please refer to the timing and schematic diagrams below as well as the MN374 T/H data sheet.

The system consists of the A/D, the T/H, a single one-shot and a dual flip-flop. The falling edge of the system clock triggers the 74LS123 one-shot, and the system clock can have any duty cycle as long as it has a minimum positive pulse width of

50nsec to accommodate the setup-time requirement of the one-shot.

The one-shot produces a 500nsec pulse, and both the Q and $\overline{Q}$ outputs are utilized. The Q output becomes the start pulse for the MN5295/5296, and the $\overline{Q}$ output drives the set pin of the first half of the 74LS74 flip-flop. The $\overline{Q1}$ output of the flip-flop controls the operational mode of the MN374 T/H. The falling edge of the $\overline{Q}$ output of the 74LS123 asynchronously sets the flip-flop driving its Q1 output high and its $\overline{Q1}$ output low. The MN374, which has an active-low control line, is immediately driven into its hold mode by the falling edge of $\overline{Q1}$.

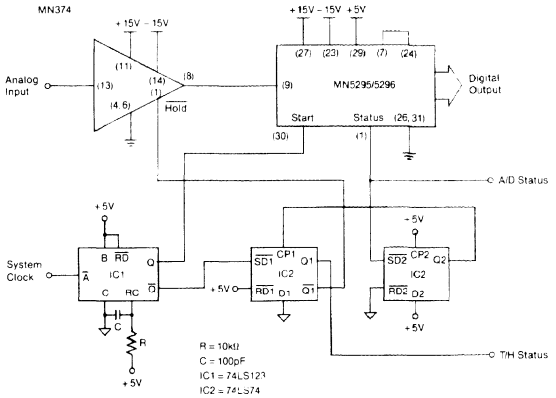
The pulse width of the 74LS123 has been selected so that there is now ample time for the MN374 track-to-hold transient to fully decay before the A/D conversion begins. After 500nsec, the Q output of the one-shot drops to "0" initiating the A/D conversion, and driving the Status output (pin 1) of the A/D to a "1". The T/H remains in hold because the rising edge of the $\overline{Q}$ output of the one-shot does not affect the first flip-flop. The rising edge of Status asynchronously resets the second flip-flop driving the Q2 output low.

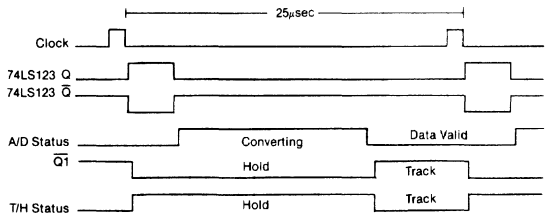
The T/H remains in the hold mode for the next 17μsec as the A/D completes its conversion. At the end of the conversion, the A/D's Status line drops to a "0", and this sets the second flip-flop. The Q2 output goes high clocking the first flip-flop which has a "0" on its D line. This forces the Q1 output low and the $\overline{Q1}$ output high driving the T/H back into the signal-acquisition (track) mode.

The status of this system can be monitored at a number of different points. Whenever pin 1 (Status) of MN5295/5296 is a logic "1", the A/D is performing a conversion, and output data is not valid. The falling edge of this line signals that the conversion is complete and that output data is now valid. The Q1 output of the first flip-flop can be used to monitor the T/H. Whenever this line is a "1", the T/H is in the hold mode. When it is a "0", the T/H is in the track mode. The falling edge here also indicates that a conversion has just been completed and that output data is now valid. If an external latch is to be used to clock data away from MN5295/5296, either of the falling edges described above may be used to strobe the latch.

Remember that the above application does not automatically take care of the T/H acquisition time and that this time must be allowed for in determining the external clock period. If the MN5295/5296 requires 17μsec to make a conversion, and the T/H requires 4μsec for acquisition time, adding 2μsec of overhead time yields a period of 23μsec. That means the system can be clocked at 43kHz and still be guaranteed to meet full accuracy and linearity performance.

It is unnecessary to have the 74LS123 one-shot in the application if the externally applied clock can be made to be a series of 50nsec-wide positive pulses occurring at a 43kHz rate. In other words, if the clock can be made to look like the output of the one-shot in our timing diagram, it is unnecessary to have the one-shot. The clock can drive the MN5295/5296 directly, and it can be inverted to drive the 74LS74.





ORDERING INFORMATION

Part Number	Specified Temperature Range	Conversion Time (μsec, Max.)	Integral Linearity (%FSR, Max.)		No Missing Codes Over Temperature	Power Consumption (mW, Max.)	Package
			+25°C	Temp.			
MN5295	0°C to +70°C	17	±0.003	±0.006	14 Bits	1200	32-pin DIP
MN5295H	−55°C to +125°C	17	±0.003	±0.006	14 Bits	1200	32-pin DIP
MN5295H/B	−55°C to +125°C	17	±0.003	±0.006	14 Bits	1200	32-pin DIP
MN5296	0°C to +70°C	17	±0.006	±0.012	13 Bits	1200	32-pin DIP
MN5296H	−55°C to +125°C	17	±0.006	±0.012	13 Bits	1200	32-pin DIP
MN5296H/B	−55°C to +125°C	17	±0.006	±0.012	13 Bits	1200	32-pin DIP

Contact factory for availability of CH device types.

MICRO NETWORKS

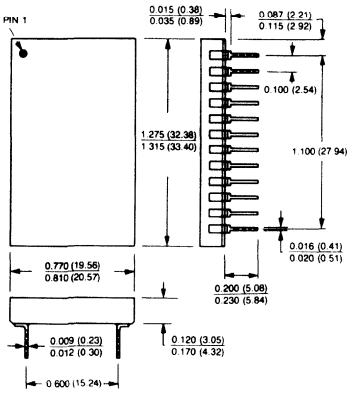
MN5825

COMPLETE
1μsec, 8-Bit
A/D CONVERTER

FEATURES

- **Complete A/D with Internal Clock and Reference**
- **1μsec Maximum Conversion Time**
- **Logic-Controlled Unipolar or Bipolar Operation**
- **±1/2LSB Max Integral Linearity Error**
- **No Missing Codes Guaranteed Over Temperature**
- **Small 24-Pin DIP**
- **Pin Compatible ADC815/825**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5825 is a complete, high-speed, 8-bit A/D converter. It contains its own internal reference and clock and guarantees a maximum 1μsec conversion time. This is a successive approximation type A/D, and unlike other A/D's in its speed class, it does not require heavy external support circuitry (references, input buffers, trimmers, etc.). It is functionally laser trimmed for gain, offset and linearity completely eliminating the need for external trimming potentiometers. MN5825 is pin and function compatible with other ADC825 8-bit A/D's and offers greater reliability resulting from an improved, lower-chip-count design.

MN5825 guarantees ±½LSB maximum integral linearity error, and "no missing codes" is guaranteed over either the 0°C to +70°C or −55°C to +125°C operating temperature range. Initial offset error is guaranteed not to exceed ±½LSB. Output data is available in either parallel or serial format. Digital output coding is straight binary for unipolar input ranges and either offset binary or two's complement for bipolar input ranges.

MN5825 is hermetically sealed in an industry-standard, 24-pin, ceramic DIP and offers 3 unipolar (0 to +5V, 0 to +10V and 0 to +20V) and 3 bipolar (±2.5V, ±5V and ±10V) input ranges. Each unit has the unique ability to be switched from unipolar to bipolar operation with a TTL-compatible control signal applied to one of the device pins.

The MN5825 family includes 5 models as summarized below. For military/aerospace or harsh-environment commercial/industrial applications, MN5825H/B CH is fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

Model Number	Conversion Time	Specified Temperature Range
MN5825	1μsec	0°C to +70°C
MN5825E	1μsec	−25°C to +85°C
MN5825H	1μsec	−55°C to +125°C
MN5825H/B	1μsec	−55°C to +125°C
MN5825H/B CH	1μsec	−55°C to +125°C

MICRO NETWORKS
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MN5825 HIGH-SPEED 8-Bit A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN5825	0°C to +70°C
MN5825E	−25°C to +85°C
MN5825H, 5825H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 3)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 4)	+0.5 to −18 Volts
+5V Supply (+Vdd, Pin 15)	−0.5 to +7 Volts
Analog Inputs (Pins 9, 10 and 11)	±25 Volts
Digital Inputs (Pins 8 and 12)	0 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5825H/B CH

Standard Part is specified for 0°C to +70°C operation.
Add "E" suffix for specified −25°C to +85°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" to "H" devices for Environmental Stress Screening.
Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

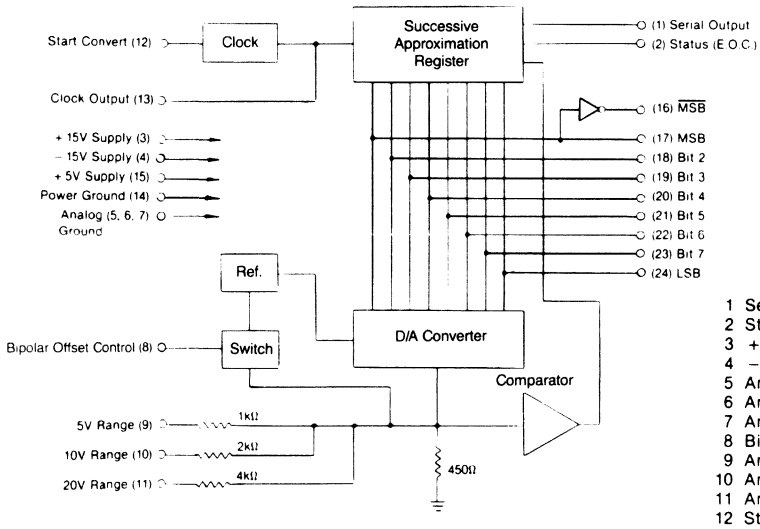
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar		0 to +5, 10, 20		Volts
Bipolar		±2.5, ±5, ±10		Volts
Input Impedance: 0 to +5V, ±2.5V		1.34		kΩ
0 to +10V, ±5V		2.29		kΩ
0 to +20V, ±10V		4.27		kΩ
DIGITAL INPUTS (Start Convert, Bipolar Offset)				
Logic Levels All Inputs: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Start Convert: Logic "1" (V_{IH} = +2.4V)			+80	μA
Logic "0" (V_{IL} = +0.4V)			−3.2	mA
Bipolar Offset Control (Note 4): Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
TRANSFER CHARACTERISTICS (Note 5)				
Integral Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 1)			±½	LSB
Differential Linearity Error		±½	±1	LSB
No Missing Codes	Guaranteed Over Temperature			
Unipolar Zero Error (Note 6): Initial (+25°C)		±¼	±½	LSB
Drift (Note 1)		±100	±150	μV/°C
Bipolar Zero Error (Note 7): Initial (+25°C)		±¼	±1	LSB
Drift (Note 1)		±25	±50	ppm of FSR/°C
Gain Error (Note 8): Initial (+25°C)		±1	±3	LSB
Drift (Note 1)		±50	±100	ppm/°C
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 9): Unipolar Ranges		SB		
Bipolar Ranges		OB, TC		
Logic Levels: Serial, Parallel, Status: Logic "1" ($I_{SOURCE} \leq 160\mu A$)	+2.4			Volts
Logic "0" ($I_{SINK} \leq 4mA$)			+0.4	Volts
Clock: Logic "1" ($I_{SOURCE} \leq 240\mu A$)	+2.4			Volts
Logic "0" ($I_{SINK} \leq 4mA$)			+0.4	Volts
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 10)			1	μsec
Start Convert Pulse Width (Note 2)	50		100	nsec
Delay Rising Edge of Start Convert to Status=1		40		nsec
Delay Falling Edge of Clock to Output Data Valid (Parallel, Serial, Status)		35		nsec
Delay Falling Edge of Status to LSB Valid		35		nsec
POWER SUPPLIES				
Power Supply Range: ±15V Supply	±14.5	±15	±15.5	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection (Note 3): +15V Supply		±0.004		%FSR/%Vs
−15V Supply		±0.004		%FSR/%Vs
+5V Supply		±0.001		%FSR/%Vs
Current Drain: +15V Supply		+25	+35	mA
−15V Supply		−10	−15	mA
+5V Supply		+80	+100	mA
Power Consumption		925	1250	mW

SPECIFICATION NOTES:

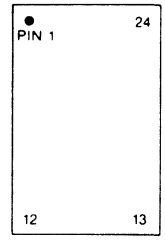
1. Listed specifications apply over the 0°C to +70°C temperature range for MN5825, over the −25°C to +85°C temperature range for MN5825E and over the −55°C to +125°C temperature range for MN5825H and H/B.
2. Rising edge of start convert pulse resets converter. Falling edge starts clock and initiates conversion. See Timing Diagram.
3. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0001 to 0000 0000 output transitions occur verses a change in power-supply voltage.
4. Apply logic "1" for bipolar operation, logic "0" for unipolar operation.
5. FSR stands for full scale range and is equivalent to the nominal peak-to-peak voltage of the selected input range, i.e., FSR=5 Volts for 0 to +5V and ±2.5V ranges. FSR=10 Volts for 0 to +10V and ±5V ranges. FSR=20 Volts for 0 to +20V and ±10V ranges. For an 8-bit converter, 1LSB=0.39%FSR.
6. Unipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 when operating on a unipolar range. See Digital Output Coding.
7. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating on a bipolar range. See Digital Output Coding.
8. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 0000 0000 to 0000 0001 to the voltage at which it changes from 1111 1110 to 1111 1111.
9. Coding applies for both serial and parallel outputs. Serial output is in standard NRZ format with MSB appearing first. SB=straight binary. OB=offset binary. TC=two's complement.
10. Conversion time is defined as the width of Status. Listed specifications assume start convert pulse is 50nsec wide.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



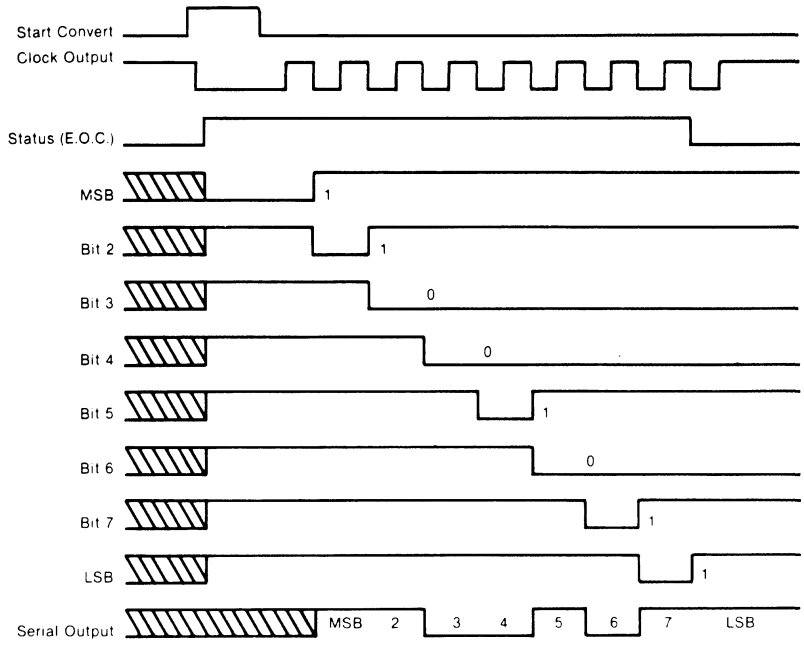
1	Serial Output	24	Bit 8 (LSB)
2	Status (E.O.C.)	23	Bit 7
3	+15V Supply	22	Bit 6
4	−15V Supply	21	Bit 5
5	Analog Ground	20	Bit 4
6	Analog Ground	19	Bit 3
7	Analog Ground	18	Bit 2
8	Bipolar Offset Control	17	Bit 1 (MSB)
9	Analog Input, 5V Range	16	$\overline{\text{Bit 1 (MSB)}}$
10	Analog Input, 10V Range	15	+5V Supply
11	Analog Input, 20V Range	14	Power Ground
12	Start Convert	13	Clock Output

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—See Block Diagram. The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). The rising edge of the start convert pulse applied to pin 12 resets the converter (MSB = 0, all other bits = 1 and Status = 1). The internal clock is enabled and the conversion commences on the falling edge of the start convert pulse. Start convert must remain low during the conversion.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first falling clock edge after the Start has gone low, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator

TIMING DIAGRAM



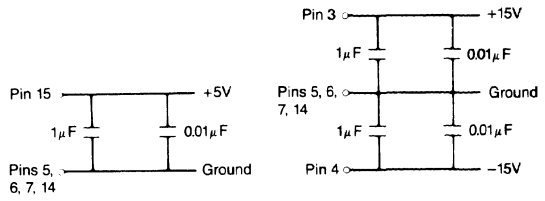
TIMING DIAGRAM NOTES:

1. Operation is shown for the digital output 1100 1011.
2. The Start Convert command must be at least 50nsec wide and must remain low during conversion.
3. The rising edge of Start Convert resets the converter (MSB = 0, other bits = 1, Status = 1). The internal clock is enabled and the conversion cycle commences on the falling edge of the Start Convert signal.
4. Conversion time is defined as the width of the status pulse.
5. The delay from the rising edge of Start Convert to the rising edge of Status is typically 40nsec.
6. Both serial and parallel data bits become valid on the same falling clock edges. Serial data is valid on subsequent rising clock edges, and the edges can be used to clock serial data into receiving registers.

determines whether this value is greater or less than the analog input. On the next falling clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. The successive approximation procedure continues until all the output bits are set. The falling clock edge that sets the LSB (bit 8) also drops the Status Output to a "0" signaling that the conversion is complete and turning off the internal clock. Output data is now valid and will remain so until another conversion is started.

LAYOUT CONSIDERATIONS AND GROUNDING—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from the MN5825. The unit's four ground pins (pins 5, 6, 7, 14) are not connected to each other internally. They must be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large analog ground plane beneath the package.

Power supplies should be decoupled with electrolytic or tantalum and ceramic capacitors located close to the MN5825. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.



POWER SUPPLY DECOUPLING

Analog inut leads should be a short as possible and unused analog inputs must be connected to ground. See Input Range Selection table.

STATUS (E.O.C.)—Status (End of Conversion, E.O.C., pin 2) will be set to a logic "1" 40nsec (typical) after the rising edge of Start Convert; will remain a logic "1" during the conversion; and will be set to a logic "0" when the conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until 35nsec after Status has returned low.

START CONVERT—The rising edge of the start convert signal resets the converter; the MSB is set to a logic "0", the remaining bits are set to a logic "1" and Status (E.O.C.) is set to a logic "1". The converter will remain in the reset state until the start convert signal is brought low. The internal clock is enabled and the conversion commences on the falling edge of the start convert signal. The start convert positive pulse width is 50nsec minimum and must not exceed 100nsec maximum in order to meet the 1μsec conversion time specification. See Timing Diagram.

SERIAL OUTPUT—Serial output data is provided in addition to parallel data and is in standard non-return-to-zero (NRZ) format with the MSB appearing first. Serial output data is coded straight binary (SB) for unipolar ranges and offset binary (OB) for bipolar ranges. Serial data bits become valid on rising clock edges and are delayed one clock pulse from valid parallel data bits. Therefore, rising clock edges may be used to clock serial data into receiving registers.

BIPOLAR OFFSET CONTROL—Bipolar Offset Control (pin 8) is a digital input and must be connected to a logic "0" for unipolar operation or to a logic "1" for bipolar operation. Logic levels are TTL-compatible and loading is 1 TTL load maximum.

ANALOG INPUTS—MN5825 has three analog inputs and input ranges are configured by selecting the desired full scale range and grounding the unused inputs. For example, if a 10V full scale range is desired (±5V or 0 to +10V), the input signal is connected to pin 10, and pins 9 and 11 are hardwired to ground. See Input Range Selection table. Bipolar operation is selected by applying a logic "1" to Bipolar Offset Control (pin 8) and unipolar operation is selected by applying a logic "0". See section labeled Bipolar Offset Control.

INPUT RANGE SELECTION

	Analog Input Voltage Ranges					
Pin Connections	**0 to +5V**	**0 to +10V**	**0 to +20V**	**±2.5V**	**±5V**	**±10V**
Input Impedance (kΩ)	1.34	2.29	4.27	1.34	2.29	4.27
Connect Pin 9 to	Input	Ground	Ground	Input	Ground	Ground
Connect Pin 10 to	Ground	Input	Ground	Ground	Input	Ground
Connect Pin 11 to	Ground	Ground	Input	Ground	Ground	Input
Connect Pin 8 to	Logic "0"	Logic "0"	Logic "0"	Logic "1"	Logic "1"	Logic "1"

INPUT RANGE SELECTION NOTES:
1. Bipolar Offset Control (pin 8) is a digital input and must be connected to a logic "0" for unipolar operation or to a logic "1" for bipolar operation.
2. Unused analog inputs must be connected to ground.

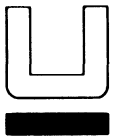
DIGITAL OUTPUT CODING

Analog Input Voltage		Digital Output
0 to +5V, +10V, +20V	**±2.5V, ±5V, ±10V**	**MSB LSB**
+F.S.	+F.S.	1111 1111
+F.S. −3/2LSB	+F.S. −3/2LSB	1111 111Ø
+½F.S. +½LSB	+½LSB	1000 000Ø
+½F.S. −½LSB	−½LSB	ØØØØ ØØØØ
+½F.S. −3/2LSB	−3/2LSB	0111 111Ø
+½LSB	−F.S. +½LSB	0000 000Ø
0	−F.S.	0000 0000

DIGITAL OUTPUT CODING NOTES:
1. For 5 Volts FSR, 1 LSB = 19.5mV.
2. For 10 Volts FSR, 1 LSB = 39mV.
3. For 20 Volts FSR, 1 LSB = 78.1mV.
4. For unipolar ranges, the coding is straight binary.
5. For bipolar ranges, the coding is offset binary or two's complement if $\overline{MSB}$ output is used.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN5825 continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the ±10V range, the transition from output code 1111 1111 to output code 1111 1110 (or vice versa) will ideally occur at an input of +9.883V (+FS − 3/2LSB). Subsequently, any voltage greater than +9.883V will give a digital output of all "1s". The transition from digital output 0111 1111 to 1000 0000 (or vice versa) will ideally occur at an input of −0.039V. The 0000 0000 to 0000 0001 transition will occur at −9.961V. An input more negative than this level will give all "0's."



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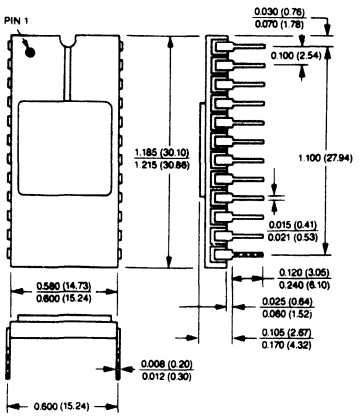
MN5902

8-Bit, 20MHz CMOS FLASH A/D CONVERTER

FEATURES

- **20MHz Sampling Rate**
- **Single +5V Supply Operation**
- **Low Harmonic Distortion**
- **Latched 3-State Outputs**
- **Easy Cascading to 9 Bits**
- **Low 350mW Power Consumption**
- **Small 24-Pin DIP**
- **−55°C to +125°C Operating Temperature Range**
- **Optional Environmental Stress Screening**

24 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5902 is a high-speed, 8-bit monolithic CMOS Flash A/D converter that provides a 20MHz sampling rate over its full operating temperature range. Operating from a single +5V supply, the MN5902 provides high-speed performance while consuming less power than other available 8-bit, 20MHz devices. Its 3-state latched data outputs include an overflow signal that allows easy cascading of two devices to obtain 9-bit resolution.

The MN5902 utilizes 255 CMOS sampling comparators to convert the analog input signal into a digital output word; one additional comparator provides an overflow signal when an input overrange condition occurs. Proprietary circuitry auto-zeros the comparators during each conversion to eliminate any dc offset errors that might arise from comparator mismatches.

The MN5902 operates in a pipelined mode, which allows high sampling rates and helps to eliminate spurious codes. A companion device, the MN5908, operates in a transparent mode, which allows one-shot operation for subranging and sampling applications (see the MN5908 data sheet).

Outstanding performance features of the MN5902 include guaranteed maximum differential and integral linearity specifications as well as no-missing-codes performance over the full operating temperature range. The MN5902 is specified for 0°C to +70°C operation; the MN5902E is specified for −25°C to +85°C operation while the MN5902H is specified for −55°C to +125°C operation. For military/aerospace applications, the MN5902H/B is available with Environmental Stress Screening.

APPLICATIONS

Video Digitizers
RADAR Systems
Pulse Measurement Systems
Subranging A/D Converters
Synchronous Demodulation
Infrared Imaging
Communications
Medical Imaging
Thermal Imaging
Waveform Analyzers
ECM Equipment

This data sheet contains preliminary information regarding the MN5902. Please contact the factory for up-to-date performance and product information.

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MN5902 8-Bit, 20MHz CMOS FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN5902	0°C to +70°C
MN5902H or MN5902H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+5V Supply (Pin 1, 10, 19)	−0.5 to +7.0 Volts
Digital Inputs (Pins 2, 11, 12)	−0.5 to +5.5 Volts
Digital Outputs: (Pins 13-17, 21-24)	−0.5 to +5.5 Volts
(Short-circuit protected to Ground)	
Analog Input	−0.5 to V_{DD} +0.5 Volts

ORDERING INFORMATION

PART NUMBER — **MN5902 H/B**

Standard device is specified for 0°C to +70°C operation.

Add "E" suffix for −25°C to +85°C operation. Add "H" suffix for -55°C to +125°C operation.

Add "/B" suffix to "H" model for Environmental Stress Screening.

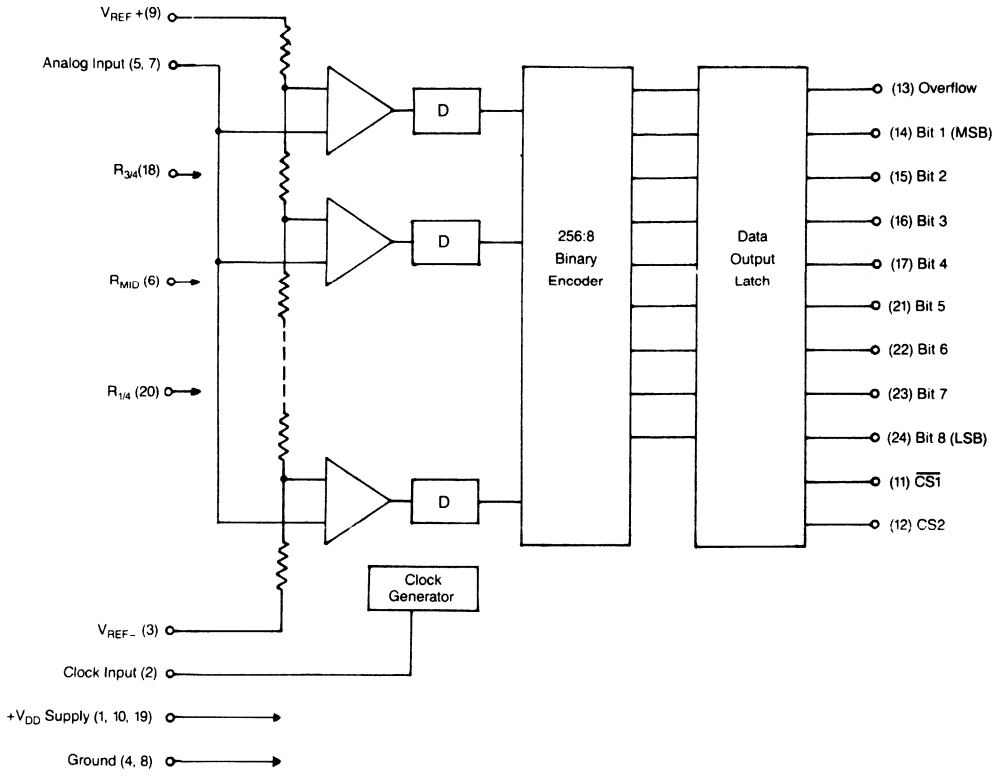
SPECIFICATIONS (T_A = +25°C, V_{DD} = +5.0V, V_{REF+} = +3.0V, V_{REF-} = 0V, and sampling rate = 15MHz unless otherwise indicated)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	0		3.5	Volts
Input Capacitance: Static		10		pF
Dynamic		32		pF
REFERENCE INPUTS				
Reference Ladder Resistance		300		Ohms
Reference Input Range	+0.5	+3.0	+3.5	Volts
DIGITAL INPUTS				
Logic Levels: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
Logic Currents: Logic "1" (V_{IH} = +4.0V)		+0.01	+5	μA
Logic "0" (V_{IL} = +0.4V)		−0.01	−5	μA
Minimum Clock Pulse Width	20			nsec
DIGITAL OUTPUTS				
Logic "1" Voltage at 4mA Load	4.5	4.9		Volts
Logic "0" Voltage at 4mA Load		0.1	0.4	Volts
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Differential Linearity: Initial		±0.35	±0.6	LSB
Over Temperature		±0.4	±0.6	LSB
Integral Linearity: Initial (Note 1)		±0.85	±1.0	LSB
Over Temperature		±1.5	±1.8	LSB
No Missing Codes	Guaranteed Over Temperature			
Zero-Scale Offset (Note 2)		40	70	mV
Gain Error: Initial			1.0	LSB
Over Temperature			1.5	LSB
DYNAMIC PERFORMANCE				
Sampling Rate		20		MHz
Signal-to-Noise Ratio		TBD		dB
Total Harmonic Distortion		−48	−44	dB
(4MHz Analog Input)				
Full-Power Bandwidth	40	50		MHz
Output Data-Valid Delay	10	20	25	nsec
(From Rising Clock Edge)				
Aperture Delay	−5	0	+5	nsec
Aperture Uncertainty		50		psec
POWER SUPPLY REQUIREMENTS				
Power Supply Range	+4.5	+5.0	+5.5	Volts
Power Supply Rejection		±0.01	+0.02	%FSR/%V_{DD}
Power Supply Current: Initial		+70	+80	mA
Over Temperature		+93	+100	mA

SPECIFICATION NOTES

1. Integral linearity specifications are based on end-point measurements, and assume an unadjusted reference mid-point.
2. Zero-scale offset is the difference between the measured input voltage required to produce the transition of code 00000000 to code 00000001, and the voltage theoretically corresponding to 0.5LSB.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The block diagram illustrates the architecture of the MN5902, a fully parallel 8-bit A/D converter. A total of 256 sampling comparators are used to convert the signal on the V_{IN} line to a digital word. The pulses at the CLK input are converted internally into the three phases that control the operation of the comparators. The first cycle, Phase 1, is initiated when the CLK switches to the high state. An analog switch at the input to each comparator then samples a reference voltage that is established by a 256-element resistor ladder between the V_{REF+} and V_{REF-} pins. Each unique reference-voltage tap represents one of the quantization levels to which the signal at V_{IN} will be compared.

Overlapping with Phase 1, the Phase 2 cycle serves to auto-zero the comparators. This operation has the purpose of cancelling dc-offset errors that arise from device mismatch between comparators. At the end of the Phase 2 interval, the capacitor at the input to each comparator stores the difference between the reference tap voltage and the auto-zeroed bias point. The capacitor will hold the comparator at a high-gain trigger point in preparation for sampling the input signal.

The low-going transition of the clock terminates the auto-zeroing interval and initiates the input-sampling interval. The Phase 3 period is non-overlapping with Phase 2 to minimize coupling of the reference to the input. A sampling glitch will be observed on the V_{IN} line at the beginning of Phase 3, as the input buffer amplifier must charge or discharge the coupling capacitors from their reference levels to the new level of the input signal. The comparators serve as track-and-hold amplifiers over the duration of the sampling interval. When the clock returns high, the sampling switches are turned off and the comparator levels are latched into flip-flops.

To determine the quantized level of the input signal, it is necessary to find the transition points between comparators that produce logic "1" results and those that produce logic "0" results. This transition point, corresponding to the signal residing at the end of the sampling interval, will lie within a 1LSB (least-significant-bit) voltage range. This function of thermometer decoding is fulfilled by the 3-input NAND gates at the output of each comparator latch.

The thermometer decoder will cause just one of the 256 NAND gates to assume a low-level output. This signal will represent an address to the 256-to-8 encoder, which can then produce a properly encoded binary output. Latches on the digital outputs can be used to store the digitized result. The MN5902 utilizes latches in a signal-processing pipeline fashion. Digital inputs, $\overline{CS1}$ and CS2, are used to set the latches' outputs to the high-impedance state.

For the MN5902, the total conversion period upon start-up is two clock periods (see the timing diagram in Figure 2); the conversions proceed thereafter at the clock rate.

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (VDC)	OVERFLOW	DIGITAL OUTPUT MSB	LSB
$+V_{REF}$	1	1111	1111
$+V_{REF}-1/2LSB$	Ø	1111	1111
$+V_{REF}-LSB$	0	1111	1111
$+V_{REF}-3/2LSB$	0	1111	111Ø
$+1/2V_{REF}+1/2LSB$	0	1000	000Ø
$+1/2V_{REF}-1/2LSB$	0	ØØØØ	ØØØØ
$+1/2V_{REF}-3/2LSB$	0	0111	111Ø
+1/2LSB	0	0000	000Ø
0	0	0000	0000

Analog inputs indicated are the theoretical values for the transitions of the codes indicated above. With the converter continously converting, the output bits indicated as Ø will change from logic "0" to logic "1" or vise versa as the input voltage passes through the indicated level.

LAYOUT AND GROUNDING CONSIDERATIONS — The MN5902 and other high-speed devices require that careful consideration be given to high-speed and low-noise design techniques. Care must be taken to assure that seperation of analog signals and digital signals is maintained. The use of ground and power planes as well as signal shielding are highly recommended. Bypass capacitors should be used and located as close to the device as possible. It is also recommended that circuitry interfacing to the MN5902 be located as close to the device as possible to minimize transmission line effects.

3-STATE OUTPUT CONTROL — Both $\overline{CS1}$ and CS2 can be used to enable the 8-bit output lines or to set them to the high-impedance state. $\overline{CS1}$ controls the 8-bit output lines, while CS2 controls both the output lines and the Overflow output. This arrangement makes it possible to stack two devices in a 9-bit configuration, in which Overflow becomes the MSB (most-significant bit), and to select the lower eight bits from either the upper or lower A/D converter.

TRUTH TABLE

$\overline{CS1}$	CS2	B1 — B8	OVERFLOW
0	1	Valid	Valid
1	1	High-Z	Valid
X	0	High-Z	HIgh-Z

INTERMEDIATE RESISTOR TAPS — Intermediate taps at each quarter point of the reference resistor ladder are brought out to package pins. In high-speed operation, it is necessary to provide capacitive decoupling of these points to ground in order to prevent clock noise from interfering with the conversion. It is possible to adjust the dc potentials at these points to trim integral linearity, or to obtain a non-linear transfer characteristic.

CASCADING FOR 9-BIT OPERATION — It is possible to stack or cascade two MN5902 Flash A/D converters to configure a 9-bit digitizer. Cascading entails connecting the reference-resistor ladders in two devices in series. The bottom of the upper converter's ladder ($V_{REF}-$) connects to the top of the lower converter's ladder ($V_{REF}+$). The reference voltage source is connected to $V_{REF}+$ of the upper converter while the $V_{REF}-$ connection of the lower converter is tied to ground. Mid-scale of the cascaded A/D system is established at the point where the lower A/D converter overflows.

The Overflow output from the lower A/D converter detects the overflow condition and becomes the MSB of the 9-bit system, and in addition, serves to multiplex the lower eight bits between the two A/D converters.

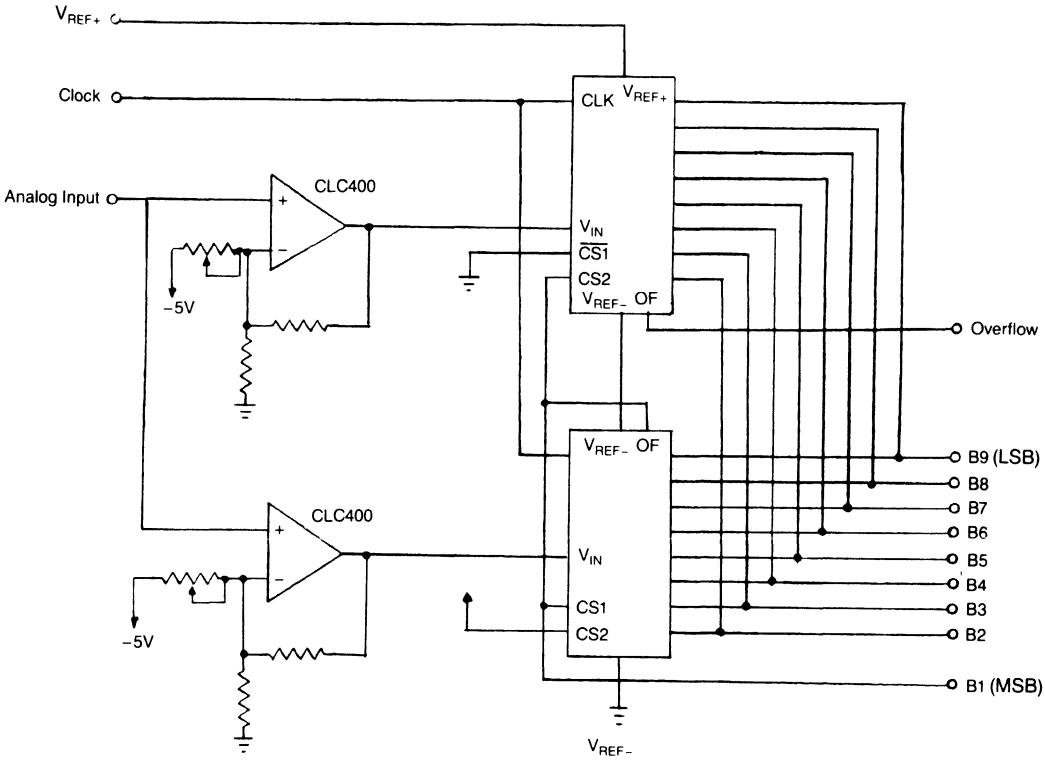
Two output controls are provided by the MN5902. CS2 controls the 3-state output function of the eight data output bits plus the overflow output. A logic "1" applied to the CS2 input enables these outputs while a logic "0" forces the output into the high-impedance state. $\overline{CS1}$ only has an effect on the eight data output bits. A logic "0" applied to $\overline{CS1}$ enables these data lines while a logic "1" forces them into the high-impedance state.

In the cascaded configuration, the MSB is set high (upon the overflow condition of the lower 8-bit A/D converter), it disables the lower data output bits while enabling the output bits and overflow bits of the upper A/D converter. Because the upper A/D converter is experiencing an underflow condition at the crossover point, a proper mid-scale code is produced. A 9-bit system overflow signal is available from the upper A/D converter.

The use of signal input buffer amplifiers are recommended in cascading applications. Separate signal paths for each A/D converter provide several benefits. First, input bandwidth and settling time performance in the switched-capacitor input of each MN5902 will benefit from being driven from a unique source. Secondly, offset and gain errors in each A/D will manifest themselves as large differential and integral linearity errors in the output transfer function of the 9-bit system.

o minimize these errors, it is possible to effect separate adjustments n the CLC400 current-feedback amplifiers. The offset potentiometer f the upper amplifier provides an adjustment for system differential nearity at the mid-scale point. The gain of the amplifiers provide a neans for achieving gain matching between the two eight-bit devices nereby allowing trim of the system integral linearity error. The expression for the gain is 1+RF/Req, where Req is the parallel combination of the resistors at the amplifiers input with the feedback path disconnected. Because gain and offset are interrelated, the offset potentiometer should be large relative to the other resistor (10K Ohms for example).

igure 3. MN5902 9-Bit Cascade Connection

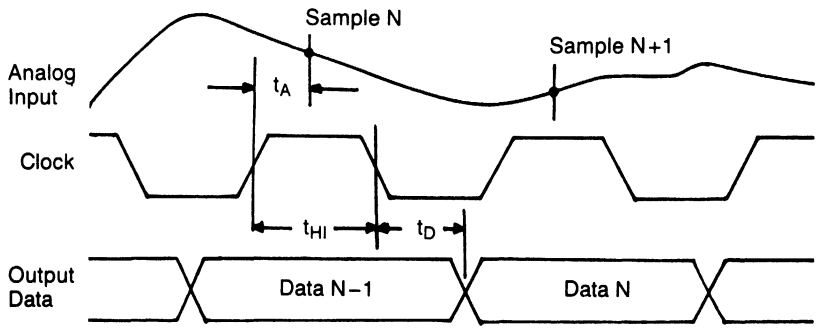


PIN DESCRIPITONS

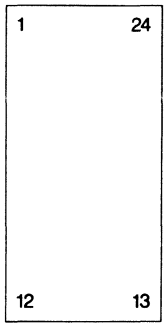
PIN	SYMBOL	FUNCTIONAL DESCRIPTION
1	V_{DD}	Supplies power to analog and digital sections of chip. Nominal level +5V.
2	CLK	Externally supplied clock signal; used internally to generate three distinct phases for the comparator sampling sequence, comparator latches, and bit-output latches.
3	V_{REF-}	Voltage potential at the bottom of the resistor ladder that sets the lower limit of the A/D converter's range. Also sets the offset code for 0 to 1 transition.
4	GND	Ground potential for the analog and digital circuitry. Also the silicon substrate potential.
5	V_{IN}	The analog signal input to the lower half of the A/D converter.
6	R_{MID}	Midpoint of the resistor ladder, at the boundary between codes 128 and 129. Normally decoupled through a capacitor to ground, but may be used to adjust linearity or to impart a non-linear transfer function.
7	V_{IN}	The analog signal input to the upper half of the A/D converter.
8	GND	Ground potential for the analog and digital circuitry. Also the silicon substrate potential.
9	V_{REF+}	Voltage potential to the top of the resistor ladder that sets the upper limit of the A/D converter's range. Can be used to make gain adjustments. Nominally +3.0V.
10	V_{DD}	Supplies power to analog and digital sections of chip. Nominal level +5V.
11	$\overline{CS1}$	3-state control for output bits B1 to B8. When CS2 is high, output bits are enabled (When $\overline{CS1}$ is low). $\overline{CS1}$ is a don't care (X) when CS2 is low.

PIN	SYMBOL	FUNCTIONAL DESCRIPTION
12	CS2	3-state control for output bits B1 to B8 and the Overflow output. When CS2 is high, output bits B1 to B8 are enabled if $\overline{CS1}$ is low. CS2 has independent control of the Overflow output. If CS2 is low, B1 to B8 and Overflow are in the high-impedance state.
13	OF	When high, Overflow indicates that the input voltage exceeds the top reference tap point, nominally V_{REF+} −½LSB. Outputs B1 to B8 assume all "1's" when Overflow is high.
14	B1	(MSB) Most-significant bit of the digitized 8-bit output. Has a weight of FSR/2 where FSR (full-scale range) is V_{REF+} −V_{REF-}.
15	B2	2nd most-significant bit of the digitized 8-bit output. Has a weight of FSR/4.
16	B3	3rd most-significant bit of the digitized 8-bit output. Has a weight of FSR/8.
17	B4	4th most-significant bit of the digitized 8-bit output. Has a weight of FSR/16.
18	R3/4	3rd quarter point of the A/D converter's resisitor ladder, at the boundary between codes 64 and 65. Normally decoupled through a capacitor to ground, but can be used to adjust integral linearity or to impart a non-linear transfer function.
19	V_{DD}	Supplies power to analog and digital sections of chip. Nominal level +5V.
20	R1/4	1st quarter point of the A/D converter's resistor ladder, at the boundary between codes 64 and 65. Normally decoupled through a capacitor to ground, but can be used to adjust integral linearity or to impart a non-linear transfer function.
21	B5	5th most-significant bit of the digitized 8-bit output. Has a weight of FSR/32.
22	B6	6th most-significant bit of the digitized 8-bit output. Has a weight of FSR/64.
23	B7	7th most-significant bit of the digitized 8-bit output. Has a weight of FSR/128.
24	B8	(LSB) Least-significant bit of the digitized 8-bit output. Has a weight of FSR/256.

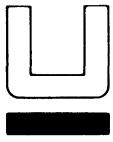
TIMING DIAGRAM



PIN DESIGNATIONS



1 $+V_{DD}$ Supply	24 Bit 8 (LSB)
2 Clock	23 Bit 7
3 V_{REF-}	22 Bit 6
4 Ground	21 Bit 5
5 Analog Input	20 $R_{1/4}$
6 R_{MID}	19 $+V_{DD}$
7 Analog Input	18 $R_{3/4}$
8 Ground	17 Bit 4
9 V_{REF+}	16 Bit 3
10 $+V_{DD}$	15 Bit 2
11 $\overline{CS1}$	14 Bit 1 (MSB)
12 CS2	13 Overflow



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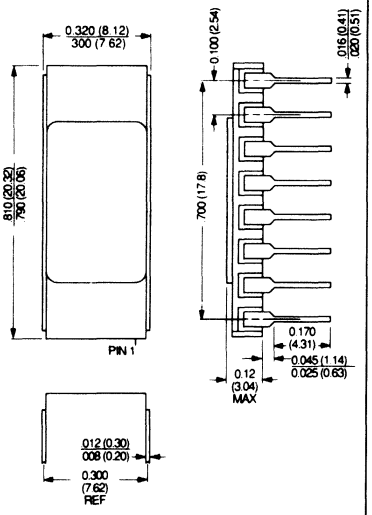
MICRO NETWORKS

MN5903

6-Bit, 75MHz
FLASH A/D CONVERTER

FEATURES

- **6-Bit Resolution**
- **75MHz Conversion Rate**
- **140MHz Input Bandwidth**
- **36dB SNR at 35MHz**
- **Low Harmonic Distortion**
  -44dB at 10MHz
  -36dB at 35MHz
- **Overflow Output (7th bit)**
- **Low Input Capacitance, 25pF**
- **ECL 10K Compatible Output Data**
- **Operating Temperature Range –55°C to +125°C, case (S and T Grades)**
- **Improved Pin-for-Pin Compatibility with AD9000 (MN5903 Model)**



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5903 is an ultra-high speed 6-bit monolithic Analog to Digital converter with a guaranteed conversion speed (strobe frequency) of up to 75MHz. The MN5903 utilizes the "Flash" or parallel principle whereby a field of 64 comparators simultaneously determine the precise analog input. The comparators' outputs are converted to ECL compatible outputs through two encoding stages which are activated by the Encode signal.

The MN5903 is offered in two logic configurations. The MN5903A is designed to be used as a stand-alone 6-bit A/D converter or as a terminating device for a 7 or 8-bit A/D. The MN5903 is designed to be used as a cascading device with the MN5903A for 7 or 8-bit applications. The MN5903 also offers improved performance and pin-for-pin compatibility to the AD9000.

The MN5903 has a low input capacitance of 25pF and a 13kOhm input impedance which allows the input to be easily driven by interfacing circuitry.

The MN5903's broad input bandwidth of 140MHz and low aperture uncertainty of 25psec eliminate the user's need for an additional track and hold amplifier. The MN5903 also provides an overflow signal which indicates when the analog input signal exceeds the $+V_{REF}$ voltage. A hysteresis control function is provided that allows the user to modify the comparator's sensitivity.

Packaged in a small, 16-pin, hermetically sealed package, the MN5903 offers an outstanding Signal-to-Noise-Ratio (SNR) of 36dB at 35MHz and low Total Harmonic Distortion (THD) of –44dB at 10MHz.

Micro Networks offers premium "K" and "T" grades of the MN5903 and MN5903A devices. Their superior performance includes the following specifications which are guaranteed over their full operating temperature range: ±1/2LSB max. differential linearity, ±0.75LSB max. full scale error, 33dB min. SNR at 10MHz analog input and -35dB max. THD at 10MHz analog input.

MN5903 Devices are specified for 0°C to +70°C (case, J and K models) operation, and 55°C to +125°C (case, S and T models) operation. For applications in harsh-environment industrial or military/aerospace systems, S/B and T/B models are available with Environmental Stress Screening.

APPLICATIONS

Radar Systems
Digital Oscilloscopes
Automatic Test Equipment
ECM Equipment
Analytical Systems

July1990

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MN5903 6 Bit 75MHz FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (case)	-55°C to +125°C
Specified Temperature Range (case)	
MN5903J,MN5903K	0°C to +70°C
MN5903S, MN5903T	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Positive Supply Voltage ($+V_S$)	-0.3 to +6 Volts
Negative Supply Voltage ($-V_S$)	+0.3 to -6 Volts
Analog Input Voltages (V_{IN}, $+V_{REF}$, $-V_{REF}$)	-3.5 to +2.5 Volts
Encode Input Voltage	$-V_S$ to 0 Volts
Hysteresis Control Voltage (V_H)	0 to 3.0 Volts
Digital Input Voltages	-3.5 to +0.0 Volts
Digital Output Current	20 mA
Analog Ground to	±0.5 Volts
Digital Ground Voltage Differential	

ORDERING INFORMATION

PART NUMBER — **MN5903XX/B**

Select MN5903 or MN5903A Model.

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

ELECTRICAL SPECIFICATIONS (T_A=+25°C, $+V_{REF}$=+1.0V, $-V_{REF}$=-1.0V, $+V_S$=+5.0V, $-V_S$=-5.2V unless otherwise indicated. Specifications apply to all grades unless specific grades are referenced).

PARAMETER	Min	Typ	Max	Units
RESOLUTION		6		Bits
ANALOG INPUTS				
Input Voltage Range over Temperature		±2		Volts
Input Bias Current (Sampling)			700	µA
over Temperature (Note 1)				
Input Bias Current (Latched)			700	µA
over Temperature (Note 1)				
Input Resistance		13		kOhms
Input Capacitance (Note 2)		25	50	pF
Full Power Bandwidth (Note 3)		140		MHz
REFERENCE INPUTS (Note 4)				
Reference Ladder Resistance	80		200	Ohms
Reference Ladder Tempco		0.275		Ohms/°C
Reference Input Bandwidth		20		MHz
TRANSFER CHARACTERISTICS				
Differential Linearity: Initial (+25°C): J, S Grades		0.25	0.5	LSB
over Temperature: J, S Grades			1.0	LSB
Differential Linearity: Initial (+25°C): K, T Grades		0.25	0.35	LSB
over Temperature: K, T Grades			0.5	LSB
Integral Linearity: Initial (+25°C): J, S Grades		0.25	0.5	LSB
over Temperature: J, S Grades			1.0	LSB
Integral Linearity: Initial (+25°C): K, T Grades		0.25	0.35	LSB
over Temperature: K, T Grades			0.5	LSB
No Missing Codes		Guaranteed Over Temperature		
+Full Scale Input Error: Initial (+25°C): J, S Grades		0.3	7/8	LSB
over Temperature: J, S Grades			1.5	LSB
+Full Scale Input Error: Initial (+25°C): K, T Grades		0.15	0.5	LSB
over Temperature: K, T Grades			0.75	LSB
-Full Scale Input Error: Initial (+25°C): J, S Grades		0.25	7/8	LSB
over Temperature: J, S Grades			1.5	LSB
-Full Scale Input Error: Initial (+25°C): K, T Grades		0.15	0.5	LSB
over Temperature: K, T Grades			0.75	LSB
DYNAMIC PERFORMANCE				
Conversion Rate: J Grade	50	70		MHz
Conversion Rate: K, S, and T Grades	75	80		MHz
Conversion Time: J Grade			20	nsec
Conversion Time: K, S, and T Grades			13.3	nsec
Aperture Delay (t_D)		2		nsec
Aperture Uncertainty (Jitter)		25		psec
Output Propagation Delay (t_{PD}) **(Note 2, 5)**	7		12	nsec
Output Hold Time (t_{OH}) **(Note 2, 6)**	8		14	nsec

ELECTRICAL SPECIFICATIONS (Continued)

PARAMETER	Min	Typ	Max	Units
DYNAMIC PERFORMANCE (Continued)				
Transient Response Time (Note 7)		13		nsec
Overvoltage Recovery Time (Note 8)		11		nsec
Output Rise or Fall Time: J Grade (Note 9)			5	nsec
Output Rise or Fall Time: K, S, and T Grades (Note 9)			4.5	nsec
ENCODE INPUT				
Logic "1" Voltage over Temperature	-1.1			Volts
Logic "0" Voltage over Temperature			-1.5	Volts
Logic "1" Current over Temperature			100	µA
Logic "1" Current over Temperature			100	µA
Encode Pulse Width High (t_{PWH})	6.6			nsec
Encode Pulse Width Low (t_{PWL})	6.6			nsec
AC LINEARITY (Note 10)				
Dynamic Linearity (Note 11)		0.5		LSB
In-Band Harmonics				
(DC to 1MHz)		48		dBc
(1MHz to 5MHz)		48		dBc
(5MHz to 8MHz)		46		dBc
Signal to Noise Ratio (Note 12)				
(540kHz Analog Input): J and S Grades	31	38		dB
(540kHz Analog Input): K and T Grades	35	38		dB
(10MHz Analog Input): J and S Grades		37		dB
(10MHz Analog Input): K and T Grades	35	37		dB
(10MHz Analog Input): K and T Grades over Temperature	33			dB
(20MHz Analog Input)		37		dB
(35MHz Analog Input): J and S Grades		36		dB
(35MHz Analog Input): K and T Grades	31	36		dB
Total Harmonic Distortion (THD)				
(2MHz Analog Input)		-47		dB
(10MHz Analog Input): J and S Grades		-44		dB
(10MHz Analog Input): K and T Grades		-44	-38	dB
over Temperature			-35	dB
(20MHz Analog Input)		-43		dB
(35MHz Analog Input): J and S Grades		-34		dB
(35MHz Analog Input): K and T Grades		-34	-30	dB
DIGITAL OUTPUTS (Note 13)				
Logic "1" Voltage over Temperature	-1.1			Volts
Logic "0" Voltage over Temperature			-1.5	Volts
POWER SUPPLIES				
Positive Supply Current (+5.0V)		71	85	mA
over Temperature			90	mA
Negative Supply Current (-5.2V)		65	75	mA
over Temperature			80	mA
Nominal Power Dissipation		693		mW
Reference Ladder Dissipation		20		mW

SPECIFICATION NOTES

1. Measured with $A_{IN}=+V_{REF}$.
2. Listed specification is for reference only and is not tested.
3. Full Power Bandwidth is the input frequency at a 75MHz sampling rate at which the reconstructed output amplitude drops 3dB with respect to the output.
4. The differential reference voltages may be varied under normal operating conditions from ±0.5 Volts to ±2.0 Volts. $+V_{REF}$ must always be greater than $-V_{REF}$.
5. Measured from leading edge of ENCODE to data out on Bit 1 (MSB).
6. Measured from trailing edge of ENCODE to data out on Bit 1 (MSB).
7. For a full-scale step input, 6 bit accuracy is obtained in the specified time.
8. Time to recover to 6 bit accuracy after an overvoltage whose input is equal to 150% of the full-scale input voltage.
9. Measured on the MSB (Bit 1) only.
10. Measured at 50MSPS encode rate.
11. Analog Input frequency =15MHz.
12. RMS signal to RMS noise.
13. Measured with outputs terminated with 100 Ohm resistors to -2.0 volts.

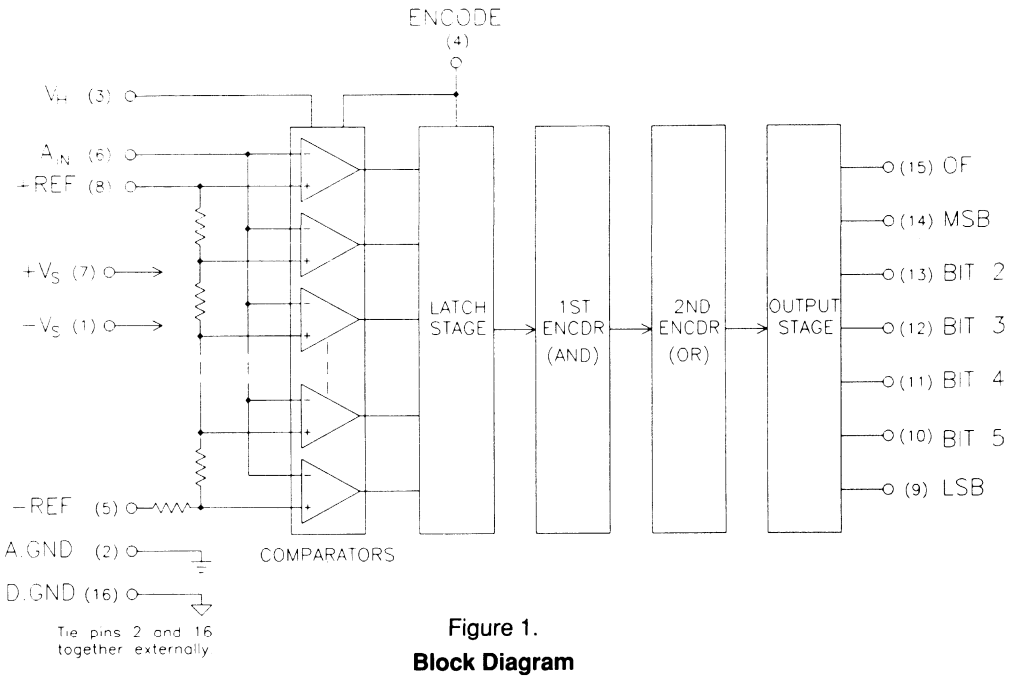


Figure 1.
Block Diagram

APPLICATION INFORMATION

The MN5903A has a nonreturn-to-zero output logic coding when $A_{IN} \geq +V_{REF}$. This coding is desirable for applications that require stand-alone 6-bit A/D converters. The MN5903 has a return-to-zero logic coding when $A_{IN} \geq +V_{REF}$. (See Digital Output Coding.) This facilitates the cascading of the MN5903 with the MN5903A for applications requiring 7 or 8-bits. The MN5903's coding is usually not desired for stand-alone 6-bit applications as additional external circuitry is required to convert the output logic to nonreturn-to-zero coding. The MN5903 is recommended for those applications that can benefit from superior performance and pin-for-pin compatibility with the AD9000.

The MN5903 and MN5903A have open emitter outputs which allow the output of several devices to be WIRE-OR'D when cascaded for increased resolution. Figure 3 shows how the MN5903 and MN5903A may be stacked together for usage as a 7-bit A/D converter.

HYSTERESIS CONTROL FUNCTION

The MN5903 has a Hysteresis Control Voltage Input, V_H, which allows the user to affect the comparators' sensitivity. An input voltage of 0V to +3V applied to V_H (Pin 3) causes the comparator hysteresis to vary from approximately 15mV to 50mV. Increasing the comparator hysteresis reduces the error rate (number of false full-scale output codes in a given period). The MN5903 is tested with the V_H input open and produces a very low error rate. Use of the hysteresis control function may be considered for error sensitive applications, especially those employing a high (greater than 50MHz) encode rate. The V_H input, when used, should be decoupled to ground through a 0.1µF ceramic capacitor.

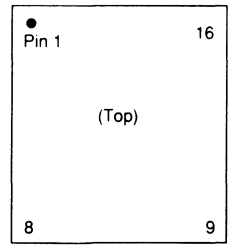
LAYOUT SUGGESTIONS

It is strongly recommended that a substantial ground plane be placed under and around the MN5903. It is recommended that the MN5903's Analog Ground and Digital Ground be connected together at the MN5903 and also connected to the ground plane.

The power supplies and reference inputs should be decoupled to ground directly at the MN5903 with 0.1µF ceramic capacitors in order to reduce the effects of system noise on converter accuracy. Chip capacitors will produce the best results because they do not have the lead inductance inherent to discrete devices. The reference inputs should be driven from a low source impedance. This will help to minimize errors caused by noise on the reference source and also minimize errors otherwise caused by the reference's source impedance. Test Figure 4 includes circuitry that has been proven to be a simple and effective means of driving the reference inputs.

PIN DESIGNATIONS

Pin	Symbol	Function	Pin	Symbol	Function
1	$-V_{_}$	Negative Supply Voltage.	16	Dig Gnd	Digital Ground
2	Ana Gnd	Analog Ground	15	OF	Overflow Signal
3	V_H	Hysteresis Control Voltage	14	Bit 1	Bit 1 (MSB)
4	Encode	Signal	13	Bit 2	Bit 2
5	$-V_{REF}$	Negative Reference Voltage	12	Bit 3	Bit 3
6	A_{IN}	Analog Input	11	Bit 4	Bit 4
7	$+V_S$	Positive Supply Voltage	10	Bit 5	Bit 5
8	$+V_{REF}$	Positive Reference Voltage	9	Bit 6	Bit 6 (LSB)



DIGITAL OUTPUT CODING

MN5903 Analog Input	Digital Output						
	OF (Bit 1)	MSB				LSB (Bit 6)	
$+V_{REF}$	1	0	0	0	0	0	0
$+V_{REF}$ -1/2LSB	*	*	*	*	*	*	*
$+V_{REF}$ -3/2LSB	0	1	1	1	1	1	*
+1/2LSB	0	1	0	0	0	0	*
0	0	1	0	0	0	0	0
-1/2LSB	0	*	*	*	*	*	*
$-V_{REF}$ +1/2LSB	0	0	0	0	0	0	*
$-V_{REF}$	0	0	0	0	0	0	0

MN5903A Analog Input	Digital Output						
	OF (Bit 1)	MSB				LSB (Bit 6)	
$+V_{REF}$	1	1	1	1	1	1	1
$+V_{REF}$ -1/2LSB	*	1	1	1	1	1	1
$+V_{REF}$ -3/2LSB	0	1	1	1	1	1	*
+1/2LSB	0	1	0	0	0	0	*
0	0	0	1	0	0	0	0
-1/2LSB	0	*	*	*	*	*	*
$-V_{REF}$ + 1/2LSB	0	0	0	0	0	0	*
$-V_{REF}$	0	0	0	0	0	0	0

Note: * indicates a bit transition whereby the output bit(s) is(are) changing from "1" to "0" or vice versa.
The analog input voltages shown above are the theoretical voltages for the corresponding digital output.
Example: With an analog input of $-V_{REF}$ + 1/2LSB, the output code will be at the transition of the codes 0 000000 and 0 000001.

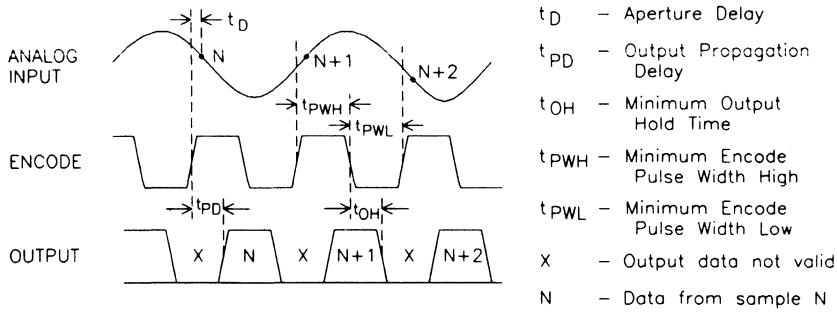


Figure 2.
Timing Diagram

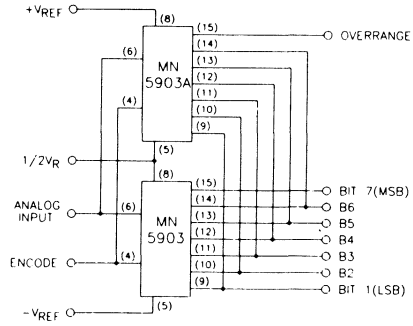


Figure 3.
Cascading 7-Bit Operation

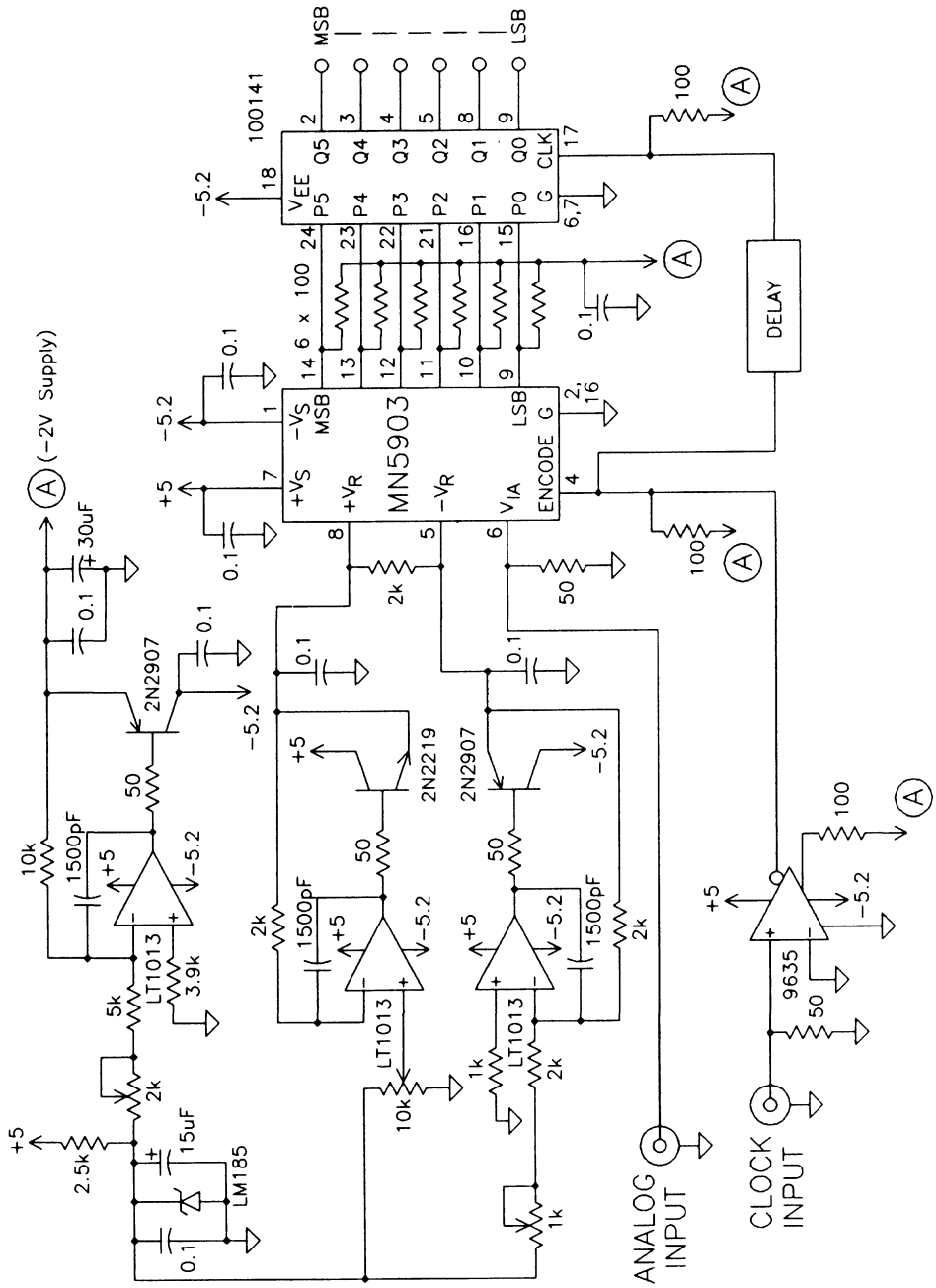


Figure 4.
Test Circuit

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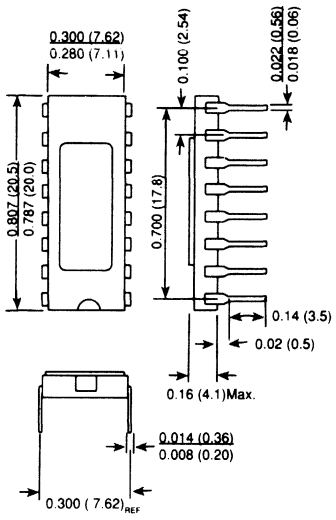
MN5904/5905

6-Bit, 100MHz
FLASH A/D CONVERTER

FEATURES

- **100MHz Conversion Rate**
- **140MHz Input Bandwidth**
- **High Input Impedance**
- **ECL 10K Compatible Outputs**
- **Overflow Output (7th Bit)**
- **Low 25pF Input Capacitance**
- **Operating Temperature Range -55°C to +125°C Case (H Grade)**
- **Pin-for-Pin Compatibility With SDA 5200N and SDA 5200S**

16-PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5904/5905 is an ultra-high-speed 6-bit monolithic A/D converter capable of operating at sampling rates as high as 100MHz. The device uses a parallel-comparator, or "flash", architecture to convert ±2 V analog input signals to ECL-level outputs through two encoding stages. The converter is offered in two logic configurations. The MN5905 is designed for use either as a stand-alone 6-bit A/D converter or as a terminating device or configuring a cascaded 7- or 8-bit A/D converter. The MN5904 is designed for use as a cascading device in these enhanced-resolution applications.

The MN5904/5905's 25pF input capacitance and 150μA input current make the devices extremely easy to drive in high-frequency applications. In addition, the devices' 140 MHz input bandwidth and 25psec aperture uncertainty eliminate the need for a track-and-hold amplifier at the input.

The MN5904 provides an overflow signal that indicates analog input voltages in excess of the $+V_{REF}$ voltage. A hysteresis control function allows the user to optimize input characteristics by modifying the input comparators' sensitivity.

Packaged in a small, hermetically sealed 16-pin DIP, the MN5904/5905 offers outstanding specifications: ±½LSB maximum differential nonlinearity and ±0.75LSB maximum full-scale error at 25°C, and no-missing-codes performance over the full operating-temperature range. MN5904/5905 Series devices are specified for operation over 0°C to +70°C (case) and −55°C to +125°C (case). The MN5904 and MN5905 are pin-compatible equivalents to Siemens' SDA 5200N and SDA 5200S, respectively.

APPLICATIONS

Radar Systems
Digital Oscilloscopes
Medical Imaging
Analytical Systems
Video Digitizing
Subranging A/D Systems
Video Test Systems
Automatic Test Equipment

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MN5904/5905 6-Bit, 100MHz FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Rance (case)	-55°C to +125°C
Specified Temperature Range (case)	
MN5904, 5905	0°C to +70°C
MN5904E, 5905E	-40°C to +85°C
MN5904H, 5905H	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Positive Supply Voltage ($+V_S$)	-0.3 to +6.0 Volts
Negative Supply Voltage ($-V_S$)	-6.0 to +0.3 Volts
Analog and Reference Inputs	-3.5 to +2.5 Volts
Encode Input	$-V_S$ to +0.0 Volts
Hysteresis Control	0 to +3.0 Volts
Digital Inputs	-3.5 to +0.0 Volts
Analog -Digital Ground Voltage Differential	±0.5 Volts

ORDERING INFORMATION

PART NUMBER ——— MN590XH

Select P/N MN5904 or MN5905 for desired output logic coding.

Add no suffix for 0°C to +70°C (case) operating temperature.

Add "E" suffix for -40°C to +85°C (case) operating temperature.

Add "H" suffix for -55°C to +125°C (case) operating temperature.

ELECTRICAL SPECIFICATIONS (T_A=+25°C; $+V_S$=+5.0V; $-V_S$=-5.2V; $\pm V_{REF}$=±1V; f_{ENCODE}=75MHz unless otherwise indicated.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Resolution		6		Bits
ANALOG INPUTS				
Input Range	$-V_{REF}$		$+V_{REF}$	Volts
Input Span for ½LSB DNL (Note 1)	1.2	0.6		Volts
Input Span for ¼LSB DNL	2.4	1.2		Volts
Input Current at $V_{AIN}=+V_{REF}$		150	500	µA
Input Current at $V_{AIN}=-V_{REF}$	-500		500	nA
Input Capacitance		25		pF
REFERENCE INPUTS				
Positive Reference Voltage (Note 2)	-2.5		+2.0	Volts
Negative Reference Voltage (Note 2)	-3.0		+1.5	Volts
Reference Ladder Resistance	96	128	195	Ohms
Total Reference Span (Note 2)			5.0	Volts
TRANSFER CHARACTERISTICS				
Differential Linearity at +25°C		±0.25	±0.5	LSB
over Temperature			±1.0	LSB
Integral Linearity at +25°C		±0.25	± 0.5	LSB
over Temperature			± 1.0	LSB
No Missing Codes	Guaranteed Over Temperature			
+Full Scale Input Error at +25°C		±0.3	±7/8	LSB
Over Temperature			±1.5	LSB
-Full Scale Input Error at +25°C		±0.25	±7/8	LSB
Over Temperature			±1.5	LSB
ENCODE INPUT				
"1" Level	-1.1	-0.9	-0.6	Volts
"0" Level	-2.0	-1.7	-1.6	Volts
"1" Input Current		6	50	µA
"0" Input Current		6	50	µA
Encode Pulse Width High (t_{PWH})	6.6			nsec
Encode Pulse Width Low (t_{PWL})	6.6			nsec
DATA OUTPUTS (Note 3)				
"1" Output Level	-1.1	-0.9	-0.7	Volts
"0" Output Level	-2.0	-1.7	-1.5	Volts

ELECTRICAL SPECIFICATIONS (CONTINUED)

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Aperture Delay (t_D) Aperture Uncertainty (Jitter)		2 25		nsec psec
Output Propagation Delay (t_{PD}; Note 4) Output Hold Time (t_{OH}; Note 5)		9 11		nsec nsec
Maximum Encode Rate	75	100		MHz
Input Slew Rate Input -3dB Bandwidth (Note 6)		500 140		V/µsec MHz
AC LINEARITY (Note 7)				
Dynamic Linearity at f_{AIN}=15MHz		1/2		LSB
In-Band Harmonics DC to 1MHz 1 to 5MHz 5 to 8MHz		 48 48 46		 dBc dBc dBc
Signal-to-Noise Ratio (Note 8) 10MHz Analog Input 35MHz Analog Input		 37 36		 dB dB
Total Harmonic Distortion (THD) 10MHz Analog Input 35MHz Analog Input		 -44 -34		 dB dB
POWER SUPPLIES				
Positive Supply Negative Supply Positive Supply Current Negative Supply Current	+4.5 -5.7	+5.0 -5.2 50 55	+5.5 -4.7 80 80	Volts Volts mA mA

Notes:

1. Span, also called full-scale range (FSR), is the maximum negative-to-positive excursion of the input voltage. DNL is differential nonlinearity, the deviation from the theoretical step size for any code.
2. Total Reference Span is $+V_{REF}$-($-V_{REF}$). $+V_{REF}$ must always be more positive than $-V_{REF}$.
3. Measured with outputs terminated with 100Ω resistors to -2.0V.
4. Measured from leading edge of ENCODE to data out on Bit6 (MSB).
5. Measured from trailing edge of ENCODE to data out on Bit6 (MSB).
6. Input frequency at a 75MHz sampling rate at which the reconstructed output amplitude drops 3dB with respect to the input signal.
7. Measured with 50MHz sampling rate.
8. RMS signal to RMS noise.

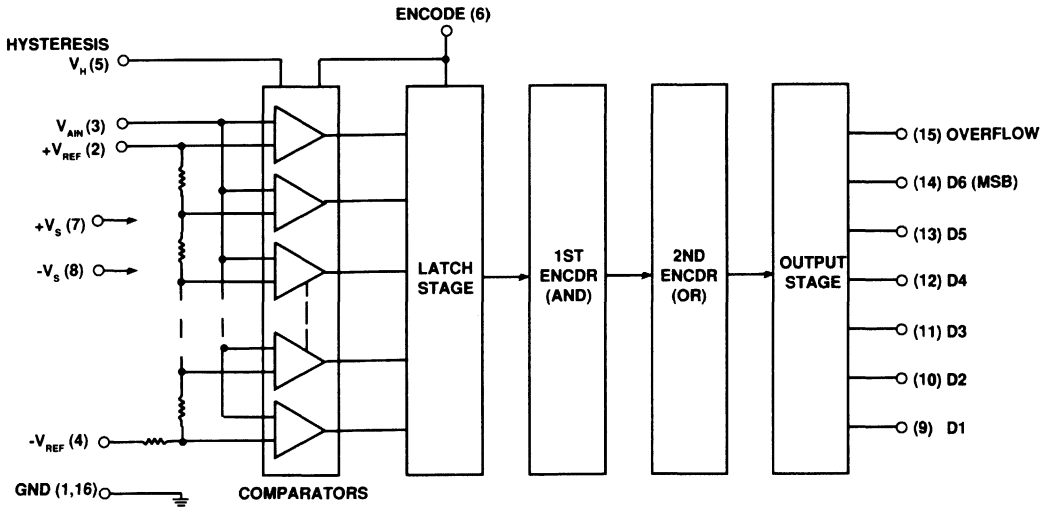


Figure 1. **Block Diagram**

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION - In accordance with industry convention, both the MN5904 and MN5905 are designed to produce their first logic transition (000000 to 000001) when the analog input voltage surpasses $-V_{REF}+1/2$LSB. This convention centers the codes such that an ideal D/A converter with an output-voltage range matching the input-voltage range of the MN5904/5905, connected to the input of the MN5904/5905, will produce unambiguous, identical codes in the MN5904/5905 (see Digital Output Coding). With this coding scheme, the last transition (111110 to 111111) occurs when the analog-input voltage surpasses $+V_{REF}-1\frac{1}{2}$LSB.

The MN5904 and MN5905 differ in their output coding when the analog-input voltage surpasses $+V_{REF}-1\frac{1}{2}$LSB. For both models, the overflow output changes from "0" to "1" at this point. In the MN5905, the output code remains 111111; in the MN5904, however, the code changes from 111111 to 000000. Because of its nonreturn-to-zero coding, the MN5905 is the A/D converter of choice for stand-alone 6-bit applications. The return-to-zero coding, of the MN5904 makes the device suitable for cascading with the MN5905 to obtain 7 or 8 bits of resolution. The open-emitter output architecture of both devices facilitates the cascade connection (Figure 3).

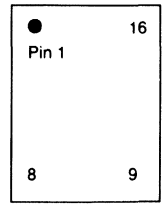
HYSTERESIS CONTROL FUNCTION - A Hysteresis Control Voltage (V_H) pin in the MN5904/5905 provides an adjustment of the input comparators' sensitivity. An input voltage of 0V to +3V applied to V_H causes the comparator hysteresis to vary from approximately 15mV to 50mV. Increasing the comparator hysteresis reduces the error rate (number of false full-scale output codes in a given period). It may be desirable to consider the use of the hysteresis control function for error-sensitive applications, especially those employing a high (greater than 50MHz) sampling rate. The V_H input, when used, should be decoupled to ground through a 0.1µF capacitor.

LAYOUT SUGGESTIONS - It is strongly recommended that a substantial ground plane be placed under and around the MN5904/5905. It is further recommended that the two ground pins be connected together as closely as possible to the MN5904/5905, and also connected to the ground plane. The power supplies and reference inputs should be decoupled to ground directly at the MN5904/5905 with 0.1µF capacitors in order to reduce the effects of system noise on converter accuracy.

Chip capacitors produce the best results because they do not exhibit the lead inductance inherent in discrete components. The reference inputs should be driven from a source having low output impedance. The low impedance will help to minimize errors caused by noise on the reference line and will also reduce errors that could otherwise arise from the reference's source impedance. Figure 4 shows circuitry that has proven to be a simple and effective means of driving the reference inputs.

PIN DESIGNATIONS

1	Digital Ground 1	16	Digital Ground 2
2	$+V_{REF}$	15	Overflow Output
3	V_{AIN}	14	D6 (MSB)
4	$-V_{REF}$	13	D5
5	Hysteresis Control	12	D4
6	Encode	11	D3
7	$+V_S$	10	D2
8	$-V_S$	9	D1 (LSB)

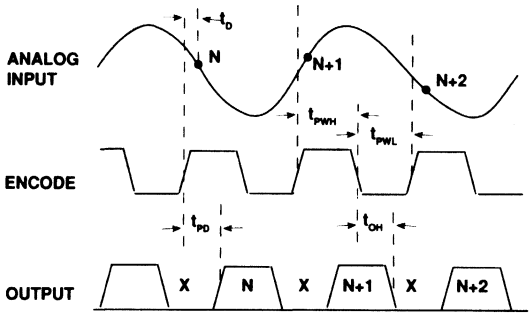


DIGITAL OUTPUT CODING

Analog Input	Overflow	MSB					LSB
$-V_{REF}$	0	0	0	0	0	0	0
$V_{REF}+{}^1/_2$LSB	0	0	0	0	0	0	Ø
$-{}^1/_2$LSB	0	Ø	Ø	Ø	Ø	Ø	Ø
0V	0	1	0	0	0	0	0
$+{}^1/_2$LSB	0	1	0	0	0	0	Ø
$+V_{REF}-1{}^1/_2$LSB	0	1	1	1	1	1	Ø

Analog Input	Overflow	MSB					LSB
$+V_{REF}$-1LSB	0	1	1	1	1	1	1
$+V_{REF}$-½LSB (MN5905)	Ø	1	1	1	1	1	1
$+V_{REF}$-½LSB (MN5904)	Ø	Ø	Ø	Ø	Ø	Ø	Ø
$+V_{REF}$-(MN5905)	1	1	1	1	1	1	1
$+V_{REF}$-(MN5904)	1	0	0	0	0	0	0

NOTE: The symbol Ø Indicates a bit transition, in which the indicated bit is alternating between "0" and "1".



t_D - **Aperture Delay**
t_{PD} - **Output Propagation Delay**
t_{OH} - **Minimum Output Hold Time**
t_{PWH} - **Minimum Encode Pulse Width High**
t_{PWL} - **Minimum Encode Pulse Width Low**
x - **Output data not valid**
N - **Data from sample N**

Figure 2. **Timing Diagram**

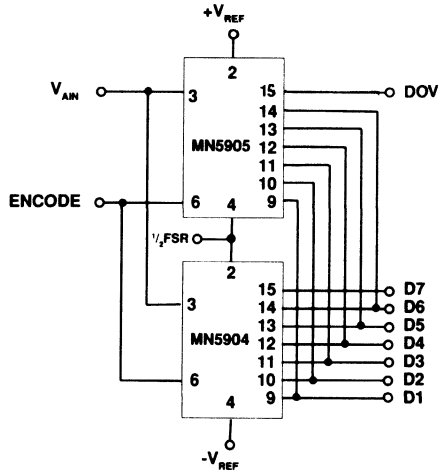


Figure 3. **Cascaded 7-Bit Operation**

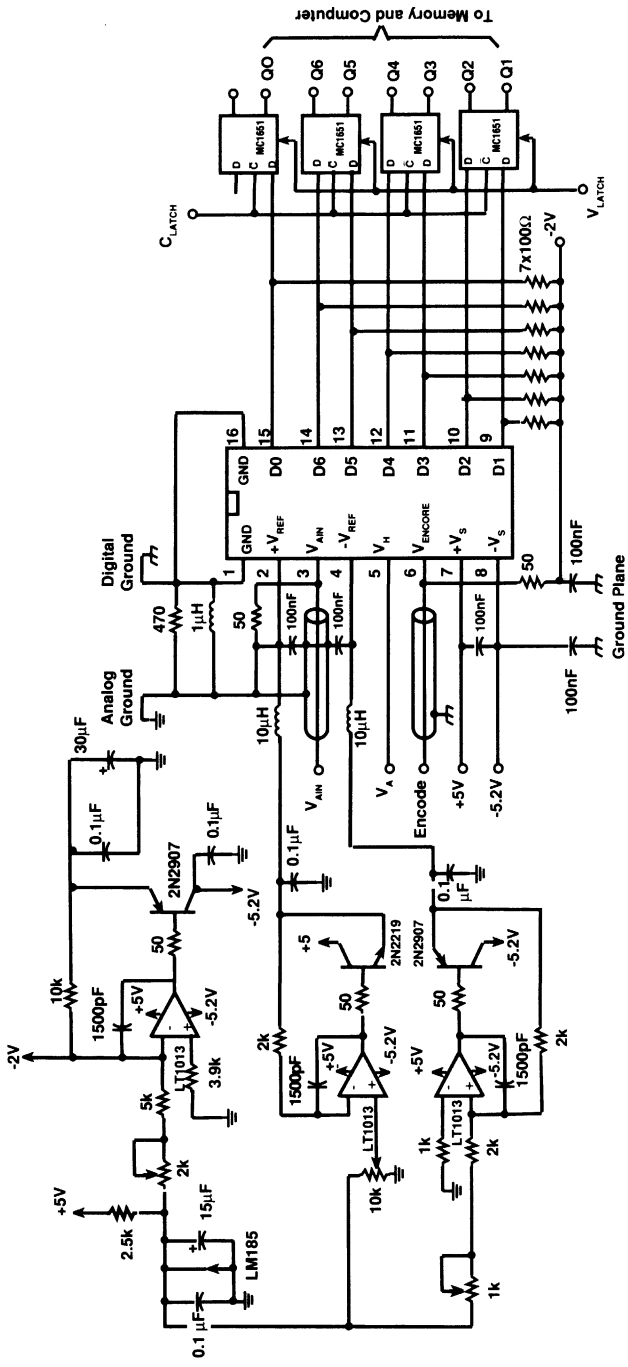


Figure 4. **Reference Drive**

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MN5906

6-Bit, 50MHz CMOS
FLASH A/D CONVERTER

FEATURES

- 6-Bit Resolution Plus Overflow Bit
- 50MHz Typical Conversion Rate
- Single +5V Operation
- Low Input Capacitance
- Low Power (190mW, typ.)
- Small 18-Pin Ceramic or Plastic DIP
- 3-State Outputs
- Optional Environmental Stress Screening

DESCRIPTION

The MN5906 is a high-speed, low-power, monolithic CMOS Flash A/D converter. The MN5906 converts analog input signals into six-bit digital words at an impressive 50MHz (typ) rate. The device's pipelined flash architecture contains 64 auto-zeroed comparators, reference resistor ladder, decode logic and output 3-state latches. An intermediate tap is provided for user adjustments of integral linearity.

The converter provides six TTL-compatible output bits plus an overflow flag signal. Overflow can be used in conjunction with 3-state output controls to stack multiple MN5906's for higher resolution applications.

The MN5906 is available for commercial/industrial applications in both ceramic side-brazed and plastic DIP packages. The MN5906 H/B is also available with Environmental Stress Screening for application in military/aerospace systems.

Model Number	Package	Temperature Range	Mil
MN5906PD	Plastic DIP	0°C to +70°C	No
MN5906CD	Ceramic DIP	0°C to +70°C	No
MN5906PDE	Plastic DIP	-25°C to +85°C	No
MN5906CDE	Ceramic DIP	-25°C to +85°C	No
MN5906CDH	Ceramic DIP	-55°C to +125°C	No
MN5906CDH/B	Ceramic DIP	-55°C to +125°C	Yes

APPLICATIONS

Video

RADAR Systems

Pulse Measurement Systems

Subranging A/D Converters

Synchronous Demodulation

Infrared Imaging

Communications

This data sheet contains preliminary information regarding the MN5906. Please contact the factory for up-to-date performance and product information.

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324 Clark St., Worcester, MA 01606 (508) 852-5400

April 1992
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MN5906 6-Bit, 50MHz CMOS FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN5906PD, CD	0°C to +70°C
MN5906PDE, CDE	−25°C to +85°C
MN5906CDH, CDH/B	−55°C to +125°C
Storage Temperature Range	
MN5906PD, PDE	−65°C to +100°C
MN5906CDE, CDH, CDH/B	−65°C to +150°C
Power Supply Voltages (+V_{DD}, Pins 5, 6)	−0.5 to +7.0 Volts
Digital Inputs (Pins 3, 4, 18)	−0.5 to +V_{DD} +0.5 Volts
Analog Input (Pin 8)	−0.5 to +V_{DD} +0.5 Volts

ORDERING INFORMATION

PART NUMBER — **MN5906 CD H/B**

Select suffix "PD" for plastic DIP or "CD" for ceramic DIP.

Standard "PD" and "CD" are specified for 0°C to +70°C operation.

Add "E" suffix to models for specified −25°C to +85°C operation.

Add "H" suffix to "CD" models for specified −55°C to +125°C operation.

Add "/B" suffix to "CDH" models for Environmental Stress Screening.

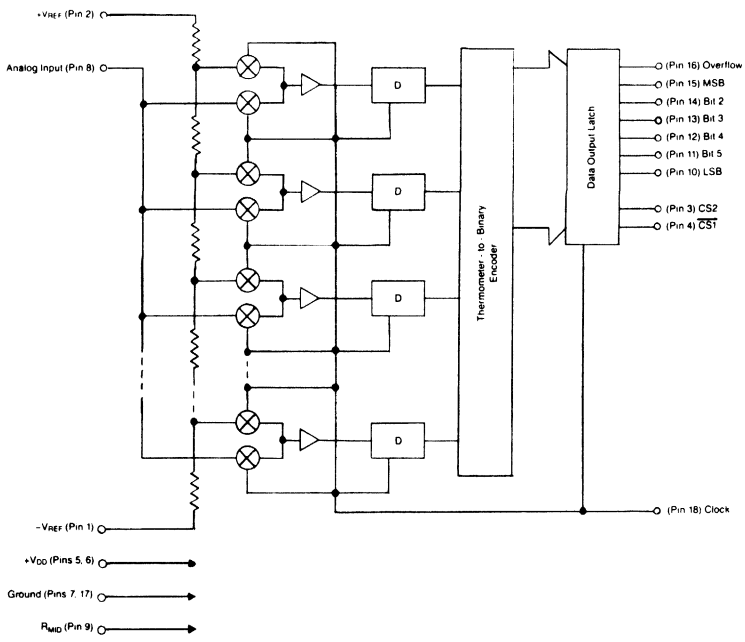
SPECIFICATIONS (T_A = +25°C, Supply Voltage +V_{DD} = +5V, V_{REF} = +2.75V, f_{CLK} = 35 MHz unless otherwise indicated)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to V_{REF}		Volts
Input Capacitance		12		pF
Full Power Bandwidth		100		MHz
REFERENCE INPUTS				
Reference Voltage (+V_{REF})		+2.75		Volts
Reference Ladder Resistance		90		Ω
Reference Ladder Tempco		0.3		Ω/°C
DIGITAL INPUTS				
Logic Levels: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
Logic Loading: Logic "1" (V_{IH} = +4.5V)		+1	+5	μA
Logic "0" (V_{IL} = +0.5V)		−1	−5	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{OH} = 4mA)	+4.5			Volts
Logic "0" (I_{OL} = 4mA)			+0.4	Volts
TRANSFER CHARACTERISTICS				
Integral Linearity Error (Notes 1, 2)		± ¾	± 1	LSB
Differential Linearity Error (Notes 1, 3)		± ¼	± ¾	LSB
DYNAMIC PERFORMANCE				
Conversion Rate	35	50		MHz
Aperture Delay		5		nsec
Output Propagation Delay	10	14	20	nsec
Signal-to-(Noise and Distortion) Ratio (SINAD)				
f_{AIN} = 1MHz	34			dB
f_{AIN} = 10MHz	33			dB
Spurious Free Dynamic Range (SFDR)				
f_{AIN} = 1MHz	43			dB
f_{AIN} = 10MHz	37			dB
POWER SUPPLY				
Power Supply Voltage (+V_{DD} Supply)	+4.75	+5	+5.25	Volts
Power Supply Current (+V_{DD} Supply)		+38		mA

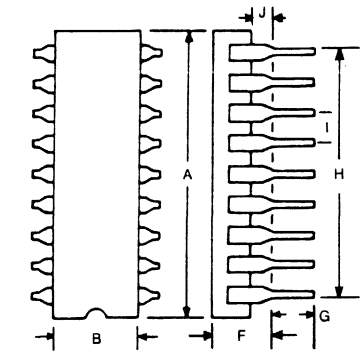
SPECIFICATION NOTES:

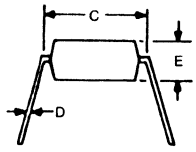
1. Measured while operating at specified conversion rate
2. Integral Linearity Error is specified using transfer function endpoints often times referred to as endpoint linearity
3. Differential Linearity Error measurements are based on code transitions

BLOCK DIAGRAM



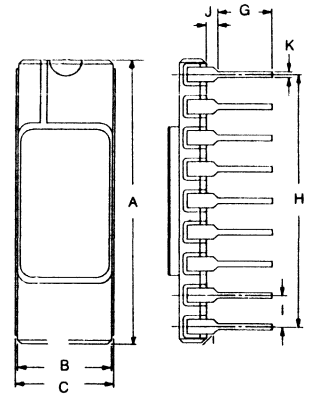
PACKAGE OUTLINES

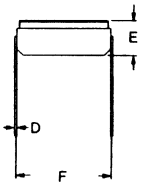




DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.845	0.925	21.47	23.49
B	0.240	0.280	6.10	7.11
C	0.300	0.325	7.62	8.25
D	0.008	0.015	0.204	0.381
E	0.115	0.195	2.93	4.95
F	—	0.210	—	5.33
G	0.125	0.200	3.18	5.05
H	0.800 BASIC		20.32 BASIC	
I	0.100 BASIC		2.54 BASIC	
J	0.015	0.060	0.380	1.52

Package A
for "PD" devices





DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.890	0.910	22.61	23.11
B	0.285	0.305	7.24	7.75
C	0.300	0.320	7.62	8.13
D	0.008	0.015	0.20	0.38
E	—	0.123	—	3.12
F	0.300	BASIC	7.62	BASIC
G	0.140	0.160	3.56	4.06
H	0.800 BASIC		20.32 BASIC	
I	0.100 BASIC		2.54 BASIC	
J	0.025	0.045	0.64	1.14
K	0.016	0.020	0.41	0.51

Package B
for all "CD" devices.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—The MN5906, CMOS Flash A/D converter, operates in a pipelined fashion such that two operations are performed during each phase of the clock. In the first high phase of the clock, the 64 internal comparators are auto-zeroed. During the subsequent low phase of the clock, the analog input signal is sampled by the 64 comparators. The so-called "thermometer code" output of these comparators represents the digitized value of the sampled analog input signal. During the next high phase of the clock, the thermometer code of the "nth" conversion is latched internally and propagates through the internal encoder while the 64 comparators are auto-zeroed for the "n+1" conversion. Valid output data is latched to the digital outputs on the next negative clock transition while the "n+1" sample is taken by the 64 comparators. See the Timing Diagram.

LAYOUT AND GROUNDING CONSIDERATIONS — The MN5906 and other high-speed devices require that careful consideration be given to high-speed and low-noise design techniques. The pinout of the MN5906 has been carefully chosen to maintain as much separation of digital and analog signals as possible. The use of ground and power planes and signal shielding is highly recommended. Bypass capacitors of 0.01 and 0.001 μf should be used and located as close to the device as possible.

It is also recommended that circuits interfacing with the MN5906 (such as data latches, etc.) be located within 2 inches of the device to avoid transmission line effects (rise and fall times of the MN5906 output drivers are 2nsec or less implying frequency components in the hundreds of MHz).

EVALUATION BOARDS — The MN5906 is supported with an evaluation board, the MN5906EVB. This evaluation board embodies the concepts discussed above and is a complete subsystem. The MN5906EVB has an onboard reference, signal gain and offset circuits, and operates from user supplied ± 5V power supplies. The EVB accepts a 1Vp-p bipolar analog input signal and provides both digital (latched from a 74F574) and reconstructed analog (via the onboard D/A converter) output signals.

Please contact the factory for information regarding the MN5906EVB as well as additional applications information regarding the application of high-speed CMOS Flash A/D converters.

PIN DESCRIPTIONS

PIN	NAME	SYMBOL	DESCRIPTION
1, 2	Reference Inputs	$-V_{REF}$, $+V_{REF}$	Bottom and top of the reference resistor string. $-V_{REF}$ normally tied to GND, $+V_{REF}$ normally tied to +2.75 Volts.
3	3-State Control (Overflow and Data Bits)	CS2	Overflow bit valid when CS2 = Logic "1". Output bits and overflow bit in high-impedance state when CS2= Logic "0". See Truth Table.
4	3-State Control (Data Bits)	$\overline{CS1}$	Data bits valid when $\overline{CS1}$ = Logic "0". Data bits in high-impedance state when $\overline{CS1}$ = Logic "1". $\overline{CS1}$ is a "don't care" (X) when CS2 is a Logic "0". See Truth Table.
5, 6	Power Supply	$+V_{DD}$	Connected to +5V Supply for normal operation.
7	Ground	GND	Connected to System Analog Ground plane.
8	Analog Input	A_{IN}	Connect analog input signal to be digitized. Nominally 0V to $+V_{REF}$.
9	Referehce Resistor Midpoint	R_{MID}	Midpoint tap to resistor ladder.
10,11,12, 13,14,15	Data Output Bits	B6-B1	Digital Output Bits.
16	Overflow Bit	OF	Set to a Logic "1" when analog input exceeds $+V_{REF}$ $-½$LSB.
17	Ground	GND	Connected to System Analog Ground plane.
18	Clock	CLK	Clock Input.

DIGITAL OUTPUT CODING

ANALOG INPUT	OF	MSB				LSB	
$+V_{REF}$	1	1	1	1	1	1	1
$+V_{REF} - ½$LSB	Ø	1	1	1	1	1	1
$+V_{REF} - 1$LSB	0	1	1	1	1	1	1
$+V_{REF} - 3/2$LSB	0	1	1	1	1	1	Ø
$+½V_{REF} + ½$LSB	0	1	0	0	0	0	Ø
$+½V_{REF} - ½$LSB	0	Ø	Ø	Ø	Ø	Ø	Ø
$+½V_{REF} - 3/2$LSB	0	0	1	1	1	1	Ø
$+½$LSB	0	0	0	0	0	0	Ø
0	0	0	0	0	0	0	0

Analog inputs indicated are the theoretical values for the transitions of codes indicated above. With the converter continuously converting, the output bit indicated as Ø will change from Logic "0" to Logic "1" or vise versa as the input voltage passes through the indicated level.

TRUTH TABLE

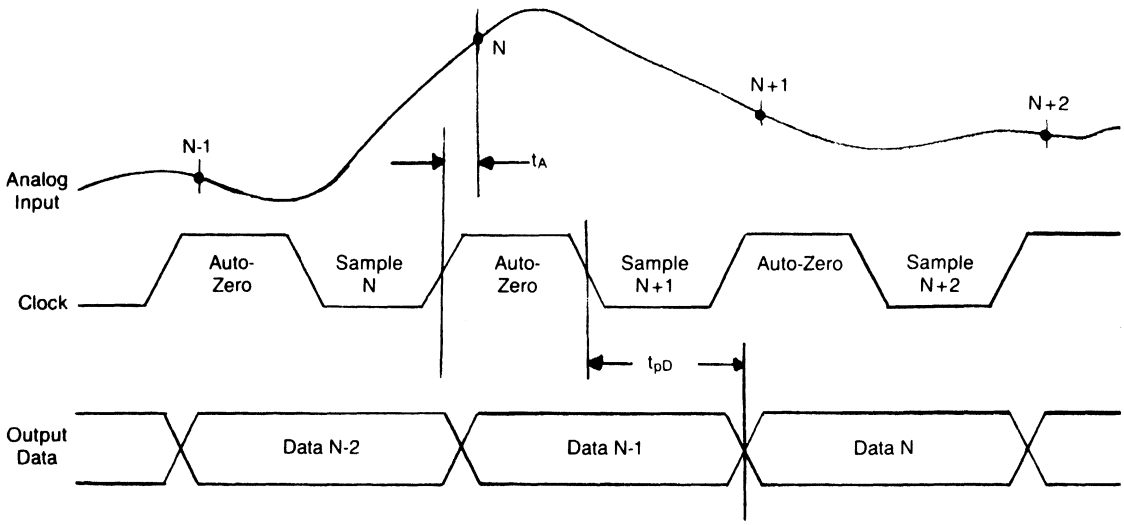
$\overline{CS1}$	CS2	B1 - B6	OF
0	1	Valid	Valid
1	1	High-Z	Valid
X	0	High-Z	High-Z

PIN DESIGNATIONS

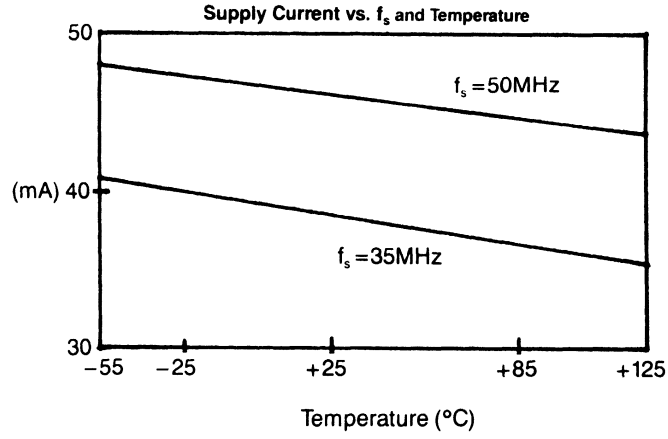


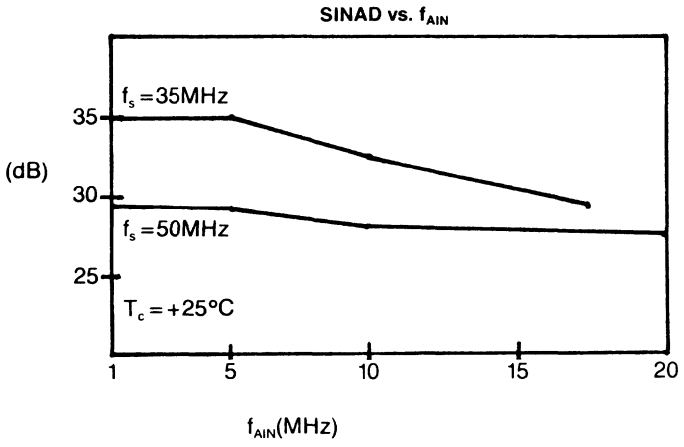
1	$-V_{REF}$	18	Clock Input
2	$+V_{REF}$	17	Ground
3	3-State Control (CS2)	16	Overflow
4	3-State Control ($\overline{CS1}$)	15	Bit 1 (MSB)
5	$+V_{DD}$ Supply	14	Bit 2
6	$+V_{DD}$ Supply	13	Bit 3
7	Ground	12	Bit 4
8	Analog Input	11	Bit 5
9	Reference Ladder Midpoint	10	Bit 6 (LSB)

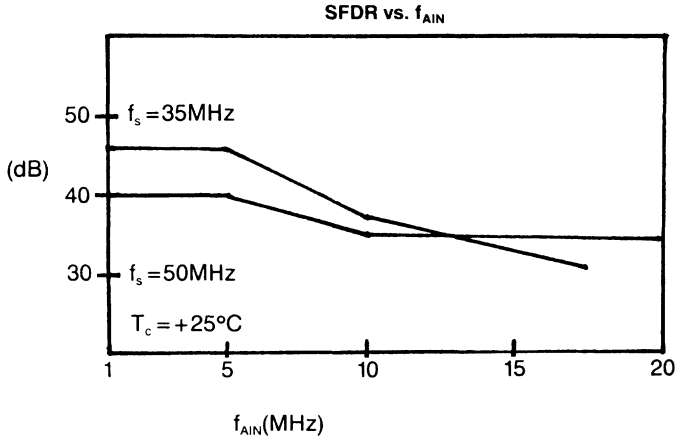
TIMING DIAGRAM

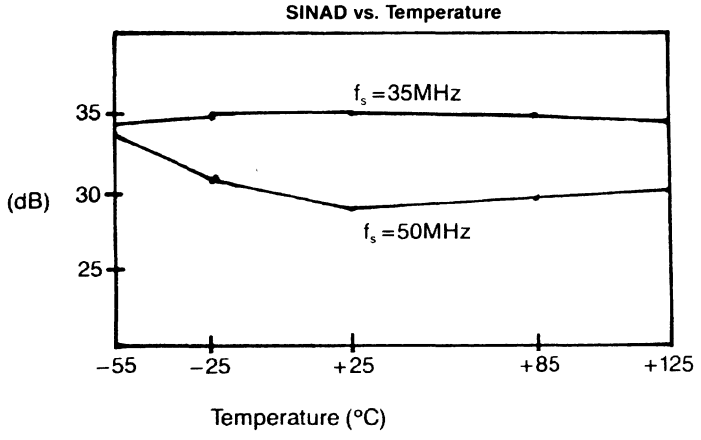


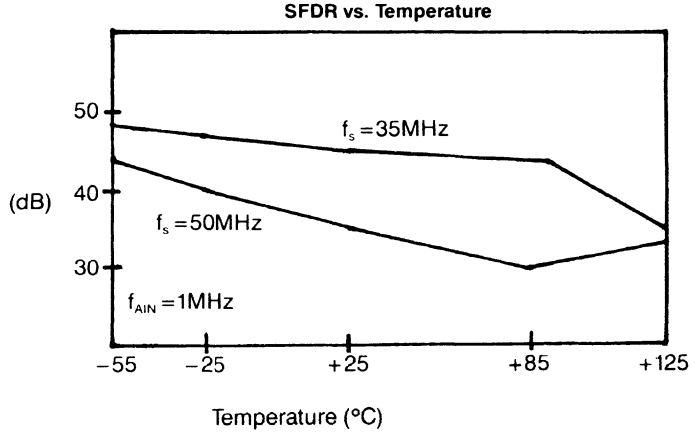
TIMING NOTES:
1. Aperture Delay (t_A) is 5nsec (typ.).
2. Output Propagation Delay (t_{pD}) is 14nsec (typ.).



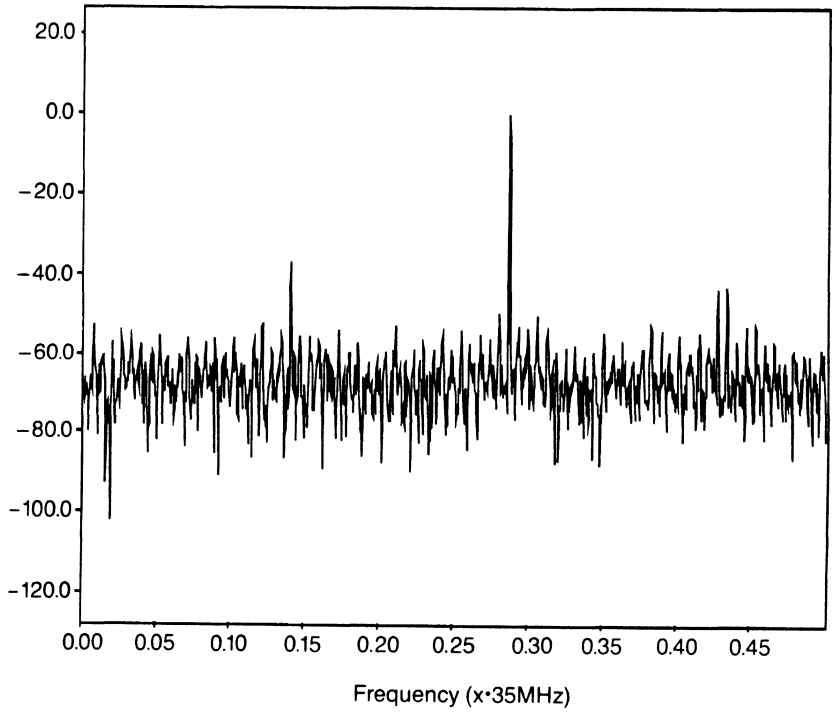

SINAD vs. f_{AIN}
f_s =35MHz
f_s =50MHz
T_c = +25°C
(dB)
35
30
25
1
5
10
15
20
f_{AIN}(MHz)


SFDR vs. f_{AIN}
f_s =35MHz
f_s =50MHz
T_c = +25°C
(dB)
50
40
30
1
5
10
15
20
f_{AIN}(MHz)

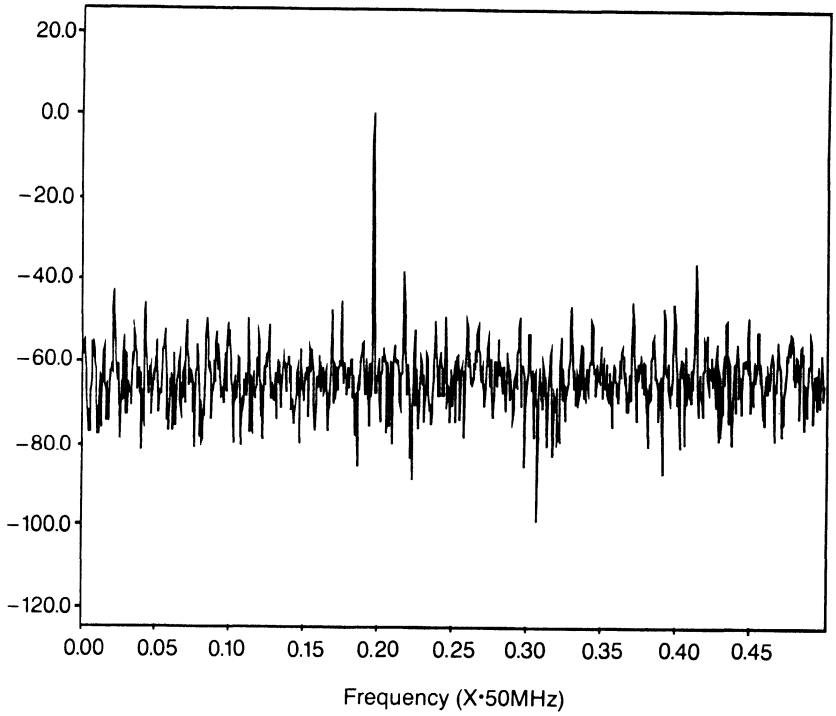

SINAD vs. Temperature
f_s =35MHz
f_s =50MHz
(dB)
35
30
25
−55
−25
+25
+85
+125
Temperature (°C)

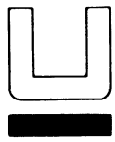

SFDR vs. Temperature
f_s =35MHz
f_s =50MHz
f_{AIN} =1MHz
(dB)
50
40
30
−55
−25
+25
+85
+125
Temperature (°C)

35MHz Sampling Rate, 10.032MHz Input Signal



50MHz Sampling Rate, 9.79MHz Input Signal





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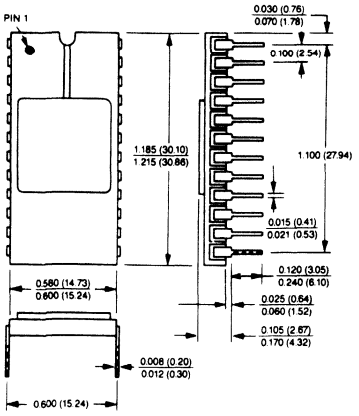
MN5908

8-Bit, 15MHz CMOS FLASH A/D CONVERTER

FEATURES

- **15MHz Guaranteed Sampling Rate**
- **Single +5V Supply Operation**
- **Low Harmonic Distortion**
- **Latched 3-State Outputs**
- **Easy Cascading to 9 Bits**
- **Low 350mW Power Consumption**
- **Small 24-Pin DIP**
- **−55°C to +125°C Operating Temperature Range**
- **Optional Environmental Stress Screening**

24 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5908 is a high-speed, 8-bit monolithic CMOS Flash A/D converter that provides a guaranteed 15MHz sampling rate over its full operating temperature range. Operating from a single +5V supply, the MN5908 provides high-speed performance while consuming less power than other available 8-bit, 15MHz devices. Its 3-state transparent data outputs include an overflow signal that allows easy cascading of two devices to obtain 9-bit resolution.

The MN5908 utilizes 255 CMOS sampling comparators to convert the analog input signal into a digital output word; one additional comparator provides an overflow signal when an input overrange condition occurs. Proprietary circuitry auto-zeros the comparators during each conversion to eliminate any dc offset errors that might arise from comparator mismatches. The MN5908 operates in a transparent mode, which allows one-shot operation for subranging and sampling applications. A companion device, the MN5902, operates in a pipelined fashion providing improved performance (20MHz sampling rate).

Outstanding performance features of the MN5908 include guaranteed maximum differential and integral linearity specifications as well as no-missing-codes performance over the full operating temperature range. The MN5908 is specified for 0°C to +70°C operation; the MN5908E is specified for −25°C to +85°C operation while the MN5908H is specified for −55°C to +125°C operation. For military/aerospace applications, the MN5908H/B is available with Environmental Stress Screening.

APPLICATIONS

RADAR Systems
Analytical Systems
ECM Equipment
Medical Imaging
Digital Oscilloscopes
Video Digitizers
Optical Scanners
Video Digitizers
Waveform Analyzers
Thermal Imagers/Video

This data sheet contains preliminary information regarding the MN5908. Please contact the factory for up-to-date performance and product information.

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MN5908 8-Bit, 15MHz CMOS FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN5908	0°C to +70°C
MN5908H or MN5908H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+5V Supply (Pin 1, 10, 19)	−0.5 to +7.0 Volts
Digital Inputs (Pins 2, 11, 12)	−0.5 to +5.5 Volts
Digital Outputs: (Pins 13-17, 21-24)	−0.5 to +5.5 Volts
(Short-circuit protected to Ground)	
Analog Input	−0.5 to V_{DD} +0.5 Volts

ORDERING INFORMATION

PART NUMBER — **MN5908 H/B**

Standard device is specified for 0°C to +70°C operation.

Add "E" suffix for −25°C to +85°C operation. Add "H" suffix for −55°C to +125°C operation.

Add "/B" suffix to "H" model for Environmental Stress Screening.

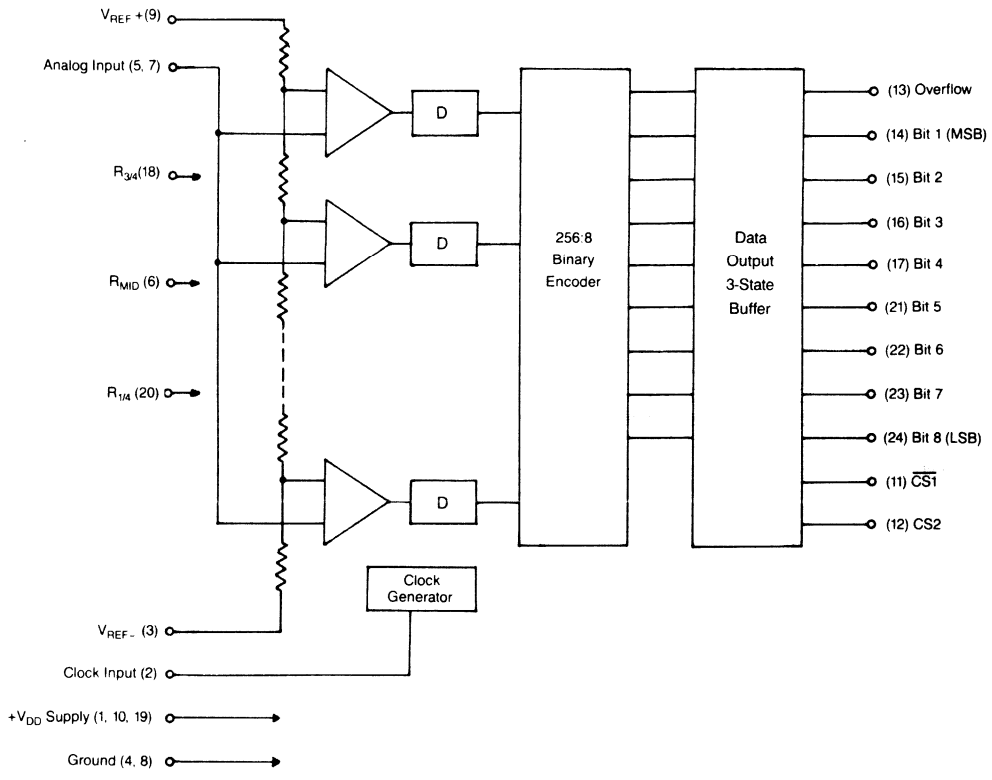
SPECIFICATIONS (T_A = +25°C, V_{DD} = +5.0V, V_{REF+} = +3.0V, V_{REF-} = 0V, and sampling rate = 15MHz unless otherwise indicated)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	0		3.5	Volts
Input Capacitance: Static		10		pF
Dynamic		32		pF
REFERENCE INPUTS				
Reference Ladder Resistance		300		Ohms
Reference Input Range	+0.5	+3.0	+3.5	Volts
DIGITAL INPUTS				
Logic Levels: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
Logic Currents: Logic "1" (V_{IH} = +4.0V)		+0.01	+5	μA
Logic "0" (V_{IL} = +0.4V)		−0.01	−5	μA
Minimum Clock Pulse Width	25			nsec
DIGITAL OUTPUTS				
Logic "1" Voltage at 4mA Load	4.5	4.9		Volts
Logic "0" Voltage at 4mA Load		0.1	0.4	Volts
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Differential Linearity: Initial		±0.35	±0.6	LSB
Over Temperature		±0.4	±0.6	LSB
Integral Linearity: Initial (Note 1)		±0.85	±1.0	LSB
Over Temperature		±1.5	±1.8	LSB
No Missing Codes	Guaranteed Over Temperature			
Zero-Scale Offset (Note 2)		40	70	mV
Gain Error: Initial			1.0	LSB
Over Temperature			1.5	LSB
DYNAMIC PERFORMANCE				
Sampling Rate	15			MHz
Signal-to-Noise Ratio		TBD		dB
Total Harmonic Distortion (4MHz Analog Input)		−48	−44	dB
Full-Power Bandwidth	40	50		MHz
Output Data-Valid Delay (From Rising Clock Edge)	10	20	25	nsec
Aperture Delay	−15	0	+15	nsec
Aperture Uncertainty		50		psec
POWER SUPPLY REQUIREMENTS				
Power Supply Range	+4.5	+5.0	+5.5	Volts
Power Supply Rejection		±0.01	+0.02	%FSR/%V_{DD}
Power Supply Current: Initial		+70	+80	mA
Over Temperature		+93	+100	mA

SPECIFICATION NOTES

1. Integral linearity specifications are based on end-point measurements, and assume an unadjusted reference mid-point.
2. Zero-scale offset is the difference between the measured input voltage required to produce the transition of code 00000000 to code 00000001, and the voltage theoretically corresponding to 0.5LSB.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The block diagram illustrates the architecture of the MN5908, a fully parallel 8-bit A/D converter. A total of 256 sampling comparators are used to convert the signal on the V_{IN} line to a digital word. The pulses at the CLK input are converted internally into the three phases that control the operation of the comparators. The first cycle, Phase 1, is initiated when the CLK switches to the high state. An analog switch at the input to each comparator then samples a reference voltage that is established by a 256-element resistor ladder between the V_{REF+} and V_{REF-} pins. Each unique reference-voltage tap represents one of the quantization levels to which the signal at V_{IN} will be compared.

Overlapping with Phase 1, the Phase 2 cycle serves to auto-zero the comparators. This operation has the purpose of cancelling dc-offset errors that arise from device mismatch between comparators. At the end of the Phase 2 interval, the capacitor at the input to each comparator stores the difference between the reference tap voltage and the auto-zeroed bias point. The capacitor will hold the comparator at a high-gain trigger point in preparation for sampling the input signal.

The low-going transition of the clock terminates the auto-zeroing interval and initiates the input-sampling interval. The Phase 3 period is non-overlapping with Phase 2 to minimize coupling of the reference to the input. A sampling glitch will be observed on the V_{IN} line at the beginning of Phase 3, as the input buffer amplifier must charge or discharge the coupling capacitors from their reference levels to the new level of the input signal. The comparators serve as track-and-hold amplifiers over the duration of the sampling interval. When the clock returns high, the sampling switches are turned off and the comparator levels are latched into flip-flops.

To determine the quantized level of the input signal, it is necessary to find the transition points between comparators that produce logic "1" results and those that produce logic "0" results. This transition point, corresponding to the signal residing at the end of the sampling interval, will lie within a 1-LSB (least-significant-bit) voltage range. This function of thermometer decoding is fulfilled by the 3-input NAND gates at the output of each comparator latch.

The thermometer decoder will cause just one of the 256 NAND gates to assume a low-level output. This signal will represent an address to the 256-to-8 encoder, which can then produce a properly encoded binary output. The MN5908 utilizes unlatched output circuitry in a non-pipelined fashion. Digital inputs, $\overline{CS1}$ and CS2, are used to set the outputs to the high-impedance state.

The transparent, or non-pipelined mode of operation reduces the conversion cycle to 1.5 clock cycles. This mode allows the MN5908 to be utilized in applications where one-shot digitizing of the analog signal is required. The Clock Input can be held indefinitely in the high-state, then pulsed low to sample the input signal. Output data then propagates out after the Clock Input returns high. See the Timing Diagram.

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (VDC)	OVERFLOW	DIGITAL OUTPUT MSB	LSB
$+V_{REF}$	1	1111	1111
$+V_{REF}-1/2LSB$	Ø	1111	1111
$+V_{REF}-LSB$	0	1111	1111
$+V_{REF}-3/2LSB$	0	1111	111Ø
$+1/2V_{REF}+1/2LSB$	0	1000	000Ø
$+1/2V_{REF}-1/2LSB$	0	ØØØØ	ØØØØ
$+1/2V_{REF}-3/2LSB$	0	0111	111Ø
+1/2LSB	0	0000	000Ø
0	0	0000	0000

LAYOUT AND GROUNDING CONSIDERATIONS — The MN5908 and other high-speed devices require that careful consideration be given to high-speed and low-noise design techniques. Care must be taken to assure that seperation of analog signals and digital signals is maintained. The use of ground and power planes as well as signal shielding are highly recommended. Bypass capacitors should be used and located as close to the device as possible. It is also recommended that circuitry interfacing to the MN5908 be located as close to the device as possible to minimize transmission line effects.

3-STATE OUTPUT CONTROL — Both $\overline{CS1}$ and CS2 can be used to enable the 8-bit output lines or to set them to the high-impedance state. $\overline{CS1}$ controls the 8-bit output lines, while CS2 controls both the output lines and the Overflow output. This arrangement makes it possible to stack two devices in a 9-bit configuration, in which Overflow becomes the MSB (most-significant bit), and to select the lower eight bits from either the upper or lower A/D converter.

TRUTH TABLE

$\overline{CS1}$	CS2	B1 — B8	OVERFLOW
0	1	Valid	Valid
1	1	High-Z	Valid
X	0	High-Z	High-Z

INTERMEDIATE RESISTOR TAPS — Intermediate taps at each quarter point of the reference resistor ladder are brought out to package pins. In high-speed operation, it is necessary to provide capacitive decoupling of these points to ground in order to prevent clock noise from interfering with the conversion. It is possible to adjust the dc potentials at these points to trim integral linearity, or to obtain a non-linear transfer characteristic.

CASCADING FOR 9-BIT OPERATION — It is possible to stack or cascade two MN5908 Flash A/D converters to configure a 9-bit digitizer. Cascading entails connecting the reference-resistor ladders in two devices in series. The bottom of the upper converter's ladder ($V_{REF}-$) connects to the top of the lower converter's ladder ($V_{REF}+$). The reference voltage source is connected to $V_{REF}+$ of the upper converter while the $V_{REF}-$ connection of the lower converter is tied to ground. Mid-scale of the cascaded A/D system is established at the point where the lower A/D converter overflows.

The Overflow output from the lower A/D converter detects the overflow condition and becomes the MSB of the 9-bit system, and in addition, serves to multiplex the lower eight bits between the two A/D converters.

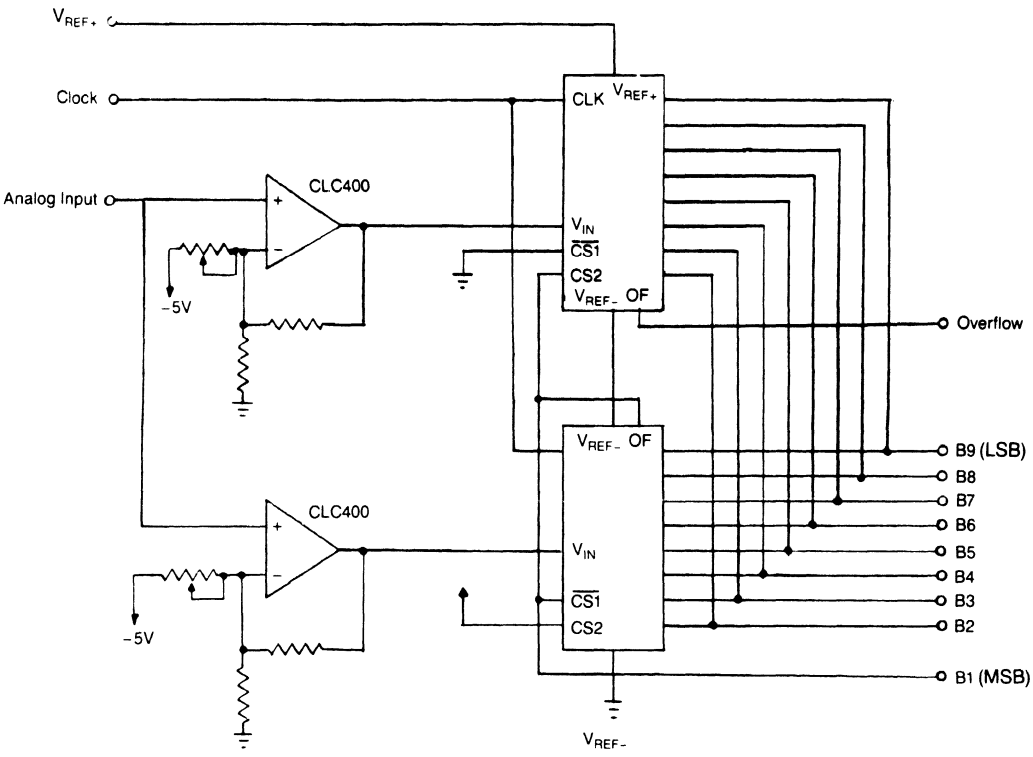
Two output controls are provided by the MN5908. CS2 controls the 3-state output function of the eight data output bits plus the overflow output. A logic "1" applied to the CS2 input enables these outputs while a logic "0" forces the output into the high-impedance state. $\overline{CS1}$ only has an effect on the eight data output bits. A logic "0" applied to $\overline{CS1}$ enables these data lines while a logic "1" forces them into the high-impedance state.

In the cascaded configuration, the MSB is set high (upon the overflow condition of the lower 8-bit A/D converter), it disables the lower data output bits while enabling the output bits and overflow bits of the upper A/D converter. Because the upper A/D converter is experiencing an underflow condition at the crossover point, a proper mid-scale code is produced. A 9-bit system overflow signal is available from the upper A/D converter.

The use of signal input buffer amplifiers are recommended in cascading applications. Separate signal paths for each A/D converter provide several benefits. First, input bandwidth and settling time performance in the switched-capacitor input of each MN5908 will benefit from being driven from a unique source. Secondly, offset and gain errors in each A/D will manifest themselves as large differential and integral linearity errors in the output transfer function of the 9-bit system.

To minimize these errors, it is possible to effect separate adjustments on the CLC400 current-feedback amplifiers. The offset potentiometer of the upper amplifier provides an adjustment for system differential linearity at the mid-scale point. The gain of the amplifiers provide a means for achieving gain matching between the two eight-bit devices thereby allowing trim of the system integral linearity error. The expression for the gain is 1+RF/Req, where Req is the parallel combination of the resistors at the amplifiers input with the feedback path disconnected. Because gain and offset are interrelated, the offset potentiometer should be large relative to the other resistor (10K Ohms for example).

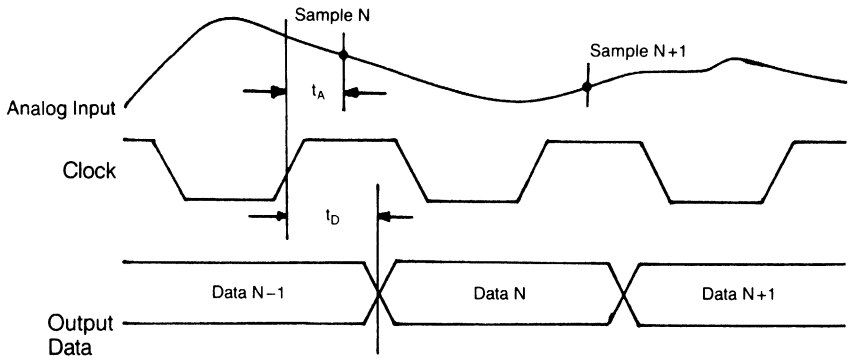
Figure 3. MN5908 9-Bit Cascade Connection



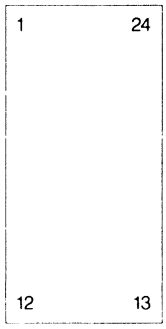
PIN DESCRIPITONS

PIN	SYMBOL	FUNCTIONAL DESCRIPTION
1	V_{DD}	Supplies power to analog and digital sections of chip. Nominal level +5V.
2	CLK	Externally supplied clock signal; used internally to generate three distinct phases for the comparator sampling sequence and comparator latches.
3	V_{REF-}	Voltage potential at the bottom of the resistor ladder that sets the lower limit of the A/D converter's range. Also sets the offset code for 0 to 1 transition.
4	GND	Ground potential for the analog and digital circuitry. Also the silicon substrate potential.
5	V_{IN}	The analog signal input to the lower half of the A/D converter.
6	R_{MID}	Midpoint of the resistor ladder, at the boundary between codes 128 and 129. Normally decoupled through a capacitor to ground, but may be used to adjust linearity or to impart a non-linear transfer function.
7	V_{IN}	The analog signal input to the upper half of the A/D converter.
8	GND	Ground potential for the analog and digital circuitry. Also the silicon substrate potential.
9	V_{REF+}	Voltage potential to the top of the resistor ladder that sets the upper limit of the A/D converter's range. Can be used to make gain adjustments. Nominally +3.0V.
10	V_{DD}	Supplies power to analog and digital sections of chip. Nominal level +5V.
11	$\overline{CS1}$	3-state control for output bits B1 to B8. When CS2 is high, output bits are enabled (When $\overline{CS1}$ is low). $\overline{CS1}$ is a don't care (X) when CS2 is low.
12	CS2	3-state control for output bits B1 to B8 and the Overflow output. When CS2 is high, output bits B1 to B8 are enabled if $\overline{CS1}$ is low. CS2 has independent control of the Overflow output. If CS2 is low, B1 to B8 and Overflow are in the high-impedance state.
13	OF	When high, Overflow indicates that the input voltage exceeds the top reference tap point, nominally V_{REF+} −½LSB. Outputs B1 to B8 assume all "1's" when Overflow is high.
14	B1	(MSB) Most-significant bit of the digitized 8-bit output. Has a weight of FSR/2 where FSR (full-scale range) is $V_{REF+} - V_{REF-}$.
15	B2	2nd most-significant bit of the digitized 8-bit output. Has a weight of FSR/4.
16	B3	3rd most-significant bit of the digitized 8-bit output. Has a weight of FSR/8.
17	B4	4th most-significant bit of the digitized 8-bit output. Has a weight of FSR/16.
18	R3/4	3rd quarter point of the A/D converter's resisitor ladder, at the boundary between codes 64 and 65. Normally decoupled through a capacitor to ground, but can be used to adjust integral linearity or to impart a non-linear transfer function.
19	V_{DD}	Supplies power to analog and digital sections of chip. Nominal level +5V.
20	R1/4	1st quarter point of the A/D converter's resistor ladder, at the boundary between codes 64 and 65. Normally decoupled through a capacitor to ground, but can be used to adjust integral linearity or to impart a non-linear transfer function.
21	B5	5th most-significant bit of the digitized 8-bit output. Has a weight of FSR/32.
22	B6	6th most-significant bit of the digitized 8-bit output. Has a weight of FSR/64.
23	B7	7th most-significant bit of the digitized 8-bit output. Has a weight of FSR/128.
24	B8	(LSB) Least-significant bit of the digitized 8-bit output. Has a weight of FSR/256.

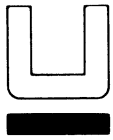
IMING DIAGRAM



'IN DESIGNATIONS



1 $+V_{DD}$ Supply	24 Bit 8 (LSB)
2 Clock	23 Bit 7
3 V_{REF-}	22 Bit 6
4 Ground	21 Bit 5
5 Analog Input	20 $R_{1/4}$
6 R_{MID}	19 $+V_{DD}$
7 Analog Input	18 $R_{3/4}$
8 Ground	17 Bit 4
9 V_{REF+}	16 Bit 3
10 $+V_{DD}$	15 Bit 2
11 $\overline{CS1}$	14 Bit 1 (MSB)
12 CS2	13 Overflow



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MN5909

6-Bit, 100MHz CMOS
FLASH A/D CONVERTER

FEATURES

- **6-Bit Resolution Plus Overflow Bit**
- **100MHz Typical Conversion Rate**
- **Single +5V Operation**
- **Low Input Capacitance**
- **Low Power (200mW, Typical)**
- **Externally-Strobed, Auto-Zeroed Comparators**
- **Small 20-Pin Ceramic or Plastic DIP**
- **3-State Outputs**
- **Optional Environmental Stress Screening**

DESCRIPTION

The MN5909 is a high-speed, low-power, monolithic CMOS Flash A/D converter. The MN5909 converts analog input signals into six-bit digital words at an impressive 100MHz (typ) rate. The device's transparent flash architecture contains 64 externally-strobed, auto-zeroed comparators, reference resistor ladder, decode logic and output 3-state buffers. An intermediate tap is provided for user adjustments of integral linearity.

The converter provides six TTL-compatible output bits plus an overflow flag signal. Overflow can be used in conjunction with 3-state output controls to stack multiple MN5909's for higher resolution applications.

The MN5909 is available for commercial/industrial applications in both ceramic side-brazed and plastic DIP packages. The MN5909H/B is also available with Environmental Stress Screening for application in military/aerospace systems.

Model	Package	Temp. Range	Mil
MN5909PD	Plastic DIP	0°C to +70°C	No
MN5909CD	Ceramic DIP	0°C to +70°C	No
MN5909PDE	Plastic DIP	−25°C to +85°C	No
MN5909CDE	Ceramic DIP	−25°C to +85°C	No
MN5909CDH	Ceramic DIP	−55°C to +125°C	No
MN5909CDH/B	Ceramic DIP	−55°C to +125°C	Yes

APPLICATIONS

Video

RADAR Systems

Pulse Measurement Systems

Infrared Imaging

Communications

High-Speed Digitizers

EW and ECM Systems

This data sheet contains preliminary information regarding the MN5909. Please contact the factory for up-to-date performance and product information.

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MN5909 6-Bit, 100MHz CMOS FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN5909PD, CD	0°C to +70°C
MN5909PDE, CDE	−25°C to +85°C
MN5909CDH, CDH/B	−55°C to +125°C
Storage Temperature Range	
MN5909PD, PDE	−65°C to +100°C
MN5906CD, CDE, CDH, CDH/B	−65°C to +150°C
$+V_{DD}$ Supply (Pins 5, 6, 7)	−0.5 to +7.0 Volts
Digital Inputs (Pins 3, 4, 19, 20)	−0.5 to $+V_{DD}$ +0.5 Volts
Analog Input (Pin 9)	−0.5 to $+V_{DD}$ +0.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5909 CD H/B

- Select suffix "PD" for plastic DIP or "CD" for ceramic DIP.
- Standard "PD" and "CD" are specified for 0°C to +70°C operation.
- Add "E" suffix to either "PD" or "CD" models for specified −25°C to +85°C operation.
- Add "H" suffix to "CD" models for specified −55°C to +125°C operation.
- Add "/B" suffix to "CDH" models for Environmental Stress Screening.

SPECIFICATIONS (T_A = +25°C, $+V_{DD}$ = +5V, V_{REF+} = +2.75V, V_{REF-} = 0.0V, f_{CLK} = 100 MHz unless otherwise indicated)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to $+V_{REF}$		Volts
Input Capacitance		12		pF
Full Power Bandwidth		100		MHz
REFERENCE INPUTS				
Reference Voltage (V_{REF+},)		+2.75		Volts
Reference Ladder Resistance		90		Ω
Reference Ladder Tempco		0.3		Ω/°C
DIGITAL INPUTS				
Logic Levels: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
Logic Currents: Logic "1"			+5	μA
Logic "0"			−5	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1"	+4.5			Volts
Logic "0"			+0.4	Volts
TRANSFER CHARACTERISTICS				
Integral Linearity Error		± ¾	± 1	LSB
Differential Linearity Error		± ¼	± ¾	LSB
No Missing Codes		Guaranteed		
DYNAMIC PERFORMANCE				
Conversion Rate		100		MHz
Aperture Delay		5		nsec
Output Propagation Delay	10	14	20	nsec
AC LINERITY				
Signal-to-(Noise and Distortion)				
f_{AIN} = 1MHz	34			dB
f_{AIN} = 10MHz	33			dB
Spurious Free Dynamic Range:				
f_{AIN} = 1MHz	43			dB
f_{AIN} = 10MHz	37			dB
POWER SUPPLY				
Power Supply ($+V_{DD}$ Supply)	+4.75	+5	+5.25	Volts
Power Supply Drain ($+V_{DD}$ Supply)		+40		mA

SPECIFICATION NOTES:

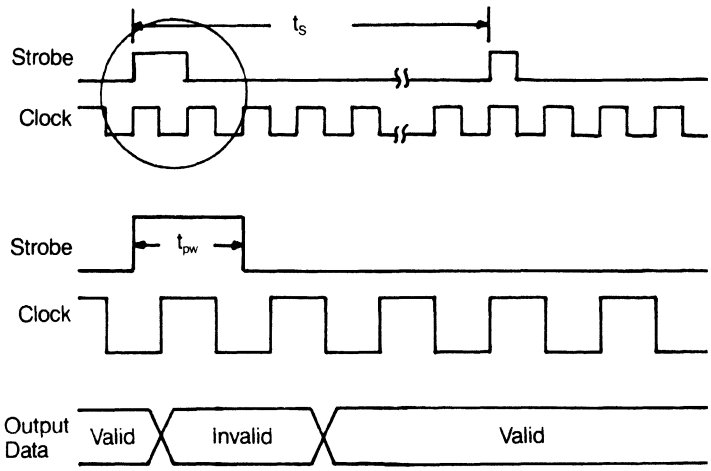
1. Measured while operating at specified conversion rate with an auto-zero pulse repitition rate of 40kHz.
2. Integral Linearity Error is specified using transfer function endpoints.
3. Differential Linearity Error measurements are based on code transitions.

IN DESIGNATIONS



1	V_{REF-}	20	Conversion Clock
2	V_{REF+}	19	Auto-zero Strobe
3	3-State Control (CS2)	18	Ground
4	3-State Control ($\overline{CS1}$)	17	Overflow
5	$+V_{DD}$ Supply	16	Bit 1 (MSB)
6	$+V_{DD}$ Supply	15	Bit 2
7	$+V_{DD}$ Supply	14	Bit 3
8	Ground	13	Bit 4
9	Analog Input	12	Bit 5
10	R_{MID}	11	Bit 6 (LSB)

ACKAGE OUTLINE

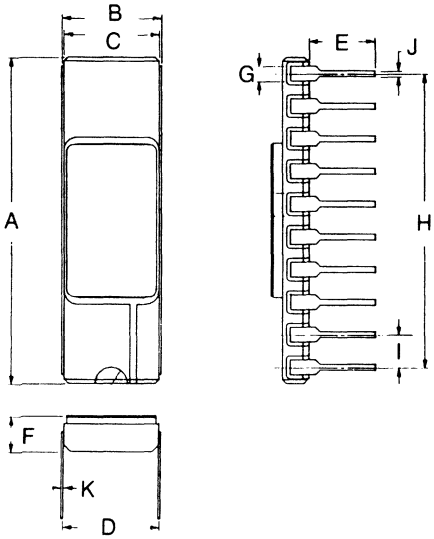


TIMING NOTES:

1. t_{pw} must be high for one full clock cycle. Strobe may be asynchronous with Clock.
2. t_s = Strobe repetition rate = 40kHz.
3. Output data is indeterminate when strobe = "1". Output data returns valid upon falling edge of clock after strobe returns to "0".

MN5909

J DESCRIPTIONS



	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	1.010	0.990	25.65	25.15
B	0.300	0.320	7.62	8.13
C	0.285	0.305	7.24	7.75
D	0.295	0.305	7.49	7.75
E	0.125	0.200	3.18	5.08
F	—	0.123	—	3.12
G	0.048	0.052	1.22	1.32
H	0.900 BASIC		22.86 BASIC	
I	0.100 BASIC		2.54 BASIC	
J	0.016	0.020	0.41	0.51
K	0.005	0.015	0.13	0.38

Package shown is for MN5909CD, CDE, CDH and CDH/B. Please contact factory for information regarding dimensions and availability of "PD" and "PDE" models.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN5909 6-Bit, 100MHz CMOS Flash A/D converter, operates in a transparent fashion with an externally supplied asynchronous, auto-zero pluse. Typical CMOS Flash A/D converters auto-zero the sampling comparators during each clock cycle. The MN5909's unique architecture utilizes an externally-applied asynchronous pulse to auto-zero the sampling comparators every 40,000 conversions (typically).

The auto-zero pulse must be high during a low-to-high transition of the applied conversion clock and must remain high for a minimum of one clock cycle. It is recommended that a 40kHz repetition rate of the auto-zero pulse be utilized.

Output data present during the auto-zero phase should be considered invalid.

LAYOUT AND GROUNDING CONSIDERATIONS — The MN5909 and other high-speed devices require that careful consideration be given to high-speed and low-noise design techniques. The pinout of the MN5909 has been carefully chosen to maintain as much separation of digital and analog signals as possible. The use of ground and power planes and signal shielding is highly recommended. It is recommended that bypass capacitors of 0.01 and 0.001 μF should used and located as close to the device as possible.

It is also recommended that circuits interfacing with the MN5909 (such as data latches, etc.) be located within 2 inches of the device to avoid transmission line effects (rise and fall times of the MN5909 output drivers are 2nsec or less implying frequency components in the hundreds of MHz).

PIN DESCRIPTIONS

PIN	NAME	SYMBOL	DESCRIPTION
1, 2	Reference Inputs	$-V_{REF}$, $+V_{REF}$	Bottom and top of the reference resistor string. $-V_{REF}$ normally tied to GND, $+V_{REF}$ normally tied to +2.75 Volts.
3	3-State Control (Overflow Bit)	CS2	Overflow bit valid when CS2 = Logic "1". Output bits and overflow bit in high-impedance state when CS2= Logic "0". See Truth Table.
4	3-State Control (Data Bits)	$\overline{CS1}$	Data bits valid when $\overline{CS1}$ = Logic "0". Data bits in high-impedance state when $\overline{CS1}$ = Logic "1". $\overline{CS1}$ is a "don't care" (X) when CS2 is a Logic "0". See Truth Table.
5, 6, 7	Power Supply	$+V_{DD}$	Connected to +5V Supply for normal operation.
8	Ground	GND	Connected to System Analog Ground plane.
9	Analog Input	A_{IN}	Connect analog input signal to be digitized. Nominally 0V to $+V_{REF}$.
10	Reference Resistor Midpoint	R_{MID}	Midpoint tap to resistor ladder.
11,12,13 14,15,16	Data Output Bits	B6-B1	Digital Output Bits.
17	Overflow Bit	OF	Set to a Logic "1" when analog input exceeds $+V_{REF}$ $-1/2$LSB.
18	Ground	GND	Connected to System Analog Ground plane.
19	Strobe	STB	Externally-applied auto-zero strobe pulse.
20	Clock	CLK	Clock Input.

DIGITAL OUTPUT CODING

ANALOG INPUT	OF	MSB					LSB
$+V_{REF}$	1	1	1	1	1	1	1
$+V_{REF} - 1/2$LSB	ø	1	1	1	1	1	1
$+V_{REF} - 1$LSB	0	1	1	1	1	1	1
$+V_{REF} - 3/2$LSB	0	1	1	1	1	1	ø
$+1/2V_{REF} + 1/2$LSB	0	1	0	0	0	0	ø
$+1/2V_{REF} - 1/2$LSB	0	ø	ø	ø	ø	ø	ø
$+1/2V_{REF} - 3/2$LSB	0	0	1	1	1	1	ø
$+1/2$LSB	0	0	0	0	0	0	ø
0	0	0	0	0	0	0	0

Analog inputs indicated are the theoretical values for the transitions of codes indicated above. With the converter continuously converting, the output bit indicated as ø will change from Logic "0" to Logic "1" or vise versa as the input voltage passes through the indicated level.

TRUTH TABLE

$\overline{CS1}$	CS2	B1 - B6	OF
0	1	Valid	Valid
1	1	High-Z	Valid
X	0	High-Z	High-Z

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Digital-to-Analog Converters

Digital-to-Analog Converters

Micro Networks offers a complete line of D/A converters ranging in resolution from 8 to 16-bits. Included are many 8-bit (MN3000 Series, MN3020), 12-Bit (MN3850, MN3860, DACHK, DAC85, DAC87, DAC88) and 16-bit (MN3290-I Series, MN3290-V Series, DAC71) devices that have become multisourced industry standards. We also have a complete line of high-speed D/A's with internal data input latches (MN3020, MN3040, MN3860, DAC88) to facilitate microprocessor interfacing.

The MN3290-I and MN3290-V Series of extended temperature range, 16-Bit D/A converters are targeted for application in the most demanding military/aerospace and industrial systems. The MN3290 devices are exactly pin-for-pin and function compatable with older, industry-standard DAC71/72 devices. A total of 36 different models (I-Out, V-Out, 0°C to +70°C, and −55°C to +125°C) makes the MN3290 Series suitable for almost any high-resolution, extended-temperature range application.

MN3290-I Series

Current-Output
Extended-Temperature
Range
16-Bit D/A Converters

FEATURES

- 16-Bit Resolution
- Fully Specified
  −55°C to +125°C Operation
- ±0.006% FSR Integral
  Linearity
- 14-Bit Monotonic
  Guaranteed Over Temperature
- Internal Reference
- Three Models:
  MN3290-I, 0 to −2mA, $R_F = 5k$
  MN3291-I, ±1mA, $R_F = 5k$
  MN3292-I, ±1mA, $R_F = 10k$
- Fast Output Settling:
  1μsec Max to ±0.003%FSR
- DAC71/72 Pin-for-Pin and
  Function Compatible
- DESC SMD 5962-89531
- MIL-STD-883 Screening
  Optional. MIL-STD-1772 Qualified
  Facility

MN3290-V Series

Voltage-Output
Extended-Temperature
Range
16-Bit D/A Converters

FEATURES

- 16-Bit Resolution
- Fully Specified
  −55°C to +125°C Operation
- ±0.006% FSR Integral
  Linearity
- 14-Bit Monotonic
  Guaranteed Over Temperature
- Internal Reference
  and Output Op Amp
- Three Models:
  MN3290-V, 0 to +10V
  MN3291-V, ±5V
  MN3292-V, ±10V
- Fast Output Settling:
  Full Scale Step to
  ±0.003%FSR, 8μsec Max
- DAC71/72 Pin-for-Pin and
  Function Compatible
- DESC SMD 5962-89531
- MIL-STD-883 Screening
  Optional. MIL-STD-1772 Qualified
  Facility

Digital-to-Analog Converters

Resolution	Model Number	Maximum Setting Time (μsec) (1)	Internal Ref. and Output Op Amp	Specified Temperature Range (°C)	Maximum Linearity Error (%FSR)	Monotonic Over Temperature	Power (mW)	DIP Package	Hi-Rel Option	DESC SMD (5962-)	Page No.
16-Bits	DAC71-V DAC71-I	10 1	Yes (2)	0 to +70	±0.003	(Note 3)	525	24 Pin	No	N.A.	7-9
	MN3290-V MN3290-I Series	8 1	Yes (2)	0 to +70 −55 to +125	±0.003	(Note 3)	525 435	24 Pin	Yes	8953103 8953104 8953102	7-51
12-Bits	DAC80-V DAC80-I	4 0.3 (Typ)	Yes (2)	0 to +70	±0.012	Yes	345	24 Pin	No	N.A.	7-13
	DAC85-V DAC85-I	4 0.3 (Typ)	Yes (2)	0 to +70 −25 to +85	±0.012	Yes	345	24 Pin	No	N.A.	7-17
	DAC87	4	Yes	−25 to +85 −55 to +125	±0.012	Yes	345	24 Pin	Yes	8300301	7-21
	DACHK	4	Yes	0 to +70 −55 to +125	±0.012	Yes	975	24 Pin	Yes	(Note 4)	7-5
	MN3850	4	Yes	0 to +70 −55 to +125	±0.012	Yes	345	24 Pin	Yes	(Note 4)	7-61
	DAC88	7	Yes	0 to +70 −55 to +125	±0.012	Yes	495	24 Pin	Yes	(Note 4)	7-25
	MN3860	7	Yes	0 to +70 −55 to +125	±0.012	Yes	495	24 Pin	Yes	9057001	7-65
	MN3348	8	Yes	0 to +70 −55 to +125	±0.012	Yes	195	24 Pin	Yes	(Note 4)	7-57
	MN3349	10	Yes	0 to +70 −55 to +125	±0.012	Yes	195	24 Pin	Yes	(Note 4)	7-59
	MN370 MN371	60 35	Yes	0 to +70 −55 to +125	±0.012	Yes	90	18 Pin	Yes	8981401 8981402	7-29
10-Bits	MN3040	10	Yes	0 to +70 −55 to +125	±0.05	Yes	450	18 Pin	Yes	(Note 4)	7-47
	MN3003 Series	30	Yes	0 to +70 −55 to +125	±0.05	Yes	450	16 Pin	Yes	(Note 4)	7-35
8-Bits	MN3008 MN3009	1	Yes	0 to +70 −55 to +125	±0.2	Yes	495	16 Pin	Yes	8768801 8768802	7-39
	MN3020	3	Yes	0 to +70 −55 to +125	±0.2	Yes	505	18 Pin	Yes	8971801	7-43
	MN3014	2.5	Yes	0 to +70 −55 to +125	±0.2	Yes	420	16 Pin	Yes	(Note 4)	7-41
	MN3000 Series	30	Yes	0 to +70 −55 to +125	±0.2	Yes	510	14 Pin	Yes	(Note 4)	7-31

NOTES: 1. Specified for a full scale output step settling to ±½LSB.
2. Current-output models do not have internal output op amps.
3. Monotonicity for 14 bits guaranteed over temperature.
4. Contact the factory for information regarding DESC SMD's for these device types.

✓ Indicates New Product.

D/A



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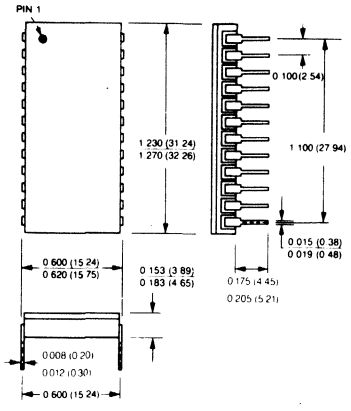
DACHK

12-Bit
D/A CONVERTER
with INPUT REGISTER

FEATURES

- Complete With Internal:
  Input Register
  Output Op Amp
  Low-Drift Reference
- ±1/2 LSB Max
  Linearity Error
- Monotonicity Guaranteed
  Over Temperature
- 50nsec Data Setup Time
- 4μsec Settling Time
- 5 Output Ranges
  2 Coding Options
- Multisourced
- Full Mil Operation
  −55°C to +125°C
- MIL-H-38534 Screening
  Optional. MIL-STD-1772
  Qualified Facility

24 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

DACHK is a complete, voltage-output, 12-bit D/A converter that contains a low-drift reference and a high-speed input register to facilitate microprocessor interfacing. The register has a minimum setup time of 50nsec; a hold time of 0nsec; and pulses as narrow as 60nsec can be used to latch new data. Output settling time for a 20V step settling to ±½LSB is 4μsec.

DACHK is packaged in a standard, hermetically-sealed, 24-pin, ceramic dual-in-line and offers 5 user-selectable output ranges (0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V) and 2 input coding options (straight binary or two's complement). Units require ±15V and +5V supplies and consume 975mW of power.

DACHK is functionally laser trimmed for linearity, gain and offset, eliminating the need for external trimming potentiometers. Units are available for three operating temperature ranges (0°C to +70°C, −25°C to +85°C and −55°C to +125°C), and each unit guarantees 12-bit monotonicity over its entire range. For military/aerospace or harsh environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

Model Number	Coding	Specified Temp. Range
DACHK	Straight Binary	0°C to +70°C
DACHKE	Straight Binary	−25°C to +85°C
DACHKH	Straight Binary	−55°C to +125°C
DACHKH/B	Straight Binary	−55°C to +125°C
DACHKH/B CH	Straight Binary	−55°C to +125°C
DACHK-2	Two's Complement	0°C to +70°C
DACHK-2E	Two's Complement	−25°C to +85°C
DACHK-2H	Two's Complement	−55°C to +125°C
DACHK-2H/B	Two's Complement	−55°C to +125°C
DACHK-2H/BCH	Two's Complement	−55°C to +125°C

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DACHK 12-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
DACHK, DACHK-2	0°C to +70°C
DACHKE, DACHK-2E	−25°C to +85°C
DACHKH, H/B; DACHK-2H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 22)	0 to +18 Volts
Negative Supply (−Vcc, Pin 14)	0 to −18 Volts
Logic Supply (+Vdd, Pin 13)	−0.5 to +7 Volts
Register Enable (Pin 16)	−0.5 to +5.5 Volts
Digital Inputs (Pins 1-12)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — DACHK-2H/BCH

Standard Part is specified for 0°C to +70°C operation.
Add "E" suffix for specified −25°C to +85°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" to "H" devices for Environmental Stress Screening.
Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

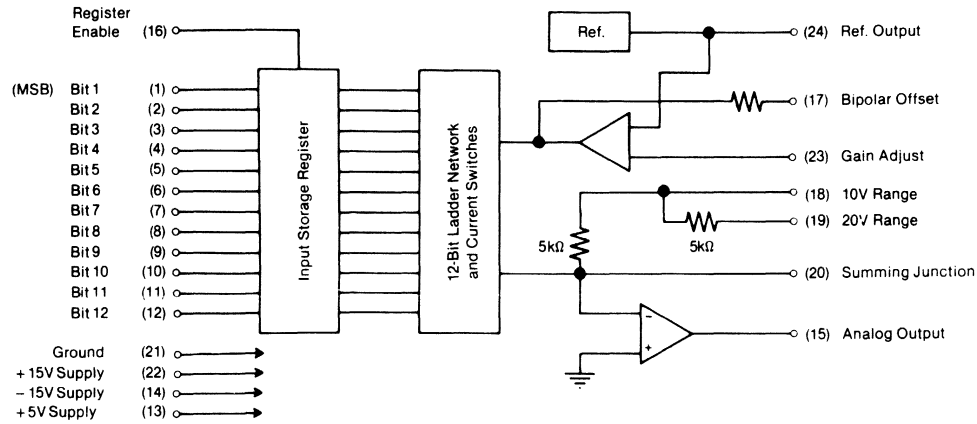
SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 1)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Input Currents: Data Inputs: Logic "1" (V_{IH} = +2.4V)		+20		µA
Logic "0" (V_{IL} = +0.4V)		−0.4		mA
Register Enable: Logic "1" ($V_{\overline{IH}}$ = +2.4V)		+60		µA
Logic "0" ($V_{\overline{IL}}$ = +0.4V)		−1.2		mA
Logic Coding (Note 2): DACHK: Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
DACHK-2: Bipolar Ranges		Two's Complement		
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar		0 to +5, 0 to +10		Volts
Bipolar		±2.5, ±5, ±10		Volts
Output Current	±5			mA
Output Impedance		0.05		Ω
TRANSFER CHARACTERISTICS (Note 3)				
Integral Linearity Error		± ¼	± ½	LSB
Differential Linearity Error		± ½		LSB
Temperature Range for Guaranteed Monotonicity:				
DACHK, DACHK-2	0		+70	°C
DACHKE, DACHK-2E	−25		+85	°C
DACHKH, H/B; DACHK-2H, H/B	−55		+125	°C
Unipolar Offset Error (Notes 4, 5)		±0.1		%FSR
Bipolar Offset Error (Notes 4, 6)		±0.1		%FSR
Gain Error (Notes 4, 7)		±0.1		%
DRIFT SPECIFICATIONS (Note 8)				
Integral Linearity Drift		±2		ppm of FSR/°C
Unipolar Offset Drift		±3	±5	ppm of FSR/°C
Bipolar Offset Drift		±7	±10	ppm of FSR/°C
Gain Drift		±15	±20	ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ± ½ LSB: 20V Step		4		µsec
10V Step		3		µsec
1 LSB		0.8		µsec
Slew Rate		±20		V/µsec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection: +15V Supply		±0.002		%FSR/%Supply
−15V Supply		±0.002		%FSR/%Supply
Current Drain: +15V Supply		+20		mA
−15V Supply		−35		mA
+5V Supply		+30		mA
Power Consumption		975		mW

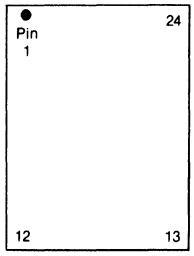
SPECIFICATION NOTES:

1. Unless otherwise indicated, listed specifications apply for all DACHK and DACHK-2 models.
2. DACHK is available with either binary input coding (DACHK, DACHKE, DACHKH and DACHKH/B) or two's complement input coding (DACHK-2, DACHK-2E, DACHK-2H and DACHK-2H/B). See Ordering Information.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ± 10V output range, FSR is 20V, and 1 LSB is ideally equal to 4.88mV. For the 0 to + 10V and ± 5V ranges, FSR is 10V, and 1 LSB is ideally equal to 2.44mV. For the 0 to +5V and ± 2.5 ranges, FSR is 5V, and 1 LSB is ideally equal to 1.22mV.
4. Initial offset and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
5. Unipolar offset error is defined as the difference between the actual and the ideal output voltage when configured in a unipolar output range with a digital input of 0000 0000 0000.
6. Bipolar offset error is defined as the difference between the actual and the ideal output voltage when configured in a bipolar output range with a digital input of 0000 0000 0000 (1000 0000 0000 for DACHK-2 models).
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage span from the 1111 1111 1111 (0111 1111 1111 for DACHK-2 models) output to the 0000 0000 0000 (1000 0000 0000 for DACHK-2 models) output.
8. Drift specifications apply over the 0°C to +70°C temperature range for DACHK and DACHK-2; over the −25°C to +85°C temperature range for DACHKE and DACHK-2E; and over the −55°C to +125°C temperature range for DACHKH, DACHKH/B and DACHK-2H, DACHK-2H/B.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Bit 1 (MSB)	24	Ref. Out (+6.2V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply (+Vcc)
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	20V Range
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Register Enable
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply (−Vcc)
12	Bit 12 (LSB)	13	+5V Supply (+Vdd)

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the DACHK. The unit's Ground (pin 21) must be tied to circuit analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used.

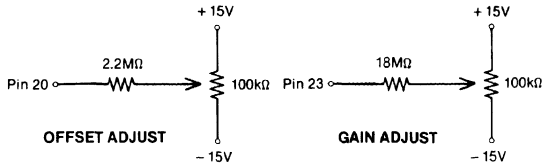
Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20) for bipolar operation. If external gain and offset adjustments are to be used, the series resistors should be located as close to the unit as possible.

REFERENCE OUTPUT—The DACHK contains an internal +6.2V reference, and the units are actively laser trimmed to operate from this reference. If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 20μA.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS — The DACHK will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be grounded.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply all "0's" to the digital inputs.* Adjust the potentiometer until the analog output is equal to zero volts for the unipolar output ranges or negative full scale for bipolar output ranges.

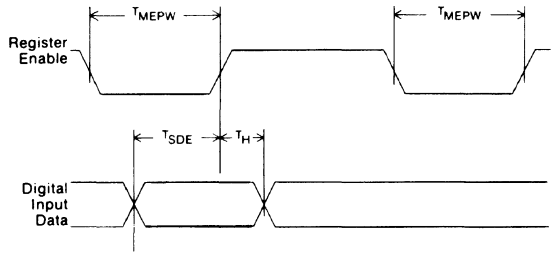
GAIN ADJUSTMENT—Connect the gain potentiometers as shown and apply all "1's" to the digital inputs.** Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the Input Logic Coding table.



* "1" and all "0's" for 2's complement ** "0" and all "1's" for 2's complement

REGISTER ENABLE — When the Register Enable (pin 16) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60nsec and digital input data must be valid for a minimum of 50nsec prior to Register Enable going high again. See Timing Diagram.

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW}	Minimum Enable Pulse Width is 60nsec.
T_{SDE}	Minimum Setup Time Digital Data to Enable is 50nsec.
T_H	Digital Data Hold Time from Register Enable is 0nsec.

INPUT LOGIC CODING

STRAIGHT BINARY		OUTPUT RANGES	
MSB	LSB	0 to +5V	0 to +10V
1111	1111 1111	+4.9988	+9.9976
1100	0000 0000	+3.7500	+7.5000
1000	0000 0000	+2.5000	+5.0000
0100	0000 0000	+1.2500	+2.5000
0000	0000 0001	+0.0012	+0.0024
0000	0000 0000	0.0000	0.0000

OFFSET BINARY		TWO'S COMPLEMENT		OUTPUT RANGES		
MSB	LSB	MSB	LSB	+2.5V	±5V	±10V
1111	1111 1111	0111	1111 1111	+2.4988	+4.9976	+9.9951
1100	0000 0000	0100	0000 0000	+1.2500	+2.5000	+5.0000
1000	0000 0000	0000	0000 0000	0.0000	0.0000	0.0000
0100	0000 0000	1100	0000 0000	−1.2500	−2.5000	−5.0000
0000	0000 0001	1000	0000 0001	−2.4988	−4.9976	−9.9951
0000	0000 0000	1000	0000 0000	−2.5000	−5.0000	−10.0000

CODING NOTES:

1. For unipolar operation, the coding is straight binary.
2. For bipolar operation, the coding is either offset binary or two's complement.
3. For FSR = 20V, 1 LSB = 4.88mV
4. For FSR = 10V, 1 LSB = 2.44mV
5. For FSR = 5V, 1 LSB = 1.22mV

OUTPUT RANGE SELECTION

Pin Connections	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect Pin 15 to	18	18	18	18	19
Connect Pin 17 to	21	21	20	20	20
Connect Pin 19 to	20	—	20	—	15

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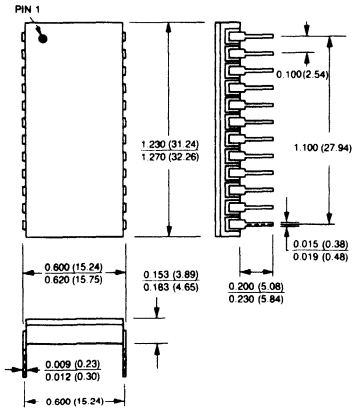
DAC71

INDUSTRY-STANDARD
16-Bit
D/A CONVERTER

FEATURES

- **16-Bit Resolution**
- **Complete With Internal Reference and Output Op Amp (V Models)**
- **Current or Voltage Output**
- **±0.003%FSR Linearity Guaranteed**
- **14-Bit Monotonicity Guaranteed Over Temperature**
- **Fast Settling:**
  10μsec (V Models)
  1μsec (I Models)
- **24-Pin Side-Brazed DIP**
- **Multisourced**

24-PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

DAC71 is a 16-bit hybrid digital-to-analog converter in a small, 24-pin, dual-in-line package. This high-resolution D/A includes an internal reference and is available in both voltage and current output models. The DAC71 offers a guaranteed maximum linearity error of ±0.003%FSR at +25°C and guarantees 14-bit monotonicity over temperature.

Utilizing the most advanced functional laser trimming techniques, DAC71 eliminates the need for external trimpots, and all parameters are specified without adjustment. Optional gain and offset adjustment points are available for applications requiring greater accuracy.

All models of DAC71 have complementary binary coded inputs. Units are available with output voltage ranges of 0 to +10V or ±10V or output current ranges of ±1mA or 0 to -2mA. Devices operate from ±15V power supplies; consume 525mW; and are direct pin-for-pin replacements for DAC71 devices from other manufacturers.

DAC71 is the ideal choice for applications requiring high resolution, small size and low cost. Typical applications include robotics, high-resolution servo and control systems, high-accuracy function generation and precision instrumentation.

Model Number	Input Code	Output Mode
DAC71-COB-V	Complementary Offset Binary	-10V to +10V
DAC71-CSB-V	Complementary Straight Binary	0 to +10V
DAC71-COB-I	Complementary Offset Binary	-1mA to +1mA
DAC71-CSB-I	Complementary Straight Binary	0 to -2mA

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DAC71 INDUSTRY-STANDARD 16-Bit D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 23)	0 to +18 Volts
Negative Supply (−Vcc, Pin 19)	0 to −18 Volts
Digital Inputs (Pins 1-16)	−0.5 to +18 Volts

ORDERING INFORMATION

PART NUMBER ——— DAC71-CSB-V

Select "COB" suffix for Complementary Offset Binary coding or "CSB" suffix for Complementary Straight Binary coding.

Select "V" suffix for voltage output or "I" suffix for current output

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, unless otherwise indicated) (Note 1)

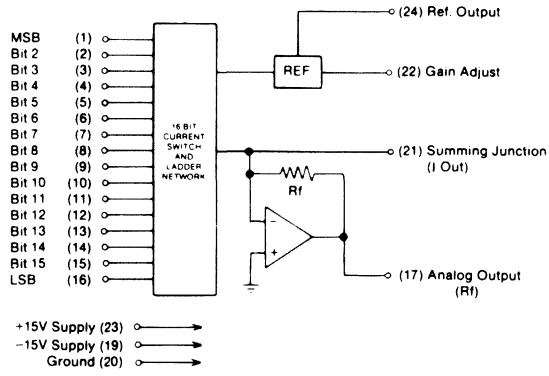
DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1" Logic "0"	+2.4		 +0.8	Volts Volts
Input Currents: Logic "1" (V_{IH} = +2.7V) Logic "0" (V_{IL} = +0.4V)		+40 −1.0		µA mA
ANALOG OUTPUTS (VOLTAGE MODELS)				
Voltage Models (Note 2): DAC71-CSB-V DAC71-COB-V		0 to +10 ±10		Volts Volts
Output Current	±5			mA
Output Impedance		0.15		Ω
Short Circuit Duration		Indefinite to Ground		
ANALOG OUTPUTS (CURRENT MODELS)				
Current Models (Note 2): DAC71-CSB-I DAC71-COB-I		0 to −2 ±1		mA mA
Compliance Voltage		±2.5		Volts
Output Impedance: Unipolar Bipolar		4 2.45		kΩ kΩ
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error			±0.003	%FSR
Temperature Range For 14-Bit Monotonicity	0		+70	°C
Unipolar Offset Error (Notes 4, 5): DAC71-CSB-V DAC71-CSB-I			±0.1 ±0.1	%FSR %FSR
Bipolar Offset Error (Notes 4, 6): DAC71-COB-V DAC71-COB-I			±0.1 ±0.1	%FSR %FSR
Gain Error (Notes 4, 7): Voltage Output Current Output		±0.05 ±0.05	±0.1 ±0.1	% %
DRIFT SPECIFICATIONS (Notes 3, 8)				
Unipolar Offset Drift: DAC71-CSB-V DAC71-CSB-I			±10 ±10	ppm of FSR/°C ppm of FSR/°C
Bipolar Offset Drift: DAC71-COB-V DAC71-COB-I			±15 ±40	ppm of FSR/°C ppm of FSR/°C
Gain Drift: Voltage Models Current Models			±20 ±45	ppm/°C ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time (Voltage Models): 20V Step to ±0.003%FSR 1 LSB Step (Note 10)		5 3	10	µsec µsec
Slew Rate (Voltage Models)		±10		V/µsec
Settling Time (Current Models) 1mA Step to ±0.003%FSR: 10Ω to 100Ω Load 1kΩ Load			1 3	µsec µsec

REFERENCE OUTPUT	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage		+6.3		Volts
Tempco		±10		ppm/°C
External Current	±1.5	±2.5		mA
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
Power Supply Rejection: +15V Supply		±0.001		%FSR/%Vs
−15V Supply		±0.001		%FSR/%Vs
Current Drain: +15V Supply		+18	+35	mA
−15V Supply		−17	−30	mA
Power Consumption		525	975	mW

SPECIFICATION NOTES:

1. Unless otherwise indicated, listed specifications apply for all DAC71 models.
2. DAC71 is available in both voltage output (DAC71-CSB-V, DAC71-COB-V) and current output (DAC71-CSB-I, DAC71-COB-I) models.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ±10V output range, FSR is 20 Volts, and 1LSB is ideally equal to 300μV. For the 0 to +10V range, FSR is 10 Volts, and 1LSB is ideally equal to 150μV.
4. Initial offset and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
5. Unipolar offset error is defined as the difference between the actual and the ideal output voltage with a digital input of 1111 1111 1111 1111.
6. Bipolar offset error is defined as the difference between the actual and the ideal output voltage with a digital input of 1111 1111 1111 1111.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage or current span from the 1111 1111 1111 1111 output to the 0000 0000 0000 0000 output.
8. Drift specifications apply over the 0°C to +70°C temperature range for all models.
9. Specified with gain and offset errors adjusted to zero at +25°C.
10. LSB step is for 14-bit resolution.

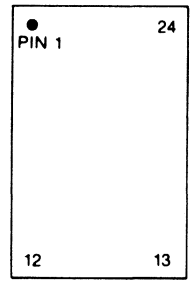
BLOCK DIAGRAM



Note:
Current Output models do not include output op amp

Rf = 5K(CSB), 10K(COB)

PIN DESIGNATIONS



1	Bit 1 (MSB)	24	Vref Out
2	Bit 2	23	+15V Supply
3	Bit 3	22	Gain Adjust
4	Bit 4	21	Summing Junction (I Out for Current Out)
5	Bit 5	20	Ground
6	Bit 6	19	−15V Supply
7	Bit 7	18	N.C.
8	Bit 8	17	Vout R_F for Current Out)
9	Bit 9	16	Bit 16 (LSB)
10	Bit 10	15	Bit 15
11	Bit 11	14	Bit 14
12	Bit 12	13	Bit 13

INPUT LOGIC CODING

Digital Input MSB LSB	Voltage Output (Volts) CSB	Voltage Output (Volts) COB	Current Output (mA) CSB	Current Output (mA) COB
0000 0000 0000 0000	+9.99985	+9.99969	−1.99997	−0.99997
0000 0000 0000 0001	+9.99970	+9.99939	−1.99994	−0.99994
0111 1111 1111 1111	+5.00000	0.00000	−1.00000	0.00000
1000 0000 0000 0000	+4.99985	−0.00031	−0.99997	+0.00003
1111 1111 1111 1110	+0.00015	+9.99969	−0.00003	+0.99997
1111 1111 1111 1111	0.00000	−10.00000	0.00000	+1.00000

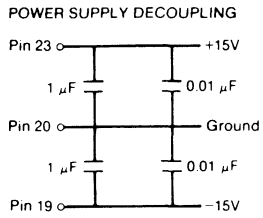
CODING NOTES

1. CSB=Complementary straight binary for unipolar output ranges.
2. COB=Complementary offset binary for bipolar output ranges.
3. For FSR=20V, 1 LSB=300μV
4. For FSR=10V, 1 LSB=150μV
5. For FSR=2mA, 1 LSB=30nA

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from DAC71. The unit's ground connection (pin 20) must be tied to circuit analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the following diagrams.



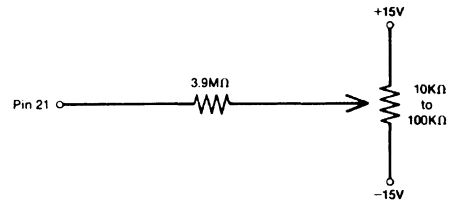
Coupling between analog and digital signals should be minimized to avoid noise pickup. If external gain and offset adjustments are to be used, the series resistors should be located as close to the unit as possible.

DAC71 has a guaranteed linearity specification of 14 bits. If the 16-bit resolution of the device is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5V through a single 1kΩ resistor.

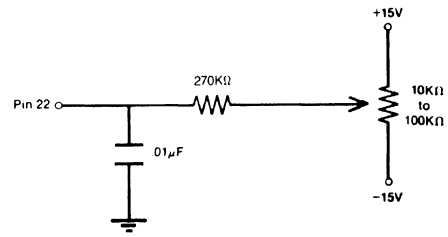
High resolution devices such as DAC71 present unique layout problems. Grounding and contact resistance become a matter of critical importance. A 16-bit converter with a 10V FSR has an LSB value of 150μV. Assuming a 5mA load, series wiring and contact resistance of only 30mΩ will throw the output off 1LSB. In terms of system layout, the impedance of #18 wire is approximately 0.064Ω/ft. Assuming 0 contact resistance, less than 6 inches of wire could produce a 1LSB error in the analog output. Careful layout and the use of external trim potentiometers for gain and offset can eliminate many potential sources of error.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS—DAC71 will operate as specified without external adjustment. If desired, however, gain and offset errors can be trimmed with potentiometers. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors should be ±20% carbon composition or better and must be located as close as possible to the package to prevent noise pickup. A 0.01μF ceramic capacitor should be connected from gain adjust (pin 22) to ground.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for unipolar output ranges or minus full scale voltage for bipolar output ranges.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the Coding table.



REFERENCE OUTPUT—All DAC71 models contain an internal +6.3V voltage reference. The reference output (pin 24) may be used to drive an external load. A buffer amplifier is recommended if external load current exceeds 1.5mA.

OUTPUT COMPLIANCE VOLTAGE—Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. DAC71 is specified for a compliance voltage swing of ± 2.5V, and an absolute maximum range of 5V is permitted without damage to the device.

MICRO NETWORKS

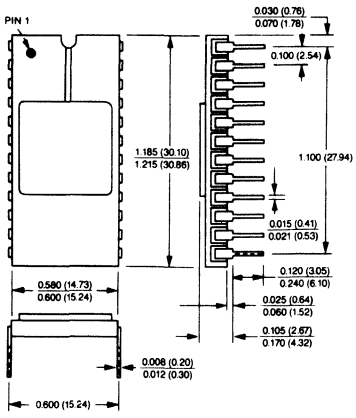
DAC80

LOW-COST
MONOLITHIC, 12-Bit
D/A CONVERTERS

FEATURES

- **Low-Cost Single-Chip Design**
- **Current or Voltage Output**
- **Complete With Internal Reference and Output Op Amp (V Models)**
- **±½LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **Fast Settling:**
  3μsec (V Models)
  300nsec (I Models)
- **±12V to ±15V Supplies**
- **345mW Power Consumption**
- **24-Pin Side-Brazed Ceramic DIP**
- **Multisourced**

24 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The Micro Networks DAC80 is a complete, single-chip, low-cost, 12-bit D/A converter. It represents the most recent monolithic implementation of the venerable hybrid DAC80 that has long been an industry standard. The popularity of this proven product is due to its low cost; its multisource availability; its guaranteed performance over temperature; its optional current or voltage output; its fast settling time; and its ability to operate from either ±12V or ±15V supplies. This latest design employs an on-chip buried-zener reference for low noise; the newest thin-film fabrication and laser-trimming techniques for tight accuracy and linearity guaranteed over temperature; a proprietary reference-buffer circuit that permits fully specified operation over a wide supply range; and an on-chip output op amp for current-to-voltage conversion and fast settling.

These D/A's are TTL voltage compatible; however, they draw low enough logic currents to be driven from CMOS logic. ±½LSB linearity and monotonicity for 12-bits are guaranteed over the full 0°C to +70°C operating temperature range. Output settling time for a 20V step to ±½LSB is 4μsec maximum. A 2mA step typically settles in 300nsec.

DAC80 is packaged in a 24-pin, side-brazed, ceramic DIP and requires supplies that can range from ±12V to ±15V. On-chip, laser trimmed, thin-film, range resistors allow users to select output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V and output current ranges of ±1mA or 0 to −2mA. The Micro Networks monolithic DAC80 is a pin-for-pin, functionally equivalent replacement for earlier hybrid versions of this device except that it no longer requires a +5V supply. Some other monolithic DAC80's are not exact replacements. The DAC80 "Z" model is no longer a necessary ordering option as all models now operate from ±12V to ±15V supplies. For −25°C to +85°C or −55°C to +125°C operation, please see the Micro Networks DAC85 or DAC87.

Model	Input Code	Output Mode	Power Supplies
DAC80-CBI-V	Complementary Binary	Voltage	±12V/±15V
DAC80-CBI-I	Complementary Binary	Current	±12V/±15V

April 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

DAC80 LOW-COST MONOLITHIC 12-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−25°C to +85°C
Specified Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
+Vcc Supply (Pin 22)	0 to +18 Volts
−Vcc Supply (Pin 14)	0 to −18 Volts
Digital Inputs (Pins 1-12)	−1 to +18 Volts
Analog Output	(Note 1)

ORDERING INFORMATION

PART NUMBER ——— **DAC80-CBI-X**

Select "V" suffix for voltage output or "I" suffix for current output.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution		12		Bits
Logic Coding (Note 2): Voltage Output		CSB,COB		
Current Output		CSB,COB		
Logic Levels: Logic "1"	+2.0		+16.5	Volts
Logic "0"	0		+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−180	μA
ANALOG OUTPUTS (VOLTAGE MODEL)				
Output Voltage Ranges		±2.5, ±5, ±10, 0 to +5, 0 to +10		Volts
Output Current	±5			mA
Output Impedance		0.05		Ω
ANALOG OUTPUTS (CURRENT MODEL)				
Output Current Ranges		±1, 0 to −2		mA
Output Impedance: Unipolar Range	4.6	6.6	8.6	kΩ
Bipolar Range	2.6	3.2	3.7	kΩ
Compliance Voltage	±2.5			Volts
TRANSFER CHARACTERISTICS (Note 3)				
Integral Linearity Error (0°C to +70°C)		±¼	±½	LSB
Differential Linearity Error (0°C to +70°C)		±½	±¾	LSB
Temperature Range For Guaranteed Monotonicity	0		+70	°C
Unipolar Offset Error (Notes 4, 5)		±0.05	±0.15	%FSR
Bipolar Offset Error (Notes 4, 6)		±0.05	±0.15	%FSR
Gain Error (Notes 4, 7)		±0.1	±0.3	%
DRIFT SPECIFICATIONS (Note 8)				
Total Bipolar Drift (Note 9)		±10	±25	ppm of FSR/°C
Total Error (0°C to +70°C) (Note 10): Unipolar		±0.08	±0.15	%FSR
Bipolar		±0.06	±0.12	%FSR
Unipolar Offset Drift		±1	±3	ppm of FSR/°C
Bipolar Offset Drift		±5	±15	ppm of FSR/°C
Gain Drift: Including Internal Reference		±15	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time (Note 11) Voltage Output:				
With 10kΩ Feedback		3	4	μsec
With 5kΩ Feedback		2	3	μsec
For 1 LSB Change		1		μsec
Settling Time (Note 11) Current Output:				
For 10Ω to 100Ω Loads		300		nsec
For 1kΩ Load		1		μsec
Slew Rate (Voltage Models)	±10	±5		V/μsec

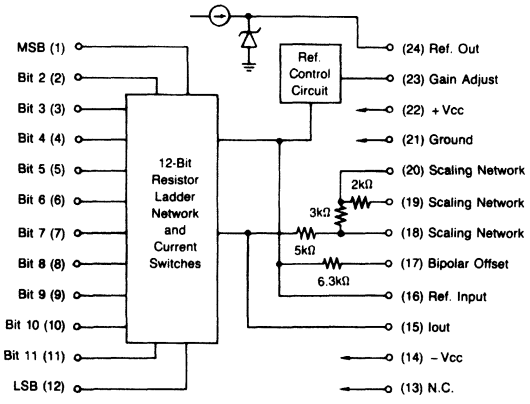
INTERNAL REFERENCE	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage		+6.3		Volts
Accuracy		±1		%
Drift		±10	±20	ppm/°C
External Current			2.5	mA
POWER SUPPLIES				
Power Supply Range: +Vcc Supply	+11.4	+15	+16.5	Volts
-Vcc Supply	-11.4	-15	-16.5	Volts
Power Supply Rejection: +Vcc Supply		±0.002		%FSR/%Supply
-Vcc Supply		±0.002		%FSR/%Supply
Current Drains: +Vcc Supply		+8	+12	mA
-Vcc Supply		-15	-20	mA
Power Consumption		345	480	mW

SPECIFICATION NOTES:

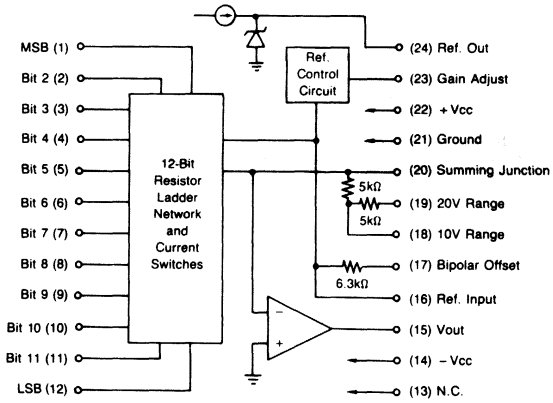
1. The DAC80's output is short-circuit protected and units can withstand a sustained short to ground or either power supply.
2. CSB = Complementary Straight Binary. COB = Complementary Offset Binary. See Digital Input Coding table for details.
3. FSR stands for full scale range and is equivalent to the nominal peak-to-peak voltage (current) of the selected output range. FSR = 5 volts for 0 to +5V and ±2.5V output ranges. FSR = 10 volts for 0 to +10V and ±5V output ranges etc.. For a 12-bit converter, 1LSB = 0.024%FSR.
4. Initial offset and gain errors are adjustable to zero with user-optional, external, trimming potentiometers.
5. Unipolar offset error is the difference between the actual and the ideal output when operating on a unipolar output range with a digital input of 1111 1111 1111.
6. Bipolar offset error is the difference between the actual and the ideal output when operating on a bipolar output range with a digital input of 1111 1111 1111.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage or current span from the 1111 1111 1111 output to the 0000 0000 0000 output.
8. To maintain published drift specifications, current output models must use internal feedback resistors.
9. Includes gain, offset and linearity drifts.
10. With initial gain and offset errors adjusted to zero at +25°C.
11. Settling time specified for an FSR step settling to ±0.01%FSR (±½LSB).

BLOCK DIAGRAMS and PIN DESIGNATIONS

(Current Models)



(Voltage Models)



1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+Vcc Supply
4	Bit 4	21	Ground
5	Bit 5	20	Scaling Network
6	Bit 6	19	Scaling Network
7	Bit 7	18	Scaling Network
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. Input
10	Bit 10	15	Output Current
11	Bit 11	14	-Vcc Supply
12	Bit 12 (LSB)	13	N.C.

1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+Vcc Supply
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	20V Range
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. Input
10	Bit 10	15	Output Voltage
11	Bit 11	14	-Vcc Supply
12	Bit 12 (LSB)	13	N.C.

APPLICATIONS INFORMATION

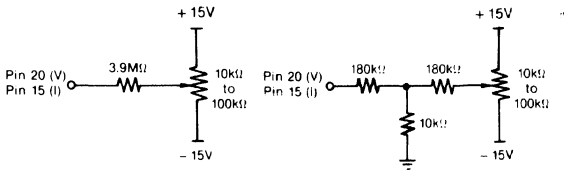
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed from the DAC80. The unit's ground (pin 21) must be tied to circuit analog ground as close to the package as possible, preferably through a large analog ground plane underneath the package. Power supplies should be decoupled with tantalum or electrolytic and ceramic capacitors located close to the unit. For optimum performance, 1μF tantalums paralleled with 0.01μF ceramic capacitors should be used. Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16) and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20, V models) or Output (pin 15, I models) for bipolar operation. If external gain and offset adjustments are to be used, the series resistors and trim pots should be located as close to the unit as possible.

REFERENCE OUTPUT—The DAC80 contains an internal +6.3V ±1% voltage reference, and the units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 2.5mA.

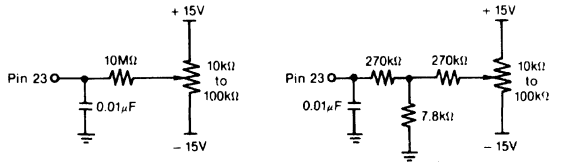
±12V OPERATION—All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA over the entire ±Vcc range.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS—The DAC80 will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced to ±½LSB by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should be connected as described elsewhere (do not ground).

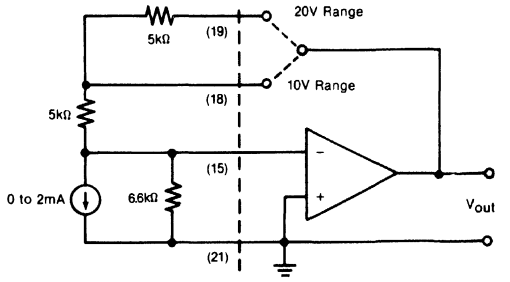
OFFSET ADJUSTMENT—Connect the offset potentiometer to pin 20 for voltage output models or pin 15 for current output models and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the appropriate value for unipolar or bipolar output ranges as listed in the Digital Input Coding table.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the appropriate value listed in the Digital Input Coding table.



DRIVING EXTERNAL OP AMPS (I Out Models)



OUTPUT RANGE SELECTION

Output Range	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	19	20	15	24
±5V	18	20	N.C.	24
±2.5V	18	20	20	24
0 to +10V	18	21	N.C.	24
0 to +5V	18	21	20	24
±1mA	17	15	N.C.	24
0 to −2mA	N.C.	21	N.C.	24

DIGITAL INPUT CODING

Digital Input	Voltage Output					Current Output	
MSB LSB	0 to +5V	0 to +10V	±2.5V	±5V	±10V	0 to −2mA	±1mA
0000 0000 0000	+4.9988	+9.9976	+2.4988	+4.9976	+9.9951	−1.9995	−0.9995
0000 0000 0001	+4.9976	+9.9951	+2.4976	+4.9951	+9.9902	−1.9990	−0.9990
0111 1111 1111	+2.5000	+5.0000	0.0000	0.0000	0.0000	−1.0000	0.0000
1000 0000 0000	+2.4988	+4.9976	−0.0012	−0.0024	−0.0049	−0.9995	+0.0005
1111 1111 1110	+0.0012	+0.0024	−2.4988	−4.9976	−9.9951	−0.0005	+0.9995
1111 1111 1111	0.0000	0.0000	−2.5000	−5.0000	−10.0000	0.0000	+1.0000

MICRO NETWORKS

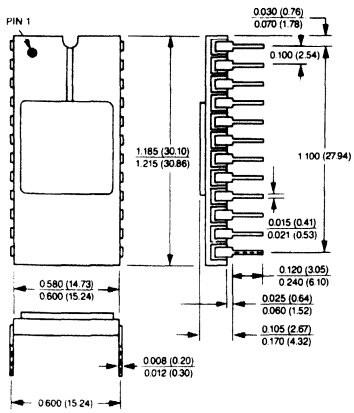
DAC85

HIGH-SPEED
INDUSTRIAL, 12-Bit
D/A CONVERTERS

FEATURES

- **Low-Cost Single-Chip Design**
- **−25°C to +85°C Operation**
- **Current or Voltage Output**
- **Complete With Internal Reference and Output Op Amp (V Models)**
- **± ½LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **Fast Settling:**
  3μsec (V Models)
  300nsec (I Models)
- **±12V to ±15V Supplies**
- **345mW Power Consumption**
- **24-Pin Side-Brazed Ceramic DIP**
- **Multisourced**

24 PIN SIDE-BRAZED DIP



Dimensions In Inches (millimeters)

DESCRIPTION

The Micro Networks DAC85 is a complete, single-chip, low-cost, 12-bit D/A converter. It represents the most recent monolithic implementation of the hybrid DAC85 — a proven device whose small package, high reliability and guaranteed performance over the −25°C to +85°C temperature range have made it a standard for demanding industrial applications. This newest version of the DAC85 now guarantees its settling time (4μsec for a 20V step settling to ± ½LSB) and has the ability to operate from either ±12V or ±15V supplies. It employs an on-chip, buried-zener reference for low noise; the newest thin-film fabrication and laser-trimming techniques for tight accuracy and linearity guaranteed over temperature; a proprietary reference buffer circuit that permits fully specified operation over a wide supply range; and an on-chip output op amp for current-to-voltage conversion and fast settling.

These D/A's are TTL voltage compatible; however, they draw low enough logic currents to be driven from CMOS logic. ± ½LSB linearity and monotonicity for 12-bits are guaranteed over the full −25°C to +85°C operating temperature range.

DAC85 is packaged in a 24-pin, side-brazed, ceramic DIP and requires supplies that can range from ±12V to ±15V. On-chip, laser trimmed, thin-film, range resistors allow users to select output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V and output current ranges of ±1mA or 0 to −2mA.

The Micro Networks monolithic DAC85 is a pin-for-pin, functionally equivalent replacement for earlier hybrid versions of this device except that it no longer requires a +5V supply. Some other monolithics are not exact replacements. The DAC85 "Z" model is no longer a necessary ordering option as all models now operate from ±12V to ±15V supplies. For −55°C to +125°C operation with or without MIL-STD-883 screening, please see Micro Networks DAC87.

Model Number	Temperature Range	Input Code	Output Mode
DAC85-CBI-I	−25°C to +85°C	Complementary Binary	Current
DAC85-CBI-V	−25°C to +85°C	Complementary Binary	Voltage

April 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

DAC85 HIGH-SPEED INDUSTRIAL 12-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
+Vcc Supply (Pin 22)	0 to +18 Volts
−Vcc Supply (Pin 14)	0 to −18 Volts
Digital Inputs (Pins 1-12)	−1 to +18 Volts
Analog Output	(Note 1)

ORDERING INFORMATION

PART NUMBER — **DAC85-CBI-X**

Select "V" suffix for voltage output or "I" suffix for current output.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±12V or ±15V unless otherwise indicated)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution		12		Bits
Logic Coding (Note 2): Voltage Output Current Output		CSB,COB CSB,COB		
Logic Levels: Logic "1" Logic "0"	+2.0 0		+16.5 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			+20 −180	μA μA
ANALOG OUTPUTS (VOLTAGE MODEL)				
Output Voltage Ranges	±2.5, ±5, ±10, 0 to +5, 0 to +10			Volts
Output Current	±5			mA
Output Impedance		0.05		Ω
ANALOG OUTPUTS (CURRENT MODEL)				
Output Current Ranges		±1, 0 to −2		mA
Output Impedance: Unipolar Range Bipolar Range	4.6 2.6	6.6 3.2	8.6 3.7	kΩ kΩ
Compliance Voltage	±2.5			Volts
TRANSFER CHARACTERISTICS (Note 3)				
Integral Linearity Error (−25°C to +85°C)		±¼	±½	LSB
Differential Linearity Error (−25°C to +85°C)		±½	±¾	LSB
Temperature Range For Guaranteed Monotonicity	−25		+85	°C
Unipolar Offset Error (Notes 4, 5) Bipolar Offset Error (Notes 4, 6) Gain Error (Notes 4, 7)		±0.05 ±0.05 ±0.1	±0.1 ±0.15 ±0.2	%FSR %FSR %
DRIFT SPECIFICATIONS (Note 8)				
Total Bipolar Drift (Note 9)		±10	±25	ppm of FSR/°C
Total Error (−25°C to +85°C) (Note 10): Unipolar Bipolar		±0.08 ±0.06	±0.2 ±0.12	%FSR %FSR
Unipolar Offset Drift Bipolar Offset Drift		±1 ±5	±3 ±10	ppm of FSR/°C ppm of FSR/°C
Gain Drift: Including Internal Reference Excluding Internal Reference		±15 ±5	±20 ±10	ppm/°C ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time (Note 11) Voltage Output: With 10kΩ Feedback With 5kΩ Feedback For 1 LSB Change		 3 2 1	 4 3	 μsec μsec μsec
Settling Time (Note 11) Current Output: For 10Ω to 100Ω Loads For 1kΩ Load		 300 1		 nsec μsec
Slew Rate (Voltage Models)	±10	±15		V/μsec

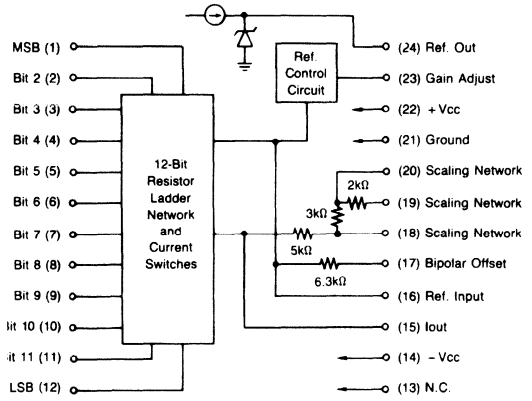
INTERNAL REFERENCE	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage		+6.3		Volts
Accuracy		±1		%
Drift		±10	±20	ppm/°C
External Current			2.5	mA
POWER SUPPLIES				
Power Supply Range: +Vcc Supply	+11.4	+15	+16.5	Volts
−Vcc Supply	−11.4	−15	−16.5	Volts
Power Supply Rejection: +Vcc Supply		±0.002		%FSR/%Supply
−Vcc Supply		±0.002		%FSR/%Supply
Current Drains: +Vcc Supply		+8	+12	mA
−Vcc Supply		−15	−20	mA
Power Consumption		345	480	mW

PECIFICATION NOTES:

1. The DAC85's output is short-circuit protected and units can withstand a sustained short to ground or either power supply.
2. CSB=complementary straight binary. COB=complementary offset binary. See Digital Input Coding table for details.
3. FSR stands for full scale range and is equivalent to the nominal peak-to-peak voltage (current) of the selected output range. FSR=5 volts for 0 to +5V and ±2.5V output ranges. FSR=10 volts for 0 to +10V and ±5V output ranges etc.. For a 12-bit converter, 1LSB=0.024%FSR.
4. Initial offset and gain errors are adjustable to zero with user-optional, external, trimming potentiometers.
5. Unipolar offset error is the difference between the actual and the ideal output when operating on a unipolar output range with a digital input of 1111 1111 1111.
6. Bipolar offset error is the difference between the actual and the ideal output when operating on a bipolar output range with a digital input of 1111 1111 1111.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full voltage or current output span from the 1111 1111 1111 output to the 0000 0000 0000 output.
8. To maintain published drift specifications, current output models must use internal feedback resistors.
9. Includes gain, offset and linearity drifts.
10. With initial gain and offset errors adjusted to zero at +25°C.
11. Settling time specified for an FSR step settling to ±0.01%FSR (±½LSB).

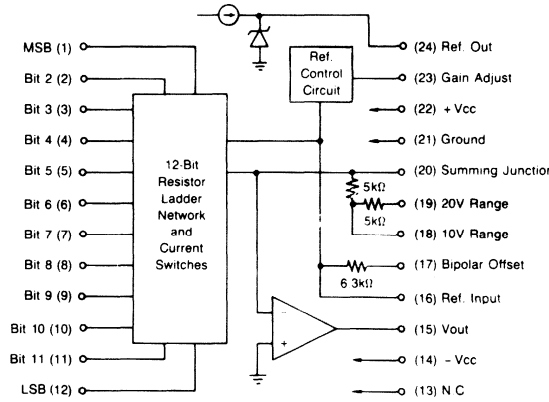
BLOCK DIAGRAMS and PIN DESIGNATIONS

(Current Models)



1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+Vcc Supply
4	Bit 4	21	Ground
5	Bit 5	20	Scaling Network
6	Bit 6	19	Scaling Network
7	Bit 7	18	Scaling Network
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. Input
10	Bit 10	15	Output Current
11	Bit 11	14	−Vcc Supply
12	Bit 12 (LSB)	13	N.C.

(Voltage Models)



1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+Vcc Supply
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	20V Range
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. Input
10	Bit 10	15	Output Voltage
11	Bit 11	14	−Vcc Supply
12	Bit 12 (LSB)	13	N.C.

PPLICATIONS INFORMATION

AYOUT CONSIDERATIONS—Proper attention to layout and coupling is necessary to obtain specified accuracy and speed om the DAC85. The unit's Ground (pin 21) must be tied to circuit alog ground as close to the package as possible, preferably through a large analog ground plane underneath the package. Power supplies should be decoupled with electrolytic and ceramic capacitors located close to the unit. For optimum performance, 1μF tantalums paralleled with 0.01μF ceramic capacitors should be used.

Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16) and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20, V models) or Output (pin 15, I models) for bipolar operation. If external gain and offset adjustments are to be used the series resistors and trim pots should be located as close to the unit as possible.

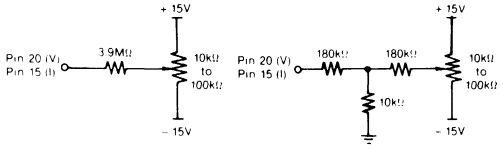
REFERENCE OUTPUT—The DAC85 contains an internal +6.3V ±1% voltage reference, and the units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 2.5mA.

OUTPUT RANGE SELECTION

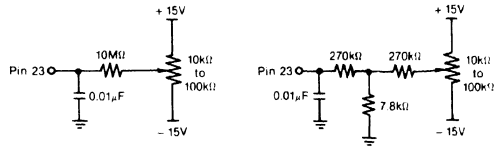
Output Range	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	19	20	15	24
±5V	18	20	N.C.	24
±2.5V	18	20	20	24
0 to +10V	18	21	N.C.	24
0 to +5V	18	21	20	24
±1mA	17	15	N.C.	24
0 to −2mA	N.C.	GND	N.C.	24

OPTIONAL GAIN AND OFFSET ADJUSTMENTS—The DAC85 will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced to ±½LSB by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should be connected as described elsewhere (do not ground).

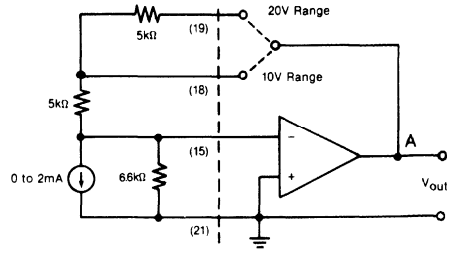
OFFSET ADJUSTMENT—Connect the offset potentiometer to pin 20 for voltage output models or pin 15 for current output models and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the appropriate value for unipolar or bipolar output ranges as listed in the Digital Input Coding table.



GAIN ADJUSTMENT—Connect the Gain potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the appropriate value listed in the Digital Input Coding table.



CURRENT OUTPUT MODELS—Current output models of the DAC85 may be used to drive the summing junction of an output op amp to produce an output voltage. Using the internal feedback resistors of the DAC85-CBI-I provides the same output voltage ranges as the voltage model. To obtain the desired output voltage range when connecting an external op amp, refer to the figure and table below.



Output Range	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	19	15	A	24
±5V	18	15	N.C.	24
±2.5V	18	15	15	24
0 to +10V	18	21	N.C.	24
0 to +5V	18	21	15	24

DAC85-CBI-I has an output current of 0 to −2mA (shunted by 6.6kΩ or ±1mA (shunted by 3.2kΩ). If desired, the current-output model can be terminated directly with a resistive load (R_L) to provide a voltage output over a range of ±2.5V. The full scale outputs will be as follows:

$$V_O = -2mA \frac{(6.6k\Omega \times R_L)}{(6.6k\Omega + R_L)} \text{ or } \pm 1mA \frac{(3.2k\Omega \times R_L)}{(3.2k\Omega + R_L)}$$

In order to obtain the best temperature tracking characteristics, it is suggested that the bulk of the load resistor be made up by paralleling the internal feedback resistors. For example, paralleling the 5k, 3k and 2k resistors gives an equivalent impedance of 968Ω. This impedance in series with an external 210Ω resistor yields a voltage range of 0 to −2V. External resistors should be good quality metal-film types with a maximum of 100 ppm/°C temperature coefficient.

DIGITAL INPUT CODING

Digital Input	Voltage Output					Current Output	
MSB LSB	0 to +5V	0 to +10V	±2.5V	±5V	±10V	0 to −2mA	±1mA
0000 0000 0000	+4.9988	+9.9976	+2.4988	+4.9976	+9.9951	−1.9995	−0.9995
0000 0000 0001	+4.9976	+9.9951	+2.4976	+4.9951	+9.9902	−1.9990	−0.9990
0111 1111 1111	+2.5000	+5.0000	0.0000	0.0000	0.0000	−1.0000	0.0000
1000 0000 0000	+2.4988	+4.9976	−0.0012	−0.0024	−0.0049	−0.9995	+0.0005
1111 1111 1110	+0.0012	+0.0024	−2.4988	−4.9976	−9.9951	−0.0005	+0.9995
1111 1111 1111	0.0000	0.0000	−2.5000	−5.0000	−10.0000	0.0000	+1.0000

MICRO NETWORKS

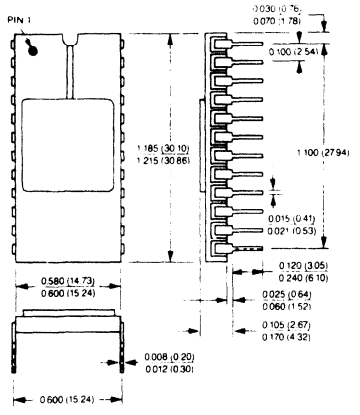
DAC87

INDUSTRY-STANDARD
MILITARY, 12-Bit
D/A CONVERTERS

FEATURES

- **Fully Guaranteed −55°C to +125°C Operation**
- **Linearity and Monotonicity Guaranteed Over Temperature**
- **4μsec Settling Time**
- **Low Drift: Gain ±20ppm/°C Max Offset ±3ppm of FSR/°C Max**
- **Small 24-Pin Hermetic DIP**
- **No +5V Supply Required**
- **480mW Maximum Power Consumption**
- **Pin-Compatible DAC85-CBI-V, AD DAC87**
- **MIL-STD-1772 Qualified Facility**

24 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The DAC87 is a high-performance, TTL-compatible, 12-bit digital-to-analog converter in a 24-pin, hermetically sealed ceramic dual-in-line package. The DAC87 is a monolithic voltage-output D/A complete with an internal reference and fast output amplifier. It is pin-for-pin compatible with industry standard DAC87 and DAC85/80 D/A converters and guarantees a 4μsec output settling time (20V step settling to ±0.5LSB). Other critical accuracy performance parameters are fully specified and guaranteed over the entire operating temperature range. Linearity and monotonicity are guaranteed over temperature, and total unadjusted error is specified as ±0.3% FSR maximum over temperature.

The Micro Networks DAC87 has 5 user-selectable output ranges, a fully short-circuit protected output, and a maximum power consumption of 480mW. The DAC87's rugged ceramic package is hermetically sealed, and for military/aerospace applications, DAC87H/B is available with Environmental Stress Screening.

DAC87 type 12-bit D/A converters have become the industry standard for military/aerospace and demanding industrial applications. The DAC87's monolithic design results in improved reliability. Guaranteed monotonicity over temperature makes the DAC87 an excellent choice for closed-loop servo systems.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

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DAC87 INDUSTRY-STANDARD MILITARY 12-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
DAC87	−25°C to +85°C
DAC87H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 22)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 14)	+0.5 to −18 Volts
Digital Inputs (Pins 1-12)	−0.5 to +18 Volts
Output Current	(Note 1)

ORDERING INFORMATION

PART NUMBER — **DAC87H/B**

Standard device is specified for −25°C to +85°C operation.

Add "H" suffix for specified −55°C to +125°C operation.

Add "/B" suffix to "H" models for Environmental Stress Screening.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated) (Note 2)

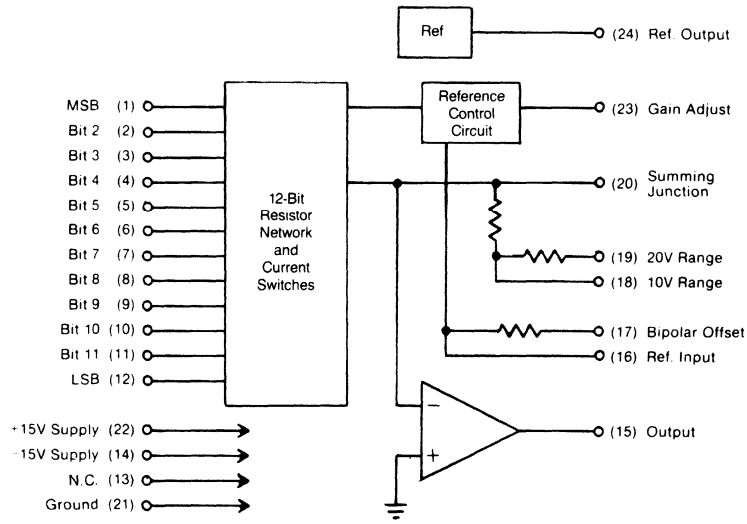
DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Input Currents: Logic "1" (V_{IH} = +2.4V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−180	μA
Logic Coding: Unipolar Output Ranges	Complementary Straight Binary			
Bipolar Output Ranges	Complementary Offset Binary			
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar	0 to +5, 0 to +10			Volts
Bipolar	±2.5, ±5, ±10			Volts
Output Impedance (Note 11)		0.05	0.20	Ω
Output Current (Notes 1, 11)	±5			mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 4)			±¾	LSB
Differential Linearity Error		±½		LSB
Monotonicity	Guaranteed Over Temperature			
Total Error, Without Adjustment (Note 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 4)		±0.15	±0.3	%FSR
Unipolar Offset Error (Notes 6, 7): Initial (+25°C)		±0.02	±0.05	%FSR
Over Temperature (Note 4)		±0.04	±0.08	%FSR
Drift (Note 10)		±1	±3	ppm of FSR/°C
Bipolar Offset Error (Notes 6, 8): Initial (+25°C)		±0.02	±0.05	%FSR
Over Temperature (Note 4)		±0.05	±0.1	%FSR
Drift (Note 10)		±5	±10	ppm of FSR/°C
Gain Error (Notes 6, 9): Initial (+25°C)		±0.05	±0.1	%
Over Temperature (Note 4)		±0.15	±0.25	%
Drift (Note 10)		±10	±20	ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ±0.01%FSR: 20V Step		3	4	μsec
10V Step		2	3	μsec
1 LSB Step (Note 11)		1		μsec
Slew Rate (Note 11)	±10	±12		V/μsec
INTERNAL REFERENCE				
Internal Reference (Note 11): Voltage		+6.3		Volts
Accuracy		±5		%
Drift		±10		ppm/°C
External Current			2.5	mA

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.25	+15	+15.75	Volts
−15V Supply	−14.25	−15	−15.75	Volts
Power Supply Rejection: +15V Supply		±0.02	±0.04	%FSR/%Supply
−15V Supply		±0.002	±0.004	%FSR/%Supply
Current Drains: +15V Supply		+8	+12	mA
−15V Supply		−15	−20	mA
Power Consumption		345	480	mW

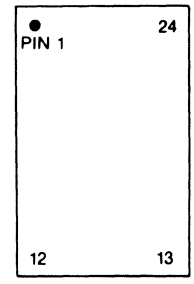
SPECIFICATION NOTES:

1. The DAC87 is short-circuit protected to ground or either supply.
2. Unless otherwise indicated, listed specifications apply for all DAC87 models.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ±10V output range, FSR is 20 Volts, and 1 LSB is ideally equal to 4.88mV. For the 0 to +10V and ±5V ranges, FSR is 10 Volts, and 1 LSB is ideally equal to 2.44mV. For the 0 to +5V and ±2.5V ranges, FSR is 5 Volts, and 1 LSB is ideally equal to 1.22mV.
4. DAC87 is specified for −25°C to +85°C operation. DAC87H and DAC87H/B are specified for −55°C to +125°C operation.
5. This specification applies to both unipolar and bipolar output ranges and is specified without adjustment. With optional gain and offset adjustment, initial accuracy error can be reduced to ±0.012%FSR(±½LSB).
6. Initial offset and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
7. Unipolar offset error is defined as the difference between the actual and the ideal output voltage when configured in a unipolar output range with a digital input of 1111 1111 1111.
8. Bipolar offset error is defined as the difference between the actual and the ideal output when configured in a bipolar output range with a digital input of 1111 1111 1111.
9. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage span from the 1111 1111 1111 output to the 0000 0000 0000 output.
10. For −25°C to +85°C operation (DAC87), the maximum drift tempcos are the following: Unipolar offset drift ±5ppm of FSR/°C
    Bipolar offset drift ±15ppm of FSR/°C
    Gain drift ±30ppm/°C
11. These parameters are listed for reference only and are not tested.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Bit 1 (MSB)	24	Reference Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply (+Vcc)
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	20V Range
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Reference Input
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply (−Vcc)
12	Bit 12 (LSB)	13	N.C.

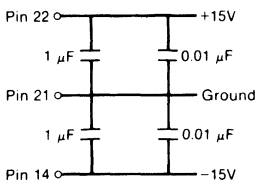
APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and bypassing is necessary to obtain specified accuracies from the DAC87. The unit's ground pin (pin 21) should be tied to system analog ground as close to the package as possible, preferably to a large analog ground plane beneath the package. Coupling between analog and digital signals should be minimized to avoid noise pickup. A short jumper should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16). Pin 20, the line to the Summing Junc-

tion of the output amplifier, is particularly noise susceptible. Care should be taken to avoid long runs or runs parallel to digital lines when tying to this pin for output range selection. If optional external offset and gain adjusting is used, the series resistors should be located as close to the package as possible, and short conductor runs should be used.

For optimum performance and noise rejection, power supplies should be bypassed with capacitors located as close to the unit as possible. We have found 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors to be a cost-effective combination. Single 1μF ceramic capacitors can be used to save space.

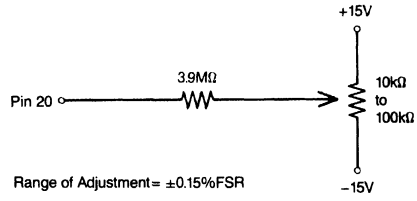
POWER SUPPLY BYPASSING



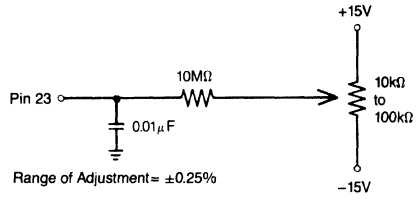
REFERENCE OUTPUT—The DAC87 contains an internal +6.3V ±5% voltage reference, and units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, the load current should not exceed 2.5mA.

OPTIONAL OFFSET AND GAIN ADJUSTMENTS—The DAC87 will operate as specified without additional adjustments. If desired, input/output accuracy error can be reduced to ±½LSB (±0.012%FSR) by following the trimming procedures described below. Adjustments should be made following warmup, and to avoid interaction, offset must be adjusted before gain. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be connected to ground.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown below and apply the digital input 1111 1111 1111. Adjust the offset potentiometer until the output is exactly zero volts for unipolar ranges and minus full scale for bipolar ranges. See Input Logic Coding.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply a 0000 0000 0000 digital input. Adjust the gain potentiometer until the output voltage is at its ideal positive full scale value (+F.S.-1 LSB, see Input Logic Coding).



OUTPUT RANGE SELECTION

Pin Connections	Output Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect Pin 24 to	16	16	16	16	16
Connect Pin 17 to	21	21	20	20	20
Connect Pin 15 to	18	18	18	18	19
Connect Pin 19 to	20	N.C.	20	N.C.	15
Connect Pin 20 to	19	N.C.	19,17	17	17

INPUT LOGIC CODING

Digital Input	Analog Output				
MSB LSB	0 to +5V	0 to +10V	±2.5V	±5V	±10V
0000 0000 0000	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
0000 0000 0001	+4.9976V	+9.9951V	+2.4976V	+4.9951V	+9.9902V
0111 1111 1111	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
1000 0000 0000	+2.4988V	+4.9976V	-0.0012V	-0.0024V	-0.0049V
1111 1111 1110	+0.0012V	+0.0024V	-2.4988V	-4.9976V	-9.9951V
1111 1111 1111	0.0000V	0.0000V	-2.5000V	-5.0000V	-10.0000V

CODING NOTES

1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR=20V, 1 LSB=4.88mV.
4. For FSR=10V, 1 LSB=2.44mV.
5. For FSR=5V, 1 LSB=1.22mV.

MICRO NETWORKS

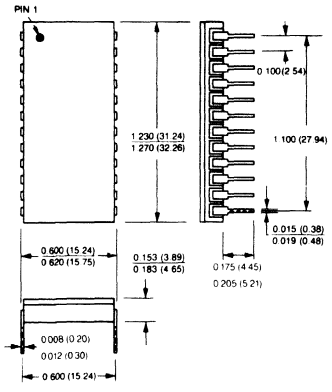
DAC88

12-Bit
D/A CONVERTER
with INPUT REGISTER

FEATURES

- **Complete With Internal:**
  Input Register
  Output Op Amp
  Low-Drift Reference
- **±½LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **40nsec Data Setup Time**
- **±0.1% FSR Unadjusted Absolute Accuracy**
- **7μsec Max Settling Time (20V step to ±½LSB)**
- **Small 24-Pin DIP**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The DAC88 is a 12-bit digital-to-analog converter with a fast, internal, TTL input register. It is packaged in a hermetically sealed, ceramic, 24-pin dual-in-line package and is complete with internal reference and output amplifier. Three user selectable output ranges are available (0 to +10V, ±5V and ±10V), and performance features include the following: fast output settling (7μsec for a 20V change), ±0.1%FSR maximum absolute accuracy, and ±½LSB linearity and monotonicity guaranteed over the full operating temperature range. Maximum power consumption is 730mW.

The DAC88 is functionally laser trimmed for linearity, gain and offset, eliminating the need for external potentiometers. Units are available for three operating temperature ranges (0°C to +70°C, −25°C to +85°C and −55°C to +125°C). Linearity and accuracy are tested 100% and guaranteed both at room and temperature extremes. For military/aerospace or harsh-environment commercial/industrial applications, "H/B" models are available with Environmental Stress Screening while "H/B CH" models are screened in accordance with MIL-H-38534.

The DAC88 is TTL compatible, and its internal input register facilitates interfacing to microprocessor and minicomputer data buses. Applications include microprocessor-based data distribution systems, programmable power supplies and servo drivers. Optional MIL-H-38534 processing and guaranteed linearity and accuracy specifications over the −55°C to +125°C temperature range make the DAC88H/B an excellent choice for military avionics and fire control systems.

Model Number	Temperature Range	Input Coding	Max. Power Consumption
DAC88	0°C to +70°C	CSB/COB	730mW
DAC88E	−25°C to +85°C	CSB/COB	730mW
DAC88H	−55°C to +125°C	CSB/COB	730mW
DAC88H/B	−55°C to +125°C	CSB/COB	730mW
DAC88H/BCH	−55°C to +125°C	CSB/COB	730mW

MICRO NETWORKS
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February 1992
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DAC88 12-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
DAC88	0°C to +70°C
DAC88E	−25°C to +85°C
DAC88H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 22)	0 to +18 Volts
Negative Supply (−Vcc, Pin 14)	0 to −18 Volts
Logic Supply (+Vdd, Pin 13)	−0.5 to +7 Volts
Register Enable (Pin 19)	−0.5 to +5.5 Volts
Digital Inputs (Pins 1-12)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — DAC88H/B CH

- Standard Part is specified for 0°C to +70°C operation.
- Add "E" suffix for specified −25°C to +85°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

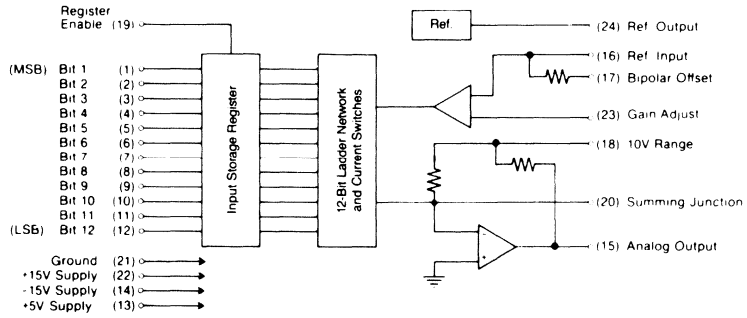
SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V +Vdd = +5V unless otherwise indicated) (Note 1)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.7	Volts
Input Currents: Data Inputs: Logic "1" (V_{IH} = +2.4V)			+30	μA
Logic "0" (V_{IL} = +0.4V)			−0.6	mA
Register Enable: Logic "1" (V_{IH} = +2.4V)			+60	μA
Logic "0" (V_{IL} = +0.4V)			−1.2	mA
Register Enable (Note 2): Pulse Width	60			nsec
Setup Time Digital Data to Enable	40			nsec
Logic Coding: Unipolar Range	Complementary Straight Binary			
Bipolar Ranges	Complementary Offset Binary			
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar		0 to +10		Volts
Bipolar		±5, ±10		Volts
Output Impedance		0.5		Ω
Output Current	±4	±5		mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 8)			±½	LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 4, 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 8)		±0.15	±0.3	%FSR
Zero Error (Notes 4, 6): Initial (+25°C)		±0.025	±0.05	%FSR
Over Temperature (Note 8)		±0.05	±0.1	%FSR
Gain Error (Notes 4, 7)		±0.1		%
Gain Drift		±10		ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ±0.01% for 20V Step		5	7	μsec
Output Slew Rate		±20		V/μsec
REFERENCE OUTPUT				
Internal Reference: Voltage		+6.3		Volts
Accuracy		±2		%
Tempco		±10		ppm/°C
External Current			2.5	mA
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
+5V Supply	+4.75	+5.00	+5.25	Volts
Power Supply Rejection: +15V Supply		±0.01	±0.04	%FSR/%Supply
−15V Supply		±0.001	±0.004	%FSR/%Supply
Current Drain: +15V Supply		+8	+12	mA
−15V Supply		−15	−20	mA
+5V Supply		+30	+50	mA
Power Consumption		495	730	mW

SPECIFICATIONS

1. Unless otherwise indicated, listed specifications apply for all DAC88 models.
2. The analog output will follow its digital input when Register Enable is a logic "0". Digital input data will be latched and analog output voltage constant when Register Enable is logic "1". The minimum Register Enable pulse width to latch new digital input data is 60nsec. See Timing Diagram.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ± 10V output range, FSR is 20 Volts, and 1LSB is ideally equal to 4.88mV. For the 0 to +10V and ± 5V ranges, FSR is 10 Volts, and 1LSB is ideally equal to 2.44mV.
4. Initial zero and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
5. Full Scale Absolute Accuracy Error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. For unipolar output ranges, Full Scale Absolute Accuracy Error refers to the deviation between the actual and the ideal output with an all "0's" digital input applied. For bipolar output ranges, the spec refers to the deviation between the actual and the ideal output with either all "0's" (positive full scale) or all "1's" (negative full scale) applied.
6. Zero error is defined as the difference between the actual and the ideal output voltage for the input code which ideally produces 0 Volts out. For the 0 to +10V range, zero error is measured with a digital input of 11111 1111 1111. For ± 5V and ± 10V ranges, zero error is measured with a digital input of 0111 1111 1111.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output span from the 1111 1111 1111 output to the 0000 0000 0000 output.
8. Listed specifications apply over the 0°C to +70°C temperature range for standard products, over the −25°C to +85°C range for "E" products, and over the −55°C to +125°C range for "H" products.

BLOCK DIAGRAM



PIN DESIGNATIONS

1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	Register Enable
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. In
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply
12	Bit 12 (LSB)	13	+5V Supply

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the DAC88. The units' Ground (pin 21) must be tied to circuit analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum performance, 1 μF capacitors paralleled with 0.01 μF ceramic capacitors should be used.

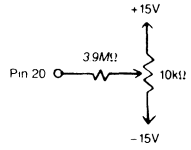
Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16) and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20) for bipolar operation. If external gain and offset adjustments are to be used, the series resistors should be located as close to the unit as possible.

REFERENCE OUTPUT—The DAC88 contains an internal +6.3V ±2% voltage reference, and the units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 2.5mA.

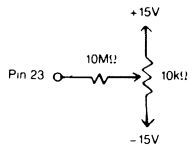
OPTIONAL GAIN AND OFFSET ADJUSTMENTS—The DAC88 will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced to ±1LSB by following the trimming procedure described below. Adjustments should be made following warmup and, to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be grounded.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for the unipolar output ranges or minus full scale for bipolar output ranges.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the Coding table.



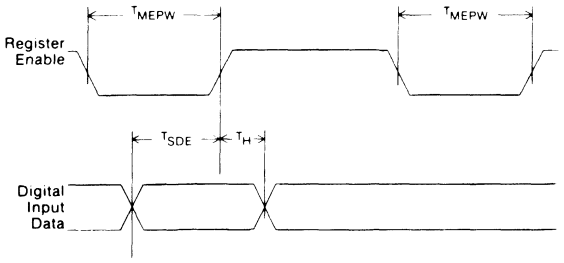
OFFSET ADJUST



GAIN ADJUST

REGISTER ENABLE—When the Register Enable (pin 19) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60nsec and digital input data must be valid for a minimum of 40nsec prior to Register Enable going high again. See Timing Diagram.

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW} Minimum Enable Pulse Width is 60nsec.
T_{SDE} Minimum Setup Time Digital Data to Enable is 40nsec.
T_H Digital Data Hold Time from Register Enable is 0nsec.

OUTPUT RANGE SELECTION

Pin Connections	Analog Output		
Output Range	**0 to +10V**	**±5V**	**±10V**
Connect Pin 24 to	16	16	16
Connect Pin 17 to	21	20	20
Connect Pin 15 to	18	18	N.C.
Connect Pin 20 to	N.C.	17	17

INPUT LOGIC CODING

Digital Input		Analog Output		
MSB	**LSB**	**0 to +10V**	**±5V**	**±10V**
0000 0000 0000		+9.9976V	+4.9976V	+9.9951V
0000 0000 0001		+9.9951V	+4.9951V	+9.9902V
0111 1111 1111		+5.0000V	0.0000V	0.0000V
1000 0000 0000		+4.9976V	−0.0024V	−0.0049V
1111 1111 1110		+0.0024V	−4.9976V	−9.9951V
1111 1111 1111		0.0000V	−5.0000V	−10.0000V

CODING NOTES:

1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR=20V, 1LSB=4.88mV.
4. For FSR=10V, 1LSB=2.44mV.

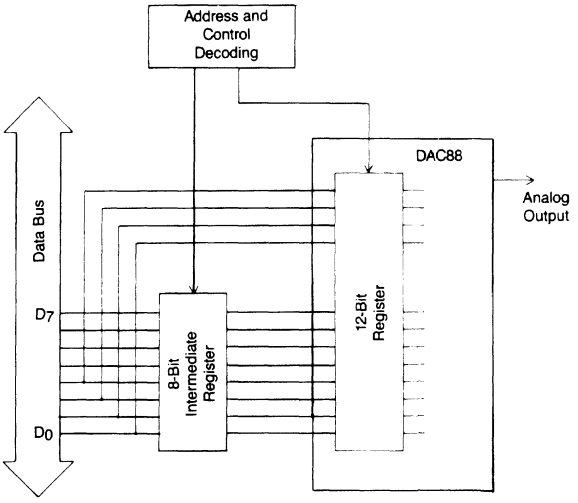
MICROPROCESSOR INTERFACING

Interfacing the DAC88 to 8, 12 and 16-bit microprocessors is simplified by the DAC88's internal 12-bit register. External address and control decoding will be required, however.

Interfacing to 12 and 10-bit processors is fairly direct and can usually be accomplished by NANDing the desired address lines with the processor's MEMORY WRITE or I/O WRITE line and using the output to drive the DAC88's Register Enable input. For most processors, valid data remains on the data bus for a period of time after the removal of either valid address or control signals. This results in data being latched into the DAC88 immediately after one of the address or control signals changes but before valid data goes away.

Interfacing to 8-bit processors is slightly more complicated and an 8-bit external register is needed as shown in the sketch below.

Address decoding must be organized such that the 8-bit intermediate register and the DAC88's internal 12-bit register appear at two different addresses. The 12 bits of digital data are sent to the DAC88 via two data transfers. First, the 8 least significant bits of digital data are written to the intermediate latch. Then, the 4 most significant bits of digital data are written to the DAC88's 12-bit latch. The result is that the 4 MSB's on the data bus and the 8 LSB's held in the intermediate latch are all latched into the DAC88's latch simultaneously. This technique is called double buffering and it avoids the analog output slewing to an undesirable state determined by the LSB's of the new digital data and the MSB's of the previous digital data.



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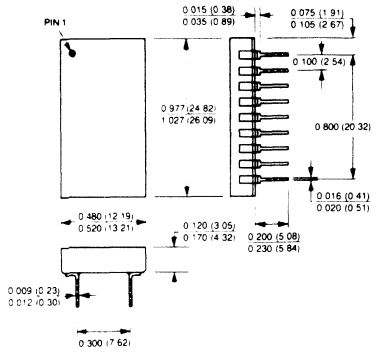
MN370
MN371

LOW-POWER, 12-Bit
D/A CONVERTERS

FEATURES

- **Complete D/A Converters:**
  Internal Reference
  Internal Output Amplifier
- **Low Power**
  135mW Maximum
  Adjustment Free
- **±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **Small 18-Pin DIP**
- **0 to +10V (MN371) and ±10V (MN370) Output Ranges**
- **Full Mil Operation**
  −55°C to +125°C
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

18 PIN DIP



Dimensions in Inches (millimeters)

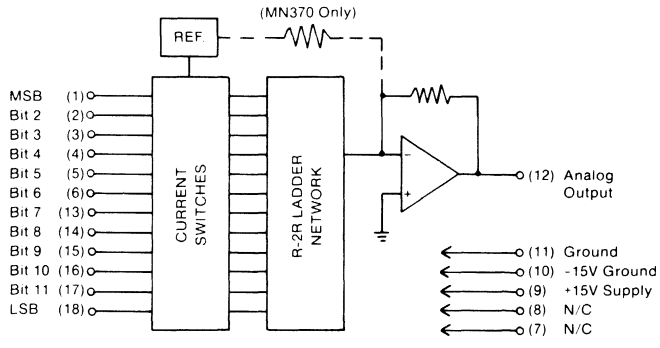
DESCRIPTION

MN370 and MN371 are precision, ultra-low-power, voltage-output, 12-bit D/A converters. Each is complete with internal voltage reference and output amplifier; consumes only 120mW of power (maximum); and is packaged in an 18-pin, hermetically sealed, ceramic dual-in-line.

MN370 has a bipolar ±10 output range; MN371 has a unipolar 0 to +10V output range. Both use functional laser trimming of thin-film nichrome resistor networks to guarantee ±0.05% FSR unadjusted absolute accuracy eliminating the need for gain and offset adjusting potentiometers and periodic recalibration.

MN370 and MN371 are excellent choices for satellite, airborne and remote-site applications that require high reliability and the precision of a 12-bit D/A converter but are unable to tolerate the size and power consumption of conventional designs. Adjustment-free operation and guaranteed accuracies assure field interchangeability without the need for recalibration. Units are fully specified for either −55°C to +125°C ("H" models) or 0°C to +70°C operation. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

BLOCK DIAGRAM



MN370/371

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MN370 MN371 LOW-POWER 12-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN370, MN371	0°C to +70°C
MN370H, H/B, MN371H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 9)	0 to +17 Volts
−15V Supply (−V_{CC}, Pin 10)	0 to −17 Volts
Digital Inputs (Pins 1-6, 13-18)	0 to +15 Volts

ORDERING INFORMATION

PART NUMBER — MN370H/B CH

- Select MN370 or MN371 model.
- Standard part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.4			Volts
Logic "0"			+0.8	Volts
Input Currents: Logic "1"			+10	μA
Logic "0"			−10	μA
ANALOG OUTPUTS				
Output Range: MN370		−10 to +10		Volts
MN371		0 to +10		Volts
Output Impedance			5	Ohms
Output Load Current	± 1			mA
TRANSFER CHARACTERISTICS				
Linearity Error (Note 1): 0°C to +70°C		± ¼	± ½	LSB
−55°C to +125°C			± ½	LSB
Monotonocity	Guaranteed Over Temperature			
Absolute Accuracy Error (Notes 2, 3):				
+25°C		±0.025	±0.05	% FSR
0°C to +70°C			±0.2	% FSR
−55°C to +125°C			±0.3	% FSR
DYNAMIC CHARACTERISTICS				
Settling Time: 10V Step to ±1/2 LSB		25	35	μsec
20V Step to ±1/2 LSB		50	60	μsec
Output Slew Rate		±0.5		V/μSec
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
Power Supply Rejection: +15V Supply		±0.01	±0.02	% FSR/% Vs
−15V Supply		±0.015	±0.03	% FSR/% Vs
Current Drain Output Unloaded: +15V Supply		+3	+4	mA
−15V Supply		−3	−5	mA
Power Consumption		90	135	mW

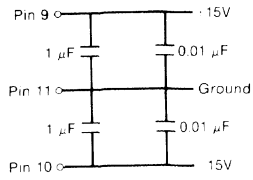
SPECIFICATION NOTES:

1. Micro Networks tests and guarantees maximum linearity error at room temperature and both extremes of the specified operating temperature range.
2. The Absolute Accuracy Error of a voltage output D/A is the difference between the actual output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. Absolute Accuracy Error includes gain, offset, linearity, and noise errors and encompasses the drifts of these errors when specified over temperature. For the MN370, we measure the Absolute Accuracy Error when the digital inputs are 1111 1111 1111 and 0000 0000 0000. For the MN370, we measure it for 1111 1111 1111, 0000 0000 0000 and 0111 1111 1111. We perform these measurements at +25°C and at both the high and low extremes of the specified operating temperature range. These measurements, coupled with our linearity tests, allow us to guarantee that, at +25°C, the analog output, for any given digital input, will be within ±0.05%FSR of its ideal value, and that over the entire operating temperature range, the analog output will be within ±0.3%FSR of its ideal value.
3. For a 12 bit converter, 1 LSB corresponds to 0.024% FSR. FSR stands for Full Scale Range and is equivalent to the peak to peak voltage of the converter's output range. For the ±10V output range, FSR is 20V and 1 LSB = 4.88mV. For the 0 to +10V output range, FSR is 10V and 1 LSB = 2.44mV.

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (DC VOLTS) MN370	MN371
0000 0000 0000	+ 9.9951	+9.9976
0000 0000 0001	+ 9.9902	+9.9951
0111 1111 1111	0.0000	+5.0000
1000 0000 0000	− 0.0049	+4.9976
1111 1111 1110	− 9.9951	+0.0024
1111 1111 1111	−10.0000	0.0000

For the MN370, the coding is Complementary Offset Binary.
For the MN371, the coding is Complementary Straight Binary.

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessry to obtain specified accuracies. The unit's ground pin (Pin 11) should be connected to system analog ground, preferably through a large ground plane beneath the package. Power supplies should be decoupled with 1 μF capacitors paralleled with 0.01 μF ceramic capacitors as shown in the diagram.



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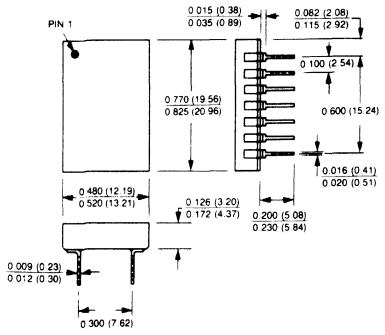
MN3000 Series

HIGH-ACCURACY
8-Bit D/A CONVERTERS

FEATURES

- **Complete D/A Converters:**
  Internal Reference
  Internal Output Op Amp
- **Small 14-Pin DIP**
- **±1/2 LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **±1/4LSB Zero Error Over Temperature**
- **±1LSB Absolute Accuracy Over Temperature**
- **Adjustment-Free**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

14 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN3000 Series are 8-bit, voltage-output, digital-to-analog converters that offer high accuracies, particularly around zero, and adjustment-free operation. Each unit contains an internal reference and output amplifier and is packaged in a 14-pin, ceramic, hermetically sealed dual-in-line package.

Units are available for either 0°C to +70°C or −55°C to +125°C ("H" models) operation. Functional laser trimming of our own ultra-stable thin-film resistor networks eliminates the need for gain and offset adjustments and allows us to guarantee the following over the entire operating temperature range: ± ½ LSB linearity error, ± ¼ LSB zero error and ±1 LSB unadjusted full scale absolute accuracy error.

Four output voltage ranges are available (MN3000, 0 to −10V; MN3001, ±5V; MN3002, 0 to +10V; MN3006, ±10V), and all devices operate from ±15V supplies consuming a maximum of 660mW. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

MN3000 Series D/A's are excellent choices for servo and other applications requiring high accuracy and repeatability around zero. In many cases, their excellent accuracies allow them to be used as cost-saving replacements for higher-resolution converters. Their completeness, small size, low weight, guaranteed accuracy and thin-film reliability make them excellent choices for military and aerospace applications.

May 1988

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MN3000 SERIES HIGH-ACCURACY 8-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0°C to +70°C
	-55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
+15V Supply (Pin 9)	+18 Volts
-15V Supply (Pin 7)	-18 Volts
Digital Inputs (Pins 1-4, 11-14)	-0.5 to +15 Volts

ORDERING INFORMATION

PART NUMBER — MN300XH/B CH

- Select model (MN3000, MN3001, etc.)
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified -55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

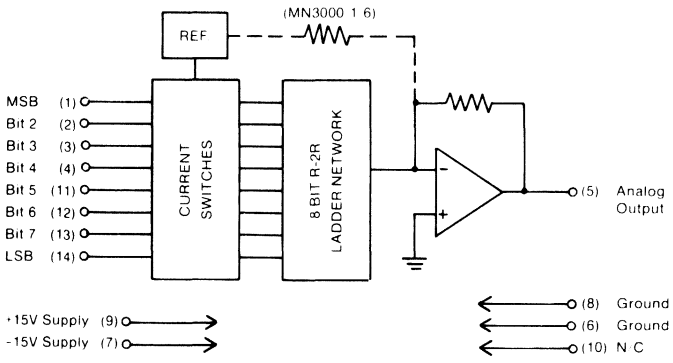
SPECIFICATIONS (T_A = 25°C, Supply Voltages +15V, unless otherwise specified).

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.8	Volts
Input Currents: Logic "1"			40	μA
Logic "0"			- 1	mA
ANALOG OUTPUTS				
Output Voltage Range: MN3000		0 to -10		Volts
MN3001		-5 to +5		Volts
MN3002		0 to +10		Volts
MN3006		-10 to +10		Volts
Output Impedance		0.5		Ohms
Output Current	± 4			mA
TRANSFER CHARACTERISTICS				
Linearity Error (Note 1): 0°C to +70°C		± ¼	± ½	LSB
-55°C to +125°C			± ½	LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 2, 3): +25°C		± ¼	± ½	LSB
-55°C to +125°C (Note 4)			± 1	LSB
Zero Error (Notes 2, 3): +25°C		± ⅛	± ¼	LSB
-55°C to +125°C (Note 4)			± ¼	LSB
Unipolar Offset Error (Notes 2, 3)				
MN3000: +25°C		± ¼	± ½	LSB
-55°C to +125°C (Note 4)			± 1	LSB
MN3002: +25°C		± ⅛	± ¼	LSB
-55°C to +125°C (Note 4)			± ½	LSB
Bipolar Offset Error (Notes 2, 3) MN3001, MN3006: +25°C		± ¼	± ½	LSB
-55°C to +125°C (Note 4)			± 1	LSB
Offset Drift: MN3002		± 2		ppmofFSR/°C
MN3000, MN3001, MN3006		±10		ppmofFSR/°C
Gain Error (Note 2)		± 0.1		%
Gain Drift		±20		ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time: 10V Step to ±1/2 LSB		23	30	μSec
20V Step to ±1/2 LSB		46	60	μSec
Output Slew Rate		0.5		Volts/μSec
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
-15V Supply	-14.55	-15.00	-15.45	Volts
Power Supply Rejection (Note 5): +15V Supply		± 0.01		% FSR / % Vs
-15V Supply		± 0.015		% FSR / % Vs
Current Drain:, Output Unloaded (Note 6): +15V Supply		17	22	mA
-15V Supply		-17	-22	mA
Power Consumption		510	660	mW

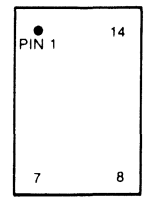
SPECIFICATION NOTES:

1. Micro Networks tests and guarantees maximum Linearity Error at room temperature and at both extremes of the specified operating temperature range.
2. See the Absolute Accuracy Error section on Page 3 for an explanation of how Micro Networks Corporation tests and specifies Full Scale Absolute Accuracy, Zero, Offset, and Gain Errors.
3. One LSB for an 8 bit converter corresponds to 0.39% FSR. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the converter's output range. For the MN3006, FSR is equal to 20V and 1 LSB is equal to 78mV. For the MN3000, MN3001, and MN3002, FSR is equal to 10V and 1 LSB is equal to 39mV.
4. For Commercial Models, this specification applies over the 0°C to +70°C temperature range. See Ordering Information.
5. The MN3000 Series will operate over a power supply range of ±14V to ±18V with reduced accuracy.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Bit 1 (MSB)	14 Bit 8 (LSB)
2 Bit 2	13 Bit 7
3 Bit 3	12 Bit 6
4 Bit 4	11 Bit 5
5 Analog Output	10 N/C
6 Ground	9 +15V Supply
7 -15V Supply	8 Ground

ABSOLUTE ACCURACY ERROR

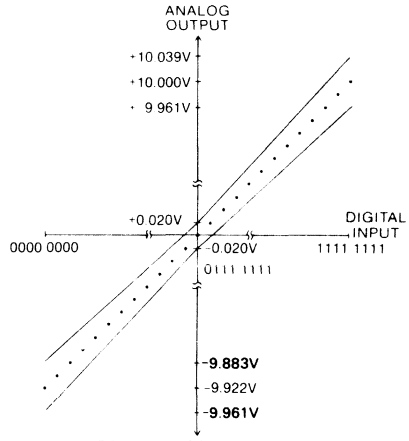
The Absolute Accuracy Error of a voltage output D/A converter is the difference between the actual, unadjusted, output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. This difference is usually expressed in LSB's or %FSR (see Note 3 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors and encompasses the drifts of these errors when specified over temperature.

For the MN3000 Series converters with unipolar output ranges (MN3000, MN3002), Micro Networks tests Absolute Accuracy Error at the zero and full scale outputs. For the units with bipolar output ranges (MN3001, MN3006), we test both the positive and negative full scale outputs as well as the zero volt output. We perform these tests at +25°C and at the high and low extremes of the specified operating temperature range. The errors appear in the specification table as the Full Scale Absolute Accuracy and Zero Errors.

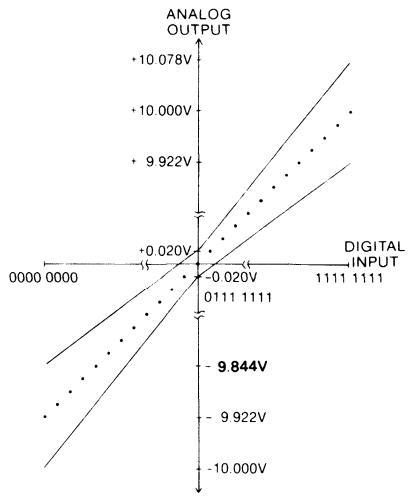
EXAMPLE: For the MN3006H (±10V output range, -55°C to +125°C), the expected output for a 0000 0000 digital input is -9.922V, the expected output for a 0111 1111 digital input is 0V, and the expected output for a 1111 1111 digital input is +10.000V. Micro Networks measures all three actual, unadjusted, output voltages at +25°C, -55°C, and +125°C. We guarantee that when the digital input is all "1's" or all "0's", the output will be at its ideal positive or negative full scale value ±39mV (±1/2 LSB) at +25°C and ±78mV (±1 LSB) at -55°C and +125°C. We guarantee that when the digital input is 0111 1111, the output will be zero volts ±20mV (±1/4 LSB) over the entire -55°C to +125°C temperature range. These limits are summarized in the two sketches below where the MN3006 digital input/analog output transfer function is shown as a dotted line, and the Absolute Accuracy limits are indicated with closed lines.

Unipolar and Bipolar Offset Error are both Absolute Accuracy Errors. Their definitions differ with respect to where along the converter's digital-input/analog-output transfer function the errors are to be measured, i.e., different analog output errors are measured at different digital input codes.

OFFSET ERROR — For the MN3000 Series, Offset Error is the Absolute Accuracy Error measured when the digital input is 0000 0000. For the MN3002, Offset Error tells how accurate the converter will be when its output is supposed to be zero volts. For this converter, Offset Error is the same



ABSOLUTE ACCURACY +25°C



ABSOLUTE ACCURACY -55°C, +125°C

as Zero Error discussed above. For the MN3000, MN3001, and MN3006, Offset Error tells how accurate the converters will be when their outputs are supposed to be at their minus full scale values. For these converters, Offset Error is equivalent to Full Scale Absolute Accuracy Error.

It is redundant to specify Bipolar and Unipolar Offset Errors after giving Full Scale Absolute Accuracy and Zero Errors as described above. We have provided the offset specifications to simplify comparing the MN3000 Series to other 8 bit D/A's. Be sure you clearly understand each manufacturer's specification definitions before you compare converters solely on a data sheet basis.

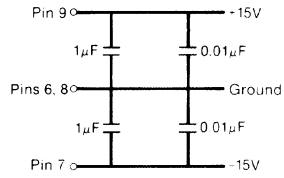
GAIN ERROR — Gain Error is the difference between the ideal and the measured values of a converter's full scale range (minus 1 LSB). See Note 3 above. It is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 1111 1111 digital input minus that measured for the 0000 0000 digital input, and it is usually expressed as a percentage.

See the Converter Tutorial Section of the Micro Networks' Product Catalogue for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN3000 Series. The units' two Ground pins (Pins 6 and 8) should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 6 and 8, as close to the package as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located as close to the MN3000 as possible. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagram below.



DIGITAL INPUT CODING

DIGITAL INPUT	ANALOG OUTPUT (DC VOLTS)			
MSB LSB	MN3000	MN3001	MN3002	MN3006
1111 1111	0.000	+5.000	+9.961	+10.000
1111 1110	-0.039	+4.961	+9.922	+9.922
1000 0000	-4.961	+0.039	+5.000	+0.078
0111 1111	-5.000	0.000	+4.961	0.000
0000 0001	-9.922	-4.922	+0.039	-9.844
0000 0000	-9.961	-4.961	0.000	-9.922

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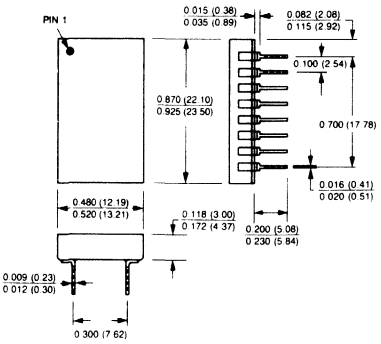
MN3003 Series

HIGH-ACCURACY
10-Bit D/A CONVERTERS

FEATURES

- **Complete D/A Converters:**
  Internal Reference
  Internal Output Amplifier
- **Small 16-Pin DIP**
- **±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **Adjustment-Free**
- **Full Scale Absolute Accuracy Error ±1LSB**
- **±1LSB Zero Error Over Temperature**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

16 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN3003 Series are 10-bit, voltage-output, digital-to-analog converters. Each unit is complete with internal reference and output amplifier and is packaged in a 16-pin, ceramic, hermetically sealed dual-in-line package.

Units are available for either 0°C to +70°C or −55°C to +125°C ("H" models) operation, and all devices are adjustment-free. Functional laser trimming of our own thin-film, nichrome resistor networks eliminates the need for external gain and offset adjustments and user calibration. The excellent stability and tracking of these resistors allows us to guarantee ± ½LSB linearity and 10-bit monotonicity over the entire operating temperature range. Zero error is guaranteed to be less than ±1 LSB over the entire operating temperature range.

Four output voltage ranges are available (MN3003, 0 to −10V; MN3004, ±5V; MN3005, 0 to +10V; MN3007, ±10V), and all devices operate from ±15V supplies consuming a maximum of 585mW. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 Micro Networks MIL-STD-1772 qualified facility.

MN3003 Series D/A converters are widely used in such applications as medical electronics, industrial control systems and automatic test equipment. They are excellent choices for servo and control applications that require tight zero error. Their small size, low weight, inherent reliability and adjustment-free operation make them excellent choices for a wide variety of military and aerospace applications.

May 1988

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MN3003 SERIES HIGH-ACCURACY 10-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0°C to +70°C
	-55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
+15V Supply (Pin 10)	+18 Volts
-15V Supply (Pin 8)	-18 Volts
Digital Inputs (Pins 1-5, 12-16)	-0.5 to +15 Volts

ORDERING INFORMATION

PART NUMBER — **MN300XH/B CH**

- Select model part number (MN3003, MN3004, etc.)
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified -55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

Contact factory for availability of CH device types.

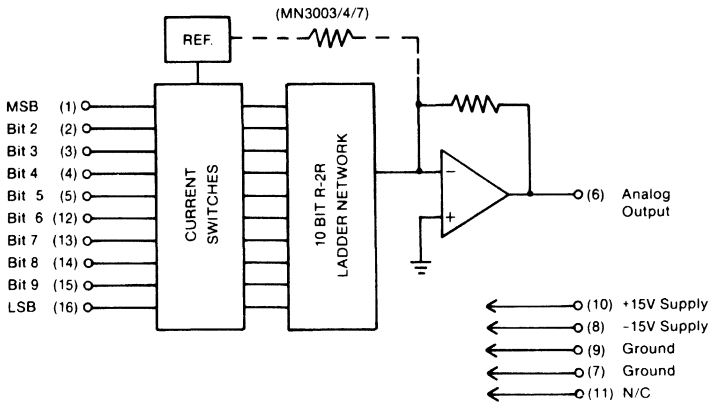
SPECIFICATIONS (T_A = 25°C, Supply Voltages ±15V, unless otherwise specified).

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.8	Volts
Input Currents: Logic "1"			40	µA
Logic "0"			- 1	mA
ANALOG OUTPUTS				
Output Voltage Range: MN3003		0 to -10		Volts
MN3004		-5 to +5		Volts
MN3005		0 to +10		Volts
MN3007		-10 to +10		Volts
Output Impedance		0.5		Ohms
Output Current	± 4			mA
TRANSFER CHARACTERISTICS				
Linearity Error (Note 1): 0°C to +70°C		± ¼	± ½	LSB
-55°C to +125°C			± ½	LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 2, 3):				
+25°C		± 0.025	± 0.1	% FSR
-55°C to +125°C (Note 4)		± 0.2	± 0.4	% FSR
Zero Error (Notes 2, 3): +25°C		± 0.025	± 0.1	% FSR
-55°C to +125°C (Note 4)		± 0.05	± 0.1	% FSR
Unipolar Offset Error (Notes 2, 3)				
MN3003: +25°C		± 0.025	± 0.1	% FSR
-55°C to +125°C (Note 4)		± 0.2	± 0.4	% FSR
MN3005: +25°C		± 0.025	± 0.1	% FSR
-55°C to +125°C (Note 4)		± 0.05	± 0.1	% FSR
Bipolar Offset Error (Notes 2, 3) MN3004, MN3007				
+25°C		± 0.025	± 0.1	% FSR
-55°C to +125°C (Note 4)		± 0.2	± 0.4	% FSR
Offset Drift: MN3005		± 2		ppm of FSR/°C
MN3003, MN3004, MN3007		±10		ppm of FSR/°C
Gain Error (Note 2)		± 0.1		%
Gain Drift		±20		ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time: 10V Step to ±1/2 LSB		23	30	µSec
20V Step to ±1/2 LSB		46	60	µSec
Output Slew Rate		0.5		Volts/µSec
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
-15V Supply	-14.55	-15.00	-15.45	Volts
Power Supply Rejection (Note 5): +15V Supply		± 0.005	± 0.015	% FSR / % Vs
-15V Supply		± 0.01	± 0.03	% FSR / % Vs
Current Drain, Output Unloaded: +15V Supply		13	17	mA
-15V Supply		-17	-22	mA
Power Consumption		450	585	mW

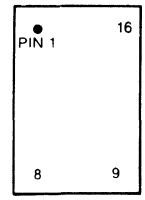
SPECIFICATION NOTES:

1. Micro Networks tests and guarantees maximum Linearity Error at room temperature and at both extremes of the specified operating temperature range.
2. See the Absolute Accuracy Error section on Page 3 for an explanation of how Micro Networks Corporation tests and specifies Full Scale Absolute Accuracy, Zero, Offset, and Gain Errors.
3. One LSB for a 10 bit converter corresponds to 0.1% FSR. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the converter's output range. For the MN3007, FSR is equal to 20V and 1 LSB is equal to 20mV. For the MN3003, MN3004, and MN3005, FSR is equal to 10V and 1 LSB is equal to 10mV.
4. For Commercial Models, this specification applies over the 0°C to +70°C temperature range. See Ordering Information.
5. The MN3003 Series will operate over a power supply range of ±14V to ±18V with reduced accuracy.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Bit 1 (MSB)	16 Bit 10 (LSB)
2 Bit 2	15 Bit 9
3 Bit 3	14 Bit 8
4 Bit 4	13 Bit 7
5 Bit 5	12 Bit 6
6 Analog Output	11 N/C
7 Ground	10 +15V Supply
8 -15V Supply	9 Ground

ABSOLUTE ACCURACY ERROR

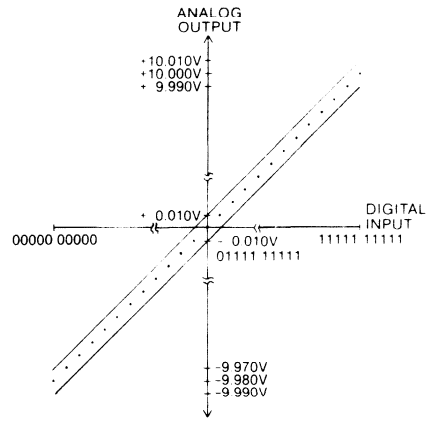
The Absolute Accuracy Error of a voltage output D/A converter is the difference between the actual, unadjusted, output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. This difference is usually expressed in LSB's or %FSR (see Note 3 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors and encompasses the drifts of these errors when specified over temperature.

For the MN3003 Series converters with unipolar output ranges (MN3003, MN3005), Micro Networks tests Absolute Accuracy Error at the zero and full scale outputs. For the units with bipolar output ranges (MN3004, MN3007)), we test both the positive and negative full scale outputs as well as the zero volt output. We perform these tests at +25°C and at the high and low extremes of the specified operating temperature range. The errors appear in the specification table as the Full Scale Absolute Accuracy and Zero Errors.

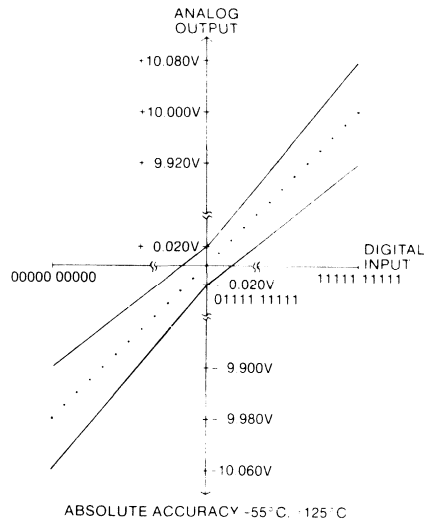
EXAMPLE: For the MN3007H (±10V output range, -55°C to +125°C), the expected output for a 00000 00000 digital input is -9.980V, the expected output for a 01111 11111 digital input is zero volts, and the expected output for a 11111 11111 digital input is +10.000V. Micro Networks measures all three actual, unadjusted, output voltages at +25°C, -55°C, and +125°C. We guarantee that when the digital input is all "1's" or all "0"s, the output will be at its ideal positive or negative full scale value ±20mV (±0.1%FSR) at +25°C and ±80mV (±0.4%FSR) at −55°C and +125°C. We guarantee that when the digital input is 01111 11111, the output will be zero volts ±20mV (±0.1%FSR) at +25°C and zero volts ±20mV (±0.1%FSR) at −55°C and +125°C. These limits are summarized in the two sketches below where the MN 3007 digital input/analog output transfer function is shown as a dotted line, and the Absolute Accuracy limits are indicated with closed lines.

Unipolar and Bipolar Offset Error are both Absolute Accuracy Errors. Their definitions differ with respect to where along the converter's digital-input/analog-output transfer function the errors are to be measured, i.e., different analog output errors are measured at different digital input codes.

OFFSET ERROR — For the MN3003 Series, Offset Error is the Absolute Accuracy Error measured when the digital input is 00000 00000. For the MN3005, Offset Error tells how



ABSOLUTE ACCURACY +25°C



ABSOLUTE ACCURACY -55°C, +125°C

MN3003 Series

accurate the converter will be when its output is supposed to be zero volts. For this converter, Offset Error is the same as Zero Error discussed above. For the MN3003, MN3004, and MN3007, Offset Error tells how accurate the converters will be when their outputs are supposed to be at their minus full scale values. For these converters, Offset Error is equivalent to Full Scale Absolute Accuracy Error.

It is redundant to specify Bipolar and Unipolar Offset Errors after giving Full Scale Absolute Accuracy and Zero Errors as described above. We have provided the offset specifications to simplify comparing the MN3003 Series to other 10 bit D/A's. Be sure you clearly understand each manufacturer's specification definitions before you compare converters solely on a data sheet basis.

GAIN ERROR — Gain Error is the difference between the ideal and the measured values of a converter's full scale range (minus 1 LSB). See Note 3 above. It is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 11111 11111 digital input minus that measured for the 00000 00000 digital input, and it is usually expressed as a percentage.

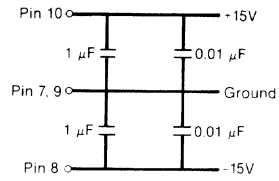
See the Converter Tutorial Section of the Micro Networks' Product Catalogue for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN3003 Series. The units' two Ground pins (Pins 7 and 9) should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package.

If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 7 and 9 as close to the package as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located as close to the MN3003 as possible. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagram below.



DIGITAL INPUT CODING

DIGITAL INPUT		ANALOG OUTPUT (DC VOLTS)			
MSB	LSB	MN3003	MN3004	MN3005	MN3007
11111	11111	0.000	+5.000	+9.990	+10.000
11111	11110	-0.010	+4.990	+9.980	+9.980
10000	00000	-4.990	+0.010	+5.000	+0.020
01111	11111	-5.000	0.000	+4.990	0.000
00000	00001	-9.980	-4.980	+0.010	-9.960
00000	00000	-9.990	-4.990	0.000	-9.980

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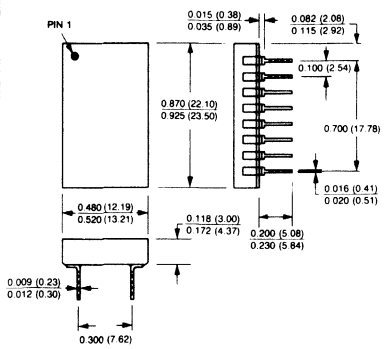
MN3008
MN3009

HIGH-SPEED, 8-Bit
D/A CONVERTERS

FEATURES

- 1μsec Maximum Settling Time (Full Scale Step to ±1/2LSB)
- Complete D/A Converters:
  Internal Reference
  Internal Output Amplifier
- ±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature
- Small 16-Pin DIP
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

16 PIN DIP



Dimensions in Inches
(millimeters)

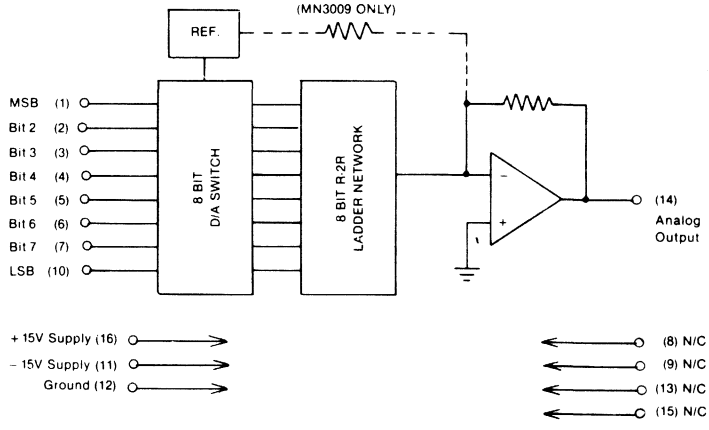
DESCRIPTION

MN3008 and MN3009 are very fast, complete, voltage-output, 8-bit digital-to-analog converters in dual-in-line packages. Both devices include an internal voltage reference and output amplifier, and both are packaged in hermetically sealed, 16-pin, ceramic DIP's.
Output settling time to ± ½ LSB is guaranteed to be less than 1μsec for a full scale (4V) change.

Models are available for either 0°C to +70°C or −55°C to +125°C ("H" models) operation. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 Qualified Facility.

Offering the inherent stability of thin-film hybrid construction and guaranteed performance over temperature, MN3008 and MN3009 are ideal choices for applications where space, weight and size are at a premium. Typical applications include avionics and fire control systems, high-speed function generators and graphic displays.

BLOCK DIAGRAM



MN3008/09

May 1988

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MN3008 AND MN3009 HIGH-SPEED 8-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C −55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
+15V Supply (Pin 16)	+18 Volts
−15V Supply (Pin 11)	−18 Volts
Digital Inputs (Pins 1-7, 10)	−0.5 to +15 Volts

ORDERING INFORMATION

PART NUMBER — MN3008H/B CH

- Select MN3008 or MN3009.
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = 25°C, Supply Voltages ±15V, unless otherwise specified).

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1" Logic "0"	2.0		 0.8	Volts Volts
Input Currents: Logic "1" Logic "0"			40 −1.0	μA mA
ANALOG OUTPUTS				
Output Voltage Range: MN3008 MN3009		0 to +4 −2 to +2		Volts Volts
Output Impedance Output Load Current	 ±3	0.5		Ohms mA
TRANSFER CHARACTERISTICS				
Linearity Error (Note 1): 0°C to +70°C −55°C to +125°C "H" Models		±¼	±½ ±½	LSB LSB
Absolute Accuracy Error (Notes 2,3): +25°C 0°C to +70°C −55°C to +125°C "H" Models		±0.1 ±0.2 ±0.5	±0.4 ±0.4 ±1.0	% FSR % FSR % FSR
DYNAMIC CHARACTERISTICS				
Settling Time (Full Scale Change to ±½ LSB) Output Slew Rate		0.5 30	1.0	μSec V/μSec
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply −15V Supply	+14.55 −14.55	+15.00 −15.00	+15.45 −15.45	Volts Volts
Power Supply Rejection: +15V Supply −15V Supply		±0.01 ±0.02	±0.02 ±0.04	% FSR/% Vs % FSR/% Vs
Current Drain, Output Unloaded: +15V Supply −15V Supply		15 −18	25 −25	mA mA
Power Consumption		495	750	mW

SPECIFICATION NOTES:

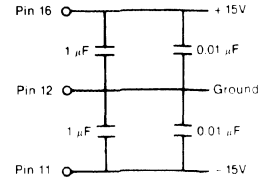
1. Micro Networks tests and guarantees maximum linearity error at room temperature and at both extremes of the specified operating temperature range.
2. The Absolute Accuracy Error of a voltage output D/A is the difference between the actual output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. Absolute Accuracy Error includes gain, offset, linearity, and noise errors and encompasses the drifts of these errors when specified over temperature. For the MN3008 and MN3009, the Absolute Accuracy Error specification applies over the converters' entire output range. We test Absolute Accuracy Error at both endpoints of the MN3008's output range and at both endpoints and the midpoint of the MN3009's output range. This testing, coupled with our linearity testing, allows us to guarantee that, from 0°C to +70°C, any analog output will be within ±0.4%FSR (±1 LSB) of its ideal level and that, from −55°C to +125°C, any analog output will be within ±1.0%FSR of its ideal level. See Note 3.
3. For an 8 bit converter, 1 LSB corresponds to 0.39%FSR. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the converters output range. For the MN3008 and MN3009, FSR equals 4V, and 1 LSB = 15.6mV.

DIGITAL INPUT CODING

DIGITAL INPUT	ANALOG OUTPUT (DC VOLTS)	
MSB LSB	MN3008	MN3009
1111 1111	+3.984	−1.984
1111 1110	+3.969	−1.969
1000 0000	+2.000	0.000
0111 1111	+1.984	+0.016
0000 0001	+0.016	+1.984
0000 0000	0.000	+2.000

LAYOUT CONSIDERATIONS

Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN3008 and MN3009. The units' Ground (Pin 12) should be tied to system analog ground as close to the package as possible, preferably through a large ground plane beneath the package. Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum noise rejection, 1 μF capacitors parallel with 0.01 μF ceramic capacitors should be used as shown in the adjacent diagram.



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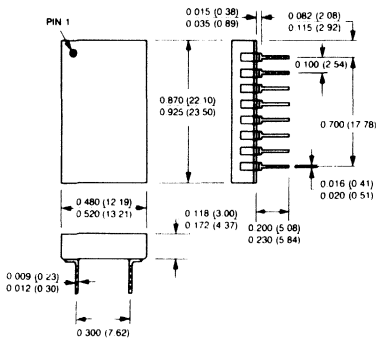
MN3014

HIGH-SPEED
8-Bit
D/A CONVERTER

FEATURES

- **Complete D/A Converter:**
  Internal Reference
  Internal Output Op Amp
- **Small 16-Pin DIP**
- **2.5 μsec Max Settling Time (20V Step to ±1/2LSB)**
- **±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **±1/2LSB Absolute Accuracy**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

16 PIN DIP



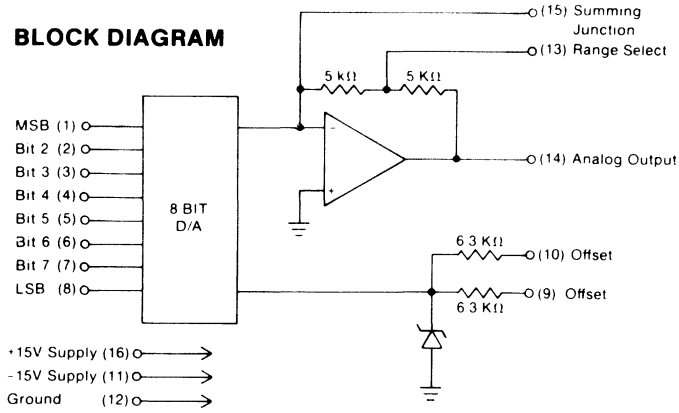
Dimensions in Inches (millimeters)

DESCRIPTION

MN3014 is a complete, high-speed (2.5μsec), adjustment-free, 8-bit digital-to-analog converter. It contains an internal reference and output amplifier and is housed in a 16-pin, hermetically sealed, ceramic dual-in-line package. MN3014 is available for either 0°C to +70°C or −55°C to +125°C operation and features the following: 570mW maximum power consumption, 4 user-selectable output ranges, ±1/2 LSB linearity guaranteed over temperature, ±1/2LSB absolute accuracy guaranteed at +25°C and ±2LSB's guaranteed over temperature. MN3014 settles to within ±1/2LSB for a 20 Volt step in 2.5μsec maximum. For military/aerospace or harsh-environment commercial/industrial applications, MN3014H/B CH is fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

MN3014 was designed for applications in which adjustment-free operation and fast settling time are required and where space, weight and size are at a premium. Use of these units minimizes design and purchasing time and assures field interchangeability without the need for adjustment or recalibration.

BLOCK DIAGRAM



May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN3014 HIGH-SPEED 8-Bit D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C -55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
+15V Supply (Pin 16)	+18 Volts
-15V Supply (Pin 11)	-18 Volts
Digital Inputs (Pins 1-8)	-10 to +18 Volts

ORDERING INFORMATION

PART NUMBER — MN3014H/B CH

- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified -55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = 25° C, Supply Voltages ±15V, unless otherwise specified).

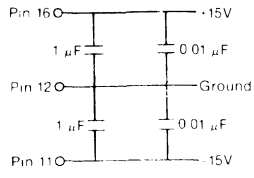
DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	2.0			Volts
Logic "0"			0.8	Volts
Input Currents: Logic "1" (Vin = 2.0 to +18 Volts)			10	μA
Logic "0" (Vin = -10 to +0.8 Volts)			10	μA
ANALOG OUTPUTS				
Unipolar Output Ranges		0 to +10, 0 to -10		Volts
Bipolar Output Ranges		±5, ±10		Volts
Output Impedance		0.5		Ω
Output Load Current	± 4			mA
TRANSFER CHARACTERISTICS				
Linearity Error (Note 1): 0°C to +70°C		± ¼	± ½	LSB
-55°C to +125°C			± ½	LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 2, 3): +25°C		± ¼	± ½	LSB
-55°C to +125°C (Note 4)			± 2	LSB
Zero Error (Note 5): +25°C		± ¼	± ½	LSB
-55°C to +125°C (Note 4)			± 1	LSB
DYNAMIC CHARACTERISTICS				
Settling Time (20 volt change to ±1/2 LSB): MN3014			2.5	μSec
Output Slew Rate: MN3014		20		V/μSec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
-15V Supply	-14.55	-15.00	-15.45	Volts
Power Supply Rejection (Note 6): +15V Supply		± 0.03		% FSR / % Vs
-15V Supply		± 0.01		% FSR / % Vs
Current Drain, Output Unloaded: +15V Supply		18	24	mA
-15V Supply		-10	-14	mA
Power Consumption		420	570	mW

SPECIFICATION NOTES:

1. Micro Networks tests and guarantees maximum linearity error at room temperature and both extremes of the specified operating temperature range.
2. The Absolute Accuracy Error of a voltage output D/A is the difference between the actual output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. Absolute Accuracy Error includes gain, offset, linearity, and noise errors and encompasses the drifts of these errors when specified over temperature. For the MN3014, the Full Scale Absolute Accuracy Error is the Absolute Accuracy Error measured when the digital input is 1111 1111 for the 0 to +10V range, 0000 0000 for the 0 to -10V range, and both 1111 1111 and 0000 0000 for the bipolar ranges (See Note 5).
3. For an 8 bit converter, 1 LSB corresponds to 0.39% FSR. FSR stands for Full Scale Range and is equivalent to the peak to peak voltage of the selected output range. For the +10V output range FSR is 20V and 1 LSB = 78 mV. For the other output ranges, FSR is 10V and 1 LSB = 39 mV.
4. For Commercial Models, this specification applies over the 0°C to +70°C temperature range. See Ordering Information.
5. Zero Error is the Absolute Accuracy Error measured when the output of the converter is supposed to be zero volts (see Note 2).
6. The MN3014 will operate over a power supply range of ±14V to ±18V with reduced accuracy.

DIGITAL INPUT	ANALOG OUTPUT (DC VOLT)			
MSB LSB	0 to +10V	0 to -10V	±5V	±10V
0000 0000	0.000	-9.961	-5.000	-10.000
0000 0001	+0.039	-9.922	-4.961	- 9.922
0111 1111	+4.961	-5.000	-0.039	- 0.078
1000 0000	+5.000	-4.961	0.000	0.000
1111 1110	+9.922	-0.039	+4.922	+ 9.844
1111 1111	+9.961	0.000	+4.961	+ 9.922
CONNECT	9 to 12	9 to 15	9 to 12	9 to 12
PIN to PIN	10 to 12	10 to 15	10 to 15	10 to 15
	13 to 15	13 to 15	13 to 15	

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies. The unit's ground pin (Pin 12) should be connected to system analog ground, preferably through a large ground plane beneath the package. Power supplies should be decoupled with 1 μF capacitors paralleled with 0.01 μF ceramic capacitors as shown in the diagram.



MICRO NETWORKS

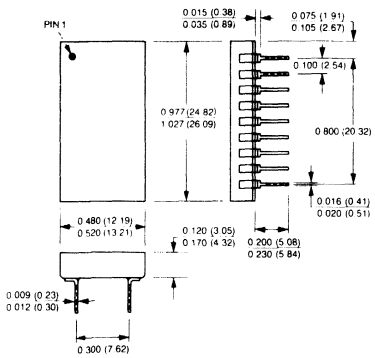
MN3020

8-Bit D/A CONVERTER
with INPUT REGISTER

FEATURES

- **Complete D/A Converters:**
  High-Speed Input Register
  Internal Reference
  Internal Output Amplifier
- **±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **Small 18-Pin DIP**
- **Adjustment-Free**
- **±1LSB Unadjusted Absolute Accuracy Over Temperature**
- **3μsec Maximum Settling Time (10V Step to ±1/2LSB)**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN3020 is an 8-bit digital-to-analog converter complete with internal reference, output amplifier and input register. It is packaged in a hermetically sealed, ceramic, 18-pin dual-in-line and features the following: 4 user-selectable output ranges (2 unipolar, 2 bipolar), fast output settling (3μsec max for a 10 Volt change) and linearity and accuracy specifications guaranteed over temperature.

The MN3020's hybrid construction combines a low-drift voltage reference, Micro Networks ultrastable thin-film resistor networks, and the newest monolithic chips available. Active laser trimming results in a device with ± ½ LSB linearity and ± 1LSB unadjusted absolute accuracy error guaranteed over the entire operating temperature range.

Units are available for either 0°C to +70°C or −55°C to +125°C (H models) operation, and Micro Networks 100% tests and guarantees both linearity and accuracy at room temperature and at both operating temperature extremes. For military/aerospace or harsh-environment commercial/industrial applications, MN3020H/B CH is fully screened to MIL-H-38534 in Micro Networks' qualified facility.

MN3020's digital inputs are TTL compatible, and its internal input register facilitates interfacing to microprocessor and minicomputer data buses. Applications include microprocessor-based data distribution systems, programmable power supplies, low-resolution displays, and servo drivers. Optional MIL-H-38534 processing and accuracy specs guaranteed over the −55°C to +125°C temperature range make the MN3020 an excellent choice for military avionics and fire control systems.

May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN3020 8-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	-55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
+15V Supply (Pin 1)	+18 Volts
-15V Supply (Pin 13)	-18 Volts
+5V Supply (Pin 11)	-0.5 to +7 Volts
Digital Inputs (Pins 2-9)	-0.5 to +5.5 Volts
Register Enable (Pin 10)	-0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— **MN3020H/B CH**

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified -55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

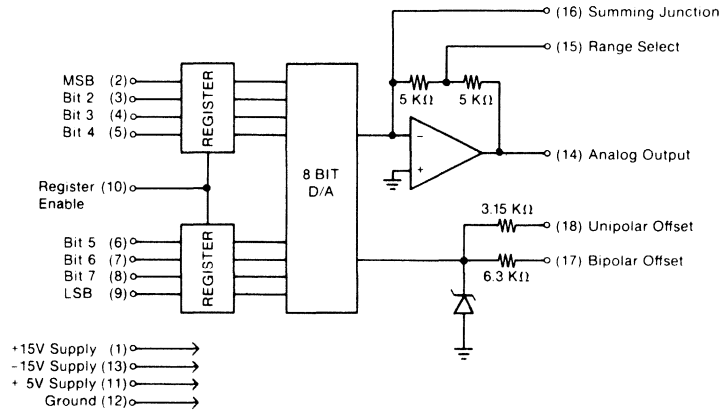
SPECIFICATIONS (T_A = 25°C, Supply Voltages ±15V and +5V, unless otherwise specified).

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution		8		Bits
Logic Coding: Unipolar Ranges Bipolar Ranges		Straight Binary Offset Binary		
Logic Levels: Logic "1" Logic "0"	2.0		 0.7	Volts Volts
Input Currents Data Inputs: Logic "1" (Vin = 2.4 Volts) Logic "0" (Vin = 0.3 Volts) Register Enable: Logic "1" (Vin = 2.4 Volts) Logic "0" (Vin = 0.3 Volts)			 30 - 0.6 40 - 0.8	 μA mA μA mA
Register Enable (Note 1): Pulse Width Setup Time Digital Data to Enable	 60 40			 nSec nSec
ANALOG OUTPUTS				
Output Voltage Ranges: Unipolar Bipolar		0 to +10, 0 to -10 ±5, ±10		Volts Volts
Output Impedance Output Current	 ±4	0.5		Ω mA
TRANSFER CHARACTERISTICS				
Linearity Error (Notes 2, 4): 0°C to +70°C -55°C to +125°C		± [illegible] 	± [illegible] ± [illegible]	LSB LSB
Monotonicity		Guaranteed Over Temperature		
Absolute Accuracy Error (Notes 3, 4): 0°C to +70°C -55°C to +125°C		± [illegible] 	± 1 ± 1	LSB LSB
Unipolar Offset Error (Notes 3, 4): 0°C to +70°C -55°C to +125°C			± 1 ± 1	LSB LSB
Bipolar Offset Error (Notes 3, 4): 0°C to +70°C -55°C to +125°C			± 1 ± 1	LSB LSB
Offset Drift (Note 6): Unipolar Positive Range Unipolar Negative Range Bipolar Ranges		± 2 ±10 ±10		ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C
Bipolar Zero Error: 0°C to +70°C -55°C to +125°C			± 1 ± 1	LSB LSB
Gain Error Gain Drift (Note 6)		± 0.1 ±15		% ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time (10 Volt Change to ±1/2 LSB) Output Slew Rate		 20	3.0	μSec Volts/μSec
POWER SUPPLIES				
Power Supply Range: +15V Supply -15V Supply +5V Supply	+14.0 -14.0 + 4.75	+15.0 -15.0 + 5.0	+18.0 -18.0 + 5.25	Volts Volts Volts
Power Supply Rejection: +15V Supply -15V Supply		± 0.03 ± 0.01		%FSR/%Vs %FSR/%Vs
Current Drain, Output Unloaded: +15V Supply -15V Supply +5V Supply		15 -11 23	20 -13 37	mA mA mA
Power Consumption		505	680	mW

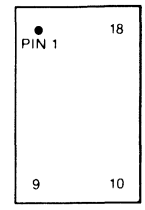
SPECIFICATION NOTES:

1. Converter analog output will follow digital input when Register Enable is a logic "0". Digital input data will be latched and analog output voltage constant when Register Enable is a logic "1". The minimum Register Enable pulse width to latch new digital input data is 60 nSec. See Timing Diagram.
2. Micro Networks tests and guarantees maximum Linearity Error at room temperature and at both extremes of the specified operating temperature range.
3. The Absolute Accuracy Error specification applies over the converter's entire output range. See Absolute Acuracy Error section below for an explanation of how Micro Networks Corporation tests and specifies Absolute Accuracy Error, Offset Error, and Bipolar Zero Error.
4. 1 LSB for an 8 bit converter corresponds to 0.39%FSR. See Note 5.
5. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected output range. For the ±10V output range, FSR is 20 volts, and 1 LSB is equal to 78mV. For the 0 to +10V range, FSR is 10 volts, and 1 LSB is equal to 39mV.
6. Over specified operating temperature range.

BLOCK DIAGRAM



PIN DESIGNATIONS



1.	+15V Supply	18.	Unipolar Offset
2.	Bit 1 (MSB)	17.	Bipolar Offset
3.	Bit 2	16.	Summing Junction
4.	Bit 3	15.	Range Select
5.	Bit 4	14.	Analog Output
6.	Bit 5	13.	-15V Supply
7.	Bit 6	12.	Ground
8.	Bit 7	11.	+5V Supply
9.	Bit 8 (LSB)	10.	Register Enable

ABSOLUTE ACCURACY ERROR

The Absolute Accuracy Error of a voltage output D/A converter is the difference between the actual, unadjusted, output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. This difference is usually expressed in LSB's or %FSR (see Note 5 above). Absolute Accuracy Error includes gain, offset, linearity, noise and all other errors, and includes the drifts of these errors when specified over temperature.

For the MN3020, Micro Networks tests Absolute Acuracy Error at both endpoints of all unipolar output ranges and at both endpoints and the midpoint of all bipolar output ranges. These tests are performed at both room temperature and at the high and low extremes of the specified extended temperature range.

Example: For the MN3020H's ±10V output range (see Input Coding and Output Range Selection), the expected output for a 0000 0000 digital input is -10 volts; the expected output for a 1000 0000 digital input is 0 volts; and the expected output for a 1111 1111 digital input is +9.922 volts. Micro Networks measures all three actual, unadjusted output voltages at -55°C, +25°C and +125°C and guarantees them to be within ±1 LSB of their ideal values.

Unipolar Offset Error, Bipolar Offset Error, and Bipolar Zero Error are all Absolute Accuracy Errors. Their definitions differ with respect to where along the converter's digital input/analog output transfer function the errors are to be measured, i.e., different analog output errors are measured at different digital input codes.

OFFSET ERROR—For the MN3020; Offset Error is the Absolute Accuracy Error measured when the digital input is 0000 0000. For the unipolar positive range, this specification tells how accurate the unadjusted converter will be when its output is supposed to be zero volts. For the unipolar negative and the bipolar ranges, it tells how accurate the unadjusted converter will be when its output is supposed to be at its munus full scale value.

BIPOLAR ZERO ERROR—Bipolar Zero Error is the Absolute Accuracy Error measured when the digital input is 1000 0000 and the converter is operating in a bipolar mode. It is the error measured when the output is supposed to be zero volts on the ±5V and ±10V output ranges.

It is redundant to specify Offset and Bipolar Zero Errors after giving an Absolute Accuracy Error spec that applies over the converter's entire output range. We have provided the Offset and Bipolar Zero Error specs to simplify comparing the MN3020 to other 8 bit D/A's. Be sure you clearly understand each manufacturer's specification definitions before you compare converters solely on a data sheet basis.

GAIN ERROR—Gain Error is the difference between the ideal and the measured values of a converter's full scale range (minus 1 LSB). See Note 5 above. It is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 1111 1111 digital input minus that measured for the 0000 0000 digital input, and it is usually expressed as a percentage.

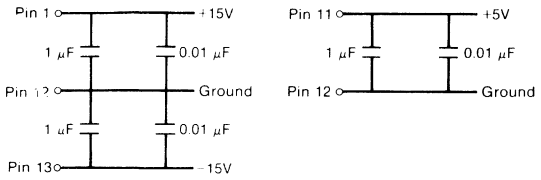
See the Converter Tutorial Section of the Micro Networks' Product Catalogue for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN3020. The unit's Ground pin (pin 12) should be tied to system analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the MN3020. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

POWER SUPPLY DECOUPLING

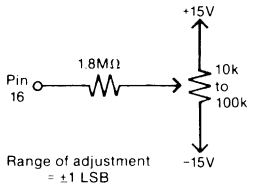


Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used when tying pins together for output range selection, especially when connecting either of the offset pins (pins 17 and 18) to the summing junction (pin 16). If external offset adjustment is employed, the 1.8 megom resistor should be located as close to the package as possible.

OPTIONAL OFFSET ADJUSTMENT—A constant offset voltage can be added to or subtracted from the output of the MN3020 for the purpose of increasing accuracy at and around a particular output level.

This is accomplished by using an external potentiometer to add or subtract current at the summing junction of the MN3020's internal output amplifier. Because the MN3020 is not equipped for gain adjustment, offsetting the output to increase the accuracy of any particular output level may degrade the accuracy of other levels. Adjustment should be made following warm-up and a multiturn potentiometer with a TCR of 100 ppm/°C or less should be used to minimize drift with temperature.

Connect the offset potentiometer as shown; apply the desired input code (see Coding Table); adjust the offset potentiometer until the desired output level is achieved. If offset adjustment is not used, pin 16 should be connected as described in the Range Selection section.



MICROPROCESSOR INTERFACING — Interfacing the MN3020 to a microprocessor is simplified by the MN3020's internal register. External address and control decoding is required, however. These functions can usually be accomplished by NANDing the appropriate address and control lines and using the output to drive the MN3020's Register Enable input.

For most processors, valid data remains on the data bus for a period of time after the removal of either valid address or control signals. This results in data being latched into the MN3020 immediately after one of the address or control signals changes but before valid data goes away.

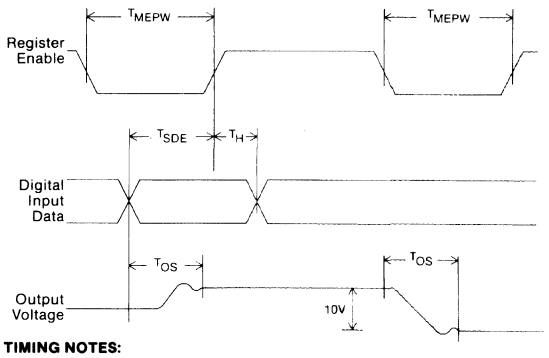
For connecting multiple MN3020's to a processor data bus in data distribution system applications, 3 line to 8 line and 4 line to 16 line decoders can be used to selectively active the MN3020s' input registers.

The MN3020's digital data inputs can usually be tied directly to the processor's data bus with each input presenting approximately one low power TTL load to the bus.

INPUT CODING AND OUTPUT RANGE SELECTION

DIGITAL INPUT	ANALOG OUTPUT (DC VOLTS)			
MSB LSB	UNIPOLAR POSITIVE	UNIPOLAR NEGATIVE	BIPOLAR ±5	BIPOLAR ±10
00000000	0.000	-9.961	-5.000	-10.000
00000001	+0.039	-9.922	-4.961	- 9.922
01111111	+4.961	-5.000	-0.039	- 0.078
10000000	+5.000	-4.961	0.000	0.000
11111110	+9.922	-0.039	+4.922	+ 9.844
11111111	+9.961	0.000	+4.961	+ 9.922
CONNECT PIN TO PIN	14 to 15 17 to GND 18 to GND	14 to 15 16 to 18 17 to GND	14 to 15 16 to 17 18 to GND	16 to 17 18 to GND

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW}	Minimum enable pulse width is 60 nSec.
T_{SDE}	Minimum setup time digital input data to enable is 40 nSec.
T_H	Hold time is defined as the required delay between the leading edge of register enable and the end of valid input data. For the MN3020, the hold time is zero.
T_{OS}	Output settling time for a 10 volt change to ±1/2 LSB is 3 μSec max.

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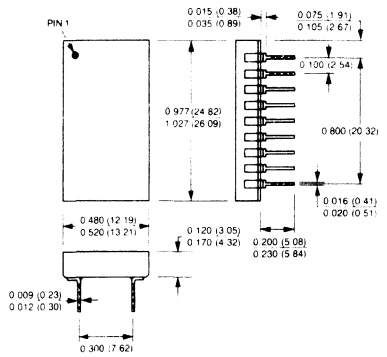
MN3040

10-Bit D/A CONVERTER
with INPUT REGISTER

FEATURES

- **Complete With Internal:**
  Input Register
  Output Op Amp
  Reference
- **±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **Small 18-Pin DIP**
- **40nsec Setup Time**
- **Adjustment-Free**
- **±0.1% FSR Unadjusted Absolute Accuracy Over Temperature**
- **10μsec Max Settling Time (20V step to ±1/2LSB)**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN3040 is a fast, 10-bit digital-to-analog converter with a fast TTL input register for easy interfacing and rapid throughputs in microprocessor-based systems. It is packaged in a hermetically sealed, ceramic, 18-pin dual-in-line and is complete with internal reference and output amplifier. Two output ranges are available (0 to −10V and ±10V), and performance features include the following: fast output settling (typically 5μsec for a 20V change), ±0.1%FSR overall accuracy, and ±½LSB linearity and monotonicity guaranteed over the entire operating temperature range. Maximum power consumption is 715 mW.

The MN3040 is actively laser trimmed as a complete device for linearity, gain and offset, eliminating the need for external adjusting potentiometers. Units are available for either 0°C to +70°C or −55°C to +125°C ("H" models) operation, and Micro Networks 100% tests and guarantees both linearity and accuracy at room temperature and at both operating temperature extremes. For military/aerospace or harsh-environment commercial/industrial applications, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

The MN3040's digital inputs are TTL compatible, and its internal input register facilitates interfacing to microprocessor and minicomputer data buses. Applications include microprocessor-based data distribution systems, programmable power supplies, low-resolution displays and servo drivers. Optional MIL-H-38534 processing and linearity and accuracy specs guaranteed over the −55°C to +125°C temperature range make MN3040 and excellent choice for military avionics and fire control systems.

May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN3040 10-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Specified Temperature	0°C to +70°C (Standard)
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
+15V Supply (Pin 8)	+18 Volts
−15V Supply (Pin 9)	−18 Volts
+5V Supply (Pin 7)	−0.5 to +7 Volts
Digital Inputs (Pins 1-5, 14-18)	−0.5 to +5.5 Volts
Register Enable (Pin 6)	−0.5 to +5.5 Volts
Output Current	(Note 1)

ORDERING INFORMATION

PART NUMBER — MN3040H/B CH

- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified −55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

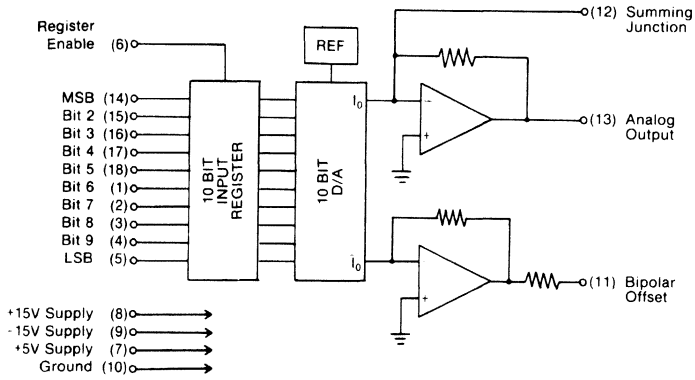
SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V, unless otherwise specified)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Coding: Unipolar (0 to −10V) Range Bipolar (−10 to +10V) Range		Complementary Binary Complementary Offset Binary		
Logic Levels: Logic "1" Logic "0"	2.0		 0.7	Volts Volts
Input Currents Data Inputs: Logic "1" (V_{in} = 2.4 Volts) Logic "0" (V_{in} = 0.3 Volts) Register Enable: Logic "1" (V_{in} = 2.4 Volts) Logic "0" (V_{in} = 0.3 Volts)			 30 − 0.6 60 − 1.2	 μA mA μA mA
Register Enable (Note 2): Pulse Width Setup Time Digital Data to Enable	 60 40			 nSec nSec
ANALOG OUTPUTS				
Output Impedance Output Load Current	 ±4	0.5		Ω mA
TRANSFER CHARACTERISTICS				
Linearity Error (Notes 3, 5): 0°C to +70°C −55°C to +125°C ("H" Models)		±¼	±½ ±½	LSB LSB
Monotonicity		Guaranteed Over Temperature		
Absolute Accuracy Error (Notes 4, 5): +25°C 0°C to +70°C −55°C to +125°C ("H" Models)		 ± 0.05 ± 0.1 ± 0.2	 ±0.1 ±0.4 ±0.4	 %FSR %FSR %FSR
Gain Error Gain Drift		± 0.1 ±15		% ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time (20V Change to ±1/2 LSB) Output Slew Rate		5 15	10	μSec V/μSec
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply −15V Supply +5V Supply	+14.00 −14.00 + 4.75	+15.00 −15.00 + 5.00	+17.00 −17.00 + 5.25	Volts Volts Volts
Power Supply Rejection: +15V Supply −15V Supply		± 0.005 ± 0.005		%FSR/%Vs %FSR/%Vs
Current Drain, Output Unloaded: +15V Supply −15V Supply +5V Supply		13 − 7 30	20 −11 50	mA mA mA
Power Consumption		450	715	mW

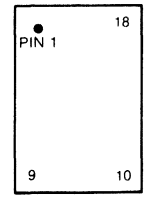
SPECIFICATIONS NOTES

1. The output is short circuit protected to ground or either supply.
2. Converter analog output will follow digital input when Register Enable is a logic "0". Digital input data will be latched and analog output voltage constant when Register Enable is a logic "1". The minimum Register Enable pulse width to latch new digital input data is 60 nSec. See Timing Diagram.
3. Micro Networks tests and guarantees maximum Linearity Error at room temperature and at both extremes of the specified operating temperature range.
4. The Absolute Accuracy Error specification applies over the converter's entire output range. See Absolute Accuracy Error section below for an explanation of how Micro Networks Corporation tests and specifies Absolute Accuracy Error and Gain Error.
5. 1 LSB for a 10 bit converter corresponds to 0.098% FSR. See Note 6.
6. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected output range. For the ±10V output range, FSR is 20 volts, and 1 LSB is equal to 19.5 mV. For the 0 to −10V range, FSR is 10 volts, and 1 LSB is equal to 9.8mV.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 Bit 6	18 Bit 5
2 Bit 7	17 Bit 4
3 Bit 8	16 Bit 3
4 Bit 9	15 Bit 2
5 Bit 10 (LSB)	14 Bit 1 (MSB)
6 Register Enable	13 Analog Output
7 +5V Supply	12 Summing Junction
8 +15V Supply	11 Bipolar Offset
9 −15V Supply	10 Ground

ABSOLUTE ACCURACY ERROR

The Absolute Accuracy Error of a voltage output D/A converter is the difference between the actual, unadjusted output voltage that appears following the application of a given digital input code and the ideal or expected output voltage for that code. This difference is usually expressed in LSB's or %FSR (see Note 6 in the Specification Notes). Absolute Accuracy Error includes gain, offset, linearity, and noise errors and encompasses the drifts of these errors when specified over temperature.

For the MN3040, Micro Networks tests Absolute Accuracy Error at both endpoints of the unipolar output range (0 to -10V) and at both endpoints and the midpoint of the bipolar output range ±10V). These tests are performed at room temperature and at the high and low extremes of the specified operating temperature range.

Example: For the MN3040H (−55°C to +125°C temperature range) operating on its ±10V output range, the expected analog output for a 11 1111 1111 digital input is 9.9805V (see Input Coding and Range Selection). The expected output for a 10 0000 0000 digital input is 0 volts, and the expected output for a 00 0000 0000 digital input is +10.0000V. Micro Networks measures all three actual, unadjusted output voltages at -55°C, +25°C, and +125°C. We guarantee that at +25°C, all three will be within ±0.1%FSR (±20mV) of their ideal values and that over the entire −55°C to +125°C operating temperature range, all three will be within ±0.4%FSR (±80 mV) of their ideal values. By also testing and guaranteeing ±½ LSB Linearity over temperature, we guarantee the transfer function will be monotonic and that every output level will be within our Absolute Accuracy specification of where it is ideally supposed to be. Please see the Input Coding Table.

OFFSET ERROR — Bipolar and Unipolar Offset Error are Absolute Accuracy Errors. It would be redundant to specify them after giving an Absolute Accuracy Error that applies over the converter's entire output range.

GAIN ERROR — Gain Error is the difference between the ideal and the measured values of a converter's full scale range (minus 1 LSB). It is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 00 0000 0000 digital input minus that measured for the 11 1111 1111 digital input, and it is usually expressed as a percentage.

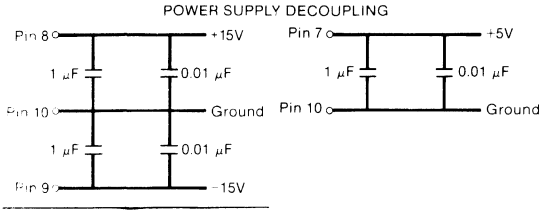
See the Converter Tutorial Section of the Micro Networks' Product Guide and Applications Manual for a complete discussion of converter specifications, and be sure you clearly understand each manufacturer's specification definition before you compare converters solely on a data sheet basis.

INPUT CODING AND OUTPUT RANGE SELECTION

DIGITAL INPUT	ANALOG OUTPUT (DC VOLTS)	
MSB LSB	0 to −10V	+10 to −10V
00 0000 0000	0.0000	+10.0000
00 0000 0001	−0.0098	+9.9805
01 1111 1111	−4.9902	+0.0195
10 0000 0000	−5.0000	0.0000
10 0000 0001	−5.0098	−0.0195
11 1111 1110	−9.9805	−9.9609
11 1111 1111	−9.9902	−9.9805
Pin Connections	Pin 11 Open Pin 12 Open	Pin 11 to Pin 12

APPLICATIONS INFORMATION

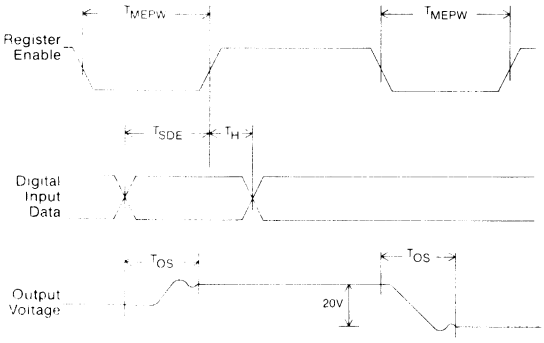
LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN3040. The unit's Ground pin (pin 10) should be tied to system analog ground as close to the package as possible, preferably through a large ground plane underneath the package.



Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the MN3040. For optimum performance, 1 μF capacitors paralleled with 0.01 μF ceramic capacitors should be used as shown in the diagrams below.

REGISTER ENABLE — When the Register Enable (Pin 6) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60 nSec and digital input data must be valid for a minimum of 40 nSec prior to Register Enable going high again.

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW}	Minimum enable pulse width is 60 nSec.
T_{SDE}	Minimum setup time digital input data to enable is 40 nSec.
T_H	Hold time is defined as the required delay between the leading edge of register enable and the end of valid input data. For the MN3040 the hold time is zero.
T_{OS}	Output settling time for a 20 volt change to ±½LSB is 10μSec max.

MICROPROCESSOR INTERFACING

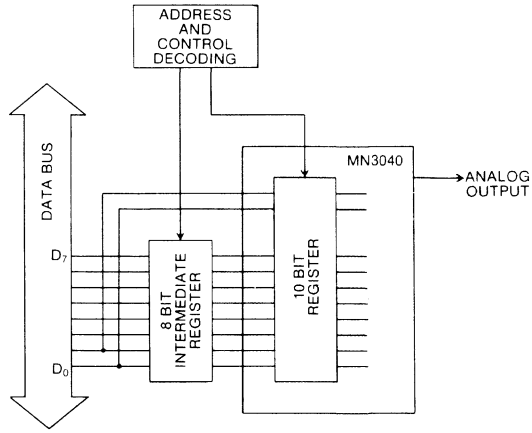
Interfacing the MN3040 to 8, 12, and 16 bit microprocessors is simplified by the MN3040's internal 10 bit register. External address and control decoding will be required, however.

Interfacing to 12 and 16 bit processors is fairly direct and can usually be accomplished by NANDing the desired address lines with processor's MEMORY WRITE or I/O WRITE line and using the output to drive the MN3040's Register Enable input. For most processors, valid data remains on the data bus for a period of time after the removal of either valid address or control signals. This results in data being latched into the MN3040 immediately after one of the address or control signals changes but before valid data goes away.

Interfacing to 8 bit processors is slightly more complicated and an 8 bit external register is needed as shown in the sketch below.

Address decoding must be organized such that the 8 bit intermediate register and the MN3040's internal 10 bit register appear at two different addresses. The 10 bits of digital data are sent to the MN3040 via two data transfers. First, the 8 least significant bits of digital data are written to the intermediate latch. Then the 2 most significant bits of digital data are written to the MN3040's 10 bit latch. The result is that the 2 MSB's on the data bus and the 8 LSB's held in the intermediate latch are all latched into the MN3040's latch simultaneously. If one wants to change only the MSB and/or bit 2, only a single write operation is necessary.

If the intermediate latch is tied to the MN3040's 8 most significant bits, it would take only a single write operation to change only the LSB and/or bit 9. To change any of the other bits would involve two write operations. This latter configuration would reduce software if one were using the MN3040 to generate smooth waveforms.



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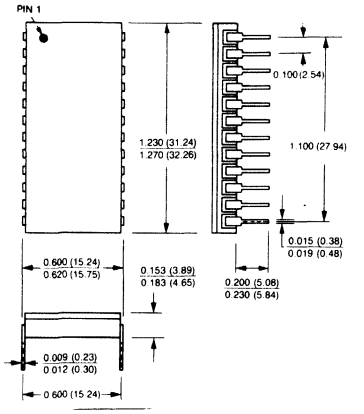
MN3290 Series

Extended-Temperature
16-Bit D/A Converters

FEATURES

- 16-Bit Resolution
- Fully Specified −55°C to +125°C Operation
- ±0.006% FSR Linearity and 14-Bit Monotonicity Guaranteed Over Temperature
- Complete with Internal Reference and Output Op Amp (V Models)
- Current or Voltage Output:
  - 3 Voltage Ranges
  - 2 Current Ranges
- Fast Settling to ±0.003%FSR:
  - 8μsec Max (V Models)
  - 1μsec Max (I Models)
- DAC71/DAC72 Pin and Function Compatible
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

24-PIN SIDE-BRAZED DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN3290 Series consists of six different devices including three voltage-output models (0 to +10V, ±5V, ±10V) and three current-output models (0 to −2mA, ±1mA with 5kΩ feedback, ±1mA with 10kΩ feedback). Each device is complete with its own precision, buried-zener reference (+6.3V) and low-noise, fast-settling, output op amp (voltage-output models). Packaging is standard, 24-pin, side-brazed, ceramic DIP. Power consumption is 975mW max, and no +5V supply is required. Settling time to ±0.003%FSR is a quick 8μsec max for "V-out" devices and 1μsec max for "I-out" devices.

For demanding military/aerospace or extended-temperature commercial/industrial applications, the MN3290 Series of 16-bit D/A converters has overcome virtually every problem associated with the multi-sourced, industry-standard, DAC71/DAC72 Family. Integral linearity, monotonicity (to the 14-bit level), gain and offset drift, and TTL compatibility are all guaranteed over each device's full specified temperature range (including −55°C to +125°C); while full DAC71/DAC72 pin and function compatibility are retained.

To accommodate any application, each of MN3290's six models offers four different electrical grades ("J" and "K" devices for 0°C to +70°C operation; "S" and "T" devices for −55°C to +125°C operation) as summarized below. "S/B" and "T/B" models are available with Environmental Stress Screening. "S/B CH" and "T/B CH" models are screened in accordance with MIL-H-38534.

Base (1) Part Number	Output Range	Monotonicity Over Temperature			
		0°C to +70°C		−55°C to +125°C	
		J	K	S (2)	T (2)
MN3290X-I	0 to −2mA	13 Bits	14 Bits	13 Bits	14 Bits
MN3290X-V	0 to +10V	13 Bits	14 Bits	13 Bits	14 Bits
MN3291X-I	±1mA	13 Bits	14 Bits	13 Bits	14 Bits
MN3291X-V	±5V	13 Bits	14 Bits	13 Bits	14 Bits
MN3292X-I	±1mA	13 Bits	14 Bits	13 Bits	14 Bits
MN3292X-V	±10V	13 Bits	14 Bits	13 Bits	14 Bits

1. Select the suffix J, K, S or T in the "X" position for full part number.
2. S and T models are available with 100% screening to MIL-STD-883. Add "/B" to part number.

September 1989

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN3290 Series Extended-Temperature 16-Bit D/A Converters

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN329XJ, MN329XK	0°C to +70°C
MN329XS, S/B; MN329XT, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 23)	0 to +18 Volts
−15V Supply (−Vcc, Pin 19)	0 to −18 Volts
Digital Input Voltage (Pins 1-16)	−1 to +18 Volts
External Voltage Applied to R_F (Pin 17, I Models)	±18 Volts
External Voltage Applied to V_{OUT} (Pin 17, V Models)	±5 Volts
Short Circuit Duration:	
Ref. Out (Pin 24) to Ground	Indefinite
V_{OUT} (Pin 17) to Ground	Indefinite

ORDERING INFORMATION

PART NUMBER — MN329XX/B-X CH

Select MN3290, MN3291, or MN3292 with either "-I" or "-V" suffix for selected output range.

Select J, K, S or T suffix for specified temperature range and electrical performance.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

Add "CH" to "S/B" or "T/B" models for 100% screening to MIL-H-38534.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution		16		Bits
Logic Levels (Note 1): Logic "1"	+2.4		+Vcc	Volts
Logic "0"	−1.0		+0.8	Volts
Input Currents (Note 1): Logic "1" (V_{IH} = +2.7V)		+20	+40	μA
Logic "0" (V_{IL} = +0.4V)		−0.35	−0.5	mA
Logic Coding (Note 2):				
Voltage Output: Unipolar Range		CSB		
Bipolar Ranges		COB		
Current Output: Unipolar Range		SB		
Bipolar Range		OB		
VOLTAGE OUTPUTS				
Output Voltage Ranges: MN3290X-V		0 to +10		Volts
MN3291X-V		±5		Volts
MN3292X-V		±10		Volts
Output Impedance		0.15		Ohms
Output Current	±5			mA
CURRENT OUTPUTS (Note 15)				
Output Current Ranges: MN3290X-I		0 to −2		mA
MN3291X-I (Note 3)		±1		mA
MN3292X-I (Note 3)		±1		mA
Output Source Impedance: MN3290X-I		4		kΩ
MN3291X-I		2.45		kΩ
MN3292X-I		2.45		kΩ
Output Compliance Voltage (Note 4)		±2.5		Volts
DYNAMIC CHARACTERISTICS				
Settling Time (to ±0.003%FSR):				
Voltage Output: Full-Scale Step		4	8	μsec
1LSB Step (Note 5)		2.5		μsec
Current Output (Note 7): 10 to 100Ω Load		0.35	1	μsec
1kΩ Load		1	3	μsec
Output Slew Rate (Voltage Output Only)		±10		V/μsec
REFERENCE OUTPUT				
Internal Reference: Voltage	+6.0	+6.3	+6.6	Volts
Drift:		±10		ppm/°C
External Source Current	1.5	2.5		mA

SPECIFICATION NOTES

1. Specified logic levels and input currents are guaranteed over each device's entire specified temperature range as selected by part number suffix.
2. CSB = Complementary straight binary; COB = Complementary offset binary; SB = Straight binary; OB = Offset binary. See Digital Input Coding.
3. The MN3291X-I has an internal 5kΩ feedback resistor which can be used with an external output op amp to generate a ±5V output voltage. The MN3292X-I has an internal 10kΩ feedback resistor which can be used to generate a ±10V output voltage.
4. For current-output devices, compliance voltage is the maximum voltage swing allowed at the output pin while still being able to maintain specified accuracy and linearity.
5. The "1LSB" settling time applies to the theoretical worst-case step which is the major carry (1000 0000 0000 0000 to 0111 1111 1111 1111).
6. Specified with no load.
7. Current-out settling time is strongly influenced by the output RC time constant and is therefore a function of load.
8. FSR = Full Scale Range and is equal to the nominal peak-to-peak voltage or current of the selected output range. A unit with a ±10V output range (MN3292X-V) has a 20V FSR. A unit with a 0 to +10V output (MN3290X-V) or ±5V output (MN3291X-V) has a 10V FSR.

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range:	±13.5	±15	±16.5	Volts
Current Drains (Note 6):				
Voltage Models: +15V Supply		+18	+35	mA
−15V Supply		−17	−30	mA
Current Models: +15V Supply		+15	+30	mA
−15V Supply		−14	−25	mA
Power Supply Rejection Ratio:				
J and S Models: +15V Supply		±0.0015	±0.006	%FSR/%Vs
−15V Supply		±0.0015	±0.006	%FSR/%Vs
K and T Models: +15V Supply		±0.0015	±0.003	%FSR/%Vs
−15V Supply		±0.0015	±0.003	%FSR/%Vs
Power Consumption: V Models		525	975	mW
I Models		435	825	mW

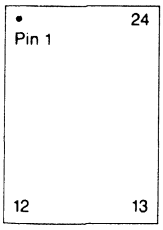
PERFORMANCE SPECIFICATIONS (Typical @ T_A = +25°C, ±Vcc = ±15V unless otherwise indicated) (Notes 8, 15)

MODEL	MN329XJ-X	MN329XK-X	MN329XS-X	MN329XT-X	Units
Integral Linearity Error (Note 9)					
Initial (+25°C, Max)	±0.006	±0.003	±0.006	±0.003	%FSR
Over Temperature (Max, Note 10)	±0.012	±0.006	±0.012	±0.006	%FSR
Resolution for which Monotonicity is Guaranteed:					
Initial (+25°C)	14	14	14	14	Bits
Over Temperature (Note 10)	13	14	13	14	Bits
Unipolar Offset Error (Notes 11, 12)					
Initial (+25°C, Max)	±0.1	±0.1	±0.1	±0.1	%FSR
Drift (Max, Note 10)	±10	±5	±10	±5	ppm of FSR/°C
Bipolar Zero Error (Notes 11, 13)					
Initial (+25°C, Max)	±0.1	±0.1	±0.1	±0.1	%FSR
Drift (Max, Note 10)	±15	±10	±15	±10	ppm of FSR/°C
Gain Error (Notes 11, 14)					
Initial (+25°C, Max)	±0.1	±0.1	±0.1	±0.1	%
Drift (Max, Note 10)	±20	±15	±20	±15	ppm/°C

SPECIFICATION NOTES

9. ±0.003% FSR is equivalent to ± ½LSB for 14 bits. ±0.006% FSR is equivalent to ± ½LSB for 13 bits.
10. J and K models are fully specified for 0°C to +70°C operation. S and T models are fully specified for −55°C to +125°C operation.
11. Initial gain and offset errors are trimmable to zero with user-optional external potentiometers.
12. Unipolar offset error applies to the MN3290X-X only. It is defined as the difference between the actual and the ideal output (zero Volts) with a digital input of all "1's".
13. Bipolar zero error applies to the MN3291X-X and MN3292X-X only. It is defined as the difference between the actual and the ideal output (zero Volts) with the digital code 0111 1111 1111 1111 applied.
14. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage or current span from the 1111 1111 1111 1111 output to the 0000 0000 0000 0000 output.
15. For current-output devices, the tolerance on output current and output impedance is ±30%. Current-out models are specified and tested (for all parameters except settling time) with an external op amp connected using the internal feedback resistor.

PIN DESIGNATIONS



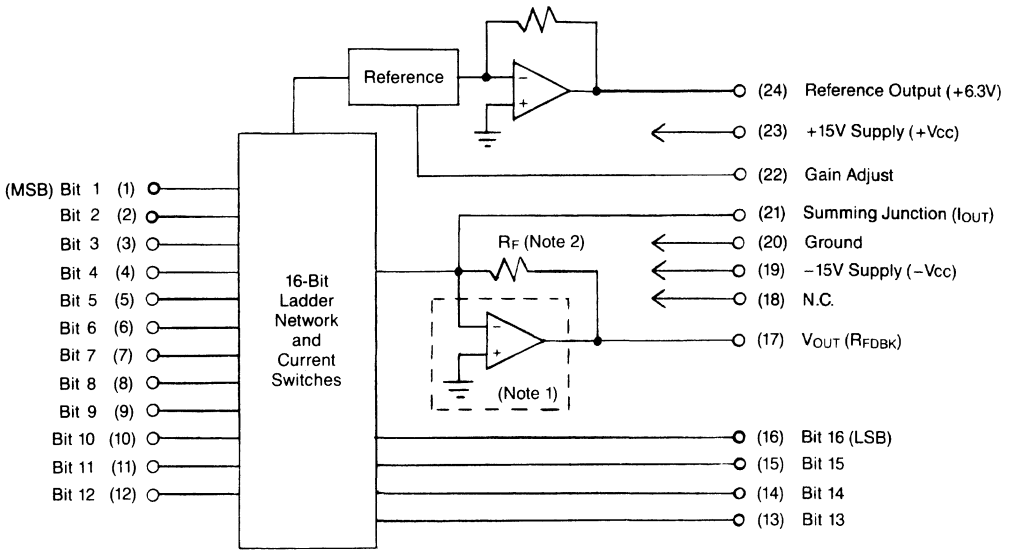
NOTES:

1. Pin 21 is also the zero-adjust point.
2. No connects (N.C.) are not connected internally.

1 Bit 1 (MSB)
2 Bit 2
3 Bit 3
4 Bit 4
5 Bit 5
6 Bit 6
7 Bit 7
8 Bit 8
9 Bit 9
10 Bit 10
11 Bit 11
12 Bit 12

24 Reference Out (+6.3V)
23 +15V Supply (+Vcc)
22 Gain Adjust
21 Summing Junction (V Models)
I_{OUT} (I Models)
20 Ground
19 −15V Supply (−Vcc)
18 N.C.
17 V_{OUT} (V Models)
$R_{FEEDBACK}$ (I Models)
16 Bit 16 (LSB)
15 Bit 15
14 Bit 14
13 Bit 13

BLOCK DIAGRAM



Notes:

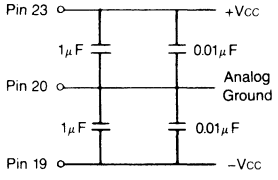
1. Current-output models do not have an internal output amplifier.
2. R_F = 5kΩ for MN3290 and MN3291.
   R_F = 10kΩ for MN3292.
3. Pin 21 is also the zero-adjust point.
4. No connects (N.C.) are not connected internally.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified linearity and accuracy from MN3290 Series devices. It is critically important that power supplies be filtered, well-regulated, and free from high-frequency noise. Use of noisy supplies can easily cause unstable output levels to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit or better accuracy unless great care is used in filtering any switching spikes present in the output.

MN3290/91/92's Ground pin (pin 20) should be connected to system analog ground, preferably through a large, low-impedance, analog ground plane beneath the package.

Power supply connections should be short and direct, and all supply lines should be decoupled (bypassed) with tantalum or electrolytic capacitors located close to the unit. For optimum performance, a relatively large tantalum (1-10μF) paralleled with a smaller (0.01-1.0μF) ceramic disc should be used as shown in the diagram below.



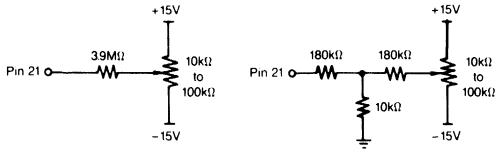
Coupling between digital inputs and analog output should be minimized to avoid noise pick-up. Pins 21 (Summing Junction), 24 (Reference Output), and 22 (Gain Adjust) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing these pins. If using external offset and gain adjustments, the series resistors and adjusting pots should be located as close to MN3290/91/92 as possible. If using optional gain adjust, an 0.01μF ceramic capacitor should be connected between pin 22 and analog ground as close to the package as possible. Similarly, if using the Reference Output (pin 24) to drive an external load, an 0.01μF ceramic capacitor should be connected between pin 24 and analog ground.

MN3290/91/92 has an integral linearity specification (±0.003%FSR) equivalent to that of a "true" 14-bit converter. If one wishes to use only 14 of MN3290/91/92's 16 digital input lines, bit 15 (pin 15) and bit 16 (pin 16) may be connected to any fixed voltage from +5V to +15V (pin 23) through a single 1kΩ resistor.

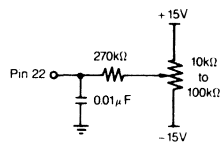
High resolution devices such as MN3290/91/92 present unique layout problems. Grounding and contact resistances become a matter of critical importance. A 16-bit converter with a 10V FSR has an LSB value of 150μV. Assuming a 5mA load, series wiring and contact resistance of only 30mΩ will throw the output off 1LSB. In terms of system layout, the impedance of #18 wire is approximately 0.064Ω/ft. Assuming 0 contact resistance, less than 6 inches of wire could produce a 1LSB error in the analog output. Careful layout and the use of external trim potentiometers for gain and offset adjusting can eliminate many potential sources of error.

OPTIONAL GAIN AND ZERO ADJUSTMENTS — MN3290 Series devices will operate as specified without external adjustment. If desired, however, gain and zero errors (either initial or at temperature) can be trimmed with external potentiometers. Adjustments should be made following warmup, and to avoid interaction, the zero adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors should be ±20% carbon composition or better and must be located as close as possible to the package to prevent noise pickup. A 0.01μF ceramic capacitor should be connected from gain adjust (pin 22) to ground.

ZERO ADJUSTMENT — Connect the zero potentiometer as shown for either current or voltage-output devices. For both unipolar and bipolar devices, zero adjusting is performed at the theoretical zero output. For example, for the MN3290-V (0 to +10V output), apply the input code of all "1's" and adjust the output for 0 volts. For the MN3292-I (±1mA output) apply a "0" and all "1's" and adjust for 0mA output. If it is not convenient to use a 3.9MΩ series resistor, the "T" network may be substituted.



GAIN ADJUSTMENT — Connect the gain potentiometer as shown for either current or voltage-output devices. Apply the digital input code that theoretically produces the maximum positive voltage, or maximum negative current, as appropriate (see Digital Input Coding). Adjust the potentiometer to achieve the desired output. Gain adjusting effectively rotates the device transfer function around zero.



REFERENCE OUTPUT — All MN3290/91/92 models contain an internal +6.3V ±5% voltage reference. The reference output (pin 24) may be used to drive an external load. The use of an external buffer is recommended if the anticipated source current will exceed 1.5mA or if the load is expected to vary while the D/A converter is in use. The reference output is short-circuit protected to ground.

OUTPUT COMPLIANCE VOLTAGE — Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified linearity and accuracy. MN3290/91/92-I is specified for a compliance voltage swing of ±2.5V, and an absolute maximum range of ±5V is permitted without damage to the device.

DRIVING A RESISTIVE LOAD WITH CURRENT-OUTPUT DEVICES — When using current-output devices to drive resistive loads, care should be taken not to exceed the compliance voltage limitation. This means that for MN3290X-I (0 to −2mA output), the effective load resistance must not exceed 1.25kΩ. For MN3291X-I and MN3292X-I (±1mA output), the effective load must not exceed 2.5kΩ.

When designing the resistive load, one should use MN3290/91/92's internal feedback resistor as often as possible. The feedback and output resistances of the DAC are implemented on the same thin-film network and will track each other, as well as the rest of the DAC, very closely. The bulk of the load resistance should be made with R_O and R_F whenever possible. See Figures 1 and 2. Paralleling R_F and R_O for the MN3290X-I produces an effective output resistance of 2.22k. Adding an external R_L of 1.82kΩ in parallel with R_F will yield an effective load of 1kΩ, producing an output voltage range of 0 to −2V.

For MN3292X-I, paralleling R_F and R_O produces an effective output impedance of 1.97kΩ. If one wishes to produce an output voltage of ±2V, an external 890Ω resistor must be put in series with R_F as shown in Figure 2.

Figure 1.

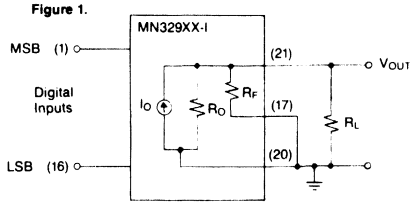


Figure 1. Driving an external resistive load in parallel with R_F.

Figure 2.

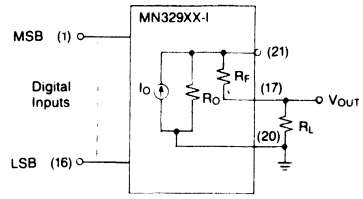


Figure 2. Driving an external resistive load in series with R_F.

Part Number	I_{OUT}	R_{OUT}	R_F	V_{OUT}
MN3290X-I	0 to −2mA	4kΩ	5kΩ	0 to +10V
MN3291X-I	±1mA	2.45kΩ	5kΩ	±5V
MN3292X-I	±1mA	2.45kΩ	10kΩ	±10V

DRIVING AN EXTERNAL OP AMP WITH CURRENT-OUTPUT DEVICES — Current-output models of MN3290/91/92 may be used to drive the summing junction of an output op amp in the traditional current-to-voltage configuration shown in Figure 3. Using the internal feedback resistors produces the same voltage ranges as the voltage-output devices and also maintains specified accuracy and drift.

Figure 3.

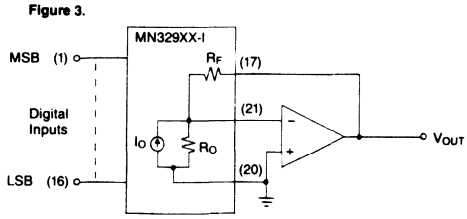


Figure 3. Driving an external op amp using the internal feedback resistor.

With the use of an external feedback resistor, the output may be scaled to any voltage; however it will be at the expense of increased gain drift. The thin-film resistors internal to MN3290/91/92 typically track each other to within ±1ppm/°C, but their absolute TCR may be as high as ±50ppm/°C. An alternative method of scaling the output voltage and preserving the low gain drift is shown in Figure 4.

For output voltages larger than ±10V, a high-voltage op amp may be employed with an external feedback resistor. Back-to-back protection diodes should be used at the summing junction to protect the DAC's output stage.

Figure 4.

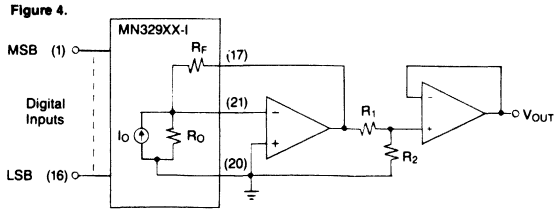


Figure 4. Using external op amps with internal and external feedback resistors to maintain low gain drift.

DIGITAL INPUT CODING

Digital Input MSB LSB	MN3290 0 to +10V	MN3290 0 to −2mA	MN3291 ±5V	MN3291 ±1mA	MN3292 ±10V	MN3292 ±1mA
0000 0000 0000 0000	+9.99985	−1.99997	+4.99985	−0.99997	+9.99969	−0.99997
0000 0000 0000 0001	+9.99969	−1.99994	+4.99969	−0.99994	+9.99939	−0.99994
0011 1111 1111 1111	+7.50000	−1.50000	+2.50000	−0.50000	+5.00000	−0.50000
0111 1111 1111 1111	+5.00000	−1.00000	0.00000	−0.00000	0.00000	0.00000
1000 0000 0000 0000	+4.99985	−0.99997	−0.00015	0.00003	−0.00031	+0.00003
1011 1111 1111 1111	+2.50000	−0.50000	−2.50000	+0.50000	−5.00000	+0.50000
1111 1111 1111 1110	+0.00015	−0.00003	−4.99985	+0.99997	−9.99969	+0.99997
1111 1111 1111 1111	0.00000	0.00000	−5.00000	+1.00000	−10.00000	+1.00000

CODING NOTES

1. For 10 Volts FSR, 1LSB for 16 bits=152.6μV. 1LSB for 14 bits=610.4μV.
2. For 20 Volts FSR, 1LSB for 16 bits=305.2μV. 1LSB for 14 bits=1.22mV.
3. For 2mA FSR, 1LSB for 16 bits=30.5μA. 1LSB for 14 bits=122.1μA.
4. For the unipolar voltage range, the coding is complementary straight binary. For bipolar voltage ranges, it is complementary offset binary.
5. For the unipolar current range, the coding is straight binary. For the bipolar current range, it is offset binary.

ORDERING INFORMATION

Part Number	Output Voltage Range	Output Current Range	Feedback Resistor	Specified Temperature Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	Guaranteed Monotonicity (2) +25°C	Guaranteed Monotonicity (2) Temp.
MN3290J-I	N.A.	0 to −2mA	5kΩ	0°C to +70°C	±0.006	±0.012	14	13
MN3290K-I	N.A.	0 to −2mA	5kΩ	0°C to +70°C	±0.003	±0.006	14	14
MN3290S-I	N.A.	0 to −2mA	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3290S/B-I(3)	N.A.	0 to −2mA	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3290T-I	N.A.	0 to −2mA	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3290T/B-I(3)	N.A.	0 to −2mA	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3290J-V	0 to +10V	N.A.	5kΩ	0°C to +70°C	±0.006	±0.012	14	13
MN3290K-V	0 to +10V	N.A.	5kΩ	0°C to +70°C	±0.003	±0.006	14	14
MN3290S-V	0 to +10V	N.A.	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3290S/B-V(3)	0 to +10V	N.A.	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3290T-V	0 to +10V	N.A.	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3290T/B-V(3)	0 to +10V	N.A.	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3291J-I	N.A.	±1mA	5kΩ	0°C to +70°C	±0.006	±0.012	14	13
MN3291K-I	N.A.	±1mA	5kΩ	0°C to +70°C	±0.003	±0.006	14	14
MN3291S-I	N.A.	±1mA	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3291S/B-I(3)	N.A.	±1mA	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3291T-I	N.A.	±1mA	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3291T/B-I(3)	N.A.	±1mA	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3291J-V	±5	N.A.	5kΩ	0°C to +70°C	±0.006	±0.012	14	13
MN3291K-V	±5	N.A.	5kΩ	0°C to +70°C	±0.003	±0.006	14	14
MN3291S-V	±5	N.A.	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3291S/B-V(3)	±5	N.A.	5kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3291T-V	±5	N.A.	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3291T/B-V(3)	±5	N.A.	5kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3292J-I	N.A.	±1mA	10kΩ	0°C to +70°C	±0.006	±0.012	14	13
MN3292K-I	N.A.	±1mA	10kΩ	0°C to +70°C	±0.003	±0.006	14	14
MN3292S-I	N.A.	±1mA	10kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3292S/B-I(3)	N.A.	±1mA	10kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3292T-I	N.A.	±1mA	10kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3292T/B-I(3)	N.A.	±1mA	10kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3292J-V	±10V	N.A.	10kΩ	0°C to +70°C	±0.006	±0.012	14	13
MN3292K-V	±10V	N.A.	10kΩ	0°C to +70°C	±0.003	±0.006	14	14
MN3292S-V	±10V	N.A.	10kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3292S/B-V(3)	±10V	N.A.	10kΩ	−55°C to +125°C	±0.006	±0.012	14	13
MN3292T-V	±10V	N.A.	10kΩ	−55°C to +125°C	±0.003	±0.006	14	14
MN3292T/B-V(3)	±10V	N.A.	10kΩ	−55°C to +125°C	±0.003	±0.006	14	14

1. Maximum error expressed in %FSR. ±0.003%FSR is equivalent to ±½LSB for 14 bits. ±0.006%FSR is equivalent to ±½LSB for 13 bits.
2. Minimum number of bits for which monotonicity is guaranteed over temperature.
3. Add "CH" to "S/B" or "T/B" models for 100% screening to MIL-H-38534.

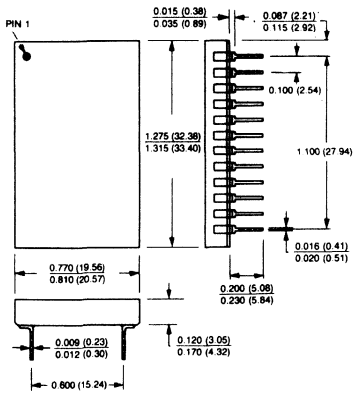
MICRO NETWORKS

MN3348

HIGH-ACCURACY
LOW-POWER
12-Bit D/A CONVERTER

FEATURES

- **Complete D/A Converter:**
  Internal Reference
  Internal Output Amplifier
- **Outstanding Accuracy:**
  ±0.05%FSR @ +25°C
  ±0.1%FSR −55°C +125°C
- **Low Power 375mW Max**
- **Small 24-Pin DIP**
- **Adjustment-free**
  No Gain and Offset
  Adjustment Necessary
- **Full Mil Operation**
  −55°C to +125°C
- **MIL-H-38534 Screening**
  Optional. MIL-STD-1772
  Qualified Facility



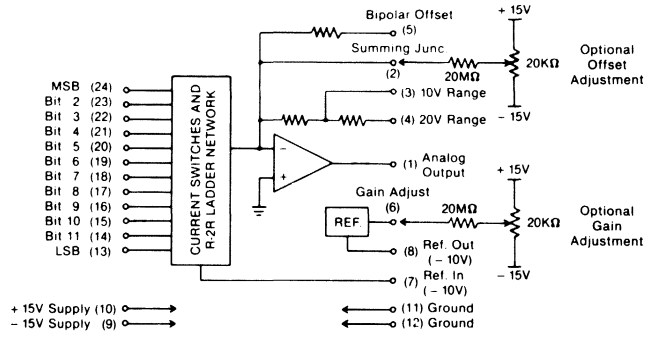
Dimensions in Inches (millimeters)

DESCRIPTION

MN3348 is a low-power 12-bit D/A that offers outstanding accuracies. The device is housed in an industry-standard, hermetically sealed, 24-pin dual-in-line package and features performance specifications guaranteed over either the 0°C to +70°C or −55°C to +125°C ("H" Model) operating temperature range. Overall unadjusted absolute accuracy is guaranteed to be better than ±0.05%FSR at room temperature and better than ±0.1%FSR from −55°C to +125°C. Power consumption is a low 375mW maximum. Other features include 5 user-selectable output ranges, 8μsec maximum settling time and guaranteed monotonicity. For military/aerospace or harsh-environment commercial/industrial applications, MN3348H/B CH is fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

MN3348 was designed for high-accuracy applications in which power and space are at a premium. Hermetic packaging, MIL-H-38534 processing and performance specs guaranteed from −55°C to +125°C make it an excellent choice for military/aerospace and avionics applications.

BLOCK DIAGRAM



MN3348

May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN3348 HIGH-ACCURACY LOW-POWER 12-Bit D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Positive Supply (Pin 10)	+18 Volts
Negative Supply (Pin 9)	−18 Volts
Digital Inputs (Pins 13-24)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN3348H/B CH

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V unless otherwise specified).

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	3.5			Volts
Logic "0"			1.5	Volts
Logic Coding: Unipolar Ranges	Complementary Binary			
Bipolar Ranges	Complementary Offset Binary			
Input Current		±10		pA
ANALOG OUTPUT				
Unipolar Output Ranges	0 to −5, 0 to −10			Volts
Bipolar Output Ranges	±2.5, ±5, ±10			Volts
Output Impedance		0.1		Ω
Output Load Current	±5	±10		mA
TRANSFER CHARACTERISTICS				
Linearity Error (Note 1):				
+25°C		±0.005	±0.012	%FSR
0°C to +70°C		±0.012	±0.024	%FSR
−55°C to +125°C ("H" Models)		±0.024	±0.048	%FSR
Differential Linearity			±1	LSB
Monotonicity	Guaranteed			
Absolute Accuracy Error (Notes 1, 2):				
+25°C		±0.025	±0.05	%FSR
0°C to +70°C		±0.04	±0.075	%FSR
−55°C to +125°C ("H" Models)		±0.05	±0.1	%FSR
DYNAMIC CHARACTERISTICS				
Settling time (20V Step to ± ½ LSB)		6	8	μSec
Output Slew Rate		10		V/μSec
REFERENCE (Note 3)				
Internal		−10		Volts
External		−10		Volts
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply	+9.00	+15.00	+18.00	Volts
−15V Supply	−13.00	−15.00	−18.00	Volts
Current Drain, Output				
Unloaded: +15V Supply		5	10	mA
−15V Supply		−8	−15	mA
Power Supply Rejection		±0.001	±0.005	%FSR/%Vs
Power Consumption		195	375	mW

SPECIFICATION NOTES:

1. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected output range. For the 0 to −5V and ±2.5V ranges, FSR = 5V. For the 0 to −10V and ±5V ranges, FSR = 10V. For the ±10 range, FSR = 20V. 1 LSB for a 12 bit converter = 0.024%FSR.
2. Absolute Accuracy Error includes gain, offset, linearity, and all other errors and is specified without adjustment. The specification applies over the converter's entire output range. Absolute Accuracy can be improved with optional gain and offset adjustments. (See below).
3. For the specified performance Pin 8 (Ref. Out) must be connected to Pin 7 (Ref. In). Any additional loading of the reference must not exceed 1 mA. If an external reference is used, its voltage must be −10.000V and it must be able to supply 1 mA.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

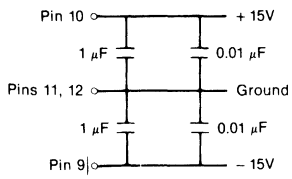
Connect the Offset and Gain Adjust potentiometers as shown in the block diagram.

UNIPOLAR RANGES—Apply a digital input of all "0's" and adjust the OFFSET potentiometer for 0V out. Apply all "1's" and adjust the GAIN potentiometer for the output value shown in the table.

BIPOLAR RANGES—Apply a digital input of all "0's" and adjust the OFFSET potentiometer for the minus full scale output. Apply all "1's" and adjust the GAIN potentiometer for the output value shown in the table.

POWER SUPPLY DECOUPLING

Power supplies should be decoupled with 1 μF capacitors paralleled with 0.01 μF ceramic capacitors as shown below.



DIGITAL INPUT CODING

DIGITAL INPUT MSB LSB	ANALOG OUTPUT 0 to −5V	0 to −10V	±2.5V	±5V	±10V
1111 1111 1111	−4.9988	−9.9976	−2.4988	−4.9976	−9.9951
1111 1111 1110	−4.9976	−9.9951	−2.4976	−4.9951	−9.9902
1000 0000 0001	−2.5012	−5.0024	−0.0012	−0.0024	−0.0049
1000 0000 0000	−2.5000	−5.0000	0.0000	0.0000	0.0000
0111 1111 1111	−2.4988	−4.9976	+0.0012	+0.0024	+0.0049
0000 0000 0001	−0.0012	−0.0024	+2.4988	+4.9976	+9.9951
0000 0000 0000	0.0000	0.0000	+2.5000	+5.0000	+10.0000
Connect Pin to Pin	8 to 7 5 to 11 1 to 3 2 to 4	8 to 7 5 to 11 1 to 3	8 to 7 5 to 7 1 to 3 2 to 4	8 to 7 5 to 7 1 to 3	8 to 7 5 to 7 1 to 4

MICRO NETWORKS

MN3349

LOW-POWER, 12-Bit
D/A CONVERTER

FEATURES

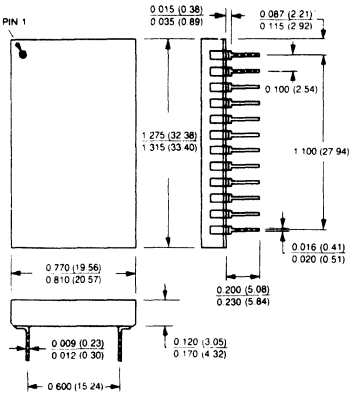
- DAC349 Pin Compatible
- Complete D/A Converter:
  Internal Reference
  Internal Output Amplifier
- Low Power 375mW Max
- Small 24-Pin DIP
- 5 User-Selectable Output Ranges
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

DESCRIPTION

MN3349 is a low-power 12-bit D/A converter. It is an exact pin-for-pin replacement for the DAC349, offering superior performance and fully guaranteed specifications. Each unit is complete with internal reference and output amplifier and is housed in an industry-standard, 24-pin dual-in-line package. Operating temperature range is −55°C to +125°C, and all key performance specifications are given as maximums and guaranteed. Features include 5 user-selectable output ranges, 10μsec maximum settling time and 375mW maximum power consumption. For military/aerospace or harsh-environment commercial/industrial applications, MN3349H/B CH fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

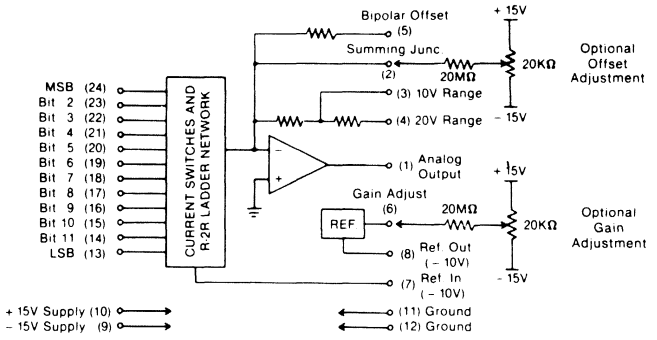
MN3349 was designed for requirements in which power, speed, size and temperature considerations are paramount. Maximum specifications minimize design and purchasing time and ensure field interchangeability without the need for recalibration.

24 PIN DIP



Dimensions in Inches (millimeters)

BLOCK DIAGRAM



MN3349

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MN3349 LOW-POWER 12-Bit D/A CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Positive Supply (Pin 10)	+18 Volts
Negative Supply (Pin 9)	−18 Volts
Digital Inputs (Pins 13-24)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN3349H/B CH

- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified −55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Streening.
- Add "CH" to "H/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V unless otherwise specified).

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1" Logic "0"	3.5		 1.5	Volts Volts
Logic Coding: Unipolar Ranges Bipolar Ranges	Complementary Binary Complementary Offset Binary			
Input Current		±10		pA
ANALOG OUTPUT				
Unipolar Output Ranges Bipolar Output Ranges	0 to −5, 0 to −10 ±2.5, ±5, ±10			Volts Volts
Output Impedance Output Load Current	 ±5	0.1 ±10		Ω mA
TRANSFER CHARACTERISTICS				
Linearity Error Differential Linearity			±½ ±1	LSB LSB
Monotonicity	Guaranteed			
Scale Factor, Gain Error (Note 1) Unipolar Offset Error (Notes 1, 2) Bipolar Offset Error (Notes 1, 2)		±0.05 ±0.05 ±0.05	±0.1 ±0.2 ±0.1	% %FSR %FSR
DYNAMIC CHARACTERISTICS				
Settling time (20V Step to ±½ LSB) Output Slew Rate		8 10	10	μSec V/μSec
DRIFT CHARACTERISTICS				
Accuracy Drift (Note 3) Linearity Drift Differential Linearity Drift			±30 ±5 ±2	ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C
REFERENCE (Note 4)				
Internal External		−10 −10		Volts Volts
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V Supply −15V Supply	+9.00 −13.00	+15.00 −15.00	+18.00 −18.00	Volts Volts
Current Drain, Output Unloaded: +15V Supply −15V Supply		5 −8	10 −15	mA mA
Power Supply Rejection		±0.001	±0.005	%FSR/%Vs
Power Consumption		195	375	mW

SPECIFICATION NOTES:

1. Initial Offset and Gain Errors are externally adjustable (see below).
2. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected output range. For the 0 to −5V and ±2.5V ranges, FSR = 5V. For the 0 to −10V and ±5V ranges, FSR = 10V. For the ±10 range, FSR = 20V. 1 LSB for a 12 bit converter = 0.024%FSR.
3. Total effect of linearity, offset, and gain drift on overall converter accuracy.
4. For the specified performance Pin 8 (Ref. Out) must be connected to Pin 7 (Ref. In). Any additional loading of the reference must not exceed 1 mA. If an external reference is used, its voltage must be −10.000V and it must be able to supply 1 mA.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

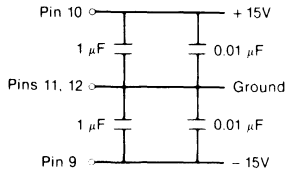
Connect the Offset and Gain Adjust potentiometers as shown in the block diagram.

UNIPOLAR RANGES—Apply a digital input of all "0's" and adjust the OFFSET potentiometer for 0V out. Apply all "1's" and adjust the GAIN potentiometer for the output value shown in the table.

BIPOLAR RANGES—Apply a digital input of all "0's" and adjust the OFFSET potentiometer for the minus full scale output. Apply all "1's" and adjust the GAIN potentiometer for the output value shown in the table.

POWER SUPPLY DECOUPLING

Power supplies should be decoupled with 1 μF capacitors paralleled with 0.01 μF ceramic capacitors as shown below.



DIGITAL INPUT CODING

DIGITAL INPUT MSB LSB	0 to −5V	0 to −10V	±2.5V	±5V	±10V
1111 1111 1111	−4.9988	−9.9976	−2.4988	−4.9976	−9.9951
1111 1111 1110	−4.9976	−9.9951	−2.4976	−4.9951	−9.9902
1000 0000 0001	−2.5012	−5.0024	−0.0012	−0.0024	−0.0049
1000 0000 0000	−2.5000	−5.0000	0.0000	0.0000	0.0000
0111 1111 1111	−2.4988	−4.9976	+0.0012	+0.0024	+0.0049
0000 0000 0001	−0.0012	−0.0024	+2.4988	+4.9976	+9.9951
0000 0000 0000	0.0000	0.0000	+2.5000	+5.0000	+10.0000
Connect Pin to Pin	8 to 7 5 to 11 1 to 3 2 to 4	8 to 7 5 to 11 1 to 3	8 to 7 5 to 7 1 to 3 2 to 4	8 to 7 5 to 7 1 to 3	8 to 7 5 to 7 1 to 4

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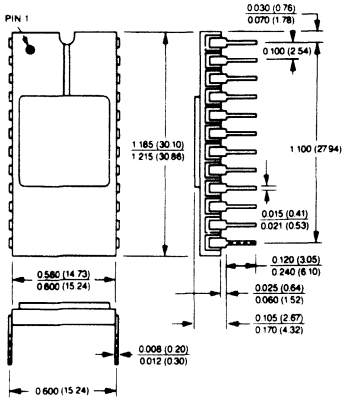
MN3850

INDUSTRY-STANDARD
MILITARY, 12-Bit
D/A CONVERTERS

FEATURES

- **Fully Guaranteed −55°C to +125°C operation**
- **Linearity and Monotonicity Guaranteed Over Temperature**
- **4μsec Settling Time**
- **Small 24-Pin Hermetic DIP**
- **No +5V Supply Required**
- **480mW Maximum Power Consumption**
- **Pin-Compatible DAC85-CBI-V, AD DAC87**
- **MIL-STD-1772 Qualified Facility**

24 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN3850 is a high-performance, TTL-compatible, 12-bit digital-to-analog converter in a 24-pin, hermetically sealed ceramic dual-in-line package. The MN3850 is a monolithic voltage-output D/A complete with an internal reference and fast-settling output amplifier. It is pin-for-pin compatible with industry standard "3850" devices as well as many DAC87 and DAC85/80 D/A converters. The MN3850 guarantees a 4μsec output settling time (20V step settling to ±0.5LSB). Other critical accuracy performance parameters are fully specified and guaranteed over the entire operating temperature range. Linearity and monotonicity are guaranteed over temperature, and full scale absolute accuracy error is specified as ±0.3% FSR maximum over temperature.

The Micro Networks MN3850 has 5 user-selectable output ranges, a fully short-circuit protected output, and a maximum power consumption of 480mW. The MN3850's rugged ceramic package is hermetically sealed, and for military/aerospace applications, MN3850H/B is available with Environmental Stress Screening.

The MN3850 was designed for military/aerospace, industrial and OEM applications in which high-speed D/A conversion in severe, wide-temperature-range environment is required. The MN3850 12-bit D/A converter has become the industry standard for military/aerospace and demanding industrial applications. The MN3850's monolithic design results in improved reliability. Guaranteed monotonicity over temperature makes the MN3850 an excellent choice for military and aerospace control systems.

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MN3850 INDUSTRY-STANDARD MILITARY 12-Bit D/A CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN3850	0°C to +70°C
MN3850H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 22)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 14)	+0.5 to −18 Volts
Digital Inputs (Pins 1-12)	−0.5 to +18 Volts
Output Current	(Note 1)

ORDERING INFORMATION

PART NUMBER ——— **MN3850H/B**

Standard device is specified for 0°C to 70°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" suffix to "H" models for Environmental Stress Screening.

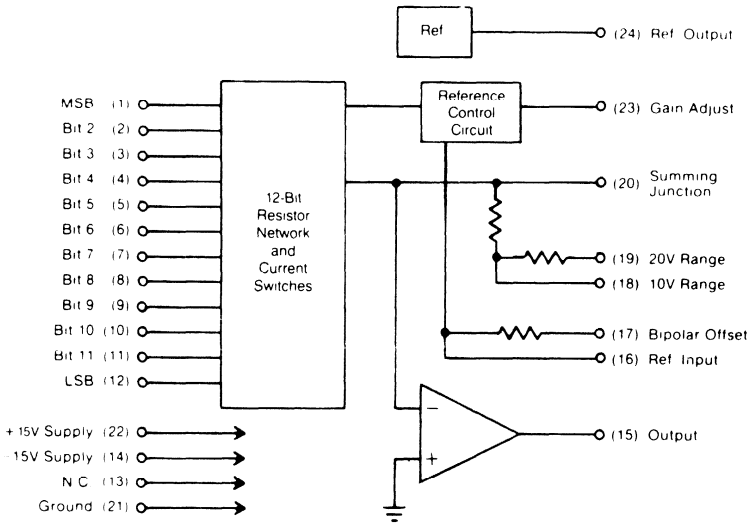
SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated) (Note 2)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Input Currents: Logic "1" (V_{IH} = +2.4V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−180	μA
Logic Coding: Unipolar Output Ranges	Complementary Straight Binary			
Bipolar Output Ranges	Complementary Offset Binary			
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar	0 to +5, 0 to +10			Volts
Bipolar	±2.5, ±5, ±10			Volts
Output Impedance (Note 9)		0.05	0.20	Ω
Output Current (Notes 1, 9)	±5			mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		± ¼	± ½	LSB
Over Temperature (Note 4)			± ½	LSB
Differential Linearity Error		± ½		LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Note 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 4)		±0.15	±0.3	%FSR
Zero Error (Notes 6, 7): Initial (+25°C)		±0.02	±0.05	%FSR
Over Temperature (Note 4)		±0.05	±0.1	%FSR
Gain Error (Notes 6, 8): Initial (+25°C)		±0.1		%
Drift		±10		ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ±0.01%FSR: 20V Step		3	4	μsec
10V Step		2	3	μsec
Slew Rate (Note 9)		±12		V/μsec
INTERNAL REFERENCE				
Internal Reference (Note 9): Voltage		+6.3		Volts
Accuracy		±5		%
Drift		±10		ppm/°C
External Current			2.5	mA
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
Power Supply Rejection: +15V Supply		±0.02	±0.04	%FSR/%Supply
−15V Supply		±0.002	±0.004	%FSR/%Supply
Current Drains: +15V Supply		+8	+12	mA
−15V Supply		−15	−20	mA
Power Consumption		345	480	mW

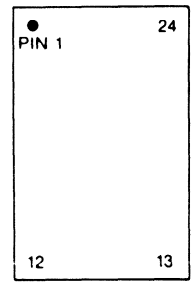
SPECIFICATIONS

1 The MN3850 is short-circuit protected to ground or either supply.
2 Unless otherwise indicated, listed specifications apply for all MN3850 models.
3 FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ± 10V output range, FSR is 20 Volts, and 1 LSB is ideally equal to 4.88mV. For the 0 to +10V and ± 5V ranges, FSR is 10 Volts, and 1 LSB is ideally equal to 2.44mV. For the 0 to +5V and ± 2.5V ranges, FSR is 5 Volts, and 1 LSB is ideally equal to 1.22mV.
4 MN3850 is specified for 0°C to +70°C operation. MN3850H and MN3850H/B are specified for −55°C to +125°C operation.
5 This specification applies to both unipolar and bipolar output ranges and is specified without adjustment. With optional gain and offset adjustment, initial accuracy error can be reduced to ± 0.012%FSR(± ½LSB).
6 Initial offset and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
7 Zero error is defined as the difference between the actual and the ideal output voltage when configured in a unipolar output range with a digital input of 1111 1111 1111. Additionally, for bipolar ranges, zero error is also defined as the difference between the actual and the ideal output when configured in a bipolar output range with a digital input of 0111 1111 1111.
8 Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage span from the 1111 1111 1111 output to the 0000 0000 0000 output.
9 These parameters are listed for reference only and are not tested.

BLOCK DIAGRAM



PIN DESIGNATIONS



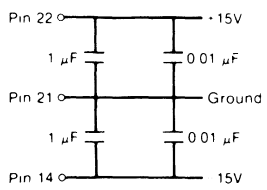
1	Bit 1 (MSB)	24	Reference Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply (+Vcc)
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	20V Range
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Reference Input
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply (−Vcc)
12	Bit 12 (LSB)	13	N C.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and bypassing is necessary to obtain specified accuracies from the MN3850. The unit's ground pin (pin 21) should be tied to system analog ground as close to the package as possible, preferably to a large analog ground plane beneath the package. Coupling between analog and digital signals should be minimized to avoid noise pickup. A short jumper should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16). Pin 20, the line to the Summing Junction of the output amplifier, is particularly noise susceptible. Care should be taken to avoid long runs or runs parallel to digital lines when tying to this pin for output range selection. If optional external offset and gain adjusting is used, the series resistors should be located as close to the package as possible, and short conductor runs should be used.

For optimum performance and noise rejection, power supplies should be bypassed with capacitors located as close to the unit as possible. We have found 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors to be a cost-effective combination. Single 1μF ceramic capacitors can be used to save space.

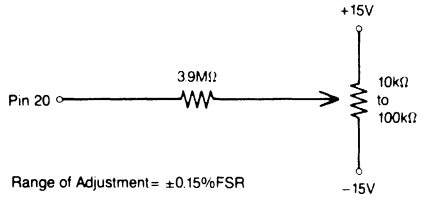
POWER SUPPLY BYPASSING



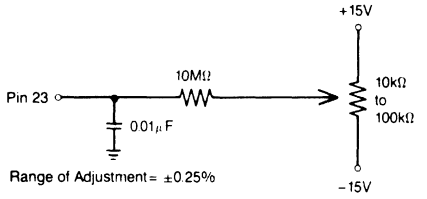
REFERENCE OUTPUT—The MN3850 contains an internal +6.3V ±5% voltage reference, and units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, the load current should not exceed 2.5mA.

OPTIONAL OFFSET AND GAIN ADJUSTMENTS—The MN3850 will operate as specified without additional adjustments. If desired, input/output accuracy error can be reduced to ±½LSB (±0.012%FSR) by following the trimming procedures described below. Adjustments should be made following warmup, and to avoid interaction, offset must be adjusted before gain. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be connected to ground.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown below and apply the digital input 1111 1111 1111. Adjust the offset potentiometer until the output is exactly zero volts for unipolar ranges and minus full scale for bipolar ranges. See Input Logic Coding.



GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply a 0000 0000 0000 digital input. Adjust the gain potentiometer until the output voltage is at its ideal positive full scale value (+F.S.−1 LSB, see Input Logic Coding).



OUTPUT RANGE SELECTION

Pin Connections	Output Range				
	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect Pin 24 to	16	16	16	16	16
Connect Pin 17 to	21	21	20	20	20
Connect Pin 15 to	18	18	18	18	19
Connect Pin 19 to	20	N.C.	20	N.C.	15
Connect Pin 20 to	19	N.C.	19,17	17	17

INPUT LOGIC CODING

Digital Input	Analog Output				
MSB LSB	0 to +5V	0 to +10V	±2.5V	±5V	±10V
0000 0000 0000	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
0000 0000 0001	+4.9976V	+9.9951V	+2.4976V	+4.9951V	+9.9902V
0111 1111 1111	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
1000 0000 0000	+2.4988V	+4.9976V	−0.0012V	−0.0024V	−0.0049V
1111 1111 1110	+0.0012V	+0.0024V	−2.4988V	−4.9976V	−9.9951V
1111 1111 1111	0.0000V	0.0000V	−2.5000V	−5.0000V	−10.0000V

CODING NOTES

1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR=20V, 1 LSB=4.88mV.
4. For FSR=10V, 1 LSB=2.44mV.
5. For FSR=5V, 1 LSB=1.22mV.

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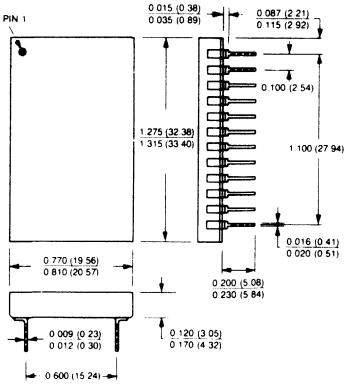
MN3860

12-Bit
D/A CONVERTER
with INPUT REGISTER

FEATURES

- **Complete With Internal:**
  Input Register
  Output Op Amp
  Low-Drift Reference
- **±1/2LSB Linearity and Monotonicity Guaranteed Over Temperature**
- **40nsec Data Setup Time**
- **±0.1% FSR Unadjusted Absolute Accuracy**
- **7μsec Max Settling Time (20V step to ±1/2LSB)**
- **Small 24-Pin Side-Brazed DIP**
- **Full MIL Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

The MN3860 is a 12-bit digital-to-analog converter with a fast, internal, TTL input register. It is packaged in a hermetically sealed, ceramic, 24-pin dual-in-line package and is complete with internal reference and output amplifier. Three user selectable output ranges are available (0 to +10V, ±5V and ±10V), and performance features include the following: fast output settling (7μsec for a 20V change), ±0.1%FSR maximum absolute accuracy, and ±½LSB linearity and monotonicity guaranteed over the full operating temperature range. Maximum power consumption is 730mW.

The MN3860 is functionally laser trimmed for linearity, gain and offset, eliminating the need for external potentiometers. Units are available for two operating temperature ranges (0°C to +70°C and −55°C to +125°C). Linearity and accuracy are tested 100% and guaranteed both at room and temperature extremes. For military/aerospace or harsh-environment commercial/industrial application, "H/B CH" models are fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

The MN3860 is TTL compatible, and its internal input register facilitates interfacing to microprocessor and minicomputer data buses. Applications include microprocessor-based data-distribution systems, programmable power supplies and servo drivers. Optional MIL-H-38534 processing and guaranteed linearity and accuracy specifications over the −55°C to +125°C temperature range make the MN3860 an excellent choice for military avionics and fire control systems.

Model Number	Temperature Range	Input Coding	Max.Power Consumption
MN3860	0°C to +70°C	CSB/COB	730mW
MN3860H	−55°C to +125°C	CSB/COB	730mW
MN3860H/B	−55°C to +125°C	CSB/COB	730mW
MN3860H/BCH	−55°C to +125°C	CSB/COB	730mW

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MN3860 12-Bit D/A CONVERTER with INPUT REGISTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN3860	0°C to +70°C
MN3860H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 22)	0 to +18 Volts
Negative Supply (−Vcc, Pin 14)	0 to −18 Volts
Logic Supply (+Vdd, Pin 13)	−0.5 to +7 Volts
Register Enable (Pin 19)	−0.5 to +5.5 Volts
Digital Inputs (Pins 1-12)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER—MN3860H/B CH

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

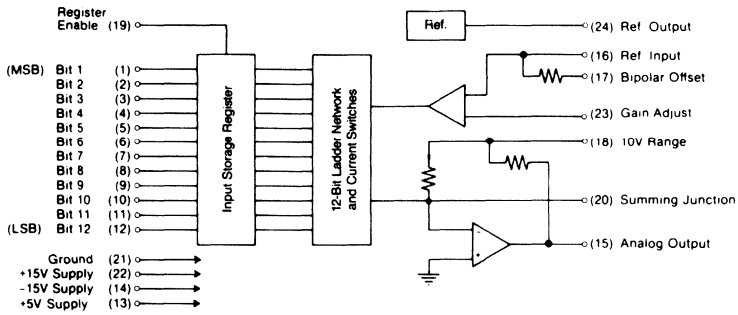
SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V +Vdd = +5V unless otherwise indicated) (Note 1)

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.7	Volts
Input Currents: Data Inputs: Logic "1" (V_{IH} = +2.4V)			+30	μA
Logic "0" (V_{IL} = +0.4V)			−0.6	mA
Register Enable: Logic "1" (V_{IH} = +2.4V)			+60	μA
Logic "0" (V_{IL} = +0.4V)			−1.2	mA
Register Enable (Note 2): Pulse Width	60			nsec
Setup Time Digital Data to Enable	40			nsec
Logic Coding: Unipolar Range	Complementary Straight Binary			
Bipolar Ranges	Complementary Offset Binary			
ANALOG OUTPUT				
Output Voltage Ranges: Unipolar		0 to +10		Volts
Bipolar		±5, ±10		Volts
Output Impedance		0.5		Ω
Output Current	±4	±5		mA
TRANSFER CHARACTERISTICS (Note 3)				
Linearity Error: Initial (+25°C)		±¼	±½	LSB
Over Temperature (Note 8)			±½	LSB
Monotonicity	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Notes 4, 5): Initial (+25°C)		±0.05	±0.1	%FSR
Over Temperature (Note 8)		±0.15	±0.3	%FSR
Zero Error (Notes 4, 6): Initial (+25°C)		±0.025	±0.05	%FSR
Over Temperature (Note 8)		±0.05	±0.1	%FSR
Gain Error (Notes 4, 7)		±0.1		%
Gain Drift		±10		ppm/°C
DYNAMIC CHARACTERISTICS				
Settling Time to ±0.01% for 20V Step		5	7	μsec
Output Slew Rate		±20		V/μsec
REFERENCE OUTPUT				
Internal Reference: Voltage		+6.3		Volts
Accuracy		±2		%
Tempco		±10		ppm/°C
External Current			2.5	mA
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
+5V Supply	+4.75	+5.00	+5.25	Volts
Power Supply Rejection: +15V Supply		±0.01	±0.04	%FSR/%Supply
−15V Supply		±0.001	±0.004	%FSR/%Supply
Current Drain: +15V Supply		+8	+12	mA
−15V Supply		−15	−20	mA
+5V Supply		+30	+50	mA
Power Consumption		495	730	mW

SPECIFICATIONS

1. Unless otherwise indicated, listed specifications apply for all MN3860 models.
2. The analog output will follow its digital input when Register Enable is a logic "0". Digital input data will be latched and analog output voltage constant when Register Enable is logic "1". The minimum Register Enable pulse width to latch new digital input data is 60nsec. See Timing Diagram.
3. FSR stands for full scale range and is equal to the peak-to-peak voltage of the selected output range. For the ±10V output range, FSR is 20 Volts, and 1LSB is ideally equal to 4.88mV. For the 0 to +10V and ±5V ranges, FSR is 10 Volts, and 1LSB is ideally equal to 2.44mV.
4. Initial zero and gain errors are adjustable to zero with user-optional, external trimming potentiometers.
5. Full Scale Absolute Accuracy Error includes offset, gain, linearity, noise, and all other errors and is specified without adjustment. For unipolar output ranges, Full Scale Absolute Accuracy Error refers to the deviation between the actual and the ideal output with an all "0's" digital input applied. For bipolar output ranges, the spec. refers to the deviation between the actual and the ideal output with either all "0's" (positive full scale) or all "1's" (negative full scale) applied.
6. Zero error is defined as the difference between the actual and the ideal output voltage for the input code which ideally produces 0 Volts out. For the 0 to +10V range, zero error is measured with a digital input of 11111 1111 1111. For ±5V and ±10V ranges, zero error is measured with a digital input of 0111 1111 1111.
7. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output span from the 1111 1111 1111 output to the 0000 0000 0000 output.
8. Listed specifications apply over the 0°C to +70°C temperature range for standard products, and over the −55°C to +125°C range for "H" products.

BLOCK DIAGRAM



PIN DESIGNATIONS

1	Bit 1 (MSB)	24	Ref. Out (+6.3V)
2	Bit 2	23	Gain Adjust
3	Bit 3	22	+15V Supply
4	Bit 4	21	Ground
5	Bit 5	20	Summing Junction
6	Bit 6	19	Register Enable
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	Ref. In
10	Bit 10	15	Analog Output
11	Bit 11	14	−15V Supply
12	Bit 12 (LSB)	13	+5V Supply

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN3860. The units' Ground (pin 21) must be tied to circuit analog ground as close to the package as possible, preferably through a large ground plane underneath the package.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the unit. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used.

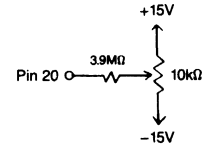
Coupling between analog and digital signals should be minimized to avoid noise pickup. Short jumpers should be used when tying the Reference Output (pin 24) to the Reference Input (pin 16) and when tying the Bipolar Offset (pin 17) to the Summing Junction (pin 20) for bipolar operation. If external gain and offset adjustments are to be used, the series resistors should be located as close to the unit as possible.

REFERENCE OUTPUT—The MN3860 contains an internal +6.3V ±2% voltage reference, and the units are actively laser trimmed to operate from this reference. Therefore, though the user has the option of using an external reference, for specified operation, the Reference Output (pin 24) must be connected to the Reference Input (pin 16). If the internal reference is used to drive an external load, it should be buffered if the load current will exceed 2.5mA.

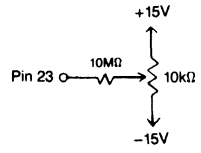
OPTIONAL GAIN AND OFFSET ADJUSTMENTS—The MN3860 will operate as specified without external adjustments. If desired, however, absolute accuracy error can be reduced to ±1LSB by following the trimming procedure described below. Adjustments should be made following warmup and, to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 23 should not be grounded.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for the unipolar output ranges or minus full scale for bipolar output ranges.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the Coding table.



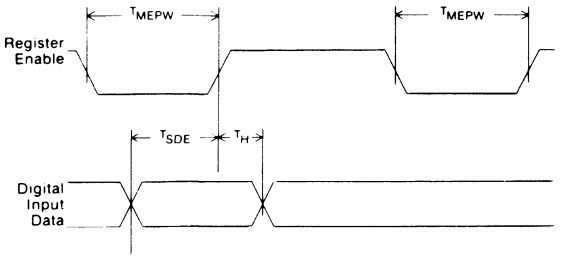
OFFSET ADJUST



GAIN ADJUST

REGISTER ENABLE—When the Register Enable (pin 19) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60nsec and digital input data must be valid for a minimum of 40nsec prior to Register Enable going high again. See Timing Diagram.

INPUT REGISTER TIMING DIAGRAM



TIMING NOTES:

T_{MEPW} Minimum Enable Pulse Width is 60nsec.
T_{SDE} Minimum Setup Time Digital Data to Enable is 40nsec.
T_H Digital Data Hold Time from Register Enable is 0nsec.

OUTPUT RANGE SELECTION

Pin Connections	Analog Output		
Output Range	**0 to +10V**	**±5V**	**±10V**
Connect Pin 24 to	16	16	16
Connect Pin 17 to Connect Pin 15 to	21 18	20 18	20 N.C.
Connect Pin 20 to	N.C.	17	17

INPUT LOGIC CODING

Digital Input		Analog Output		
MSB	**LSB**	**0 to +10V**	**±5V**	**±10V**
0000 0000 0000		+9.9976V	+4.9976V	+9.9951V
0000 0000 0001		+9.9951V	+4.9951V	+9.9902V
0111 1111 1111		+5.0000V	0.0000V	0.0000V
1000 0000 0000		+4.9976V	−0.0024V	−0.0049V
1111 1111 1110		+0.0024V	−4.9976V	−9.9951V
1111 1111 1111		0.0000V	−5.0000V	−10.0000V

CODING NOTES:

1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR=20V, 1LSB=4.88mV.
4. For FSR=10V, 1LSB=2.44mV.

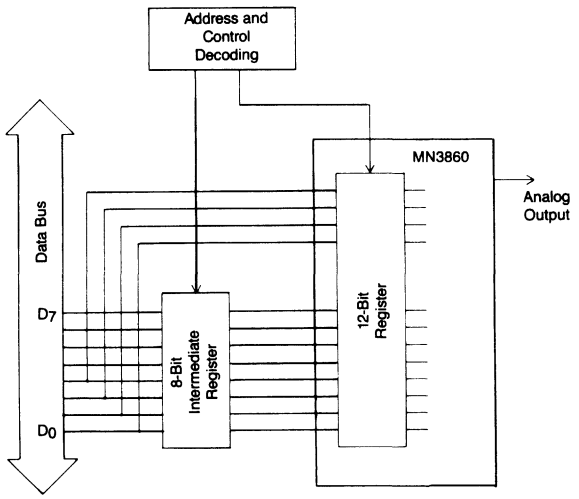
MICROPROCESSOR INTERFACING

Interfacing the MN3860 to 8, 12 and 16-bit microprocessors is simplified by the MN3860's internal 12-bit register. External address and control decoding will be required, however.

Interfacing to 12 and 10-bit processors is fairly direct and can usually be accomplished by NANDing the desired address lines with the processor's MEMORY WRITE or I/O WRITE line and using the output to drive the MN3860's Register Enable input. For most processors, valid data remains on the data bus for a period of time after the removal of either valid address or control signals. This results in data being latched into the MN3860 immediately after one of the address or control signals changes but before valid data goes away.

Interfacing to 8-bit processors is slightly more complicated and an 8-bit external register is needed as shown in the sketch below.

Address decoding must be organized such that the 8-bit intermediate register and the MN3860's internal 12-bit register appear at two different addresses. The 12 bits of digital data are sent to the MN3860 via two data transfers. First, the 8 least significant bits of digital data are written to the intermediate latch. Then, the 4 most significant bits of digital data are written to the MN3860's 12-bit latch. The result is that the 4 MSB's on the data bus and the 8 LSB's held in the intermediate latch are all latched into the MN3860's latch simultaneously. This technique is called double buffering and it avoids the analog output slewing to an undesirable state determined by the LSB's of the new digital data and the MSB's of the previous digital data.



MICRO NETWORKS
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Track-Hold and Gain Amplifiers

Track-Hold and Gain Amplifiers

Micro Networks offers a complete line of Track-Hold (T/H) amplifiers for application in low-resolution (7-9 Bit applications), medium-resolution (12-Bit applications) and high-resolution (14-16 Bit applications) systems. For example, the MN379 is a low-resolution, ultra-high speed device suitable for use with flash A/D converters; the MN376 is well suited for moderately high-speed 12-bit systems; and the MN373 and MN374 are designed for application in 14 to 16-bit systems.

Track-hold (sample-hold) amplifiers are most frequently used in conjunction with A/D converters to track (capture) rapidly changing analog signals and hold them constant while the converter is performing a conversion. If the analog input of a successive approximation or subranging A/D converter changes more than ± ½LSB during the conversion interval, significant errors may result. This means, for example, that a high-speed 12-bit A/D such as MN5245 (850nsec conversion time) can only accurately digitize signals slower than 40Hz (5V peak-to-peak) while maintaining acceptable error. The same converter used in conjunction with an MN376 T/H amplifier (200nsec acquisition time, 40psec aperture jitter) can accurately digitize a 1MHz signal.

While speed (acquisition time) is oftentimes the first criterion used in selecting a T/H amplifier, it is important to remember that T/H input/output linearity must be consistent with A/D converter and system linearity requirements. A very high-speed T/H amplifier that specifies ± 0.05% linearity (the equivalent of 10-bit linearity) should not be selected for use in a 12-bit system (± 0.01%). Similarly, speed parameters like acquisition and track-to-hold settling times should be specified to ± 0.05% accuracy for 10-bit applications or to ± 0.01% accuracy for 12-bit applications. The selection guides on the following page have been organized in a fashion that first groups products by linearity or "resolution" and then lists individual products in order of decreasing speed.

In addition to T/H amplifiers, Micro Networks offers designers two gain amplifiers. The MN2020 is a digitally programmable gain amplifier with gains of 1, 2, 4, 8, 16, 32, 64 and 128. The MN2200 is an instrumentation amplifier featuring internal gain ranges of 1, 10, 100 and 1000.

MN4000

High-Speed
12-Bit Linear
T/H Amplifier

FEATURES

- 40nsec Signal Acquisition (1V Step to ± 0.1%)
- ± 0.02% FSR Maximum Gain Nonlinearity Error
- Low 30mVp-p T/H Transient
- 50MHz Small Signal Bandwidth
- Functionally Compatible with "-0010/0025" Devices
- DESC SMD 5962-90856 Listed
- Full Mil Operation -55°C to +125°C

MN379

Flash-Converter
Compatible
T/H Amplifier

FEATURES

- Designed to Directly Drive Flash Converters
- 2psec Maximum Aperture Jitter
- Capative Loads to 500pF
- 30nsec Max Acquisition Time (1V Step to ± 0.1%)
- 15nsec Max Settling Time
- ± 300V/μsec Min Slew Rate
- 100MHz Bandwidth
- TTL or ECL Compatible
- 24-Pin DIP
- Full Mil Operation -55°C to +125°C

MN374

High-Speed
High-Resolution
Track-Hold Amplifier

FEATURES

- 4μsec Max Acquisition Time (20V Step to ± 0.003%)
- Compatible with All DIP Packaged 14-16 Bit A/D's
- 400psec Aperture Jitter
- ± 1μV/μsec Max Droop Rate
- 90dB Min Feedthrough Attenuation
- Small 14-Pin DIP
- Pin and Function Compatible with SHC76
- Full Mil Operation -55°C to +125°C

Track-Hold Amplifiers

Application	Maximum Linearity Error (%)	Acquisition Time	Gain and Voltage Range	Model	Specified Temp Range (°C)	Aperture Jitter (psec)	Droop Rate (μV/μs)	Power (mW)	DIP Package	Hi-Rel Option	DESC SMD (5962-)	Page No.
7-9 Bits	±0.1	35nsec 5V Step to ±0.1%	+1, ±2.5V	MN379	0 to +70 −55 to +125	1	±500	1575	24 Pin	Yes	(Note 2)	8-35
12-Bits	±0.01	40nsec 2V Step to ±0.1%	+1, ±1V	MN4000	0 to +70 −55 to +125	50	±200	750	24 Pin	Yes	9085601	8-53
	±0.01	160nsec 10V Step to ±0.01%	−1, ±10V	MN376	0 to +70 −55 to +125	40	±0.5	730	24 Pin	Yes	9073001	8-31
	±0.01	250nsec 10V Step to ±0.01%	−1, ±10V	MN0300A	0 to +70 −55 to +125	400	±5	730	24 Pin	Yes	(Note 2)	8-5
	±0.01	1μsec 10V Step to ±0.01%	−1, ±10V	MN346	0 to +70 −55 to +125	400	±0.1	640	14 Pin	Yes	8994001	8-13
	±0.01	1μsec 10V Step to ±0.05%	−1, ±10V	MN347	0 to +70 −55 to +125	400	±0.5	640	14 Pin	Yes	(Note 2)	8-13
	±0.01	6.5μsec 20V Step to ±0.01%	−1, ±10V	MN7130	0 to +70 −55 to +125	60(1)	±4	900	32 Pin	Yes	9057101	9-9
	±0.01	7.5μsec 10V Step to ±0.01%	−1, ±10V	MN343	0 to +70 −55 to +125	2000	±0.1	345	14 Pin	Yes	(Note 2)	8-9
	±0.01	7.5μsec 10V Step to ±0.05%	−1, ±10V	MN344	0 to +70 −55 to +125	2000	±0.4	345	14 Pin	Yes	(Note 2)	8-9
14-16 Bits	±0.003	3μsec 10V Step to ±0.003%	−1, ±10V	MN374	0 to +70 −55 to +125	400	±0.1	390	14 Pin	Yes	(Note 2)	8-25
	±0.003	8.5μsec 10V Step to ±0.003%	±1, ±10V	MN373	0 to +70 −55 to +125	1000	±0.5	300	14 Pin	Yes	(Note 2)	8-17

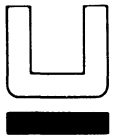
Instrumentation MN2200

Gain Ranges	Max Gain Error (%)	Offset Voltage (RTI, μV)	Offset Drift (μV/°C)	Small Signal BW (kHz)	Power (mW)	Specified Temp Range (°C)	DIP Pkg.	Mil-Std-883 Hi-Rel Option	DESC SMD (5962-)	Page No.
1, 10, 100, 1000 Internal, 1 to 1000 with External Resistor	±0.01 to ±0.1 Depending on Range	±100 (G=100)	±0.6 (G=100)	750 (G=1)	240	−25 to +85 −55 to +125	18 Pin	Yes	(Note 2)	8-47

Programmable-Gain MN2020

Gain Ranges	Max Gain Error (%)	Offset Voltage (RTI, μV)	Offset Drift (μV/°C)	Small Signal BW (kHz)	Power (mW)	Specified Temp Range (°C)	DIP Pkg.	Mil-Std-883 Hi-Rel Option	DES SMD (5962-)	Page No.
1, 2, 4, 8, 16, 32, 64, 128 Digitally Programmed	±0.005 to ±0.2 Depending on Range	±100	±5	5000 (G=1)	275	0 to +70 −55 to +125	18 Pin	Yes	(Note 2)	8-41

NOTES: 1. Listed specification is for typical Aperture Delay Time in nsec.
2. Contact the factory for information regarding DESC SMD's for these device types.
✓ Indicates New Product.



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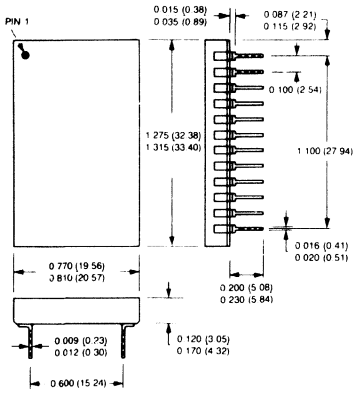
MN0300A

HIGH-SPEED
12-Bit LINEAR
T/H AMPLIFIER

FEATURES

- **300nsec Max Acquisition Time**
- **10V Step to ±0.01%**
- **±0.01%FS Linearity**
- **100psec Maximum Aperture Jitter**
- **±10V Input/Output Range**
- **G=−1, ±0.05% Gain Accuracy**
- **HTC-0300A Pin Compatible**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN0300A is a high-speed, dual-in-line packaged track-hold (sample-hold) amplifier designed for use in general-purpose data-acquisiton applications requiring performance up to the 12-bit level. Input/output linearity error is guaranteed not to exceed ±0.01%FS (equivalent to ±½LSB for 12 bits), and active laser trimming is used to minimize initial offset, pedestal and gain-accuracy errors.

MN0300A has been optimized for use in high-speed, wide-bandwidth, data-acquisition and rapid-update, data-distribution applications. Acquisition time for a 10V step acquired to ±0.01% (±1mV) is guaranteed not to exceed 300nsec; small-signal bandwidth is 8MHz; and output slew rate is typically ±250V/μsec. MN0300A's maximum output droop rate of ±7μV/μsec and minimum 70dB feedthrough attenuation make it suitable for both multiplexed and simultaneous sampling data-acquisition applications.

MN0300A has a gain of −1 and is TTL compatible. Devices require ±15V and +5V supplies and have a maximum power consumption of 875mW. Input/output voltage range is ±10V, and packaging is standard, 24-pin, ceramic dual-in-line. Standard product is specified for 0°C to +70°C (ambient) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN0300AH/B CH is fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

The MN0300A is second sourced by the Analog Devices/ Computer Labs HTC-0300A.

May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN0300A HIGH-SPEED 12-Bit LINEAR T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (Ambient)	−55°C to +125°C
Specified Temperature Range (Ambient)	
MN0300A	0°C to +70°C
MN0300AH, MN0300AH/B (Note 3)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
±15V Supply Voltage (±V_{CC}, Pins 24, 22)	±18 Volts
+5V Supply Voltage (+V_{dd}, Pin 9)	−0.5 to +7 Volts
Analog Input (Pin 13) (Note 1)	±18 Volts
Digital Input (Pins 11, 12)	−0.5 to +5.5 Volts
Output Current (Note 2)	±50 mA

ORDERING INFORMATION

PART NUMBER — **MN0300AH/B CH**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

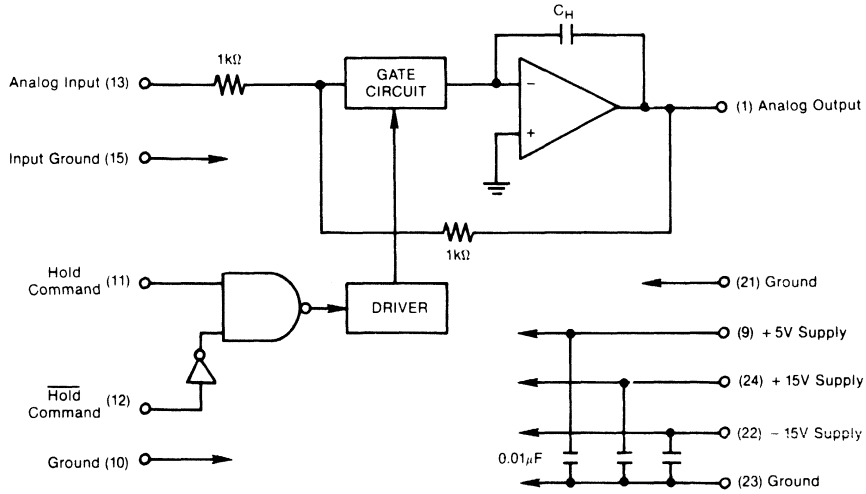
SPECIFICATIONS (T_A = +25°C, Supply Voltages = ±15V and +5V unless otherwise indicated).

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±10.25	±11.5		Volts
Input Impedance Input Bias Current		1	 ±15	kΩ μA
Output Current (Note 2) Output Impedance	±20	 0.1		mA Ω
Maximum Capacitive Load		250		pF
DIGITAL INPUT				
Logic Levels (TTL, Note 4): Logic "1" Logic "0"	+2 0		+5 +0.8	Volts Volts
Loading (Note 5)		1		TTL Load
TRANSFER CHARACTERISTICS				
Gain Gain Accuracy Gain Linearity Error (Note 6)		−1 ±0.05 ±0.005	 ±0.1 ±0.01	V/V % %FS
Offset Voltage (Track Mode) Pedestal (Note 7)		±2 ±5	±20 ±50	mV mV
Stability: Gain Drift Offset Drift (Track Mode)		±10 ±40	±50 ±75	ppm/°C ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisitiion Time (Note 6): 10V Step to ±0.01%FS (±1mV) 10V Step to ±0.1%FS (±10mV)		 250 170	 300 200	 nsec nsec
Settling Time (Track-to-Hold, Note 8) to ±0.1%FS (±10mV)		100	120	nsec
Aperture Delay Time Aperture Jitter		10	20 100	nsec psec(rms)
Output Slew Rate Small Signal Bandwidth (−3dB)	120 8	250		V/μsec MHz
Output Droop Rate		±5	±7	μV/μsec
Feedthrough (2.5MHz, 20Vp-p input)	70			dB
POWER SUPPLIES				
Voltage Range: ±15V Supplies +5V Supply	±12 +4.75	±15 +5	±18 ±5.25	Volts Volts
Power Supply Rejection Ratio		±10		mV/V
Quiescent Current Drain: +15V Supply −15V Supply +5V Supply		+21 −22 +17	+25 −25 +25	mA mA mA
Power Consumption		730	875	mW

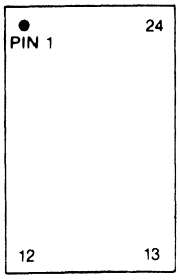
SPECIFICATION NOTES:

1. Analog input signal should not exceed supply voltage.
2. The MN0300A's output is current limited at approximately ± 50mA and can withstand a sustained short to ground. Shorts to either supply will result in destruction. In normal operation, load current should not exceed ± 20mA.
3. The MN0300AH/B is specified for − 55°C to + 125°C operation and is processed and screened to the requirements of MIL-STD-883, Method 5008.
4. See Applications Information for use of Hold and $\overline{\text{Hold}}$ inputs.
5. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
6. FS stands for Full Scale and is equivalent to 10 volts. FSR stands for Full Scale Range and is equivalent to 20 volts. For a 12-bit system, 1 LSB = 0.024%FSR.
7. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to hold mode. For many T/H's, pedestal amplitude is a function of input/output voltage level. For the MN0300A, pedestal is constant regardless of input/output level.
8. Track-to-hold settling time refers to the time interval between the point at which a device is commanded from the track to the hold mode and the point at which the analog output (following a transient) settles to within a specified error band around its final value.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Analog Output	24	+ 15V Supply
2	N/C	23	Ground
3	N/C	22	− 15V Supply
4	N/C	21	Ground
5	N/C	20	N/C
6	N/C	19	N/C
7	N/C	18	N/C
8	N/C	17	N/C
9	+ 5V Supply	16	N/C
10	Ground	15	Input Ground
11	Hold Command	14	N/C
12	$\overline{\text{Hold}}$ Command	13	Analog Input

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—In the track mode, MN0300A functions as an op amp in an inverting unity-gain configuration, and its output "follows" its input. When a logic "1" is applied to the Hold pin (pin 11), the MN0300A's output is frozen, and the output level is held until the track mode is reestablished by applying a logic "0" to the Hold pin. The held output level is the voltage applied at the input of the MN0300A at the instant (plus the aperture time) the hold command is applied.

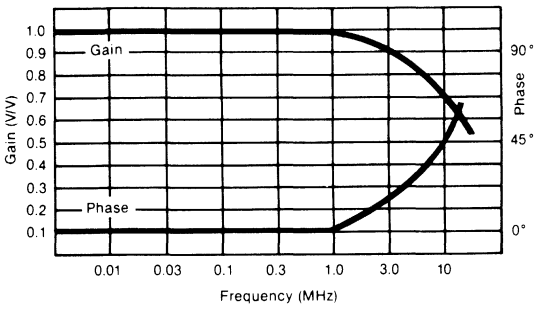
MN0300A provides a $\overline{\text{Hold}}$ input for use if the Hold command is inverted; that is if the user wishes to use a "0" for the hold condition and a "1" for the track mode. Performance of the unit is identical with either type of input.

Variations in the instants of sampling are called aperture uncertainty (jitter). It appears as jitter in the sampling point and can cause significant errors when very high dv/dt inputs are sampled. During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track-hold have high feedthrough rejection to prevent input-to-output leakage during the hold period. The droop rate is the amount the output changes during the hold period as a result of loading on the internal hold capacitor.

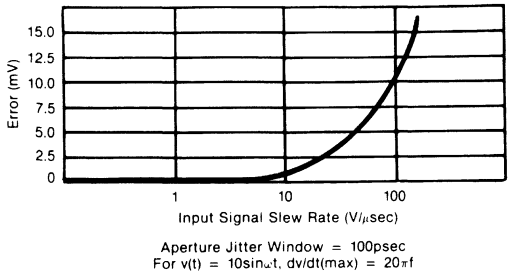
When the Hold command input returns to the track condition, the amount of time required for the track-and-hold output to reestablish accurate tracking of the input signal is called the acquisition time.

GROUNDING AND BYPASSING—With proper grounding and bypassing, MN0300A will meet all published performance specifications without any additional external components. The device has four Ground pins (pins 10, 15, 21 and 23). All four must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the MN0300A and have all four ground pins soldered directly to it.

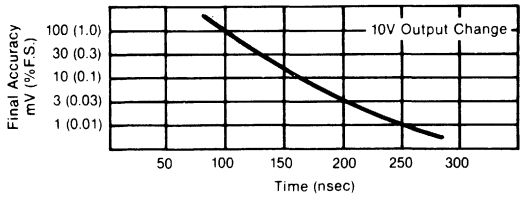
MN0300A's ±15V and +5V supply pins are bypassed to ground with 0.01μF ceramic capacitors inside the package. In critical applications, additional external 0.1μF to 1μF tantalum bypass capacitors may be required.



Track Mode Gain Amplitude and Phase Response



Accuracy Error Due to Aperture Uncertainty

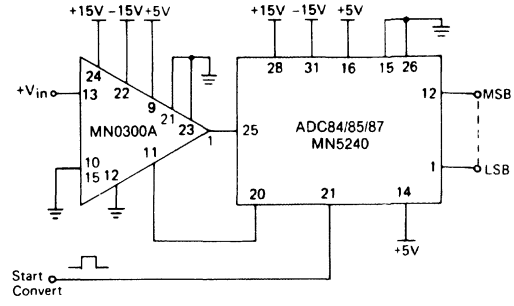


Acquisition Accuracy vs. Acquisition Time for a 10V Step

TRACK-HOLD COMMAND—A TTL logic "0" applied to pin 11 (or a logic "1" applied to pin 12) will put the MN0300A into the track (sample) mode. In this mode, the device acts as an inverting unity-gain amplifier, and its output will follow (track) its input. A logic "1" applied to pin 11 (or a logic "0" applied to pin 12) will put the MN0300A into the hold mode, and the output will be held constant at the level present when the hold command was given. If pin 11 is used to control the MN0300A, pin 12 must be connected to digital ground. If pin 12 is used to control the MN0300A, pin 11 must be tied to +5V. Pins 11 and 12 each present 1 TTL load to the digital drive circuit.

USING THE MN0300A WITH A/D CONVERTERS—There are two important considerations when using T/H's to drive successive approximation A/D's. The first is a dual requirement—the T/H's output stage should exhibit a very low impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock frequency, and the T/H should be able to recover from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the T/H will be required to sink or source large high frequency current transients and recover within one clock period. In the hold mode, the MN0300A's output impedance is typically 0.1Ω. Its output typically recovers (to ±0.01%) from a 2mA step in less than 150nsec. The second consideration involves the T/H's track-to-hold transient settling time. If the same timing pulse that puts the T/H into the hold mode initiates the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable accurate input when it makes the final decision on whether its MSB ouput should be a "1" or "0". This decision normally takes place one clock period after a conversion has begun.

In most applications using the MN0300A in front of a successive approximation A/D converter, the MN0300A's T/H command pin can be driven directly (or inverted if necessary) from the converter's status output. The status output changes state when the converter receives a convert command, and this change can drive the T/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the T/H back into the track mode. The diagram below illustrates an MN0300A mated with an ADC85 A/D in this manner. Since the ADC85's MSB output is not set to its final value until one clock period (approximately 600nsec) after a conversion begins, the MN0300A's track-to-hold transient will be completely settled, and no extra precautions are necessary.



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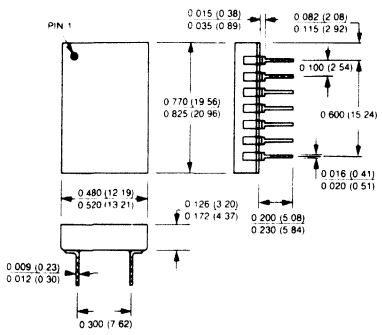
MN343
MN344

GENERAL-PURPOSE
TRACK-HOLD AMPLIFIERS

FEATURES

- Small 14-Pin DIP
- Internal Hold Capacitor
- 10μsec Max Acquisition Time (10V Step to ±0.01%, MN343)
- ±0.3μV/μsec Max Droop Rate (MN343)
- ±10V Range, G=−1
- Low Glitch 100mV
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

14 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN343 and MN344 are complete, adjustment-free track-hold amplifiers in small, 14-pin, hermetically sealed dual-in-line packages. Employing an operational "track and hold" design with neutralization of track-to-hold charge offset, they offer low offsets and fast acquisition times. MN343 acquires a signal to ±0.01% in 10μsec. MN344 acquires a signal to ±0.05% in 10μsec. Both devices guarantee hold offset including pedestal error to be less than 8.5mV.

Both models are complete with hold capacitor and are laser trimmed as complete units, eliminating the need for user adjustment. Feedthrough in the hold mode and track-hold track transients are minimized by the unique compensation scheme employed. Maximum droop rate is ±0.3μV/μsec for MN343 and ±1μV/μsec for MN344.

MN343 and MN344 are available for operation over the full −55°C to +125°C temperature range ("H" models). For military/aerospace or harsh-environment commercial/industrial applications, MN343H/B CH and MN344H/B CH are fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

MN343 and MN344 track-hold amplifiers offer circuit designers a convenient, reliable, one-component track-hold function. They are ideal for data acquisition systems, for holding time-varying analog signals during A/D conversion, and for deglitching D/A converter outputs. Small size and weight combined with reliable thin-film hybrid construction and specs guaranteed from −55°C to +125°C make these track-holds particularly well suited for military, avionics and aerospace applications.

April 1988

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324 Clark St., Worcester, MA 01606 (508) 852-5400

MN343 MN344 GENERAL-PURPOSE T/H AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN343, MN344	0°C to +70°C
MN343H, H/B; MN344H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 11)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 14)	+0.5 to −18 Volts
Analog Input (Pin 13)	±15 Volts
Digital Input (Pin 1)	−0.5 to +7 Volts
Output Current (Note 1)	±20mA

ORDERING INEORMATION

PART NUMBER ——— MN343H/B CH

Select MN343 or MN344.

Standard Part is specified for 0°C to +70°C operation.

Add "H" suffix for specified −55°C to +125°C operation.

Add "/B" to "H" devices for Environmental Stress Screening.

Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

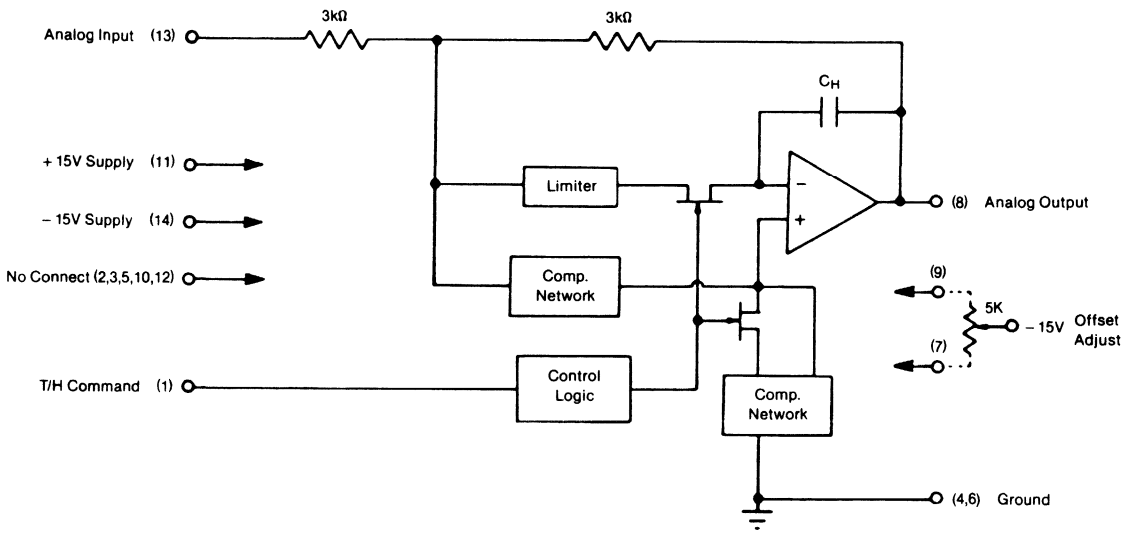
SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V unless otherwise indicated) (Note 2)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range (Note 4)	±10	±11		Volts
Input Resistance (Note 3)		3		kΩ
Output Current (Note 1)	±3			mA
DIGITAL INPUT				
Logic Levels: Logic "1" (Track Mode)	+2.0			Volts
Logic "0" (Hold Mode)			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+40	μA
Logic "0" (V_{IL} = +0.4V)			−1.6	mA
TRANSFER CHARACTERISTICS				
Gain		−1		V/V
Gain Linearity Error (Note 5)		±0.005	±0.01	%FSR
Gain Accuracy: Initial (+25°C): MN343		±0.01	±0.02	%
MN344		±0.03	±0.05	%
Over Temperature (Note 6)		±0.03	±0.05	%
Offset Voltage (Track Mode, Note 7): Initial (+25°C)		±1	±2.5	mV
Over Temperature (Note 6)		±4	±10	mV
Pedestal (Note 8): Initial (+25°C)		±3	±6	mV
Over Temperature (Note 6)		±5	±10	mV
DYNAMIC CHARACTERISTICS				
Acquisition Time: MN343: 10V Step to ±0.01% (±1mV)		7.5	10	μsec
20V Step to ±0.01% (±2mV)		10	15	μsec
MN344: 10V Step to ±0.05% (±5mV)		7.5	10	μsec
20V Step to ±0.05% (±10mV)		10	15	μsec
Track-to-Hold Transient (Note 9): Amplitude (Note 3)		±100		mV
Settling Time to ±1mV		1.5	2.5	μsec
Aperture Delay Time (Note 3)		60		nsec
Aperture Jitter (Note 3)		2		nsec
Output Slew Rate (Note 3)		±3		V/μsec
Full Power Bandwidth (10Vp-p, −3dB, Note 3)		80		kHz
Output Droop Rate: Initial (+25°C): MN343		±0.1	±0.3	μV/μsec
MN344		±0.4	±1	μV/μsec
0°C to +70°C (Note 3)		±3.5		μV/μsec
−55°C to +125°C ("H" models, Note 3)		±20		μV/μsec
Feedthrough Attenuation (@1kHz)		0.01	0.04	%
POWER SUPPLIES				
Voltage Range (Note 4)	±12	±15	±16	Volts
Power Supply Rejection Ratio (Note 3)		±100		μV/V
Current Drains: +15V Supply		+13	+17	mA
−15V Supply		−10	−12	mA
Power Consumption		345	435	mW

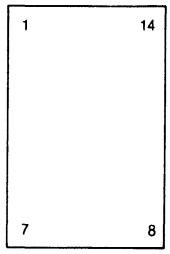
SPECIFICATION NOTES:

1. MN343/344's output is short-circuit protected, and units can withstand sustained shorts to ground or either supply with current limiting at approximately ±20mA. In normal operation, output current should not exceed ±3mA.
2. Listed specifications apply for both MN343 and MN344 unless otherwise indicated.
3. These parameters are listed for reference only and are not tested.
4. Maximum output voltage swing is typically $\pm V_{CC}$ ±4V.
5. FS stands for full scale and is equivalent to 10 Volts. FSR stands for full scale range and is equivalent to 20 Volts. For a 12-bit system, 1 LSB = 0.024% FSR.
6. Unless otherwise indicated, listed specifications apply over the 0°C to +70°C temperature range for MN343 and MN344 and over the −55°C to +125°C temperature range for MN343H, MN343H/B, MN344H and MN344H/B.
7. Adjustable to zero with user-optional external potentiometer.
8. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's, pedestal amplitude is a function of input/output voltage level. For the MN343 and MN344, pedestal is constant regardless of input/output level.
9. Track-to-hold settling time refers to the time interval between the point at which a device is commanded from the track to the hold mode and the point at which the analog output (following a transient) settles to within a specified error band around its final value.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 T/H Command	14 − 15V Supply (− Vcc)
2 No Connect	13 Analog Input
3 No Connect	12 No Connect
4 Ground	11 + 15V Supply (+ Vcc)
5 No Connect	10 No Connect
6 Ground	9 Offset Adjust
7 Offset Adjust	8 Analog Output

APPLICATIONS INFORMATION

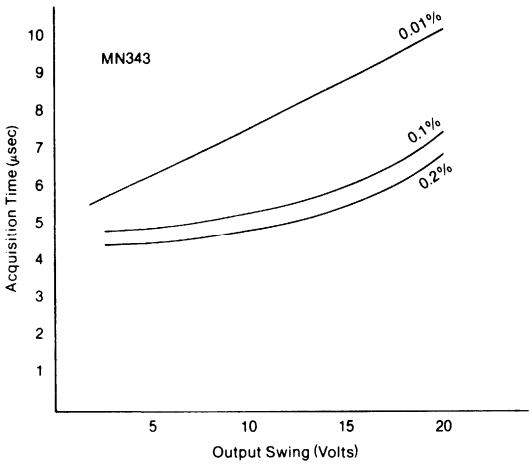
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from MN343 and MN344. The units' two Ground pins (pins 4 and 6) are not connected to each other internally. They should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

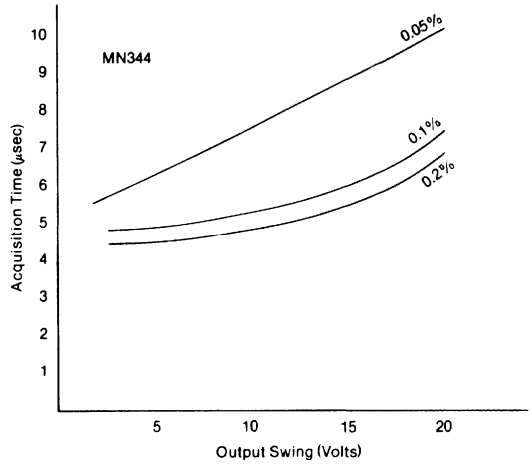
Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines. Input and output signal lines should be kept as short as possible, and if external offset adjustment is used, the potentiometer should be located as close to the unit as possible. If offset adjust is not used, pins 7 and 9 should be left open.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

OFFSET ADJUSTMENT—MN343/344's track-mode offset error can be reduced to zero with a 5kΩ potentiometer connected between pins 7 and 9 with its wiper connected to −15V. With the analog signal path grounded, the pot should be adjusted until the output equals zero volts. The pot can also be used to compensate for the effects of pedestal by performing the adjustment in the hold mode. This adjustment is normally made while continually switching from track to hold and observing the T/H output on a scope. This procedure will eliminate adjustment ambiguities resulting from output droop.

TRACK-HOLD COMMAND—A TTL logic "1" applied to pin 1 will put the MN343/344 into the track (sample) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output will follow (track) its input. A logic "0" applied to pin 1 will put the MN343/344 into the hold mode, and the output will be held constant at the level present when the hold command was given.





ORDERING INFORMATION

Part Number	Specified Temperature Range	Gain Accuracy (+25°C, Max)	Offset Voltage (+25°C, Max)	Acquisition Time (2) (10V Step, Max)	Output Droop Rate (+25°C, Max)	Power Consumption (Maximum)	Ceramic DIP Package
MN343	0°C to +70°C	±0.02%	±2.5mV	10μsec	±0.3μV/μsec	435mW	14-pin
MN343H	−55°C to +125°C	±0.02%	±2.5mV	10μsec	±0.3μV/μsec	435mW	14-pin
MN343H/B (1)	−55°C to +125°C	±0.02%	±2.5mV	10μsec	±0.3μV/μsec	435mW	14-pin
MN344	0°C to +70°C	±0.05%	±2.5mV	10μsec	±1μV/μsec	435mW	14-pin
MN344H	−55°C to +125°C	±0.05%	±2.5mV	10μsec	±1μV/μsec	435mW	14-pin
MN344H/B (1)	−55°C to +125°C	±0.05%	±2.5mV	10μsec	±1μV/μsec	435mW	14-pin

Notes:
1. Add "CH" to "H/B" models for 100% screening to MIL-H-38534.
2. For the MN343, acquisition time is specified for a final error band of ±0.01%. For the MN344, acquisition time is specified for a final error band of ±0.05%.

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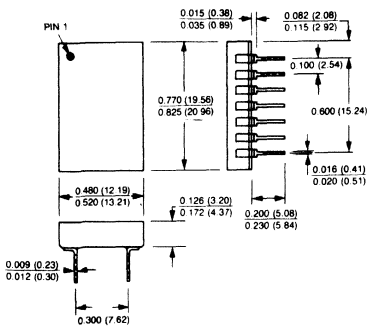
MN346
MN347

HIGH-SPEED
TRACK-HOLD AMPLIFIERS

FEATURES

- **Small 14-Pin DIP**
- **Internal Hold Capacitor**
- **2μsec Max Acquisition Time (10V Step to ±0.01%, MN346)**
- **±10V Range, G=−1**
- **±3mV Max Offset ±4mV Max Pedestal**
- **±0.5μV/μsec Max Droop Rate (MN346)**
- **Low Glitch 40mV**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

14 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN346 and MN347 are high-speed, adjustment-free track-hold amplifiers in small, 14-pin, hermetically sealed dual-in-line packages. Both units are complete with internal hold capacitor and incorporate a neutralization of track-to-hold charge offset that results in fast acquisition times and low pedestal errors. MN346 acquires a 10V step to ±0.01% in 2μsec. MN347 acquires a 10V step to ±0.05% in 2.5μsec. MN346 guarantees offset and pedestal errors to be less than ±3mV and ±4mV respectively. MN347 guarantees these errors to be less than ±5mV and ±8mV respectively.

Both MN346 and MN347 are functionally laser trimmed as complete units eliminating the need for user adjustment while saving the cost and space normally required for external components. A unique compensation scheme minimizes feedthrough and track-hold-track glitches. Maximum droop rate is ±0.5μV/μsec for the MN346 and ±1.5μV/μsec for the MN347.

MN346 and MN347 are available for operation over the full −55°C to +125°C temperature range, and high reliability processing, screening and qualification according to MIL-H-38534 are available for military/aerospace applications.

MN346 and MN347 offer the circuit designer very fast acquisition times and the convenience of a one-component track-hold function at low cost. These track-holds find application in D/A deglitching, in high-speed data distribution systems and in high-speed, simultaneously-sampling or sequential data acquisition systems requiring high scan rates. Small size and weight combined with reliable thin-film hybrid construction and specs guaranteed from −55°C to +125°C make these track-holds particularly well suited for military, avionics and aerospace applications.

May 1988

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324 Clark St., Worcester, MA 01606 (508) 852-5400

MN346 MN347 HIGH-SPEED T/H AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN346, MN347	0°C to +70°C
MN346H, H/B; MN347H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 11)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 14)	+0.5 to −18 Volts
Analog Input (Pin 13)	±15 Volts
Digital Input (Pin 1)	−0.5 to +7 Volts
Output Current (Note 1)	±20mA

ORDERING INFORMATION

PART NUMBER — MN346H/B CH

- Select MN346 or MN347.
- Standard Part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

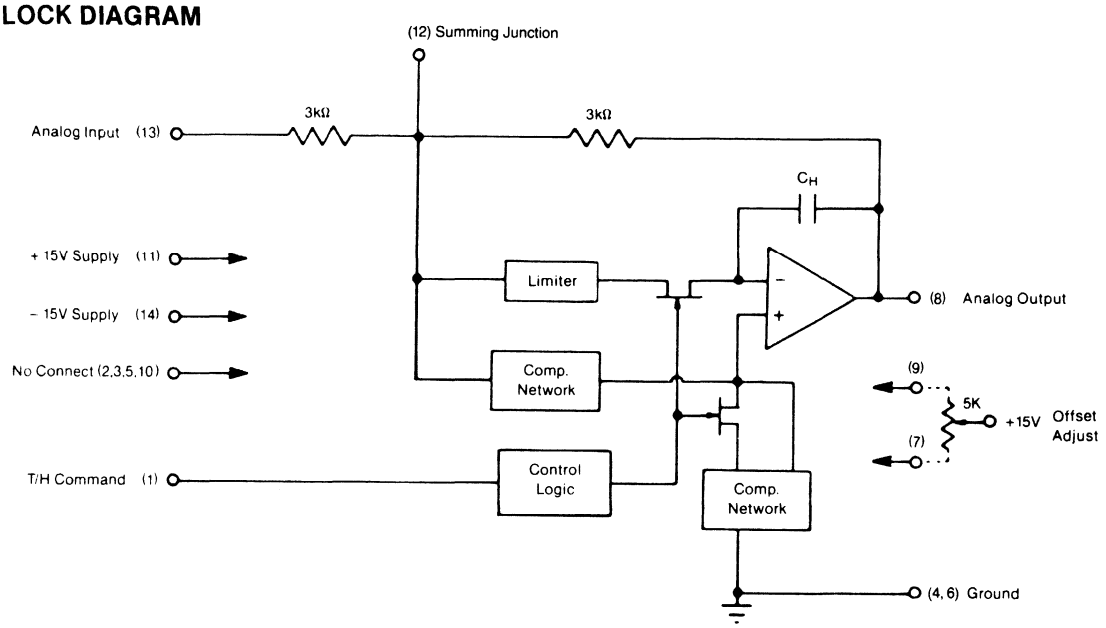
SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated) (Note 2)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range (Note 4)	±10	±11		Volts
Input Resistance (Note 3)		3		kΩ
Output Current (Note 1)	±3			mA
DIGITAL INPUT				
Logic Levels: Logic "1" (Track Mode)	+2.0			Volts
Logic "0"(Hold Mode)			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			+1	μA
Logic "0" (V_{IL} = +0.4V)			−150	μA
TRANSFER CHARACTERISTICS				
Gain		−1		V/V
Gain Linearity Error (Note 5)		±0.005	±0.01	%FSR
Gain Accuracy: Initial (+25°C): MN346		±0.01	±0.02	%
MN347		±0.03	±0.05	%
Over Temperature (Note 6): MN346		±0.03	±0.05	%
MN347		±0.06	±0.1	%
Offset Voltage (Track Mode, Note 7): Initial (+25°C): MN346		±1	±3	mV
MN347		±2	±5	mV
Over Temperature (Note 6)		±6	±20	mV
Pedestal (Note 8): Initial (+25°C): MN346		±2	±4	mV
MN347		±4	±8	mV
Over Temperature (Note 6)		±10	±20	mV
DYNAMIC CHARACTERISTICS				
Acquisition Time: MN346: 10V Step to ±0.01% (±1mV)		1	2	μsec
20V Step to ±0.01% (±2mV)		1.6	2.5	μsec
MN347: 10V Step to ±0.05% (±5mV)		1	2.5	μsec
20V Step to ±0.05% (±10mV)		1.6	3.5	μsec
Track-to-Hold Transient (Note 9): Amplitude (Note 3)		±40		mV
Settling Time to ±1mV		150	500	nsec
Aperture Delay Time (Note 3)		30		nsec
Aperture Jitter (Note 3)		400		psec
Output Slew Rate (Note 3)		±50		V/μsec
Full Power Bandwidth (10Vp-p, −3dB, Note 3)		1.4		MHz
Output Droop Rate: MN346: Initial (+25°C)		±0.1	±0.5	μV/μsec
0°C to +70°C		±20	±60	μV/μsec
−55°C to +125°C		±200	±700	μV/μsec
MN347: Initial (+25°C)		±0.5	±1.5	μV/μsec
0°C to +70°C		±60	±150	μV/μsec
−55°C to +125°C		±700	±1500	μV/μsec
Feedthrough Attenuation (@1kHz)		0.005	0.02	%
POWER SUPPLIES				
Voltage Range (Note 4)	±12	±15	±16	Volts
Power Supply Rejection Ratio (Note 3)		±100		μV/V
Current Drains: +15V Supply		+20	+28	mA
−15V Supply		−17	−25	mA
Power Consumption		640	795	mW

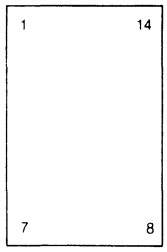
SPECIFICATION NOTES:

1. MN346/347's output is short-circuit protected and units can withstand sustained shorts to ground or either supply with current limiting at approximately ±20mA. In normal operation, output current should not exceed ±3mA.
2. Listed specifications apply for both MN346 and MN347 unless otherwise indicated.
3. These parameters are listed for reference only and are not tested.
4. Maximum output voltage swing is typically ±Vcc ±4V.
5. FS stands for full scale and is equivalent to 10 Volts. FSR stands for full scale range and is equivalent to 20 Volts. For a 12-bit system, 1 LSB=0.024%FSR.
6. Unless otherwise indicated, listed specifications apply over the 0°C to +70°C temperature range for MN346 and MN347 and over the −55°C to +125°C temperature range for MN346H, MN346H/B, MN347H and MN347H/B.
7. Adjustable to zero with user-optional external potentiometer.
8. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's, pedestal amplitude is a function of input/output voltage level. For the MN346 and MN347, pedestal is constant regardless of input/output level.
9. Track-to-hold settling time refers to the time interval between the point at which a device is commanded from the track to the hold mode and the point at which the analog output (following a transient) settles to within a specified error band around its final value.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	T/H Command	14	−15V Supply (−Vcc)
2	No Connect	13	Analog Input
3	No Connect	12	Summing Junction
4	Ground	11	+15V Supply (+Vcc)
5	No Connect	10	No Connect
6	Ground	9	Offset Adjust
7	Offset Adjust	8	Analog Output

APPLICATIONS INFORMATION

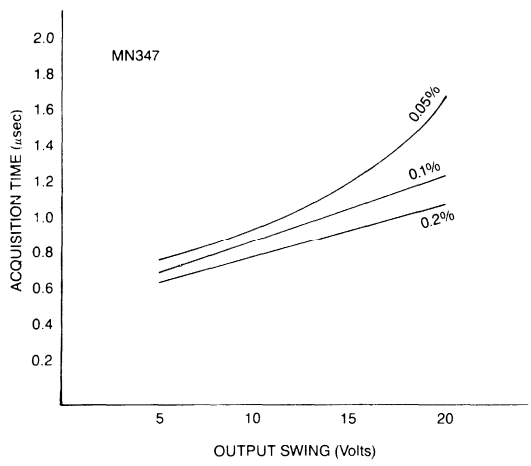
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from MN346 and MN347. The units' two Ground pins (pins 4 and 6) are not connected to each other internally. They should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

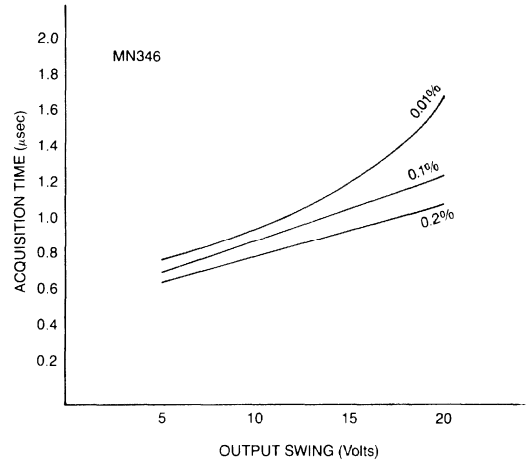
Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines. Input and output signal lines should be kept as short as possible, and if external offset adjustment is used, the potentiometer should be located as close to the unit as possible. If offset adjust is not used, pins 7 and 9 should be left open.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

OFFSET ADJUSTMENT—MN346/347's track-mode offset error can be reduced to zero with a 5kΩ potentiometer connected between pins 7 and 9 with its wiper connected to +15V. With the analog signal path grounded, the pot should be adjusted until the output equals zero volts. The pot can also be used to compensate for the effects of pedestal by performing the adjustment in the hold mode. This adjustment is normally made while continually switching from track to hold and observing the T/H output on a scope. This procedure will eliminate adjustment ambiguities resulting from output droop.

TRACK-HOLD COMMAND—A TTL logic "1" applied to pin 1 will put the MN346/347 into the track (sample) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output will follow (track) its input. A logic "0" applied to pin 1 will put the MN346/347 into the hold mode, and the output will be held constant at the level present when the hold command was given.





ORDERING INFORMATION

Part Number	Specified Temperature Range	Gain Error (Max)		Offset Error (Max)		Pedestal (Max)		Acquisition Time (2) (10V Step, Max)	Output Droop Rate (3) (Max)	
		+25°C	Temp.	+25°C	Temp.	+25°C	Temp.		+25°C	Temp.
MN346	0°C to +70°C	±0.02%	±0.05%	±3mV	±20mV	±4mV	±20mV	2μsec	±0.5	±60
MN346H	−55°C to +125°C	±0.02%	±0.05%	±3mV	±20mV	±4mV	±20mV	2μsec	±0.5	±700
MN346H/B (1)	−55°C to +125°C	±0.02%	±0.05%	±3mV	±20mV	±4mV	±20mV	2μsec	±0.5	±700
MN347	0°C to +70°C	±0.05%	±0.1%	±5mV	±20mV	±8mV	±20mV	2.5μsec	±1.5	±150
MN347H	−55°C to +125°C	±0.05%	±0.1%	±5mV	±20mV	±8mV	±20mV	2.5μsec	±1.5	±1500
MN347H/B (1)	−55°C to +125°C	±0.05%	±0.1%	±5mV	±20mV	±8mV	±20mV	2.5μsec	±1.5	±1500

Notes:
1. Add "CH" to "H/B" models for 100% screening to MIL-H-38534.
2. For the MN346, acquisition time is specified for a final error band of ±0.01%. For the MN347, acquisition time is specified for a final error band of ±0.05%.
3. The units for droop are μV/μsec.

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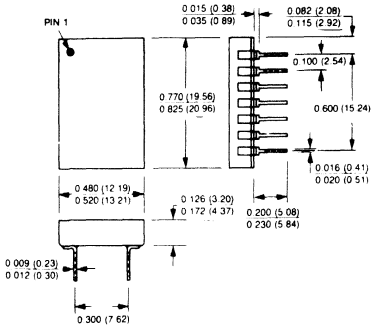
MN373

LOW-COST
HIGH-RESOLUTION
TRACK-HOLD AMPLIFIER

FEATURES

- **Low Cost**
- **Compatible with All DIP Packaged 14-16 Bit A/D's**
- **10μsec Max Acquisition Time (10V Step to ±0.003%)**
- **1nsec Aperture Jitter**
- **±0.25μV/μsec Max Droop**
- **±1mV Max Offset Error**
- **84dB Feedthrough Attenuation**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

14 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN373 is a high-resolution, moderately high-speed, track-hold (T/H) amplifier designed to be compatible with all DIP packaged 14-16 bit A/D converters available today. Some of the performance specifications that make MN373 ideal for high-resolution applications are summarized below:

Specification	Typ.	Max.	Units
Gain Linearity Error	±0.001	±0.003	%FSR
Gain Accuracy	±0.003	±0.01	%
Gain Drift	±0.25	±1	ppm/°C
Offset Voltage	±0.25	±1	mV
Offset Drift	±3	±20	μV/°C
Output Droop Rate	±0.05	±0.25	μV/μsec
Feedthrough Attenuation	84		dB

Dynamic specifications include 10μsec maximum acquisition time (for a 10V step acquired to ±0.003%), 1nsec aperture jitter and 400kHz small signal bandwidth. MN373's outstanding ±0.25μV/μsec maximum output droop rate enables the device to hold signals to the 14-bit level for up to 2.4msec and to the 16-bit level for up to 600μsec. This makes MN373 ideal for high-resolution simultaneous-sampling applications.

MN373 is packaged in a standard, 14-pin, ceramic dual-in-line and is TTL compatible. The device contains an uncommitted, high-impedance (5MΩ), input buffer amplifier that enables it to be used in numerous inverting and noninverting configurations with and without gain. The input stage has a CMV of ±10V; a CMRR of 72dB minimum; and an input bias current guaranteed not to exceed ±300nA. Required power supplies are ±15V, and maximum power consumption is 390mW.

The standard MN373 is fully specified for 0°C to +70°C (ambient) operation; with MN373H fully specified for −55°C to +125°C (ambient) operation. MN373H/B CH includes 100% screening to MIL-H-38534.

MN373 mates directly with Micro Networks MN5280/82, MN5290/91 and MN5295/96 16-bit A/D converters. For military/aerospace applications, MN373H/B can be mated with MN5290H/B to configure a full 16-bit digitizer with a 20kHz sampling rate, a 10kHz analog bandwidth, and guaranteed 14-bit no missing codes from −55°C to +125°C. With MN5295, it forms a 33kHz digitizer.

May 1988

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324 Clark St., Worcester, MA 01606 (508) 852-5400

MN373 LOW-COST HIGH-RESOLUTION T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN373	0°C to +70°C
MN373H, MN373H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 9)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 5)	+0.5 to −18 Volts
Analog Input Voltage (Pins 1 and 2)	±15 Volts
Differential Input Voltage (Pin 1 to Pin 2)	±20 Volts
Digital Input (Pin 14)	−0.5 to +7 Volts
Output Current (Note 1)	±20mA

ORDERING INFORMATION

PART NUMBER ——— **MN373H/B CH**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages = ±15V, C_H = Internal, Load = 1kΩ//50pF unless otherwise indicated)

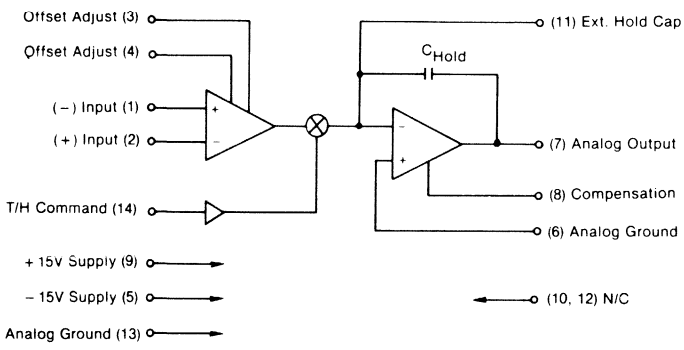
ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±10	±11		Volts
Input Resistance		5		MΩ
Input Capacitance		3		pF
Input Bias Current: Initial (+25°C)		±100	±300	nA
Over Temperature		±200	±500	nA
Input Offset Current: Initial (+25°C)		±30	±300	nA
Over Temperature		±60	±500	nA
Common Mode Voltage Range	±10			Volts
CMRR	72	90		dB
Output Current (Note 1)	±10			mA
Output Resistance (Hold Mode)		1		Ω
Maximum Capacitive Load		250		pF
Output Noise (d.c. to 10MHz): Track Mode		150		μV(rms)
Hold Mode		150		μV(rms)
DIGITAL INPUTS				
Logic Levels: Logic "1" (Hold Mode)	+2			Volts
Logic "0" (Track Mode)			+0.8	Volts
Loading: Logic "1"			+10	μA
Logic "0"			−10	μA
TRANSFER CHARACTERISTICS (Note 4)				
Open Loop Gain (d.c.)	10^6	2×10^6		V/V
Gain Accuracy (G = +1)		±0.003	±0.01	%
Gain Linearity Error (Note 2)		±0.001	±0.003	%FSR
Offset Voltage (Track Mode)		±0.25	±1	mV
Pedestal (Note 3)		±0.5	±2	mV
Stability: Gain Drift		±0.25	±1	ppm/°C
Offset Drift (Track Mode)		±3	±20	μV/°C
Pedestal Drift		±10		μV/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time:				
10V Step to ±0.003% (±0.3mV)		8.5	10	μsec
10V Step to ±0.006% (±0.6mV)		8	9.5	μsec
10V Step to ±0.01% (±1mV)		7.5	9	μsec
Track-to-Hold Transient Settling Time:				
to ±0.003%FS (±0.3mV)		250		nsec
to ±0.006%FS (±0.6mV)		225		nsec
to ±0.01%FS (±1mV)		200		nsec
Track-to-Hold Transient		25		mVp-p
Aperture Delay Time		30		nsec
Aperture Jitter		1		nsec
Output Slew Rate		±10		V/μsec
Small Signal Bandwidth (−3dB, G = +1)		400		kHz
Output Droop Rate: +25°C		±0.05	±0.25	μV/μsec
0°C to +70°C		±3	±7.5	μV/μsec
−55°C to +125°C ("H" Models)		±10	±20	μV/μsec
Feedthrough Attenuation (10kHz, 10Vp-p input)		84		dB

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Voltage Range (Note 5)	± 14.5	± 15	± 16	Volts
Power Supply Rejection: + 15V Supply − 15V Supply		± 0.1 ± 0.4		mV/V mV/V
Current Drain: + 15V Supply − 15V Supply		10 − 10	13 − 13	mA mA
Power Consumption		300	390	mW

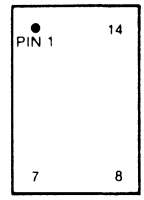
SPECIFICATION NOTES

1. The MN373's output is not short-circuit protected, and shorts to ground or either supply will result in destruction. In normal operation, continuous output current should not exceed ± 10mA.
2. FSR stands for Full Scale Range and is equal to 20 volts for the MN373. ± 0.003%FSR is equivalent to ± ½ LSB for a 14-bit system.
3. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's pedestal amplitude is a function of input/output voltage level. For the MN373, pedestal is constant regardless of input/output level. It will vary as a function of the user-optional external hold capacitor, however.
4. Gain Accuracy, Gain Linearity, Offset Voltage, Pedestal and their respective drifts are specified for the MN373 in the follower (G = + 1) configuration.
5. MN373 will operate with ± V_{CC} supplies down to ± 10.5V if input/output voltage is kept below ± 7.5V.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 (−) Input	14 T/H Command
2 (+) Input	13 Ground
3 Offset Adjust	12 N/C
4 Offset Adjust	11 External Hold Cap
5 − 15V Supply	10 N/C
6 Ground	9 + 15V Supply
7 Analog Output	8 Compensation

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from the MN373. The unit's two Ground pins (pins 6 and 13) are not connected to each other internally. They should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible. If your system distinguishes between analog signal and analog power gounds, pin 6 may be connected to system signal ground and pin 13 to system power ground.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

If external hold and compensation capacitors are used, they should be located as close to the MN373 as possible. If these capacitors are not used, pins 8 and 11 should be left open.

DESCRIPTION OF OPERATION—MN373 consists of a high-speed transconductance amplifier, an analog switch, a hold capacitor and a high-speed output integrating amplifier. With uncommitted inverting input, noninverting input and analog output terminals, MN373 operates as an uncommitted op amp whose output level can be held constant with the application of a digital control signal. The use of external resistors enables one to configure the MN373 in any number of inverting and noninverting configurations with and without gain.

The most popular use of the MN373 is as a noninverting, unity-gain track-hold amplifier. This is achieved by connecting pin 1 (Inverting Analog Input) to pin 7 (Analog Output) and applying the analog input signal to pin 2 (Noninverting Analog Input). In this configuration, with a logic "0" applied to pin 14 (T/H Command), the MN373's output will track its input. When a logic "1" is applied to pin 14, the

MN373 is driven into the hold mode holding its output constant at the value that appeared when the hold command was given.

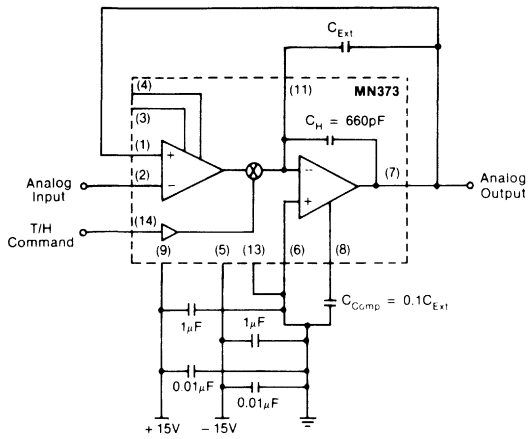


Figure 1. MN373 configured as a follower (G = +1) with additional hold capacitance.

MN373 was specifically designed for use with Micro Networks MN5290, MN5291 and MN5282 16-bit, DIP packaged, A/D converters, and its output droop rate is slow enough to hold a given analog sample to required accuracy while those devices perform a conversion. If slower droop rates are required, the MN373 can accept additional hold capacitance applied to pin 11. A later section describes this operation in detail.

MN373 can have its track mode offset error or the effect of its pedestal reduced to zero with the use of an external potentiometer. This is also described in detail in a later section.

ADDITIONAL HOLD CAPACITANCE—MN373 has an internal 660pF hold capacitor and published performance specifications are based on this capacitor. If one wishes to reduce droop rate or pedestal amplitude while trading off acquisition time, additional hold capacitance may be added between pins 11 (External Hold Cap) and 7 (Analog Output). The hold capacitor should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon and glass dielectrics offer good performance to +125°C and above. Whenever additional hold capacitance is used, additional compensation capacitance equal to one-tenth the additional hold capacitance must be connected between pin 8 (Compensation) and ground. Exact value and type for this capacitor are not critical.

OFFSET ADJUSTMENT—MN373's track-mode offset error can be reduced to zero using a 20kΩ potentiometer connected between pins 3 and 4 with its wiper connected to −15V. With the analog signal path grounded, the pot should be adjusted until the output equals zero volts. The pot can also be used to compensate for the effects of pedestal by performing the adjustment in the hold mode. This adjustment is normally made while continually switching from track to hold and observing the T/H output on a scope. This procedure will eliminate adjustment ambiguities resulting from output droop.

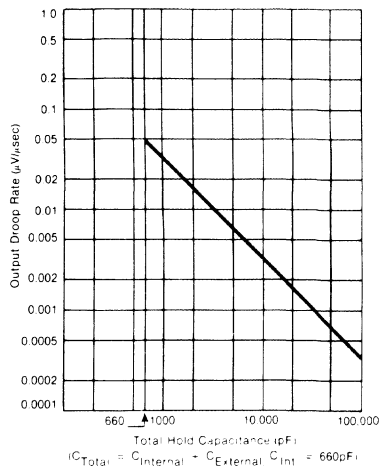


Figure 2. Output Droop Rate v.s. Hold Capacitance

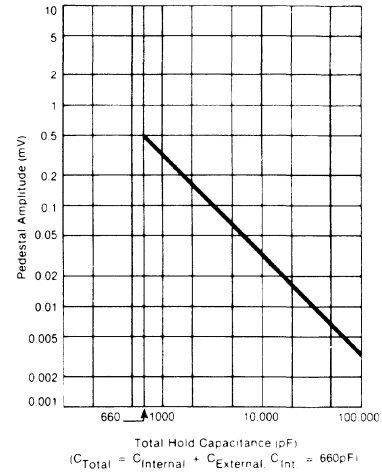


Figure 3. Pedestal Amplitude v.s. Hold Capacitance

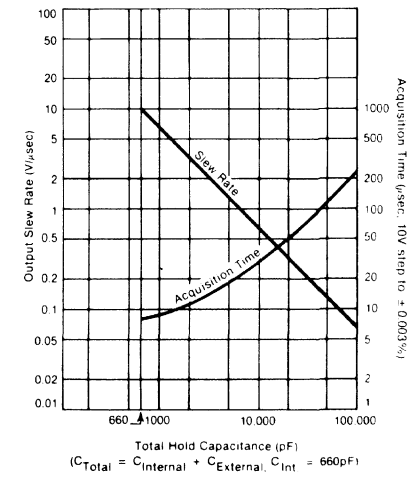


Figure 4. Slew Rate and Acquisition Time v.s. Hold Capacitance

USING MN373 WITH SUCCESSIVE APPROXIMATION A/D CONVERTERS— Successive approximation (SA) type A/D converters are oftentimes severely analog-input-signal slew-rate and bandwidth limited and can easily produce errors when used to digitize dynamically changing signals. The input-signal bandwidth limitations arise from the fact that successive approximation type A/D's sequentially determine output-bit values (from MSB to LSB) by comparing the analog equivalent of output bits already determined to the instantaneous analog input signal. The conversion process assumes the analog input signal remains "constant", and analog-input slew-rate and bandwidth limitations derive from the requirement that input signals not change more than ± ½LSB (for the appropriate resolution) during the conversion period.

$$\text{Input Slew Rate Limit} = \frac{\pm \frac{1}{2}\text{LSB}}{\text{Conversion Time}}$$

$$\text{Input Bandwidth}^{*} = \frac{\pm \frac{1}{2}\text{LSB}}{(\text{Conv. Time})(2\pi)(\text{FSR}/2)}$$

$$\text{Input Bandwidth}^{*} = \frac{(\text{FSR}/2^{n+1})}{(\text{Conv. Time})(2\pi)(\text{FSR}/2)}$$

*For full scale sine waves
FSR = A/D converter full scale range
n = resolution in bits

These A/D converter input-bandwidth limitations can be greatly overcome by using track-hold (T/H) amplifiers to track and subsequently "freeze" (hold) analog input signals that are changing too rapidly for the A/D alone to accurately digitize. If other parameters are appropriate, the slew-rate and bandwidth limiting factor of the T/H-A/D combination will be the T/H's aperture jitter (aperture uncertainty) specification, and the T/H-A/D combination will now be able to accurately sample and digitize signals slewing as much as ± ½LSB during the T/H's aperture jitter time. The formulas for determining how fast a signal a given T/H can accurately capture when used in conjunction with a given A/D converter are the same as those stated above with ± ½LSB defined for the A/D converter and with the variable (conversion time) replaced by (aperture jitter). Needless to say, aperture jitter is a significantly smaller number than conversion time, and the bandwidth improvement when using the T/H v.s. not using the T/H will equal the ratio of A/D conversion time to T/H aperture jitter.

As an example, consider Micro Networks MN5290 16-bit A/D converter. This device guarantees "no missing codes" to the 14-bit level, and it performs a 14-bit conversion in 40μsec (maximum). For this device operating on its full ±10V input voltage range, ± ½LSB (for 14 bits) is equivalent to ±0.61mV, and the analog input slew-rate limitation is equal to ± ½LSB/conversion time = ±0.61mV/40μsec = ±0.015mV/μsec. This is equivalent to the highest slew rate encountered in a full-scale (±10V) sine wave with a frequency of 0.24Hz. When used in conjunction with MN5290, MN373, with its 1nsec aperture jitter, is capable of capturing signals (to 14-bit accuracy) with slew rates up to ± ½LSB/aperture jitter = ±0.61mV/nsec = 610mV/μsec. This is the highest slew rate one would encounter in a full-scale sine wave with a frequency of 9.7kHz. As expected, the improvement ratio of 9.7kHz to 0.24Hz is equal to the ratio of 40μsec to 1nsec.

Using T/H's in conjunction with A/D's to increase analog bandwidth will reduce throughout (conversion rate) in that new digital output data cannot be realized until after the T/H has acquired a new signal (acquisition time) and the A/D has converted it (conversion time). Another consideration when calculating T/H-A/D throughput is the T/H's Track-To-Hold Transient Settling Time. If the same timing pulse is used to put the T/H into the hold mode and initiate the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable, accurate input when it makes the final decision on whether its MSB output should be a "1" or "0". This decision normally takes place one clock period after a conversion has begun.

In the case of using MN373 with MN5290, the A/D's MSB is not set to its final value until approximately 2.5μsec after a conversion has begun, and MN373's track-to-hold transient has long since died away. When using faster A/D's, a delay may have to be added between the time the T/H goes into hold and the A/D begins converting with the consequence that throughput suffers.

Returning to the MN373-MN5290 combination, the throughput time will be 50μsec (10μsec acquistion time plus 40μsec conversion time), and the conversion rate will be 20kHz. Comparing this to the 9.7kHz analog bandwidth leads one to conclude that the MN373-MN5290 pair is capable of "Nyquist digitizing" 9.7kHz sine waves at a 19.4kHz rate while guaranteeing true 14-bit resolution.

Other considerations when using T/H's with successive approximation A/D's involve the T/H's output stage. In the hold mode, it should exhibit a very low output impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock frequency. Also, the T/H should be able to fully recover (to ± ½LSB) from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the T/H will be required to sink or source high frequency current transients and recover within one clock period. The MN373's output is not current limited, and in the hold mode, output impedance is typically below 1Ω. It recovers from output current transients (to ±0.003%FS) in less than 1μsec.

In most applications using MN373 in front of a successive approximation A/D converter, MN373's T/H Command pin can be driven directly (or inverted if necessary) from the converter's status output. The status output changes state when the converter receives a convert command, and this change can drive the T/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the T/H back into the track mode. The diagram below illustrates an MN373 mated with an MN5290 in this manner. Since MN5290's MSB output is not set to its final value until one clock period (approximately 2.8μsec) after a conversion begins, MN373's track-to-hold transient will be completely settled, and no extra timing precautions are necessary.

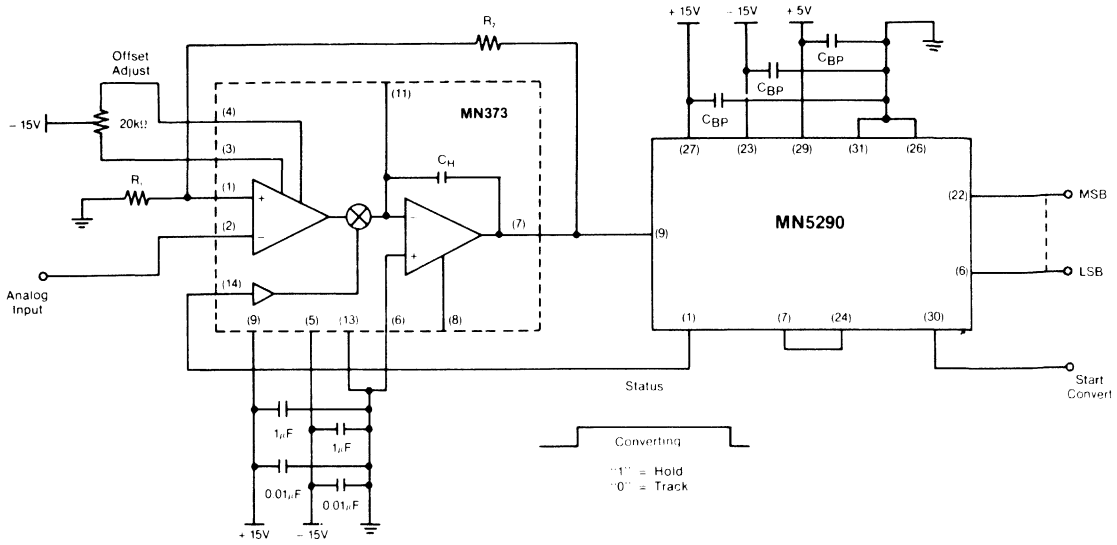


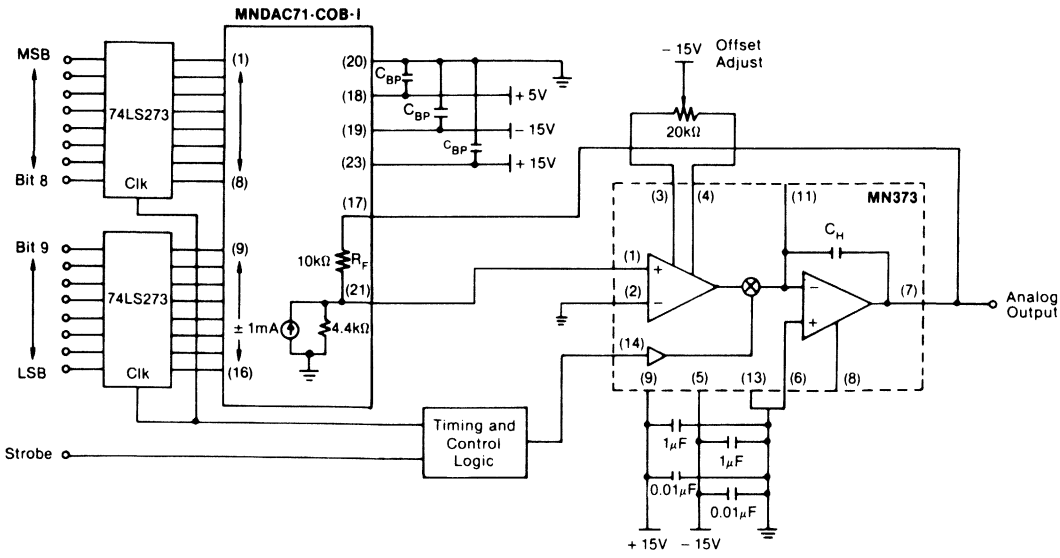
Figure 5. Combine MN373 with MN5290 to make a 14-bit digitizer with a 20kHz update rate, a 10kHz analog-signal bandwidth, and 14-bit no missing codes guaranteed over temperature.

USING MN373 TO DEGLITCH HIGH-RESOLUTION CURRENT-OUTPUT D/A CONVERTERS—Virtually all digital-to-analog (D/A) converters exhibit output transients, affectionately know as glitches, when changing output levels in response to digital-input code changes. The primary causes of glitches are unequal digital-data arrival and delay times, know as data skew, and asymmetrical switch turn-on and turn-off times. The largest glitches occur when major-carry code changes are made. In particular, the worst-case glitch occurs at half scale when the input-code change is from 0111...1 to 1000...0 or vice versa. Asymmetrical switch turn-on and turn-off delays may result in momentary slewing to the 0000...0 or 1111...1 output level until all switches achieve their final state. The binarily-weighted nature of the current switches internal to most D/A converters makes glitch slew rate and amplitude vary from transition to transition, and consequently makes glitches extremely difficult to remove with filtering. D/A converter output glitches may or may not be a problem depending upon application. In long time-constant servo applications, they will not be a problem. In high-speed, high-resolution waveform generators, they can cause severe harmonic distortions.

A deglitcher is a specially designed T/H amplifier capable of considerably reducing D/A glitch amplitude and, perhaps more importantly, making all glitches the same regardless of digital-code change. MN373 works well as a deglitcher because it has a small 25mV switching transient, and if it used to deglitch a current-output D/A, it can also act as an output amplifier supplying current-to-voltage conversion.

A T/H amplifier used as a deglitcher is connected to the output of the D/A and is kept in the track mode whenever the D/A output is stable. Just prior to the arrival of new digital data, the T/H is commanded to the hold mode to hold its output constant while the D/A's output (the T/H's input) is changing levels and experiencing its glitches. The T/H is then put back into the track mode to acquire and track the new D/A output.

The diagram on the next page illustrates MN373 performing both deglitching and current-to-voltage conversion for a current-output, 16-bit D/A converter (MNDAC71-COB-I). MN373's high-impedance input buffer allows the current-output D/A to work into a virtual ground, and the D/A's internal feedback resistor is put into MN373's feedback loop. The 16-bit D/A guarantees ±0.003%FSR maximum linearity error, and MN373's linearity error is commensurate. MN373's ±10mA minimum output current is enough to drive the feedback resistor and the load. MN373's acquisition time is equal to the D/A's settling time when used without a deglitcher so update rate is not compromised. MN373's outstanding feedthrough attenuation ensures that very little of the actual D/A glitch feeds through to the T/H output, and the unit's low output droop rate ensures that output change will be less than ±2.5μV during the approximately 10μsec that MN373 is in the hold mode.



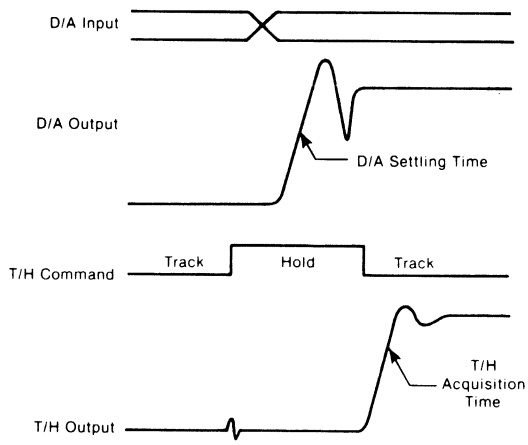
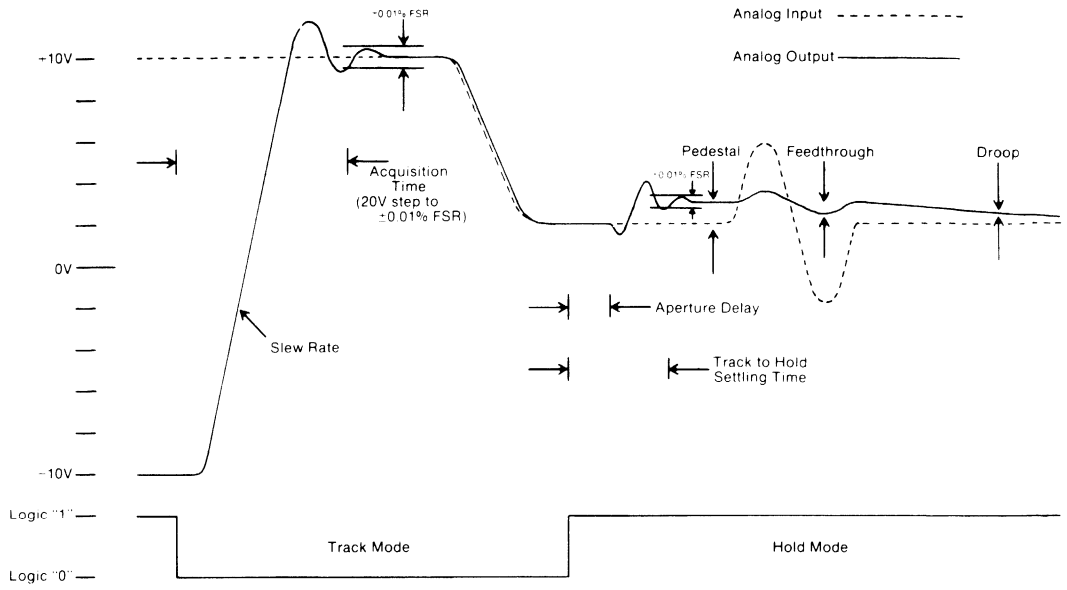
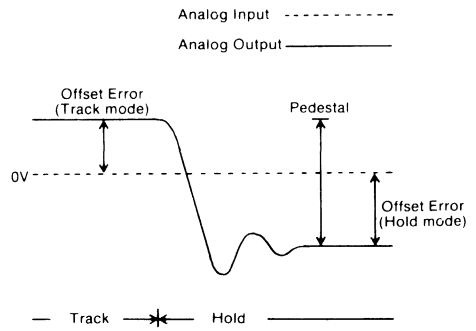


Figure 6. Use MN373 with high-resolution current-output D/A converters to perform both current-to-voltage conversion and output deglitching.

SUMMARY OF TRACK-HOLD PERFORMANCE PARAMETERS



Summary of T/H specifications. The broken line is the T/H's analog input. The solid line shows its analog output. The T/H has a ± 10V analog input range. The lower trace is the digital T/H command signal. A logic "0" puts the T/H into the track mode. A logic "1" puts it into the hold mode. See the tutorial section of the Micro Networks catalog for a detailed discussion of T/H performance specifications.



Summary of Offset (Track Mode), Offset (Hold Mode) and Pedestal Errors. Broken line is T/H analog input. Solid line is analog output. Analog input level equals zero volts.

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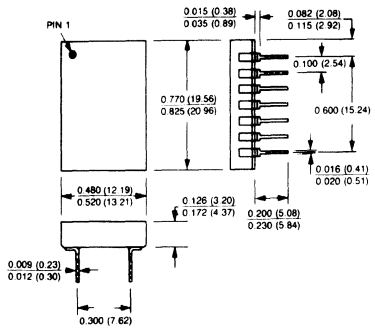
MN374

HIGH-SPEED
HIGH-RESOLUTION
TRACK-HOLD AMPLIFIER

FEATURES

- 4μsec Max Acquisition Time (20V Step to ±0.003%)
- Compatible with All DIP Packaged 14-16 Bit A/D's
- 400psec Aperture Jitter
- ±1μV/μsec Max Droop Rate
- 90dB Min Feedthrough Attenuation
- Small 14-Pin DIP
- Pin and Function Compatible with SHC76
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

14 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN374 is a high-speed (4μsec max acquisition time for a 20V step acquired to ±0.003%), high-resolution (±0.003%FSR max linearity error), unity-gain, inverting track-hold (T/H) amplifier designed to be compatible with virtually all DIP-packaged, 14-16 bit A/D converters available today. In particular, MN374 mates well with Micro Networks MN5290/5291 (40μsec, 16-bit A/D's) and MN5295/5296 (17μsec, 16-bit A/D's) as well as with other industry-standard 16-bit A/D's (ADC71/72, ADC76, AD376, etc.).

The TTL-compatible MN374 makes the speed/precision trade-off very well. Its impressive d.c. specifications include a maximum ±0.02% gain error, a maximum ±3mV offset error and a maximum ±4mV pedestal. Dynamic specifications include 4μsec max acquisition time (20V step acquired to ±0.003%); 3μsec max track-to-hold transient settling time (to ±0.003%FSR); 400psec aperture jitter; and ±30V/μsec slew rate. MN374's outstanding ±1μV/μsec maximum output droop rate enables the device to hold signals to the 14-bit level for up to 600μsec and to the 16-bit level for up to 150μsec. These performance levels make MN374 ideal for high-resolution data acquisition in either single-channel, multichannel sequenced, or multichannel simultaneous-sampling applications.

An application note in this data sheet describes how to mate MN374 with MN5295 (16-bit, 17μsec A/D) to create a 40kHz sampling A/D that guarantees 14-bit "no missing codes" over its full temperature range.

MN374 is packaged in a small, 14-pin, single-wide, ceramic DIP, and it carries the pinout that has become the de facto standard for high-resolution T/H's. MN374 is fully specified for either 0°C to +70°C or −55°C to +125°C ("H" model) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN374H/B CH is fully screened to MIL-H-38534 in Micro Networks' MIL-STD-1772 qualified facility.

Contact factory for availability of CH devices.

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MN374 HIGH-SPEED HIGH-RESOLUTION T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN374	0°C to +70°C
MN374H, MN374H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 11)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 14)	+0.5 to −18 Volts
Analog Input (Pin 13)	± 15 Volts
Digital Input (Pin 1)	−0.5 to +7 Volts
Output Current (Note 1)	± 20 mA

ORDERING INFORMATION

PART NUMBER ——— 374H/B CH

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" devices.

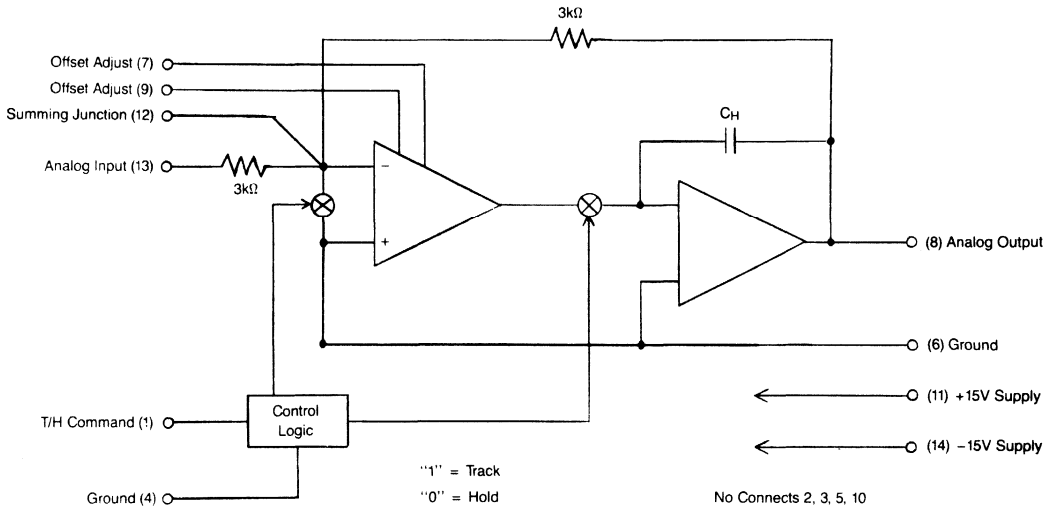
SPECIFICATIONS (T_A = +25°C, ± Vcc = ± 15V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	± 10	± 11		Volts
Input Impedance (Note 2)		3		kΩ
Output Current (Note 1)	± 5			mA
Output Impedance (Note 2)		1		Ω
Maximum Capacitive Load (Note 2)		250		pF
DIGITAL INPUT				
Logic Levels: Logic "1" (Track Mode)	+2.0			Volts
Logic "0" (Hold Mode)			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.7V)			+20	µA
Logic "0" (V_{IL} = +0.4V)			−0.4	mA
TRANSFER CHARACTERISTICS (Note 3)				
Gain		−1		V/V
Gain Linearity Error		± 0.001	± 0.003	%FSR
Gain Accuracy: Initial (+25°C)		± 0.01	± 0.02	%
Drift (Note 6)		± 1	± 5	ppm/°C
Error @ T_{min} or T_{max} (MN374H, H/B)		± 0.02	± 0.07	%
Offset Voltage (Track Mode, Note 4): Initial (+25°C)		± 0.5	± 3	mV
Drift (Note 6)		± 5	± 20	µV/°C
Error @ T_{min} or T_{max} (MN374H, H/B)		± 1	± 5	mV
Pedestal (Note 5): Initial (+25°C)		± 2	± 4	mV
Drift (Note 6)		± 10	± 40	µV/°C
Error @ T_{min} or T_{max} (MN374H, H/B)		± 3	± 8	mV
DYNAMIC CHARACTERISTICS				
Acquisition Time:				
20V Step to ± 0.003% (± 0.6mV)		2.5	4	µsec
20V Step to ± 0.01% (± 2mV, Note 2)		1.5	3	µsec
10V Step to ± 0.003% (± 0.3mV, Note 2)		3		µsec
10V Step to ± 0.01% (± 1mV, Note 2)		1.2		µsec
Track-to-Hold Transient (Note 2):				
Amplitude		200		mV
Settling Time to ± 0.003% FSR (± 0.6mV)		0.5	3	µsec
Settling Time to ± 0.01% FSR (± 2mV)		0.3	2	µsec
Aperture Delay Time (Note 2)		30		nsec
Aperture Jitter (Note 2)		400		psec
Output Slew Rate (Note 2)		± 30		V/µsec
Small Signal Bandwidth (−3dB, Note 2)		1.5		MHz
Full Power Bandwidth (Note 2)		500		kHz
Output Droop Rate: +25°C		± 0.1	± 1	µV/µsec
0°C to +70°C		± 10	± 100	µV/µsec
−55°C to +125°C ("H" Models)		± 50	± 500	µV/µsec
Feedthrough Attenuation (20kHz, 20Vp-p input)	90	100		dB
Output Noise (d.c. to 1MHz, Note 2) Track Mode		200		µV(rms)
Hold Mode		200		µV(rms)
POWER SUPPLIES				
Voltage Range (Note 7)	± 14.5	± 15	± 15.5	Volts
Power Supply Rejection: +15V Supply		± 75		µV/V
−15V Supply		± 75		µV/V
Quiescent Current Drain: +15V Supply		+15	+24	mA
−15V Supply		−11	−13	mA
Power Consumption		390	495	mW

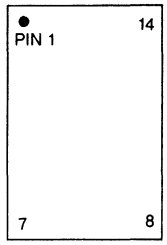
SPECIFICATION NOTES:

1. MN374's output is not short-circuit protected. Continuous shorts to ground or instantaneous shorts to either supply will result in destruction. In normal operation, continuous output current should not exceed ± 10mA.
2. These parameters are listed for reference only and are not tested.
3. FSR stands for full scale range and is equal to 20 Volts for the MN374. ± 0.003%FSR is equivalent to ± ½LSB for a 14-bit system.
4. Initial track-mode offset error is adjustable to zero with a user-optional external potentiometer. The offset adjust may also be used to compensate for pedestal. See Offset Adjustment.
5. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's, pedestal amplitude is a function of input/output voltage level. For the MN374, pedestal is constant regardless of input/output level.
6. MN374 is fully specified for 0°C to +70°C operation. MN374H and MN374H/B are fully specified for −55°C to +125°C operation.
7. MN374 will operate with ± Vcc supplies down to ± 11.4 Volts if input/output voltage is kept below ± 7.5V.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	T/H Command	14	−15V Supply (−Vcc)
2	No Connect	13	Analog Input
3	No Connect	12	Summing Junction
4	Ground	11	+15V Supply (+Vcc)
5	No Connect	10	No Connect
6	Ground	9	Offset Adjust
7	Offset Adjust	8	Analog Output

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from the MN374. The unit's two Ground pins (pins 4 and 6) are not connected to each other internally. They should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible. If your system distinguishes between analog and digital ground, pin 6 may be connected to system analog ground and pin 4 to system digital ground.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines. Input and output signal lines should be kept as short as possible, and if external offset adjustment is used, the potentiometer should be located as close to the unit as possible. If offset adjust is not used, pins 7 and 9 should be left open.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

OFFSET ADJUSTMENT—MN374's track-mode offset error can be reduced to zero using a 10kΩ to 20kΩ potentiometer connected between pins 7 and 9 with its wiper connected to −15V. With the analog signal path grounded, the pot should be adjusted until the output equals zero volts. The pot can also be used to compensate for the effects of pedestal by performing the adjustment in the hold mode. This adjustment is normally made while continually switching from track to hold and observing the T/H output on a scope. This procedure will eliminate adjustment ambiguities resulting from output droop.

TRACK-HOLD COMMAND—A TTL logic "1" applied to pin 1 will put the MN374 into the track (sample) mode. In this mode, the device acts as an inverting unity-gain amplifier, and its output will follow (track) its input. A logic "0" applied to pin 1 will put the MN374 into the hold mode, and after the switching transient settles, the output will be held constant at the level present when the hold command was given.

USING MN374 WITH SUCCESSIVE APPROXIMATION A/D CONVERTERS—Successive approximation (SA) type A/D converters are oftentimes severely analog input slew-rate and bandwidth limited and can easily produce errors when used to digitize dynamically changing signals. These input-signal bandwidth limitations arise from the fact that successive approximation type A/D's sequentially determine output-bit values (from MSB to LSB) by comparing the analog equivalent of output bits already determined to the instantaneous analog input signal. The conversion process demands that the analog input signal remain "constant", and the analog input slew-rate and bandwidth limitations derive from the requirement that input signals not change more than ± ½ LSB (for the appropriate resolution) during the conversion period.

These A/D converter input-bandwidth limitations can be overcome by using track-hold (T/H) amplifiers to track and subsequently "freeze" (hold) analog input signals that are changing too rapidly for the A/D alone to accurately digitize. If other parameters are appropriate, the slew-rate and bandwidth limiting factor of the T/H-A/D combination will become the T/H's aperture jitter (aperture uncertainty), and the T/H-A/D combination will now be able to accurately sample and digitize signals slewing as much as ± ½LSB during the T/H's aperture jitter time. The formulas for determing how fast a signal a given T/H can accurately capture when used in conjunction with a given A/D converter are the same as those stated above with ± ½LSB defined for the A/D converter and with the variable (conversion time) replaced by aperture jitter. Needless to say, aperture jitter is a significantly smaller number than conversion time, and the bandwidth improvement when using the T/H vs. not using the T/H will equal the ratio of A/D conversion time to T/H aperture jitter.

$$\text{Input Slew Rate Limit} = \frac{\pm \frac{1}{2}\text{LSB}}{\text{Conversion Time}}$$

$$\text{Input Bandwidth}^* = \frac{\pm \frac{1}{2}\text{LSB}}{(\text{Conv. Time})(2\pi)(\text{FSR}/2)}$$

$$\text{Input Bandwidth}^* = \frac{(\text{FSR}/2^{n+1})}{(\text{Conv. Time})(2\pi)(\text{FSR}/2)}$$

*For full scale sine waves
FSR = A/D converter full scale range
n = resolution in bits

As an example, consider Micro Networks MN5295 16-bit A/D converter. This device guarantees "no missing codes" to the 14-bit level, and it performs a full 16-bit conversion in 17μsec (maximum). For this device operating on its full ± 10V input voltage range, ± ½LSB/conversion time = ±0.61mV/17μsec = ±0.036mV/μsec (calculated for a 14-bit LSB). This is equivalent to the highest slew rate encountered in a full-scale (± 10V) sine wave with a frequency of 0.57Hz. When used in conjunction with MN5295, MN374 with its 400psec aperture jitter, is capable of capturing signals (to 14-bit accuracy) with slew rates up to ± ½LSB/aperture jitter = ± 0.61mV/400psec = ±1.525V/μsec. This is the highest slew rate one would encounter in a full-scale sine wave with a frequency of 24.3kHz. As expected, the improvement ratio of 24.3kHz to 0.57Hz is equal to the ratio of 17μsec to 400psec.

Using T/H's in conjunction with A/D's to increase analog bandwidth will reduce throughput (conversion rate) in that new digital output data cannot be realized until after the T/H has acquired a new signal (acquisition time) and the A/D has converted it (conversion time). Another consideration when calculating T/H-A/D throughput is the T/H's Track-to-Hold Transient Setting Time. If the same timing pulse is used to put the T/H into the hold mode and initiate the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable and accurate input when it makes the final decision on whether its MSB output should be "1" or "0". This decision normally takes place one clock period after a conversion has begun.

Other considerations when using T/H's with successive approximation A/D's involve the T/H's output stage. In the hold mode, it should exhibit a very low output impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock frequency. Also, the T/H should be able to fully recover (to ± ½LSB) from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the T/H will be required to sink or source high frequency current transients and recover within one clock period. The MN374 output is not current limited, and in the hold mode, output impedance is typically below 1Ω. It recovers from output current transients (to ± 0.003%FSR) in well under 1μsec.

For slower speed A/D converters, the most popular technique used to control the T/H's operation is to drive the T/H directly with the A/D's status line. For virtually all high-resolution A/D's in use today, including MN5295/5296, this technique does *not* work because the T/H's track-to-hold transients will

not reliably settle fast enough. The application described below is a much more cautious way to control the T/H-A/D timing because it uses a timed one-shot to delay the start of the A/D conversion. The circuit allocates a predetermined amount of time for the track-to-hold transient to fully settle before initiating the A/D conversion. After the conversion has been completed, the circuit immediately drives the T/H back into the track mode.

The principles discussed below are general and can be used for virtually any T/H-A/D combination. The system is run by an externally applied clock whose frequency determines the overall sampling/digitizing rate. Please refer to the timing and schematic diagrams below as well as the MN5295/96 data sheet.

The system consists of the A/D, the T/H, a single one-shot and a dual flip-flop. The falling edge of the system clock triggers the 74LS123 one-shot, and the system clock can have any duty cycle as long as it has a minimum positive pulse width of 50nsec to accommodate the setup-time requirement of the one-shot.

The one-shot produces a 500nsec pulse, and both the Q and $\overline{Q}$ outputs are utilized. The Q output becomes the start pulse for the MN5295/5296, and the $\overline{Q}$ output drives the set pin of the first half of the 74LS74 flip-flop. The $\overline{Q1}$ output of the flip-flop controls the operational mode of the MN374 T/H. The falling edge of the $\overline{Q}$ output of the 74LS123 asynchronously sets the flip-flop driving its Q1 output high and its $\overline{Q1}$ output low. The MN374, which has an active-low control line, is immediately driven into its hold mode by the falling edge of $\overline{Q1}$.

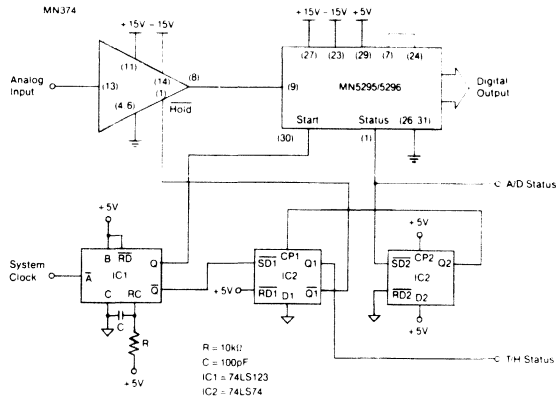
The pulse width of the 74LS123 has been selected so that there is now ample time for the MN374 track-to-hold transient to fully decay before the A/D conversion begins. After 500nsec, the Q output of the one-shot drops to "0" initiating the A/D conversion, and driving the Status output (pin 1) of the A/D to a "1". The T/H remains in hold because the rising edge of the $\overline{Q}$ output of the one-shot does not affect the first flip-flop. The rising edge of Status asynchronously resets the second flip-flop driving the Q2 output low.

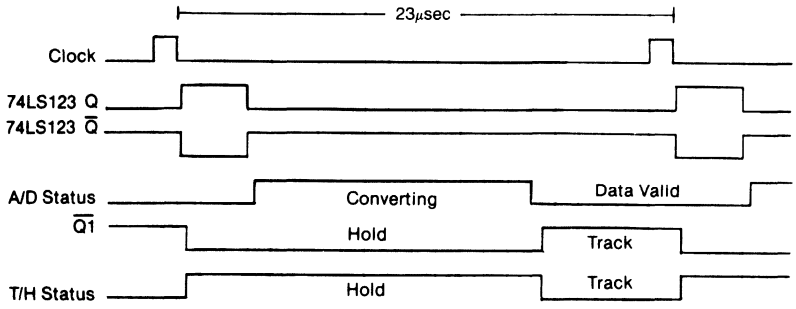
The T/H remains in the hold mode for the next 17μsec as the A/D completes its conversion. At the end of the conversion, the A/D's Status line drops to a "0", and this sets the second flip-flop. The Q2 output goes high clocking the first flip-flop which has a "0" on its D line. This forces the Q1 output low and the $\overline{Q1}$ output high driving the T/H back into the signal-acquisition (track) mode.

The status of this system can be monitored at a number of different points. Whenever pin 1 (Status) of MN5295/5296 is a logic "1", the A/D is performing a conversion, and output data is not valid. The falling edge of this line signals that the conversion is complete and that output data is now valid. The Q1 output of the first flip-flop can be used to monitor the T/H. Whenever this line is a "1", the T/H is in the hold mode. When it is a "0", the T/H is in the track mode. The falling edge here also indicates that a conversion has just been completed and that output data is now valid. If an external latch is to be used to clock data away from MN5295/5296, either of the falling edges described above may be used to strobe the latch.

Remember that the above application does not automatically take care of the T/H acquisition time and that this time must be allowed for in determining the external clock period. If the MN5295/5296 requires 17μsec to make a conversion, and the T/H requires 4μsec for acquisition time, adding 2μsec of overhead time yields a period of 23μsec. That means the system can be clocked at 43kHz and still be guaranteed to meet full accuracy and linearity performance.

It is unnecessary to have the 74LS123 one-shot in the application if the externally applied clock can be made to be a series of 50nsec-wide positive pulses occurring at a 43kHz rate. In other words, if the clock can be made to look like the output of the one-shot in our timing diagram, it is unnecessary to have the one-shot. The clock can drive the MN5295/5296 directly, and it can be inverted to drive the 74LS74.







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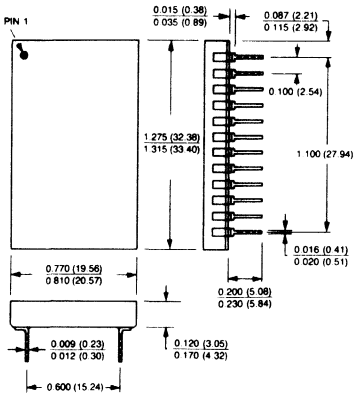
MN376

200nsec
12-Bit LINEAR
TRACK-HOLD AMPLIFIER

FEATURES

- 200nsec Max Acquisition Time 10V Step to ±0.01%
- 100nsec Max Track-to-Hold Settling Time
- ±20psec Aperture Jitter
- Use with MN5245/46 for 1MHz 12-Bit A/D Conversions; with MN5249 for 2MHz
- 78dB Feedthrough Attenuation
- TTL Compatible
- Pin-Compatible MN0300A, HTC-0300A, TP4860
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

24 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN376 is an extremely high-speed track-hold (sample-hold) amplifier. Its 200nsec maximum acquisition time (to ±0.01%) and 100nsec maximum track-to-hold transient settling time enable it to deliver accurate, 12-bit linear, analog samples at a 3.3MHz rate. Its ±5μV/μsec maximum droop rate enables it to hold acquired signals to 12-bit accuracy for periods longer than 200μsec. Its ±20psec aperture jitter (40psec total aperture window) enables it to accurately sample full scale analog signals with frequencies up to 1MHz, while its 16MHz small-signal bandwidth and 300V/μsec slew rate obviously enable it to accurately track much faster smaller-scale signals. In the hold mode, input-output feedthrough attenuation is specified at 78dB (better than ½LSB in 12 bits) at 2.5MHz.

MN376 is designed to be used with Micro Networks high-speed 12-bit A/D's to configure high-throughput, broadband, sampling/digitizing systems. It can be used with MN5245 or MN5246 (850nsec 12-bit A/D's) to configure a bonafide 1MHz sampling A/D with a 500kHz input bandwidth or with MN5249 (400nsec 12-bit A/D) to form a 2MHz digitizer with a 1MHz bandwidth.

Unlike many high-speed T/H's available today, MN376 fully guarantees acquisition time and track-to-hold settling time (a T/H's two throughput limiting specifications) to ±0.01%FS (equivalent to ±0.005% FSR or ±1mV) and not to only ±0.1% or ±1%. A 24-pin dual-in-line package, a gain of −1, an input/output range of ±10V, and TTL compatibility make the MN376 pin compatible with Micro Networks MN0300A, Analog Devices/Computer Labs HTC-0300A, and industry-standard 4860 type high-speed T/H's.

MN376 is designed to be used without external adjustments. Its thin-film nichrome resistors are actively laser trimmed to minimize gain (±0.05%), offset (±0.5mV) and pedestal (±2.5mV) errors. The stability of those resistors minimizes gain (±0.5ppm/°C), offset (±3ppm of FSR/°C) and pedestal (±4ppm of FSR/°C) drifts with temperature. Low power consumption (875mW maximum) enables full 0°C to +70°C (MN376) or −55°C to +125°C (376 H, H/B) ambient operation. Optional MIL-H-38534 screening makes the MN376H/B CH ideal for most military/aerospace high-speed sampling applications.

May 1988

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MN376 200nsec 12-Bit LINEAR T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN376	0°C to +70°C
MN376H, MN376H/B (Note 3)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
±15V Supply Voltage (±V_{CC}, Pins 24, 22)	±18 Volts
+5V Supply Voltage (+V_{dd}, Pin 9)	−0.5 to +7 Volts
Analog Input (Pin 13) (Note 1)	±18 Volts
Digital Inputs (Pins 11, 12)	−0.5 to +5.5 Volts
Output Current (Note 2)	±50mA

ORDERING INFORMATION

PART NUMBER — MN376H/B CH

Standard Part is specified for 0°C to +70°C Operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated)

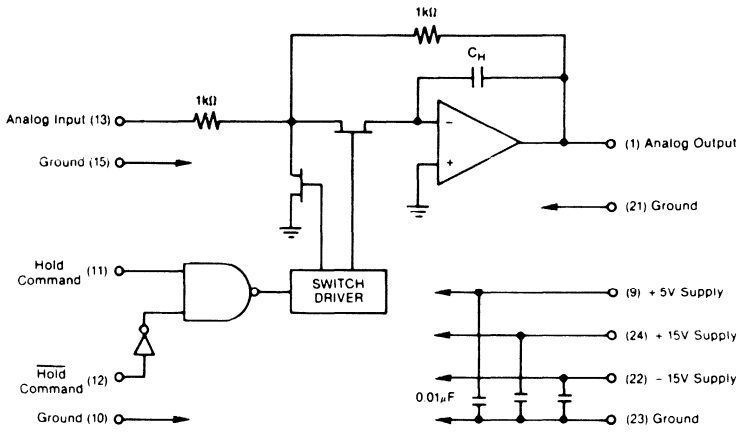
ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±10.25	±11.5		Volts
Input Impedance (Note 10)		1		kΩ
Output Current (Note 2)	±20			mA
Output Impedance (Note 10)		0.1		Ω
Maximum Capacitive Load (Note 10)		100		pF
DIGITAL INPUTS				
Logic Levels (Note 4): Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Loading (Note 5)			1	TTL Load
TRANSFER CHARACTERISTICS				
Gain		−1		V/V
Gain Accuracy		±0.05	±0.1	%
Gain Linearity Error (Note 6)		±0.005	±0.01	%FS
Offset Voltage (Track Mode)		±0.5	±5	mV
Pedestal (Note 7)		±2.5	±20	mV
Stability: Gain Drift		±0.5	±5	ppm/°C
Offset Drift (Track Mode)		±3	±15	ppm of FSR/°C
Pedestal Drift		±5		ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time (Notes 6, 8): 10V Step to ±0.01%FS (±1mV)		160	200	nsec
10V Step to ±0.1%FS (±10mV)		80	170	nsec
10V Step to ±1%FS (±100mV)		60		nsec
5V Step to ±0.01%FS (±0.5mV)		120	160	nsec
1V Step to ±1%FS (±100mV)		60		nsec
Settling Time, Track-to-Hold (Note 9): to ±0.005%FS (±0.5mV)		60	130	nsec
to ±0.01%FS (±1mV)		50	100	nsec
to ±0.1%FS (±10mV)		30		nsec
Track-to-Hold Transient (Note 10)		180		mVp-p
Aperture Delay Time (Note 10)		6		nsec
Aperture Jitter (Note 10)		±20		psec
Output Slew Rate (Note 10)		±300		V/μsec
Small Signal Bandwidth (−3dB, Note 10)		16		MHz
Large Signal Bandwidth (Notes 10, 11): 100kHz		−90		dB
500kHz		−90		dB
1MHz		−84		dB
2MHz		−75		dB
Droop: +25°C		±0.5	±5	μV/μsec
+70°C		±15		μV/μsec
+125°C		±1.2		mV/μsec
Feedthrough Attenuation (20Vp-p input): 100kHz		84		dB
500kHz		84		dB
1MHz		80		dB
2.5MHz	70	78		dB

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Voltage Range: ±15V Supplies +5V Supply		±3 ±5		% %
Power Supply Rejection Ratio		±0.5		mV/V
Quiescent Current Drain: +15V Supply −15V Supply +5V Supply		+21 −22 +17	+25 −25 +25	mA mA mA
Power Consumption		730	875	mW

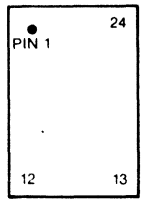
SPECIFICATION NOTES:

1. Analog input signal should not exceed supply voltage.
2. The MN376's output is current limited at approximately ±50mA and can withstand a sustained short to ground. Shorts to either supply will result in destruction. In normal operation, load current should not exceed ±20mA.
3. The MN376H/B is specified for −55°C to +125°C operation and is processed and screened to the requirements of MIL-STD-883, Method 5008.
4. See Applications Information for use of Hold and $\overline{\text{Hold}}$ inputs.
5. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
6. FS stands for Full Scale and is equivalent to 10 volts. FSR stands for Full Scale Range and is equivalent to 20 volts. For a 12-bit system, 1 LSB = 0.024%FSR.
7. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's, pedestal amplitude is a function of input/output voltage level. For the MN376, pedestal is constant regardless of input/output level.
8. Acquisition time is tested with no load and is relatively unaffected by capacitive loads to 50pF and resistive loads to 500Ω.
9. Track-to-hold settling time refers to the time interval between the point at which a device is commanded from the track to the hold mode and the point at which the analog output (following a transient) settles to within a specified error band around its final value.
10. These parameters are listed for reference only and are not tested.
11. Listed specification is the peak of the highest observed harmonic (usually the second) in the output spectrum. Measured in the track mode with a full scale input signal at the frequencies indicated.

BLOCK DIAGRAM



PIN DESIGNATIONS



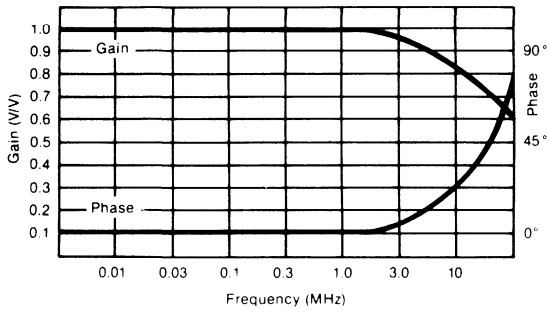
1	Analog Output	24	+15V Supply
2	N/C	23	Ground
3	N/C	22	−15V Supply
4	N/C	21	Ground
5	N/C	20	N/C
6	N/C	19	N/C
7	N/C	18	N/C
8	N/C	17	N/C
9	+5V Supply	16	N/C
10	Ground	15	Ground
11	Hold Command	14	N/C
12	$\overline{\text{Hold}}$ Command	13	Analog Input

APPLICATIONS INFORMATION

GROUNDING AND BYPASSING—With proper grounding and bypassing, the MN376 will meet all its published performance specifications without any additional external components. The device has four Ground pins (pins 10, 15, 21 and 23). All must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the MN376 and have all four ground pins soldered directly to it. Pin 10 is particularly groundnoise sensitive because in the actual construction of the MN376, most of the digital elements that constitute the switch drive circuit are grounded to pin 10. Noise in the switch drive circuit couples directly through to the main op-amp summing junction—the most noise sensitive point in any T/H circuit. Therefore, most digital ground currents will enter or leave the MN376 through pin 10, and in order to keep the output clean, care must be taken to ensure that no ground potentials can exist between pin 10 and the other ground pins. This is why pin 10 must be tied to the analog and not the digital ground system. For the same reason, the +5V digital logic supply (pin 9) should be kept as clean as possible. This supply, as well as the ±15V supplies (pins 24 and 22), is bypassed to ground with 0.01μF ceramic capacitors inside the MN376's package. In critical applications, additional external 0.1μF to 1μF tantalum bypass capacitors may be required.

TRACK-HOLD COMMAND—A TTL logic "0" applied to pin 11 (or a logic "1" applied to pin 12) will put the MN376 into the track (sample) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output will follow (track) its input. A logic "1" applied to pin 11 (or a logic "0" applied to pin 12) will put the MN376 into the hold mode, and the output will be held constant at the level present when the hold command was given. If pin 11 is used to control the MN376, pin 12 must be connected to digital ground. If pin 12 is used to control the MN376, pin 11 must be tied to +5V. Pins 11 and 12 each present 1 TTL load to the digital drive circuit.

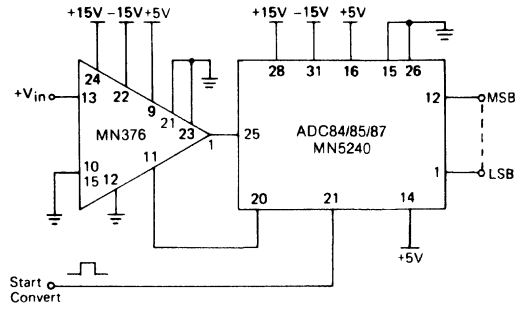
CAPACITIVE AND RESISTIVE LOADING—To avoid possible oscillations, current limiting, and performance variations over temperature, the MN376's output loading has certain restrictions. The maximum capacitive load to avoid oscillation is typically 250pF. Recommended resistive loading is 500Ω (minimum), although values as low as 250Ω may be used. Acquisition and track-to-hold settling times are relatively unaffected by resistive loads down to 500Ω and capacitive loads up to 50pF. Higher capacitances will affect both acquisition and settling time.



Track Mode Gain Amplitude and Phase Response

USING THE MN376 WITH A/D CONVERTERS—There are two important considerations when using T/H's to drive successive approximation A/D's. The first is a dual requirement—the T/H's output stage should exhibit a very low impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock frequency, and the T/H should be able to recover from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the T/H will be required to sink or source large high frequency current transients and recover within one clock period. In the hold mode, the MN376's output impedance is typically 0.1Ω. Its output typically recovers (to ±0.01%) from a 2mA step in less than 100nsec. The second consideration involves the T/H's track-to-hold transient settling time. If the same timing pulse that puts the T/H into the hold mode intitiates the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable accurate input when it makes the final decision on whether its MSB output should be a "1" or "0". This decision normally takes place one clock period after a conversion has begun.

In most applications using the MN376 in front of a successive approximation A/D converter, the MN376's T/H command pin can be driven directly (or inverted if necessary) from the converter's status output. The status output changes state when the converter receives a convert command, and this change can drive the T/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the T/H back into the track mode. The diagram below illustrates an MN376 mated with an ADC85-type A/D in this manner. Since the ADC85's MSB output is not set to its final value until one clock period (approximately 150nsec for the fastest devices in this family) after a conversion begins, the MN376's track-to-hold transient will be completely settled, and no extra timing precautions are necessary.



See the MN5245 12-bit A/D data sheet for information on how to use MN376 to configure a 1MHz, 12-bit sampling A/D with a 500kHz input bandwidth. See the MN5249 data sheet to configure a 2MHz sampling A/D with a 1MHz input bandwidth.

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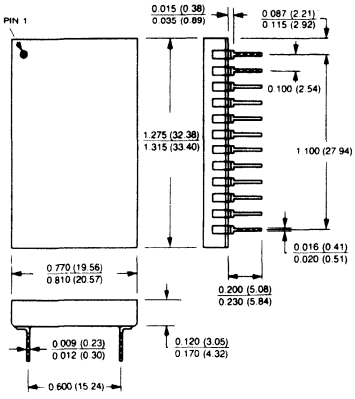
MN379

FLASH-CONVERTER COMPATIBLE T/H AMPLIFIER

FEATURES

- **Designed to Directly Drive Flash Converters**
- **2psec Maximum Aperture Jitter**
- **Capacitive Loads to 500pF**
- **30nsec Max Acquisition Time (1V Step to ±0.1%)**
- **15nsec Max Settling Time**
- **±300V/μsec Min Slew Rate**
- **100MHz Bandwidth**
- **TTL or ECL Compatible**
- **24-Pin DIP**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD 1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN379 is an extremely high-speed track-hold (T/H) amplifier designed to overcome the bandwidth and loading problems associated with many 6-9 bit, high-throughput, flash-type A/D converters. The relatively high aperture uncertainty (jitter) of many higher-resolution flash converters results in correspondingly large accuracy and linearity errors when digitizing high-slew-rate (wide-bandwidth) signals. The result is a reduction in effective-bit resolution. MN379 overcomes this problem with its outstanding 2psec maximum aperture jitter. In such aperture-reducing applications, MN379 can result in a 10 times improvement in the ability to digitize rapidly slewing signals while its 25MHz throughput causes no reduction in overall sampling rate.

An additional problem associated with higher-resolution flash converters is the high capacitive input impedance that often characterizes these devices. MN379 is designed to be unconditionally stable with capacitive loads up to 500pF, and its ability to supply instantaneous output currents up to ±100mA makes its acquisition, settling and bandwidth characteristics relatively unaffected by load.

MN379 has an input/output voltage range of ±2.5V. Its compensated open-loop design architecture gives it a minimum gain of +0.92 and a pedestal guaranteed not to exceed ±20mV. The outstanding 2psec aperture jitter is achieved using a high-speed diode-bridge switching scheme. The track-hold digital input controlling the bridge can be referenced to an external voltage for CMOS or ECL compatibility. An internal reference is supplied for TTL compatibility.

MN379 is packaged in a standard, 24-pin ceramic dual-in-line. Power supply requirements are ±15V and maximum power consumption is 2 Watts. Standard product is fully specified for 0°C to +70°C (case) operation and for military/aerospace applications, is available fully screened to MIL-H-38534 (MN379H/B CH).

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January 1992
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MN379 FLASH-CONVERTER COMPATIBLE T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN379	0°C to +70°C (case)
MN379H, MN379H/B (Note 1)	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply(+Vcc, Pin 23)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 12)	+0.5 to −18 Volts
Analog Input Voltage (Pin 5)	±5 Volts
Digital Input Voltage	
(Pins 2 or 3 to ground)	±15 Volts
Differential Digital	
Input Voltage (Pin 2 to Pin 3)	±5 Volts
Output Current (Note 2)	±35mA

ORDERING INFORMATION

PART NUMBER — MN379H/B CH

- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified −55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

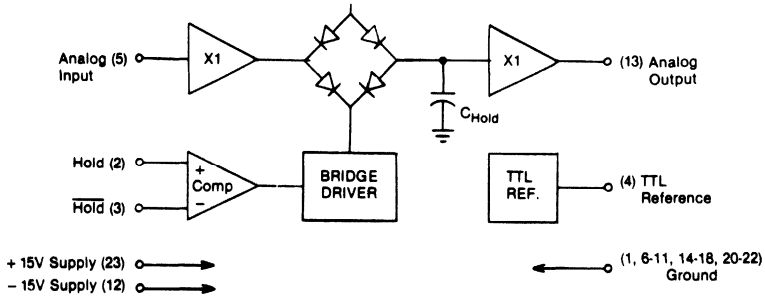
SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V, Z_{Load} = 500Ω // 15pF unless otherwise indicated)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±2.5			Volts
Input Impedance		10 // 5		kΩ // pF
Output Current (Note 2)	±25			mA
Output Impedance		10		Ω
Maximum Capacitive Load	500			pF
DIGITAL INPUTS (Note 3)				
Digital Input Threshold (Pin 2 to Pin 3)	−100		+100	mV
Digital Input Operating Range (Pins 2 and 3 to Ground)	−5.5		+5.5	Volts
Logic Levels (Pin 2 or 3 tied to Pin 4): Logic "1" Logic "0"	+2		+5.5 +0.8	Volts Volts
Logic Currents: Logic "1" Logic "0"			+10 −0.25	μA mA
TTL Reference (Pin 4) Output Voltage	+1.1	+1.25	+1.4	Volts
TTL Reference (Pin 4) Output Impedance		560		Ω
TRANSFER CHARACTERISTICS				
Gain Error: Initial (+25°C) Drift (Note 4)	+0.92	+0.96 ±20	 ±50	V/V ppm/°C
Linearity Error (Full Temperature Range) (Notes 4, 5)		±0.05	±0.1	%FSR
Offset Voltage (Track Mode): Initial (+25°C) Drift (Note 4)		±5 ±100	±10 ±200	mV μV/°C
Pedestal (Note 6): Initial (+25°C, V_{in} = 0V) Drift (Note 4) Variation with V_{in}		±10 ±100 −8	±20 ±200	mV μV/°C mV/V
DYNAMIC CHARACTERISTICS				
Acquisition Time: 5V Step to ±1% (±50mV) 5V Step to ±0.1% (±5mV) 1V Step to ±1% (±10mV) 1V Step to ±0.1% (±1mV)		25 35 15 25	30 40 20 30	nsec nsec nsec nsec
Track-to-Hold Transient: Height (Peak-to-Peak) Settling Time (to ±5mV)		60 10	 15	mV nsec
Aperture Delay Time		5	8	nsec
Aperture Jitter		1	2	psec (rms)
Slew Rate	±300	±400		V/μsec
Small Signal Bandwidth (1Vp-p)		100		MHz
Large Signal Bandwidth (5Vp-p)		25		MHz
Feedthrough Attenuation (@10MHz)	60			dB
Droop Rate: +25°C Over Temperature (Note 4)		±0.5 Doubles Every 10°C	±5	mV/μsec
POWER SUPPLIES REQUIREMENTS				
Power Supply Range	±14.25	±15	±15.75	Volts
Power Supply Rejection		±12	±25	μV/V
Current Drain: +15V Supply −15V Supply		+55 −50	+70 −65	mA mA
Power Consumption		1575	2025	mW

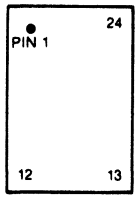
SPECIFICATION NOTES:

1. The MN379 has an approximate 50°C rise of case temperature over still, ambient air temperature.
2. Under normal operating conditions, continuous output current should not exceed ±35mA. The MN379 can withstand a continuous short to ground for approximately 10 seconds. Shorts to either supply will result in destruction.
3. The MN379's Hold and $\overline{\text{Hold}}$ inputs are essentially the direct inputs of a comparator, and the Digital Input Threshold Voltage is effectively the comparator offset. Tying either Pin 2 or Pin 3 to Pin 4 (TTL Reference) will make the other pin TTL compatible. For Pin 2: "0" = Track, "1" = Hold. For Pin 3: "1" = Track, "0" = Hold. Tying either Pin 2 or Pin 3 to other reference voltages can make the MN379 compatible with any logic family.
4. Listed specifications apply over the 0°C to +70°C (case) temperature range for the MN379 and over the −55°C to +125°C (case) temperature range for the MN379H and MN379H/B.
5. Linearity Error is expressed as a percentage of the Full Scale Range (peak-to-peak) of the input/output signal. In an 8-bit system, ½LSB is equivalent to 0.19% FSR. In a 9-bit system, ½LSB is equivalent to ±0.1% FSR.
6. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For the MN379, pedestal amplitude varies linearly with input signal amplitude. The pedestal becomes more negative as the input signal becomes more positive.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Ground	24	Ground
2	Hold Command (Note)	23	+ 15V Supply ($+V_{CC}$)
3	$\overline{\text{Hold}}$ Command (Note)	22	Ground
4	TTL Reference	21	Ground
5	Analog Input	20	Ground
6	Ground	19	N/C
7	Ground	18	Ground
8	Ground	17	Ground
9	Ground	16	Ground
10	Ground	15	Ground
11	Ground	14	Ground
12	− 15V Supply ($-V_{CC}$)	13	Analog Output

Note: Pin 2: "0" = Track, "1" = Hold
Pin 3: "1" = Track, "0" = Hold

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—The large switching currents produced by MN379's diode-bridge switching circuitry make it mandatory to provide a good ground and clean supplies to the device in order to achieve specified speed and accuracy performance. The unit has 16 ground pins (pins 1, 6-11, 14-18, 20-22 and 24). They should all be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large low-impedance, analog ground plane beneath the package.

If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

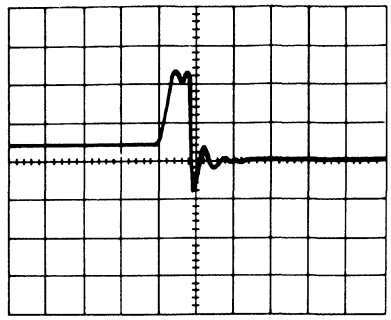
Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination.

Coupling between analog inputs and digital control signals should be minimized to avoid noise pickup. Care should be taken to avoid long analog runs or analog runs in parallel with digital lines.

TRACK-HOLD COMMAND—A logic "0" applied to pin 2 (or a logic "1" applied to pin 3) drives MN379 into the track (sample) mode. In this mode, the device performs as a unity-gain amplifier (follower), and its output follows (tracks) its input. A logic "1" applied to pin 2 (or a logic "0" applied to pin 3) drives MN379 into the hold mode, holding the output constant at the level present when the hold command was given.

MN379's Hold and $\overline{\text{Hold}}$ inputs are essentially the direct inputs of a comparator, and the specification for Digital Input Threshold Voltage is effectively the comparator offset. Tying either pin 2 or pin 3 to pin 4 (TTL Reference) will make the other pin TTL compatible. If, for example, pin 3 ($\overline{\text{Hold}}$) is tied to pin 4 (TTL Reference), a TTL logic "1" (+2.0V minimum) applied to pin 2 will drive MN379 into the hold mode.

Tying either pin 2 or pin 3 to other reference voltages can make MN379 compatible with any logic family. Tying either to −1.3 volts, for example, will make the other ECL compatible.



Scale: Vertical 20mV/div
Horizontal 10nsec/div
Glitch Amplitude: 40mV
Glitch Area: 240mV-nsec

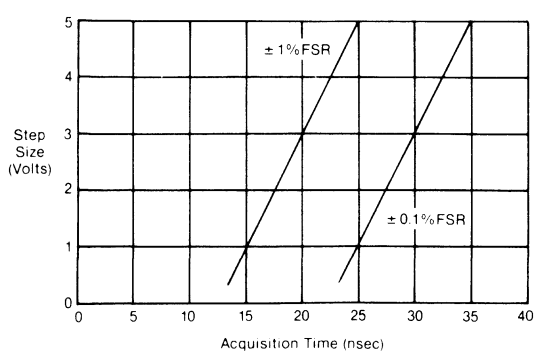
MN379 Typical Track-to-Hold Transient

MN379 ACQUISITION TIME—MN379 acquisition time for any step size settling to ±1%FSR (±50mV) or ±0.1%FSR (±5mV) can be read from the plot below or calculated using the following guidelines. Acquisition time basically consists of the following 4 components:

1) 5nsec gate delay
2) 3nsec output amplifier delay
3) 2.5nsec/volt slew rate
4) 4nsec for settling to ±1%FSR or 14nsec for settling to ±0.1%FSR

The 8nsec total delay for the gate and output amplifier circuits is constant. The total time required for slewing obviously varies as a function of step size, and the settling times are constant independent of step size. Therefore, as demonstrated below, the acquisition time is easily calculated for any step size.

	Typ	Max
5V step to ±1%	(8 + 12.5 + 4)nsec = 25nsec	30nsec
5V step to ±0.1%	(8 + 12.5 + 14)nsec = 35nsec	40nsec
1V step to ±1%	(8 + 2.5 + 4)nsec = 15nsec	20nsec
1V step to ±0.1%	(8 + 2.5 + 14)nsec = 25nsec	30nsec



MN379 Acquisition Time vs. Step Size

DRIVING CAPACITIVE LOADS—As stated earlier, MN379 is designed to directly drive most 6-9 bit flash converters. Such converters often have highly capacitive input impedances, and certain precautions must be taken to optimize MN379 performance with capacitive loads at the megahertz frequencies the device is designed to handle. In particular, the series inductance of the wire or pc card run connecting the output of MN379 to its capacitive load is no longer insignificant. In order to obtain the quickest settling at the load in response to a driving function at the T/H output, it will be necessary to add a series resistor such that the resulting RLC circuit is critically damped. Actually, a slightly underdamped response will settle somewhat faster, but the improvement is not significant. The value of the damping resistor will depend upon the length of wire and the load capacitance.

Critical damping occurs in a series RLC circuit when the resonant radian frequency (ω_0) equals the exponential damping coefficient (α):

Since $\omega_0 = 1/\sqrt{LC}$

and $\alpha = R/2L$

it follows that $R = 2\sqrt{L/C}$

where R is the required value of series resistance, L is the wire inductance and C is the load capacitance. The 10Ω output resistance of the T/H should be subtracted from the calculated value of R since it is effectively in series with the load. In making calculations, an inductance of 23nHy/in. can be assumed for straight, solid wire of AWG 20 to 28, or P.C. runs of 100 to 600 mil² cross-sectional area. This value should also serve as a good starting point for experimentation if other shapes or wire sizes are used. Bear in mind that critical damping only guarantees best settling for a given combination of L and C. There will still be practical limits on the values these can assume if settling is to be accomplished in a reasonable time.

The voltage at the load capacitor will be of the form

$$v(t) = A\{1 - (\alpha t + 1)e^{-\alpha t}\}$$

in response to a step of amplitude A at the T/H output. For settling to ±0.1%, v(t) = 0.999A and, from the equation above, $\alpha t = 9.23$. Since $\alpha = \omega_0 = 1/\sqrt{LC}$, it follows that settling to ±0.1% of the step size occurs at $t = 9.23\sqrt{LC}$.

As an example, assume $C_{LOAD} = 200pF$ and that it is 2.2 inches from the T/H output. This corresponds to a wire inductance of $L = 23nHy/in. \times 2.2in. = 51nHy$. For critical damping, $R = 2\sqrt{L/C} = 32\Omega$. Subtracting 10Ω for the T/H output yields a final value of 22Ω. This resistor should be a carbon or other non-inductive type, and its length will count as part of the inductance to be damped. With C and L as above, the settling time to $\pm 0.1\%$ will be $t = 9.23\sqrt{LC} = 30nsec$.

The actual settling time in any given situation will be somewhat longer than predicted above due to the effects of the settling time of the T/H itself. A very good approximation of the overall settling time can be obtained by assuming the two components add as the square root of the sum of their squares. In the above example, assuming 30nsec settling time for the T/H to $\pm 0.1\%$, this would mean $\sqrt{30^2 + 30^2}$, or about 42nsec total settling from the time a step is applied to the input of the T/H to the time the voltage seen by the A/D settles to $\pm 0.1\%$ of its final value.

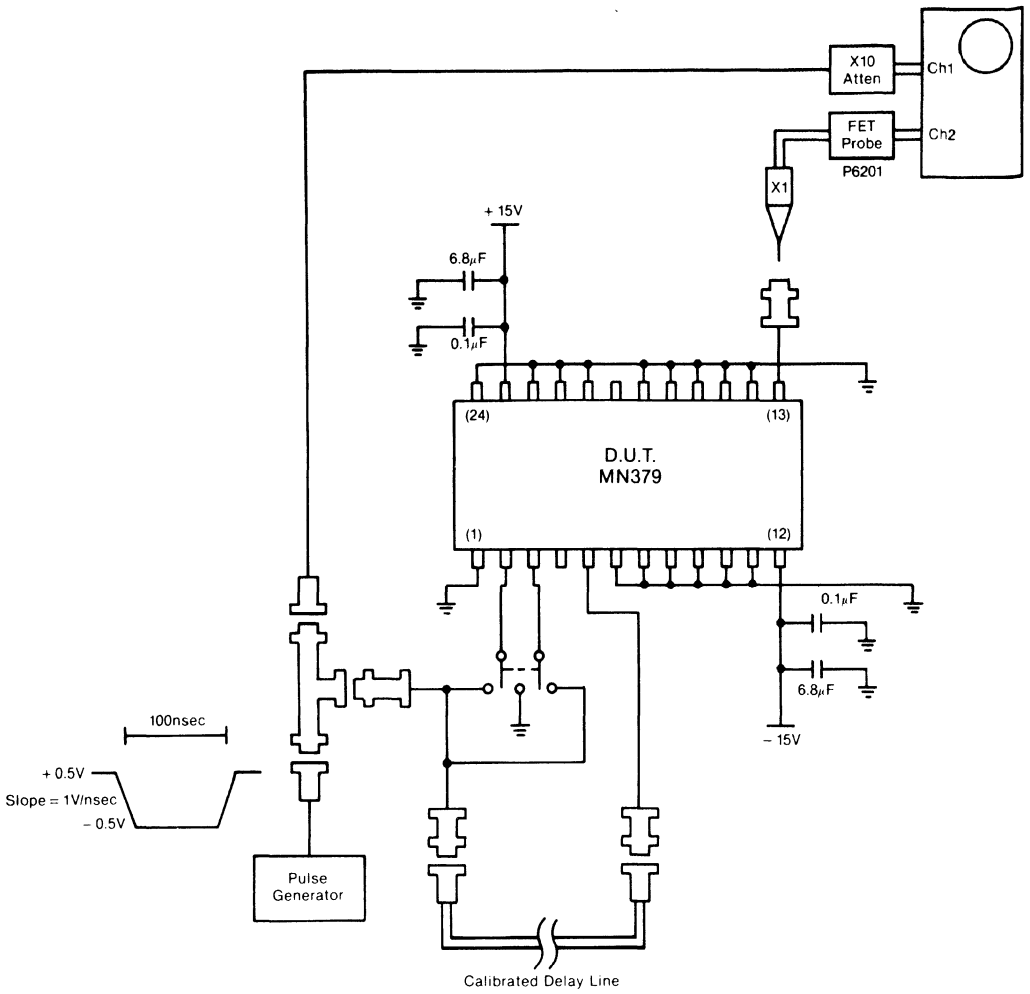
HEAT SINKING — "H" versions of MN379 are fully specified for $-55°C$ to $+125°C$ (case temperature) operation. Because of the device's high internal power dissipation, heatsinking precautions may be necessary to maintain junction temperatures below $+150°C$.

MN379 typically dissipates 1575mW (2025mW maximum). The device has a junction-to-ambient thermal resistance (θ_{JA}) of 34 °C/watt. Therefore, with no heatsinking, MN379's junction-to-ambient temperature differential is typically 53.5 °C. Following the $+150°C$ maximum junction-temperature restriction, the calculated temperature differential dictates that one not operate MN379 in still, ambient air above $+96.5°C$. Note, however, that the unit has a relatively low 7.5 °C/watt junction-to-case thermal resistance (θ_{JC}) that makes the device relatively easy to heatsink.

TESTING APERTURE JITTER—The following method is designed to measure the aperture jitter of the MN379 but, with appropriate modification of the D.U.T. socket pinout, may be used to measure any high-speed track-hold amplifier.

Please refer to the diagram labeled 'Aperture Jitter Test Set-up' for the following procedure. A pulse generator capable of generating pulses with rising and falling edges with slopes on the order of 1 Volt/ns is needed as is a sampling scope and FET probe. The pulse train is used initially to drive the Hold or $\overline{\text{Hold}}$ input of the MN379 (depending upon whether rising edge or falling edge jitter is to be measured). Since the control inputs to the MN379 are fully differential, the unused input is simply connected to ground for a reference and a symmetrical-around-ground input signal is used. The indicated signal levels were chosen so as not to overload the FET probe when used in the X1 mode. Probe noise is too high to get meaningful readings if a X10 attenuator is used. The drive signal is sent to both the sampling scope, to set levels and for triggering, and to a "calibrated delay line". The delay line compensates for aperture delay time and consists of a length of coax selected so that the aperture time (switch opening) of the track and hold occurs at the fastest rising (zero crossing) point of the input waveform. Use of this form of delay ensures no added jitter. The length of the delay line may vary from a few inches to several feet.

Once the delay line has been adjusted properly (this may be confirmed by noting that the "held' voltage is near zero volts), the FET probe is used to measure the input-signal slew rate directly at the D.U.T. input pin (pin 5). This slew rate will most likely be different for the rising vs falling edge so both should be measured. The FET probe is then returned to the Analog Output (pin 13), and the sampling scope is set to view a portion of the held waveform well past the track-to-hold settling transient. A tangential noise measurement is made by observing the width of the noise band on the scope (mVp-p). This reading is then divided by six to get the approximate rms value of the noise. This number, when divided by the slope of the input signal, will give the aperture jitter. If the units used are mV and volts/ns the calculated jitter will be in picoseconds (rms). A slightly more accurate measurement may be obtained by subtracting the contribution of system noise to overall output noise. This may be measured by observing the output on the oscilloscope while the D.U.T. is in the track mode.



Aperture Jitter Test Setup

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MICRO NETWORKS

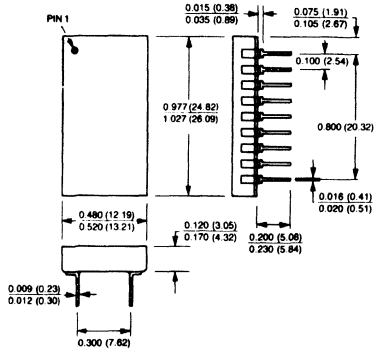
MN2020

DIGITALLY CONTROLLED
PROGRAMMABLE-GAIN
AMPLIFIER

FEATURES

- **Programmable Gain 1 to 128 in 8 Steps**
- **Gain Selected with a 3-Bit TTL Word**
- **Excellent Gain Accuracy: ±0.002% @ G=1 ±0.1% @ G=128**
- **Low Offset Voltage Drift ±5μV/°C**
- **High Input Impedance 1000 MΩ**
- **Small 18-Pin DIP**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN2020 is a precision hybrid amplifier whose gain can be set to any one of 8 levels (1 to 128) with the application of a single 3-bit digital word (TTL logic levels) to its gain control inputs. This programmable-gain amplifier may be operated under direct computer or microprocessor control to provide fully automated, gain-range data acquisition.

The use of internal, laser-trimmed thin-film resistors result in excellent gain accuracy, linearity and drift characteristics. In addition, MN2020 has 100kHz of full power bandwidth and 5MHz of small signal bandwidth resulting in a rapid settling time of 5μsec for a 20 volt step (@G=1).

The MN2020 Programmable-Gain Amplifier is packaged in a hermetically sealed, 18-pin dual-in-line package. The standard device is fully specified for either 0°C to +70°C or −55°C to +125°C ("H" model) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN2020H/B CH is fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

MN2020 is an excellent choice for requirements where stable accurate gains are necessary. Typical applications include microprocessor-based data acquisition systems that have to handle a wide dynamic range of analog inputs. MN2020 may be combined with Micro Networks MN7130 Multiplexed Track-Hold Amplifier and MN574A Microprocessor Interfaced A/D Converter to create a 16-channel, 12-bit, microprocessor-interfaced data acquisition system capable of accepting analog inputs from ±78mV to ± 10V full scale (19-bit dynamic range). Additional applications can be found in autoranging analog-to-digital conversion systems requiring wide dynamic ranges and in systems that autorange under program control.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

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MN2020 DIGITALLY CONTROLLED PROGRAMMABLE-GAIN AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Specified Temperature	0°C to +70°C
	−55°C to +125°C ("H" Model)
Storage Temperature	−65°C to +150°C
+15V Supply (Pin 16)	−0.5 to +18 Volts
−15V Supply (Pin 6)	+0.5 to −18 Volts
+5V Supply (Pin 5)	−0.5 to +18 Volts
Analog Input (Pin 10)	±15 Volts
Digital Inputs (Pins 2-4)	0 to +Logic Supply (Note 1)

ORDERING INFORMATION

PART NUMBER — **MN2020/H/B CH**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

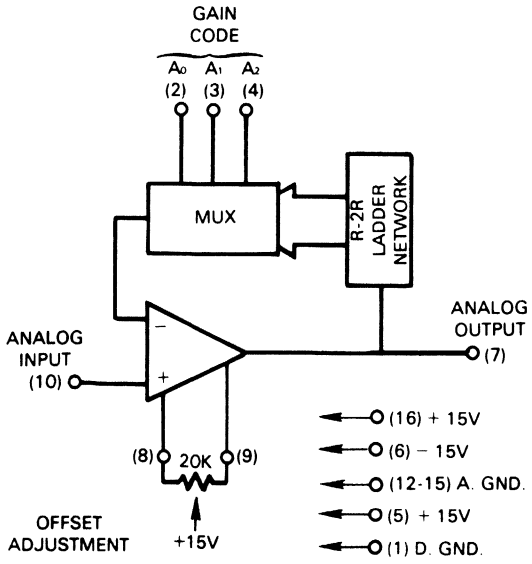
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A=+25°C, Supply Voltages ±15V, unless otherwise specified).

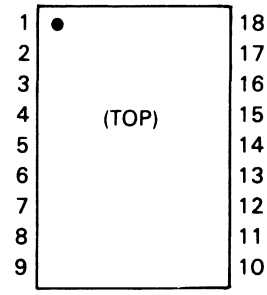
GAIN	MIN.	TYP.	MAX.	UNITS
Fixed Gain Settings		1, 2, 4, 8, 16, 32, 64, 128		
Gain Nonlinearity (Note 2): G = 1		±0.002	±0.005	% FSR (Note 3)
G = 128		±0.04	±0.08	% FSR
Gain Accuracy (Note 4) G = 1: +25°C		±0.002	±0.005	%
0°C to +70°C		±0.003	±0.008	%
−55°C to +125°C		±0.004	±0.01	%
G = 128: +25°C		±0.1	±0.2	%
0°C to +70°C		±0.1	±0.2	%
−55°C to +125°C		±0.2	±0.4	%
INPUT CHARACTERISTICS				
Input Impedance		1000		MΩ
Input Voltage Range (@G=1)		±12		V
Offset Voltage (RTI) (Notes 5 and 6)				
Initial 25°C		100		μV
Drift vs. Temperature −55°C to +125°C		5		μV/°C
Input Bias Current: +25°C		± 20	±200	pA
0°C to +70°C		± 3	± 10	nA
−55°C to +125°C ("H" Model)		±150	±500	nA
Voltage Noise (RTI)				
G=128 (0.1 to 10 Hz)		5		μVp-p
OUTPUT CHARACTERISTICS				
Output Voltage Swing	±10	±12		V
Output Current			5	mA
DYNAMIC CHARACTERISTICS				
Small Signal Bandwidth				
G=1		5		MHz
G=128		40		KHz
Full Power Bandwidth (@G=1)		100		KHz
Slew Rate		12		V/μSec
Output Settling Time to ±0.1% 20V Step (Note 7)				
G=1		5	75	μSec
G=128		65		μSec
GAIN SWITCHING				
Gain Control Logic Inputs				
Logical 1	+4.0			V
Logical 0			+0.8	V
Loading		1		μA
Gain Switching Time (Note 8)		0.6		μSec
POWER SUPPLY REQUIREMENTS (V_{OUT}=0)				
Power Supply Range		±15	±18	V
Current Drain (Analog Supply)		±9.2	±18	mA
Power Consumption		275	540	mW

Note 1: Digital inputs should not exceed logic supply level. Logic supply (pin 5) must be at least +5V to maintain logic levels.
Note 2: See definition of gain nonlinearity on Page 3.
Note 3: FSR = Full Scale Range. If output swing = ±12V, FSR = 24V.
Note 4: Measured between endpoints of input (output) range in order to negate the effects of the offset voltage.
Note 5: RTI = Referred to Input.
Note 6: Externally adjustable to zero.
Note 7: For each gain value, the magnitude of the input step was chosen to make the output step 20V.
Note 8: Between any two gain values.

BLOCK DIAGRAM



PINNING



1. DIGITAL GND.
2. A_0
3. A_1
4. A_2
5. +15 VOLTS (DIGITAL)
6. −15 VOLTS
7. ANALOG OUTPUT
8. OFFSET ADJ.
9. OFFSET ADJ.
10. ANALOG INPUT
11. NO CONNECTION
12. ANALOG GND.
13. ANALOG GND.
14. ANALOG GND.
15. ANALOG GND.
16. +15 VOLTS (ANALOG)
17. NO CONNECTION
18. NO CONNECTION

PROGRAMMABLE GAIN AMPLIFIER
SPECIFICATION DEFINITIONS

GAIN—The ratio of the amplitude of output signal voltage to the amplitude of input signal voltage.

GAIN ACCURACY—Either the percentage that actual gain differs from ideal gain (%) or the amount that the output, at a certain gain and input level, differs from the ideal value (volts, % FSR).

GAIN NONLINEARITY—Maximum deviation of the input-output voltage transfer function from the ideal, expressed as a percentage of the full output voltage range (FSR).

GAIN SWITCHING TIME—The time necessary for the amplifier gain to settle to within 0.1% of its new value following the appearance of a new digital code at its gain coding terminals.

INITIAL OFFSET VOLTAGE (Referred to Input)—The collection of internal voltage offsets summed and treated as a single offset voltage source appearing in series with the input. This offset, multiplied by the programmed gain, will appear at the amplifier output, even when the input signal is zero. This offset voltage can normally be zeroed out with an external trimpot.

INITIAL OFFSET VOLTAGE (RTI) DRIFT vs TEMPERATURE—Drift in initial offset voltage resulting from temperature variations. Usually expressed as V/°C or ppm of FSR /°C.

INPUT BIAS CURRENT—The current drawn into (or out of) the input terminals of the amplifier when the amplifier is turned on and the input signal is zero (input grounded).

INPUT IMPEDANCE—Total impedance seen looking into the amplifier input terminal (with the load connected) with respect to analog ground.

LOADING—The apparent load that the digital gain coding inputs of the amplifier present to their driving circuits. Usually expressed as standard logic loads (e.g. 3 TTL Loads) or in terms of the current sourced or sank when the input is a logic "0" or "1".

OUTPUT DRIVE CURRENT—Current that the amplifier will source or sink to the load while remaining within specification.

OUTPUT VOLTAGE SWING—Maximum allowable output excursion for faithful reproduction of the input signal. This is limited to several volts less than the associated power supply voltage range.

SETTLING TIME—The interval from the application of either an input step at a fixed gain or a new gain code at a fixed input level to the output's settling within a specified error band (usually 0.1%) of its final value.

SMALL SIGNAL BANDWIDTH—Frequency at which the amplifiers gain drops 3 dB from its D.C. value.

SLEW RATE—Maximum rate of change (V/Sec) in the output in response to a step change at the input or a gain change.

VOLTAGE NOISE (RTI) — Sum of the internal noise sources treated as a single source appearing in series with the input signal. The noise, multipled by the programmed gain, will appear at the amplifier output. Voltage noise is dependent upon bandwidth and may be reduced by using the minimum bandwidth necessary for a given application.

TYPICAL CHARACTERISTICS
(TA=25°C, Supplies ±15V)

GAIN CODES AND SETTLING TIMES

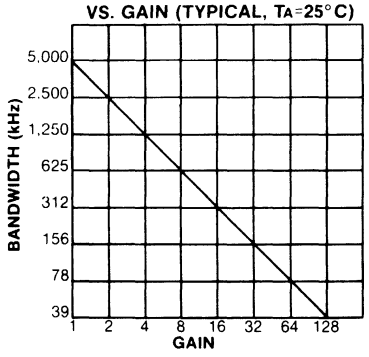
GAIN	DIGITAL CODE A2	A1	A0	OUTPUT SETTLING TIME* (±0.1% 20V Step)
1	0	0	0	2.5 μSec
2	0	0	1	3 μSec
4	0	1	0	4 μSec
8	0	1	1	6 μSec
16	1	0	0	8 μSec
32	1	0	1	17 μSec
64	1	1	0	33 μSec
128	1	1	1	65 μSec

*For each gain value the magnitude of the input step was chosen to make the output step 20V.

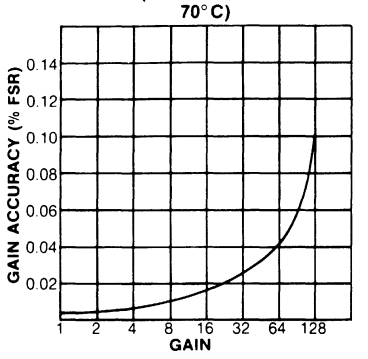
GAIN ACCURACIES

GAIN	ACCURACY (%)					
	25°C		0°C to 70°C		−55°C to +125°C	
	TYPICAL	MAX.	TYPICAL	MAX.	TYPICAL	MAX.
1	0.002	0.005	0.003	0.008	0.004	0.010
2	0.005	0.015	0.005	0.020	0.008	0.020
4	0.005	0.015	0.005	0.020	0.015	0.040
8	0.010	0.020	0.015	0.040	0.020	0.080
16	0.020	0.030	0.020	0.040	0.025	0.080
32	0.020	0.040	0.020	0.040	0.040	0.100
64	0.040	0.100	0.040	0.100	0.100	0.300
128	0.100	0.200	0.100	0.200	0.200	0.400

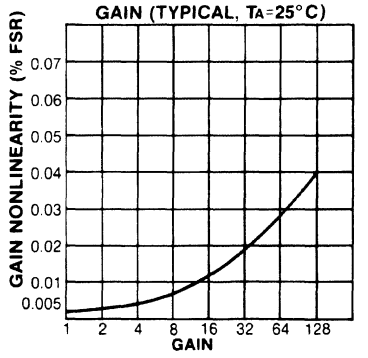
SMALL SIGNAL BANDWIDTH VS. GAIN (TYPICAL, TA=25°C)



GAIN ACCURACY VS. GAIN (TYPICAL, TA=0°C to 70°C)



GAIN NONLINEARITY VS. GAIN (TYPICAL, TA=25°C)

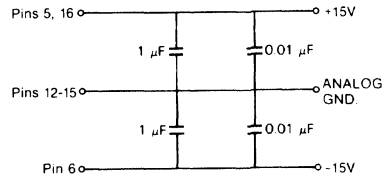


APPLICATIONS INFORMATION:

OFFSET ADJUSTMENT:
The MN2020 meets all specifications without adjustment. However, the initial offset voltage may be adjusted to zero with the addition of a trimpot between pins 8 and 9 as shown in the block diagram. A 20K, 10 turn, <100 ppm/°C TC trimpot should be used to minimize drift with temperature.

LAYOUT CONSIDERATIONS:
Proper attention to layout and decoupling is necessary to obtain specified accuracies. Analog and digital grounds are not connected internally. The four (4) analog commons (pins 12-15) and the digital common (pin 1) should be tied together as close to the package as possible, preferably to a large ground plane underneath the package. If these commons must be run separately, wide conductor runs should be used.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the device package. For optimum results, 1μF capacitors paralleled by 0.01 μF ceramic capacitors should be connected as shown in the adjacent diagram.



INTERFACING THE MN2020 TO POPULAR MICROPROCESSORS

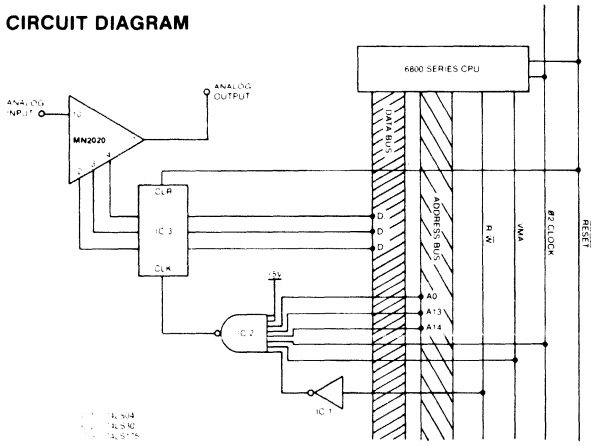
The MN2020 can be easily interfaced to microprocessors for fully automated data acquisition or other applications where it is desirable to change gain under program control. Memory mapped I/O is recommended to take advantage of the powerful memory reference instructions available in most microprocessor instruction sets. Detailed information is provided below for the 6800 Series and 8080 Series processors. Interfacing to other processors would be similar.

INTERFACING TO 6800 SERIES MICROPROCESSORS

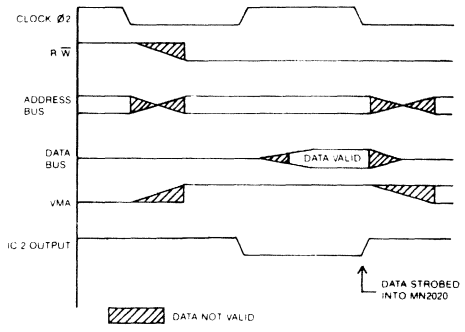
Wiring and Timing Diagrams for interfacing the MN2020 with the 6800 family of microprocessors are shown in Figure 1. In this example, the MN2020's gain control inputs are addressed and written to as a memory location with the gain code in the three lowest order bits (D_0, D_1, D_2) of the accumulator. The address bus connections shown (A14, A13, and A0) correspond to memory address 6001 hexadecimal. Redundant addressing of the MN2020 would occur at any address containing the bit combination A14, A13, A0. The MN2020 may only be written to; attempts to read the memory address assigned to the MN2020 will result in indeterminate (floating CMOS inputs) data.

The connections to the VMA, Ø2 clock and R/$\overline{W}$ lines are used to insure correct timing and to prevent spurious data that may be present on the address bus during non-memory transfer operations from addressing the MN2020. When connected as shown, the MN2020 will be reset to a gain of 1 by a reset pulse from the hardware reset control line of the 6800 System.

CIRCUIT DIAGRAM



TIMING DIAGRAM

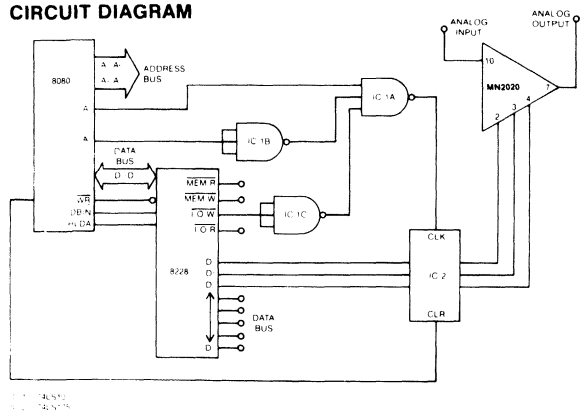


INTERFACING TO 8080 SERIES MICROPROCESSORS

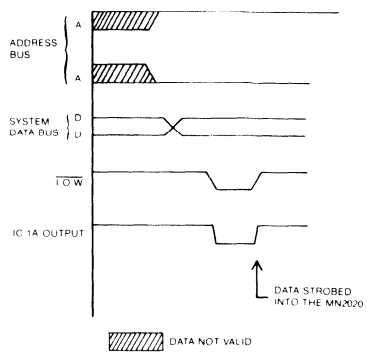
Wiring and Timing Diagrams for interfacing the MN2020 with the 8080 family of microprocessors are shown in Figure 2. In this example, an 8228 system controller is used, and the MN2020 is treated as a standard I/O device. The gain code is written, as an output instruction, to the MN2020 which is located at I/O address 80 hexadecimal.

When the values of A7, A0, and $\overline{\text{I/O W}}$ are "1", "0" and "0" respectively, the output of IC 1A will go to logic zero. When either of the address or $\overline{\text{I/O W}}$ outputs leaves the above state, the output of IC2 is forced to a logic one, with the rising edge triggering the latch IC2 which strobes the gain code information into the MN2020.

CIRCUIT DIAGRAM

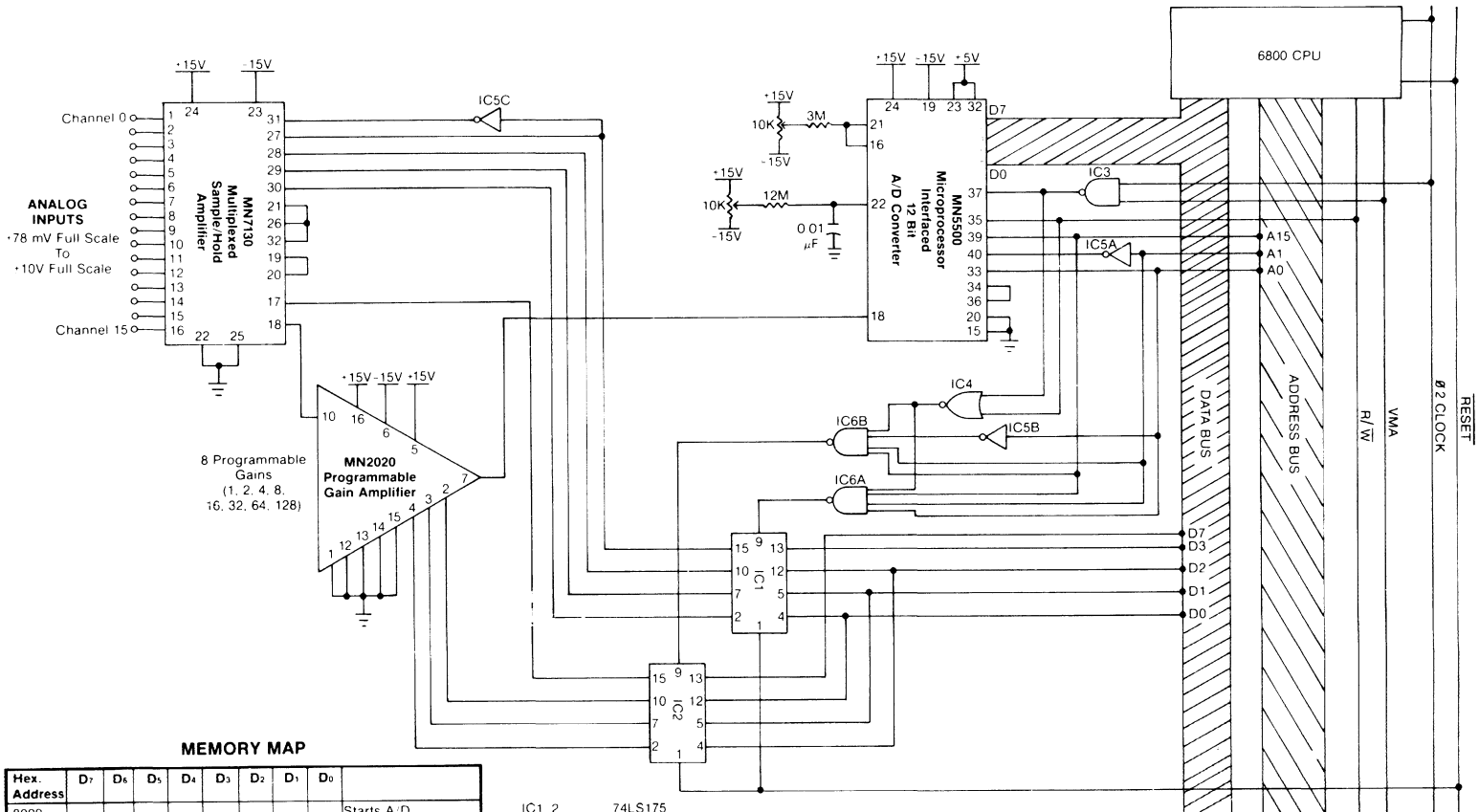


TIMING DIAGRAM



12 Bit—16 Channel Data Acquisition System

WITH 19 BITS OF DYNAMIC RANGE AND AUTORANGING CAPABILITY



MEMORY MAP

Hex. Address	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
8000 (Write)	X	X	X	X	X	X	X	X	Starts A/D Converter
8001 (Read)	"1"	"1"	"1"	"1"	MSB	Bit 2	Bit 3	Bit 4	Digitized Data MSB Byte
8000 (Read)	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	LSB	Digitized Data LSB Byte
8002 (Write)	S/H	X	X	X	X	A_2	A_1	A_0	PGA Gain S/H Command
8003 (Write)	X	X	X	X	A_3	A_2	A_1	A_0	Multiplexed S/H—Channel Address

IC1, 2	74LS175
IC3	74LS00
IC4	74LS02
IC5	74LS04
IC6	74LS20

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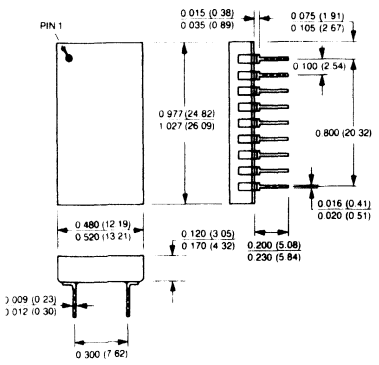
MN2200

HIGH-PERFORMANCE
INSTRUMENTATION AMPLIFIER

FEATURES

- **Internal Gain Setting Resistors for G=1, 10, 100, 1000**
- **Excellent Gain Accuracy:**
  ±0.1% G=100 +25°C
  ±0.16% G=100 +85°C
  ±0.3% G=100 +125°C
- **Low Offset Voltage Drift ±0.6μV/°C @ G=100**
- **Small 18-Pin DIP**
- **Full Mil Operation −55°C to +125°C**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN2200 is a high-performance hybrid instrumentation amplifier in a small, 18-pin, ceramic dual-in-line package. Internal, laser-trimmed, thin-film resistors provide user-selectable gains of 1, 10, 100 and 1000. The internal gain setting resistors provide much better accuracy over temperature than conventional designs requiring an external gain setting resistor. A single external resistor may also be used for gain adjustment in applications calling for gains between the fixed ranges.

An additional unique feature of MN2200 is its user-optional, two-pole Butterworth filter. Two external capacitors can be used to set the breakpoint of this lowpass filter from full bandwidth to well below 1Hz.

MN2200 has a typical input offset voltage of ±100μV at +25°C, and this can be adjusted to zero with an external trimpot. Input offset voltage drift with temperature is an extremely low ±1.5μV/°C at G=10 and drops to ±0.5μV/°C at G=1000. In addition, MN2200 offers 7kHz of full power bandwidth, 1000MΩ input impedance, and has only ±5nA of input bias current.

The standard device is fully specified for either −25°C to +85°C or −55°C to +125°C ("H" model) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN2200H/B is available with Environmental Stress Screening.

Typical applications for MN2200 include: amplifying strain guages, thermocouples and other low-output transducers; high-accuracy data acquisition systems and biomedical instrumentation.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

January 1992
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MN2200 HIGH-PERFORMANCE INSTRUMENTATION AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55° C to +125° C
Specified Temperature	−25° C to +85° C (Standard)
	−55° C to +125° C ("H" Model)
Storage Temperature	−65° C to +150° C
+Vcc Supply (Pin 12)	+18 Volts
−Vcc Supply (Pin 6)	−18 Volts
Differential Input (Pin 2 to Pin 16)	±30 Volts
Analog Inputs (Pins 2, 16)	±Vcc
Output Short Circuit	Protected

ORDERING INFORMATION

PART NUMBER — **MN2200H/B**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

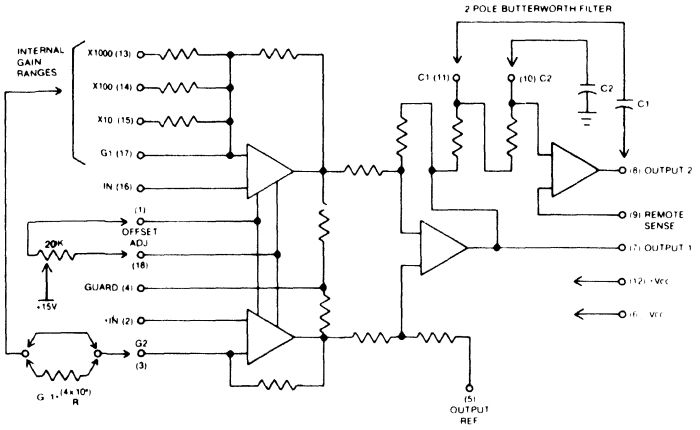
SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V unless otherwise indicated)

FIXED GAIN LEVELS (Note 4)	G=1		G=10		G=100		G=1000		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Gain Accuracy*: +25° C	±0.005	±0.01	±0.03	±0.1	±0.03	±0.1	±0.05	±0.1	%
−25° C to +85° C	±0.01	±0.02	±0.06	±0.16	±0.06	±0.16	±0.14	±0.45	%
−55° C to +125° C ("H" Model)	±0.02	±0.04	±0.1	±0.25	±0.15	±0.3	±0.25	±0.6	%
Gain Nonlinearity: +25° C	±0.001	±0.002	±0.002	±0.005	±0.002	±0.005	±0.02	±0.05	%
−25° C to +85° C	±0.002	±0.005	±0.005	±0.01	±0.005	±0.01	±0.05	±0.1	%
−55° C to +125° C ("H" Model)	±0.004	±0.01	±0.01	±0.02	±0.01	±0.02	±0.1	±0.2	%

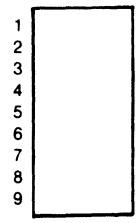
INPUT CHARACTERISTICS	MIN	TYP	MAX	UNITS
Input Impedance				
Differential	1000			MΩ
Common mode	1000			MΩ
Input Voltage Range				
Differential	±10			V
Common mode	±10	±13		V
Common Mode Rejection Ratio				
G=100 DC—10 Hz		110		dB
Offset Voltage (referred to input)*				
Initial @ G=100 (Note 1)		±100	±200	μV
Drift vs. Temperature (Note 2)*				
G=1		10	20	μV/°C
G=1000		0.5	2	μV/°C
1<G<1000		±(10/G)+0.5		μV/°C
vs. Supplies				
G=1		10		μV/% Supply
G=1000		0.5		μV/% Supply
Voltage Noise (referred to input)				
G=1 (0.1 to 10 Hz)		2.0		μVp-p
G=1000 (0.1 to 10 Hz)		0.6		μVp-p
Input Bias Current				
Initial 25° C		±5	±7	nA
Drift		12		pA/° C
Input Offset Current				
Initial 25° C		±5	±7	nA
Drift		12		pA/°C
OUTPUT CHARACTERISTICS				
Output Voltage Swing	±12	±13		V
Output Drive Current	±5	±10		mA
Output Impedance		0.2		Ω
Output Load Capacitance		250		pf
DYNAMIC CHARACTERISTICS				
Slew Rate		0.25		V/μSec.
Small Signal Bandwidth				
G=1		750		KHz
G=100		7		KHz
G=1000		700		Hz
Settling time to 0.01%, 10V step				
G=1, 10		50		μSec.
G=100		200		μSec.
G=1000		1500		μSec.
POWER REQUIREMENTS				
Power Supply Range	±5	±15	±18	V
Current Drain +Vcc*		+8	+15	mA
Current Drain -Vcc*		-8	-15	mA
Power Consumption		240	450	mW

NOTES: 1. Externally adjustable to zero.
2. Verified by testing at −25, +25, and +85° C.
3. *Parameters 100% tested. Other parameters guaranteed by design.
4. Gain can be set to any level between 1 and 1000 with a single external resistor.

BLOCK DIAGRAM



PINNING

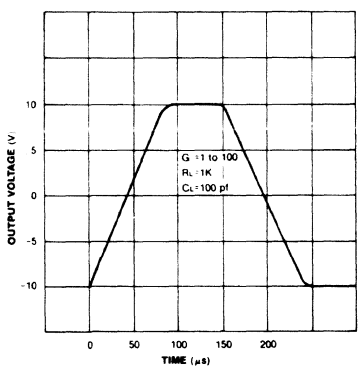


1 OFFSET ADJ.	10 C2 (FILTER)
2 + INPUT	11 C1 (FILTER)
3 GAIN 2	12 +Vcc
4 GUARD	13 X1000
5 OUTPUT REF.	14 X100
6 -Vcc	15 X10
7 OUTPUT 1	16 - INPUT
8 OUTPUT 2	17 GAIN 1
9 REMOTE SENSE	18 OFFSET ADJ.

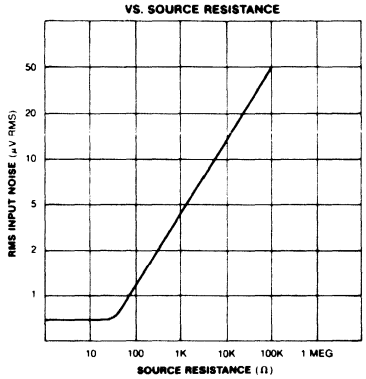
TYPICAL CHARACTERISTICS

(T_A=25° C, Supplies ±15V)

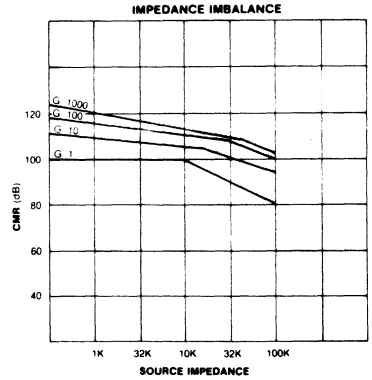
STEP RESPONSE



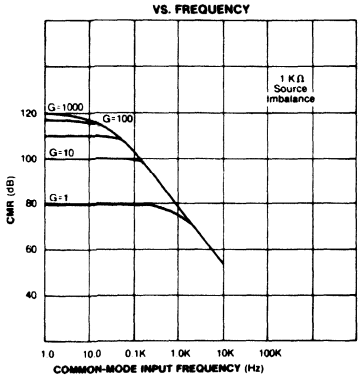
RMS INPUT NOISE VOLTAGE VS. SOURCE RESISTANCE



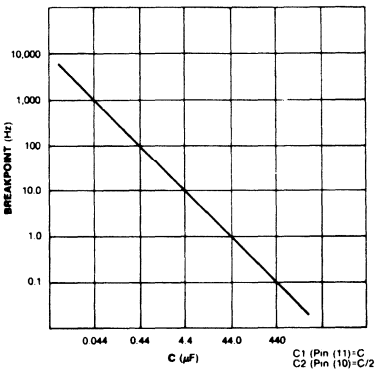
CMR VS. SOURCE IMPEDANCE IMBALANCE



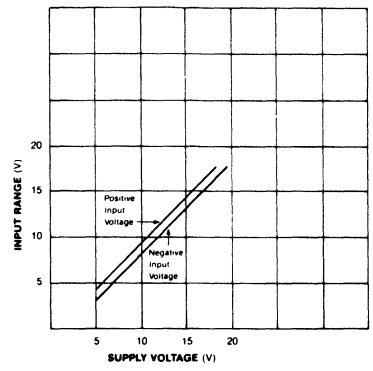
COMMON MODE REJECTION VS. FREQUENCY



FILTER BREAKPOINT



INPUT RANGE FOR LINEAR RESPONSE



MN2200

INSTRUMENTATION AMPLIFIERS

ADVANTAGES:

Instrumentation Amplifiers are committed, closed loop, gain blocks that offer significant performance advantages over simple operational amplifiers.

The principle advantages provided by Instrumentation Amplifiers are:

- Very high input impedance that is independent of gain.
- Very high common mode rejection ratios.
- High accuracies.
- Low Drifts.
- Addition of guard and reference terminals to compensate for noise and external wiring resistance.
- Immunity to temperature variations.

APPLICATIONS:

Instrumentation Amplifiers are used to accurately amplify high impedance low level signals, in the presence of noise and common mode voltages.

Typical applications include:
Amplifying thermocouples, strain gauges and other low level transducers, high accuracy data acquisition systems and biomedical monitoring.

APPLICATIONS INFORMATION:

GAIN SETTING:

The MN2200 includes internal laser trimmed thin film resistors for gains of 1, 10, 100, and 1000. These internal resistors track very closely with the other resistors in the amplifier providing superior performance over temperature, and should be used whenever possible.

Connections for internal gain selection are as follows:

Gain	Connect Pin to Pin
1	No connection
10	15 to 3
100	14 to 3
1000	13 to 3

In addition, the gain can be set to any value>1 with the addition of a single resistor connected between pins 3 and 17. Specifications will be gradually degraded for gains in excess of 1000.

This gain setting resistor should be low TC (<10 ppm/°C) metal film for best performance.

The value of the external gain setting resistor is defined by,

$$\text{Gain} = 1 + \frac{(4 \times 10^4)}{R}$$

The gain error of the above equation is typically 0.1% and a maximum of 0.5% for gains>1.0. Gain drift with temperature will be less than 0.006%/°C if resistors with TC's of 10 ppm/°C or less are used.

OFFSET ADJUSTMENT:

The MN2200 meets all specifications without adjustment. However, the initial offset voltage (200 μV max. referred to input) may be adjusted to zero with the addition of a trimpot between pins 1 and 18 as shown in the block diagram. A 10 turn <100 ppm/°C TC trimpot should be used for best performance.

GUARD TERMINAL:

The MN2200 incorporates a guard (Pin 4) to drive the input cable shield when long input runs are necessary. The use of the guard and shielded input cable greatly reduces the effects of common mode voltages and induced noise and is recommended for noisy environments and input lead runs of more than a few inches.

REMOTE SENSE:

Another feature of the MN2200 is the Remote Sense Terminal. The Remote Sense is used to eliminate the effects of external lead resistance and insure that an accurate output voltage is present at locations remote from the actual instrumentation amplifier.

OUTPUT REFERENCE:

The MN2200's Output Reference Terminal can be used in conjunction with the Sense Terminal to provide accurate output voltages at locations remote from the instrumentation amplifier.

The Output Reference can also be used to offset the instrumentation Amplifier's output by a fixed amount. Any voltage applied between analog ground and the Output Reference will appear as a fixed offset in the output. When used as an offsetting input, the Output Reference is a 20 k Ohm Resistive load. If not used to offset the output, the Output Reference Terminal should be connected to analog ground.

OPTIONAL 2 POLE BUTTERWORTH FILTER:

A unique feature of the MN2200 is the internal two pole Butterworth filter. Two external capacitors applied to pins 10 and 11 set the breakpoint of this filer from full bandwidth to well below 1 Hz.

The breakpoint of the filters is defined by:

$$f\,(\text{Hz}) = \left(\frac{44}{C(\mu f)}\right) \qquad C_1\,(\text{Pin } 11) = C \qquad C_2\,(\text{Pin } 10) = C/2$$

OUTPUTS:

The MN2200 has two analog outputs: pins 7 and 8. Normally the Pin 8 output, which includes the optional filter stage, is used. A slight improvement in offset drifts may be achieved at gains < 10 by using the pin 7 output.

The pin 8 output must be used if remote sensing is employed.

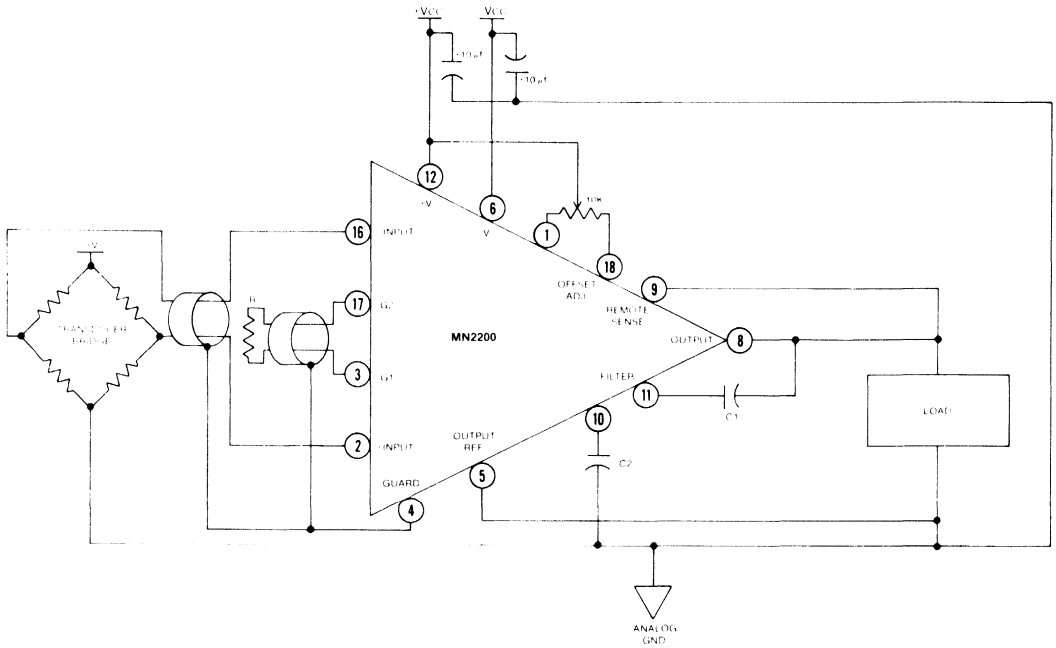
GENERAL CONSIDERATIONS:

While Instrumentation Amplifiers have inherently high common mode and power supply rejections, good bypassing, shielding, and grounding techniques should be employed.

Input leads should be shielded and the power supplies bypassed with 10 μf capacitors close to the amplifier.

In addition, when an external gain setting resistor is used it is preferable to locate it close to the amplifier. If it is necessary to locate this resistor more than a few inches from the amplifier shielded leads should be used. Remotely locating the gain setting resistor may degrade CMRR at high frequencies.

TYPICAL APPLICATION



INSTRUMENTATION AMPLIFIER SPECIFICATION DEFINITIONS

Gain—The ratio of the change in output voltage to the change in input voltage.

Gain Nonlinearity—Maximum deviation from the ideal gain transfer function over the full output range.

Gain Accuracy—The percentage that actual gain differs from ideal gain.

Differential Input Impedance—Impedance seen looking into the plus and minus input terminals with respect to each other.

Common Mode Input Impedance—Impedance seen looking into either the plus or minus input with respect to analog ground.

Initial Offset Voltage (referred to input)—Collection of internal voltage offsets summed and treated as a single offset appearing in series with the input. This offset, multiplied by the programmed gain, will appear at the amplifier output. This can normally be zeroed out with an external trimpot.

Offset Voltage Drift (referred to the input)—Drift in initial offset voltage due to temperature variation.

Offset Voltage vs. Supplies—Change in initial offset voltage due to variations in power supply voltages.

Voltage Noise (referred to input)—Sum of the internal noise sources treated as a single source appearing in series with the input signal. This noise, multiplied by the programmed gain, will appear at the amplifier output. Voltage noise is dependent on bandwidth and may be reduced by using the minimum bandwidth necessary for a given application.

Small Signal Bandwidth—Frequency at which the amplifiers gain drops 3 dB from its D.C. gain.

Settling Time—Time required for the output to reach specified accuracy for a given change in the input.

Common Mode Rejection Ratio—The ability of the amplifier to reject signals common to both the plus and minus inputs and extract the desired signal appearing between the plus and minus inputs. Usually given as the ratio of differential gain to common mode gain.

Filter Breakpoint—Frequency where the output is attenuated 3 dB by the internal filter.

Output Voltage Swing—Maximum allowable output excursion for faithful reproduction of the input signal. This is limited to several volts less than the associated power supply.

Output Drive Current—Current that the amplifier will source or sink to the load while remaining within specification.

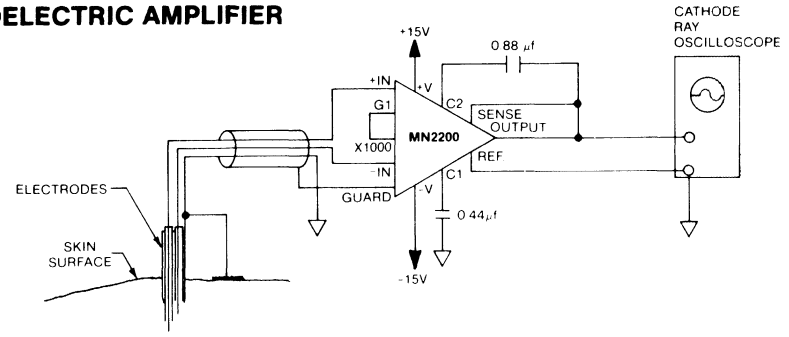
Output Impedance—Source impedance of the amplifier output.

Output Load Capacitance—Maximum capacitive load that the amplifier can drive while remaining stable and within specification.

Slew Rate—Rate of change of the output in response to a step change at the input.

APPLICATIONS INFORMATION:

BIOELECTRIC AMPLIFIER



The circuit shown may be used to measure any of a number of bioelectric phenomena.

The MN2200 high performance instrumentation amplifier is used to amplify and buffer low level signals from the bioelectric probe. The amplified signals are then displayed on a cathode ray oscilloscope or recorded by a strip chart recorder.

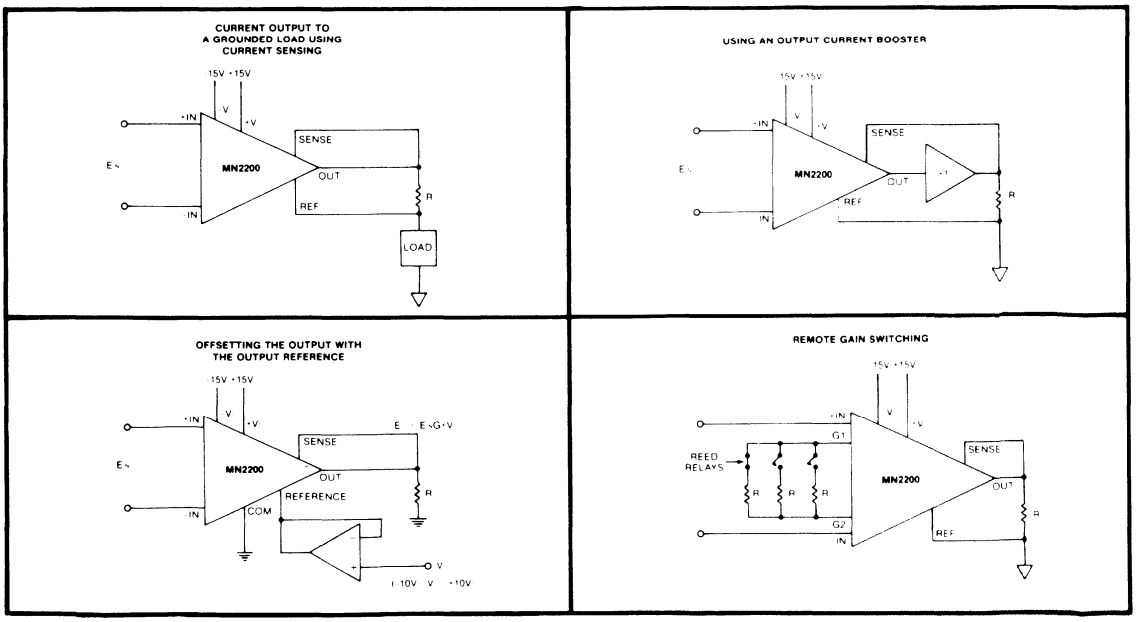
In general both AC and DC characteristics of a waveform with peak amplitude on the order of 10MV are measured. Since the electrodes used exhibit an output impedance of 20-100K it is necessary to use the MN2200's guard terminal to drive the input cable shield. This minimizes common mode error caused by the wire to shield capacitance of the input cable interacting with the unbalanced electrode impedances.

Next, there must be a path for instrumentation amplifier input bias current return.

In this circuit, the bias current return is provided by the ground plate on the skin surface. The internal fixed gain of 1000 is used because an accurate, absolute measurement of the magnitude of the input voltage is desired.

Also, wiring of the output circuit should be done so as to minimize errors caused by current flowing in ground lines or current drawn by the load. This is done by 1) connecting the instrumentation amplifier reference terminal to the ground reference of the load and 2) connecting the output sense terminal directly to the output side of the load.

A cutoff frequency (50HZ) is used in the active filter section of the MN2200 to reduce noise while maintaining sufficient bandwidth to display the AC component of the measured signal.



MICRO NETWORKS

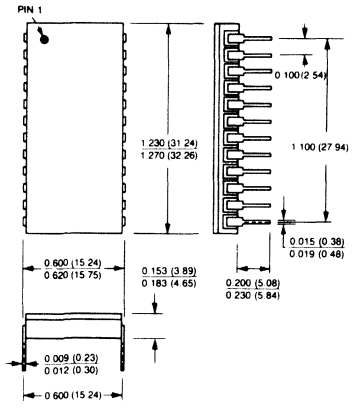
MN4000

40nsec 12-Bit LINEAR
T/H AMPLIFIER

FEATURES

- **±0.024% FSR Maximum Gain Linearity Error**
- **40nsec Full Scale Acquisition Time (to 0.01%FSR)**
- **Low 30mVp-p T/H Transient**
- **Fast 25nsec T/H Transient Settling Time**
- **50MHz Small Signal Bandwidth**
- **Functionally Compatible with Industry Standard −0010/0025**
- **DESC SMD 5962-90856 Listed**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

24-PIN SIDE BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN4000 is a very high-speed (40nsec signal acquisition to ±0.01%FSR), high-resolution (±0.024%FSR maximum gain linearity error), unity-gain, non-inverting track-hold (T/H) amplifier. The MN4000 is suitable for applications where high-speed performance is required in conjuction with high-resolution.

The MN4000 is packaged in a small, 24-pin, hermetically sealed, side-brazed DIP and maintains an established, industry-standard pinout making it a functionally compatible, performance upgrade in applications utilizing −0010/0025 type devices.

The MN4000 is available fully specified for either 0°C to +70°C or −55° to +125°C (H, H/B and H/B CH models) operation. For military/aerospace or harsh-environment commercial/industrial applications, the MN4000 H/B is available environmentally stress screened. Consult factory for availability of MN4000 H/B CH. Additionally, the MN4000 is listed on DESC SMD 5962-90856.

APPLICATIONS

High-Speed Signal Processing
RADAR and IF Processors
Instrumentation Systems
EW and ECM Systems
Video Digitizers
Communications Systems
Subranging A/D Converters

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

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MN4000 40nsec 12-Bit LINEAR T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN4000	0°C to +70°C
MN4000H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
± 15V Supply (± V_{CC}, Pins 22, 3)	± 18 Volts
+5V Supply (± V_{DD}, Pin 9)	−0.5 to +6.5 Volts
−5.2V Supply (± V_{CC}, Pin 4)	+0.5 to −6.5 Volts
Analog Input (Pin 13)	± 2 Volts
Digital Input (Pin 5)	0 to −3 Volts

ORDERING INFORMATION

PART NUMBER **MN4000H/BCH**

Standard device is specified for
0°C to +70° operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" suffix to "H" model for environmental stress screening.
Add "CH" to H/B models for 100% screening
according to MIL-H-38534. Consult factory
for availability of "CH" devices.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ± 15V, +5V and −5.2V unless otherwise indicated) (Note 1)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range (Note 2) Input Impedance (Note 2)	± 1 10			Volts kΩ
Output Current (Note 2) Output Impedance (Note 2)	± 25	 0.25	 0.5	mA Ω
DIGITAL INPUT				
Logic Levels: Logic "1" Logic "0"	−0.8		 −1.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = −0.8V) Logic "0" (V_{IL} = −1.8V)			± 500 ± 500	μA μA
TRANSFER CHARACTERISTICS				
Gain Gain Error: Initial (+25°C) Over Temperature		+1 ±0.25 ± 1	 ±0.5 ± 2	V/V %FSR %FSR
Gain Linearity Error		±0.012	± 0.024	%FSR
Input Offset Voltage: Intial (+25°C) Over Temperature		± 1 ± 10	± 5 ± 15	mV mV
Pedestal: Initial (+25°C) Over Temperature		± 2 ± 10	± 7 ± 15	mV mV
DYNAMIC CHARACTERISTICS				
Acquisition Time: 2V Step to ± 0.1% (± 2mV) 2V Step to ± 0.01% (± 0.2mV, Note 2)		30 40	50 60	nsec nsec
Track-to-Hold Transient: Height (Peak to Peak) Settling Time (to ± 2mV)		20 25	30 30	mVp-p nsec
Aperture Delay Time			5	nsec
Aperture Jitter (Note 2)			± 20	ps (rms)
Slew Rate (V_{IN} = −1V to +1V Step) (Note 2)	200	250		V/μsec
Small Signal Bandwidth (V_{IN} = 1V AC p-p) (Note 2)	50	60		MHz
Large Signal Bandwidth (V_{IN} = 2V p-p) (Note 2)		40		MHz
Feedthrough Attenuation (V_{IN} = 2V p-p @5 MHz)	60	72		dB
Droop Rate: Initial (+25°C) Over Temperature		50	200 20	μV/μsec mV/μsec
Harmonic Distortion (Track Mode, V_{IN} = ± 1V, 5MHz)		−72		dB
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +V_{CC} Supply −V_{CC} Supply +V_{DD} Supply −V_{EE} Supply	+14.55 −14.55 +4.75 −5.0	+15 −15 +5 −5.2	+15.45 −15.45 +5.25 −5.7	Volts Volts Volts Volts
Current Drain: +V_{CC} Supply −V_{CC} Supply +V_{DD} Supply −V_{EE} Supply		+8 −8 +50 −50	+10 −10 +70 −70	mA mA mA mA
Power Supply Rejection Ratio: +V_{CC} Supply −V_{CC} Supply +V_{DD} Supply −V_{EE} Supply		± 8 ± 8 ± 8 ± 8	± 15 ± 15 ± 15 ± 15	mV/V mV/V mV/V mV/V
Power Consumption		750	1014	mW

SPECIFICATION NOTES:
1. R_L = 100Ω, C_L = 50pF.
2. These parameters are listed for reference only and are not tested.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS — The MN4000 is a high-resolution high-speed device and requires that careful attention be paid to layout, grounding and bypassing in order to achieve specified accuracy and speed performance. Coupling between analog input and digital signals should be minimized to avoid noise pickup. Care should be taken to avoid long analog runs in parallel with the digital lines. In addition, particular attention must be paid to the device's external hold capacitor connection. Pin 20 should be isolated from digital signals and it is recommended that the pin be shielded by ground.

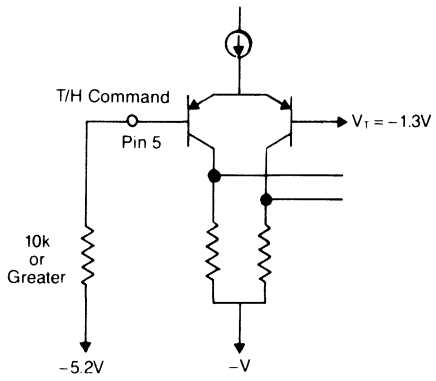
The units five ground pins (pins 7, 11, 18, 19, and 21) should be tied together at the device and connected to system analog ground preferably through a large, low-impedance analog ground plane beneath the device.

p.c. card ground runs must be run separately, wide conductor runs should be employed with 0.01uF ceramic capacitors interconnecting them as close to the device as possible.

Power supply connections should be as short and direct as possible, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. It is recommended that μF tantalum capacitors in parallel with 0.01μF ceramic, surface-mount chip capacitors be located as close to the device pins as possible.

TRACK-HOLD COMMAND — A Logic "0" applied to the Track-Hold (T/H) Command input (pin 5) drives the device into the track (sample) mode. In this mode, the MN4000 operates as a unity gain amplifier (follower) and its output tracks (follows) the applied analog input signal. A Logic "1" applied to the T/H Command (pin 5) drives the MN4000 into the hold mode holding the output of the device constant at the level present when the hold command was given.

The MN4000's T/H Command input is illustrated below. This input is compatible with ECL logic devices. However, precautions should be taken in certain test circuits where the T/H Command input is not driven with standard ECL logic devices (burn-in and some test circuits for example). Care should be taken to avoid exceeding the absolute maximum ratings when hardwiring this input to negative supply voltages. In these cases when the T/H Command input is connected to a voltage supply, we recommend the use of a series 10kΩ or greater resistor as shown below.



MN4000 ACQUISITION TIME — The MN4000's signal acquisition time is specified for full scale steps settling to a specified limit (± 0.1%FSR for 10-bit applications and ± 0.01%FSR for 12-bit applications). It is important to note, for the purpose of comparision, that Micro Networks specifies this parameter from the edge of the applied T/H Command to the point where the T/H output has settled to within the specified band. The acquisition time of the MN4000 includes the gate delay of the switch, output amplifier delay, effects of slew rate and the actual settling of the output signal. For further discussion of acquisition time and other T/H amplifier related specifications, refer to the data book tutorial section labeled Track and Hold Amplifiers.

DRIVING CAPACITIVE LOADS — Care must be taken to optimize the performance of the MN4000 in circuit applications with high capacitive loading at the megahertz frequencies these devices are designed to handle. In particular, the series inductance of the wire or p.c. card run connecting the MN4000 to its capacitive load is no longer insignificant. In order to obtain the quickest settling at the load in response to a driving function at the T/H output, it will be necessary to add a series resisitor such that the resulting RLC circuit is critically damped. The value of the damping resisitor will depend upon the length of the wire (or run) and the load capacitance.

Critical damping occurs in a series RLC circuit when the resonant radian frequency (ωo) equals the exponential damping coefficient (α).

Since $\omega_o = 1/\sqrt{LC}$

and $\alpha = R/2L$

it follows that $R = 2\sqrt{L/C}$

Where R is required value of series resistance, L is the wire (or run) inductance and C is the load capacitance. In making calculations, an inductance of 23nHy/in. can be assumed for straight, solid wire of AWG 20 to 28, or p.c. runs of 100 to 600mil² cross-sectional area. This value should also serve as a good starting point for experimentation if other shapes or wire sizes are used. Bear in mind that critical damping only guaranteed best settling for a given combination of L and C. There will still be practical limits on the values these can assume if settling is to be accomplished in a reasonable time.

The voltage at the load capacitor will be the form

$$V(t) = A\{1-(\alpha t + 1)e^{-\alpha t}\}$$

in response to a step of amplitude A at the T/H output. For settling to 0.1%, v(t) = 0.999A and, from the equation above, $\alpha t = 9.23$. Since $\alpha = \omega o = 1/\sqrt{LC}$, it follows that the settling to ± 0.01% of the step size occurs at the $t = 9.23\sqrt{LC}$.

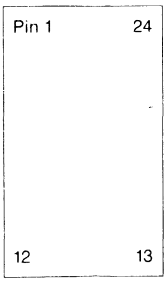
As an example, assume C_{LOAD} = 200pF and that it is 2.2 inches from the T/H ouput. This corresponds to a wire inductance of L=23nHy/in. × 2.2in.=51nHy. For critical damping, $R=2\sqrt{L/C}$ =32Ω. This resistor should be a carbon or other non-inductive type, and its length will count as part of the inductance to be damped. With C and L as above the settling time to ± 0.1% will be

$$t=9.23\sqrt{LC} = 30nsec.$$

The actual settling time in any given situation will be somewhat longer than predicted above due to the effects of the settling time of the T/H itself. A very good approximation of the overall settling time can be obtained by assuming the two components add as the square root of the sum of their squares. In the above example, assuming 30nsec settling time for the T/H to ± 0.1%, this would mean $\sqrt{30^2+30^2}$, or about 42nsec total settling from the time a step is applied to the input of the T/H to the time voltage seen be the A/D settles to ± 0.1% of its final value.

For 12-bit applications the calculations are as shown above where settling is specified to ± 0.01% and settling occurs at $11.75\sqrt{LC}$.

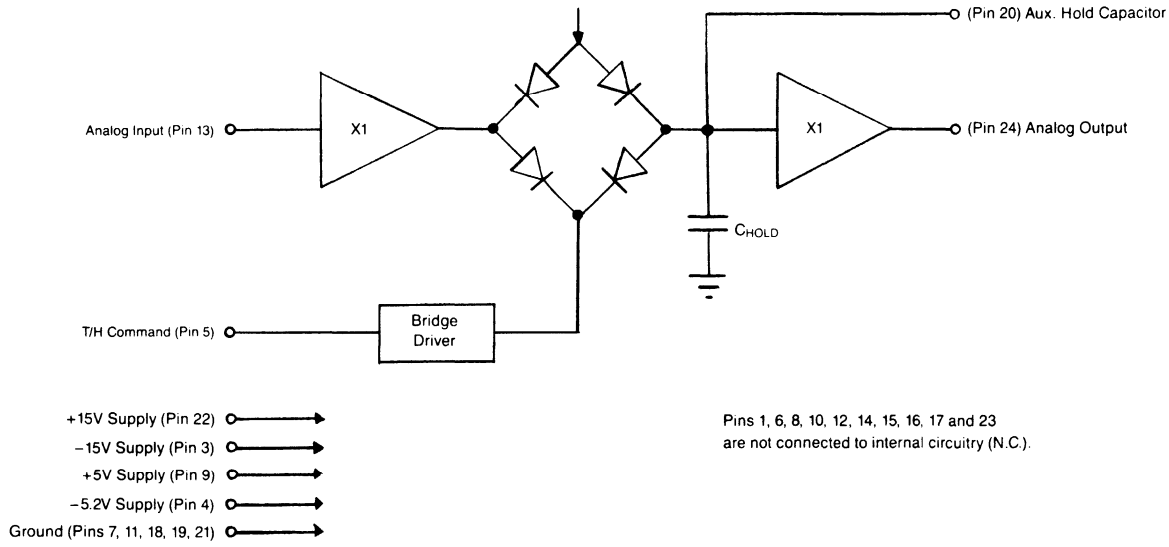
PIN DESIGNATIONS



1	N.C.	24	Analog Output
2	N.C.	23	N.C.
3	−15V Supply	22	+15V Supply
4	−5.2V Supply	21	Ground
5	Hold Command	20	Aux Hold Capacitor
6	N.C.	19	Ground
7	Ground	18	Ground
8	N.C.	17	N.C.
9	+5V Supply	16	N.C.
10	N.C.	15	N.C.
11	Ground	14	N.C.
12	N.C.	13	Analog Input

Notes:
"No Connects" (N.C.) are not connected to internal circuitry.

BLOCK DIAGRAM



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Data Acquisition Systems

Data Acquisition Systems

A single-package data acquisition system (DAS) is a device that clearly utilizes hybrid technology's ability to combine IC's from different fabrication technologies to take advantage of the best aspects of each in a single functional design.

The MN7150-8 and MN7150-16 are excellent examples of this "hybrid advantage". The MN7150 Series devices consist of an overvoltage protected CMOS multiplexer; a BiFet instrumentation amplifier; a low-leakage dielectrically isolated T/H amplifier; and a high-speed bipolar A/D converter. All these IC's are combined and functionally laser trimmed in a single design to give true 12-bit performance (± ½LSB linearity) and 50kHz throughputs. MN7145 Series DAS's contain similar fuctions and also add a complete μP interface (3-state buffer, address line, read/write line, etc.) facilitating direct microcomputer control.

Micro Networks pioneered the complete, single-package, data acquisition system in 1975 with the MN7120 (8-bit, 8-channel, 90kHz DAS). Three years later, our MN7130 (DAS front end) gave users the flexibility of selecting their own A/D converter. The MN7130 may be combined with the MN574A (or ADC80) to easily configure a low-cost, μP-compatible, 12-bit DAS. For military/aerospace applications, our MN7140 (12-bit, 20kHz DAS) was the first, single-package, 12-bit DAS to operate over the −55°C to +125°C temperature range and withstand the rigors of MIL-STD-883 screening. The MN7140 is joined by the MN7150 and MN7145/46/47 which also offer extended temperature operation and MIL-STD-883 screening performed in Micro Networks MIL-STD-1772 qualified facility.

Today, these products are joined by another Micro Networks first, the MN7450, a small, single package, 8-channel, 16-bit Data Acquisition System. This device is a complete data acquisition function in a small 40-pin DIP and contains an analog input multiplexer, software programmable gain amplifier, inherent T/H function, internal clock, reference, and a self-calibrating 16-bit A/D converter complete with microprocessor interface control lines.

MN7208
MN7216
Data Acquisition Front End

FEATURES

- Complete DAS Front End:
  - Analog Input Multiplexer
  - Instrumentation Amplifier
  - Load/Sequence Control Logic
- Small 40-Pin DIP
- 16-Single Ended or 8-Differential Input Channels
- 10μsec Channel Switching and In-Amp Settling Time
- Full Mil Operation −55°C to +125°C
- Use with MN6000 Series Sampling A/D Converters for Multi-Channel Digitizing
- Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)

MN7450
MN7451
8-Channel, 16-Bit Data Acquisition System

FEATURES

- Complete DAS:
  - Latched Input MUX
  - Software Programmable Gain Amplifier
  - Buffer Amplifier
  - Inherent T/H Function
  - Internal Reference
  - Internal Clock Option
  - 16-Bit Self-Calibrating A/D Converter
- Small Double-Wide 40-Pin DIP
- 8 X 2 Byte Output Format
- 8 Single-Ended Input Channels
- Input Over-Voltage Protection
- Low Initial Gain and Offset Error
- Fully Specified 0°C to +70° (J and K Models) or −55°C to +125°C (S and T Models)

Data Acquisition Systems

Resolution	Model	Input Channels	Acquisition Time to ±½LSB (μsec)	Conversion Time (μsec)	Throughput (Channels/sec)	Maximum Linearity Error (%FSR)	Power (mW)	DIP Package	Specified Temp Range (°C)	Hi-Rel Option	DESC SMD (5962-)	Page No.
8-Bits	MN7120	8	5	6	90,000	±0.2	680	32 Pin	0 to +70 −55 to +125	Yes	(Note 1)	9-5
12-Bits	MN7150-8 MN7150-16	8 16	9	9	55,000	±0.012	1785	62 Pin	0 to +70 −25 to +85 −55 to +125	Yes	(Note 1)	9-31
	MN7145 MN7146 MN7147	8	8	20	35,000	±0.012 ±0.024	710	28 Pin	0 to +70 −55 to +125	Yes	(Note 1)	9-23
	MN7140	8 (Expandable)	8	40	20,000	±0.012	1250	40 Pin	0 to +70 −25 to +85 −55 to +125	Yes	9079701	9-15
	MN7130	16 (Expandable)	6.5	N.A.	N.A.	±0.002 (Typ)	900	32 Pin	0 to +70 −55 to +125	Yes	9057101	9-9
16-Bits	MN7450 MN7451	8	15 (Note 3)	16 (Note 3)	47,700 (Note 3)	±0.0015	658	40 Pin	0 to +70 −55 to +125	Yes	(Note 1)	9-45
	MN7208 MN7216	8 16	10 (Note 2)	N.A.	N.A.	±0.003	245	40 Pin	0 to +70 −55 to +125	Yes	(Note 1)	9-39

NOTES: 1. Contact the factory for information regarding DESC SMD's for these device types.
2. Specification is for settling time including MUX switching and instrumentation amplifier settling time.
3. Due to the design of the MN7450 Series DAS, the channel switching and PGA settling time can be pipelined with A/D conversion allowing for total throughput in the pipelined mode of 47.7kHz.

✓ Indicates New Product.



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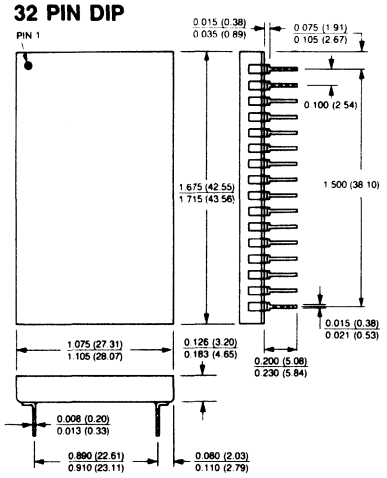
MN7120

8-Bit, 8-CHANNEL
DATA ACQUISITION SYSTEM
with 3-STATE OUTPUTS

FEATURES

- **Complete System:**
  Input Multiplexer
  Track-Hold Amplifier
  8-Bit A/D Converter
  3-State Output Buffer
  Control Logic
- **Small 32-Pin DIP**
- **±1/2 LSB Linearity and No Missing Codes Guaranteed Over Temperature**
- **Random or Sequential Addressing**
- **75,000 Channels/sec Guaranteed Throughput**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

32 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN7120 is a complete, 8-bit, 8-channel data acquisition system with 3-state outputs in a single, 32-pin, hermetically sealed dual-in-line package. Contained in the single package are input multiplexer with address register, track-hold (T/H) amplifier, A/D converter, 3-state output buffer, clock and all the necessary controlling logic. The basic system's 8 input channels can be either randomly or sequentially addressed, and input impedance is greater than 10 megohms. The number of input channels is easily expanded with external multiplexers.

MN7120 is actively laser trimmed as a complete device eliminating the normally annoying DAS errors such as T/H pedestal error. The system is adjustment-free. No external gain or offset adjusting potentiometers are required to guarantee an overall system error of better than ±1 LSB at +25°C and better than ±2 LSB's over the entire operating temperature range.

The MN7120's T/H has an acquisition time of 6μsec, and the A/D's conversion time of 7μsec allows an overall throughput rate of over 75,000 channels/sec. The standard device is fully specified for either 0°C to +70°C or −55°C to +125°C ("H" model) operation. The MN7120H/B is available with Environmental Stress Screening while the MN7120H/B CH is fully screened in accordance with MIL-H-38534.

MN7120's output buffer facilitate interfacing to microprocessor and microcomputer buses. Normally, simple address decoding is all that has to be added to give data acquisition capability to your microprocessor-based system. MN7120 is ideally suited for industrial control and monitoring systems. Highly reliable thin-film hybrid construction, optional MIL-H-38534 screening, and performance specifications guaranteed from −55°C to +125°C make it the right choice for low-resolution military/aerospace data acquisition requirements.

May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7120 8-Bit 8-CHANNEL DAS with 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7120	0°C to +70°C
MN7120H, MN7120H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (Pin 19)	−0.5 to +18 Volts
−15V Supply (Pin 20)	+0.5 to −18 Volts
Logic Supply (Pin 21)	−0.5 to +7 Volts
Analog Inputs (Pins 8-15)	±15 Volts
Digital Inputs (Pins 1-4, 32)	-0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— **MN7120H/B CH**

Standard Part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels (Note 1)		8		
Input Voltage Range		±10		Volts
Input Impedance		10		Mohm
Direct T/H Input Impedance (Pin 16)		10		Mohm
TRANSFER CHARACTERISTICS (Note 2)				
Resolution		8		Bits
Quantization Error		±½		LSB
Integral Linearity Error: Initial (+25°C)		±⅛	±½	LSB
Over Temperature (Note 3)		±¼	±½	LSB
Zero Error (Note 4): Initial (+25°C)		±¼	±1	LSB
Over Temperature (Note 3)		±½	±1	LSB
Full Scale Absolute Accuracy (Note 5): Initial (+25°C)		±½	±1	LSB
Over Temperature (Note 3)		±1	±2	LSB
DYNAMIC CHARACTERISTICS				
T/H Acquisition Time (Note 6)		5	6	μsec
T/H Aperture Delay Time		50		nsec
A/D Conversion Time		6	7	μsec
Throughput Rate (Channels/sec)	75	90		kHz
Crosstalk Attenuation	65			dB
POWER SUPPLIES				
Power Supply Range: ±15V Supply		±5		%
+5V Supply		±5		%
Power Supply Rejection: +15V Supply		±0.04		%FSR/%Vs
−15V Supply		±0.001		%FSR/%Vs
+5V Supply		±0.001		%FSR/%Vs
Current Drains: +15V Supply		+10	+16	mA
−15V Supply		−12	−25	mA
+5V Supply		+70	+110	mA
Power Consumption		680	1165	mW

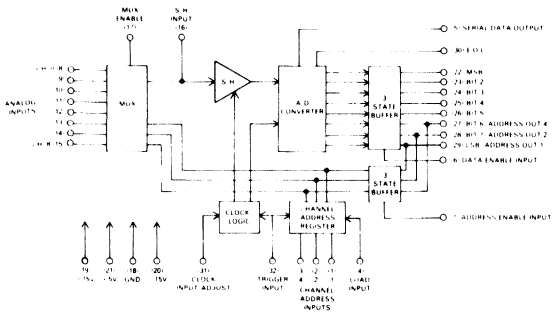
SPECIFICATION NOTES:

1. Eight single-ended input channels can be increased with external multiplexers.
2. For an 8-bit system with a 20V FSR (full scale range), 1 LSB is equal to 78.1mV.
3. MN7120 is fully specified for 0°C to +70°C operation. MN7120H and MN7120H/B are fully specified for −55°C to +125°C operation.
4. Zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000. The ideal value at which this transition should occur is 0 Volts.
5. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors and is specified without adjustment. The full scale accuracy specification applies at both positive and negative full scale. It is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1110 to 1111 1111 or from 0000 0000 to 0000 0001. The former transition ideally occurs at an input voltage 1 LSB below the nominal positive full scale voltage. The latter ideally occurs 1 LSB above the nominal negative full scale voltage. See Digital Output Coding.
6. Specified for a 20V step acquired to ±½LSB.

Analog Input (DC Volts)	Digital Output MSB LSB
+10.000	1111 1111
+9.922	1111 111Ø*
+0.078	1000 000Ø*
0.000	ØØØØ ØØØØ*
−0.078	0111 111Ø*
−9.922	0000 000Ø*
−10.000	0000 0000

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the system continuously sampling and converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. The transition from digital output 0000 0000 to digital output 0000 0001 (or vice versa) will ideally occur at −9.922V. Subsequently, an input voltage more negative than −9.922V will give an output of all "0's". The transition from digital output 0111 1111 to digital output 1000 0000 (or vice versa) will ideally occur at an input of zero volts. The 1111 1110 to 1111 1111 transition should occur at +9.922V. An input greater than +9.922V should give all "1's".

BLOCK DIAGRAM



DIGITAL INPUTS AND OUTPUTS

Digital Inputs	Logic Signal	Description	Load Presented	Min. Pulse Width	Notes
Mux Enable	"1"	Enables Internal Mux	1 uA	Level	Tie to Logic "1" unless additional external MUX's are used for expansion. Logic "0" ≤0.4V Logic "1" >4.0V
	"0"	Disables Internal Mux	1uA		
Channel Address Inputs	3 Lines 421 Binary	Selects desired channel in random address mode	TTL	125 nSec	Must be set up 100 nSec before clocking trigger and be valid through rising edge of trigger
Load	"1"	Sequential Address Mode	TTL	Level	Data will be loaded on the first rising edge of trigger
	"0"	Random Address Mode			
Trigger	"0" to "1"	Starts Data Acquisition Process	TTL	100 nSec	
Clock		System Clock	20 pf Parallel 30k	100 nSec Min 400 nSec Max.	1.5 MHz Max. Clock rate can be varied or an external clock used.
Address Enable	"0"	Enables Address Output Three State Buffers	1 uA	Level	Tie to logic "1" if Address Output is not needed.
Data Enable	"0"	Enables Data Output Three State Buffers	1 uA	Level	Tie to logic "0" if 3-State Outputs are not required.
Digital Outputs	**Logic Signal**	**Description**	**Max. Load**	**Notes**	
Data Outputs	True Binary	Parallel digital data outputs 8 lines MSB thru LSB	1 TTL	Output data is valid after E.O.C. goes low.	
Channel Address Outputs	421 Binary	Channel address outputs 3 lines	1 TTL	Indicates channel being converted.	
E.O.C.	"0"	Conversion process complete output data valid	6 TTL	E.O.C. goes to logic "1" 5 uSec after trigger returns low and returns to logic "0" when conversion is complete.	
Serial Data	NRZ	Serial Data Output	3 TTL	Output occurs during the A/D conversion period.	

PIN	FUNCTION	PIN	FUNCTION
1	Address Input – 1	17	Mux Enable
2	Address Input – 2	18	Ground
3	Address Input – 4	19	+15 Volts
4	Load	20	–15 Volts
5	Serial Data Output	21	+5 Volts
6	Data Enable Input	22	MSB Out
7	Address Enable Input	23	Bit 2
8	Channel 0	24	Bit 3
9	Channel 1	25	Bit 4
10	Channel 2	26	Bit 5
11	Channel 3	27	Bit 6/Address Output – 4
12	Channel 4	28	Bit 7/Address Output – 2
13	Channel 5	29	LSB/Address Output – 1
14	Channel 6	30	End of Conversion
15	Channel 7	31	Clock In/Adj
16	Sample/Hold Input	32	Trigger Input

INPUTS

It is recommended that unused analog inputs be grounded.

ADDRESSING

Both sequential and random addressing are available in the MN7120. For sequential addressing connect LOAD to logic "1". Channels will sequence from 0 thru 7, advancing one channel on the leading edge of each TRIGGER pulse. For random channel addressing the channel address (421 binary code) is applied to the CHANNEL ADDRESS INPUTS with LOAD at logic "0". The rising edge of the next TRIGGER pulse will update the channel address. The CHANNEL ADDRESS OUTPUTS, when enabled, indicate the last channel selected.

TRIGGERING

The rising edge of a positive TRIGGER pulse updates the channel address, the falling edge commands the sample/hold to the sample mode.

CLOCK

The MN7120 can be operated from it's internal clock or an external clock applied to the CLOCK INPUT. The internal clock is disabled during analog signal acquisition to reduce noise. A resistor (20k ohms or higher) connected from the CLOCK INPUT to +5V will increase the clock rate inversly with resistance. If the resistor is connected to ground the clock frequency will decrease inversly with resistance. The clock rate can be observed as an RC charging waveform of 0.5Vp at the CLOCK INPUT. Loading at this point should be greater than 10M ohms to avoid shifting the clock rate.

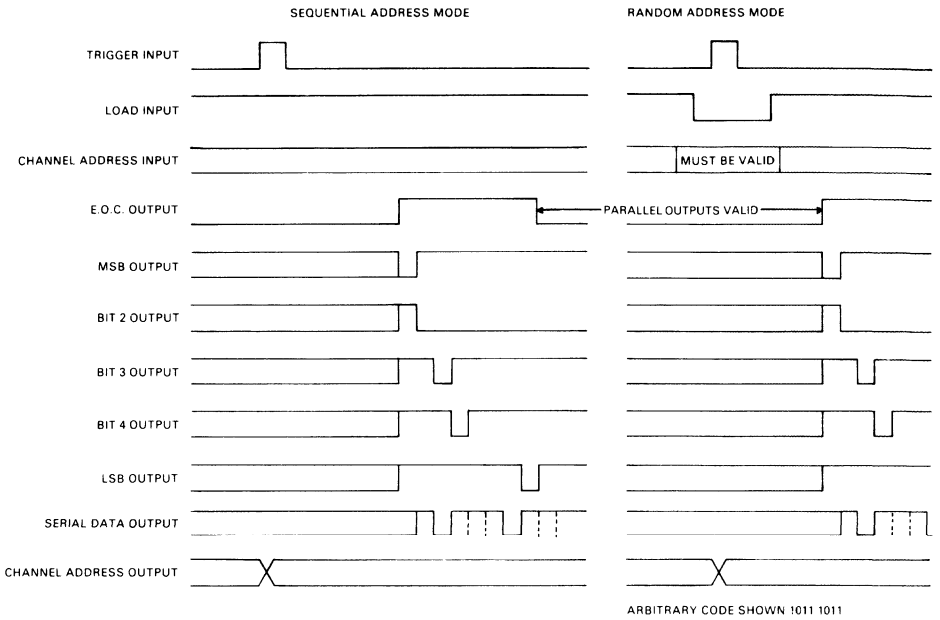
THREE STATE OUTPUTS

Three state buffers are employed on the data and channel address outputs. Channel address or data outputs are selected by a logic "0" on the corresponding ENABLE INPUT. If neither ENABLE is selected the 8 output lines will assume a high impedance state. The CHANNEL ADDRESS and DATA outputs should not be enabled simultaneously. Parallel data will be valid in 95 nsec after the Enable pulse goes Low.

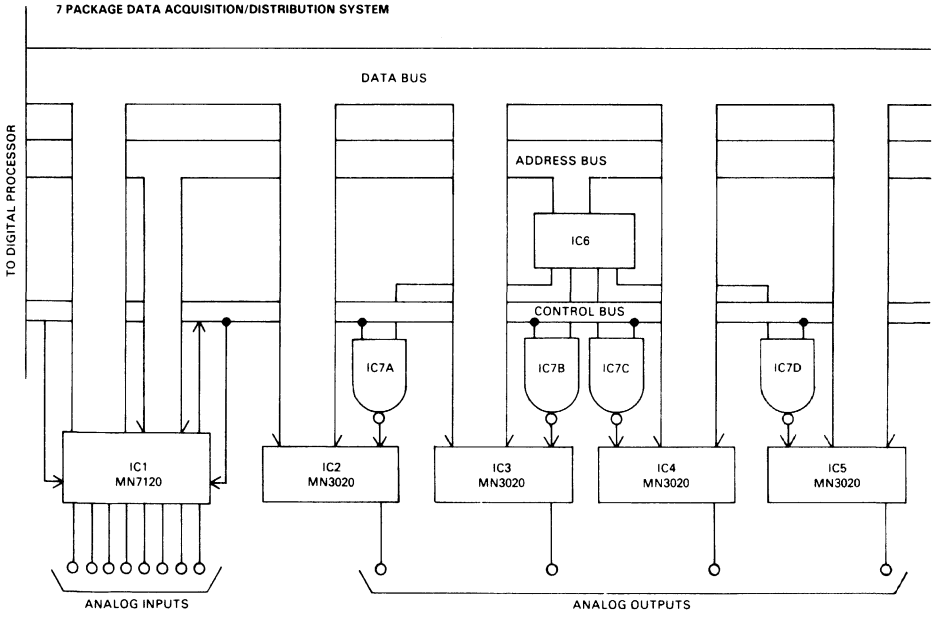
SERIAL DATA OUTPUT

The MN7120 provides serial as well as parallel data output. The first falling edge of the Bit 2 output can be used to indicate the start of the serial output data.

TIMING DIAGRAM



7 PACKAGE DATA ACQUISITION/DISTRIBUTION SYSTEM



IC1 Micro Networks MN7120 Data Acquisition System with Three State Outputs
IC2-5 Micro Networks MN3020 D/A with Input Buffers
IC6 Signetics 8223 Field Programmable ROM

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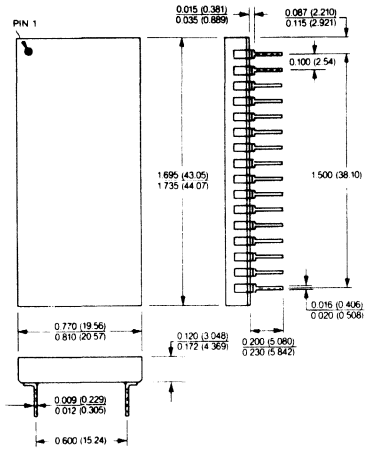
MN7130

MULTIPLEXED
TRACK-HOLD
AMPLIFIER

FEATURES

- **Complete DAS Front End:**
  2 8-Channel Multiplexers
  Instrumentation Amp
  Track-Hold Amp
- **Small 32-Pin DIP**
- **12-Bit Linearity**
- **16 Single-Ended or 8 Differential Input Channels**
- **10μsec Maximum Acquisition Time to ±0.01% (20V Step)**
- **Low Droop Rate ±7μV/μsec Maximum**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

32 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN7130 is a thin-film hybrid circuit containing two 8-channel multiplexers, a true instrumentation amplifier and a track-hold amplifier. This unique circuit is extremely versatile and can be used in conjunction with any of Micro Networks analog-to-digital converters to configure a complete, 16-channel (8 full differential) data acquisition system in as few as 2 dual-in-line packages occupying as little as 4 square inches of board space. Additionally, MN7130 can be used in any analog system for applications requiring the analog acquisition of multiple channels.

MN7130 has a maximum acquisition time of 10μsec (20V step to ±0.01%FSR) when the multiplexer, instrumentation amplifier and track-hold are serially connected, and a typical droop rate of ±4μV/μsec. The internal multiplexer may be connected for single-ended or 8 full differential input channels and is directly addressable in binary. The digital inputs are CMOS compatible, and analog inputs up to ±10V can be accommodated. For additional flexibility, all inputs and outputs of the internal subsections are available at the device pins. The standard device is fully specified for either 0°C to +70°C or −55°C to +125°C (H model) operation. The MN7130H/B is available with Environmental Stress Screening while the MN7130H/B CH is fully screened in accordance with MIL-H-38534.

MN7130 was specifically designed to fill the need for a small, low-cost data acquisition system that was physically and electrically compatible with current microprocessor technology. When used with a 12-bit A/D, the approach eliminates the need for special mountings and connectors, saves space, facilitates maintenance, and reduces costs. In addition, MN7130 allows standard board spacing, improves reliability and offers significant weight savings in aerospace and avionics applications.

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MN7130 MULTIPLEXED TRACK-HOLD AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7130	0°C to +70°C
MN7130H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+V_{CC}, Pin 24)	0 to +16 Volts
Negative Supply (−V_{CC}, Pin 23)	0 to −16 Volts
Multiplexer Inputs (Pins 1-16)	−V_{CC} to +V_{CC}
Instrumentation Amp Inputs (Pins 21, 22)	±15 Volts
T/H Amplifier Input (Pin 19)	0 to ±V_{CC} Volts
Address Inputs (Pins 27-31)	−0.3 to +V_{CC} Volts
T/H Command (Pin 17)	0 to +7 Volts
Multiplexer Outputs (Pins 26, 32)	±20mA
Instrumentation Amp Output (Pin 20)	±25mA
T/H Amplifier Output (Pin 18)	S.C. Protected to Ground

ORDERING INFORMATION

PART NUMBER — **MN7130/H/B CH**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SYSTEM SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, unless otherwise indicated) (Note 1)

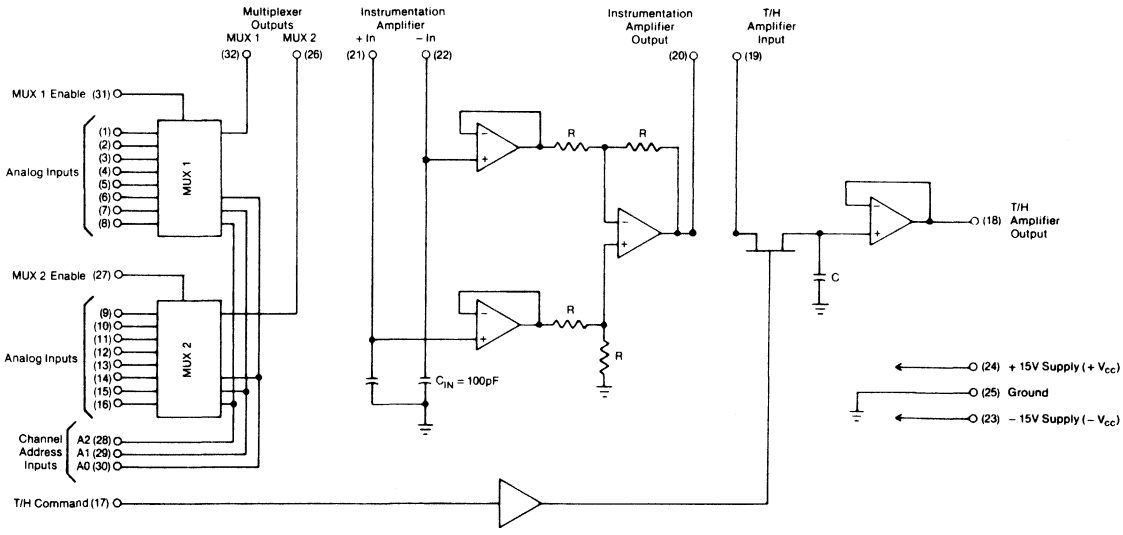
ANALOG INPUT (Multiplexer Inputs)	MIN.	TYP.	MAX.	UNITS
Voltage Range: Single-Ended		±10		Volts
Differential		±10		Volts
Common Mode	±10	±12		Volts
Input Impedance		250//100		MΩ//pF
Input Current		±15	±30	nA
Common Mode Rejection Ratio	70	80		dB
DIGITAL INPUTS (Mux Address, T/H Command)				
Logic Levels: Mux Address: Logic "1"	+4.0			Volts
Logic "0"			+0.8	Volts
T/H Command: Logic "1"	+2.4			Volts
Logic "0"			+0.8	Volts
Logic Currents: Mux Address (Note 2):				
Logic "1" (V_{IH} = +5.0V)		±10		μA
Logic "0" (V_{IL} = +0.0V)		±10		μA
T/H Command: Logic "1" (V_{IH} = +2.4V)		±10		μA
Logic "0" (V_{IL} = +0.4V)		±10		μA
ANALOG OUTPUT (T/H Amplifier)				
Output Voltage	±10			Volts
Output Current	±2			mA
Output Load Capacitance			50	pF
TRANSFER CHARACTERISTICS				
Gain		+1		V/V
Gain Error (Note 3): Initial (+25°C)		±0.1		%
Over Temperature (Note 4)		±0.1	±0.2	%
Gain Linearity Error (Note 5)		±0.002		%FSR
Offset Voltage (Track Mode): Initial (+25°C)		±2		mV
Over Temperature (Note 4)		±4	±6	mV
Offset Change (Pedestal, Hold Mode) Over Temperature (Note 4)		±15		mV
Droop Rate: +25°C		±4	±7	μV/μsec
0°C to +70°C			±10	μV/μsec
−55°C to +125°C			±40	μV/μsec

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Large Signal Bandwidth		250		kHz
Output Slew Rate		± 20		V/μsec
Acquisition Time (20V step to ± 0.01%)		6.5	10	μsec
Aperture Delay		200	400	nsec
Settling Time, Track-to-Hold to ± 1.0mV		0.5	2	μsec
Feedthrough (Hold Mode) @ 1kHz		± 0.01		%
Transients Peak Amplitude: Track-to-Hold Hold-to-Track		90 100		mV mV
POWER SUPPLIES				
Power Supply Range: + 15V Supply – 15V Supply	+ 14.55 – 14.55	+ 15 – 15	+ 15.45 – 15.45	Volts Volts
Current Drains: + 15V Supply – 15V Supply		+ 30 – 30	+ 40 – 40	mA mA
Power Consumption		900	1200	mW

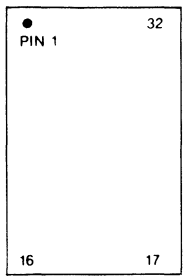
SPECIFICATION NOTES:

1. System specifications listed reflect system performance with all elements serially connected.
2. If the multiplexer inputs are to be driven from standard TTL logic, 1kΩ pullup resistors to + 5V should be connected.
3. Gain error is defined as the error in the slope of the systems input-output transfer function and is expressed in percent.
4. MN7130 is specified for 0°C to + 70°C operation. MN7130H and MN7130H/B are specified for – 55°C to + 125°C operation.
5. Gain linearity error is defined as the maximum deviation from the best-fit straight line approximation to the system's input-output transfer function and is expressed as a percentage of the system's full scale voltage swing (FSR).

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Channel 0	32	Mux 1 Output
2	Channel 1	31	Mux 1 Enable
3	Channel 2	30	A_0 Mux Address
4	Channel 3	29	A_1 Mux Address
5	Channel 4	28	A_2 Mux Address
6	Channel 5	27	Mux 2 Enable
7	Channel 6	26	Mux 2 Output
8	Channel 7	25	Ground
9	Channel 8	24	+ 15V Supply (+ V_{CC})
10	Channel 9	23	– 15V Supply (– V_{CC})
11	Channel 10	22	– In (Instrumentation Amplifier)
12	Channel 11	21	+ In (Instrumentation Amplifier)
13	Channel 12	20	Instrumentation Amplifier Output
14	Channel 13	19	T/H Amplifier Input
15	Channel 14	18	T/H Amplifier Output
16	Channel 15	17	T/H Command

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—MN7130 is a complete data acquisition system front end containing user-configurable components (multiplexers, instrumentation amplifier and track-hold amplifier).

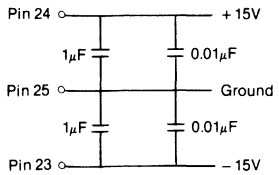
In order to preserve maximum flexibility, all inputs and outputs of the subsections are available at the device pins. The internal 8-channel multiplexers can be connected for 16 single-ended or 8 fully differential input operation and may be directly addressed via three address lines and two mux enable lines. The internal instrumentation amplifier offers high input impedance (250MΩ/100pF) and 70dB common mode rejection ratio. The internal track-hold amplifier completes this analog front-end function allowing dynamic input signals to be acquired and then held for analog-to-digital conversion.

MN7130 can be used in conjunction with MN574A μP-compatible 12-bit A/D converters to configure a complete and inexpensive, 16-channel, 12-bit μP-compatible DAS capable of 28,000 channels/sec throughput rates in a minimum of board space. Substituting MN5240 for MN574A increases throughput to 60,000 channels/sec.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified performance from the MN7130. The unit's ground pin (pin 25) should be tied to system analog ground as close to the unit as possible, preferably through a large analog ground plane underneath the package.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.



MULTIPLEXER-INSTRUMENTATION AMPLIFIER—The multiplexer section of the MN7130 is addressed with a three or four bit binary word and can be configured for 8 full differential inputs or 16 single-ended inputs. The use of differential inputs provides high rejection of common mode noise and elimination of ground return offsets. Differential inputs must be used when both sides of the input signal are off ground. Connections and truth tables for both modes of operation are shown on the following pages.

Approximately 1μsec access time should be allowed after addressing before the analog outputs of the multiplexer are used. A particular point to note is the minimum logic "1" for the multiplexer inputs is + 4.0V. If the multiplexer inputs are to be driven from standard TTL logic, 1kΩ pullup resistors to + 5V should be used.

The following diagrams show typical connections for both full differential and single-ended applications along with truth tables which demonstrate multiplexer address (A_0, A_1, A_2) and enable (Mux_1 Enable, Mux_2 Enable) line functions.

MN7130 is specified and tested as a system (all elements serially connected). Typical specifications for the multiplexer and instrumentation amplifier appear below.

Typical Mux Performance Specifications	
Numbers of Channels	16 Single-Ended 8 Full Differential
Input Voltage Range	± 10V
Input Impedance	250MΩ/100pF
Logic Levels: Logic "1" (min.) Logic "0" (max.)	+ 4.0V + 0.8V
Logic Currents: Logic "1" Logic "0"	± 10μA ± 10μA
Access Time	500nsec
On Resistance	2kΩ
Cross Talk (1kΩ Source, 1kHz, 20vp-p)	– 68dB

Typical Instrumentation Amplifier Performance Specifications	
Voltage Range	± 10V
Input Impedance	250MΩ/100pF
Input Current (max.)	± 30nA
Common Mode Rejection Ratio (min.)	70dB
Gain	+ 1V/V
Gain Error: Initial (+ 25 °C) Over Temperature	± 0.02% ± 0.05%
Gain Nonlinearity	± 0.002%
Large Signal Bandwidth	250kHz
Output Slew Rate	± 20V/μsec
Settling Time (20V Step to ± 0.01%)	4μsec
Output Voltage Swing (min.)	± 10V
Output Current (min.)	± 2mA
Output Load Capacitance (max.)	50pF

TRACK-HOLD AMPLIFIER—The track-hold amplifier is in the hold mode when the T/H command is a logic "1" and in the sample mode when the T/H command is a logic "0". A total of 10μsec should be allowed after addressing the multiplexer before the T/H is commanded to the hold mode to allow for full scale (20V) changes. Maximum acquisition times for changes less than full scale are shown on the following page.

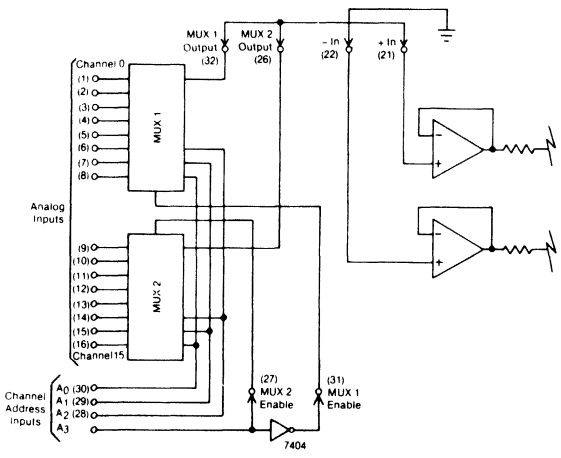
In data acquisition applications, the T/H command input can usually be driven directly from the A/D converter Status (E.O.C.) output.

As stated earlier, the MN7130 is specified and tested as a system (all elements serially connected). Typical T/H amplifier specifications are listed below.

Typical T/H Amplifier Performance Specifications	
Voltage Range	± 10V
Input Impedance	$10^{10}\Omega$
Input Bias Current	± 15nA
Logic Levels: Logic "1" (min.) Logic "0" (max.)	+2.4V +0.8V
Logic Currents: Logic "1" Logic "0"	± 10μA ± 10μA
Gain	+ 1V/V
Gain Nonlinearity: Initial (+ 25 °C) Over Temperature	± 0.002% ± 0.005%
Offset Voltage (Track Mode): Initial (+ 25 °C) Over Temperature	± 2mV ± 4mV
Offset Change (Pedestal, Hold Mode) Over Temperature	± 15mV
Droop Rate: Initial (25 °C) (max.) 0 °C to + 70 °C (max.) − 55 °C to + 125 °C (max.)	± 7μV/μsec ± 10μV/μsec ± 40μV/μsec
Acquisition Time (20V Step to ± 0.01%) (max.)	10μsec
Aperture Time (max.)	400nsec
Feedthrough (Hold Mode) @ 1kHz	± 0.01%
Transients Peak Amplitude: Track-to-Hold Hold-to-Track	90mV 100mV

MULTIPLEXER CONNECTIONS and ADDRESSING

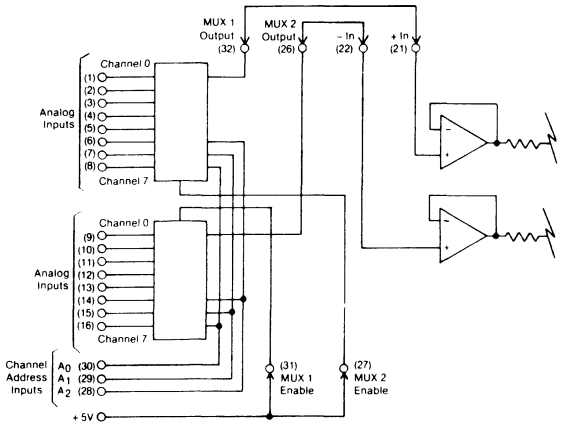
16 Single Ended Input Channels



Address Inputs			Enable Inputs		On Channel
A_2	A_1	A_0	MUX 1	MUX 2	
X	X	X	1	1	ILLEGAL
X	X	X	0	0	NONE
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	1	0	2
0	1	1	1	0	3
1	0	0	1	0	4
1	0	1	1	0	5
1	1	0	1	0	6
1	1	1	1	0	7
0	0	0	0	1	8
0	0	1	0	1	9
0	1	0	0	1	10
0	1	1	0	1	11
1	0	0	0	1	12
1	0	1	0	1	13
1	1	0	0	1	14
1	1	1	0	1	15

Logic "1" > + 4.0V
Logic "0" < + 0.8V

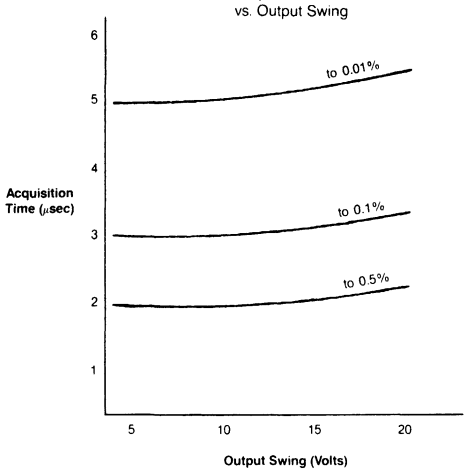
8 Differential Input Channels



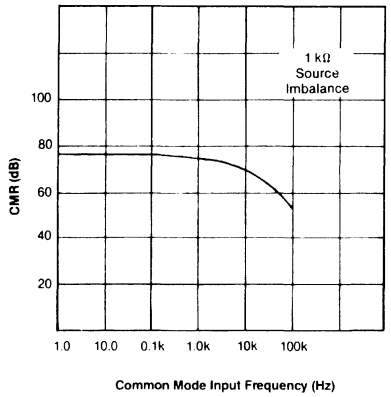
Address Inputs			Enable Inputs		On Channel
A_2	A_1	A_0	MUX 1	MUX 2	
X	X	X	0	1	ILLEGAL
X	X	X	1	0	ILLEGAL
X	X	X	0	0	NONE
0	0	0	1	1	0
0	0	1	1	1	1
0	1	0	1	1	2
0	1	1	1	1	3
1	0	0	1	1	4
1	0	1	1	1	5
1	1	0	1	1	6
1	1	1	1	1	7

Logic "1" > +4.0V
Logic "0" < +0.8V

MN7130
Acquisition Time
vs. Output Swing



MN7130
Common Mode Rejection
vs. Frequency



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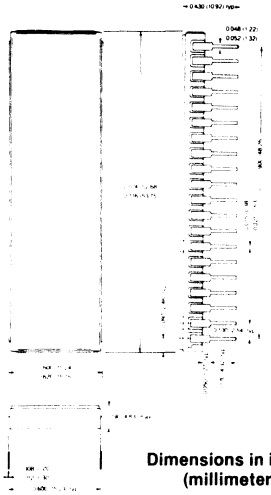
MN7140

12-Bit, 8-CHANNEL
DATA ACQUISITION SYSTEM

FEATURES

- **Complete DAS:**
  Input Multiplexer
  Address Register
  Instrumentation Amp
  Track-Hold Amp
  12-Bit A/D Converter
  Clock, Control Logic
- **Industry Standard 40-Pin Double-Wide DIP**
- **Random or Sequential Addressing**
- **±0.1%FSR Maximum Overall System Accuracy**
- **Adjustment-Free: No Gain or Offset Adjustments Necessary**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

40 PIN DIP



Dimensions in inches (millimeters)

DESCRIPTION

MN7140 is a complete 12-bit data acquisition system in an industry-standard, 40-pin, double-wide dual-in-line package. This unit contains an 8-channel input multiplexer (with latch and counter for either random or sequential addressing), a true instrumentation amplifier (G=1, Z_{in} =100MΩ), a track-hold amplifier (with internal hold capacitor), a 12-bit successive approximation A/D converter (with internal clock and reference), and all the timing and control logic necessary to operate the system with a single trigger pulse. The standard MN7140 has 8 single-ended inputs and can easily be expanded to 16 single-ended or 8 differential inputs with the addition of a single external multiplexer.

Active laser trimming of fully assembled units enables us to produce adjustment-free devices that guarantee performance equal to or exceeding all other modular and hybrid systems. Overall system linearity (±1/2LSB) and absolute accuracy (±0.1%FSR) are fully specified and guaranteed at all temperatures. The standard device is fully specified for either 0°C to +70°C or −55 C to +125°C ("H" model) operation. The MN7140H/B and MN7143H/B are available with Environmental Stress Screening while MN7140H/B CH and MN7143H/B CH are screened in accordance with MIL-H-38534. Contact factory for availability of "CH" devices.

For years, MN7140 was the only DIP-packaged 12-bit DAS to fully specify and guarantee linearity and overall system accuracy, without adjustment, over its entire operating temperature range. This feature, coupled with hermetic packaging and optional MIL-H-38534 screening make it the established choice for high-resolution military/aerospace and severe-environment industrial data acquisition applications. Its thin-film hybrid construction and low chip count ensure the highest reliability.

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MN7140 12-Bit 8-CHANNEL DATA ACQUISITION SYSTEM

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Specified Temperature	0°C to +70°C (Standard)
	−25°C to +85°C ("E" Model)
	−55°C to +125°C ("H" Model)
Storage Temperature	−65°C to +150°C
+15V Supply (Pin 20)	−0.5 to +18 Volts
−15V Supply (Pin 21)	+0.5 to −18 Volts
Logic Supply (Pin 23)	−0.5 to +16 Volts
Analog Inputs (Pins 1-4, 37-40)	±15 Volts
Digital Inputs (Pins 31-36, 11)	−0.5 to +Logic Supply

ORDERING INFORMATION

PART NUMBER — MN714X H/B CH

- Select MN7140 (±10V) or MN7143 (0 to +10V).
- Standard Part is specified for 0°C to +70°C operation. Add "E" suffix for specified −25°C to +85°C operation. Add "H" suffix for specified −55°C to+125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V, unless otherwise specified)

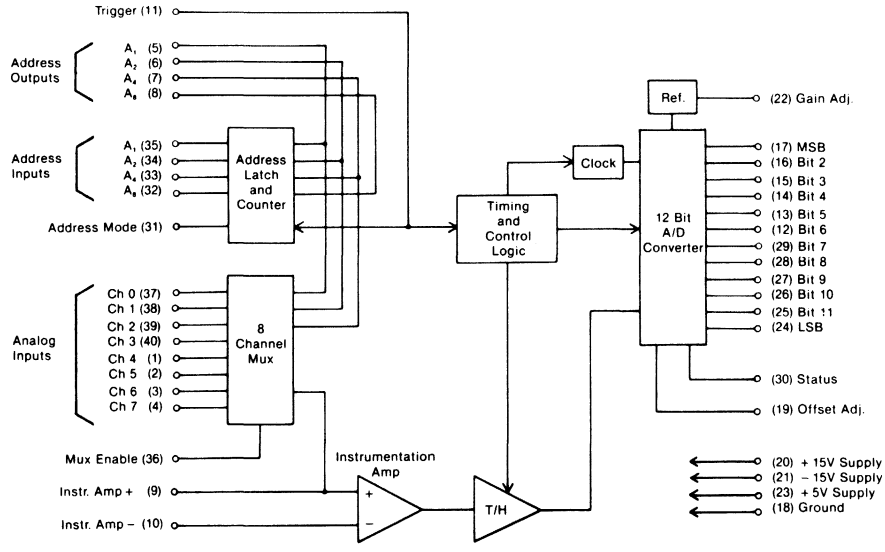
ANALOG INPUTS	MIN.	TYP.	MAX	UNITS
Number of Input Channels (Note 1)		8		Channels
Input Voltage Range (Note 2)		0 to +10V, ±10V		Volts
Input Impedance	100			Mohm
Input Capacitance		10		pF
Input Bias Current (Note 3): +25°C		10	25	nA
−55°C to +125°C			250	nA
CMRR (Note 4)		80		dB
DIGITAL INPUTS				
Logic Levels: Logic "1"				
Mux Enable	4			Volts
Other Inputs (Note 5)	3.5			Volts
Logic "0"				
Mux Enable			0.8	Volts
Other Inputs (Note 5)			1.5	Volts
Loading: Logic "1"				
Mux Enable		0.005	10	μA
Other Inputs (Note 5)		0.005	1.3	μA
Logic "0"				
Mux Enable		−0.005	−10	μA
Other Inputs (Note 5)		−0.005	−1.3	μA
Trigger Pulse Width	240			nSec
Setup Time, Address Mode and Address Inputs to Trigger (Note 6)	300			nSec
TRANSFER CHARACTERISTICS				
Linearity Error (Notes 7, 8):				
+25°C		±¼	±½	LSB
0°C to +70°C		±½	±1	LSB
−25°C to +85°C ("E" Model)		±½	±1	LSB
−55°C to +125°C ("H" Model)		±½	±1	LSB
Differential Linearity Error		±½		LSB
No Missing Codes		Guaranteed		
Absolute Accuracy Error (Notes 9, 10):				
+25°C		±0.05	±0.1	%FSR
0°C to +70°C		±0.15	±0.4	%FSR
−25°C to +85°C ("E" Model)		±0.15	±0.4	%FSR
−55°C to +125°C ("H" Model)		±0.2	±0.4	%FSR
Gain Error (Note 10)		±0.025		%
Gain Drift		±20		ppm/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time (20V Step to ±0.01%) (Note 11)		8	10	μSec
A/D Conversion Time		20	25	μSec
Throughput Rate (Channels/Sec.)	28.5	35		KHz
Full Power Bandwidth (Note 12)		250		KHz
Crosstalk (1KHz, 1KΩ Source Impedance)		−80		dB
Feedthrough (1KHz, 20Vp-p) (Note 13)		±0.01		%
DIGITAL OUTPUTS				
Digital Output Coding		Complementary Offset Binary		
Logic Levels (All Outputs): Logic "1" I_o = −10 μA	4			Volts
I_o = −360 μA	2.4			Volts
Logic "0" I_o = 10 μA			0.5	Volts
I_o = 360 μA			0.4	Volts

POWER SUPPLY REQUIREMENTS				
Power Supply Range: + 15V Supply − 15V Supply + 5V Supply	+ 14.55 − 14.55 + 4.75	+ 15.00 − 15.00 + 5.00	+ 15.45 − 15.45 + 5.25	Volts Volts Volts
Power Supply Rejection: + 15V Supply − 15V Supply + 5V Supply		± 0.003 ± 0.003 ± 0.001		%FSR/%Vs %FSR/%Vs %FSR/%Vs
Current Drains: + 15V Supply − 15V Supply + 5V Supply		30 − 50 10	50 − 75 16	mA mA mA
Power Consumption		1250	1955	mW

SPECIFICATION NOTES:

1. The standard MN7140 has 8 single-ended input channels. See page 6 for expanded single-ended and differential operation using additional external multiplexers.
2. Contact factory for other available input voltage ranges.
3. Input bias current specification is for the "on" multiplexer channel. "Off" channel leakage current is ± 50 nA maximum at all temperatures.
4. CMRR specification is for full differential operation using an external multiplexer. See page 6.
5. Other Digital Inputs include: ADDRESS INPUTS A_1, A_2, A_4, and A_8, and the ADDRESS MODE INPUT.
6. If using random addressing or if changing from one addressing mode to the other, ADDRESS INPUT or ADDRESS MODE information must be present a minimum of 300 nSec prior to the rising edge of TRIGGER.
7. Micro Networks tests and guarantees maximum linearity error at room temperature and at the high and low extremes of the specified operating temperature range. See Ordering Information.
8. One LSB for a 12 bit system corresponds to 0.024%FSR. See note 9.
9. FSR stands for Full Scale Range and is equivalent to the peak to peak voltage of the system's input range. For the MN7140, FSR = 20 volts, and 1 LSB = 4.88 mV.
10. See sections on Absolute Accuracy and Gain Errors for an explanation of how Micro Networks tests and specifies these parameters. the tutorial section of the Micro Networks Product Guide and Applications Manual for a complete discussion of DAS specifications.
11. The MN7140's internal timing control logic allows 10 μSec for channel switching, amplifier settling, and signal acquisition. See Summary of Operation.
12. This spec applies from analog input to the output of the internal S/H amplifier and it applies when the S/H is acquiring and tracking an analog input signal. It is the frequency at which a 20V-pp input/output sine wave becomes slew rate limited.
13. This spec also applies from the analog input to the output of the internal S/H amplifier and it applies when the S/H is holding an analog signal i.e., when the A/D converter is converting.

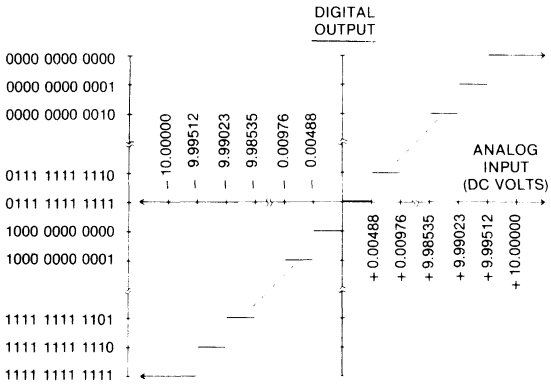
BLOCK DIAGRAM



ABSOLUTE ACCURACY ERROR

The MN7140 is a complete Data Acquisition System (DAS) including input multiplexer, instrumentation amplifier, track/hold amplifier (T/H), A/D converter, and control logic. Accuracy and linearity are specified for the complete system from analog input to digital output, eliminating the need for ordinarily important DAS component specifications such as instrumentation amp linearity, instrumentation amp gain accuracy, and T/H pedestal error.

Specifying the accuracy of the MN7140 as a system is similar to specifying the accuracy of an A/D converter. Portions of the MN7140's analog input/digital output transfer function are sketched below. Notice the quantization effect. A given digital output code is valid for a "band" or "range" of analog input voltages that theoretically, is 1 LSB wide. For the MN7140 (± 10V input range, 12 bit resolution), 1 LSB equals 4.88 mV. Ideally, any analog input between 4.88 mV and 9.76 mV should give a digital output of 0111 1111 1110. If we assign this code to the nominal midpoint of the band of input voltage for which it is valid, we can say that the 0111 1111 1110 digital output corresponds to analog inputs of +7.32 mV ±2.44 mV which can be written as +7.32 mV ± ½ LSB. The ± ½ LSB is an irreducible quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error, and its magnitude can be reduced only by going to higher resolution converters, i.e., ones that have smaller LSB's.



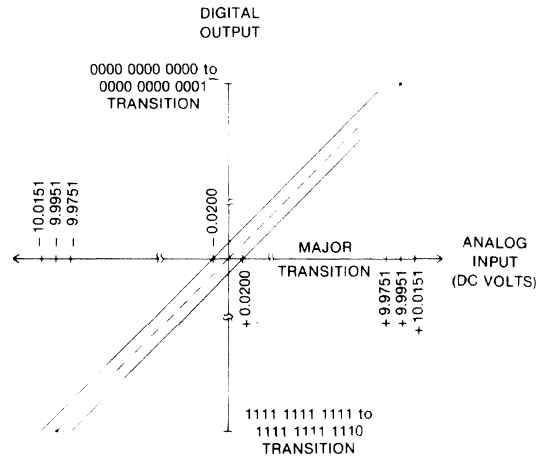
MN7140 INPUT/OUTPUT TRANSFER FUNCTION

It is difficult and time consuming to measure the center of a quantization band (the +7.32 mV in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the analog input voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted*, analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR. Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors. For the MN7140, Micro Networks tests Absolute Accuracy Error at both endpoints and the midpoint of the system transfer function.

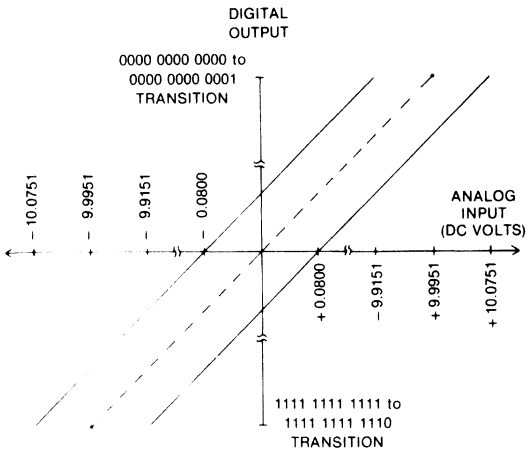
Return to the ideal analog input/digital output transfer function at the beginning of this discussion. Notice that the digital output data is supposed to change from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from −10.000V to −9.9951V. It should change from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to −9.9951V. This voltage, −9.9951V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The 1000 0000 0000 to 0111 1111 1111 transition (called the major transition because all the output bits change) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9951V.

For the MN7140, Micro Networks measures the three transition voltages just discussed. We perform these tests at +25°C and at 0°C and +70°C for commercial models and at −55°C and +125°C for "H" models (see Ordering Information). This testing, coupled with our linearity testing, allows us to guarantee that at +25°C, the analog input voltage at which any given digital output transition occurs will be within ±0.1%FSR (±20 mV) of its ideal value and that over the specified operating temperature range (−55°C to +125°C for "H" models), the analog input voltage at which any given digital output transition occurs will be within ±0.4%FSR (±80 mV) of its ideal value.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is represented by the broken line and the absolute accuracy limits by the solid lines. We guarantee that at +25°C, the MN7140's actual transfer function will be better than ± ½ LSB linear and that all the transition voltages will fall within the boundaries indicated. We also guarantee that at 0°C and +70°C for commercial models and at −55°C and +125°C for "H" models, the actual transfer function will be better than ±1 LSB linear, and the transition voltages will fall within the boundaries indicated.



MN7140 ABSOLUTE ACCURACY +25°C



MN7140H ABSOLUTE ACCURACY – 55°C, + 125°C

For temperatures intermediate to + 25 °C and the extremes of the specified operating temperature range, maximum Absolute Accuracy Errors can be found through interpolation. At + 75 °C, for example, the maximum Absolute Accuracy Error of the MN7140H will be ± 0.25% FSR.

OFFSET ERROR—We have not specified an Offset Error for the MN7140. Offset Error is an Absolute Accuracy Error, and it would be redundant and potentially confusing to specify Offset Error after giving an Absolute Accuracy Error that applies over the converter's full input range.

GAIN ERROR—Gain Error is the difference between the ideal and the measured values of the DAS's Full Scale Range (minus 2 LSB's); it is a measure of the slope of the DAS's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 0000 0000 0000 to 0000 0000 0001 transition minus that measured for the 1111 1111 1111 to 1111 1111 1110 transition.

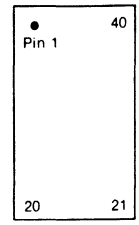
DIGITAL OUTPUT CODING

ANALOG INPUT (DC VOLTS)		DIGITAL OUTPUT
MN7143	MN7140	MSB LSB
0.0000	+ 10.0000	0000 0000 0000
+ 0.0024	+ 9.9951	0000 0000 000◊*
+ 0.0049	+ 0.0098	0111 1111 11◊◊*
+ 4.9976	+ 0.0049	0111 1111 111◊*
+ 5.0000	0.0000	◊◊◊◊ ◊◊◊◊ ◊◊◊◊*
+ 5.0024	– 0.0049	1000 0000 000◊*
+ 9.9951	– 0.0098	1000 0000 00◊◊*
+ 9.9976	– 9.9951	1111 1111 111◊*
+ 10.0000	– 10.0000	1111 1111 1111

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the DAS continuously acquiring and converting data, the output bits indicated as ◊ will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages and a sketch of the MN7140's transfer function.

The transition from output code 0000 0000 0000 to code 0000 0000 0001 will ideally occur at an input voltage of + 9.9951V. Subsequently, any input voltage greater than + 9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1110 to 1111 1111 1111 transition should occur at – 9.9951 volts. An input more negative than 9.9951 volts will give all "1's".

PIN DESIGNATIONS



1	Channel 4 Input	40	Channel 3 Input
2	Channel 5 Input	39	Channel 2 Input
3	Channel 6 Input	38	Channel 1 Input
4	Channel 7 Input	37	Channel 0 Input
5	Address Output (A_1)	36	Mux Enable
6	Address Output (A_2)	35	Address Input (A_1)
7	Address Output (A_4)	34	Address Input (A_2)
8	Address Output (A_8)	33	Address Input (A_4)
9	Mux Output, Amp In (+)	32	Address Input (A_8)
10	Instr. Amp Input (–)	31	Address Mode
11	Trigger Input	30	Status Output (E.O.C.)
12	Bit 6	29	Bit 7
13	Bit 5	28	Bit 8
14	Bit 4	27	Bit 9
15	Bit 3	26	Bit 10
16	Bit 2	25	Bit 11
17	Bit 1 (MSB)	24	Bit 12 (LSB)
18	Ground	23	Logic Supply (+Vdd)
19	Offset Adjust	22	Gain Adjust
20	+ 15V Supply (+ Vcc)	21	– 15V Supply (– Vcc)

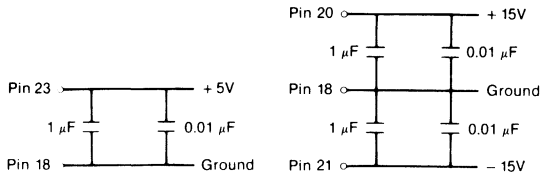
APPLICATIONS INFORMATION

The digital circuitry used in the MN7140 is CMOS. The standard precautionary measures for handling CMOS should be followed. For standard single-ended operation, Pin 10 (the minus input to the internal instrumentation amplifier) should be grounded, and Pin 36 (multiplexer enable) should be tied to a logic "1".

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN7140. The unit's GROUND (Pin 18) should be connected to system analog ground, preferably through a large ground plane underneath the package. Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Analog input runs should be well separated from digital clock lines and other noise sources. The OFFSET ADJUST point (Pin 19) is particularly noise susceptible. Care should be taken to avoid long analog runs or runs close to digital lines when utilizing this input.

When external offset adjustment is employed (see page 7), the 3.3 megohm resistor and trimpot should be located as close to the package as possible. Whether or not external gain adjustment is used (see page 7), a 0.01 μF ceramic bypass capacitor should be located close to the package connecting the GAIN ADJUST point (Pin 22) to analog ground.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the MN7140. For optimum performance and noise rejection, 1 μF capacitors paralleled with 0.01 μF ceramic capacitors should be used as shown in the diagram below.



POWER SUPPLY DECOUPLING

SUMMARY OF OPERATION—The rising edge of a TRIGGER pulse loads the multiplexer (Mux) channel address and initiates a data acquisition and conversion cycle. If sequential addressing is being used (see below), the next channel will be accessed. If random addressing is being used, the channel whose address has been applied to the CHANNEL ADDRESS INPUTS will be accessed. The rising edge of the TRIGGER pulse simultaneously fires an internal one-shot (10 μSec pulse duration) whose output disables the internal clock. 10 μSec later, the falling edge of the one-shot drives the track/hold amp (T/H) into the hold mode, gates on the clock, generates a start convert signal for the 12 bit A/D converter, and drives the STATUS OUTPUT to a logic "1". Gating off the clock during the time the Mux is settling into its new channel and the T/H is acquiring a new signal reduces noise errors. When the conversion is complete (approximately 20 μSec later), the STATUS output returns to a logic "0" indicating that the conversion is complete, that the digital output is valid, and that the T/H amplifier has returned to the tracking mode. The unit is now ready to be triggered for the acquisition and conversion of the next channel.

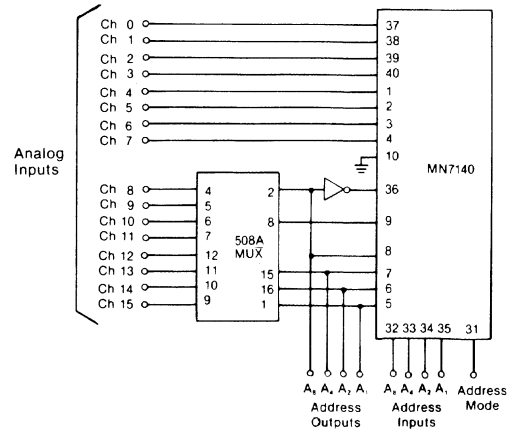
ADDRESSING—The MN7140's input channels may be randomly or sequentially addressed. For random addressing, the ADDRESS MODE input (Pin 31) must be tied to a logic "0" and the desired channel address (in 8421 binary) applied to the CHANNEL ADDRESS INPUTS (Pins 32-35). In this addressing mode, the MN7140's internal address latch/counter acts as a 4 bit parallel register. The rising edge of the TRIGGER pulse latches the new channel address and initiates the data acquisition and conversion cycle. If the MN7140 is not being expanded (see below) and only its 8 internal channels are being used, the A_8 address bit (Pin 32) is unnecessary, and this input can be tied either high or low but should not be left open.

For sequential addressing, the ADDRESS MODE input (Pin 31) must be tied to a logic "1". In this mode, the internal address latch/counter acts as a 4 bit binary counter. Each rising edge of the TRIGGER input will increment the channel address and initiate the data acquisition and conversion cycle. Channel 0000 will be accessed after channel 1111. As one changes from random to sequential addressing, the next channel accessed will be one higher than the channel last randomly addressed. Changing digital data appearing at the ADDRESS INPUTS will not affect the MN7140 when it is in the sequential addressing mode.

SEQUENTIAL ADDRESSING CONTINUOUS CONVERSIONS—The MN7140 can be made to continuously sequence through channels acquiring and converting data by applying a logic "1" to the ADDRESS MODE input (Pin 31) and inverting the STATUS output (Pin 30) and tying it back to the TRIGGER INPUT (Pin 11). In this mode, the STATUS OUTPUT going low at the end of a conversion becomes the rising TRIGGER edge that addresses the next channel and initiates the next data acquisition and conversion cycle. After each channel has been converted and the STATUS has dropped to a "0", the output data will be valid for approximately the next 10 μSec while the multiplexer is switching channels and the T/H is acquiring the new signal. The falling edge of STATUS may be used to latch output data into an external receiving register (please read the section describing the STATUS output). When continuously converting, an external TRIGGER signal should be provided at power-on to avoid possible latch-up.

CHANNEL ADDRESS OUTPUTS—The MN7140's CHANNEL ADDRESS OUTPUTS (Pins 5-8) are tied directly to the unit's internal address counter/latch. They indicate, in 8421 binary, the multiplexer channel presently being accessed. When using external multiplexers for differential or expanded single-ended operation (see below), these outputs can be used to address the external multiplexers, eliminating the need for any additional address decoding circuitry. When using sequential addressing, the appropriate CHANNEL ADDRESS OUTPUTS can be NORed together to generate a frame sync pulse each time channel 7 (8 channel systems) or channel 15 (16 channel systems) is being addressed. In microprocessor-based systems, the ADDRESS OUTPUTS can be 3-state buffered to add channel read-back capability.

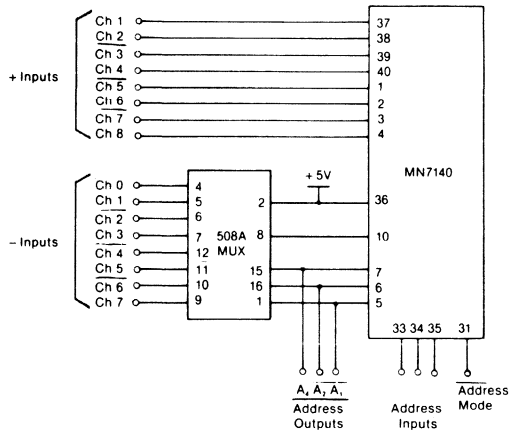
CHANNEL EXPANSION—The MN7140's input capabilities can be expanded beyond the 8 basic channels with the addition of external analog multiplexers. The diagram below shows a 16 channel single-ended system using an external 508A type multiplexer. Note that no additional address



16 SINGLE-ENDED INPUT CHANNELS

decoding circuitry is necessary. The MN7140's internal address latch/counter (see above) is a 4 bit unit that can be used to either randomly or sequentially address up to 16 channels. For further expansion, additional mux's can be tied to Pin 9 (the noninverting input to the internal instrumentation amplifier) or cascaded in front of the MN7140's internal mux. Remember that for single-ended operation, Pin 10 (the minus input to the internal instrumentation amplifier) has to be grounded.

DIFFERENTIAL INPUT OPERATION—The MN7140 can be configured for 8 differential input channels with the addition of a single external multiplexer. A system using a 508A type multiplexer is shown below. No additional address decoding circuitry is necessary. Further expansion is possible with additional mux's tied to Pins 9 and 10 (the inputs to the internal instrumentation amplifier).



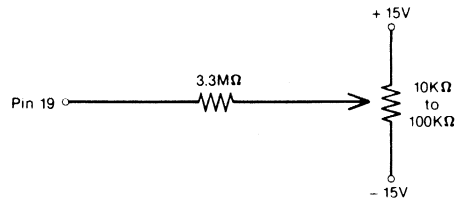
8 DIFFERENTIAL INPUT CHANNELS

PIN 36 MULTIPLEXER ENABLE—When Pin 36 has a logic "0" applied, the MN7140's internal mux is disabled. When Pin 36 has a logic "1" applied, the internal mux is enabled and can be accessed through ADDRESS INPUTS A_1, A_2, and A_4 (Pins 33-35).

STATUS OUTPUT (E.O.C.)—The STATUS or END OF CONVERSION (E.O.C.) output (Pin 30) indicates whether the MN7140 is tracking or converting an input signal. When STATUS is a logic "0", the MN7140's internal T/H amplifier is in the tracking mode and digital output data from the previous conversion is still valid. When the STATUS is a logic "1", the T/H is in the hold mode, and the internal A/D is converting. The output data is not valid. The falling edge of STATUS indicates that the conversion is complete, that the output data is valid, and that the T/H has returned to the tracking mode. Output data will be valid and enabled a minimum of 300 nsec before STATUS returns low.

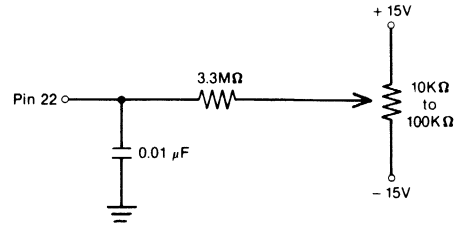
OPTIONAL OFFSET AND GAIN ADJUSTMENTS—The MN7140 will operate as specified without additional adjustments. If desired, however, Absolute Accuracy Error can be reduced to ± 1 LSB by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the Offset Adjustment must be made before the Gain Adjustment. Multiturn potentiometers with TCR'S of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ± 20% carbon composition or better. If these adjustments are not used, Pins 19 and 22 should be left open. Do not ground.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown, and apply an analog input voltage of −9.9951V. With the MN7140 performing repeated conversions, adjust the offset potentiometer down until all the output bits are "1". Then adjust up until the LSB just turns to a "0".



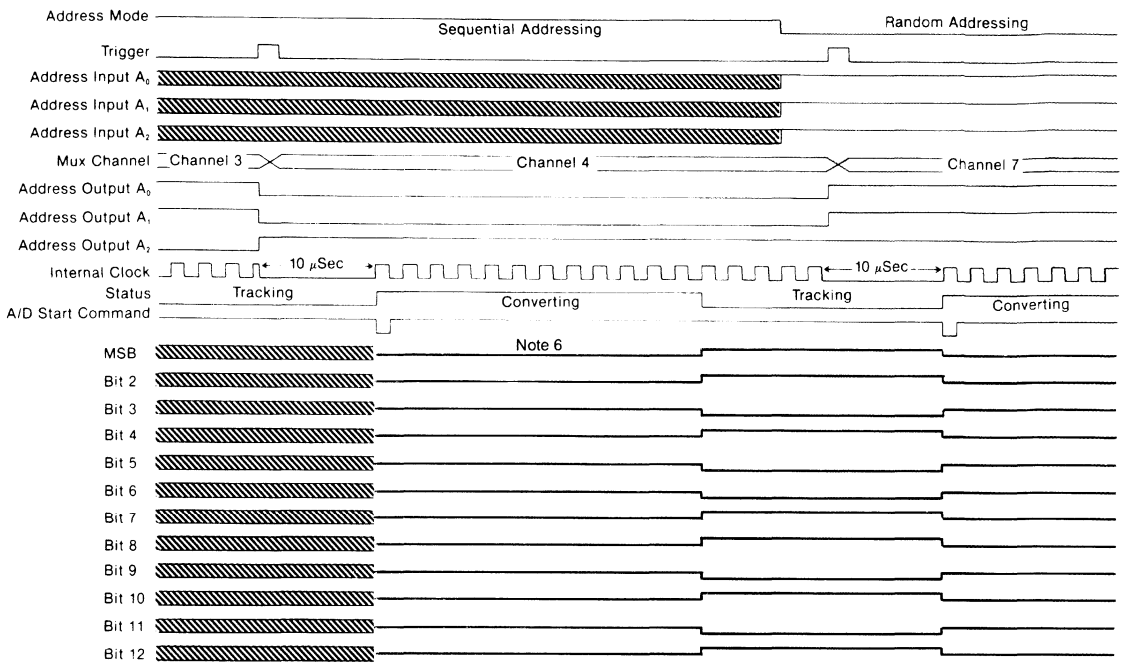
OFFSET ADJUSTMENT

GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply an analog input voltage of + 9.9951V. With the MN7140 performing repeated conversions, adjust the gain potentiometer up until all the output bits are "0". Then adjust down until the LSB just turns to a "1".



GAIN ADJUSTMENT

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. For sequential addressing, set ADDRESS MODE = "1". For random addressing, set ADDRESS MODE = "0".
2. The minimum TRIGGER pulse width is 240 nSec, but the TRIGGER does not have to be brought back down for the acquisition and conversion cycle to continue.
3. In the random addressing mode, ADDRESS INPUT data must be valid at least 300 nSec prior to TRIGGER.
4. The rising edge of TRIGGER disables the internal clock for 10 μSec during signal acquisition.
5. When STATUS = "1" the internal T/H is in the hold mode, and the A/D converter is performing a conversion. When STATUS = "0", the conversion is complete; output data is valid; and the T/H has returned to the track mode.
6. All output bits are 3-stated during the A/D conversion. They become valid and enabled a minimum of 300nsec before STATUS returns low.
7. Operation shown is for the digital word 1101 0011 0101 which corresponds to an analog input of −6.5137V.
8. Conversion time is defined as the time the STATUS output is high.
9. Once an acquisition and conversion cycle has begun, it cannot be stopped by applying another TRIGGER pulse.
10. When the system is initially "powered up", it may come on at any point in the cycle.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7145 Series

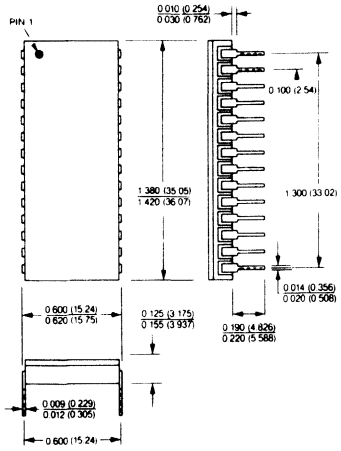
MICRO NETWORKS

8-CHANNEL, 12-Bit
DATA ACQUISITION SYSTEM
with μP INTERFACE

FEATURES

- **Complete, 8-Channel, 12-Bit DAS with MUX, T/H, ADC, Ref. and 3-State Output**
- **25,000 Channels/sec Guaranteed Throughput**
- **Microprocessor Interface (3-State Output, Address Line, Read/Convert, etc.)**
- **Small 28-Pin Side-Brazed DIP**
- **18 Models (3 Input Voltage Ranges)**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

28 PIN DIP



Dimensions In Inches (millimeters)

DESCRIPTION

The MN7145, MN7146 and MN7147 are complete, single-package, 8-channel, 12-bit, data acquisition systems with internal decoding logic and 3-state output buffers which greatly facilitate microprocessor control. Packing a lot of function into a 28-pin, side-brazed, ceramic DIP, MN7145 Series DAS's each contain an 8-channel, overvoltage protected (±35V) multiplexer; a high-speed (10μsec), high-impedance ($10^{10}\Omega$), T/H amplifier; a high-speed (25μsec), 12-bit A/D with reference and clock; and all the timing and control logic (3-state buffer, address line, read/convert line) necessary for μP control. System throughput rate is guaranteed at 25,000 channels/sec for full rated accuracy.

These devices are manufactured using contemporary hybrid assembly techniques, and they illustrate the technology's ability to combine I.C.'s made with different processing technologies into a single functional design that takes advantage of the best aspects of each semiconductor technology. The overvoltage protected mux is CMOS. The T/H is high-speed bipolar with an npo hold cap. The A/D combines high-speed bipolar technology with state-of-the-art thin-film technology and TTL compatible CMOS. Active laser trimming of fully assembled devices compensates for summed accuracy and linearity errors to produce overall system linearity (±½LSB) and accuracy (±0.05%FSR offset error) that may not be achievable when assembling a similar system with individual components. Small size, low power (1 Watt max), high sampling rate and low cost may make the MN7145 Series the most economical way possible to achieve multichannel, 12-bit, data acquisition today.

MN7145 (0 to +10V input range), MN7146 (±5V) and MN7147 (±10V) are fully specified over both 0°C to +70°C (J and K models) and −55°C to +125°C (S and T models) temperature ranges. Assorted linearity grades (±½LSB, ±1LSB) at room temperature and over temperature are available as outlined in the specification table. All devices guarantee "no missing codes" over temperature (to either the 12-bit or 11-bit level).

February 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7145 SERIES 8-CHANNEL, 12-Bit, DATA ACQUISITION SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
J and K Models	0°C to +70°C
S. S/B, T, T/B Models	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 19)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 7)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 6)	0 to +7 Volts
Digital Inputs (Pins 3, 4, 8-10)	−0.5 to (+Vdd +0.5) Volts
Analog Inputs: (Pins 11-18)	±Vcc ±20V
(Pins 20, 21)	±Vcc

ORDERING INFORMATION

PART NUMBER — MN714XX/B CH

- Select MN7145 (0 to +10V), MN7146(±5V) or MN7147(±10V)
- Select suffix J,K,S or T for desired performance and specified temperature range.
- Add "/B" to "S" or "T" models for Environmental Stress Screening
- Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels		8 Single-Ended		
Input Voltage Ranges: MN7145 MN7146 MN7147		0 to +10 ±5 ±10		Volts Volts Volts
Input Impedance (Note 2): On Channel Off Channels		10^{10} / 100 10^{10} / 10		Ω/pF Ω/pF
Input Bias Current (On Channel): +25°C (Note 2) T_{min} to T_{max} (Note 3)		±1 ±50	 ±250	nA nA
Input Leakage Current (Off Channels, Note 2): +25°C T_{min} to T_{max} (Note 3)		±1 ±50		nA nA
DIGITAL INPUTS				
Logic Levels: A_0, R/$\overline{C}$: Logic "1" Logic "0" MA_0-MA_2 (Note 4): Logic "1" Logic "0"	+2.4 −0.5 +4.0 0		+5.5 +0.8 +5.5 +0.8	Volts Volts Volts Volts
Logic Currents (All Inputs): Logic "1" Logic "0"			±10 ±10	μA μA
DIGITAL OUTPUTS (Status, DBO-DB11)				
Output Coding (Note 5): Unipolar Ranges Bipolar Ranges		Straight Binary Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 500\mu A$) Logic "0" ($I_{sink} \leq 1.6mA$)	+2.4		 +0.4	Volts Volts
Leakage (DBO-DB11) in High-Z State		±1	±10	μA
Output Capacitance (Note 2)		5		pF
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supplies +V_{dd} Supply	±13.5 +4.5	±15 +5	±16.5 +5.5	Volts Volts
Power Supply Rejection (Note 6): +V_{CC} Supply −V_{CC} Supply +V_{dd} Supply		±0.002 ±0.002 ±0.002	±0.005 ±0.005 ±0.005	%FSR/% Supply %FSR/% Supply %FSR/% Supply
Current Drains: +V_{CC} Supply −V_{CC} Supply +V_{dd} Supply		+18 −26 +10	+25 −35 +20	mA mA mA
Power Consumption		710	1000	mW
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 7): 12-Bit Conversion 8-Bit Conversion		20 13	25 17	μsec μsec
Throughput Rate	25	35		kHz

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, ±Vcc = ±15V, + Vdd = +5V unless otherwise indicated) (Note 8)

MODEL	MN7145J MN7146J MN7147J	MN7145K MN7146K MN7147K	MN7145S MN7146S MN7147S	MN7145T MN7146T MN7147T	UNITS
Integral Linearity Error:					
Initial (+25°C) (Maximum)	±1	±½	±1	±½	LSB
T_{min} to T_{max} (Maximum, Note 3)	±1	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed:					
Initial (+25°C)	11	12	11	12	Bits
T_{min} to T_{max} (Note 3)	11	12	11	12	Bits
Unipolar Offset Error (Notes 9,10):					
Initial (+25°C) (Maximum)	±0.05	±0.05	±0.05	±0.05	% FSR
Drift (Maximum)	±15	±10	±25	±20	ppm of FSR/°C
Bipolar Offset Error (Notes 9,11):					
Initial (+25°C) (Maximum)	±0.25	±0.1	±0.25	±0.1	% FSR
Drift (Maximum)	±25	±20	±25	±20	ppm of FSR/°C
Gain Error (Notes 9,12):					
Initial (+25°C) (Maximum)	±0.3	±0.3	±0.3	±0.3	%
Drift (Maximum)	±50	±25	±50	±25	ppm/°C

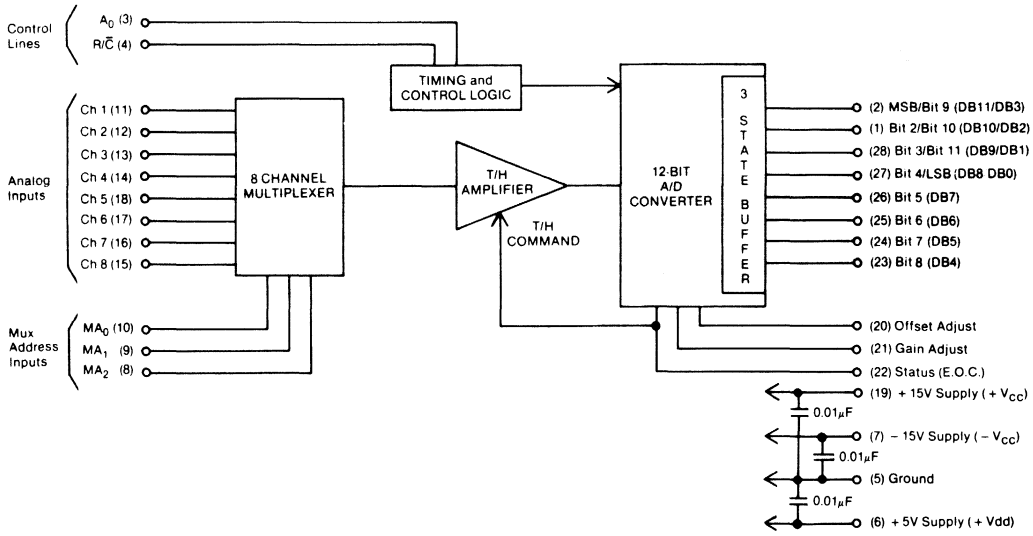
SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet. FSR = Full Scale Range. MN7145 (0 to +10V input voltage range) and MN7146 (±5V input voltage range) have a 10V FSR. MN7147 (±10V input voltage range) has a 20V FSR.
2. These parameters are listed for reference only and are not tested.
3. J and K models are fully specified for 0°C to +70°C operation. S, S/B, T and T/B models are fully specified for −55°C to +125°C operation. See ordering information.
4. If the multiplexer inputs are driven from standard TTL logic, 1kΩ pullup resistors to +5V should be used.
5. See table of transition voltages in section labeled Digital Output Coding.
6. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
7. Whenever the Status Output (pin 22) is low (logic "0"), the internal T/H is in the track mode and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
8. All performance specifications are specified and tested while sampling and converting at a 25kHz throughput rate.
9. Adjustable to zero with external potentiometer.
10. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN7145 on its unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
11. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN7146 or MN7147 on a bipolar range. The ideal value at which this transition should occur is −F.S. +½LSB. See Digital Output Coding.
12. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

BLOCK DIAGRAM

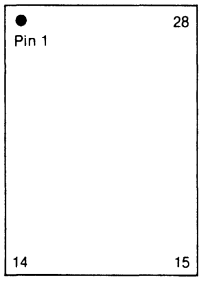


ORDERING INFORMATION

Part Number	Input Voltage Range	Specified Temp. Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	No Missing Codes Over Temp.	Guaranteed Throughput Rate (Channels/sec)	Package
MN7145J	0 to +10V	0°C to +70°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7145K	0 to +10V	0°C to +70°C	±½	±½	12 Bits	25,000	28-Pin DIP
MN7145S	0 to +10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7145S/B (2)	0 to +10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7145T	0 to +10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7145T/B (2)	0 to +10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7146J	±5V	0°C to +70°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7146K	±5V	0°C to +70°C	±½	±½	12 Bits	25,000	28-Pin DIP
MN7146S	±5V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7146S/B (2)	±5V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7146T	±5V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7146T/B (2)	±5V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7147J	±10V	0°C to +70°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7147K	±10V	0°C to +70°C	±½	±½	12 Bits	25,000	28-Pin DIP
MN7147S	±10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7147S/B (2)	±10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7147T	±10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7147T/B (2)	±10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP

1. Maximum error expressed in LSB's for 12 bits.
2. Includes 100% screening to MIL-STD-883.

PIN DESIGNATIONS



1 Bit 2/Bit 10 (DB10/DB2)
2 MSB/Bit 9 (DB11/DB3)
3 Address Line (A_0)
4 Read/Convert (R/$\overline{C}$)
5 Ground
6 +5V Supply (+V_{dd})
7 −15V Supply (−V_{CC})
8 Mux Address A_2 (MA_2)
9 Mux Address A_1 (MA_1)
10 Mux Address A_0 (MA_0)
11 Channel 1 Input
12 Channel 2 Input
13 Channel 3 Input
14 Channel 4 Input
28 Bit 3/Bit 11 (DB9/DB1)
27 Bit 4/LSB (DB8/DB0)
26 Bit 5 (DB7)
25 Bit 6 (DB6)
24 Bit 7 (DB5)
23 Bit 8 (DB4)
22 Status (E.O.C.)
21 Gain Adjust
20 Offset Adjust
19 +15V Supply (+V_{CC})
18 Channel 5 Input
17 Channel 6 Input
16 Channel 7 Input
15 Channel 8 Input

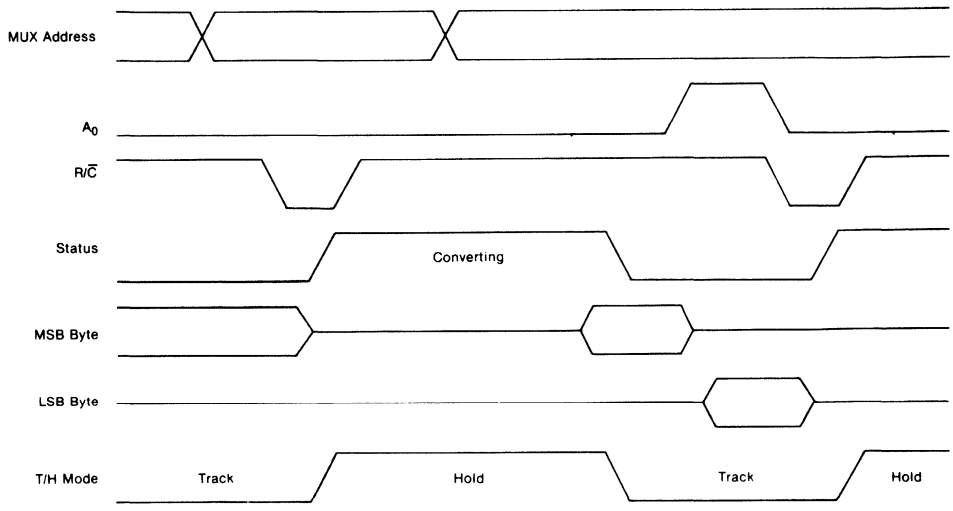
APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — MN7145 Series devices are 8-channel, 12-bit, data acquisition systems with internal 8-channel multiplexer, track-hold (T/H) amplifier, 12-bit analog-to-digital (A/D) converter, and microprocessor interface logic (3-state buffer, address line, read/convert line). A minimal amount of signals need to be supplied externally to these devices in order to achieve true multichannel data acquisition. High input impedance and low input bias currents allow analog signal sources to be connected directly to the multiplexer inputs. Multiplexer channels are randomly selected via three mux address lines (MA_0, MA_1, MA_2). The T/H is controlled directly by the A/D and requires no external commands. The address (A_0) and read/convert (R/$\overline{C}$) lines are used in assorted combinations to: initiate (write) 12-bit conversions, initiate 8-bit conversions, read back MSB data and read back LSB data. In normal operation, a mux address is selected (000 = channel 1, 111 = channel 8), and time must be allowed for the mux to switch and settle and for the T/H to acquire and track the new analog input signal. Then the A/D conversion is initiated by dropping the R/$\overline{C}$ line. Once a conversion has been initiated, the device's Status output (pin 22) rises to a logic "1" signaling that a conversion is in progress. This action drives the T/H into the hold mode instantaneously "freezing" the appropriate analog input and holding it constant while the A/D conversion proceeds. When the conversion is complete, Status drops back to a logic "0"; the T/H is driven back into the track mode; and output data is held in a 3-state buffer ready to be read. At this point, output data is available in two 8-bit bytes (multiplexed on a single set of output lines) and can be enabled by bringing R/$\overline{C}$ high and toggling A_0 (A_0 = "0" enables MSB data byte; A_0 = "1" enables LSB data byte). If R/$\overline{C}$ is brought high during a conversion, output data is automatically enabled when the conversion is complete. The output data lines return to the high-impedance state when R/$\overline{C}$ is brought low initiating a new conversion.

The multiplexer address can be changed during or after a conversion. In order to achieve maximum device performance, the multiplexer address may be changed 1μsec after initiating a conversion. If the multiplexer is updated in this fashion, and a new channel is selected while a conversion is in process, the T/H will immediately start to acquire and track

the new analog input signal when the conversion is complete. This allows the microprocessor to read output data while the T/H is acquiring the next analog input signal. The diagram below illustrates the relationships of the timing signals previously discussed. For more detailed timing information, see the timing section of this data sheet.

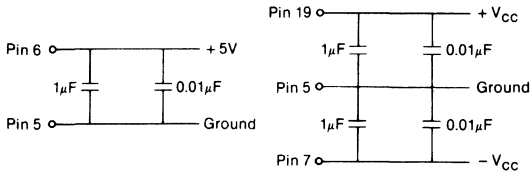
TIMING DIAGRAM



LAYOUT CONSIDERATIONS AND GROUNDING—Proper attention to layout and decoupling is necessary to obtain specified accuracy from MN7145 Series devices. It is critically important that the devices' power supplies be filtered, well-regulated and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power-supply pins; the supply decoupling capacitors should be connected directly from Vdd (pin 6), + Vcc (pin 19) and − Vcc (pin 7) to Ground (pin 5). Suitable decoupling capacitors are 1μF tantalum types in parallel with 0.01μF ceramic discs. See diagram below.

POWER SUPPLY DECOUPLING



Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Analog input runs should be well separated from digital clock lines and other noise sources. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the device as possible. If external adjustment potentiometers are not used, Offset Adjust (pin 20) and Gain Adjust (pin 21) should be left open. Do not ground.

Ground (pin 5) should be connected to system analog ground as close to the unit as possible, preferably through a large analog ground plane beneath the package.

CONTROL FUNCTIONS—Operating MN7145 Series devices under microprocessor control is most easily understood by examining the control-line funtions in a truth table. Table 1 below is a summary of the control-line functions. Table 2 is the control-line truth table.

Table 1: MN7145 Series Control Line Functions

Pin Designations	Definition	Function
MA_0-MA_2 (Pins 8-10)	MUX Address In	Selects MUX channel to be held and converted.
R/$\overline{C}$ (Pin 4)	Read/Convert ("1" = Read) ("0" = Convert)	R/$\overline{C}$ 1→0 edge is used to initiate 8 or 12-bit conversions. R/$\overline{C}$ = "1" enables output data during a read cycle.
A_0 (Pin 3)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data, A_0 selects the output data format. A_0 = "0" enables high and middle bits. A_0 = "1" enables low bits and trailing "0's".

Multiplexer input channels on MN7145 Series devices are randomly accessed via Address lines (MA_0, MA_1, MA_2). The multiplexer address may be changed after a conversion cycle is complete. However, if desired, the multiplexer address may be changed during a conversion cycle. If doing so, caution must be used to ensure that the address is not updated within 1μsec of having initiated the conversion.

The Read/Convert input (R/$\overline{C}$, pin 4) is used in combination with the Byte Address/Short Cycle input (A_0, pin 3) to initiate either 8 or 12-bit conversion cycles and to read back output data stored in the A/D's 3-state output buffer. Conversion cycles are initiated by bringing R/$\overline{C}$ low. Read cycles are initiated by bringing R/$\overline{C}$ high. R/$\overline{C}$ may remain low during a conversion or it may be brought back high. If it is returned high, it must be done so within 1.5μsec after the conversion begins. If R/$\overline{C}$ is left low during a conversion, it should not be brought high until after the status line has fallen indicating that the conversion is complete.

Output data is only enabled when Status = "0" and R/$\overline{C}$ = "1". However, if R/$\overline{C}$ has been brought high during the conversion, output data will automatically be enabled 300nsec (minimum) prior to the fall of Status. If R/$\overline{C}$ is left low during a conversion, the output lines will remain in the high-impedance state when Status returns low. R/$\overline{C}$ must then be brought high to read output data.

The Byte Address/Short Cycle input (A_0, pin 3) is used in combination with R/$\overline{C}$ when initiating conversions and reading output data. When initiating a conversion, the signal applied to A_0 determines whether a 12-bit (A_0 = "0") or an 8-bit conversion is initiated (A_0 = "1"). As discussed earlier, conversion cycles are initiated by the falling edge of R/$\overline{C}$. When reading digital output data from MN7145 Series devices, the signal applied to A_0 determines which 8-bit data byte is multiplexed to the eight digital output lines. When A_0 = "0", the MSB byte (MSB through bit 8) is enabled. When A_0 = "1", the LSB byte (bit 9 through LSB) is enabled.

Table 2: MN7145 Series Truth Table

Control Lines					
R/$\overline{C}$	A_0	MA_2	MA_1	MA_0	Device Operation
X	X	0	0	0	Select MUX Channel 1
X	X	0	0	1	Select MUX Channel 2
X	X	0	1	0	Select MUX Channel 3
X	X	0	1	1	Select MUX Channel 4
X	X	1	0	0	Select MUX Channel 5
X	X	1	0	1	Select MUX Channel 6
X	X	1	1	0	Select MUX Channel 7
X	X	1	1	1	Select MUX Channel 8
1→0	0	X	X	X	Initiate 12-Bit Conversion on Selected Channel
1→0	1	X	X	X	Initiate 8-Bit Conversion on Selected Channel
1	0	X	X	X	Enable 8 MSB's (high and middle bits)
1	1	X	X	X	Enable 4 LSB's (low bits) and 4 trailing "0's"
0	X	X	X	X	Output Data Disabled (high-impedance state)

TABLE 1. TABLE 2 NOTES:

1. "1" indicates TTL logic high (2.4V minimum).
2. "0" indicates TTL logic low (0.8V maximum).
3. X indicates "don't care".
4. 1→0 indicates logic transition (falling edge).
5. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

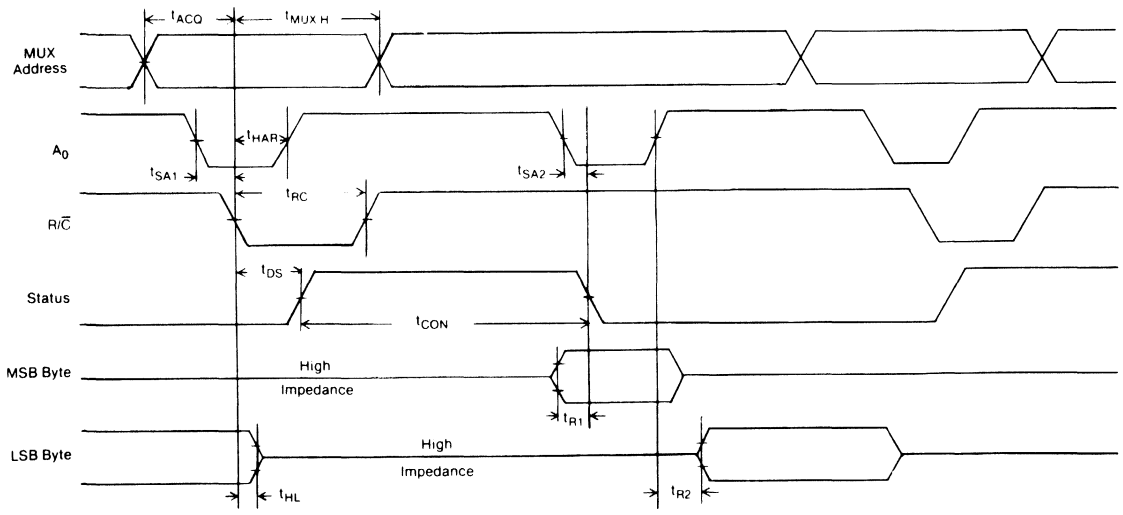
TIMING - MUX ADDRESSING—MN7145 Series devices' input multiplexer is randomly addressed by applying the desired channel address (000 = channel 1, 111 = channel 8) to the address lines (MA_0, MA_1, MA_2). Once the desired channel is selected, 10μsec must be allowed for T/H acquisition time (t_{ACQ}) prior to initiating a conversion. The multiplexer address may be updated as early as 1μsec (t_{MUXH}) after the conversion cycle has begun if this is necessary to meet system timing requirements. This address hold time (t_{MUXH}) ensures that the T/H amplifier has fully switched into the hold mode prior to being presented with the signal on the next channel.

TIMING - INITIATING CONVERSIONS—As stated earlier, the falling edge of R/$\overline{C}$ in combination with A_0 initiates either 8-bit conversion cycles (A_0 = "1") or 12-bit conversion cycles (A_0 = "0"). If the multiplexer address has been changed prior to initiating a conversion, a minimum of 10μsec must be allowed for T/H acquisition time. As stated earlier, the multiplexer address may be changed during an ongoing conversion. In this case, the T/H will be commanded back into the track mode and will start acquiring the new channel's signal as soon as the ongoing conversion is complete.

Timing for a typical 12-bit conversion cycle is shown below. In this example, the multiplexer is addressed; 10μsec T/H acquisition time is allowed; and A_0 is set to a logic "0" all prior to initiating the 12-bit conversion cycle. A_0 must remain valid for 50nsec while R/$\overline{C}$ is low to ensure that a 12-bit conversion cycle is properly initiated (t_{HAR} = 50nsec min.). Status output rises to a logic "1" 200nsec after R/$\overline{C}$ is brought low (t_{DS} = 200nsec max.) commanding the T/H amplifier into the hold mode and signaling that a conversion cycle is in progress. While Status is high, the output buffers return to the high-impedance state and output data cannot be read. The multiplexer address is updated after a minimum address hold time of 1μsec (t_{MUXH} = 1μsec min.). In this example, R/$\overline{C}$ is returned high during the conversion cycle so that output data will be automatically enabled upon completion of the cycle. Once a conversion has started, additional R/$\overline{C}$ falling edges will be ignored. However, if A_0 changes state after a conversion begins, additional R/$\overline{C}$ falling edges will latch the new state of A_0, possibly causing a wrong cycle length (8 vs. 12 bits) for that conversion. Not shown in the example below, R/$\overline{C}$ may remain low during the conversion in which case the output data will remain in the high-impedance state when Status returns low at the end of the conversion. Output data can then be enabled by bringing R/$\overline{C}$ high and asserting A_0 as desired.

TIMING - RETRIEVING DATA—When the conversion cycle is complete and Status output is low, the combination of signals applied to R/$\overline{C}$ and A_0 allows output data bytes to be read (A_0 = "0" MSB byte, A_0 = "1" LSB byte). In the example below, R/$\overline{C}$ is returned high during the conversion, and A_0 is set so that the MSB byte is automatically enabled 300nsec before the end of the conversion cycle. After the MSB byte has been accessed by the system, the LSB byte is multiplexed to the data output lines by bringing A_0 high. Break-before-make action ensures that MSB and LSB data bytes will not be enabled at the same time. Data access time is 150nsec from the change of A_0 (t_{R2} = 150nsec max.). If one desires, R/$\overline{C}$ may remain low during the conversion, in which case, output data will not be enabled until Status is low and R/$\overline{C}$ is brought high. In this case, data access from R/$\overline{C}$ = "1" is similarly 150nsec.

TIMING DIAGRAM



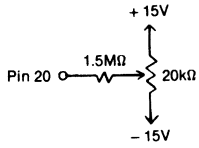
MN7145 Series Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{ACQ}	T/H Acquisition Time	10	6		μsec
t_{MUXH}	Multiplexer Address Hold Time	1			μsec
t_{SA1}	A_0 Setup to R/C̄ Low	0			nsec
t_{SA2}	A_0 Setup to Status Low	100	50		nsec
t_{HAR}	A_0 Valid During R/C̄ Low	50			nsec
t_{RC}	R/C̄ Pulse Width	50			nsec
t_{DS}	Status Delay from R/C̄ Low		100	200	nsec
t_{R1}	Status Delay After Data Valid	300	500	1000	nsec
t_{R2}	Data Access Time from A_0		60	150	nsec
t_{HL}	Data Valid After R/C̄ Low	25			nsec
t_{CON}	Conversion Time:				
	8-Bit Cycle	10	13	17	μsec
	12-Bit Cycle	15	20	25	μsec

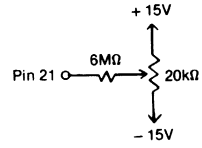
OPTIONAL OFFSET AND GAIN ADJUSTMENTS—MN7145 Series devices will operate as specified without additional adjustments. If desired, however, system absolute accuracy error can be improved by following the trimming procedure below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment should be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 21 should be left open. Do not ground. If gain and offset adjusting is performed on MN7145 Series devices, reference voltages may be applied to any of the analog input channels. It is recommended that offset and gain adjustments be made while the system is performing continuous or at least repeated conversions.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown below and apply an analog input voltage equivalent to + ½ LSB (MN7145) or – FS + ½ LSB (MN7146/7147). See Digital Output Coding section for the appropriate analog input voltages. While the device is performing repeated conversions, monitor the output and adjust the offset potentiometer "down" until all output bits are "0". Then adjust "up" until the LSB "flickers" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the analog input voltage equivalent to + FS – 1½ LSB. See Digital Output Coding section for the appropriate analog input voltages. While the device is performing repeated conversions, monitor the output and adjust the gain potentiometer "up" until all output bits are "1". Then adjust "down" until the LSB "flickers" on and off.



OFFSET ADJUST

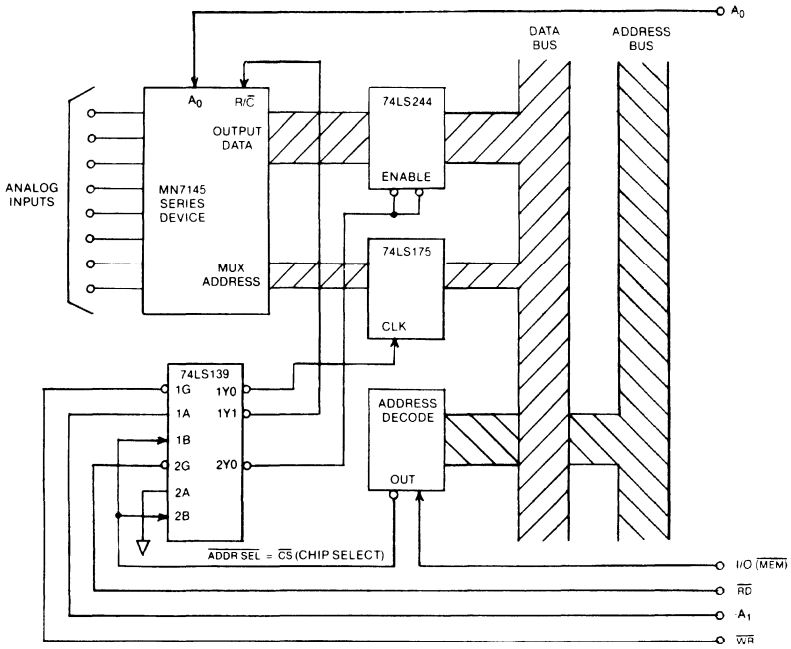


GAIN ADJUST

DIGITAL OUTPUTS—MN7145 Series devices have 8 digital output lines (pins 1, 2, 23-28) on which a 12-bit data word can be read in two 8-bit bytes. In the read mode, the state of A_0 determines if the MSB byte (A_0 = "0") or the LSB byte (A_0 = "1") is multiplexed to the digital output lines. Break-before-make action guarantees that the MSB and LSB bytes will not be enabled at the same time. Digital output data can only be read between conversions because output data lines are returned to the high impedance state whenever a conversion is in progress. See Pin Designations for data bit (DB0-DB11) assignments.

MICROPROCESSOR INTERFACE—The MN7145 Series DAS can be interfaced with most popular microprocessors. The DAS may be addressed either as a memory location (memory mapped) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM to which READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O ENABLE can be substituted for MEMORY ENABLE or $\overline{I/OR}$ and $\overline{I/OW}$ substituted for $\overline{MEMR}$ and $\overline{MEMW}$. The accompanying diagram shows a typical scheme to implement this interface.

STS is not used in this example; the μP must read data 30μsec after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).



DIGITAL OUTPUT CODING

Analog Input Voltage (Volts)			Digital Output
MN7145	**MN7146**	**MN7147**	
0 to +10V	±5V	±10V	MSB LSB
+10.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+4.9963	+9.9927	1111 1111 111Ø*
+5.0012	+0.0012	+0.0024	1000 0000 000Ø*
+4.9988	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+4.9963	−0.0037	−0.0073	0111 1111 111Ø*
+0.0012	−4.9988	−9.9976	0000 0000 000Ø*
0.0000	−5.0000	−10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input range, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN7147 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition will occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

MN7150-8
MN7150-16

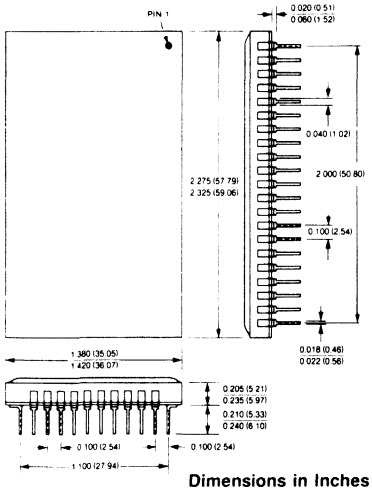
MICRO NETWORKS

8 and 16-CHANNEL
DIP-PACKAGED, 12-Bit
DATA ACQUISITION SYSTEMS

FEATURES

- **Complete DAS:**
  Multiplexer
  Address Counter
  Instrumentation Amp
  Track-Hold Amp
  12-Bit A/D Converter
  3-State Output Buffer
  Timing and Control Logic
- **8 Differential or 16 Single-ended Input Channels**
- **Instrumentation Amplifier Gains from 1 to 1000**
- **Random or Sequential Addressing**
- **50,000 Channels/sec Guaranteed Throughput**
- **Small 62-Pin Package**
- **Full Mil Operation**
  −55°C to +125°C
  MIL-H-38534 Optional

62 PIN PACKAGE



Dimensions in Inches (millimeters)

DESCRIPTION

MN7150-8 and MN7150-16 are complete, single-package, 12-bit data acquisition systems. Built with contemporary hybrid construction techniques, each system contains: an overvoltage protected (±35V) input multiplexer; a multiplexer channel-address latch/counter; a high-impedance ($10^8\Omega$) instrumentation amplifier that can have its gain set from 1 to 1000; a high-speed (10μsec max acquisition time) track-hold amplifier with hold capacitor; a high-speed (10μsec max conversion time) 12-bit A/D converter with 3-state output buffer; a 10 Volt buffered reference; and all timing and control logic necessary to operate the system with a single strobe command. The MN7150-8 offers 8 differential input channels; while the MN7150-16 offers 16 single-ended input channels. Both devices guarantee minimum throughput rates of 50,000 channels/sec.

The gain of MN7150's internal instrumentation amplifier is set anywhere from 1 to 1000 with a single external resistor making the full scale input range of the system variable from ±10V to ±10mV. This resistor, ±15V and +5V supplies with bypass caps, and user-optional gain and offset adjust potentiometers are all that is required to configure a fully functional, 12-bit, 50kHz data acquisition system.

MN7150 offers outstanding flexibility. The 12 bits of digital output data can be accessed in any combination of 3 four-bit bytes and a 4-bit mux-address register permits input-channel addresses to be read back if desired. Track-hold acquisition time and droop rate can be varied by adding an external resistor or capacitor. Expansion to 32 single-ended or 16 differential input channels is accomplished with 2 additional IC's.

MN7150 is packaged in a unique, 62-pin, hermetically sealed, ceramic package that occupies approximately 3.2 sq. in.. Devices are fully specified for 0°C to +70°C, −25°C to +85°C (MN7150E), or −55°C to +125°C (MN7150H) operation, and for military/aerospace applications, 100% screening to MIL-H-38534 is optional.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

January 1992
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MN7150 8 and 16-CHANNEL DIP-PACKAGED, 12-Bit DATA ACQUISITION SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7150	0°C to +70°C
MN7150E	−25°C to +85°C
MN7150H, MN7150H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 43)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 44)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pin 18)	−0.5 to +7 Volts
Analog Inputs (Pins 1-4, 51-62, Note 1)	±35 Volts
Digital Inputs	0 to +7 Volts

ORDERING INFORMATION

PART NUMBER — MN7150-16H/B CH

- Select MN7150-8 or MN7150-16 model
  - Standard Part is specified for 0°C to +70°C operation.
- Add "E" suffix for specified −25°C to +85°C operation.
- Add "H" suffix for specified −55°C to +125°C operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages = ±15V and +5V unless otherwise specified)

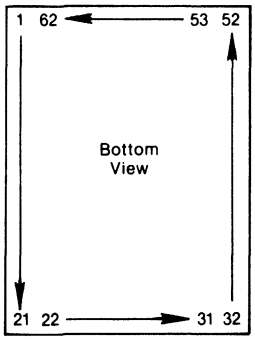
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels: MN7150-8		8 Differential		
MN7150-16		16 Single-Ended		
Input Voltage Ranges (Note 2): Unipolar		0 to +10		Volts
Bipolar		−10 to +10		Volts
Common Mode Voltage Range	±10			Volts
CMRR: G = 1 (10kHz)		72		dB
G = 1000 (60Hz)		100		dB
Input Resistance		100		MΩ
Input Capacitance: Off Channels		10		pF
On Channel: MN7150-8		50		pF
MN7150-16		100		pF
Input Bias Current: Initial (+25°C)		±100	±200	pA
Drift (Note 3)		Doubles Every 10°C		
Input Offset Current: Initial (+25°C)		±25	±50	pA
Drift (Note 3)		Doubles Every 10°C		
Input Offset Voltage (Note 4): Initial (+25°C)		±7	±12	mV
Drift (Note 3)		20+10G		μV/°C
Voltage Noise (RTI, Note 5): G = 1		150		μV(RMS)
G = 1000		1.6		μV(RMS)
DIGITAL INPUTS				
Logic Levels: Mux Enable (Pin 5): Logic "1"	+4			Volts
Logic "0"			+0.8	Volts
Other Inputs (Note 6): Logic "1"	+2			Volts
Logic "0"			+0.8	Volts
Loading: Mux Enable (Pin 5, Note 19)		1kΩ Pullup to +5V		
Load Input (Pin 19, Note 14)		2		LS TTL Loads
Other Inputs (Pins 8, 13-16, 20, 21, 26, 31; Note 14)		1		LS TTL Load
TRANSFER CHARACTERISTICS (Notes 7, 8)				
Integral Linearity Error: Initial (+25°C)		±¼	±½	LSB
Max Over Temperature (Note 3)		±½	±1	LSB
Differential Linearity Error: Initial (+25°C)		±½		LSB
Drift (Note 3)		±2		ppm of FSR/°C
12-Bit No Missing Codes		Guaranteed Over Temperature		
Unipolar Offset Error (Notes 9, 10): Initial (+25°C)		±0.05	±0.1	%FSR
Drift (Note 3)		±15	±20	ppm of FSR/°C
Bipolar Zero Error (Notes 9, 11): Initial (+25°C)		±0.05	±0.1	%FSR
Drift (Note 3)		±25	±35	ppm of FSR/°C
Gain Error (Notes 9, 12): Initial (+25°C)		±0.1	±0.2	%
Drift (Note 3)		±10	±30	ppm/°C
DIGITAL OUTPUTS (Note 13)				
Logic Levels: Logic "1"	+2.4			Volts
Logic "0"			+0.4	Volts
Fanout (Note 14)		5		TTL Loads
Logic Coding (Note 15): Unipolar Ranges		SB		
Bipolar Ranges		OB		

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
T/H Acquisition Time (Note 16)		9	10	μsec
A/D Conversion Time		9	10	μsec
Throughput Rate (Continuous Convert Mode)	50	55		kHz
$\overline{\text{Strobe}}$ Command Pulse Width	40			nsec
T/H Aperture Jitter T/H Output Droop Rate		1 1		nsec μV/μsec
Feedthrough (@1kHz, Note 17)		± 0.005	± 0.01	%
Mux Crosstalk Attenuation (@1kHz)		74		dB
Setup Time Digital Inputs (Note 18) to Strobe Hold Time Digital Inputs (Note 18) from Strobe	50		 50	nsec nsec
POWER SUPPLIES				
Power Supply Range: ± 15V Supplies + 5V Supply	± 14.5 + 4.75	± 15 + 5	± 15.5 + 5.25	Volts Volts
Power Supply Rejection: + 15V Supply − 15V Supply + 5V Supply		± 0.003 ± 0.003 ± 0.001		%FSR/%Supply %FSR/% Supply %FSR/% Supply
Current Drains: + 15V Supply − 15V Supply + 5V Supply		42 − 42 125	60 − 55 135	mA mA mA
Power Consumption		1885	2400	mW

SPECIFICATION NOTES

1. The MN7150's input multiplexer can withstand continuous voltages up to 20 volts greater than either supply and instantaneous transients up to several hundred volts. In a power-off condition, analog input voltage should not exceed ± 20 volts.
2. The gain of the MN7150's internal instrumentation amplifier is set from 1 to 1000 with a single external resistor between pins 47 and 48. Listed input ranges (0 to + 10V, ± 10V) are for the MN7150's A/D converter. If amplifier gain is greater than 1, the system input range will equal 0 to + 10V or ± 10V divided by G.
3. Listed specification applies over specified temperature range as selected by part number suffix.
4. This specification applies only to the front end of the MN7150 and is defined as the voltage seen at the output of the T/H amplifier with the T/H in the track mode, with the mux inputs grounded and with the instrumentation amplifier G = 1.
5. Measured at the output of the T/H amplifier.
6. Includes Strobe (pin 8), Mux Address inputs (pins 13-16), Load (pin 19), Clear (pin 20), and Enables (pins 21, 26, 31).
7. Transfer specifications refer to the entire system from mux input to A/D converter output with instrumentation amplifier G = 1.
8. FSR = Full Scale Range. In the unipolar mode, FSR = 10 volts. In the bipolar mode, FSR = 20 volts. For a 12-bit system, 1 LSB = 0.024%FSR.
9. Initial offset and gain errors are adjustable to zero with optional external potentiometers.
10. Unipolar Offset error is defined as the difference between the actual and the ideal input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition occurs when operating on a unipolar input range.
11. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs when operating on a bipolar input range.
12. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
13. Includes Parallel Data, Mux Address and Status (E.O.C.) outputs.
14. One LS TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.4mA with a logic "0" applied. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
15. SB = Straight Binary. OB = Offset Binary. See Output Coding table for details.
16. Includes mux switching and settling time, instrumentation amp settling time and T/H amp acquisition time. Specified for a 20V step settling to ± 0.01% FSR.
17. Measured at the output of the T/H with the T/H in the hold mode.
18. Includes Mux Address, Mux Enable, Clear and Load inputs.
19. The MN7150's Mux Enable input (pin 5) goes directly to the enable input of a 506A type CMOS multiplexer and has a 1kΩ pullup resistor to + 5V. The enable input of the multiplexer itself draws ± 10μA max.

PIN DESIGNATIONS

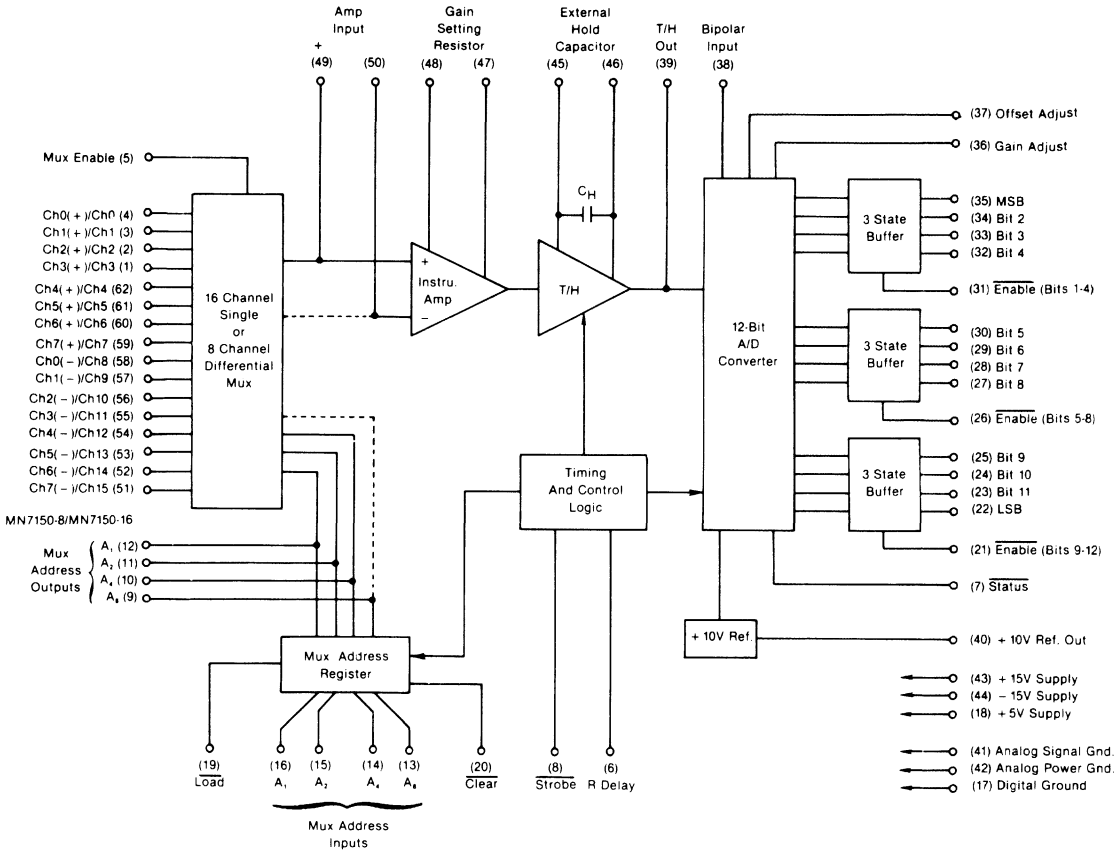


Dot on top of package references pin 1

1	Ch3(+)/Ch3	22	Bit 12 (LSB)	43	+ 15V Supply
2	Ch2(+)/Ch2	23	Bit 11	44	− 15V Supply
3	Ch1(+)/Ch1	24	Bit 10	45	External Hold Cap
4	Ch0(+)/Ch0	25	$\overline{\text{Bit 9}}$	46	External Hold Cap
5	Mux Enable	26	$\overline{\text{Enable}}$ (Bits 5-8)	47	Gain Setting Resistor
6	R Delay	27	Bit 8	48	Gain Setting Resistor
7	$\overline{\text{Status}}$ (E.O.C.)	28	Bit 7	49	Instru. Amp (+) Input
8	$\overline{\text{Strobe}}$	29	Bit 6	50	Instru. Amp (−) Input
9	A_8	30	$\overline{\text{Bit 5}}$	51	Ch7 (−)/Ch15
10	A_4 Mux Address	31	$\overline{\text{Enable}}$ (Bits 1-4)	52	Ch6 (−)/Ch14
11	A_2 Outputs	32	Bit 4	53	Ch5 (−)/Ch13
12	A_1	33	Bit 3	54	Ch4 (−)/Ch12
13	A_8	34	Bit 2	55	Ch3 (−)/Ch11
14	A_4 Mux Address	35	Bit 1 (MSB)	56	Ch2 (−)/Ch10
15	A_2 Inputs	36	Gain Adjust	57	Ch1 (−)/Ch9
16	A_1	37	Offset Adjust	58	Ch0 (−)/Ch8
17	Digital Ground	38	Bipolar Input	59	Ch7 (+)/Ch7
18	+ 5V Supply	39	Track-Hold Output	60	Ch6 (+)/Ch6
19	$\underline{\text{Load}}$	40	+ 10V Reference Out	61	Ch5 (+)/Ch5
20	$\overline{\text{Clear}}$	41	Analog Signal Ground	62	Ch4 (+)/Ch4
21	$\overline{\text{Enable}}$ (Bits 9-12)	42	Analog Power Ground		

Pins 1-4 and 51-62 are defined for MN7150-8/MN7150-16.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

SUMMARY OF OPERATION—The falling edge of a Strobe pulse loads the multiplexer (mux) channel address and initiates a signal-acquisition and data-conversion cycle. If sequential addressing is being used, the next channel will be accessed. If random addressing is being used, the channel whose address has been applied to the Mux Address Inputs will be accessed. The falling edge of Strobe simultaneously fires an internal one-shot (10μsec pulse duration) whose output controls the operational mode of the track-hold amplifier (T/H). The T/H is driven into the signal-acquisition (tracking) mode for 10μsec during which the mux and instrumentation amplifier settle and the T/H acquires the new signal. After 10μsec, the falling edge of the one-shot drives the track-hold amp into the hold mode, gates on the internal clock, generates a start-convert signal for the 12-bit A/D converter, and drives the Status Output to a logic "1". Gating off the clock during the time the mux is settling into its new channel and the T/H is acquiring a new signal reduces noise errors. When the conversion is complete (a maximum 10μsec later), the Status output returns to a logic "0" indicating that the conversion is complete, that the digital output is valid, and that the T/H amplifier has returned to the tracking mode. The unit is now ready to be triggered for the acquisition and conversion of the next channel.

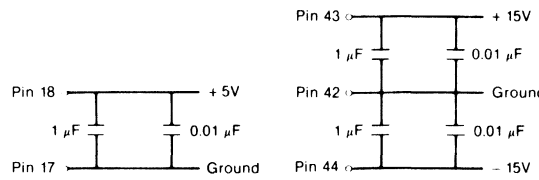
LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN7150-8 and MN7150-16. Units are designed with separate pins for Analog Power Ground (pin 42), Digital Ground (pin 17) and Analog Signal Ground (pin 41), and if your system distinguishes these grounds, the MN7150's pins should be connected respectively. If not, the MN7150's three ground pins should be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large analog ground plane beneath the package.

For the MN7150-16, the inverting input to the internal instrumentation amplifier (pin 50) is not connected to the internal multiplexer and this pin should be connected along with pin 41 (Analog Signal Ground) to the signal-source reference point.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Pins 36 (Gain Adjust), 37 (Offset Adjust) and 38 (Bipolar Input) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing these inputs. If optional gain and offset adjusting is used, care should be taken to locate potentiometers and series resistors as close to the MN7150 as possible.

The output of the MN7150's T/H amp is internally connected directly to the input of the A/D converter. When operating in a unipolar (0 to + 10V) mode, however, pin 39 (T/H Output) must be connected to pin 38 (Bipolar Input) for proper operation. For bipolar (± 10V) operation, pin 40 (+ 10V Ref. Out) must be connected to pin 38 (Bipolar Input) and pin 39 left open.

MN7150 has internal 0.01μF bypass capacitors on each supply line. It is recommended that power supplies be additionally decoupled with tantalum and ceramic capacitors located as close to the device as possible. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams.



POWER SUPPLY DECOUPLING

DIGITAL PIN FUNCTIONS

Pin Designation	Function
Mux Enable (Pin 5)	"0" disables internal mux. "1" enables internal mux. Use to disable internal mux when addressing additional external multiplexers.
$\overline{\text{Status}}$ (E.O.C.) (Pin 7)	End of conversion. "0" = signal acquisition cycle in progress. "1" = A/D conversion cycle in progress. 1→0 indicates conversion complete. See Timing Diagrams.
$\overline{\text{Strobe}}$ (Pin 8)	"1"→"0" falling edge updates (increments) mux channel and initiates signal acquisition and A/D conversion cycles.
Mux Address Out (pins 9-12)	Output of mux address register. Shows channel currently on. Straight binary coding. See section describing Channel Address Modes.
Mux Address In (Pins 13-16)	Selects mux channel in random address mode. Straight binary coding. See section describing Channel Address Modes.
$\overline{\text{Load}}$ (Pin 19)	"0" = random address mode. "1" = sequential address mode.
$\overline{\text{Clear}}$ (Pin 20)	A logic "0" applied to this pin forces mux address to Ch0 on next falling edge of strobe regardless of Load and Mux Address Inputs. Tie to logic "1" when not in use.
$\overline{\text{Enable}}$ (Bits 9-12) (Pin 21)	"0" enables three-state buffer for A/D converter bits 9-12 (LSB). "1" disables buffer.
$\overline{\text{Enable}}$ (Bits 5-8) (Pin 26)	"0" enables three-state buffer for A/D converter bits 5-8. "1" disables buffer.
$\overline{\text{Enable}}$ (Bits 1-4) (Pin 31)	"0" enables three-state buffer for A/D converter bits 1(MSB)-4. "1" disables buffer.

ANALOG PIN FUNCTIONS

Pin Designation	Function
R Delay (Pin 6)	Connect external resistor to lengthen T/H acquisition time when instrumentation amp is set for high gain. R = (Acq. Time) 10^9 – 9kΩ. For normal operation pin 6 must be connected to + 5V.
Gain Adjust (Pin 36)	Connect user-optional, external, 20kΩ, gain-adjust potentiometer here.
Offset Adjust (Pin 37)	Connect user-optional, external, 20kΩ, offset-adjust potentiometer here.
Bipolar Input (Pin 38)	Connect to T/H Output (pin 39) for unipolar (0 to + 10V) operation. Connect to + 10V Ref. Out (pin 40) for bipolar (± 10V) operation.
T/H Output (Pin 39)	Connect T/H Output to Bipolar Input (pin 38) for unipolar operation. Leave open for bipolar operation.
+ 10V Ref. Out (Pin 40)	Connect to Bipolar Input (pin 38) for bipolar (± 10V) operation. Open for unipolar (0 to + 10V) operation. Accuracy = ± 0.05% typical. Drift = ± 10ppm/°C typical. Buffer if used to drive external load.
External Hold Capacitor (Pins 45-46)	Add external polypropylene or teflon hold capacitor to improve T/H droop rate.
Gain Setting Resistor (Pins 47-48)	Select gain resistor with formula R = 20k/(G – 1). Leave open for G = 1.
Instrumentation Amp Inputs (Pins 49-50)	Use when adding additional external multiplexers for expanded single-ended or differential operation. Connect pin 50 to Analog Signal Common for MN7150-16.

$\overline{\text{STATUS}}$ OUTPUT (E.O.C.)—The status or End of Conversion (E.O.C.) output (pin 7) indicates whether the MN7150 is tracking or converting an input signal. When Status is a logic "0", the MN7150's internal T/H amplifier is in the tracking mode and digital output data from the previous conversion is still valid. When the Status is a logic "1", the T/H is in the hold mode, the internal A/D is converting, and the output data is not valid. The falling edge of Status indicates that the conversion is complete, that the output data is valid, and that the T/H has returned to the tracking mode.

CHANNEL ADDRESS MODES

The MN7150-8 and MN7150-16 may have their input multiplexer channels either randomly or sequentially addressed. For random addressing, pin 19 (Load) must have a logic "0" applied. For sequential addressing, pin 19 must have a logic "1" applied.

Address Mode	Mux Enable	$\overline{\text{Load}}$	$\overline{\text{Clear}}$	Address Inputs	Address Outputs	$\overline{\text{Strobe}}$
Random	1	0	1	Next Channel	On Channel	1→0
Sequential	1	1	1	Don't Care	On Channel	1→0
Free Running Sequential (Note 2)	1	1	1	Don't Care	On Channel (Note 1)	1→0

NOTES

1. In the free running sequential address mode, the channel address output lines indicate the channel currently being sampled (Ch_n) while digital output data is valid for the previously sampled channel. ($Ch_n - 1$).

2. The free running sequential mode is implemented by tying the Status output (pin 7) to the Strobe input (pin 8). At the end of each conversion, the falling edge of Status increments the address counter and initiates the next acquisition/conversion cycle.

RANDOM ADDRESSING—For random channel addressing, the Load pin (pin 19) must be tied to logic "0"; the Clear pin (pin 20) tied to logic "1" (or left open); and the desired channel address (in 8421 binary) applied to the Mux Channel Address Inputs (pins 13-16, pin 16 = A_1, pin 15 = A_2, pin 14 = A_4, pin 13 = A_8). In this address mode, the MN7150's internal address latch/counter acts as a 4-bit parallel register. The falling edge of the Strobe pulse latches the new channel address and initiates the data acquisition and conversion cycle. For the MN7150-8 (8-channel differential input), address line A_8 is not required and pin 13 is a "don't care".

When Clear (pin 20) has a "0" applied, the next falling edge of the Strobe command will drive the mux to channel 0 (address 0000) regardless of the data on the address input lines and regardless of the signal applied to the Load line.

Because the Strobe line activates the control logic and does not drive the address latch directly, channel-address input data must be valid 50nsec both before and after the falling edge of the Strobe pulse.

SEQUENTIAL ADDRESSING—For sequential channel addressing, the Load pin (pin 19) and the Clear pin (pin 20) must both be tied to logic "1". In this mode, the internal address latch/counter acts as a 4-bit counter, and the falling edge of the Strobe pulse increments the channel address and initiates the data acquisition and conversion cycle. Channel 0 will be accessed after channel 7 (MN7150-8) or channel 15 (MN7150-16). If one changes from random to sequential addressing, the next channel accessed will be one higher than the channel last randomly addressed. Changing digital data appearing at the address inputs will not affect the MN7150 when it is in the sequential address mode.

SEQUENTIAL ADDRESSING CONTINUOUS CONVERSIONS—The MN7150 can be made to continuously sequence through channels acquiring and converting data by applying logic "1's" to the Load and Clear pins (pins 19 and 20) and tying the Status (E.O.C.) output (pin 7) back to the Strobe input (pin 8). In this mode, Status going low at the end of a conversion becomes the falling edge of Strobe that addresses the next channel and initiates the next data acquisition and conversion cycle. After each channel has been converted and the Status has dropped to a "0", the output data will be valid for approximately the next 10μsec while the multiplexer is switching channels and the T/H is acquiring the new signal. When continuously converting in this manner, an external Strobe signal should be provided at power-on to avoid possible latch-up.

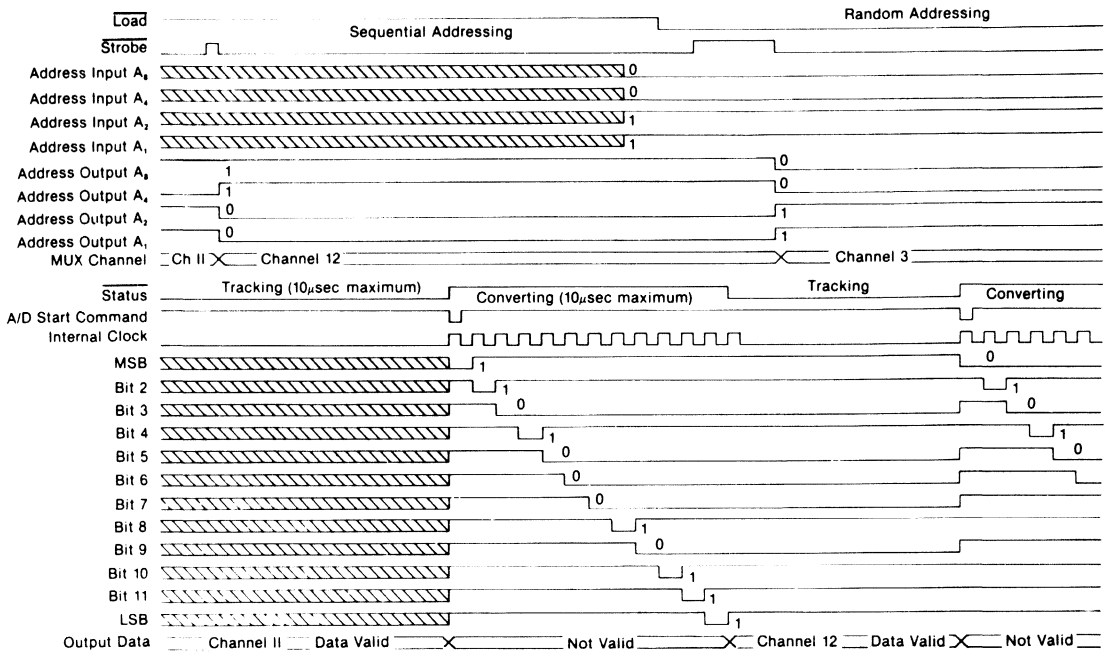
Address Inputs				Mux Enable	Channel Selected	
A_8	A_4	A_2	A_1			
X	X	X	X	0	None	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	
0	1	1	1	1	7	MN7150-8
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	
1	1	1	1	1	15	MN7150-16

NOTES

1. For the MN7150-8, Mux Address Input Line A_8 (pin 13) is a "don't care". Pin 13 is connected to the MN7150-8's address latch/counter, however, the A_8 output of the latch/counter is not connected to the MN7150-8's internal mux.

CHANNEL ADDRESS OUTPUTS—The MN7150's Channel Address Outputs (pins 9-12) are tied directly to the unit's internal address counter/latch. They indicate, in 8421 binary, the multiplexer channel presently being accessed. When using external multiplexers for expanded differential or single-ended operation, these outputs can be used to address the external multiplexers, eliminating the need for any additional address decoding circuitry. When using sequential addressing, the appropriate Channel Address Outputs can be NORed together to generate a frame sync pulse each time channel 7 (8 channel systems) or channel 15 (16 channel systems) is being addressed. In microprocessor-based systems, the Address Outputs can be 3-state buffered to add channel read-back capability.

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. MN7150's internal clock and A/D start-convert command signals are not pinned out externally. They are included here to help the user understand MN7150 operation.
2. The data acquisition/conversion cycle is initiated by the falling edge of strobe. The strobe has a minimum positive or negative pulse width of 40nsec. In other words, strobe must be positive a minimum of 40nsec prior to its falling edge and negative a minimum of 40nsec after its falling edge.
3. Strobe may be brought high after an acquisition/conversion cycle has begun with a new cycle not beginning until the next falling edge.
4. Mux Address, Load and Clear inputs must be valid 50nsec before and after the falling edge of strobe.
5. Mux Address Outputs become valid typically 40nsec after the falling edge of strobe.
6. The internal clock is gated off during the 10μsec signal acquisition period to reduce noise.
7. When Status = "1", the internal T/H is in the hold mode, and the A/D converter is performing a conversion. When Status = "0", the conversion is complete; output data is valid; and the T/H has returned to the track mode. Data will remain valid until Status goes high again.
8. When the Status goes high indicating that an A/D conversion has begun, the MSB goes to a "0" and all other output bits go to a "1". Output bits are set to their final state on succeeding rising clock edges.
9. When enabling 3-state output buffers to access digital data, data becomes valid no longer than 50nsec after an enable line is brought low.

DIGITAL OUTPUT CODING

Analog Input Voltage (Volts)					
Unipolar Ranges		Bipolar Ranges		Digital Output	
General	0 to +10V	General	±10V	MSB	LSB
FS	+10.0000	+FS	+10.0000	1111 1111 1111	
FS – 1½LSB	+9.9963	+FS – 1½LSB	+9.9927	1111 1111 111Ø*	
½FS + ½LSB	+5.0012	0 + ½LSB	+0.0024	1000 0000 000Ø*	
½FS – ½LSB	+4.9988	0 – ½LSB	–0.0024	ØØØØ ØØØØ ØØØØ*	
½FS – 1½LSB	+4.9963	0 – 1½LSB	–0.0073	0111 1111 111Ø*	
0 + ½LSB	+0.0012	–FS + ½LSB	–9.9976	0000 0000 000Ø*	
0	0.0000	–FS	–10.0000	0000 0000 0000	

NOTES

1. FSR stands for full scale range and is equivalent to the nominal peak-to-peak voltage of the selected input voltage range.
2. 1LSB for a 12-bit system is equivalent to FSR/4096. Therefore, for a 20V FSR, 1LSB = 4.88mV; for a 10V FSR, 1LSB = 2.44mV, etc.
3. For unipolar input ranges, output coding is straight binary. For bipolar input ranges, output coding is offset binary.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

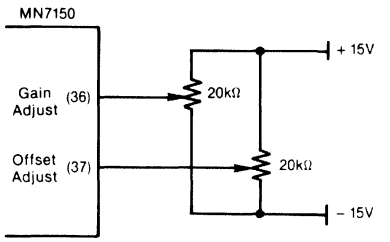
EXAMPLE: For an MN7150 operating on its ± 10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of – 9.9976 volts. Subsequently, any input voltage more negative than – 9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of – 0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at + 9.9927 volts. An input more positive than + 9.9927 volts will give all "1's".

OPTIONAL OFFSET AND GAIN ADJUSTMENTS—The MN7150 will operate as specified without additional adjustments. If desired, however, system absolute accuracy error can be reduced to ±1LSB by following the trimming procedure described below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment must be made before the gain adjustment. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, Pins 36 and 37 should be left open. Do not ground. If gain and offset adjusting is being performed on the MN7150-16, reference voltages may be applied to any channel. If gain and offset adjusting is being performed on the MN7150-8, reference voltages should be applied to the (+) input of a given channel with the (−) input tied to analog ground.

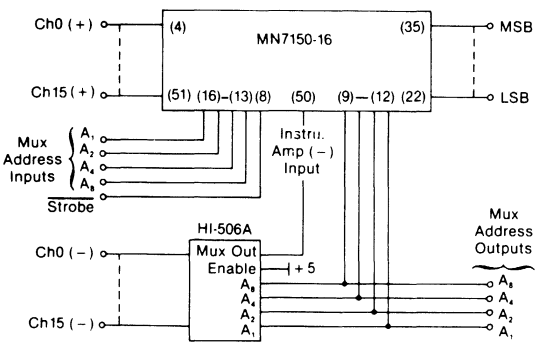
It is recommended that gain and offset adjusting be accomplished while the system is performing continuous or at least repeated conversions. If random addressing is used, the mux will have to be held on one channel during the process. If the continuous-converting sequential-address mode is used (Status output tied to Strobe input), the Clear line will have to be held low to keep the input multiplexer on channel 0. Alternatively, the voltages may be applied to all channels simultaneously.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown and apply an analog input voltage equivalent to + ½LSB if operating in a unipolar mode or −½ LSB if operating in a bipolar mode. Have the MN7150 performing repeated conversions, either by being in the continuous converting mode or by being under external control. For the unipolar mode, adjust the offset potentiometer "down" until all the output bits are "0". Then adjust "up" until the LSB just turns to a "1". For bipolar mode, adjust the potentiometer "down" until the bits are MSB 0111 1111 1111 LSB. Then adjust it "up" until the bits just turn to MSB 1000 0000 0000 LSB.

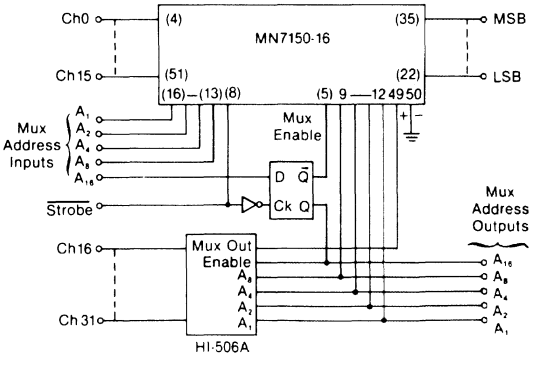
GAIN ADJUSTMENT—Connect the gain potentiometer as shown and apply an analog input voltage equivalent to +FS−1½ LSB. With MN7150 performing repeated conversions, adjust the gain potentiometer "up" until all the output bits are "1". Then adjust "down" until the LSB just turns to a "0".



MULTIPLEXER EXPANSION—The MN7150-16's input capabilities are easily expanded beyond 16 channels with the addition of external analog multiplexers. The diagrams below show the implementation of 32-channel single-ended and 16-channel differential systems. For further single-ended expansion, additional mux's can be tied to pin 49 (the noninverting input to the internal instrumentation amplifier) or cascaded in front of the MN7150's internal mux. Remember that for single-ended operation, pin 50 (the inverting input to the internal instrumentation amplifier) has to be grounded. For further differential expansion, additional multiplexers will have to be tied to both the inverting (pin 50) and noninverting (pin 49) inputs of the internal instrumentation amplifier.



Expansion to 16 Differential Channels



Expansion to 32 Single-ended Channels

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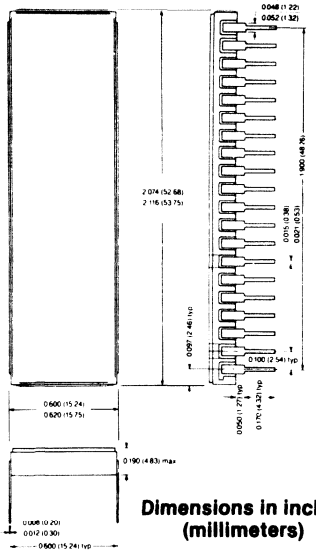
MICRO NETWORKS

MN7208
MN7216

DATA ACQUISITION SYSTEM
FRONT-END

FEATURES

- **Complete DAS Front End:**
  Analog Input Multiplexer
  Instrumentation Amplifier
  Load/Sequence Control Logic
- **Small 40-Pin DIP**
- **16-Single-Ended or 8-Differential Input Channels**
- **10μsec Channel Switching and In-Amp Settling Time**
- **Full Mil Operation −55°C to +125°C**
- **Use with MN6000 Series Sampling A/D Converters for Multi-Channel Digitizing**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**



Dimensions in inches (millimeters)

DESCRIPTION

The MN7208 and MN7216 are thin-film hybrid circuits containing two 8-channel multiplexers, random and sequential address control logic and a precision instrumentation amplifier. This DAS front-end function is packaged in a 40-pin side-brazed DIP and can be used with Micro Networks MN6000 Series of sampling A/D converters to configure a complete, 16-channel single-ended or an 8-channel full differential data acquisition system in as few as 2 dual in-line packages. Extremely versatile, the MN7208/7216 can be used in a wide variety of multi-channel data acquisition applications.

The multiplexer section of the MN7208 and MN7216 features over voltage protected analog inputs and break-before-make channel switching. The internal control logic allows both random and sequential channel addressing. The precision instrumentation amplifier's fast settling time and internal gain setting resistors combine to offer high-speed and precision gain accuracy and low drift.

Channel access and settling time for both the MN7208 and MN7216 to ±0.01% for a 20V step is 10μsec maximum. These devices, when used with the MN6774 12-Bit, 100kHz sampling A/D converter, can be configured into a μP-interfaced 12-Bit, 50kHz data acquisition system (multi-channel A/D) complete with multiplexer, instrumentation amplifier, T/H amplifier, A/D converter and all interface and address decode logic.

The MN7208 and MN7216 have been designed to offer the user maximum flexibility when designing for multi-channel data conversion applications where small size and physical/electrical compatibility are paramount considerations. Standard devices are specified fully for 0°C to +70°C (J and K models) or −55°C to +125°C (S and T models) operation. For military/aerospace or harsh-environment industrial applications, "S" and "T" models are available with environmental stress screening. Contact factory for availability of fully compliant MIL-H-38534 devices.

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October 1990
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MN7208/MN7216 DATA ACQUISITION SYSTEM FRONT-END

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7208J, K; MN7216J, K	0°C to +70°C
MN7208S, S/B, T, T/B	−55°C to +125°C
MN7216S, S/B, T, T/B	−55°C to +125°C
Positive Supply ($+V_{CC}$, Pin 28)	0 to +18 Volts
Negative Supply ($-V_{CC}$ Pin 24)	0 to −18 Volts
Logic Supply ($+V_{DD}$, Pin 34)	−0.5 to +7 Volts
Analog Inputs:	
CH_0 — CH_{15} (Pins 1-16)	$\pm V_{CC}$ ±20 Volts
−RG, G500, +Amp, −Amp, G10 (Pins 17-20, 23)	$\pm V_{CC}$
Digital Inputs:	
Address Inputs (Pins 37-40)	0 to +7 Volts
Load, Reset, Clock (Pins 27, 36, 35)	0 to +7 Volts
MUX Enable (Pin 25)	0 to +7 Volts

ORDERING INFORMATION

PART NUMBER **MN7208 T/B CH**

Select 8-channel differential (MN7208) or 16-channel single-ended (MN7216) model.
Select suffix J,K,S or T for desired performance and specified temperature range.
Add "/B" suffix to "S" or "T" models for Environmental Stress Screening.
Add "CH" suffix to "S/B" or "T/B" models for MIL-H-38534 compliant devices.
Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V unless otherwise noted)

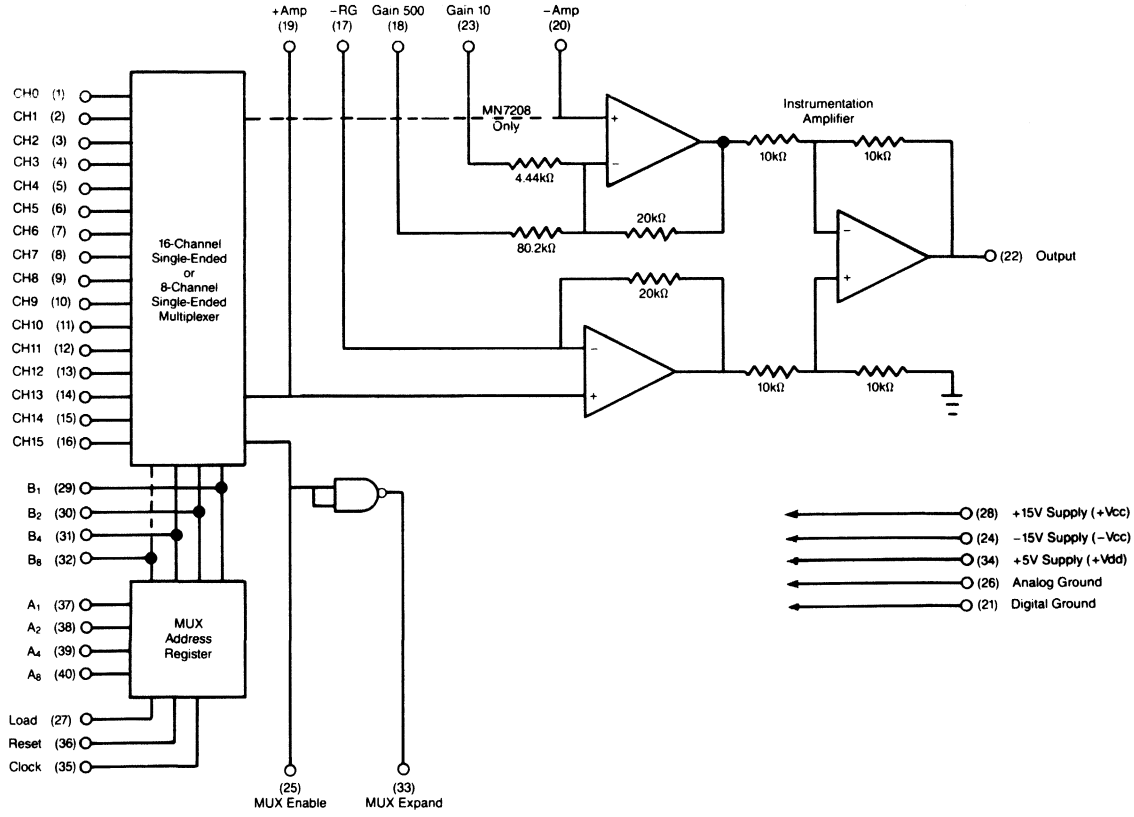
ANALOG INPUTS (Multiplexer Inputs)	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Voltage Range: Single-Ended (MN7216)		±10		Volts
Differential (MN7208)		±10		Volts
Common Mode	±10	±12		Volts
Input Impendance: Single-Ended (MN7216)		5//6		mΩ/pF
Differential (MN7208)		2//1		mΩ/pF
DIGITAL INPUTS (MUX Address, Load, Reset, Clock, MUX Enable)				
Logic Levels: MUX Enable (Note 2): Logic "1"	+4.0			Volts
Logic "0"			+0.8	Volts
MUX Address, Load, Reset, Clock: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: MUX Enable (Note 2): Logic "1" (V_{IH} = 4.0V)			−1	mA
Logic "0" (V_{IL} = 0.4V)			−4.6	mA
MUX Address, Load, Reset, Clock: Logic "1" (V_{IH} = 2.4V)			+20	μA
Logic "0" (V_{IL} = 0.4V)			−0.4	mA
ANALOG OUTPUT (Instrumentation Amplifier)				
Output Voltage	±10	±12		Volts
Output Current	±5	±25		mA
Capacitive Load (Stability)		5000		pF
DYNAMIC CHARACTERISTICS				
Large Signal Bandwidth		270		kHz
Output Slew Rate		17		V/μsec
Settling Time (20V Step to ±0.01%, G=1)		7	10	μsec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15 Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Current Drains: +15V Supply		+4	+7	mA
−15V Supply		−3	−6	mA
+5V Supply		+28	+35	mA
Power Consumption		245	370	mW

TRANSFER CHARACTERISTICS	J	K	S	T	UNITS
Offset Error (Max): Initial G=1	±5	±5	±5	±5	mV
(RTI) G=10	±0.5	±0.5	±0.5	±0.5	mV
G=500	±200	±200	±200	±200	μV
Over Temperature (Note 3): G=1	±10	±5	±10	±5	mV
G=10	±1	±0.5	±1	±0.5	mV
G=500	±400	±200	±400	±200	μV
Offset Drift (Max): G=1	±100	±50	±100	±50	μV/°C
(RTI) G=10	±70	±35	±70	±35	μV/°C
G=500	±10	±5	±10	±5	μV/°C
Gain Error (Max, Note 5) Initial: G=1	±0.04	±0.04	±0.04	±0.04	%
G=10	±0.05	±0.05	±0.05	±0.05	%
G=500	±0.05	±0.05	±0.05	±0.05	%
Over Temperature (Note 3): G=1	±0.08	±0.04	±0.08	±0.04	%
G=10	±0.10	±0.05	±0.10	±0.05	%
G=500	±0.10	±0.05	±0.10	±0.05	%
Gain Drift (Max): G=1	±20	±10	±20	±10	ppm/°C
G=10	±20	±10	±20	±10	ppm/°C
G=500	±20	±10	±20	±10	ppm/°C
Gain Nonlinearity (Max, Note 4) (G=1): Initial	±0.005	±0.003	±0.005	±0.003	%FSR
Over Temperature (Note 3)	±0.01	±0.006	±0.01	±0.006	%FSR

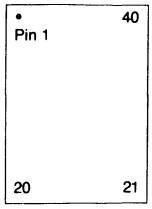
NOTES:

1. System specifications listed reflect the performance of both the multiplexer and instrumentation amplifier serially connected.
2. Internal 1K resistor connected to +5V for operation with standard TTL logic.
3. J and K models specified for 0°C to +70°C operation. S and T models specified for −55°C to +125°C operation.
4. Gain linearity error is defined as the maximum deviation from the best-fit straight line approximation to the system's input-output transfer function and is expressed as a percentage of the system's full scale voltage swing (FSR).
5. Gain error is defined as the error in the slope of the system's input-output transfer function and is expressed in percent.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Channel 0	40	Address Input A_1
2	Channel 1	39	Address Input A_2
3	Channel 2	38	Address Input A_4
4	Channel 3	37	Address Input A_8
5	Channel 4	36	Reset
6	Channel 5	35	Clock
7	Channel 6	34	+5V Supply (+Vdd)
8	Channel 7	33	MUX Expand
9	Channel 8	32	Address Output B_8
10	Channel 9	31	Address Output B_4
11	Channel 10	30	Address Output B_2
12	Channel 11	29	Address Output B_1
13	Channel 12	28	+15V Supply (+Vcc)
14	Channel 13	27	Load
15	Channel 14	26	Analog Ground
16	Channel 15	25	MUX Enable
17	-RG	24	-15V Supply (-Vcc)
18	Gain 500	23	Gain 10
19	+Amp	22	Output
20	-Amp	21	Digital Ground

APPLICATIONS INFORMATION

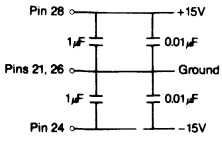
DESCRIPTION OF OPERATION — The MN7208 and MN7216 are data acquisition system building blocks. Each device contains an analog input multiplexer, address decode control logic circuitry and an instrumentation amplifier. The MN7208 provides an eight channel differential input multiplexer, while the MN7216 provides 16 single-ended inputs. Control logic circuitry enables either random or sequential channel addressing. Multiplexer outputs are connected internally to the instrumentation amplifier inputs. The instrumentation amplifier can be configured in gains of 1, 10 and 500 via the internal gain setting resistors or set to any user defined value with the use of external resistors.

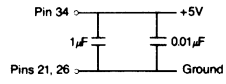
LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified performance from the MN7208/7216. The unit's analog and digital ground pins are not connected to each other internal to the device, therefore, they should be tied together outside the device package and connected to system analog ground through a large ground plane beneath the unit.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Care should be taken to avoid long runs or runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1uF tantalum capacitors in parallel with 0.01μF ceramic capacitors can be used if necessary to conserve board space.

POWER SUPPLY DECOUPLING





MULTIPLEXER AND CONTROL LOGIC — The Load (pin 27) input controls the random or sequential mode of operation. If Load Input (pin 27) is set to a logic 1, the device will access input channels sequentially with every rising edge of the Clock Input. If set to a logic 0, the device will access the channel selected via the Address Inputs (A1-A8, pins 37-40). In either mode of operation, the state of the Load Input is latched on the rising edge of the signal applied to Clock Input (pin 35).

Other control lines include Reset (pin 36) and MUX Enable (pin 25). As they imply, Reset can be used to initialize or reset the multiplexer to channel 0 and the MUX Enable input can be used in systems which require input channel expansion.

In addition to address inputs, address outputs are provided for use in identifying converted data. Applications requiring additional channel inputs can utilize the MUX Expand output for enabling additional multiplexers. These features can be better understood by referencing the Truth Tables for both the MN7208 and MN7216.

INSTRUMENTATION AMPLIFIER — The instrumentation amplifier can be configured for gains of 1, 10 and 500 utilizing internal gain setting resistors. Gains are selected via external pin connections (see section labeled Gain Selection). User definable gains can be set using external resistors.

GAIN SELECTION — Gain selection is accomplished via external pin connections. To operate the MN7208/7216 in a gain of 1, pin 17 should be left open. If a gain of 10 is desired, connect pin 17 to pin 23. If a gain of 500 is desired, connect pin 17 to pin 18. Care should be taken when laying out circuit runs to avoid introducing errors. Keep connections as short and direct as possible.

The gain may be set to values other than 1, 10 and 500 by using an external gain setting resistor. The equation for choosing the value of the external resistor is shown below.

$$RG=[40k/(G-1)]-50 \text{ Ohms}$$

INPUT - OUTPUT TRUTH TABLES

MN7216 — Truth Table

DIGITAL INPUTS								DIGITAL OUTPUTS					
Address Inputs							MUX	Address Outputs					
A_3	A_2	A_1	A_0	Load	Reset	Clock	Enable	B_3	B_2	B_1	B_0	Expand	Output
X	X	X	X	X	X	X	X	X	X	X	X	H	+Amp
X	X	X	X	X	L	↑	H	L	L	L	L	L	CH0
H	H	H	H	L	H	↑	H	H	H	H	H	L	CH15
L	H	H	H	L	H	↑	H	L	H	H	H	L	CH7
L	L	L	H	L	H	↑	H	L	L	L	H	L	CH1
L	L	L	L	L	H	↑	H	L	L	L	L	L	CH0
X	X	X	X	H	H	↑	H	L	L	L	H	L	CH1
X	X	X	X	H	H	↑	H	L	L	H	L	L	CH2
X	X	X	X	H	H	↑	H	L	L	H	H	L	CH3
X	X	X	X	H	H	↑	H	L	H	L	L	L	CH4
X	X	X	X	H	H	↑	H	L	H	L	H	L	CH5
X	X	X	X	H	H	↑	H	L	H	H	L	L	CH6
X	X	X	X	H	H	↑	H	L	H	H	H	L	CH7
X	X	X	X	H	H	↑	H	H	L	L	L	L	CH8
X	X	X	X	H	H	↑	H	H	L	L	H	L	CH9
X	X	X	X	H	H	↑	H	H	L	H	L	L	CH10
X	X	X	X	H	H	↑	H	H	L	H	H	L	CH11
X	X	X	X	H	H	↑	H	H	H	L	L	L	CH12
X	X	X	X	H	H	↑	H	H	H	L	H	L	CH13
X	X	X	X	H	H	↑	H	H	H	H	L	L	CH14
X	X	X	X	H	H	↑	H	H	H	H	H	L	CH15
X	X	X	X	H	H	↑	H	L	L	L	L	L	CH0

MN7208 — Truth Table

DIGITAL INPUTS							DIGITAL OUTPUTS				
Address Inputs						MUX	Address Outputs				
A_2	A_1	A_0	Load	Reset	Clock	Enable	B_2	B_1	B_0	Expand	Output
X	X	X	X	X	X	X	X	X	X	H	+Amp
X	X	X	X	L	↑	H	L	L	L	L	CH0
H	H	H	L	H	↑	H	H	H	H	L	CH7
L	H	H	L	H	↑	H	L	H	H	L	CH3
L	L	H	L	H	↑	H	L	L	H	L	CH1
L	L	L	L	H	↑	H	L	L	L	L	CH0
X	X	X	H	H	↑	H	L	L	H	L	CH1
X	X	X	H	H	↑	H	L	H	L	L	CH2
X	X	X	H	H	↑	H	L	H	H	L	CH3
X	X	X	H	H	↑	H	H	L	L	L	CH4
X	X	X	H	H	↑	H	H	L	H	L	CH5
X	X	X	H	H	↑	H	H	H	L	L	CH6
X	X	X	H	H	↑	H	H	H	H	L	CH7
X	X	X	H	H	↑	H	L	L	L	L	CH0
X	X	X	H	H	↑	H	L	L	H	L	CH1

NOTES:

1. "H" indicates TTL logic high (+2.0V minimum) for MUX Address, Load, Reset and Clock digital inputs. For MUX Enable, "H" indicates a logic high of +4.0V minimum.
2. "L" indicates TTL logic zero (+0.8V maximum) for all digital inputs.
3. "X" indicates "don't care."
4. "↑" indicates a "L" to "H" (low to high) transition.

TYPICAL PERFORMANCE SPECIFICATIONS

Typical MUX Performance Specifications	
Number of Channels: MN7208	8 Full Differential
MN7216	16 Single Ended
Input Voltage Range	±10V
Input Impendance	250mΩ/100pF
Logic Levels: Logic "1" (min)	+4.0V
Logic "0" (max)	+0.8V
Logic Currents: Logic "1"	±1μA
Logic "0"	±1μA
Access Time	500nsec
On Resistance	1.5kΩ
Cross Talk (1kΩ Source, 1KHz, 20Vp-p)	−68dB

Typical Instrumentation Amplifier Performance Specifications	
Voltage Range (min)	±10V
Input Impedance: Differential (MN7208)	$5\times10^{12}\Omega$//6pF
Single Ended (MN7216)	$2\times10^{12}\Omega$//1pF
Input Bias Current	20pA
Input Offset Current	2pA
Common Mode Rejection Ration (min): G=1	70dB
G=100	100dB
Gain Error (G=1): Initial (+25°C)	±0.04%
Over Temperature	±0.08%
Gain (G=1) Nonlinearity (max)	±0.01%
Large Signal Bandwidth	270kHz
Output Slew Rate	17V/μsec
Output Voltage Swing (min)	±10V
Output Current (min)	±5mA
Output Load Capacitance (Stability)	5000pF

CONFIGURING A DATA ACQUISITION SYSTEM

The MN7208/16 can be used with 12- and 16-bit sampling A/D converters to configure multi-channel data acquisition systems. The MN7208/16 provides a single-package solution for front-end signal conditioning/processing including multiplexing with control logic circuitry and an instrumentation amplifier (selectable fixed gains of 1, 10, 500 or user defined via external resistors). The Sampling A/D converter provides the T/H amplifier, necessary control logic circuitry, reference, clock, A/D and in some cases, a complete microprocessor interface. When these two products are used together, complete Data Acquisition Systems can be configured in a space efficient manner.

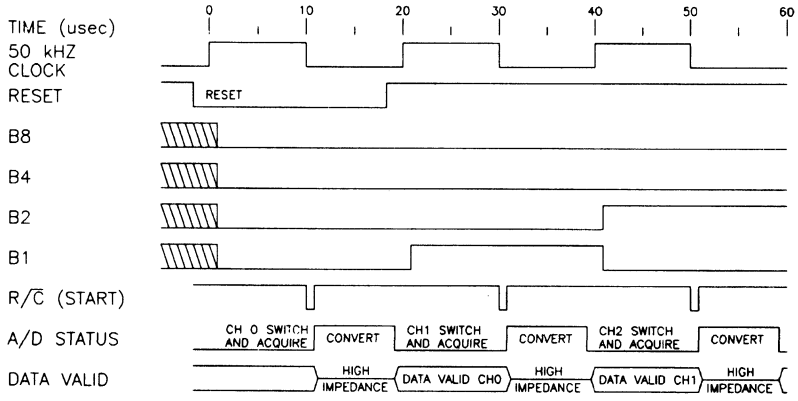
Single channel acquisition and conversion is accomplished by selecting the desired channel, stobing clock input and initiating the conversion cycle. The T/H amplifier internal to the Sampling A/D acquires and tracks the analog input during the MUX switching and settling time. Once settled and acquired, conversions can be initiated.

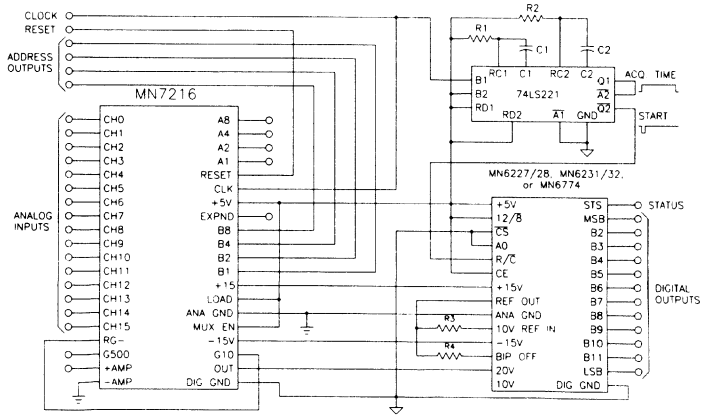
The circuit and timing diagram below illustrates a 16-channel, single-ended, 12-bit data acquisition system with a minimum of components. In this case, the MN7216 can be used with either the MN6227/28, MN6231/32 or the MN6774 Sampling A/D converters.

For the sake of simplicity, the sampling A/D is shown configured in a stand-alone mode of operation (these particular devices include a complete microprocessor interface and can be operated under full microprocessor control). The MN7216 is configured to operate in the sequential mode with an instrumentation amplifier gain of +10.

In the example, Reset is brought low prior to the rising edge of Master Clock, resetting the MUX address to channel 0. Additionally, the rising edge of Master Clock triggers the B1 input of the one-shot, creating a delayed start convert signal for the Sampling A/D. This delay allows for MUX switching, instrumentation amplifier settling and T/H acquisition times. The acquisition time delay is set by the values of R1 and C1. When the Q1 output of the one-shot times out, its falling edge triggers the A2 input, thereby creating the sampling A/D converters start convert signal. The values of R2 and C2 set the width of the start convert signal. When the conversion is complete (signaled by the falling edge of the sampling A/D converter's Status output), valid output data can be read. The next rising edge of Master Clock increments the channel address to Channel 1 and initiates the settling/acquisition conversion process again.

Other system options might include random MUX addressing, in which case, the address inputs A1 thru A8 would be set to the desired address prior to the rising edge of the Master Clock signal. In this case, Load (pin 27) would be tied to ground.





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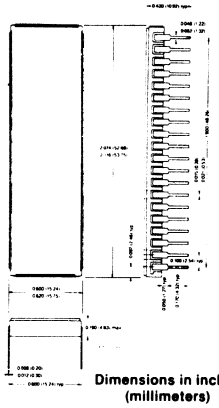
MN7450
MN7451

8-CHANNEL 16-Bit
DATA ACQUISITION SYSTEM

FEATURES

- **Complete DAS:**
  - **Latched Input MUX**
  - **Software Programmable Gain Amplifier**
  - **Buffer Amplifier**
  - **Inherent T/H Function**
  - **Internal Reference**
  - **Internal Clock Option**
  - **16-Bit Self-Calibrating A/D Converter**
- **Small Double-Wide 40-Pin DIP**
- **8X2 Byte Output Format**
- **8 Single-Ended Input Channels**
- **Input Over-Voltage Protection**
- **Full Digital Control:**
  - **MUX Channel**
  - **Gain Range**
  - **Unipolar/Bipolar**
- **Low Initial Gain and Offset Error**

40 PIN SIDE BRAZED DIP



Dimensions in inches (millimeters)

DESCRIPTION

The MN7450 and MN7451 are self-calibrating 8-channel, 16-bit data acquisition systems offered in a small, industry-standard, 40-pin, double-wide dual-in-line package. These units are complete, single-package data acquisition components and contain an input multiplexer, software programmable gain amplifier, input buffer and a 16-bit self-calibrating sampling A/D converter.

The multiplexer features eight single-ended, over-voltage-protected input channels whose latched address inputs are both TTL and CMOS logic compatible. In addition, the input multiplexer features break-before-make operation. The software-programmable gain amplifier features latched selections of gain (1,2,4 or 8) without the need for additional external components. The A/D converter section of this complete DAS features self-calibration and completeness of function. Features include an on-board user-optional internal clock, analog input buffer amplifier, internal reference and data output demultiplexer (8 x 2 output format).

These devices guarantee 16-bit no-missing-codes performance at 25°C and 15-bit no-missing codes over temperature. Gain error is specified as ±0.1% maximum while initial zero errors are specified as ±0.05%FSR maximum (after initial self-calibration). The system can be operated in two modes. In the pipelined mode, signal acquisition is accomplished during the conversion cycle. Maximum throughput in this mode of operation is 47.65kHz. In the non-pipelined mode, analog input channels are selected and then converted in a serial fashion. Throughput in the non-pipelined mode is 17.5kHz.

The small size and completeness of function of the MN7450 and MN7451 make them ideal for applications in high-end industrial and military/aerospace applications where size and performance are paramount considerations. These devices are available with optional Environmental Stress Screening. Contact the factory for availability of MIL-H-38534 compliant devices.

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324 Clark St., Worcester, MA 01606 (508) 852-5400

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MN7450/7451 8-CHANNEL 16-BIT DATA ACQUISITION SYSTEM

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN7450, MN74501J, K	0°C to 6+70°C
MN7450, MN7451S, T	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
$+V_{CC}$ Supply (Pin 13)	0 to +18V
$-V_{CC}$ Supply (Pin 14)	0 to −18V
$+V_{DD}$ Supply (Pin 35)	−0.3 to +6 Volts
$-V_{DD}$ Supply (Pin 37)	+0.3 to −6 Volts
Analog Inputs	$\pm V_{CC}$ ±2 Volts
Digital Inputs	−0.3 to $+V_{DD}$ +0.3 Volts

ORDERING INFORMATION

PART NUMBER **MN7450 T / B CH**

Select MN7450 (0 to +5V, ±5V) or MN7451 (0 to +10V, ±10V).
Select suffix J, K, S, or T for desired performance and specified temperature range.
Add /B to S or T models for Environmental Stress Screening.
Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.
Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, $\pm V_{CC}$ = ±15V, $\pm V_{DD}$ = ±5V, F_{CLK} = 4MHz (EXTERNAL) unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels		8 Single-Ended		
Input Voltage Range:				
MN7450: Unipolar		0 to +5		Volts
Bipolar		±5		Volts
MN7451: Unipolar		0 to +10		Volts
Bipolar		±10		Volts
Input Bias Current			±10	nA
Input Leakage Current		±1		nA
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.4	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			±10	μA
Logic "0" (V_{IL} = +0.4V)			±10	μA
DIGITAL OUTPUTS				
Output Coding: Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" (I_{OH} = −40μA)	+2.4			Volts
Logic "0" (I_{OL} = +1.6mA)			+0.4	Volts
3-State Output Leakage			±10	μA
REFERENCE OUTPUT				
Reference Voltage	+4.45	+4.5	+4.55	Volts
POWER SUPPLY REQUIREMENTS				
Power Supply Range: $\pm V_{CC}$ Supplies	±14.55	±15	±15.45	Volts
$\pm V_{DD}$ Supplies	±4.5	±5	±5.5	Volts
Power Supply Rejection Ratio: $\pm V_{CC}$ Supplies			±0.001	%FSR/%VS
$\pm V_{DD}$ Supplies			±0.001	%FSR/%VS
Current Drains: $+V_{CC}$ Supply		+18	+25	mA
$-V_{CC}$ Supply		−17	−25	mA
$+V_{DD}$ Supply		+13.5	+20	mA
$-V_{DD}$ Supply		−13.5	−20	mA
Power Consumption		658	950	mW
DYNAMIC CHARACTERISTICS				
Conversion Time			16.5	μsec
Throughput Rate	47.5	50		kHz

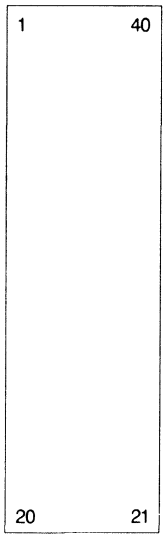
PERFORMANCE SPECIFICATIONS (T_A = +25°C, $\pm V_{CC}$ = ±15V, $\pm V_{DD}$ = ±5V, F_{CLK} = 4MHz unless otherwise indicated)

MODEL	MN7450J MN7451J	MN7450K MN7451K	MN7450S MN7451S	MN7450T MN7451T	UNITS
Integral Linearity Error: Initial (+25°C) (Max.)	±0.003	±0.0022	±0.003	±0.0022	%FSR
Over Temperature (Max.)	±0.006	±0.0045	±0.006	±0.0045	%FSR
Resolution for which No Missing Codes is Guaranteed:					
Initial (25°C)	15	16	15	16	Bits
Over Temperature	14	15	14	15	Bits
Unipolar Offset Error (Max.):					
Initial (+25°C)	±0.06	±0.04	±0.06	±0.04	%FSR
Drift	±7	±5	±7	±5	ppm of FSR/°C
Bipolar Zero Error (Max.):					
Initial (+25°C)	±0.06	±0.04	±0.06	±0.04	%FSR
Drift	±4	±2.5	±4	±2.5	ppm of FSR/°C
Gain Error (Max):					
Initial (+25°C)	±0.1	±0.05	±0.1	±0.05	%
Drift	±15	±10	±15	±10	ppm/°C

SPECIFICATION NOTES:

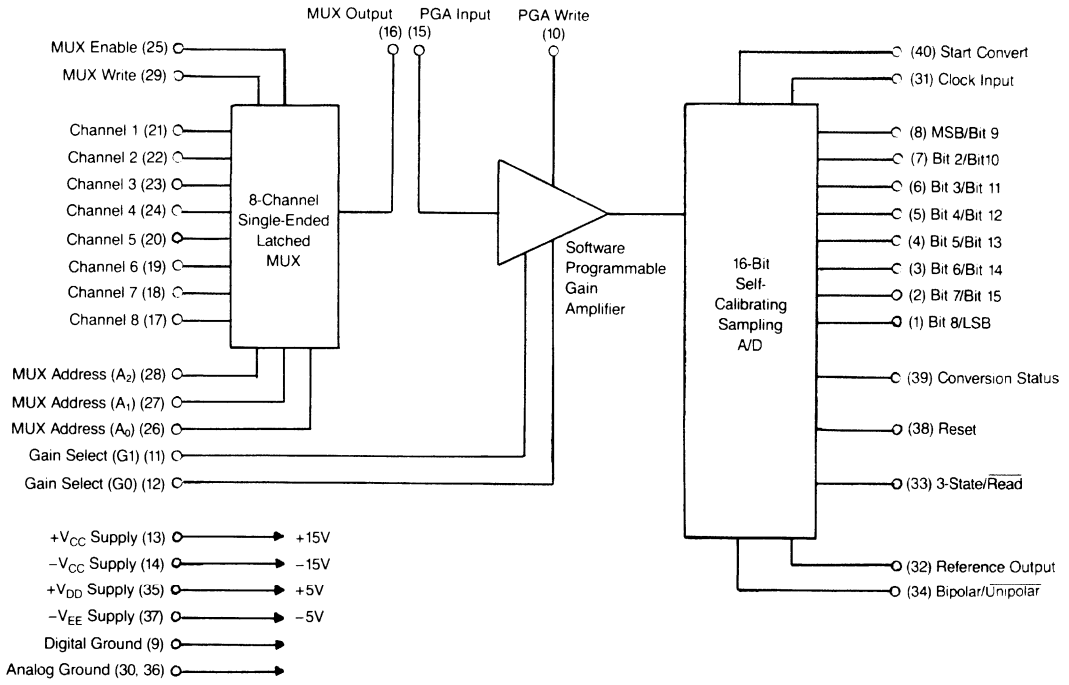
1. Specifications apply after initial calibration following power-up at +25°C.
2. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with a 0.1μF capacitor. Reference must not be used for application circuitry without buffering.
3. Performance specifications apply to overall system (MUX, PGA, and A/D) with PGA Gain set to G=1.

PIN DESIGNATIONS



1	Bit 8/LSB	40	Start Convert
2	Bit 7/Bit 15	39	Conversion Status
3	Bit 6/Bit 14	38	Reset
4	Bit 5/Bit 13	37	−5V Supply
5	Bit 4/Bit 12	36	Analog Ground
6	Bit 3/Bit 11	35	+5V Supply
7	Bit 2/Bit 10	34	Bipolar/Unipolar
8	MSB/Bit 9	33	3-State/Read
9	Digital Ground	32	Reference Output
10	PGA Write	31	Clock In
11	Gain Select G1	30	Analog Ground
12	Gain Select G0	29	Mux Write
13	+15V Supply	28	Address A2
14	−15V Supply	27	Address A1
15	PGA Input	26	Address A0
16	Mux Output	25	Mux Enable
17	Channel 8	24	Channel 4
18	Channel 7	23	Channel 3
19	Channel 6	22	Channel 2
20	Channel 5	21	Channel 1

BLOCK DIAGRAM



DESCRIPTION OF OPERATION

MUX OPERATON/CHANNEL SELECTION — The 8-channel single-ended multiplexer with latch features overvoltage protection up to ±35V, channel selection and control inputs that are fully compatible with both CMOS and TTL logic levels, and guaranteed break-before-make switching.

The MUX Address input lines A2, A1, and A0 (pins 28, 27, and 26) are used to select 1 of 8 input channels. These address lines can be changed (MUX is in a transparent state similar to unlatched multiplexers) when Mux Write (pin 29) is low and Mux Enable (pin 25) is high. The channel address is latched by bringing Mux Write high. Changes to the Mux Address lines while Mux Write is high do not affect the channel selection, freeing a microprocessor from providing constant address inputs in order to remain on a desired channel. A new channel can be addressed while Mux Write is high although it will not be selected until Mux Write returns low.

MUX Channel Selection

MUX Address A2	A1	A0	MUX Enable	MUX Write	Channel Selected
X	X	X	0	0	None
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8
X	X	X	X	1	Maintains Previous Selection

When MUX Enable and MUX Write are both low, all 8 channels are turned off. This function allows for cascading of additional input channels into the PGA Input (pin 15) or other external series signal conditioning normally connected to the MUX Output (pin 16).

PROGRAMMABLE GAIN AMP OPERATION — The single-ended software-programmable gain amplifier features latched selection of gains of 1, 2, 4 or 8 without the need for external resistors. The digital control inputs PGA Gain Select G1 (pin 11), G0 (pin 12) and PGA Write (pin 10) are TTL compatible.

As with the MUX, the PGA has both a transparent and latched mode of operation. The PGA will respond to changes of the gain select inputs while PGA Write is low. The PGA Gain Select inputs G1 and G0 are latched when PGA Write is brought high, and remain latched until PGA Write is returned low.

In application, PGA Write can be tied to MUX Write and together controlled from the same microprocessor or digital control line. Optimum performance of the DAS with regards to integral linearity drift over the full temperature range is achieved when the PGA is operated at a gain of 2.

PGA Gain Selection

Gain Select G1	G0	PGA Write	Gain
0	0	0	1
0	1	0	2
1	0	0	4
1	1	0	8
X	X	1	Previous State Latched

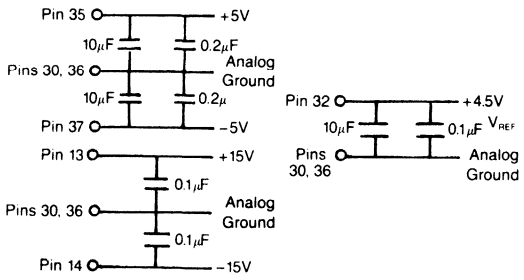
APPLICATIONS INFORMATION

POWER SUPPLIES/REFERENCE VOLTAGE — The DAS is powered from standard supplies of ±15V and ±5V. All supplies are internally connected to analog components and therefore must be of suitable quality. Supplies are decoulped internally to provide power for digital logic functions. It is strongly recommended that the power supplies be externally bypassed in the following manner.
The +15V (pin 13) and −15V (pin 14) supplies should be bypassed to analog ground with ceramic 0.1μF capacitors.

The +5V (pin 35) and −5V (pin 37) supplies should be bypassed to analog ground with tantalum 10μF caps in parallel with ceramic 0.2μF caps.

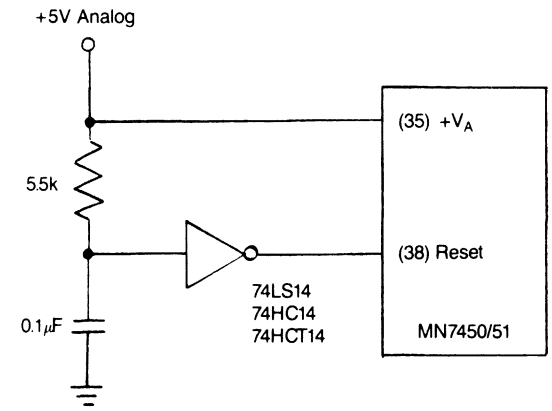
The Analog Grounds (pins 30, 36) and Digital Ground (pin 9) should be connected together and to a ground plane.

The Reference Output (pin 32) should be bypassed to analog ground with a tantalum 10μF cap in parallel with a ceramic 0.1μF cap. The reference output is an internally generated +4.5V that should not be used to drive any additional circuitry. If it absolutely needs to be used, it must be buffered.



Power Supply and Reference Decoupling

POWER-UP/CALIBRATION — Although the internal components are protected against overvoltage conditions, it is recommended that the ±15V supplies be applied simultaneously to or shortly after the ±5V supplies. Once the device is powered up, a reset calibration must be performed. The required initial reset is initiated by strobing the Reset (pin 38) high for a minimum of 100nsec. When Reset returns low, a full calibration cycle begins. This calibration cycle lasts 1,441,020 master clock cycles (equivalent to 360.255msec with a 4MHz external clock). During this time Conversion Status (pin 39) will be high, and return low when calibration is complete.



The reset calibration can be performed either under microprocessor control or by hardware using a reset circuit triggered at device power-up, as shown. The reset calibration may be used at any time or at any operating temperature throughout the lifetime of the device to ensure optimum performance.

During calibration the A/D's differential linearity self-adjusts to minimize errors due to internal component ratio drift mismatch.

ANALOG INPUT RANGES — There are two DAS models to choose from, each with unipolar and bipolar input ranges. With the PGA in a gain of 1, the MN7450 has a unipolar range of 0 to +5V and a bipolar range of -5V to +5V. The MN7451 has a unipolar range of 0 to +10V and a bipolar range of −10V to +10V. The unipolar ranges are digitally represented in Straight Binary coding. The bipolar ranges are digitally represented in Offset Binary coding. Selection of a unipolar or bipolar input transfer function is made digitally using Bipolar/Unipolar (pin 34).

MASTER CLOCK — The user has an option to use the internally generated master clock by tying Clock In (pin 31) low or to externally supply a master clock to the Clock In pin. The internal clock frequency (with Clock In low) will be a minimum of 2MHz. The external user supplied clock can be of TTL or CMOS levels and from a frequency minimum of 100kHz to a maximum of 4MHz. All device timing characteristics scale directly to the master clock frequency.

DIGITAL OUTPUT BITS — The DAS presents parallel data out in an 8-bit x 2 byte format upon execution of read operations. A read operation is performed by bringing 3-State/Read (pin 33) low. The first read following a completed conversion will bring the digital output lines out of the 3-state condition and present the 8 MSB's (MSB on pin 8 through Bit 8 on pin 1). The second read following a conversion is executed by bringing 3-State/Read back high and then low again. The 8 LSB's appear at the output (Bit 9 on pin 8 through LSB on pin 1). On subsequent reads before another conversion is complete, the MSB/LSB byte will toggle.

INITIATING CONVERSIONS — A falling edge on Start Convert (pin 40) sets the DAS into the hold mode and initiates a conversion cycle. The Start Convert input must remain low for a minimum of one master clock cycle plus 50nsec (300nsec w/4MHz clock). It must return high before the minimum conversion time of 69 master clock cycles plus 235nsec (17.235μsec w/4 MHz clock) to allow for sufficient acquisition time for the next sample.

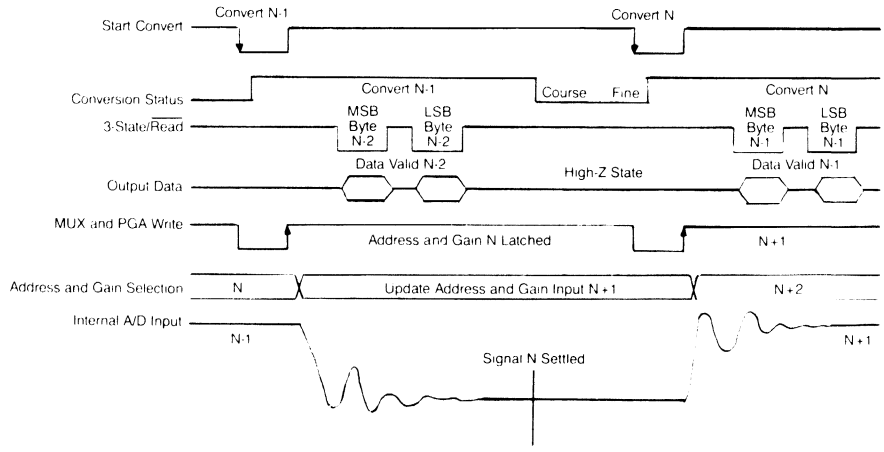
The Conversion Status output indicates that a conversion cycle is complete and data is valid when it falls low. It will return high on the first subsequent read operation or at the start of a new conversion cycle.

SIGNAL ACQUISITION — Upon completion of a conversion cycle, the sampling A/D automatically enters the track mode to acquire and follow the analog input before another conversion cycle is begun.

To operate at maximum throughput, the desired signal to be converted must already have been switched and settled through the MUX, PGA and buffer when the sampling A/D enters the track mode. This is acheived by selecting the new input signal channel and gain immediately after the sampling A/D enters the hold mode and begins to convert the old input signal channel. This pipelining technique allows the new input signal sufficient time to settle at the buffer output, which is internally disconnected to the sampling A/D input, until the old conversion is complete. The new signal then has only to be acquired by the sampling A/D, which has an acquisition time of six master clock cycles plus 2.25μsec (3.75μsec w/ 4MHz clock).

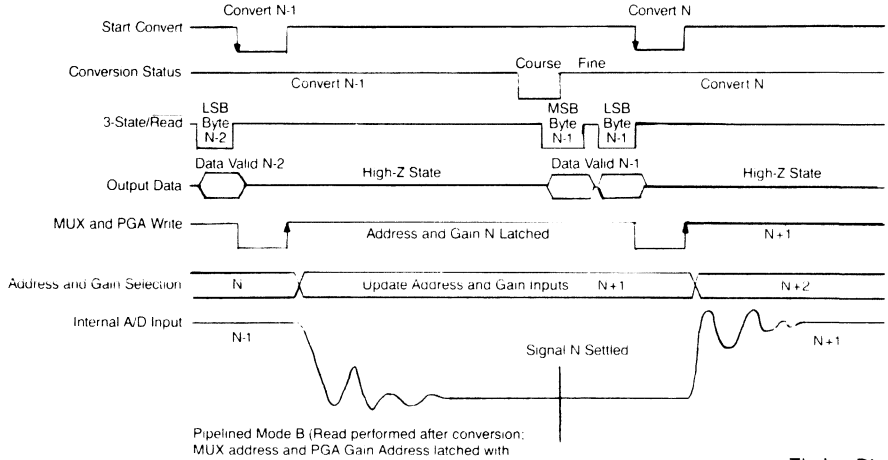
The throughput of the DAS when operated in this configuration is 47.65kHz. This pipelined configuration can be implemented by using the Start Convert signal to control both MUX Write and PGA Write. The channel and gain selections made during the conversion cycle are updated and latched as the previous channel conversion initiates.

There is a nonlinear reduction in throughput if insufficient time is allotted for switching and settling of a new channel before the acquisition cycle begins (at the fall of conversion status). This is due to the sampling A/D's method of acquisition, which is to coarse charge the hold capacitor for six master clock cycles (1.5μsec w/4MHz clock) immediately after the previous conversion is completed, and then fine charge the hold cap (and track the acquired signal) for a minimum of 2.25μsec until another Start Convert pulse is received. The required time for a new channel to be switched and settled at the buffer output is a worst case maximum of 6μsec. If the signal switched through the MUX, PGA and buffer is not settled completely before coarse charge begins, the bulk (or potentially all) of the signal acquisition must be performed in the slower fine charge mode. The absolute maximum worst case acquisition time, which occurs for a full scale step switched after completion of a previous conversion, is 40μsec. This corresponds to a worst case maximum throughput of approximately 17.5kHz (w/ 4MHz clock) for the non-pipelined configuration.



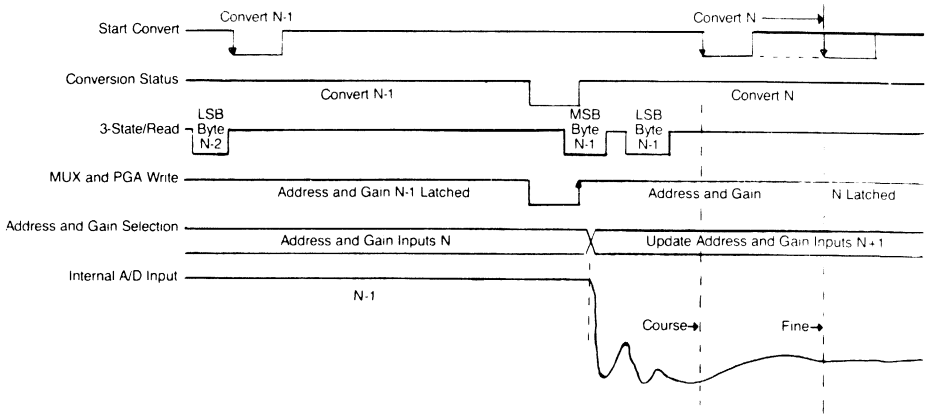
Pipelined Mode A (Read performed during conversion: MUX address and PGA Gain Address latched with Start Convert)

Timing Diagram Mode A



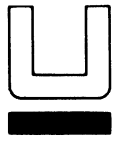
Pipelined Mode B (Read performed after conversion; MUX address and PGA Gain Address latched with Start Convert)

Timing Diagram Mode B



Non-Pipelined Mode C (Read performed after conversion; MUX address and PGA Gain Address latched with Conversion Complete)

Timing Diagram Mode C



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V/F Converters

V/F Converters

In applications where speed is not an essential consideration, voltage-to-frequency and frequency-to-voltage converters provide an ideal means to translate analog signals into the digital domain and vice-versa. For example, these devices provide an alternative to analog-to-digital converters that use successive-approximation, flash, or subranging architectures. Depending on the model and frequency range selected, Micro Networks' V/F converters offer effective dynamic ranges greater than 2,000,000:1, 5,000,000:1, or 10,000,000:1, otherwise expressed as 126, 134, or 142 dB.

In addition to their unmatched dynamic range, V/F and F/V converters offer other important advantages. Their transfer functions are inherently monotonic, with no missing codes. Further, it's possible to totally reject 50- or 60-Hz noise by appropriately selecting the counting period. Their serial outputs/inputs make it easy to provide isolation by optical coupling or other means. The noise immunity, serial format, and ease of isolation make these devices ideal in such applications as medical instrumentation, factory environments, and telemetry.

Micro Networks' line of V/F converters includes the MD3802/3805/3810 and MD3902/3905/3910 Series, which offer full-scale frequencies of 2, 5, and 10MHz. The MD38XX devices are configurable as both V/F and F/V converters, whereas the MD39XX units are dedicated V/F converters. Models MD2840/2841/2842 are A/D converters that make use of internal V/F converters to provide 20 bits of effective resolution at conversion times of 100, 200, and 500 msec, respectively. Though not a V/F or A/D converter, Model MD5024 24-bit, 50MHz counter/timer relates to these devices through its flexible control of counting and timing intervals.

MD3802/3805/3810
MD3902/3905/3910

High-Speed
V/F Converters

FEATURES

- Guaranteed Min/Max Specifications
- Dynamic Range 2,000,000:1 to 10,000,000:1
- 0.01% to 0.05% Linearity
- 10 μV/°C Offset Drift
- 5% Overrange
- Overvoltage Protection
- Voltage or Current Inputs
- Complementary Outputs TTL/CMOS Compatible
- Small 24-Pin DIP

MD2840/2841/2842

20-Bit
Integrating
A/D Converters

FEATURES

- Programmable Conversion Time
- Continuous Sampling
- $<$10-μV Sensitivity
- Repeatability to 0.3 ppm
- Resolution to 23 Bits
- 50- and 60-Hz Noise Immunity
- 5% Overrange
- Overvoltage Protection
- Small 32-Pin DIP

MD5024

24-Bit, 50-MHz
Programmable
Counter/Timer

FEATURES

- Programmable Time Base
- No Missing Counts Between Intervals
- Dual Measurement Techniques:
  - –Frequency Counting
  - –Period Averaging
- Dual Operating Modes:
  - –Continuous
  - –Triggered
- 8- or 16-Bit Data Bus
- External Clock or Onboard Crystal Drive
- Bidirectional Input/Output Bus
- Small 40-Pin DIP

V/F, F/V Converter Selection Guide

Full-Scale Range	Model #	Input Range	Dynamic Range	Type	Linearity	Power (mW)	DIP Package	Page No.
2MHz	**MD3802**	0 to −10V	>2,000,000:1 >126 dB	V/F, F/V	±0.01%FS ±0.01% of Input	750	24 Pin	10-11
5MHz	**MD3805**	0 to −10V	>5,000,000:1 >134 dB	V/F, F/V	±0.02%FS ±0.02% of Input	850	24 Pin	10-11
10MHz	**MD3810**	0 to −10V	>10,000,000:1 >142 dB	V/F, F/V	±0.05%FS ±0.05% of Input	1000	24 Pin	10-11
2MHz	**MD3902**	0 to −10V	>2,000,000:1 >126 dB	V/F	±0.01%FS ±0.01% of Input	650	24 Pin	10-15
5MHz	**MD3905**	0 to −10V	>5,000,000:1 >134 dB	V/F	±0.02%FS ±0.02% of Input	800	24 Pin	10-15
10MHz	**MD3910**	0 to −10V	>10,000,000:1 >140 dB	V/F	±0.05%FS ±0.05% of Input	850	24 Pin	10-15

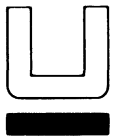
V/F - Based 20-Bit A/D Converters MD2840/2841/2842

Conversion Time (msec)	Model #	V/F Full-Scale	Differential Linearity (ppm)	Integral Linearity	Power (mW)	DIP Package	Page No.
100	**MD2840**	10MHz	0.1	±0.05%FS ±0.05% of Input	1195	32 Pin	10-5
200	**MD2841**	5MHz	0.2	±0.02%FS ±0.02% of Input	1195	32 Pin	10-5
500	**MD2842**	2MHz	0.5	±0.01%FS ±0.01% of Input	1195	32 Pin	10-5

24-Bit, 50MHz Counter/Timer MD5024

Counter Range	Programmable Time Base	Operating Mode	μP Interface	Application Mode	Power (mW)	DIP Package	Page No.
24 Bits	1 to 16 X 10^7 Clock Periods	Continuous or Triggered	8 or 16 Bits	Frequency Counting or Period Measurement	700	40 Pin	10-19

✓ Indicates New Product.



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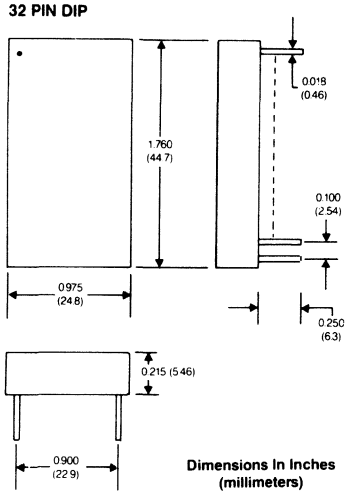
MD2840/2841/2842

100/200/500msec
INTEGRATING A/D CONVERTERS

FEATURES

- **20-Bit Integrating A/D**
- **Programmable Conversion Time**
- **Continuous Sampling**
- **$<10\mu V$ Sensitivity**
- **Repeatability to 0.3ppm**
- **Microprocessor Compatible**
- **1,000,000:1 Dynamic Range**
- **No Dead Time**

32 PIN DIP



Dimensions In Inches (millimeters)

DESCRIPTION

Models MD2840/2841/2842 are complete, integrating A/D converters performing 20-bit conversions in 100 milliseconds, 200 milliseconds and 500 milliseconds respectively. This series uses a charged-balanced asynchronous V/F converter architecture with internal counter/timer for ultra-precise repeatability of wide-dynamic-range, slowly varying signals.

With an input range of $-10\mu V$ to $-10V$, this series provides A/D conversion with a dynamic range of 1,000,000:1 (120db) without the complications and errors associated with gain-ranging or logarithmic schemes.

Their unique architecture allows for continuous integration of the input signal, improving noise rejection and avoiding the annoying dead time associated with most integrating converters. The MD2840/2841/2842 Series achieves remarkable repeatability of 0.3 ppm at up to 100 samples per second depending on mode, speed, and resolution chosen (see respective applications criteria).

Commands to the converter and data from the converter are communicated over an 8-bit microprocessor-compatible bus. The unit can be used in continuous-sample or triggered mode, where a data-ready flag alerts the μP that the conversion is complete.

APPLICATIONS

Analytical Instrumentation
Automatic Test Equipment
Clinical Chemistry
Data-Acquisition Systems
Elemental Analysis
Magnetometers
Medical Instrumentation
Seismology
Thickness & Weighing Systems
Industrial Data Collection

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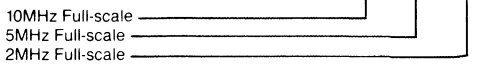
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MD2840/2841/2842 V/F, F/V CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +100°C
+15V Supply (Pin 31)	+15.45 V
−15V Supply (Pin 32)	−15.45 V
+5V Analog Supply (Pin 29)	+5.25 V
+5V Digital Supply (Pin 15)	+5.25 V
Digital Inputs (Pins 4, 5, 6, 20, 21, 22, 23, 25, 26)	−0.3V to +5.3V
Analog Input	−15 V to +15V

ORDERING INFORMATION
PART NUMBER MD2840 / 2841 / 2842



SPECIFICATIONS (T_A = +25°C, Supplies = ±15V and +5V unless otherwise specified)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to −10		Volts
Overrange			5	%
Configuration		Single-Ended		
Input Impedance MD2840, MD2841 MD2842		 6 14		 kΩ kΩ
Offset Voltage (trimmable to zero)			±10	mV
TRANSFER CHARACTERISTICS				
Full-Scale Output MD2840 MD2841 MD2842		10 5 2		MHz MHz MHz
Gain Error (trimmable to zero)			±1	%
Differential Nonlinearity MD2840 MD2841 MD2842			0.1 0.2 0.5	ppm of FSR ppm of FSR ppm of FSR
Integral Nonlinearity MD2840 (maximum) MD2841 MD2842		±0.05% FS ± 0.05% V_{IN} ±0.02% FS ± 0.02% V_{IN} ±0.01% FS ± 0.01% V_{IN}		
Full-Scale Step Response MD2840 (maximum) MD2841 MD2842		5μsec + 2 cycles of new f_{OUT} 10μsec + 2 cycles of new f_{OUT} 20μsec + 2 cycles of new f_{OUT}		
Overload Recovery MD2840 (maximum) MD2841 MD2842		12 cycles of new f_{OUT} 10 cycles of new f_{OUT} 8 cycles of new f_{OUT}		
Noise (3σ) MD2840 (V_{IN} = −10V, 1 sample/sec, MD2841 3 minutes) MD2842		5 4 3		μV μV μV
STABILITY				
Gain Temperature Coefficient		60	100	ppm of FSR/°C
Offset Temperature Coefficient		10	30	ppm of FSR/°C
Power Supply Rejection Gain Offset			200 10	ppm of FSR/%V_S μV/%V_S
Warm-up Time (to specified accuracy)			2	Minutes
DIGITAL INPUTS				
Logic Levels Logic "1" Logic "0"	+2.4		 +0.4	Volts Volts
Pulse Width R/W All Others	50 10			nsec nsec
POWER SUPPLY REQUIREMENTS				
±15V Supplies +5V Supplies	±14.55 +4.75		±15.45 +5.25	Volts Volts
Current Drains +15V −15V +5V		3 10 200		mA mA mA

THEORY OF OPERATION

The MD2840/2841/2842 Series uses a charge-balanced asynchronous V/F converter with internal counter-timer architecture as shown in Figure 1. The full-scale range of the V/F is 10MHz for the 2840, 5MHz for the 2841 and 2MHz for the 2842. The input signal is tracked by the V/F, producing a pulse frequency linearly proportional to its full scale, ie:

$$\frac{V_{in}}{V_{FS}} = \frac{F_{out}}{F_{FS}}$$

This frequency is accumulated by the counter/timer for the full conversion time of the A/D and presented at the output as a binary word up to 24 bits wide. The continuous tracking and accumulation of pulses performs an inherently monotonic integrating function.

Once the pulse accumulation is complete, the count is instantaneously transferred to the output stage, ready to be accessed by the μP. In the continuous sample mode, the counter/timer instantaneously begins to accumulate counts for the next measurement. In the external trigger mode, the counter/timer awaits a trigger command before beginning the next accumulation of pulses.

In both cases the V/F continues to generate a pulse frequency proportionately tracking the input signal. There is no dead time on these converters, so the integration period and the conversion time is the same and the terms are used interchangeably.

SENSITIVITY VS SPEED — The sensitivity of the MD2840/2841/2842 Series is directly proportional to the amount of time the converter is allowed to integrate the input signal.

$$\text{Sensitivity} = \frac{V_{FS}}{F_{FS} \bullet T_C}$$

Where V_{FS} = Full-scale Voltage
F_{FS} = Full-scale Frequency of the V/F
T_C = Conversion Time

EXAMPLE — If the MD2840, (with its 10MHz V/F) integrates the input signal for 1/10th of a second, it will accumulate 1,000,000 pulses. If the full-scale input voltage is 10V, each pulse counted will represent 10μV. Thus, the sensitivity of the MD2840 at 10 samples per second is 10μV.

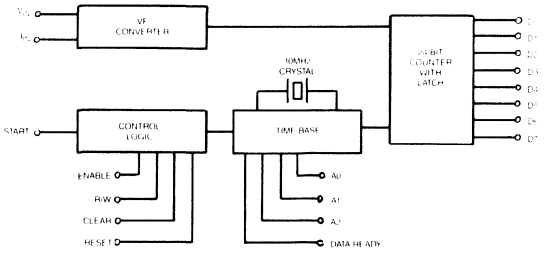


Figure 1. Md2840/2841/2842 Block Diagram

CHOOSING A CONVERSION TIME — The architecture of the MD2840/2841/2842 Series allows the designer to choose the conversion time of the A/D converter, for the sensitivity, for integration period, or for a combination of both criteria.

A. For Sensitivity — Often sensitivity, that is, the minimum change in input voltage detectable by the converter, will be the overriding criterion.

In that case, calculate the percent of full-scale represented by the sensitivity. The inverse of that number represents the full scale count needed.

$$S = V_{FS}/(F_{FS} \bullet T_C)$$

For Example
10μV on 10V_{FS} = 1ppm
1/1ppm = 10^6 counts
or
1mV on 10V = 0.01%
1/0.01% = 10^4 counts

Next, determine the amount of time required for the V/F to generate that count full scale. That will be your conversion time:

Model	10^6 Counts		10^4 Counts
MD2840 (10MHz)	0.1 sec	or	0.001 sec
MD2841 (5MHz)	0.2 sec		0.002 sec
MD2842 (2MHz)	0.5 sec		0.005 sec

B. For Integration Period —

Integration Period = $T_C = V_{FS}/(F_{FS} \bullet \text{Sensitivity})$

Example: At 100 msec integrating (conversion) time

Model	Count	Resolution	Sensitivity
MD2840 (10MHz)	10^6 counts FS	~20 Bits	10μV
MD2841 (5MHz)	5×10^5 counts FS	~19 Bits	20μV
MD2842 (2MHz)	2×10^5 counts FS	~18 Bits	50μV

C. Combination — In multiplexed systems different sensitivity/speed combinations may be required for each channel. This is easily accomplished with the MD2840/2841/2842 Series by a simple program command setting the conversion time.

With the very wide dynamic range of the MD2840/2841/2842 Series the entire input range can be sampled at high speed and low resolution until the desired level is detected. Then the integration time can be extended for higher-sensitivity measurements.

Where several instruments share one analog front-end design — a combination of speed and sensitivity can be programmed into the MD2840/2841/2842 Series "on the fly."

Sometimes the conversion time dominates the design decision. This is true when trying to reject periodic normal-mode noise — such as 50/60 Hz line pickup. Then the conversion time should be set at an integer multiple of the period of the noise (ie. 20 msec or 40 msec or 60 msec for 50Hz rejection). 100 msec integration is common as it rejects both 50 and 60 Hz pickup. Once the conversion time is chosen, the resolution and sensitivity can be calculated.

Model/ Conversion Time	**MD2840** 10MHz	**MD2841** 5MHz	**MD2842** 2MHz
100 SPS	100μV (16 Bits)	200μV (15 Bits)	500μV (14 Bits)
10 SPS	10μV (20 Bits)	20μV (19 Bits)	50μV (18 Bits)
1 SPS	1μV (23 Bits)	2μV (22 Bits)	5μV (21 Bits)

Table 1 - Sensitivity and Resolution With 0-10V F.S.

PROGRAMMING CONVERSION TIME

Conversion time is programmed by writing an 8-bit word to the A/D converter. R/W should be placed in a logic 0. Program data are loaded on lines D0-D7 and the Enable command is strobed low per Figure 2.

Note setup and hold time of 10 nsec minimum before and after Enable and the 50 nsec minimum Enable pulse width.

The programmed conversion time (T_C) is related to an external clock (F_{Clk}) by the following formula. Clock frequencies up to 50MHz are acceptable.

$$T_C = \frac{1}{F_{Clk}} \times B \times 10^N$$

For a 10MHz Crystal $T_C = \frac{1}{10^7} \times B \times 10^N$

STEP 1: Select desired conversion (integration) time.
STEP 2: Multiply time base by F_{Clk}. The answer is B X 10^N.
STEP 3: Choose B as large as possible within 1-16 range. Determine appropriate N.
STEP 4: Assemble program byte (with MSB = 1) selecting N & B from Table 2.

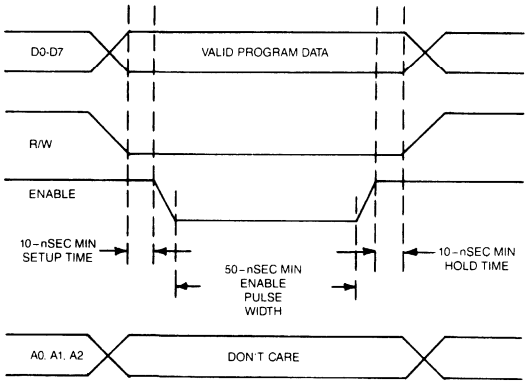


Figure 2. WRITE Command Timing

MSB D7		D6	D5	D4		LSB D3	D2	D1	D0
MSB		N2	N1	N0		B3	B2	B1	B0
0	N=	N2	N1	N0	B=	B3	B2	B1	B0
0	0	0	0	0	1	1	1	1	1
0	1	0	0	1	2	1	1	1	0
	2	0	1	0	3	1	1	0	1
	3	0	1	1	4	1	1	0	0
	4	1	0	0	5	1	0	1	1
	5	1	0	1	6	1	0	1	0
	6	1	1	0	7	1	0	0	1
	7	1	1	1	8	1	0	0	0
					9	0	1	1	1
					10	0	1	1	0
					11	0	1	0	1
					12	0	1	0	0
					13	0	0	1	1
					14	0	0	1	0
					15	0	0	0	1
					16	0	0	0	0

Table 2 - Compiling the Conversion Time Byte.

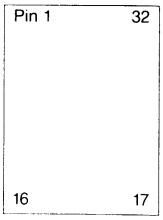
Example 1

1) For T_C = 100 msec and F_{Clk} = 10MHz
2) $T_C \times F_{Clk} = B \times 10^N$
   100 msec x 10 x 10^6 = 10 x 10^5
3) Choose N=5 B=10
4) Code — MSB 0, N 101, B 0110

Example 2

1) For T_C = 1 msec and F_{Clk} = 10MHz
2) $T_C \times F_{Clk} = B \times .10^N$
   1 msec X 10 X 10^6 = 10 X 10^3
3) Choose N=3 B=10
4) Code — MSB 0, N 011, B 0110

PIN DESIGNATIONS



1	V_{IN}	32	−15V
2	I_{IN}	31	+15V
3	Offset Trim	30	Analog Ground
4	A2	29	+5V (ANA)
4	A1	28	F_{OUT} −V/F Output Frequency
6	A0	27	F_{IN} −Input to Counter
7	D0	26	R/W−Read/Write Select
8	D1	25	Enable
9	D2	24	DR−Data Ready
10	D3	23	R−Reset
11	D4	22	S−Start
12	D5	21	CS/SS
13	D6	20	CLK In
14	D7	19	CLK Out
15	+5V (DIG)	18	Xtal
16	Digital Ground	17	Xtal

READING THE DATA

The MD2840/2841/2842 Series is capable of up to 24-bit measurements. These are read out on the 8-bit bus in three bytes. There are also overflow and programming bytes. The bytes are addressed at pin A0, A1, A2 per Table 3 via the timing commands in Figure 3.

To read data, set the R/W line to the logical "1" (high) state, and the A0, A1, A2 control lines to the appropriate states for the data byte desired. The order in which these signals are applied isn't important, as long as they are present and static for at least 10 nsec before the Enable (E) line is activated, and for a minimum of 10 nsec after Enable (E) is removed. The Enable line performs the actual read operation; it is a negative pulse, at least 50 nsec wide. Valid data is present on the output bus 30 nsec maximum after the leading edge of Enable; the data bus returns to a high impedance state 25 nsec maximum after the trailing edge of the Enable pulse.

A0	A1	A2	COMMAND	BYTE
0	0	0	READ	LOWER
1	0	0	READ	MIDDLE
0	1	0	READ	UPPER
1	1	0	READ	OVER-FLOW
1	0	1	READ	PROG BYTE

Table 3 - Addressing the data bytes.

OVERFLOW AND PROGRAMMING READBACK BYTES

If the 24-Bit counter overflows, the overflow bit (D_0) on the Overflow Byte (A = 110) will be in a high state. The data bits will roll over to zero and continue to count. Thus, using the overflow bit, it is possible to use the MD2840/2841/2842 Series as a 25-bit converter. See Table 3 and Figure 3 for commands and timing.

At any time the A/D can be interrogated as to its programmed status by reading the Program Readback Byte (A = 101). This will read back the conversion time program byte.

OPTIONS

1. Offset voltage may be trimmed to zero using a 20KΩ potentiometer with drift less than 100ppm/°C.
2. Full Scale output can be trimmed to zero error using a 200Ω potentiometer with drift less than 100ppm/°C.
3. +5V (ANA) may be regulated for optimal performance using a National 78L05 (typical) +5V regulator.
4. An optical isolator or isolation transformer may be inserted between F_{out} and F_{in} to isolate the analog and digital sections of the A/D, if dictated by system requirements.
5. Clock frequency may come from a system clock, up to 50MHz maximum, applied to CLK_{IN} (pin 20). Alternately an oscillator clock can be generated using a crystal (10MHz typical). C_{Trim} may then be added to trim the crystal to the exact frequency desired. C_{Trim} values between 2 and 25pF are typical.

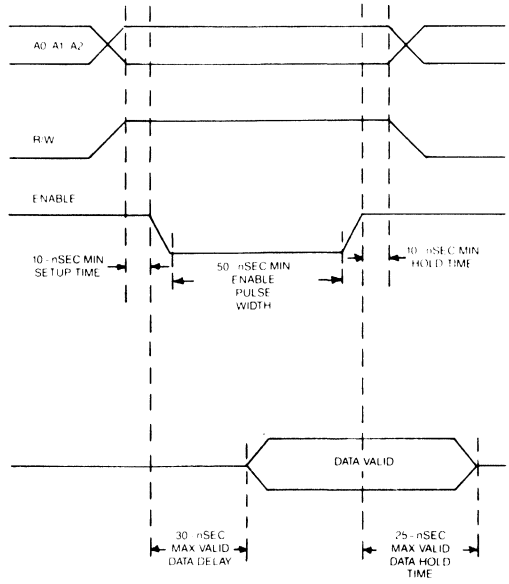


Figure 3. READ Command Timing

NOTES:

DR — Data Ready — Generates a logical "1" that indicates that data has been latched and is ready to read. On Reset (pin 23) Data Ready becomes active high and remains high until a READ operation is performed.

R — Reset — When logical "0" is applied to pin 23 all operations are stopped and all counters and latches are reset to zero. A minimum pulse width of 100 nsec at logical 0 is requred.

S — Start and CS/SS — Continuous Sample /Synchronous Start — When CS/SS is low, the converter, after receiving a single start command, will continuously convert the input. When CS/SS is High, the converter will wait for a START command before beginning the next conversion. The START command is positive edge - triggered.

+5V (DIG) and +5V (VFC) may be supplied from the same +5V supply. See Option #3.

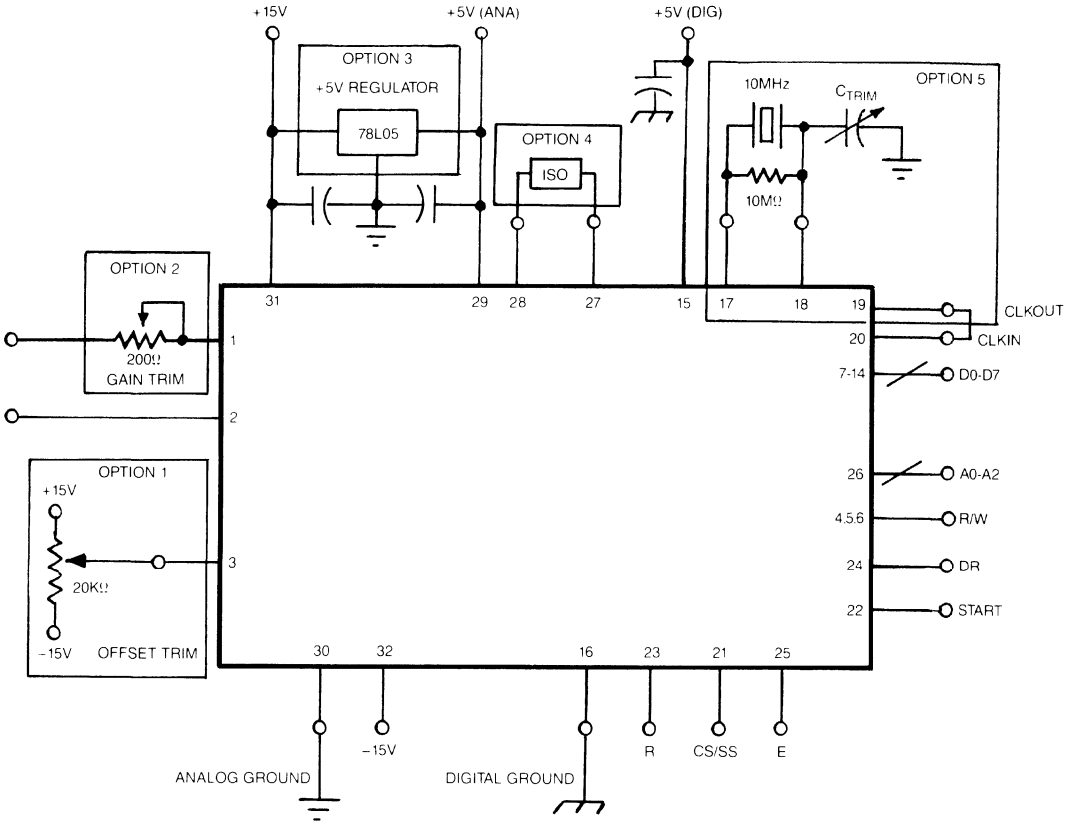
F_{out} and F_{in} should be tied together for normal operation. F_{out} can be used as a test point to check the output of the V/F. An optical isolator or isolation transformer may be inserted between F_{out} and F_{in} to totally isolate the analog and digital sections of the converter. See Option #4.

CLK IN Receives a system clock up to 50MHz. CLK_{in} should be tied to CLK_{out} if Crystal Oscillator Clock Circuit is used. See Option #5.

Xtal No connection if clock is supplied by System to pin 20 (CLK_{in}). For self-generated Crystal Clock See Option #5.

ORDERING INFORMATION

MD284020 Bits • 100 msec
MD284120 Bits • 200 msec
MD284220 Bits • 500 msec



Connection Diagram With Options

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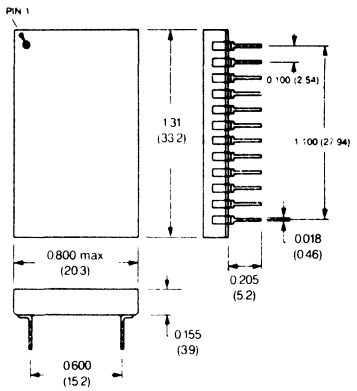
MD3802/3805/3810

2/5/10MHz
V/F, F/V CONVERTERS

FEATURES

- **Guaranteed Minimum/ Maximum Specifications**
- **Wide Dynamic Range**
  >2,000,000/5,000,000/10,000,000:1
  >126/134/142 dB
- **Excellent Linearity**
  ±0.01/0.02/0.05% FSR
  ±0.01/0.02/0.05% of Input
- **Excellent Stability**
  10 μV/°C Offset
  75 ppm/°C Gain
- **Voltage or Current Inputs**
- **Offset and Gain Error Trimmable to Zero**
- **Complementary Frequency Outputs-TTL/CMOS Compatible**
- **Small 24-Pin DIP**
- **Low Power**
  <0.75/0.85/1.0W

24-PIN CERAMIC DIP



Dimensions In Inches (millimeters)

DESCRIPTION

Models MD3802/3805/3810 are high-performance, precision 2/5/10MHz full-scale voltage-to-frequency converters, intended for those applications that require maximum performance at the most economical cost. These converters feature >125/134/142-dB dynamic range, ±0.01/0.02/0.05% linearity, and ±5% overrange capability.

All models accept a −100μV to −10V full-scale analog input signal that is converted to an output signal whose frequency is proportional to the full-scale frequency within ±0.01/0.02/0.05% linearity, using the long-proven charge-balance technique. The devices offer buffered complementary TTL-compatible frequency outputs that will drive capacitive loads as high as 50 pF.

Models MD3802/3805/3810, in addition to functioning as V/F converters, can also be used as F/V converters. In this configuration, the converters will accept frequencies from dc to 2/5/10MHz and will produce proportional single-ended output voltages from 0V to −10V.

In applications where overall system throughput must be maintained at a specific rate, or where fixed offset or different scale voltages would be more convenient, custom frequencies and/or custom trimming can be easily accommodated. By increasing the full-scale output frequency by 10 to 20% for example, additional time would be available for the system microprocessor to access the results of each conversion. Please contact the factory to discuss your specific timing requirements.

All models are packaged in a 1.31″ x 0.80″ x 0.15″ 24-pin ceramic DIL package. Power dissipation is lower than 0.75/0.85/1.0 watts, and operation to specified accuracy is guaranteed over the 0°C to +70°C temperature range.

APPLICATIONS

Precision Integration
Digital Data Transmission
Frequency Synthesis
Analytical Instrumentation
Medical Instrumentation
Telemetry
Data Recording
Weighing Systems
Tachometers
Accelerometers
Flow Meters
Robotics

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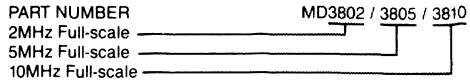
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MD3802/3805/3810 V/F, F/V CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (Pin 1)	+15.45 V
−15V Supply (Pin 5)	−15.45 V
+5V Supply (Pin 20)	+5.25 V
Analog Input (Pins 11)	−15 V to +15V

ORDERING INFORMATION



SPECIFICATIONS (T_A = +25°C, Supplies = ±15V and +5V unless otherwise specified)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to −10		Volts
Nonsaturating Overrange	5			%
Configuration		Single-Ended		
Input Impedance MD3802		15		kΩ
MD3805		10		kΩ
MD3810		5		kΩ
Offset Voltage (trimmable to zero)		±7	±10	mV
TRANSFER CHARACTERISTICS				
Full-Scale Output MD3802	2			MHz
MD3805	5			MHz
MD3810	10			MHz
Transfer Function MD3802		$2MHz \bullet (V_{IN}/10V)$		
MD3805		$5MHz \bullet (V_{IN}/10V)$		
MD3810		$10MHz \bullet (V_{IN}/10V)$		
Gain Error (trimmable to zero)			±1	%
Nonlinearity (max.) MD3802		$\pm 0.01\%FS \pm 0.01\%V_{IN}$		
(not specified under overrange conditions) MD3805		$\pm 0.02\%FS \pm 0.02\%V_{IN}$		
MD3810		$\pm 0.05\%FS \pm 0.05\%V_{IN}$		
Full-Scale Step Response MD3802		2 cycles of new f_{OUT} +20μsec		
(maximum; to 0.01%) MD3805		2 cycles of new f_{OUT} +10μsec		
MD3810		2 cycles of new f_{OUT} +5μsec		
Overload Recovery MD3802		8 cycles of new f_{OUT}		
MD3805		10 cycles of new f_{OUT}		
MD3810		12 cycles of new f_{OUT}		
STABILITY				
Gain Temperature Coefficient MD3802		50	75	ppm of FSR/°C
MD3805, MD3810		75	100	ppm of FSR/°C
Offset Temperature Coefficient		10	30	ppm of FSR/°C
Power Supply Rejection Gain			200	ppm of FSR/%V_S
Offset			10	μV/%V_S
Warm-up Time (to specified accuracy)			2	Minutes
OUTPUT				
Pulse Width MD3802	200	250	300	nsec
MD3805	80	100	120	nsec
MD3810	40	50	60	nsec
Logic Levels: Logic "1"	+3.5	+4.0	+4.5	Volts
Logic "0" (3 mA sink)			0.4	Volts
POWER SUPPLY REQUIREMENTS				
±15V Supplies	±14.55		±15.45	Volts
+5V Supply	+4.75		+5.25	Volts
+15V Current Drain MD3802			20	mA
MD3805			25	mA
MD3810			35	mA
−15V Current Drain			10	mA
+5V Current Drain MD3802			45	mA
MD3805			50	mA
MD3810			60	mA
Power Dissipation MD3802			750	mW
MD3805			850	mW
MD3810			1000	mW

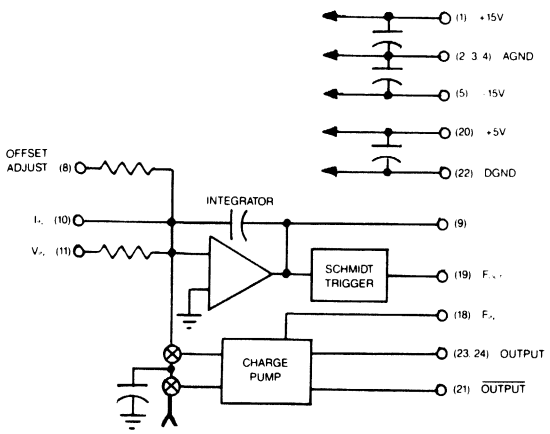


Figure 1. MD3802/3805/3810 Block Diagram.

USING THE MD38XX

GENERAL CONSIDERATIONS — A typical circuit configuration for the MD38XX models used as V/F converters is depicted in Figure 2. The layout should be clean, with output pulses routed as far away from the input analog signals as possible. To obtain maximum performance, bypass capacitors, as shown in both figures, should be mounted right at the appropriate pins of the converters.

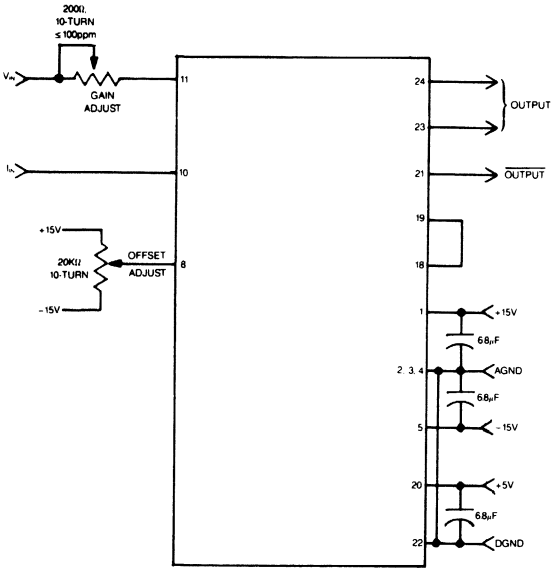


Figure 2. V/F Converter Configuration.

OFFSET AND GAIN TRIMMING — The OFFSET adjustment potentiometer should be a 20 kΩ, 10-turn unit. With this pot in the circuit, initial offsets of up to ±10mV may be trimmed to zero.

The GAIN adjustment potentiometer should be a 200Ω, 10-turn unit. To ensure that the temperature coefficient of the potentiometer does not become significant relative to the overall gain tempco specification, a 100 ppm or better potentiometer is recommended. With this pot in the circuit, initial gain errors of up to ±2% may be trimmed to zero.

GROUNDING — The Analog and Digital grounds are internally separate in the MD38XX models. The use of ground plane is not necessary for proper operation of the MD38XX. However, a ground plane is recommended with any analog signal conditioning circuitry that my be used in a V/F application, especially if this circuitry involves high gains. Any amplifiers used ahead of the MD38XX should have decoupling capacitors on their power supply pins to help eliminate potential problems with the high-frequency output of the V/F.

OFFSET AND GAIN CALIBRATION

OFFSET CALIBRATION — Offset calibration should be performed prior to gain calibration. With a −1mV analog input signal at pin 11 of the MD38XX, adjust the OFFSET potentiometer until a frequency of 200/500/1000Hz is observed on output pins 21, 23 or 24.

GAIN CALIBRATION — With a full scale analog input voltage of −10.00V on pin 11 (MD38XX), adjust the GAIN potentiometer until a full scale frequency of 2.000/5.000/10.000MHz is observed on output pin 21, 23, or 24.

N/C PINS — Pins marked as N/C (no connection) have no electrical connection to the internal circuitry of the MD38XX.

OUTPUT PINS — Pins 23 and 24 are tied together internally. Either or both may be used as the source of the frequency output of the MD38XX, as long as the load specifications are not exceeded. Pin 21 provides a complementary signal relative to pins 23 and 24 with similar loading limits.

V/F MODE

ANALOG INPUTS — Single-ended analog inputs from 0 to −10V are applied to pin 11 of the V/F converter through the GAIN adjustment potentiometer.

F/V MODE

Figure 3 depicts the typical circuit configuration for the MD38XX used in the F/V mode. In this mode, the MD38XX will accept a 0 to 2/5/10MHz input pulse train, with negative-going pulses, (250±50) (100±20) (50±10)nsec in width, and will produce a voltage output proportional to the input frequency. Riding on the ouput voltage will be a ripple voltage. Additional filtering of the output voltage by the use of a 2-pole active filter will reduce the output ripple as shown in Table 1. A representive 2-pole active filter circuit is shown in Figure 4. Suitable component values are listed in Table 1. It is recommended that a high input impedance, low noise op amp be used, and that offset nulling be done in order to obtain accurate dc performance.

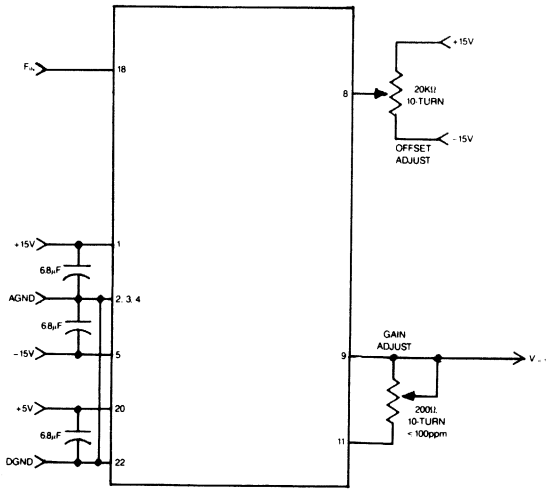


Figure 3. F/V Converter Configuration.

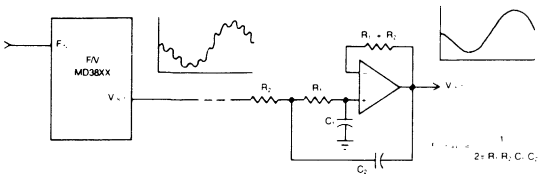


Figure 4. Typical 2-Pole Active Filter

V/F/V ANALOG DATA INK — Figure 5 depicts the MD38XX used as both the V/F and F/V in an analog data link. Low-level analog data may be transmitted over considerable distances with no degradation due to noise using this system, and with total system linearity of 0.02/0.04/0.10%.

F_{CUTOFF}	C_1(pF)	C_2(pF)	R_1(kΩ)	R_2(kΩ)	Output Ripple (mV) MD3802	MD3805	MD3810
20 kHz	180	470	16.2	46.2	70	35	5
25 kHz	150	330	21.0	39.2	60	20	5
30 kHz	150	330	17.4	27.4	60	40	5
50 kHz	68	180	16.9	48.7	50	20	5
100 kHz	33	100	14.3	53.6	80	20	5

Table 1. Ripple Reduction by Active Filter

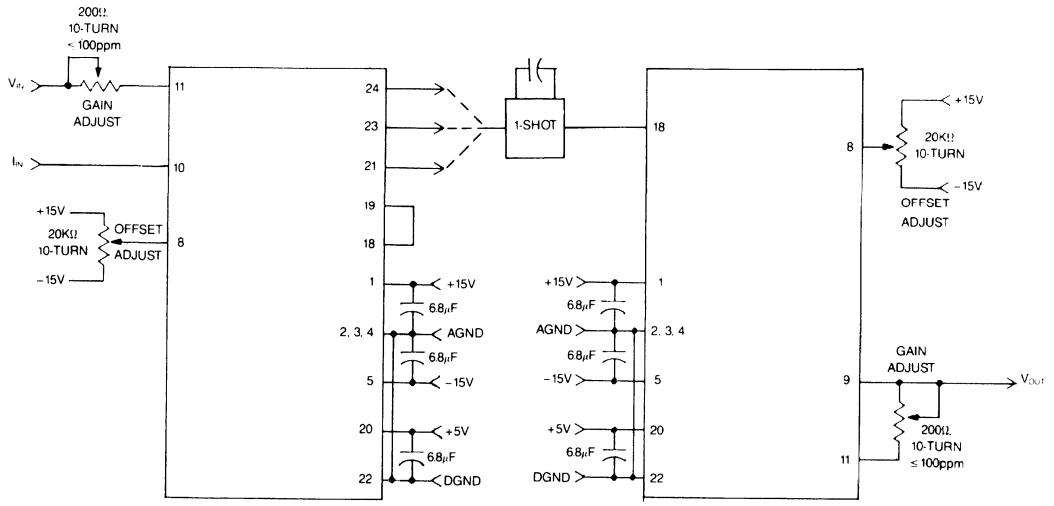
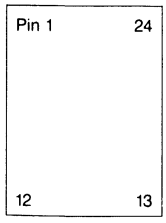


Figure 5. Analog Data Link.

PIN DESIGNATIONS



1 +15V Supply
2 Analog Ground
3 Analog Ground
4 Analog Ground
4 −15V Supply
6 No Connect
7 No Connect
8 Offset Trim
9 V_{OUT}
10 I_{IN}
11 V_{IN}
12 No Connect
24 Output
23 Output
22 Digital Ground
21 Output
20 +5V Supply
19 F_{OUT}
18 F_{IN}
17 No Connect
16 No Connect
15 No Connect
14 No Connect
13 No Connect

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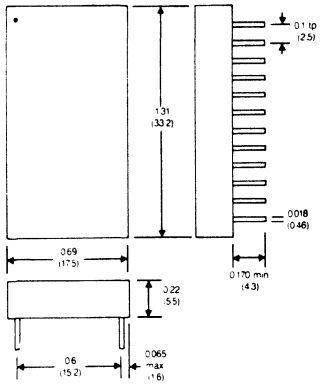
MD3902/3905/3910

2/5/10MHz
V/F CONVERTERS

FEATURES

- **Outstanding Price/ Performance Ratio**
- **Guaranteed Minimum/ Maximum Specifications**
- **Wide Dynamic Range**
  >2,000,000/5,000,000/10,000,000:1
  >126/134/142 dB
- **Excellent Linearity**
  ±0.01/0.02/0.05% FSR
  ±0.01/0.02/0.05% of Input
- **Excellent Stability**
  10 μV/°C Offset
  60 ppm/°C Gain
- **Voltage or Current Inputs**
- **Offset and Gain Error Trimmable to Zero**
- **Complementary Frequency Outputs-TTL/CMOS Compatible**
- **Small 24-Pin DIP**
- **Low Power**
  < 0.65/0.80/0.85W

24-PIN CERAMIC DIP



Dimensions In Inches
(millimeters)

DESCRIPTION

Models MD3902/3905/3910 are high-performance, precision 2/5/10MHz full-scale voltage-to-frequency converters, intended for those applications that require maximum performance at the most economical cost. These converters feature >125/134/142-dB dynamic range, ±0.01/0.02/0.05% linearity, and ±5% overrange capability. The MD3902/3905/3910 devices feature overall performance and stability virtually identical to that of similar units costing 40% or more.

All models accept a −100μV to −10V full-scale single-ended analog input signal that is converted to an output signal whose frequency is proportional to the full-scale frequency, within 0.01/0.02/0.05% linearity, using the long-proven charge-balance technique. The devices offer 5% overrange capability, and buffered complementary TTL-compatible frequency outputs that will drive capacitive loads as high as 50 pF.

Stability of the MD3902/3905/3910 Series is excellent for V/F converters in the respective price ranges, with 10μV/°C typical, 30μV/°C maximum offset and 60 ppm/°C typical, 100 ppm/°C maximum gain temperature coefficients. Warm-up time to specified accuracy is less than two minutes.

In applications where overall system throughput must be maintained at a specific rate, or where fixed offset or different scale voltages would be more convenient, custom frequencies and/or custom trimming can be easily accommodated. By increasing the full scale output frequency by 10 to 20%, for example, additional time would be available for the system microprocessor to access the results of each conversion. Please contact the factory to discuss your specific timing requirements.

All models are packaged in a 1.31″ x 0.69″ x 0.22″ 24-pin plastic DIL package. Power dissipation is lower than 0.65/0.80/0.85 watts, and operation to specified accuracy is guaranteed over the 0°C to +70°C temperature range.

APPLICATIONS

Precision Integration
Digital Data Transmission
Frequency Synthesis
Analytical Instrumentation
Medical Instrumentation
Telemetry
Data Recording
Weighing Systems
Tachometers
Accelerometers
Flow Meters
Robotics

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MD3902/3905/3910 V/F CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (Pin 1)	+15.45 V
−15V Supply (Pin 5)	−15.45 V
+5V Supply (Pin 20)	+5.25 V
Analog Input (Pins 11)	−15V to +15V

ORDERING INFORMATION

PART NUMBER MD3902 / 3905 / 3910
2MHz Full-scale
5MHz Full-scale
10MHz Full-scale

SPECIFICATIONS (T_A = +25°C, Supplies = ±15V and +5V unless otherwise specified)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to −10		Volts
Nonsaturating Overrange	5			%
Configuration		Single-Ended		
Input Impedance MD3902		15		kΩ
MD3905		6		kΩ
MD3910		6		kΩ
Offset Voltage (trimmable to zero)		±7	±10	mV
TRANSFER CHARACTERISTICS				
Full-Scale Output MD3902	2			MHz
MD3905	5			MHz
MD3910	10			MHz
Transfer Function MD3902		2MHz•(V_{IN}/10V)		
MD3905		5MHz•(V_{IN}/10V)		
MD3910		10MHz•(V_{IN}/10V)		
Gain Error (trimmable to zero)			±1	%
Nonlinearity (max.) MD3902		±0.01%FS±0.01%V_{IN}		
(not specified under overrange conditions) MD3905		±0.02%FS±0.02%V_{IN}		
MD3910		±0.05%FS±0.05%V_{IN}		
Full-Scale Step Response MD3902		2 cycles of new f_{OUT} +20μsec		
(maximum; to 0.01%) MD3905		2 cycles of new f_{OUT} +10μsec		
MD3910		2 cycles of new f_{OUT} +5μsec		
Overload Recovery MD3902		8 cycles of new f_{OUT}		
MD3905		10 cycles of new f_{OUT}		
MD3910		12 cycles of new f_{OUT}		
STABILITY				
Gain Temperature Coefficient		60	100	ppm of FSR/°C
Offset Temperature Coefficient		10	30	ppm of FSR/°C
Power Supply Rejection Gain			200	ppm of FSR/%V_S
Offset			10	μV/%V_S
Warm-up Time (to specified accuracy)			2	Minutes
OUTPUT				
Pulse Width MD3902	200	250	300	nsec
MD3905	80	100	120	nsec
MD3910	35	50	65	nsec
Logic Levels: Logic "1"	+3.5	+4.0	+4.5	Volts
Logic "0" (3 mA sink)			0.4	Volts
POWER SUPPLY REQUIREMENTS				
±15V Supplies	±14.55		±15.45	Volts
+5V Supply	+4.75		+5.25	Volts
+15V Current Drain MD3902			20	mA
MD3905			30	mA
MD3910			30	mA
−15V Current Drain			10	mA
+5V Current Drain MD3902			40	mA
MD3905			40	mA
MD3910			50	mA
Power Dissipation MD3902			650	mW
MD3905			800	mW
MD3910			850	mW

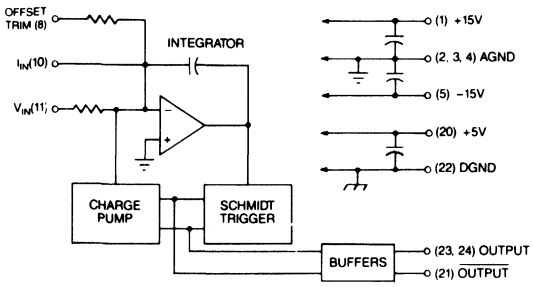


Figure 1. MD3902/3905/3910 Block Diagram

USING THE MD39XX

GENERAL CONSIDERATIONS — Figure 2 depicts a typical circuit configuration for the MD39XX. The layout should be clean, with output pulses routed as far away from the input analog signals as possible. To obtain maximum performance, bypass capacitors, as shown in Figure 2, should be mounted right at the appropriate pins of the MD39XX.

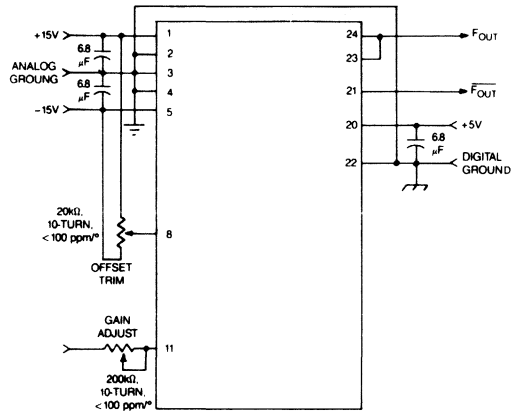
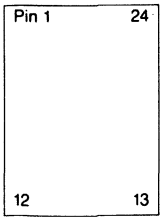


Figure 2. Typical Circuit Configuration

PIN DESIGNATIONS



1 +15V Supply	24 Output
2 Analog Ground	23 Output
3 Analog Ground	22 Digital Ground
4 Analog Ground	21 $\overline{Output}$
5 -15V Supply	20 +5V Supply
6 No Connect	19 No Connect
7 No Connect	18 No Connect
8 Offset Trim	17 No Connect
9 No Connect	16 No Connect
10 I_{IN}	15 No Connect
11 V_{IN}	14 No Connect
12 No Connect	13 No Connect

OFFSET AND GAIN TRIMMING — The OFFSET adjustment potentiometer should be a 20 kΩ, 10-turn unit. To insure that the temperature coefficient of the potentiometer does not become significant relative to the overall offset tempco specification, a 100 ppm or better potentiometer is recommended. With this pot in the circuit, initial offsets of up to ±10mV may be trimmed to zero.

The GAIN adjustment potentiometer should be a 200Ω, 10-turn unit with a recommended temperature coefficient of 100 ppm or better. With this pot in the circuit, initial gain errors of up to ±2% may be trimmed to zero.

GROUNDING — The Analog and Digital grounds are internally separate in the MD39XX. The use of ground plane is not necessary for proper operation of the MD39XX. However, a ground plane is recommended with any analog signal conditioning circuitry that may be used in front of the V/F, especially if this circuitry involves high gains. Any amplifiers used ahead of the MD39XX should be decoupled to eliminate potential problems with the high-frequency output of the V/F.

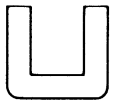
OFFSET AND GAIN CALIBRATION

OFFSET CALIBRATION — Offset calibration should be performed prior to gain calibration. With a -10mV analog input signal at pin 11 of the MD39XX, adjust the OFFSET potentiometer until a frequency of 2.000/5.000/10.000kHz is observed on output pins 21, 23 or 24.

GAIN CALIBRATION — With a full-scale analog input voltage of -10.00V on pin 11, adjust the GAIN potentiometer until a full-scale frequency of 2.000/5.000/10.000MHz is observed on output pin 21, 23, or 24.

N/C PINS — Pins marked as No Connect have no electrical connection to the internal circuitry of the MD39XX.

OUTPUT PINS — Pins 23 and 24 are tied together internally. Either or both may be used as the source of the frequency output of the MD39XX, as long as the load specifications are not exceeded. Pin 21 provides a complementary signal relative to pins 23 and 24 with similar loading limits.



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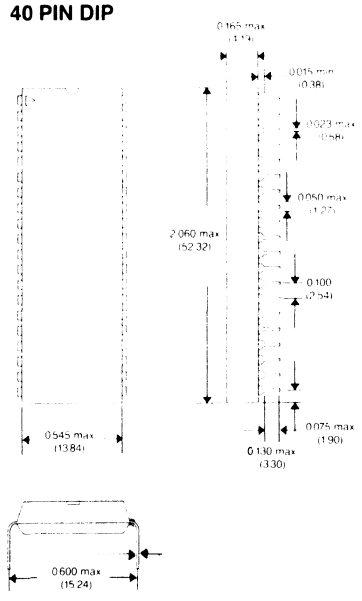
MD5024

24-Bit, 50MHz
COUNTER/TIMER

FEATURES

- **24-Bit, 50MHz Counter**
- **Wide-Range, Programmable Time Base**
- **Microprocessor-Compatible**
- **No Missing Counts Between Counting Intervals**
- **8- or 16-bit Data Bus**
- **Dual Measurement Techniques Frequency Counting or Period Averaging**
- **Dual Operating Modes Continuous or Triggered**

40 PIN DIP



Dimensions In Inches
(millimeters)

DESCRIPTION

The MD5024 is a 24-bit, 50MHz, counter/timer fully programmable and microprocessor compatible. It is capable of implementing the complete counter/timer function in one 40-pin monolithic IC.

It contains a 24-bit, 50MHz counter; a wide range, programmable time base; a crystal-oscillator drive circuit for establishing a crystal-controlled clock; a multiplexer for switching between frequency counting and period measurement; an interface to an 8- or 16-bit microprocessor bus; and status lines to report the state of the counter/timer and associated circuitry.

Under microprocessor control, the MD5024 can switch between frequency counting and period measurement; and between triggered mode and continuous sample mode. The program may be changed for each cycle or set once and forgotten.

The MD5024 has a unique counter architecture that captures every incoming pulse, even during bus transfers, and thus guarantees not to miss a single pulse. This is achieved without external synchronizing circuitry.

An on-board crystal drive circuit is provided if a system clock is not utilized. Clock rates up to 50MHz will be accepted. The period of the clock establishes the minimum resolution of the time base.

The time base of the MD5024 is programmable from one clock period to 16 x 10^7 clock periods. For a 10MHz clock that's 100 nsec to 16 seconds.

Data and command Input/Output is accomplished through a bi-directional data bus configurable in 8- or 16-bit bytes.

APPLICATIONS

Wide Dynamic Range A/D Converters for Analytical Instrumentation

Seismic Data Acquisition

Biomedical Data Acquisition

Frequency Meters

Period Averaging Counters

General Purpose Counter/Timer

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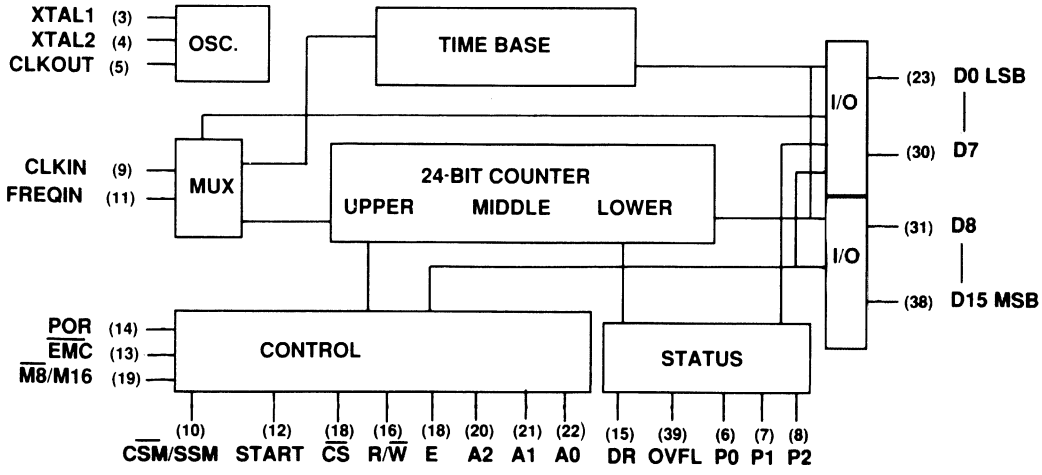
MD5024 24-Bit, 50MHz COUNTER/TIMER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +100°C
+5V Supply (V_{DD})	+4.75 to +5.25V

SPECIFICATIONS (T_A =0°C to +70°C, V_{DD} = +5V ± 5%, V_{SS} = 0V unless otherwise specified)

LOGIC LEVELS	MIN.	TYP.	MAX.	UNITS
Digital Inputs Logic "1"	+3.15			Volts
Logic "0"			0.8	Volts
Digital Outputs Logic "1"	+3.9			Volts
Logic "0"			+0.4	Volts
M8/M16 Data Bus Output		CMOS Levels		
CSM/SSM Mode Input		CMOS Levels		
P_0, P_1, P_2 User-Defined Inputs		CMOS Levels		
TIMING				
EMC Pulse Width (⌐‾⌐)	50			nsec
Start Trigger (⌐‾⌐)	10			nsec
FREQIN Frequency Input (⌐‾⌐)		10	50	MHz
CLKIN Clock Input (⌐‾⌐)		10	50	MHz
CS Chip Select Setup Time	10			nsec
R/W Read Cycle Time	50			nsec
Write Cycle Time			50	nsec
A_0, A_1, A_2 Byte Select Setup Time	10			nsec
Enable Setup Time	10			nsec
Hold Time	10			nsec
D_7 - D_0 (Write) Program Code Setup Time	10			nsec
Program Code Hold Time	10			nsec
D_{15} - D_0 (Read) Data Out Delay Time	30			nsec
Date Out Hold Time	25			nsec
Enable Setup Time	10			nsec
Hold Time	10			nsec
DR Data Ready	4			Clock Cycles
OVFLW Counter Overflow	1		1	Clock Cycle
POWER SUPPLY REQUIREMENTS				
V_{DD} +5V Supply	+4.75		+5.25	Volts
Power Dissipation (V_{DD} = +5.25V; 50MHz Clock)			700	mW



MD5024 Block Diagram

MD5024 DESCRIPTION

CHOOSING A CLOCK SOURCE — The MD5024 requires a clock to operate as a counter/timer. The clock can be provided by an external source such as a system clock or may be generated using a crystal oscillator circuit. Crystal drive circuitry is provided in the MD5024. The crystal should be connected across XTAL1 and XTAL2 with R and C as shown in Figure 1. The output of this block (CLKOUT) should be connected to the clock input (CLKIN). If a system clock is used, the oscillator block connections should be left open and the system clock should be connected directly to CLKIN.

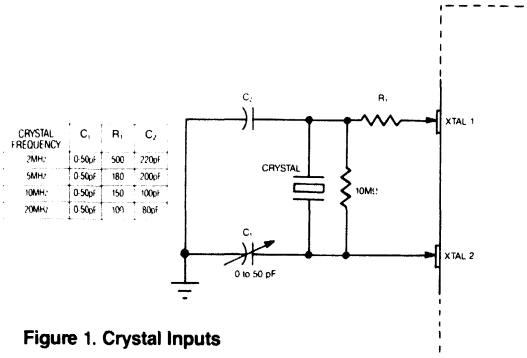


Figure 1. Crystal Inputs

RESET SIGNALS — POR — Power on Reset — provides a full reset of the MD5024 on power-up. To utilize this function connect a resistor and capacitor to pin 14 as shown in Figure 2. If not used, connect pin 14 to ground. Increasing R will provide a longer reset time. R should not exceed 15kΩ.

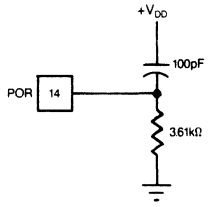


Figure 2. Power-On Reset Circuit

$\overline{\text{EMC}}$ — External Master Clear — a negative pulse stops all operations and resets all counters and latches to zero.

STATIC CONTROL LINES — M8/$\overline{\text{M16}}$ — Sets the MD5024 to communicate with an 8- or 16-bit bus. A low level selects an 8 bit path.

$\overline{\text{CSM}}$/SSM — The MD5024 can operate in a continuous mode or a triggered mode. When $\overline{\text{CSM}}$/SSM is high, the MD5024 completes a cycle and waits for a START command, a positive edge, before beginning a new cycle.

START COMMAND — After reset, one START pulse is necessary to begin the counter/timer cycle. In the continuous start mode ($\overline{\text{CSM}}$), the MD5024, thereafter, operates continuously, clearing its registers and resetting its timer at the end of each cycle and automatically beginning a new cycle. In the synchronous start mode (SSM), the MD5024 completes its cycle and awaits a new START pulse before beginning the next cycle. The MD5024 is triggered on the positive edge of the START pulse.

INPUT MULTIPLEXER — The input multiplexer accept the clock input (CLKIN) from an external source or from the crystal oscillator drive circuit; and from the input signal frequency (FREQIN); and sends them to the TIME BASE BLOCK or the COUNTER BLOCK depending on the MODE set by the microprocessor. This allows the MD5024 to shift from frequency counting to period measurement under microprocessor control.

READ/WRITE CONTROL LINES

$\overline{\text{CS}}$ — Chip Select — Selects this device to communicate with the bus when $\overline{\text{CS}}$ is active low.

R/$\overline{\text{W}}$ — Read/Write — Controls the direction of communication on the data bus. A high signal allows the processor to read information from the MD5024; a low signal allows the processor to write information to the MD5024.

E — Enable — Is the strobe for issuing the commands and instructions to the MD5024.

A2, A1, A0 — Address Bits — For selecting which of five possible 8 bit data bytes or three possible 16 bit data words are being read. (see Figure 7.)

$\overline{\text{CS}}$, R/$\overline{\text{W}}$, A0, A1, A2 — Timing relationships between these signals and Enable are shown in Figures 3 and 4.

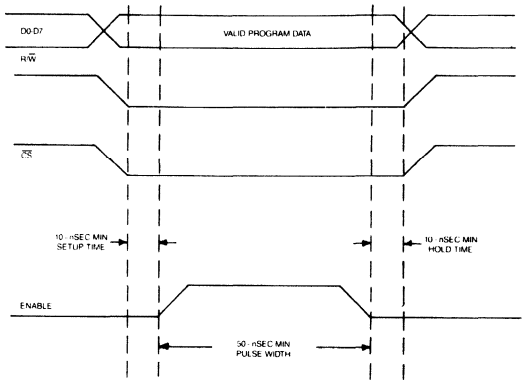


Figure 3. WRITE Command Timing

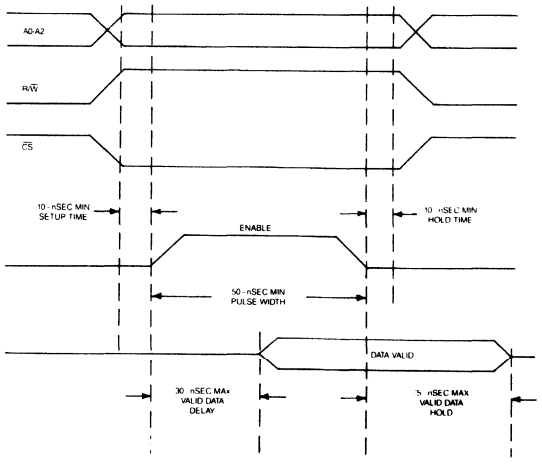


Figure 4. READ Command Timing

STATUS BLOCK — DR — Data Ready — Provides a logical "1" that indicates that data has been latched and is ready to be read. On POR or $\overline{EMC}$, DR becomes high and remains high until either, (1) a READ operation is performed, or (2) the time base interval is completed. On initiation of the READ operation, DR goes low and remains low until 4 clock cycles after the TIME BASE ends. If there is no READ operation, DR goes low at the end of the TIME BASE interval, and returns high 4 clock cycles after the TIME BASE interval is complete (see Figure 5).

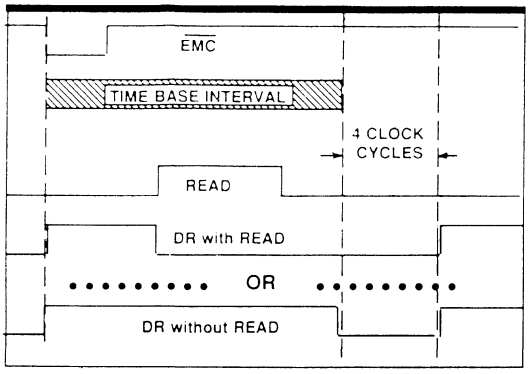


Figure 5. DATA RESET (DR) Timing

OVFL — Overflow — A high on this pin indicates the 24 bit counter has overflowed. The counter will roll over and continue to count. The OVFL signal is a pulse that will remain high for one period of the signal at FREQIN.

P0, P1, P2, — These are user defined status signals that may be read onto the bus via the MD5024. Whatever data is connected to these inputs appears on the data bus when reading the STATUS BYTE.

MD5024 WRITE OPERATION

FREQUENCY COUNTING — In the frequency counting mode, the counter counts the input pulses ove the time base (TB) programmed into the MD5024. TB is related to the clock frequency (CLKIN) by the following formula:

$$\underset{\text{(in sec)}}{TB} \times \underset{\text{(in Hz)}}{CLKIN} = B \times 10^{N}$$

PROGRAM BYTE Code

1. Choose the MSB as 0 for frequency counting.
2. Decide on the desired time base interval. Multiply the TIME BASE (in seconds) by the clock frequency (in Hz) and arrange in the form

$$B \times 10^{N}$$

3. From Table 1 determine the codes for B and N.
4. Compile the PROGRAM BYTE code from Table 1.

EXAMPLE — To count the input frequency for 100 msec, using a Clock of 10MHz:

1. Choose MSB = 0 for frequency counting
2. TB = 100 x 10^{-3} (100 msec)
   CLKIN = 10 x 10^{6} (10MHz)
   TB x CLKIN = 100 x 10^{-3} x 10 x 10^{6} = 10 x 10^{5}
3. B = 10 = 0110 and N = 5 = 101
4. The PROGRAM BYTE code from Table 1 is:

	MSB	N	B
Code	0	101	0110

D7		D6	D5	D4		D3	D2	D1	D0
MSB	N=	N2	N1	N0	B=	B3	B2	B1	B0
0/1	0	0	0	0	1	1	1	1	1
	1	0	0	1	2	1	1	1	0
	2	0	1	0	3	1	1	0	1
	3	0	1	1	4	1	1	0	0
	4	1	0	0	5	1	0	1	1
	5	1	0	1	6	1	0	1	0
	6	1	1	0	7	1	0	0	1
	7	1	1	1	8	1	0	0	0
					9	0	1	1	1
					10	0	1	1	0
					11	0	1	0	1
					12	0	1	0	0
					13	0	0	1	1
					14	0	0	1	0
					15	0	0	0	1
					16	0	0	0	0

Table 1 — PROGRAM BYTE Code

WRITING THE PROGRAM BYTE

The PROGRAM BYTE is written into the MD5024 by:

A. Set the Read/Write (R/$\overline{W}$) to a logical "0" state.
B. Load the code from Table 1 onto lines D7-D0.
C. Set the Chip Select line ($\overline{CS}$) to a logical "0" state. The order in which these signals are applied isn't important, as long as they conform to the timing constraints relating to Enable (E) shown in Figure 3.
D. Activate the Enable (E) line. The Enable line performs the actual read operation. It is a positive pulse, at least 50 nsec wide.

PERIOD MEASUREMENT

In the period measurement mode, the multiplexer automatically applies the clock to the counter and uses the period of the input (FREQIN) to gate the clock. The number of clock pulses accumulated is directly proportional to the period of the input. The MD5024 can be programmed to accumulate clock pulses for one to 16 x 10^{7} input periods, allowing for period averaging measurement.

PROGRAM BYTE Code

1. Choose the MSB as 1 for period measurement.
2. Decide on the desired number of periods to be counted and represent the number in the form

$$B \times 10^{N}$$

3. From Table 1 determine the codes for B and N.
4. Compile the PROGRAM BYTE code from Table 1.

EXAMPLE — To count 100 periods of the input (FREQIN):

1. Choose the MSB as 1 for period measurement:
2. For 100 periods:
   B x 10^{N} = 10 x 10^{1}
3. From Table 1 the codes for B and N are:
   B = 0 1 1 0
   N = 0 0 1
4. The PROGRAM BYTE code from Table 1 is:

	MSB	N	B
Code	1	001	0110

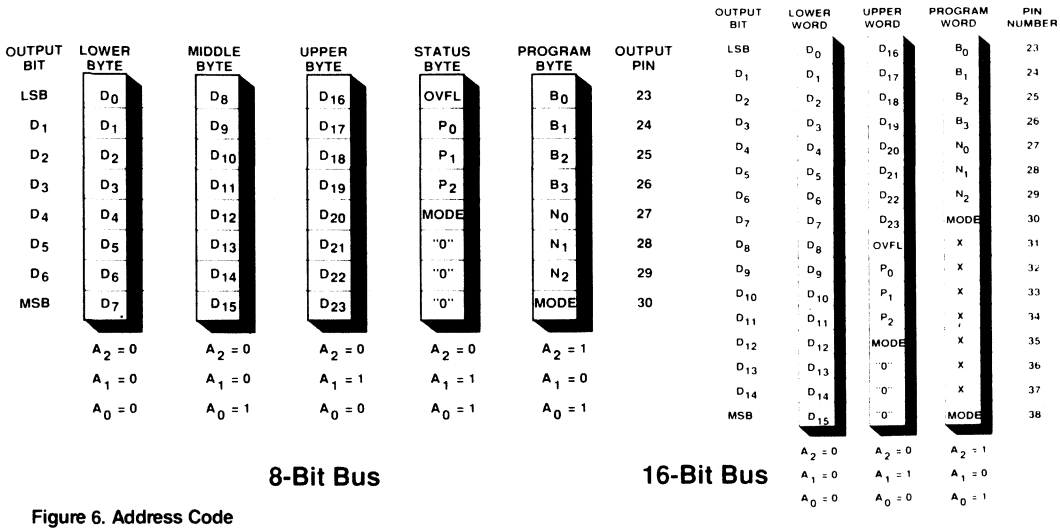


Figure 6. Address Code

MD5024 READ OPERATION

DATA OUTPUT — The information read from the MD5024 contains:

- data from the counter;
- user defined parameters - P0, P1, and P2;
- and program information

conveniently arranged in byte format. The information is read individually as bytes onto an 8 bit bus or, in pairs as words onto a 16 bit bus.

DATA BYTES — The MD5024 is capable of counting up to 24 bits. The data from the counters is contained in three bytes as shown in Figure 6.

STATUS BYTE — The STATUS BYTE keeps track of information related to the data from the counter; and loads the user defined signals, P0, P1, and P2 onto the data bus.

If the the 24 bit counter has overflowed, the overflow bit (LSB of the STATUS BYTE) will be high.

NOTE that the counter will roll over and continue to count. Thus, it is important to monitor the overflow bit if the counter has any chance of overflowing to be sure the data is valid.

Bits P0, P1, and P2 - the user defined inputs - can be conveniently read on the STATUS BYTE. They may contain information identifying the source of the data, as in a multiplexed data acquisition system, or the setting of a PGA, if one is used.

Bit 4 of the STATUS BYTE is the mode bit that tells the processor whether the data information was acquired in the frequency count or period measurement mode and thus defines the nature of the data.

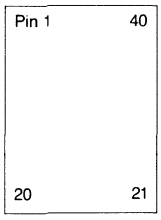
Bits 5, 6, and 7 are unused and set to logic 0.

PROGRAM BYTE — The PROGRAM BYTE carries the time based information associated with the data. The program code is defined in Table 1. The seventh bit of the PROGRAM BYTE contains the mode bit, defining the method of data acquisition — frequency counting or period measurement.

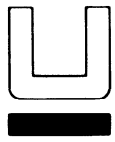
READING THE DATA — To READ data from the MD5024

A. Set the R/$\overline{W}$ line in the logical "1" (high) state.
B. Set the A2, A1, and A0 control lines to the appropriate states for the byte or word to be read per Figure 6.
C. Set the Chip Select line ($\overline{CS}$) to a logical "0". The order in which these signals are applied is not important, as long as they conform to the timing constraints relating to the Enable (E) line shown in Figure 4.
D. Activate the Enable (E) line. The Enable line performs the actual read operation. It is a positive pulse, at least 50 nsec wide. Valid data is present on the output bus 30 nsec maximum after the leading edge of Enable; the data bus returns to a high impedance state 25 nsec maximum after the trailing edge of the enable pulse.

PIN DESIGNATIONS



1 Ground
2 Ground
3 XTAL 1
4 XTAL 2
4 CLKOUT
6 P0
7 P1
8 P2
9 CLKIN
10 CSM/SSM
11 FREQIN
12 START
13 EMC
14 POR
15 DR
16 R/W
17 E
18 CS
19 M8/16
20 A2
40 +5V Supply
39 OVFL
38 D15 (MSB)
37 D14
36 D13
35 D12
34 D11
33 D10
32 D9
31 D8
30 D7
29 D6
28 D5
27 D4
26 D3
25 D2
24 D1
23 D0 (LSB)
22 A0
21 A1



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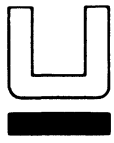
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