

INTEGRIDAD DE SEÑAL

Fundamentos y Metodologías: tiempo y frecuencia



Héctor Carreño

Application Engineer

hector_carreno@agilent.com

Need help?

contactcenter_spain@agilent.com

91 631 3300

AGENDA



Unlocking Measurement Insights for 75 Years

- Introduction / Signal Integrity Definition
- Evolution of Test Parameters
- Traditional TDR/TDT instrument
- Vector Network Analyzer Basis
- Single Ended / Differential Topologies
- Physical Layer Test System (PLTS Software)



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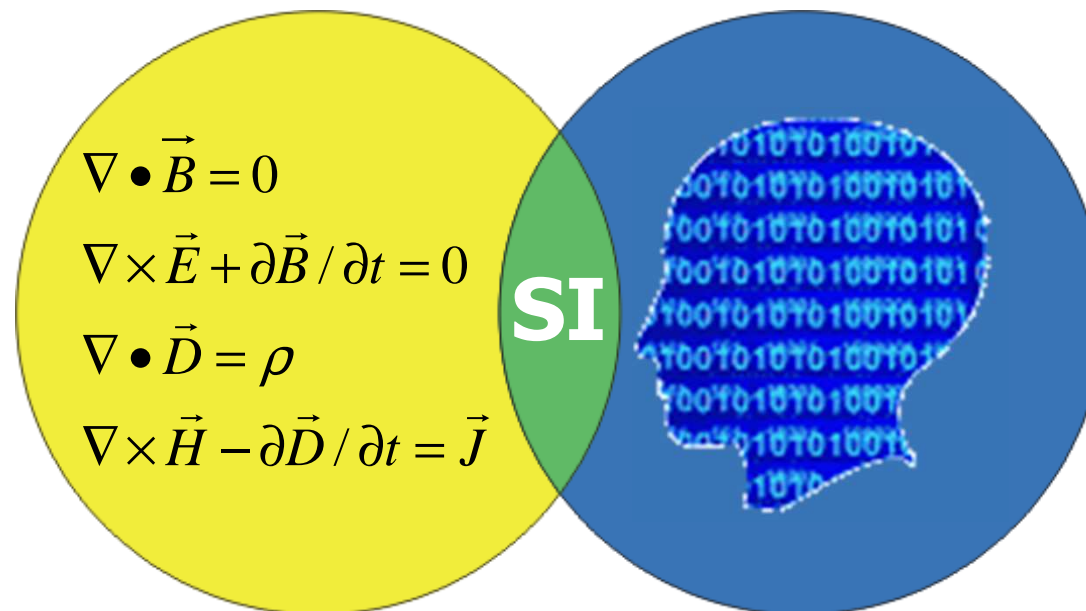


Unlocking Measurement Insights for 75 Years

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What is Signal Integrity ?

➤ from Marketing's Viewpoint



Mr. Maxwell meet Mr. Boole and Mr. Moore !

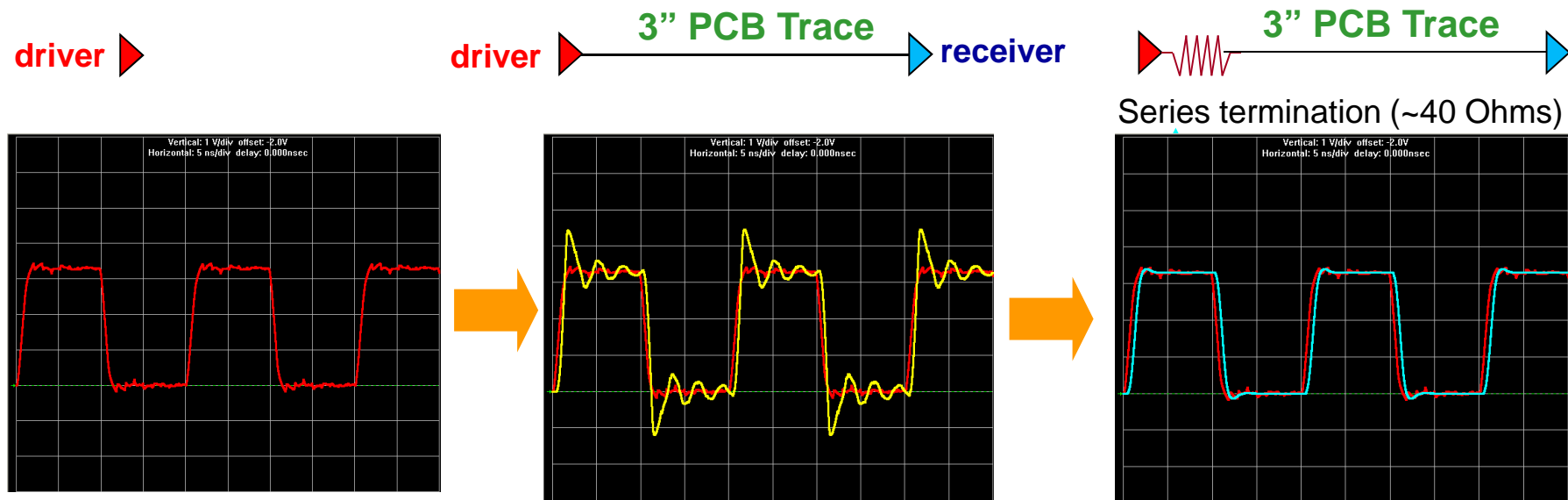


What is Signal Integrity ?



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➤ from Engineer's Viewpoint



Signal Integrity =

Where the electrical properties of the interconnects can cause significant distortions in digital signals.



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What is Signal Integrity ?



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➤ from http://en.wikipedia.org/wiki/Signal_integrity

Signal integrity or **SI** is a measure of the **quality of an electrical signal**. In digital electronics, a stream of binary values is represented by a voltage (or current) waveform.

Over short distances and at low bit rates, a simple conductor can transmit this with sufficient fidelity. However, at **high bit rates** and over **longer distances**, various effects can degrade the electrical signal to the point where errors occur, and the system or device fails.

Signal integrity engineering is the task of analyzing and mitigating these impairments. Signal integrity engineering is at all levels of electronics packaging, from internal connections of an IC through the package, the printed circuit board (PCB), the backplane, and inter-system connections.

Some of the main issues of concern for signal integrity are *ringing, crosstalk, ground bounce, distortion, signal loss, and power supply noise*.



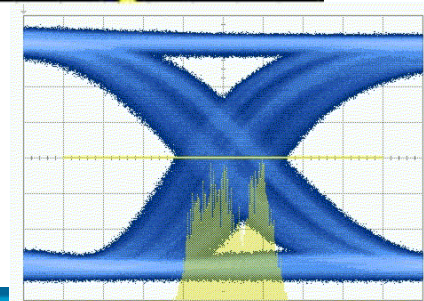
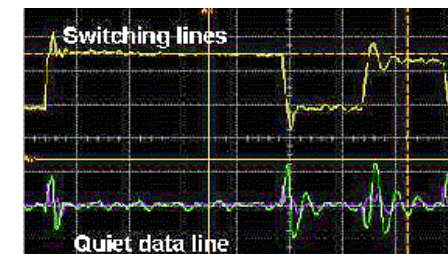
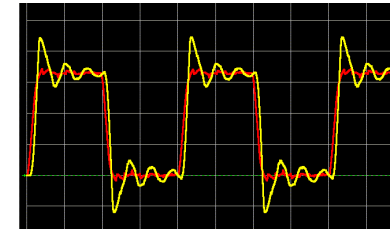
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4 SI problems and their cause



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1. **Poor signal quality of one net:** reflections and distortions from impedance discontinuities in the signal or return path. Manufacturing tolerances for PCB and packages. Line width changes, Vias, Serpentine, Connectors, Cables...
2. **Crosstalk between multiple nets:** electromagnetic coupling between signal lines. Trace-to-trace crosstalk, Via-to-Via coupling, Digital-to-RF coupling.
3. **Power/Ground Noise:** voltage drops across impedance in the power/ground network
4. **Jitter and EMI** from causes listed above and variety of other sources

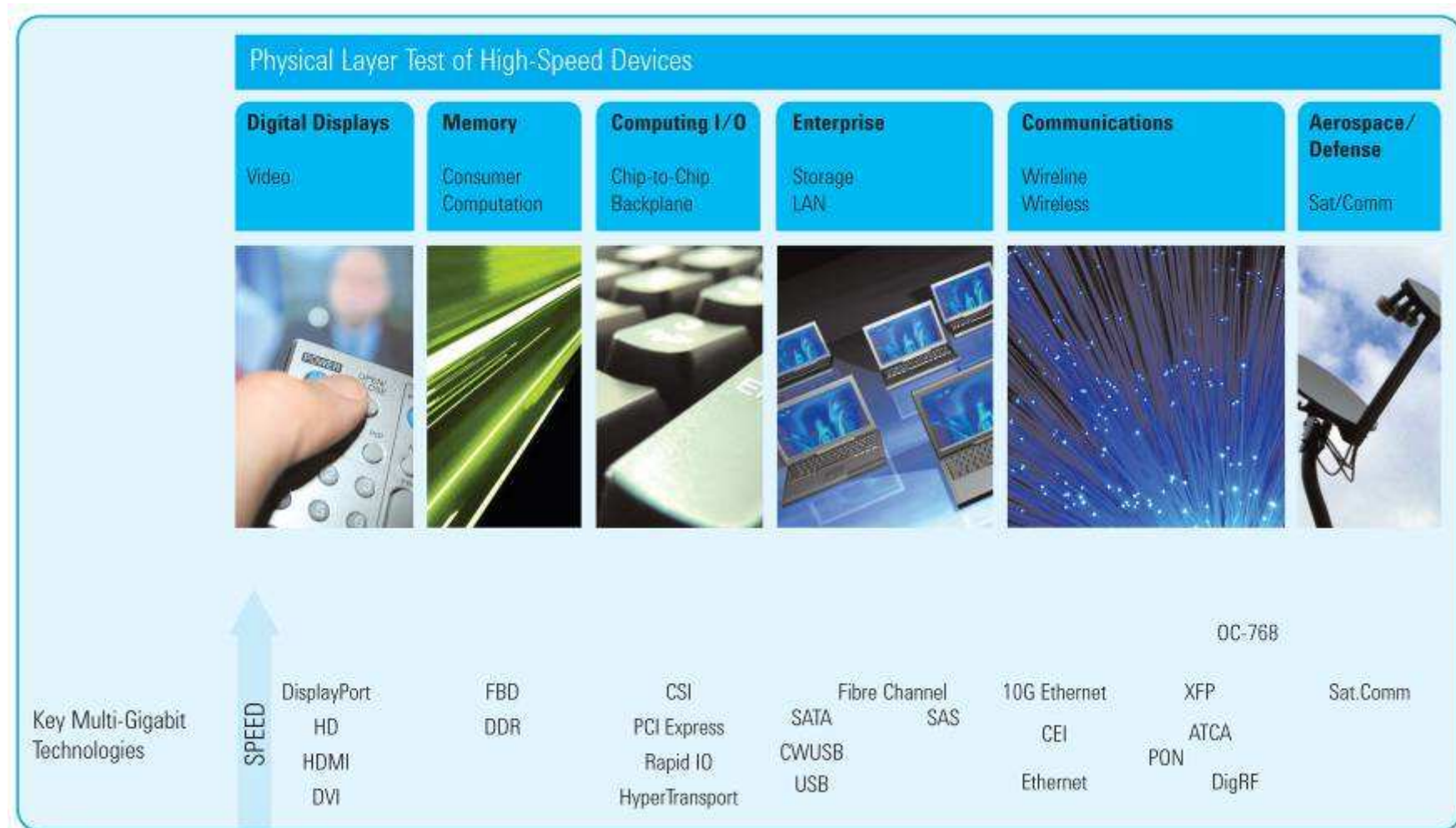


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Today High Speed I/O Standards



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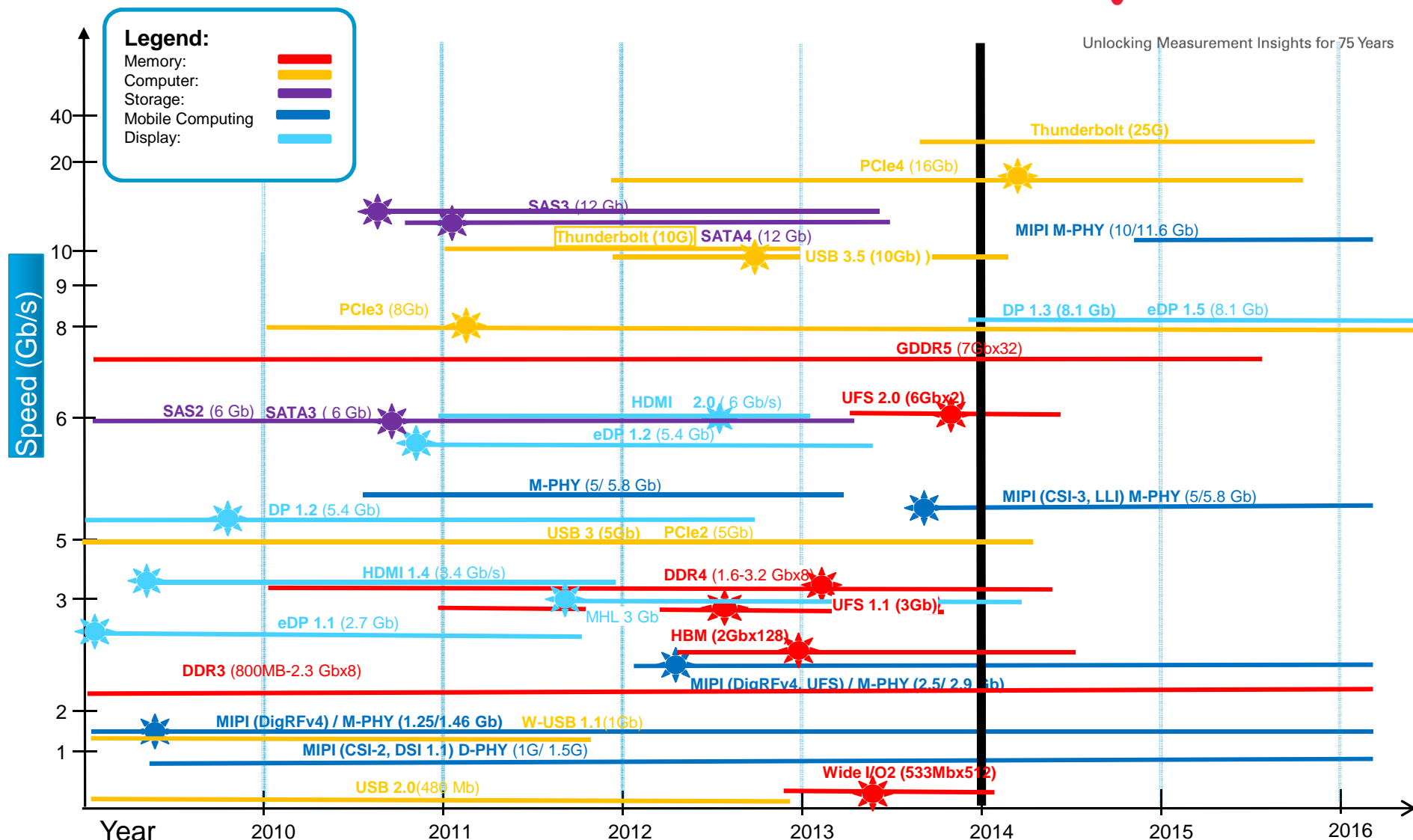


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Data Rates continuously increasing



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SI is becoming more important

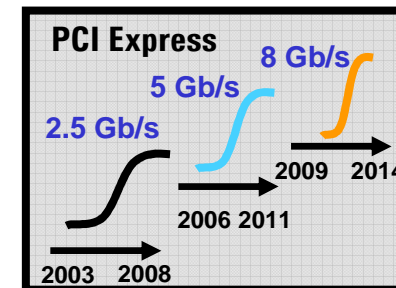
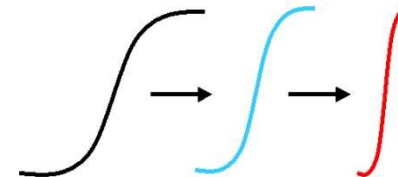


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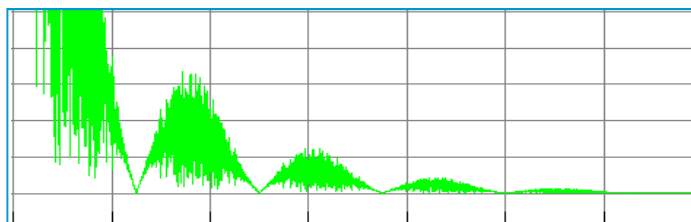
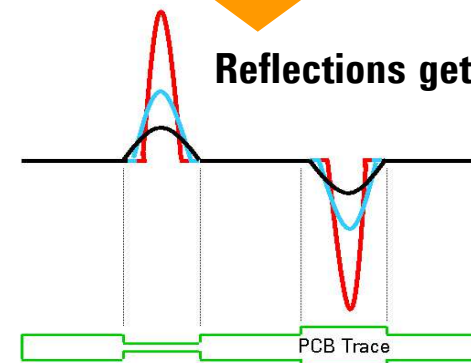
High Speed Digital Committees



Risetimes become faster



Reflections get larger



Frequency Domain data is ALSO required

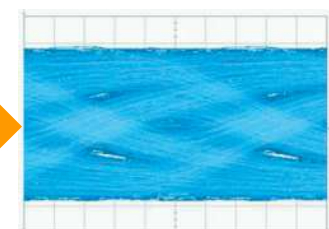
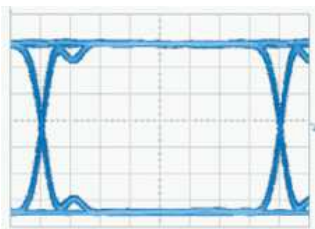
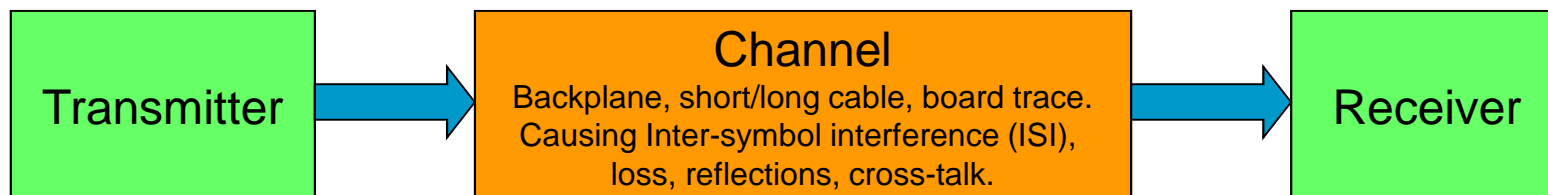
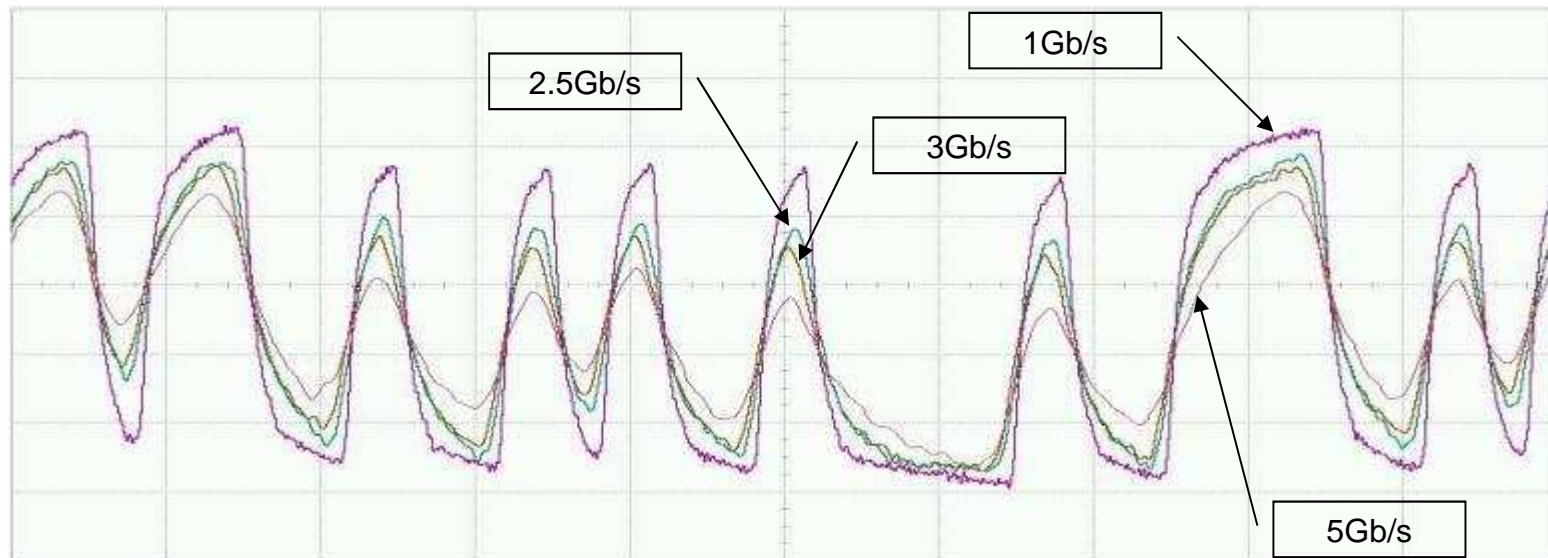


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What about using existing channels ?



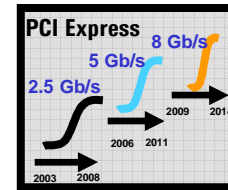
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Example: FR4 is showing its limitations

FR4 is common, low cost and easy to manufacture BUT it has problems:

- Reflections at high speeds
- Dispersion varies with frequency
- High Insertion Loss
- ISI induced Jitter
- Effects vary with temperature and humidity



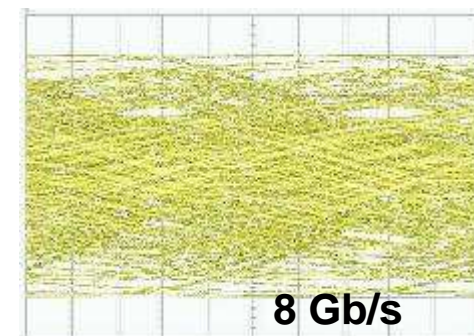
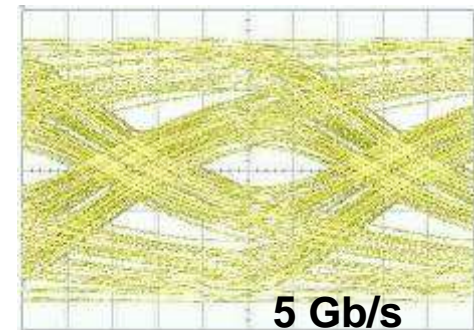
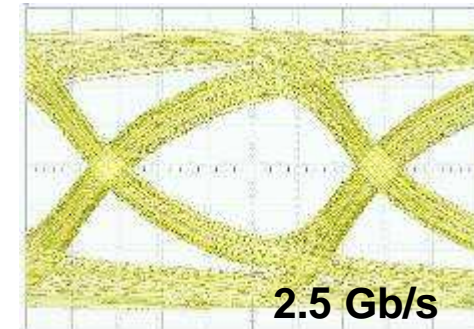
What Works
Today

Gets Worse
The Next
Time

No longer
usable



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Signal Integrity Challenge



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USB 3.0	4.8 Gb/s
HDMI	5 Gb/s
DVI	8 Gb/s
DP	8.6 Gb/s
PCIe	5 Gb/s
SATA	3 Gb/s
DDR3	0.8-2.133 Gb/s



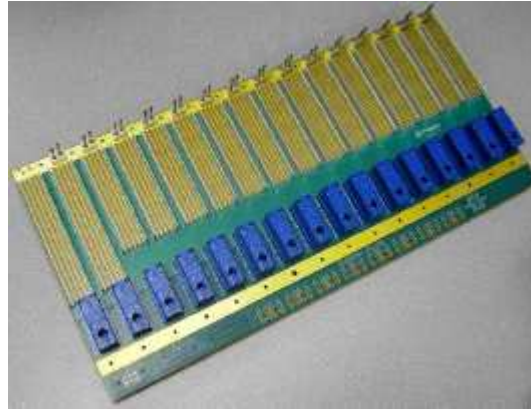
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Signal Integrity problems everywhere !



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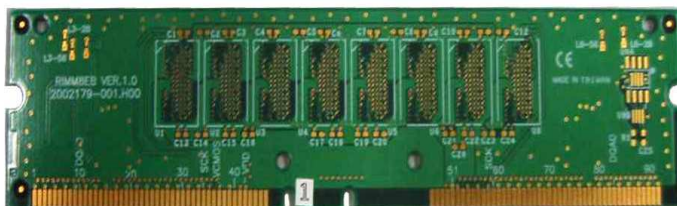
Backplanes



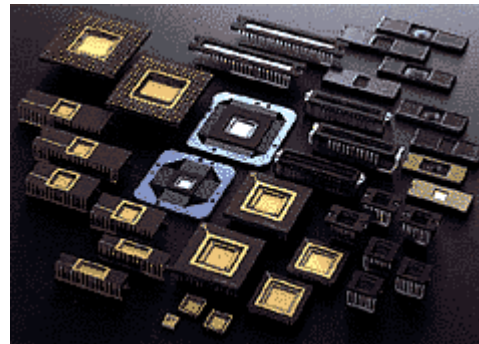
Connectors



PC Boards



IC Packages



Cables



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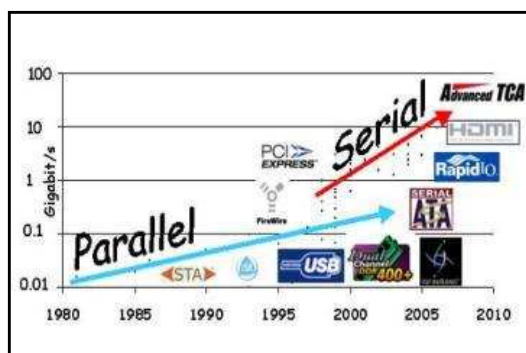
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Trends in Compliance Test



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With the increase in bit rates, standards continue to evolve and new measurements are often the result. There is a growing need in the industry for more thorough evaluation of components, as well as evaluation under actual operating conditions



	High-speed serial standards	Compliance Test Parameters
1990s	Gen 1 (~100s Mbps)	•time domain (impedance, delay, skew, ...)
2000~	Gen 2 (1~3 Gbps)	•time domain (impedance, delay, skew) •frequency domain (insertion loss, return loss, ...)
2007~	Gen 3 (~3 Gbps)	•time domain (impedance, delay, skew) •frequency domain (insertion loss, return loss, crosstalk, mode conversion, ...)
2010~	Next Gen (~6 Gbps)	•time domain (impedance, impedance in active state , delay, skew, eye diagram) •frequency domain (insertion loss, return loss, crosstalk, mode conversion, ...)



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Traditional Test



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Time Domain

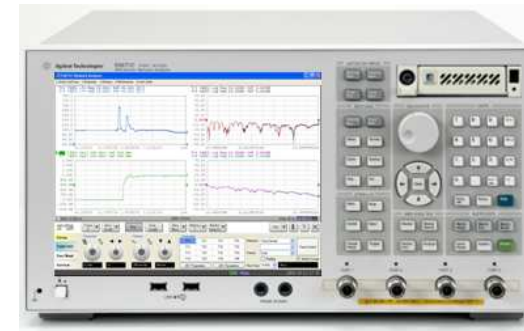
(impedance, delay, skew, eye diagram)

Frequency Domain

(return/insertion losses, xtalk, mode conv.)



Oscilloscopes / TDRs



Vector Network Analyzers

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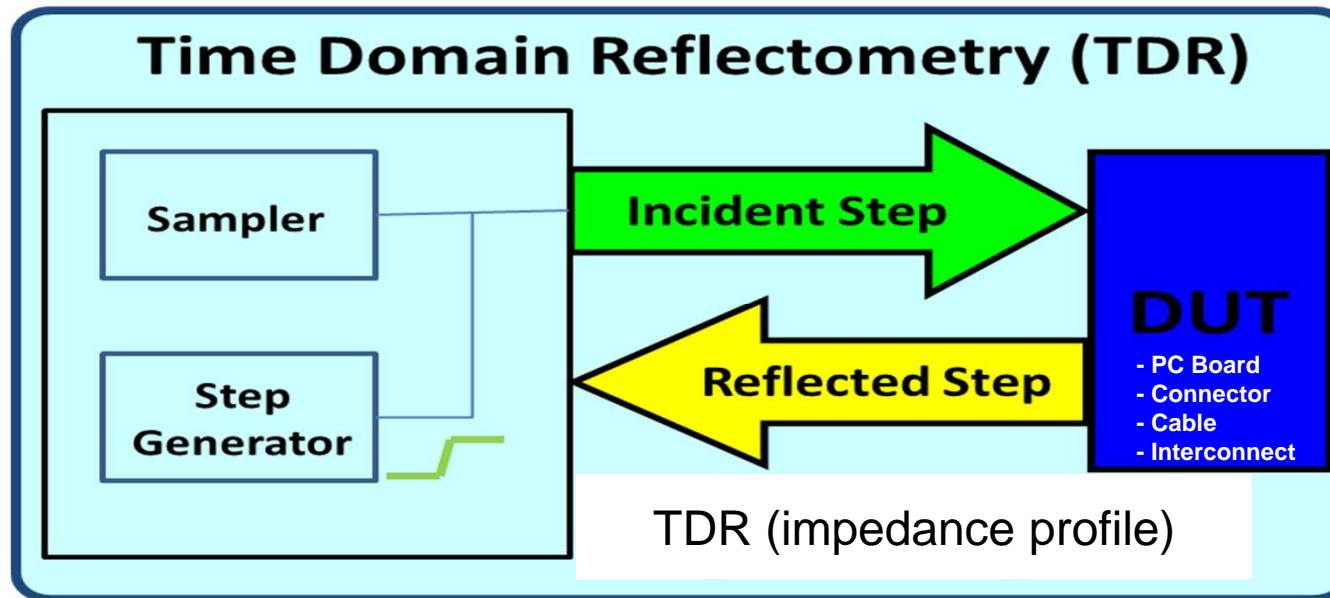


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Time Domain Reflectometry (TDR)



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Time Domain Reflectometry (TDR)

- Impedance measurements
- Locate the position and nature of each discontinuity
- Propagation/Time delay
- Excess Reactance (Capacitance or Inductance)
- Effective dielectric constant

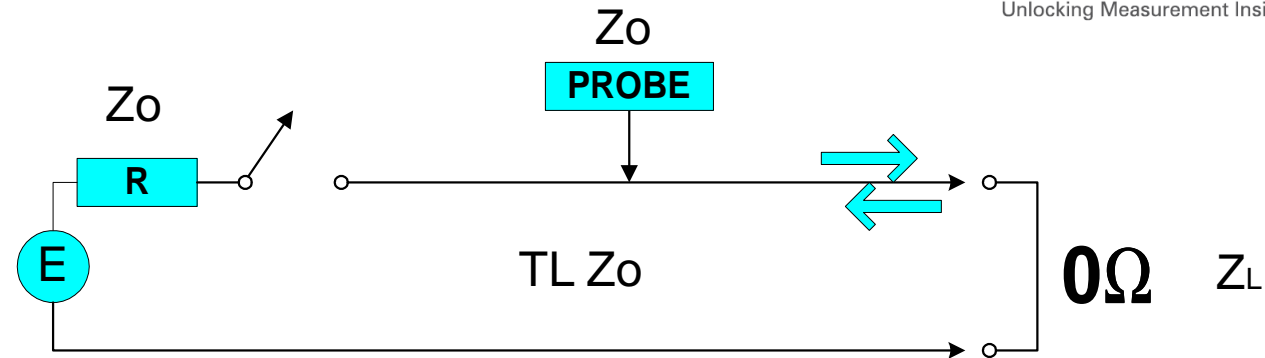


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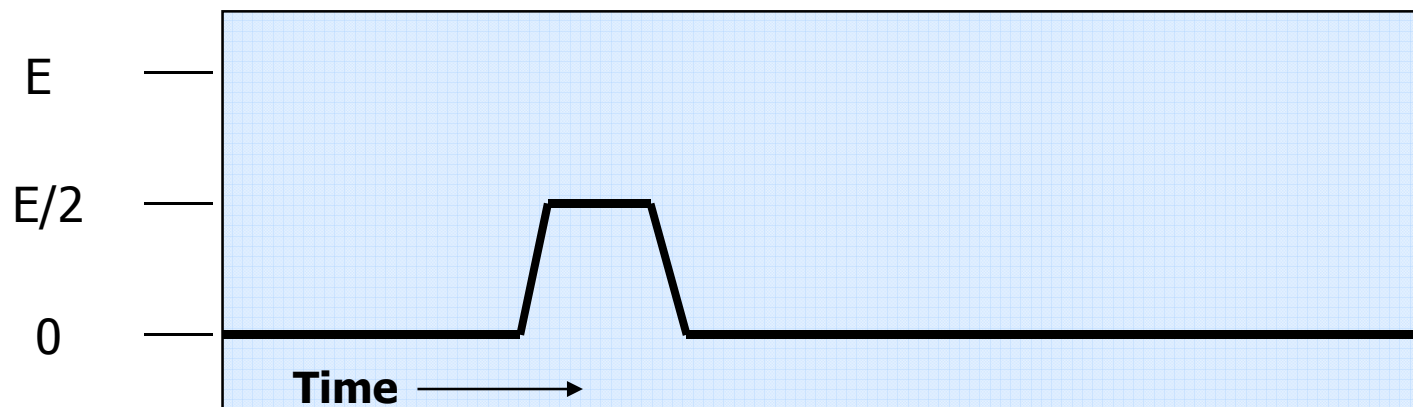
TDR - Short Termination



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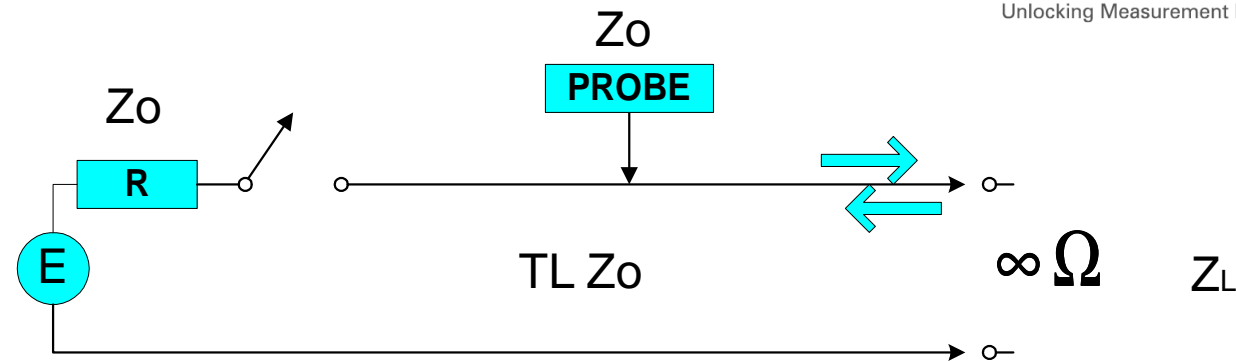
What do you expect to see at the probe before, during, and after you close the switch?



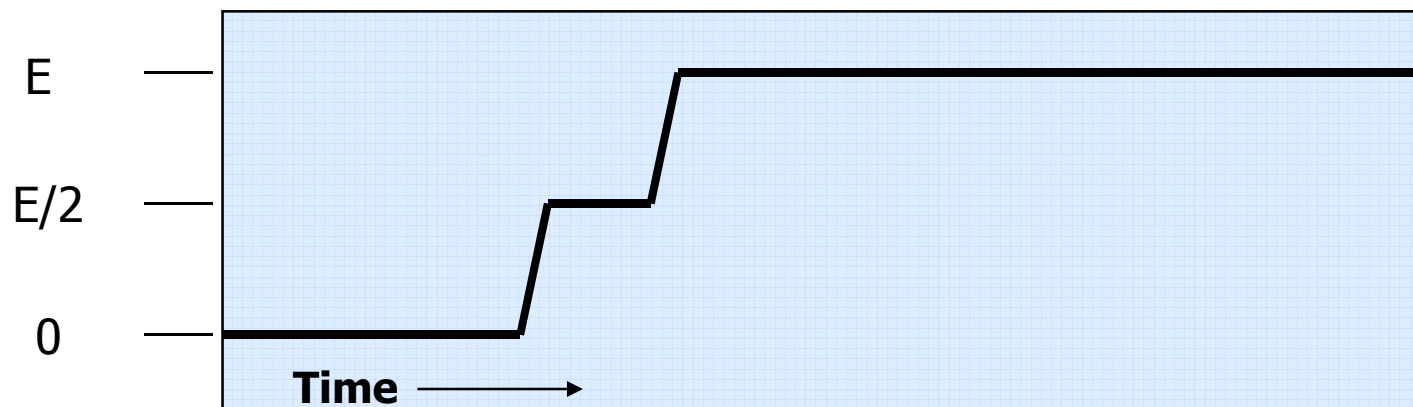
TDR - Open Termination



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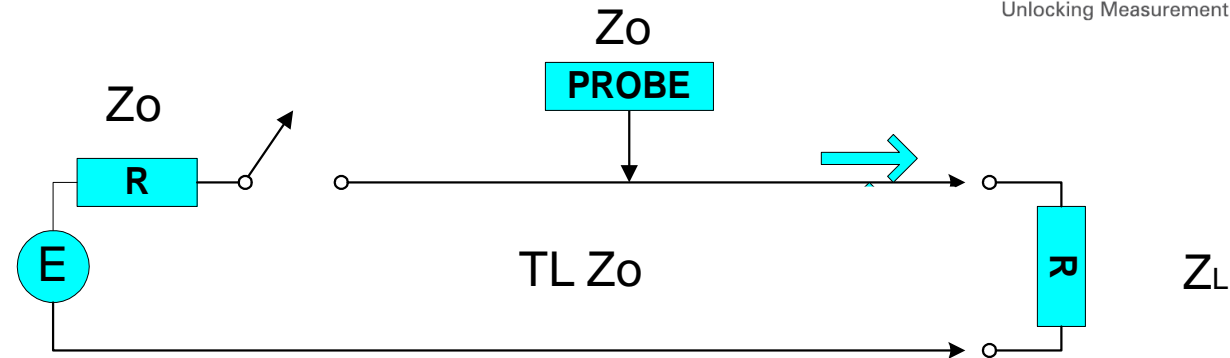
What do you expect to see at the probe before, during, and after you close the switch?



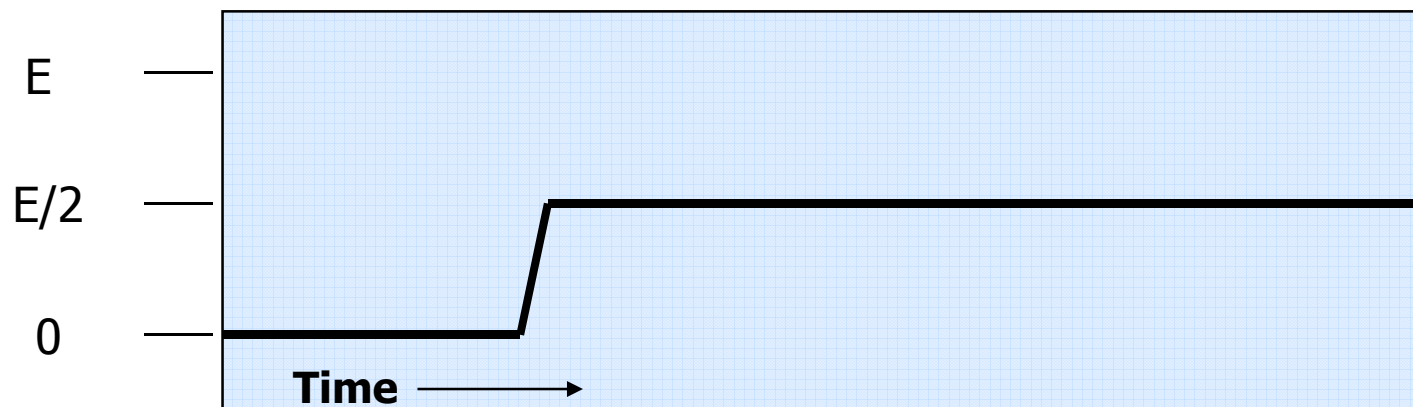
TDR - Perfect Termination



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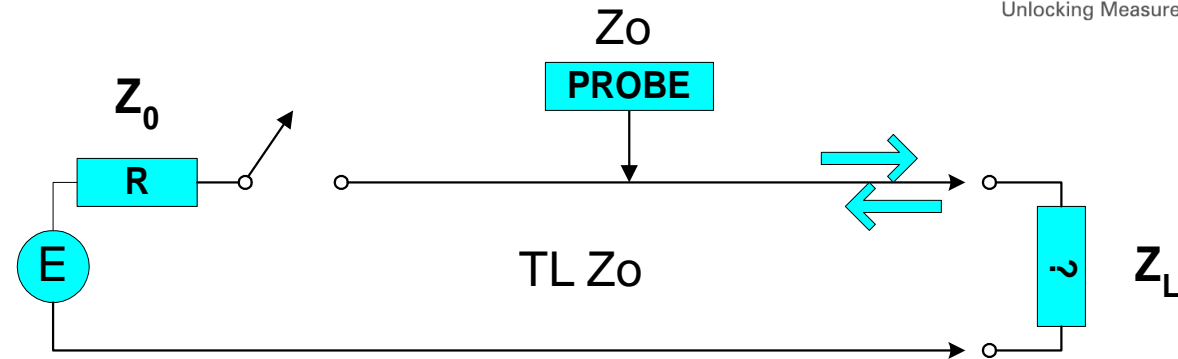
What do you expect to see at the probe before, during, and after you close the switch?



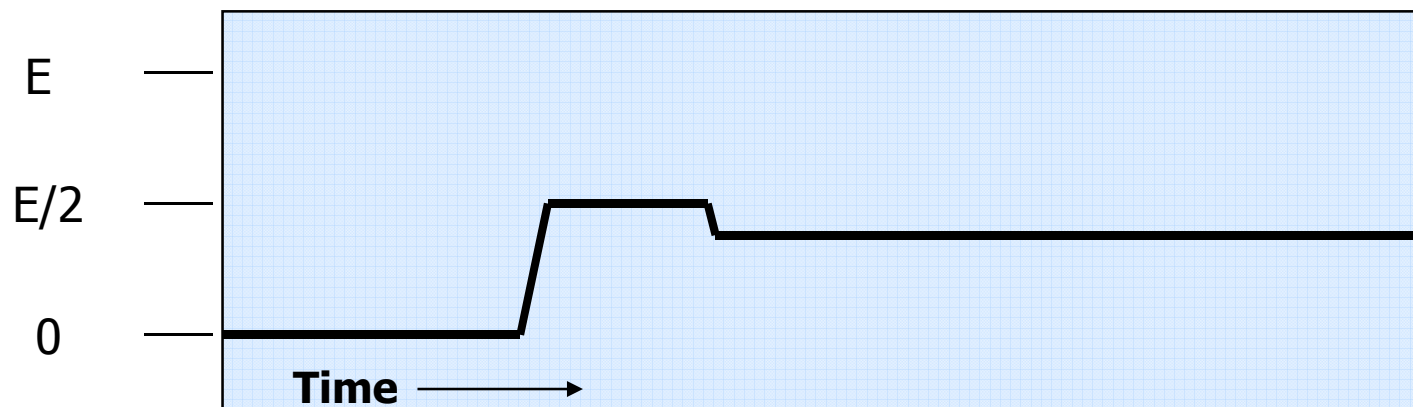
TDR - Unknown Termination



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Is the unknown resistor closer to a short (zero Ω) or an open ($\infty\ \Omega$)?



TDR - Impedance Mismatch Terms



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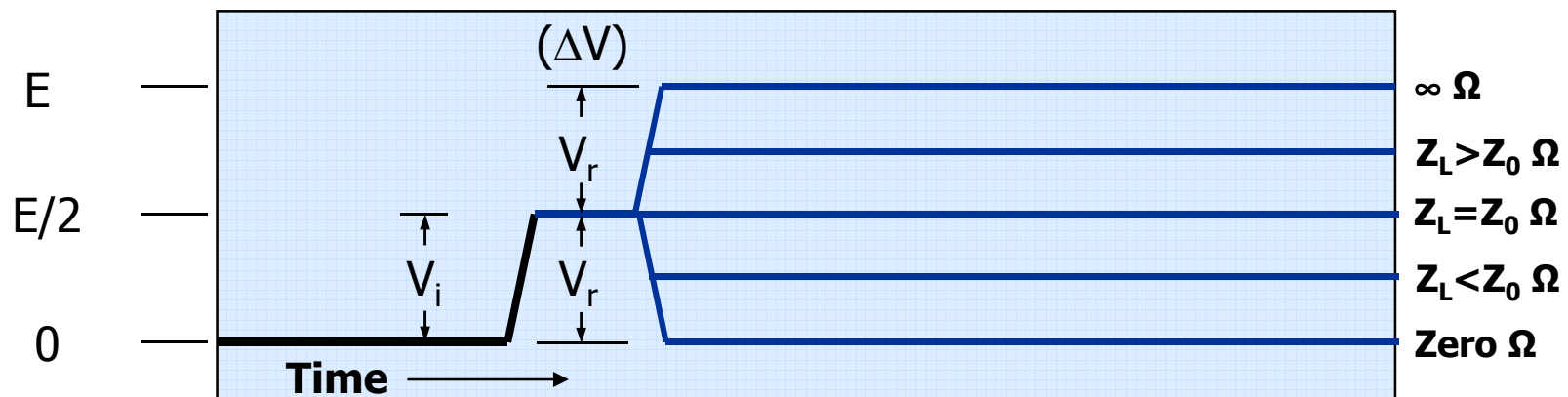
What is the value of Z_{load} ?

$$Z_L = Z_0 \frac{1 + \rho}{1 - \rho}$$

Impedance Calculated from
Source Impedance and
Reflection Coefficient.

$$\rho = \frac{V_r}{V_i}$$

Reflection Coefficient, rho:
How much was reflected?

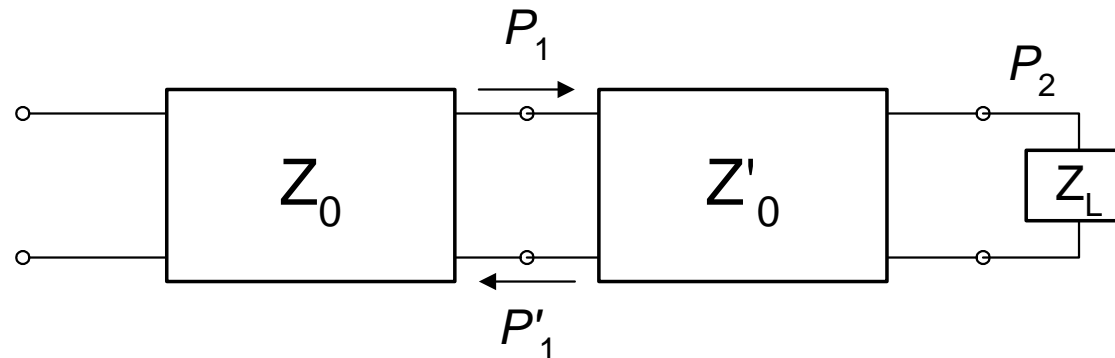


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TDR - Multiple Discontinuities

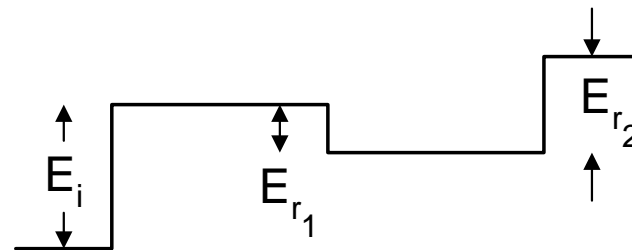


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$$P_1 = \frac{Z'_0 - Z_0}{Z'_0 + Z_0}$$

$$P_2 = \frac{Z_L - Z'_0}{Z_L + Z'_0}$$



**Accuracy decreases as you look further down
a line with multiple discontinuities**

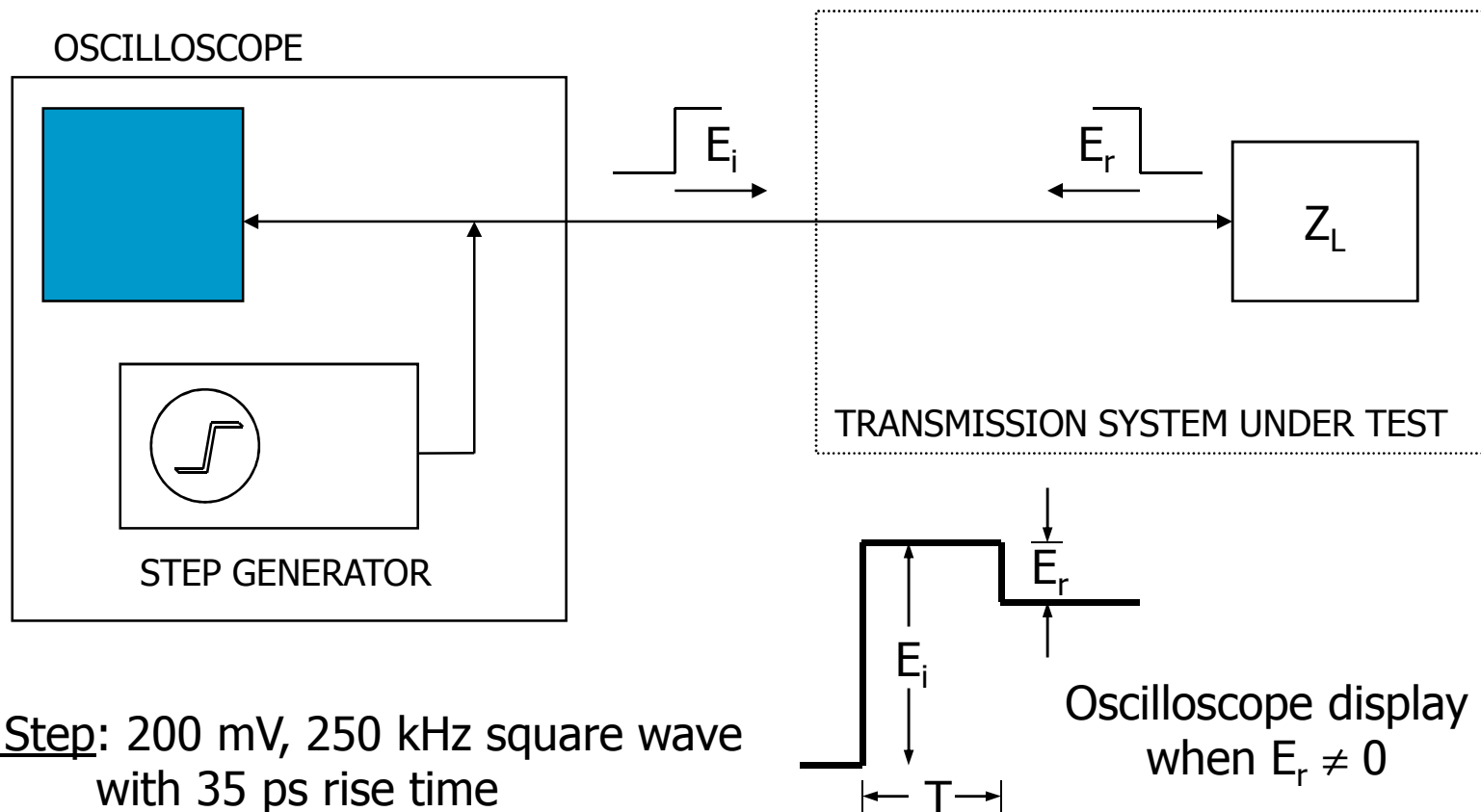


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TDR in the time domain



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Typical Step: 200 mV, 250 kHz square wave
with 35 ps rise time

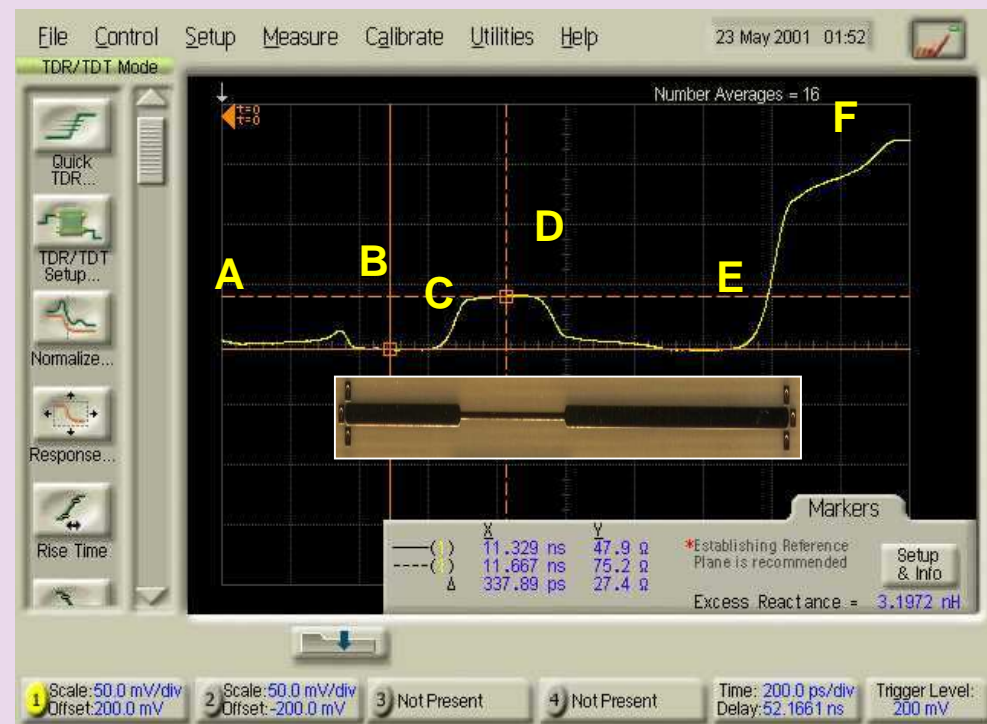
TDR measurement based on Scope



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Typical TDR result

- A: 50 Ohm cable
- B: Launch to microstrip
- C: 50 Ohm microstrip
- D: 75 Ohm microstrip
- E: 50 Ohm microstrip
- F: “open” circuit

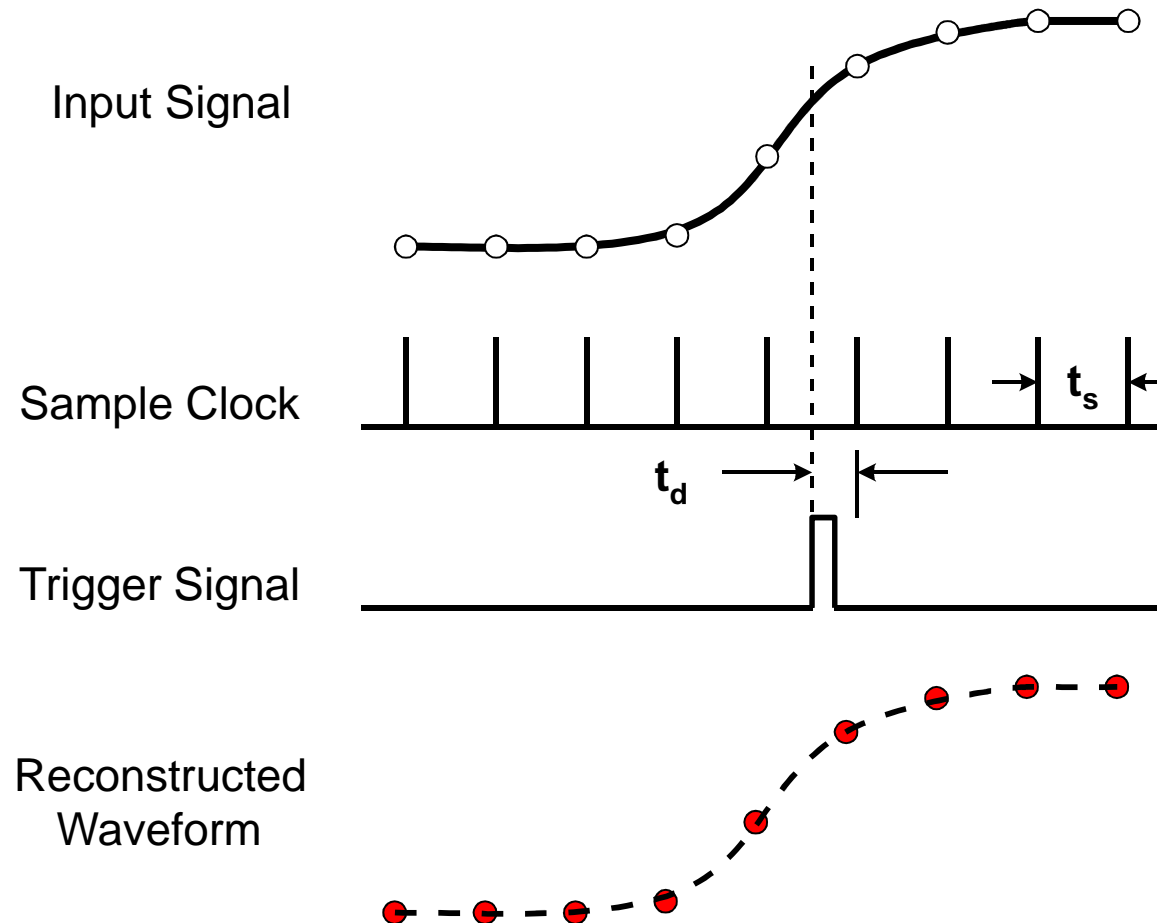


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Real-Time Oscilloscope



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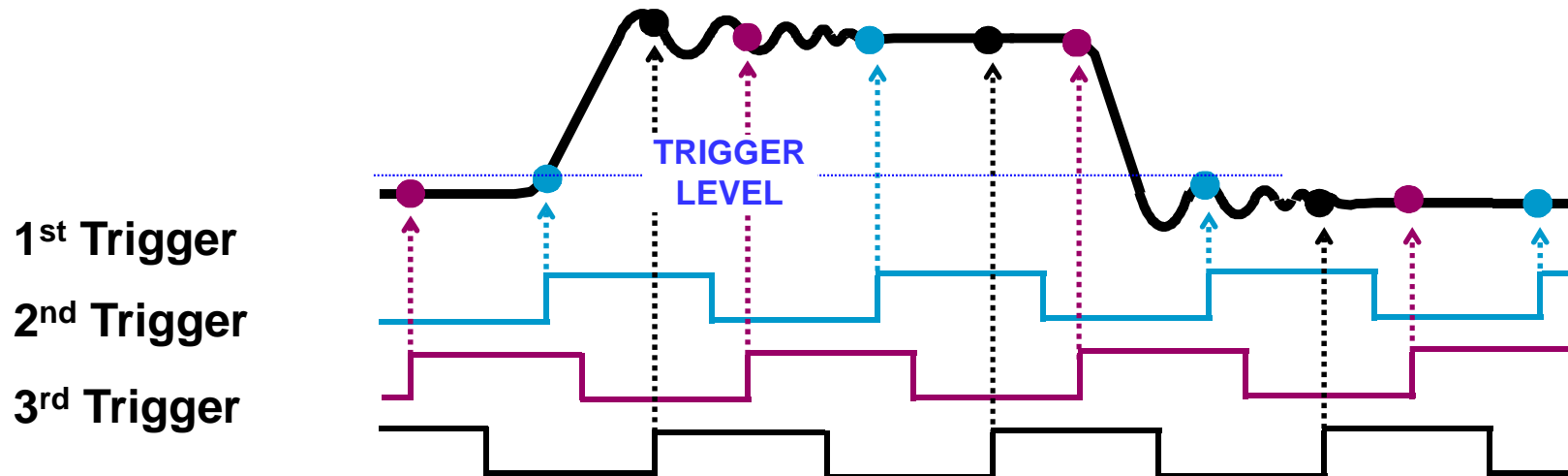
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Equivalent Time Oscilloscope



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- 1) Builds up the waveform over several sweeps
 - 2) samples part of the signal on the first sweep, then another part on the second sweep, and so on....
 - 3) Laces all information together to recreate the waveform
- Useful for high-frequency signals
 - Used ONLY with Repetitive Signals! No Glitches will be captured!
 - Sample Rate is Not a Major Factor

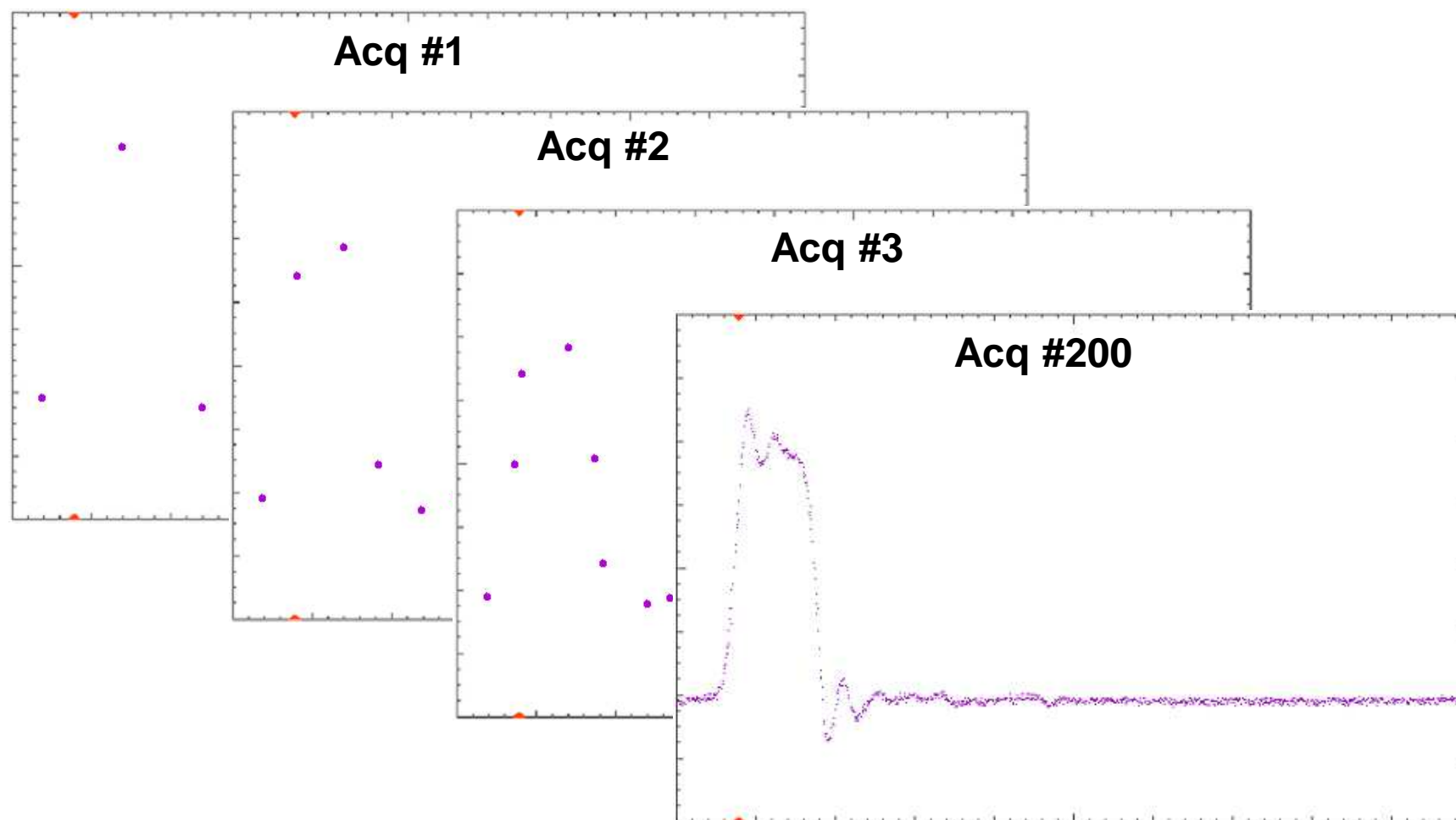


Equivalent Time (Repetitive) Technique



Build Up of Waveform over multiple sample events

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TDR – Spatial Resolution

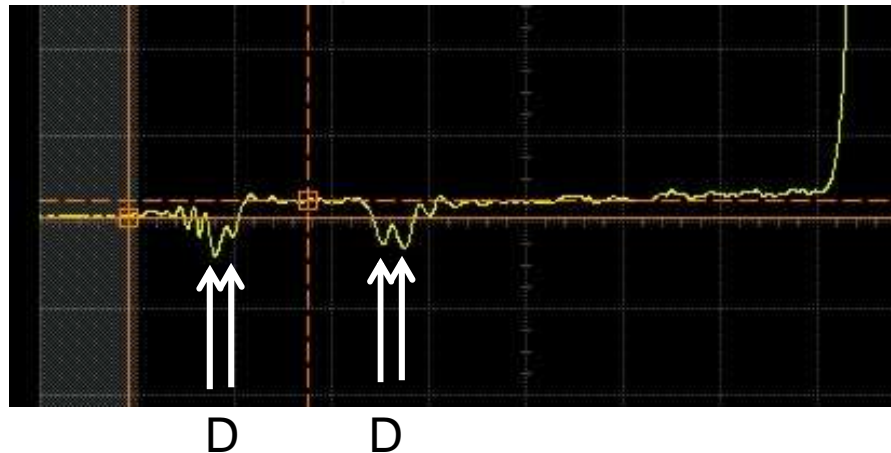


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TDR Resolution

The faster the edge, the closer two impedance discontinuities can be identified as separate events on the TDR trace.

$$D_{\min} = \frac{c \cdot t_{\text{rise}}}{2\sqrt{\epsilon}}$$



- $t_{r_{\text{system}}} = \sqrt{t_{r_{\text{step}}}^2 + t_{r_{\text{scope}}}^2}$
- ϵ = dielectric constant of the transmission system
- c = speed of light in a vacuum.

For $\epsilon = 4$ and system rise time of 8 ps, $D_{\min} < 1\text{mm}$.



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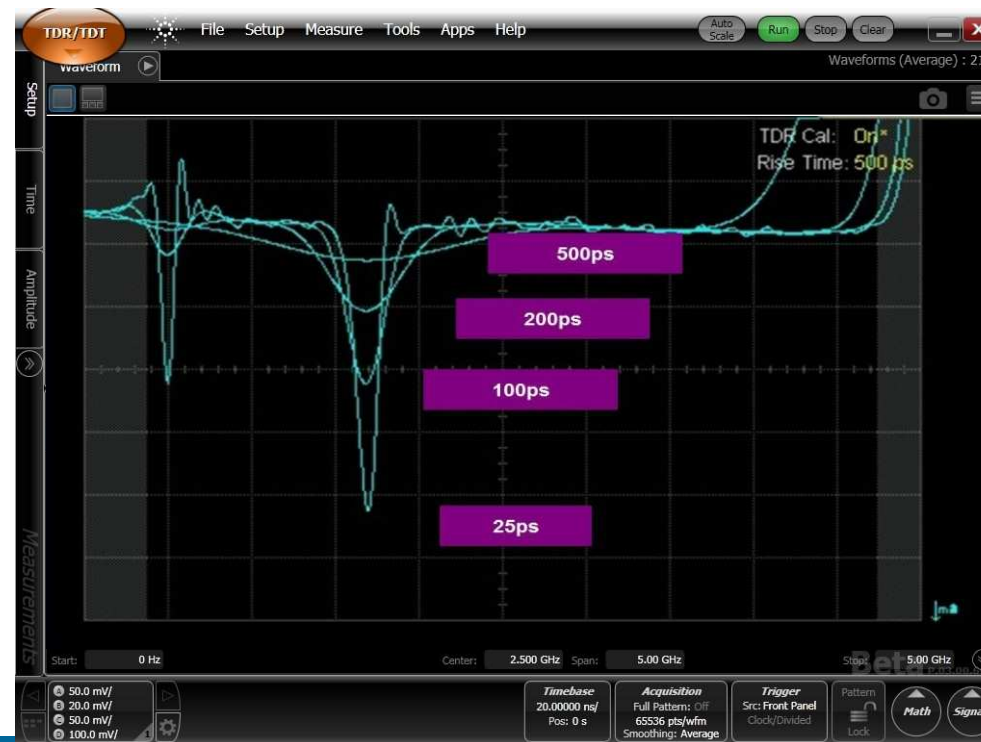
What TDR edge should I use?



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Select a solution based on your **application**:

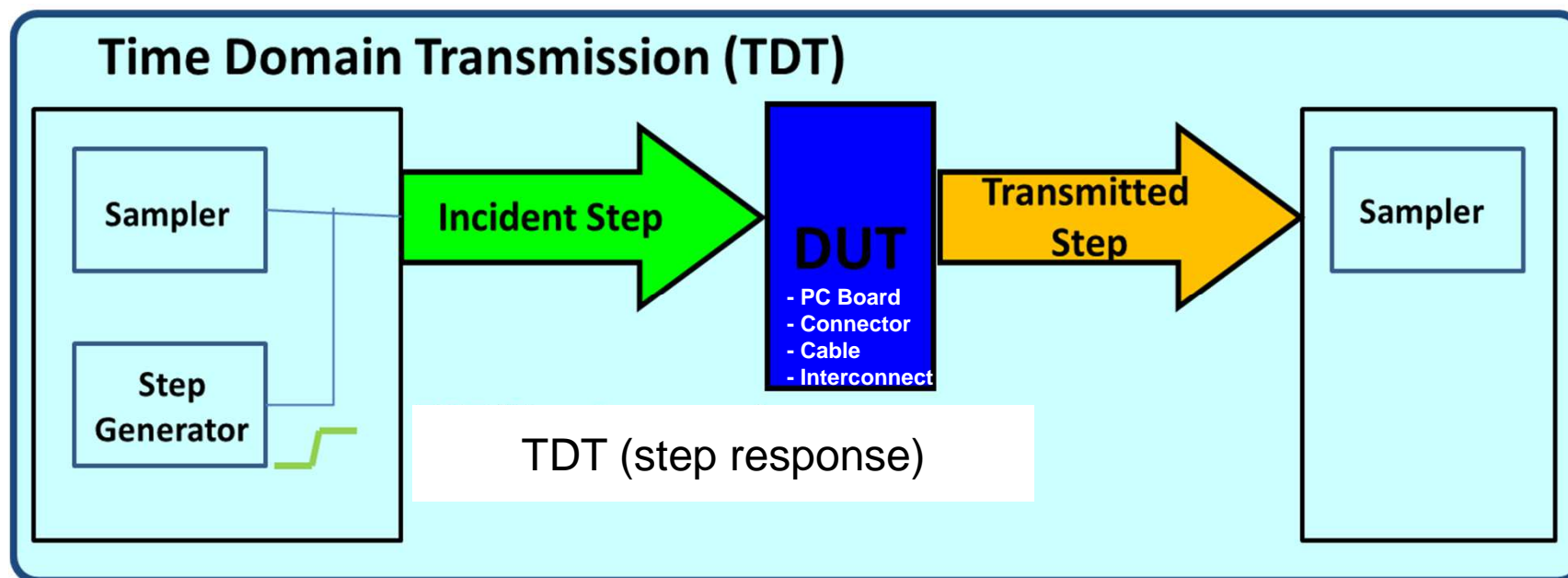
- **Too fast:** you'll see impedance discontinuities that will not affect the real signals in your design (you'll waste time fixing things that do not matter)
- **Too slow:** discontinuities are masked



Time Domain Transmission (TDT)



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Time Domain Transmission (TDT)

- Step Response
- Propagation/Time delay
- Propagation velocity
- Rise time degradation
- Near-end crosstalk (NEXT)
- Far-end crosstalk (FEXT)
- Skew



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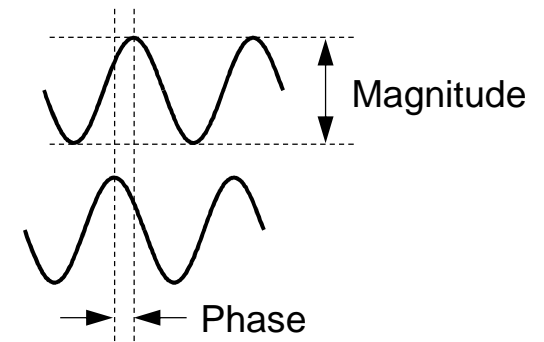
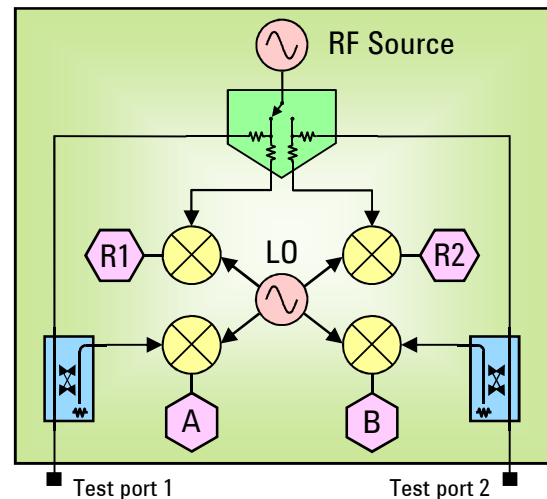
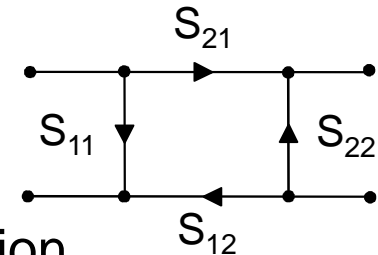
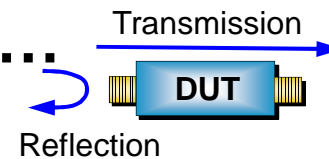
What is Vector Network Analyzer?



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Vector network analyzers (VNAs)...

- Are stimulus-response test systems
- Characterize forward and reverse reflection and transmission responses (S-parameters) of RF and microwave components
- Quantify linear magnitude and phase
- Are very fast for swept measurements
- Provide the highest level of measurement accuracy

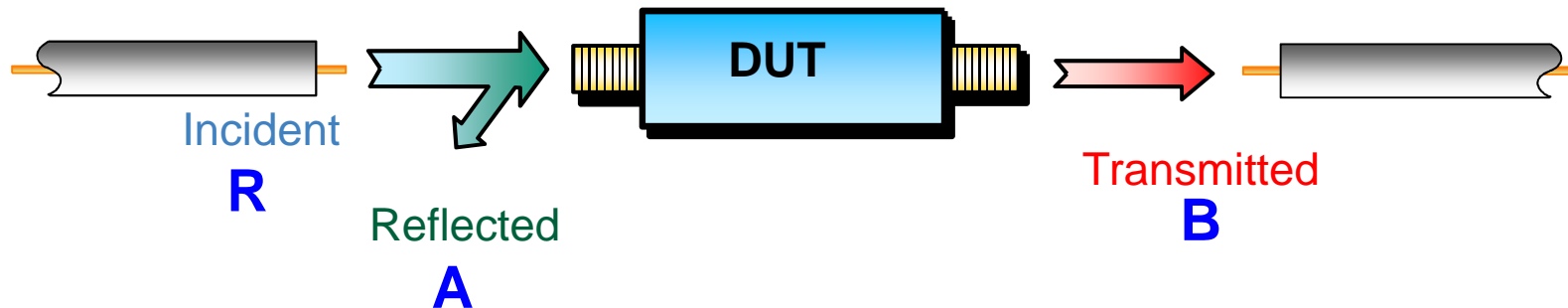


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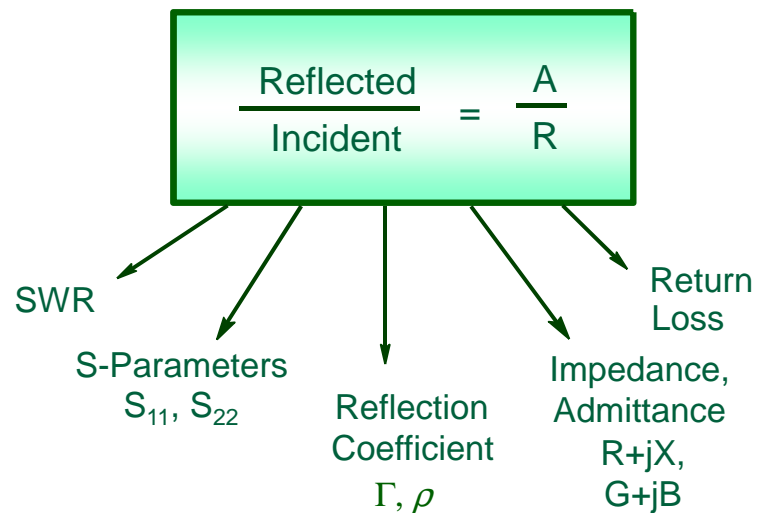
Reflection / Transmission Coefficients



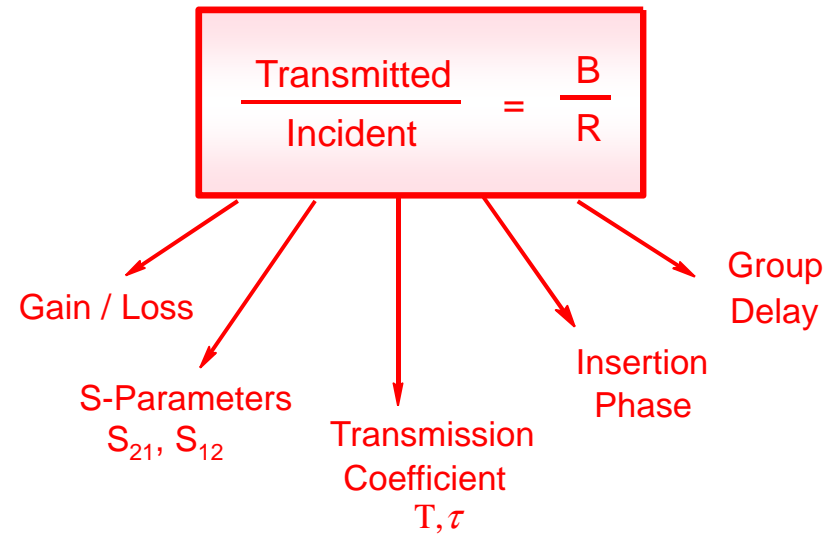
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REFLECTION



TRANSMISSION



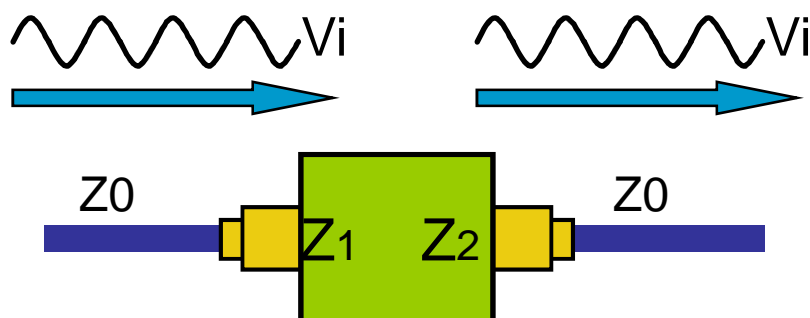
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Signal Integrity vs S-Parameters



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GOOD Signal Integrity



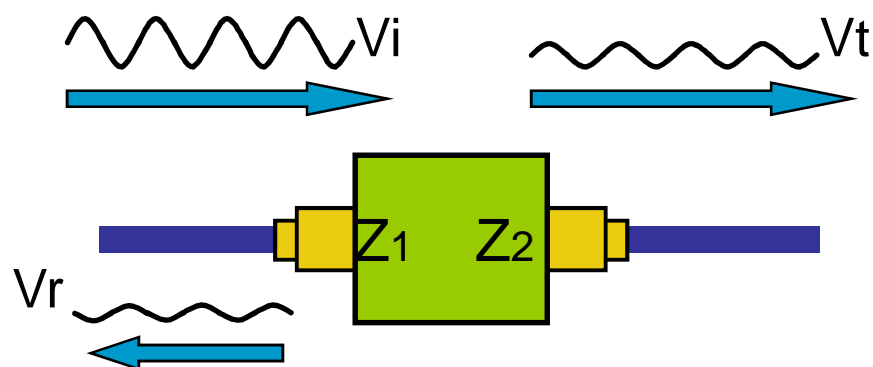
$$Z1=Z2=Z0$$

Well Controlled
Impedance Environment

S11 → low reflections

S21 → high transmission

POOR Signal Integrity



$$Z1, Z2 \neq Z0$$

Impedance
Discontinuities Present

S11 → high reflections

S21 → low transmission

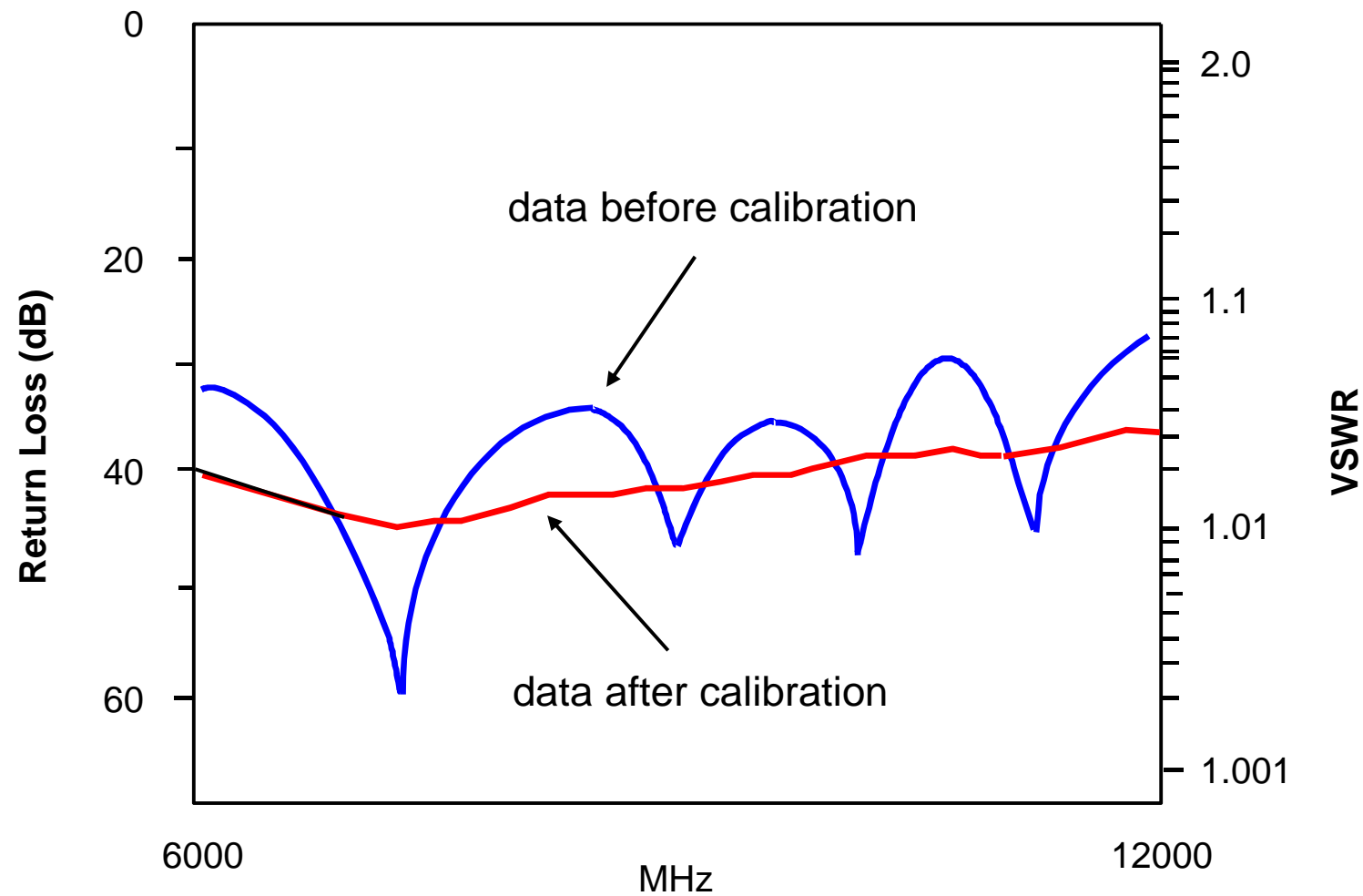


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Importance of Calibration !



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Trend to Differential Topologies



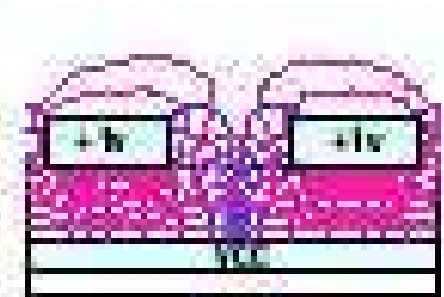
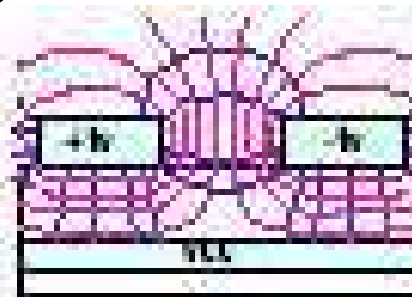
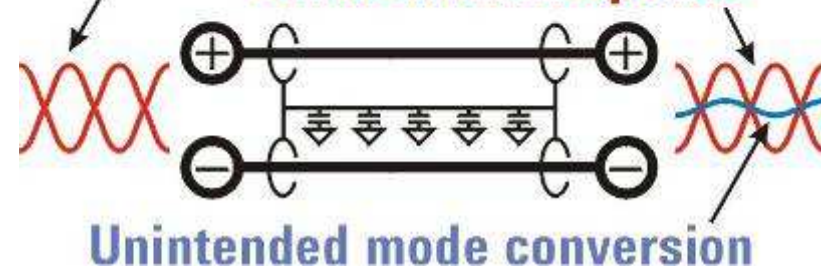
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- **Ideal differential devices**
 - Low voltage requirements
 - Noise and EMI immunity
 - Virtual grounding
- **Non-ideal devices are not symmetric**
 - Can be identified by mode-conversions
 - Differential \rightarrow Common
 - Common \rightarrow Differential
- **Differential signal integrity design tools are needed**

Differential Structure



Differential Stimulus Differential Response



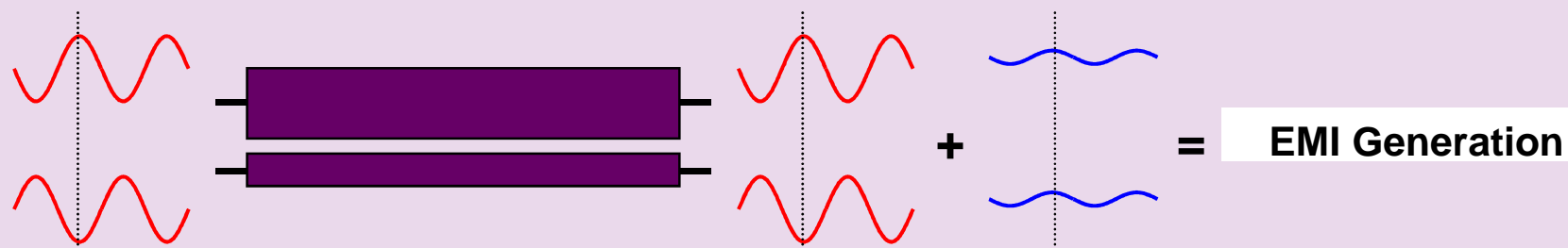
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What about non-ideal devices?



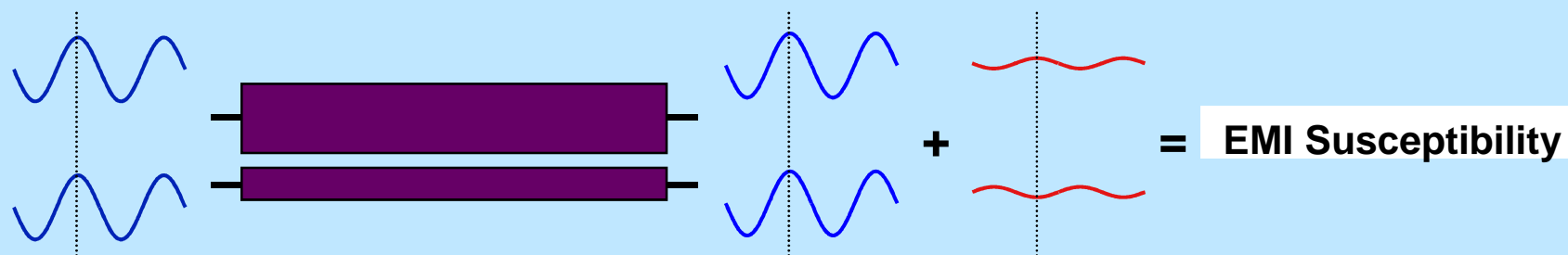
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- **Differential-stimulus to common-response conversion**



Imperfectly matched lines mean the electromagnetic fields of the signals are not as well confined as they should be – giving rise to generation of interference to neighboring circuits.

- **Common-stimulus to differential-response conversion**

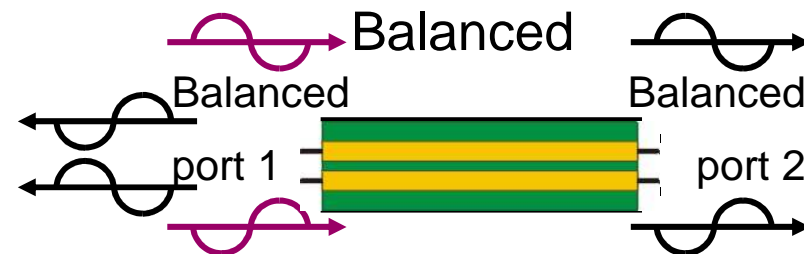
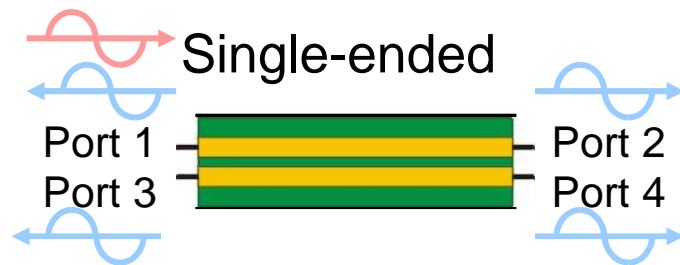


Imperfectly matched lines mean that interfering signals do not cancel out completely when subtraction occurs at the receiver. Measured by stimulating common-mode to simulate interference.

Single-ended to Differential [S]



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Response

Stimulus

S₁₁

S₂₁

S₃₁

S₄₁

S₁₂

S₂₂

S₃₂

S₄₂

S₁₃

S₂₃

S₃₃

S₄₃

S₁₄

S₂₄

S₃₄

S₄₄

MATH...

Differential-Mode Response

Port 1

Port 2

Common-Mode Response

Port 1

Port 2

Differential-Mode Stimulus

Port 1

Port 2

Common-Mode Stimulus

Port 1

Port 2

S_{DD11}

S_{DD21}

S_{CD11}

S_{CD21}

S_{DD12}

S_{DD22}

S_{CD12}

S_{CD22}

S_{DC11}

S_{DC21}

S_{CC11}

S_{CC21}

S_{DC12}

S_{DC22}

S_{CC12}

S_{CC22}

MATH...

Naming Convention:

$S_{\text{mode res., mode stim., port res., port stim.}}$

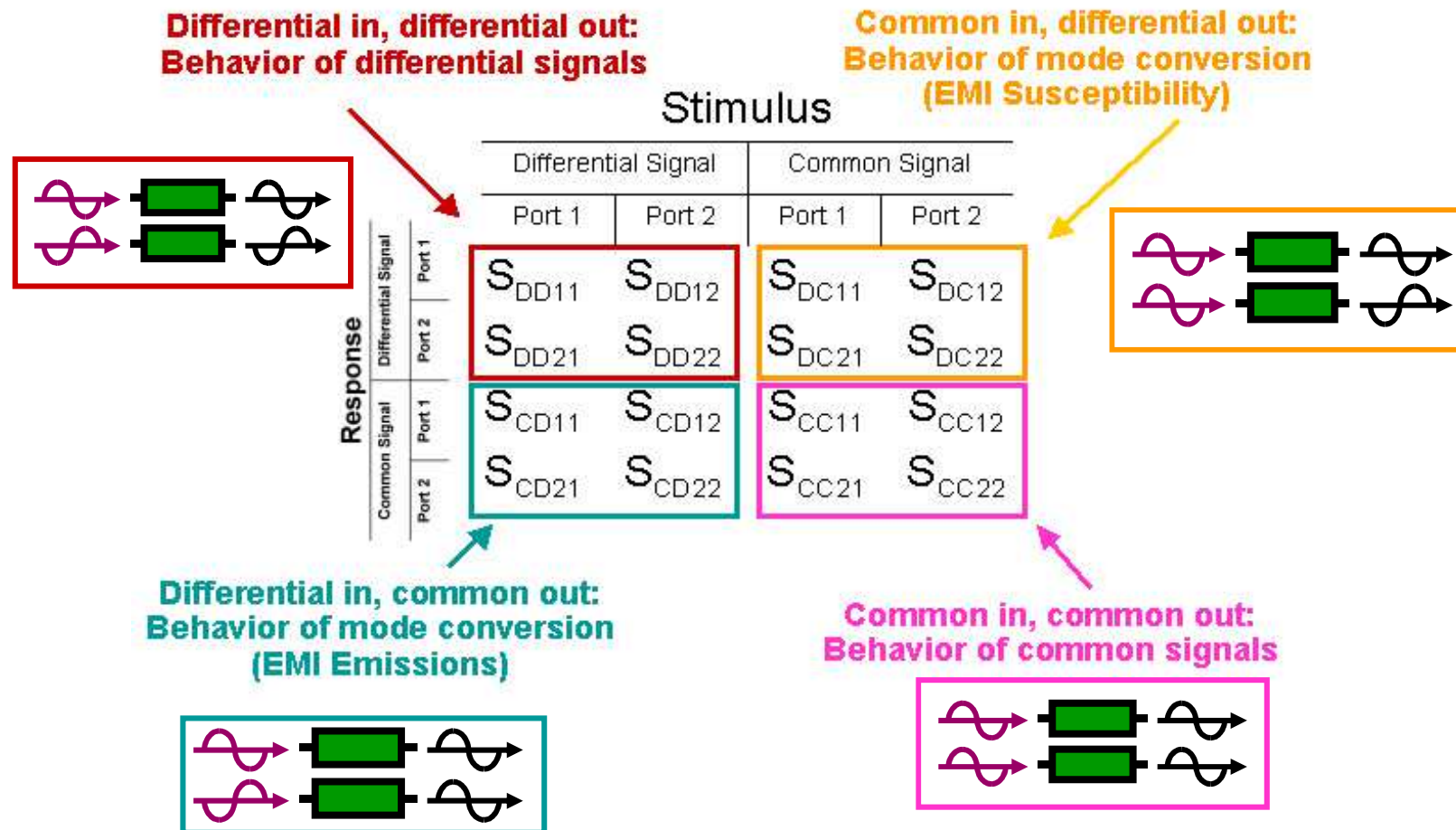


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Mixed-Mode S-Parameters



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Example S_{CD21} : Drive port 1 differentially and measure what has been converted to common mode at port 2



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AGENDA



Unlocking Measurement Insights for 75 Years

- Introduction / Signal Integrity Definition
- Evolution of Test Parameters
- Traditional TDR/TDT instrument
- Vector Network Analyzer Basis
- Single Ended / Differential Topologies
- **Physical Layer Test System (PLTS Software)**

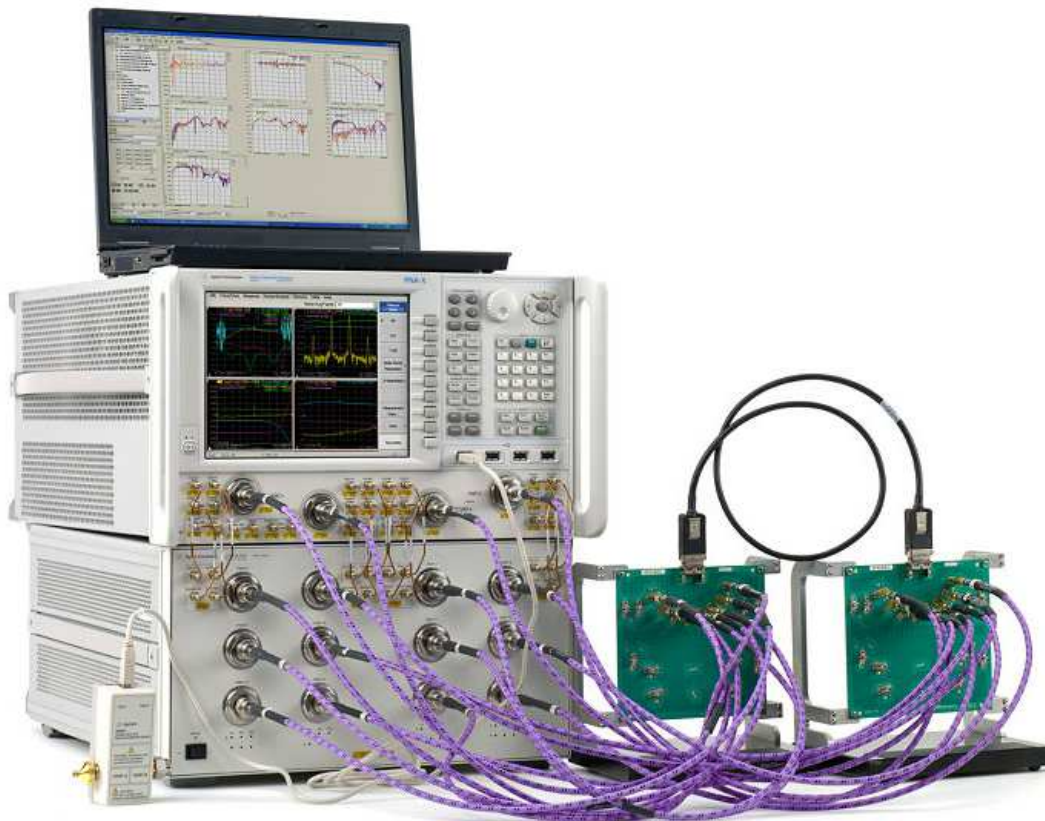


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What is PLTS?



Unlocking Measurement Insights for 75 Years



- N1930B - Software Solution
- Industry standard for interconnect analysis
- Calibrate, measure and analyze linear passive devices
- Use either VNA or TDR
- Provides Advanced Calibration Techniques

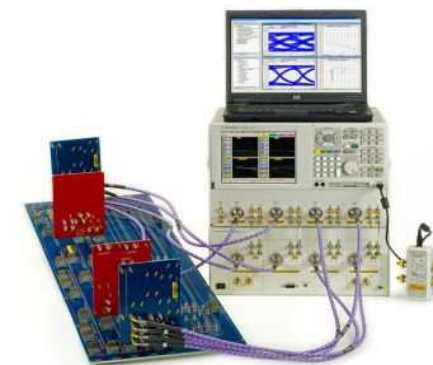
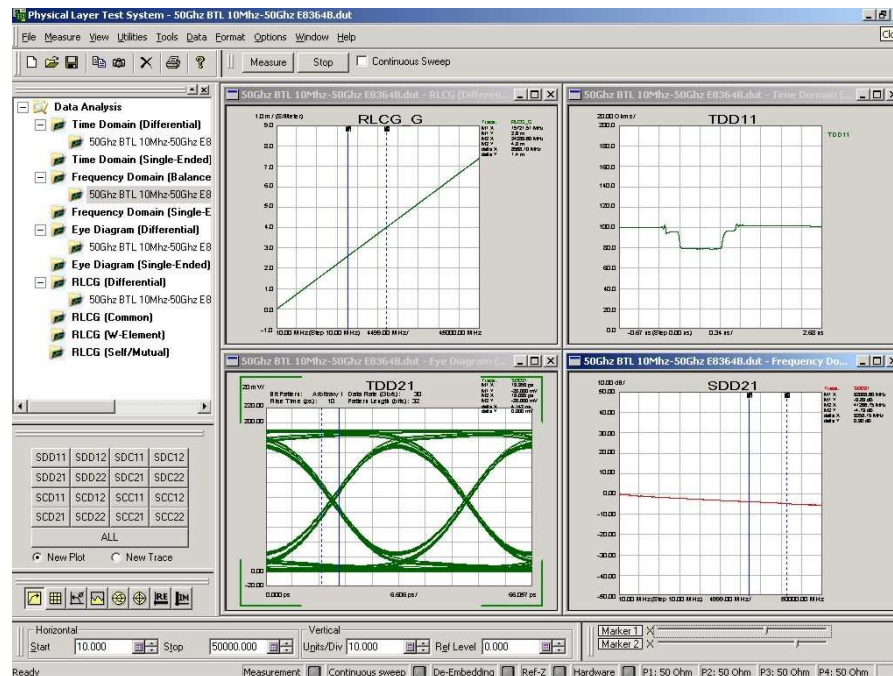
PLTS: The Ultimate SI Solution



Unlocking Measurement Insights for 75 Years

Agilent Physical Layer Test Systems (PLTS) are the most accurate and comprehensive tools for characterizing high-speed digital interconnects.

- Reduce development times
- Increase performance margins
- Improve signal quality
- Reduce EMI emissions/susceptibility
- Improve models for simulation
- Develop more competitive products

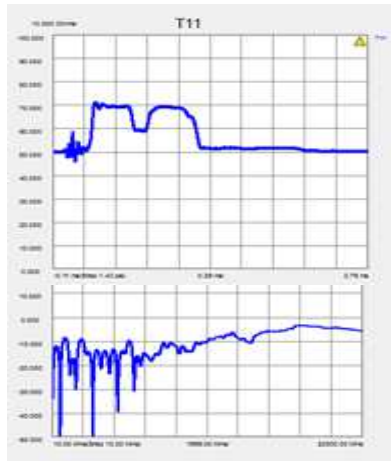


N1930B Physical Layer Test System (PLTS)

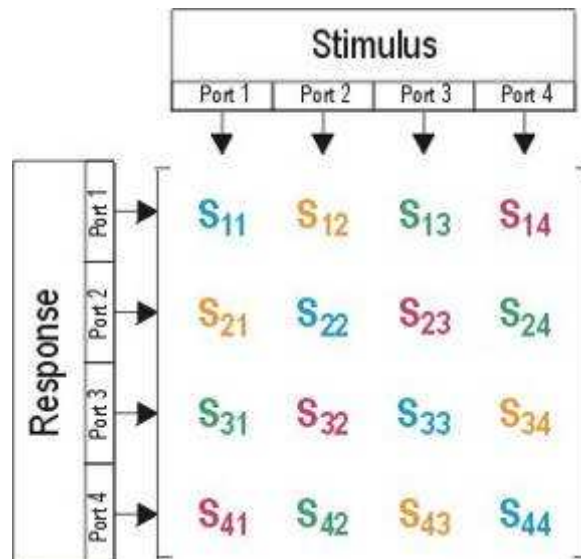
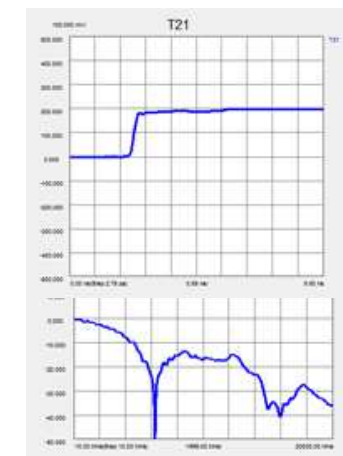


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TDR/TDT and S-Parameters

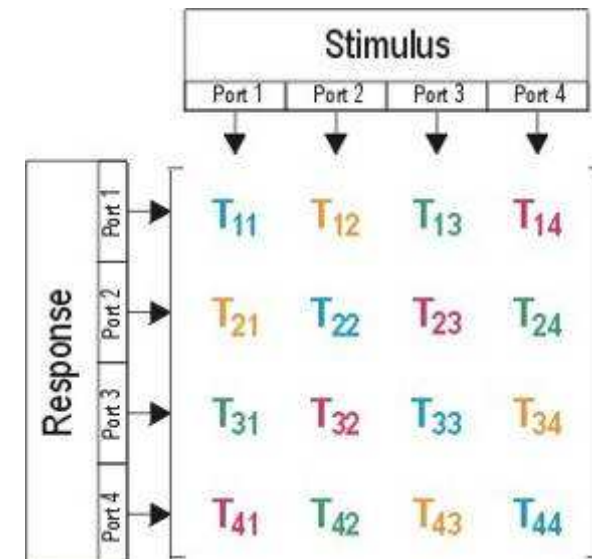


Tremendous insight together.



Frequency Domain Parameters

Return Loss or TDR
Insertion Loss or TDT
Near End Crosstalk (NEXT)
Far End Crosstalk (FEXT)



Time Domain Parameters

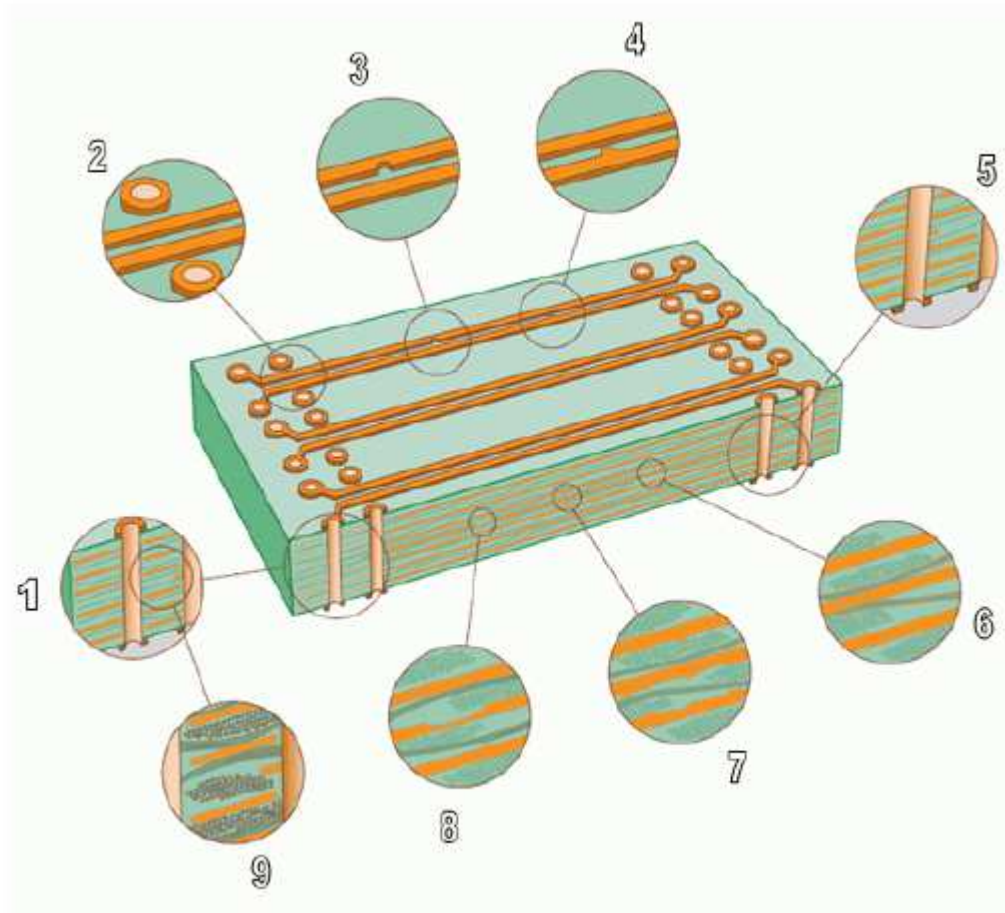


Find out what's causing impedance discontinuities on your PCB



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1. Parasitic capacitance in through hole
2. Localized crosstalk
3. Localized changes in conductor width
4. Localized changes in conductor spacing
5. Reflections due to via stub
6. Non-uniform dielectric
7. Dielectric constant variation
8. Surface treatment thickness non-uniformity
9. Localized changes in foil thickness

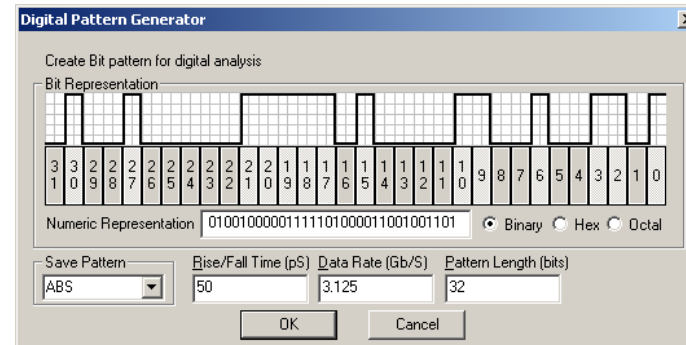


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PLTS Eye diagram



PLTS Virtual Pattern Generator



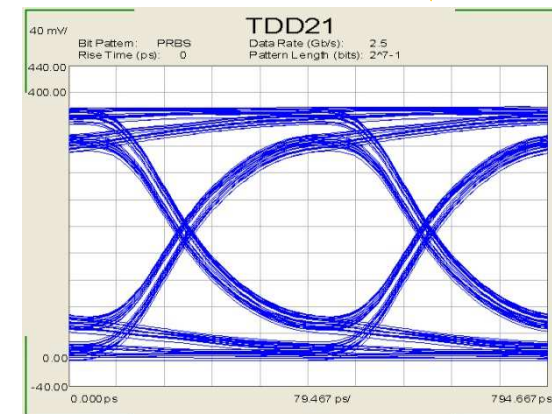
Measurement Insights for 75 Years

Measured Data
(TDR or VNA)

Impulse
Response

Convolution

Eye
Diagram



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PLTS RLCG Model Extraction

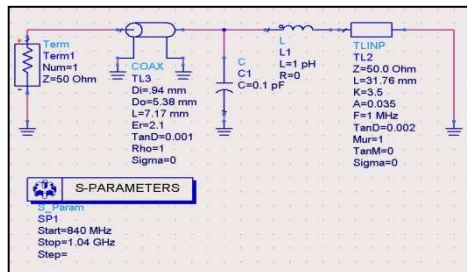
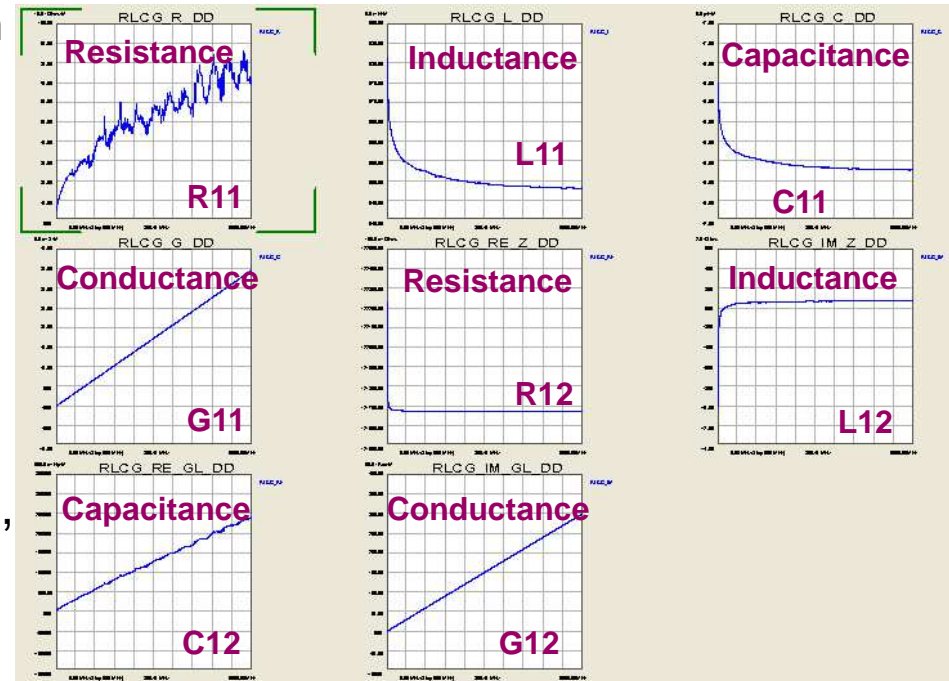


Unlocking Measurement Insights for 75 Years

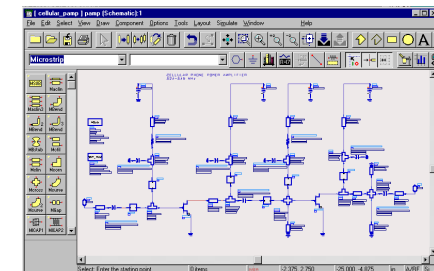
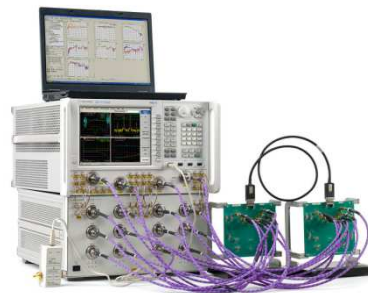
RLCG models describe electrical behavior of passive transmission lines in an equivalent circuit model

PLTS creates highly accurate, measurement-based coupled transmission line model

PLTS can export into modeling and simulation software such as Agilent ADS, Synopsis HSPICE, and TDA Systems Iconnect



Transmission line RLCG model



ADS schematic



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Demo: PLTS



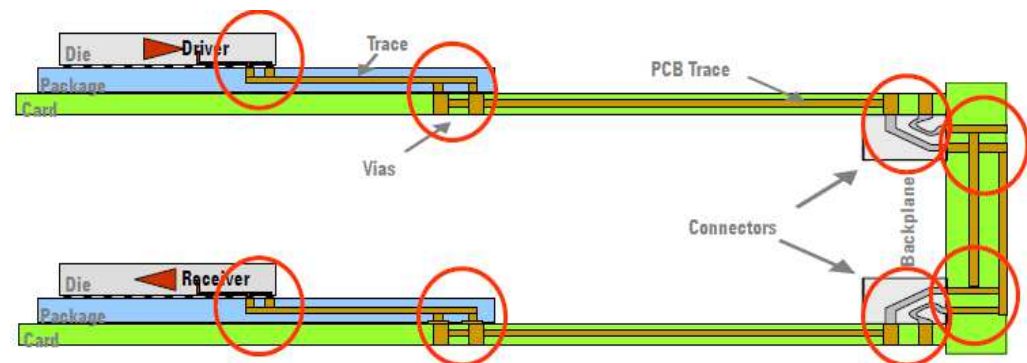
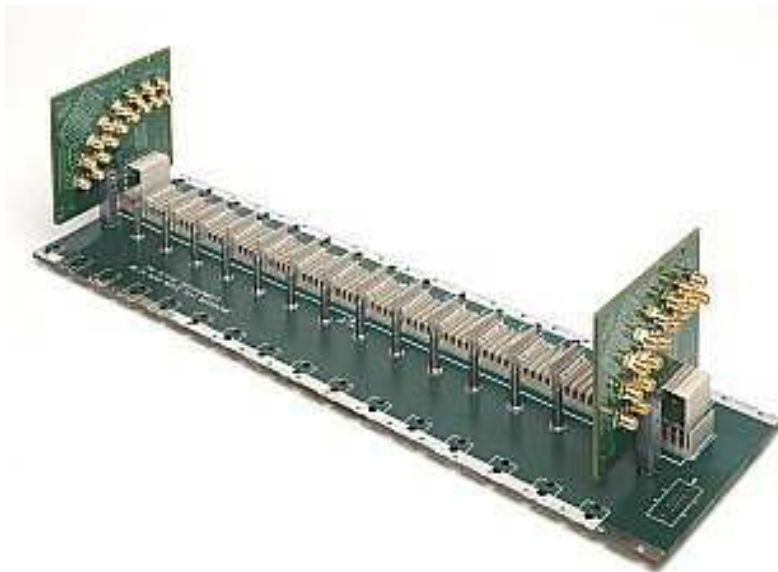
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XAUI Backplane Interconnect

The XAUI is designed as an interface extender, and the interface, which it extends, is the XGMII, the 10 Gigabit Media Independent Interface.

Differential Topology, Data Rate = 3.125Gbps , rise time = 60ps

Want to know more about XAUI?... <http://cp.literature.agilent.com/litweb/pdf/5988-5509EN.pdf>



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Non Coaxial Challenge



Unlocking Measurement Insights for 75 Years

Signal Integrity devices do not have coax connectors

- Packages, high speed differential connectors, traces, cables, backplanes, etc

Many RF devices are fixtured for measurements

There are two choices (both can give good results):

- **Probe your device**
 - Expensive, probing expertise required, can be difficult
- **Build a Fixture for your device to get to coax**
 - How to remove your fixture effects when they can't be ignored?



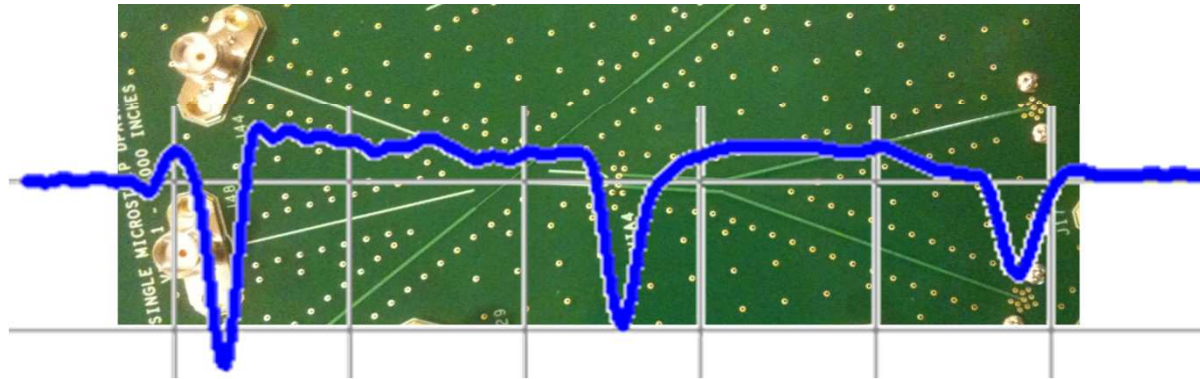
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The Problem...

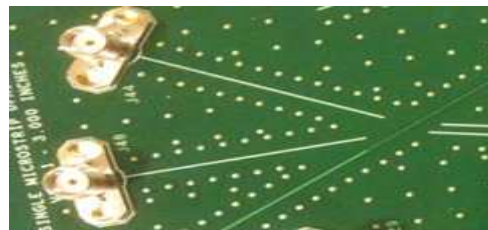


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What I want to measure is embedded in the middle of a bunch of interconnect I don't care about



I just want the via structure, or the connector, or the cable, or the interface, or the uniform trace,...

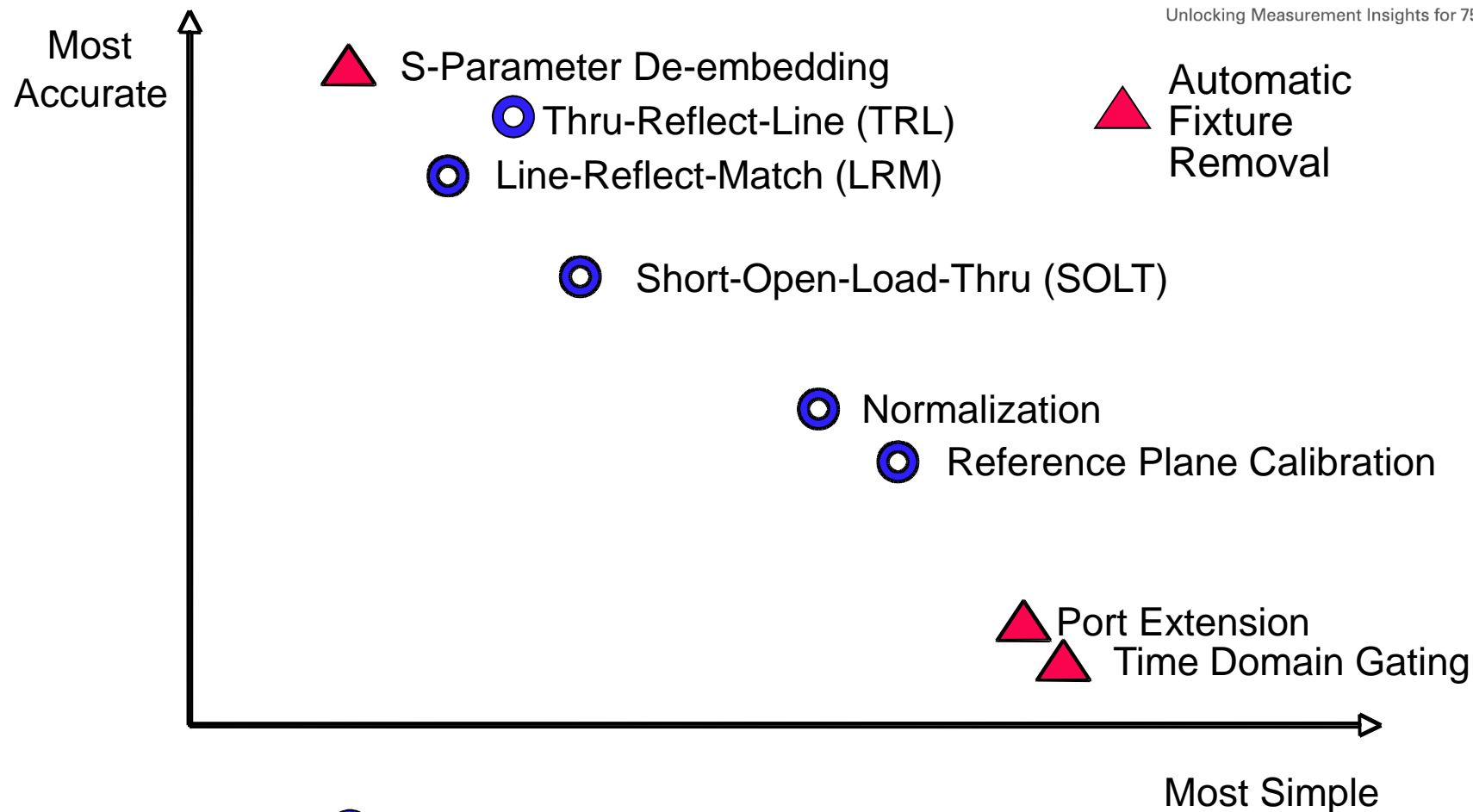


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Error Correction Techniques



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○ = Pre-measurement error correction

▲ = Post-measurement error correction



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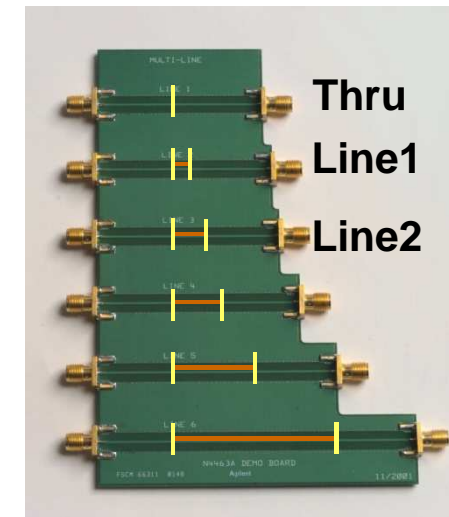
The Solution...



Unlocking Measurement Insights for 75 Years

Traditional Calibration

- SOLT
- TRL (thru, reflect, line)
- LRM (line, reflect, match)



De-embedding using

- Measured test fixtures
- Calculated test fixtures by 3D full wave field solver
- Calculated test fixtures by approximation (port extension)

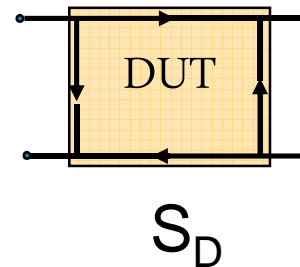
The new way: really simple, **automatic fixture removal (AFR)**

De-Embedding “Automagically”

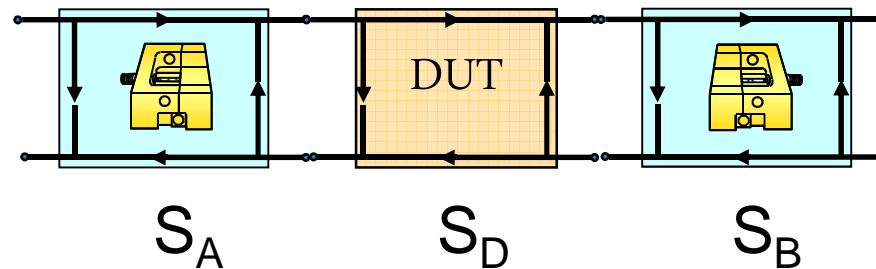


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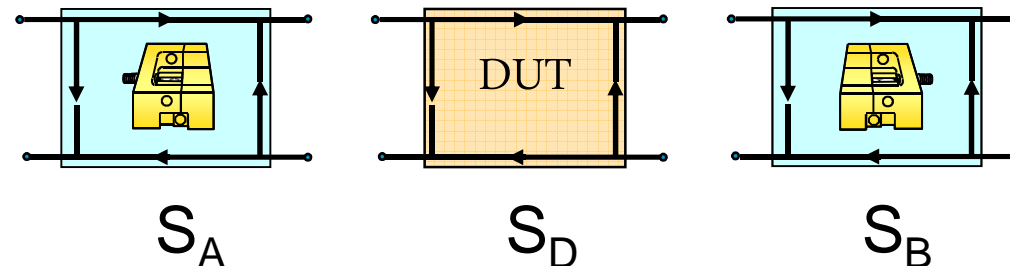
What we want: DUT performance



What we measure:
composite measurement
of DUT and fixtures



With the separate fixtures' S-Parameters, we can de-embed the DUT alone from the composite measurements



The challenge: getting the S_A and S_B de-embed files



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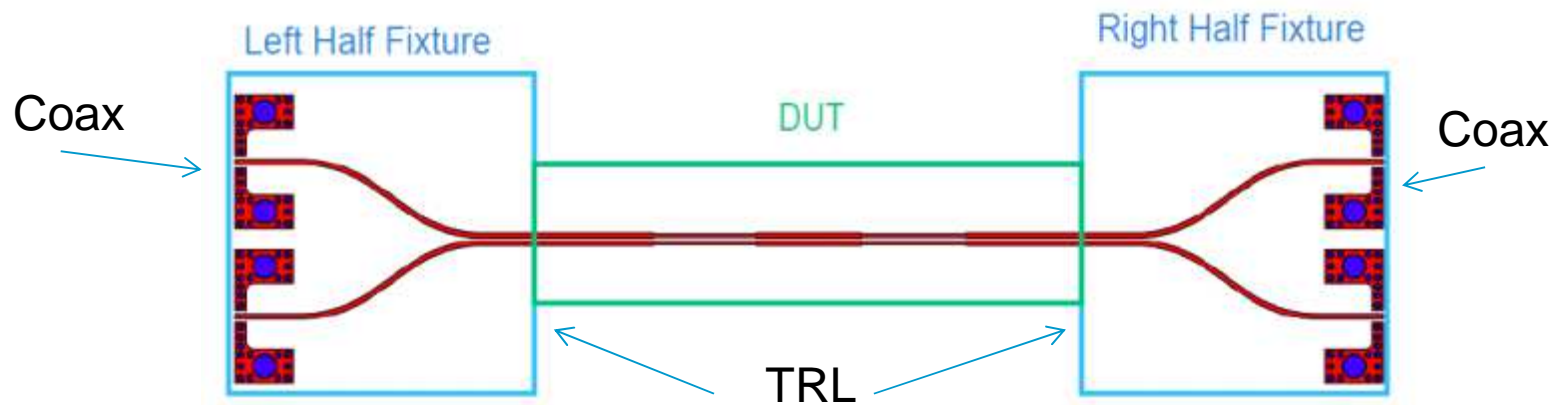
Removing Fixtures



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Historically – 2 methods:

- Model fixture using EM Simulation and de-embed the fixtures from the measurement
- Use a TRL calibration technique to move measurement reference planes to the DUT.



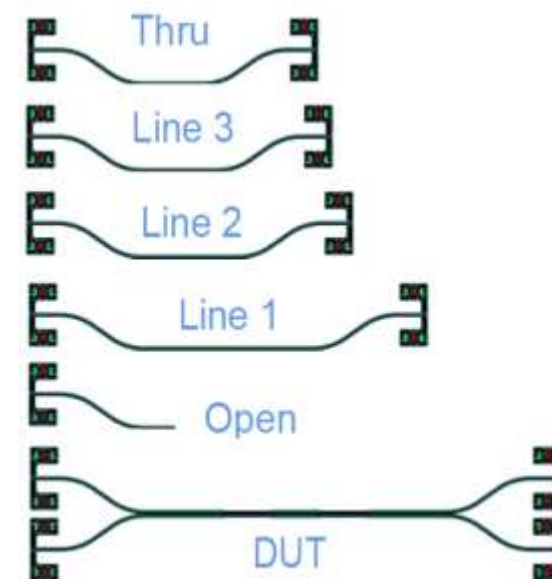
TRL (Single Ended)



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Assumptions for single ended TRL

- Connectors and launches are identical
- All lines have same Transmission Line characteristics
 - Impedance, loss, propagation
 - Only differ in length
- Lines are usable 20 to 160 degrees relative to thru
- **No coupling in fixture is removed**
- Usually 2-4 lines depending on frequency range



Differential Cross Talk Calibration



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4-port TRL Calibration Technique

Fixture may be asymmetric

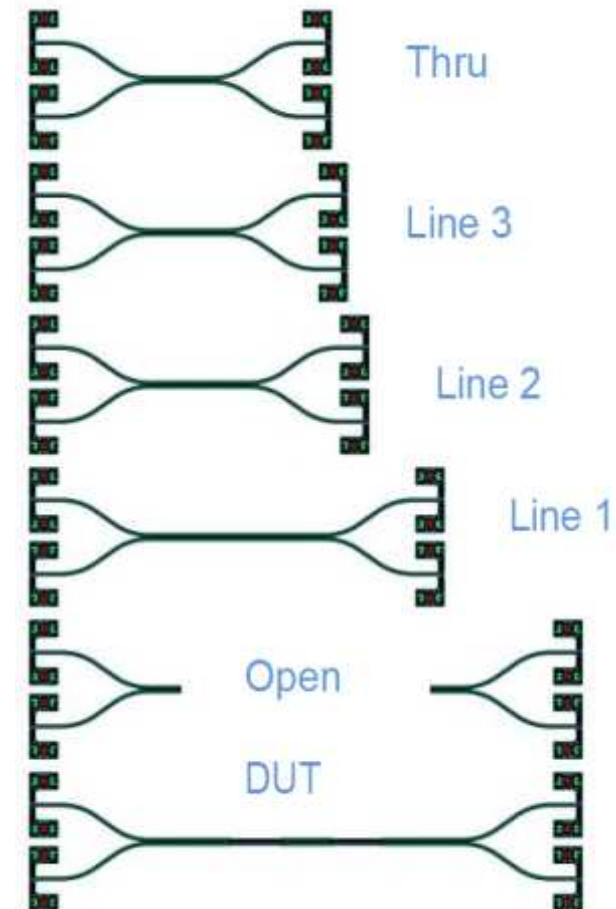
Similar assumptions to single ended TRL

- Repeatability of connector, launch, and line
- lines are usable 20 to 160 degrees relative to thru

Additional differential constraints

- SDCnm and SCDnm < -30 dB
- Skew between lines < 10 degrees

Coupling in fixture is removed

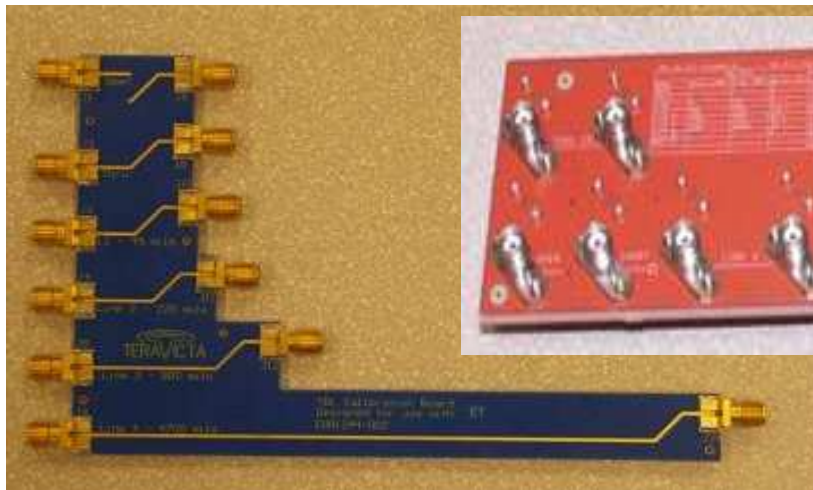
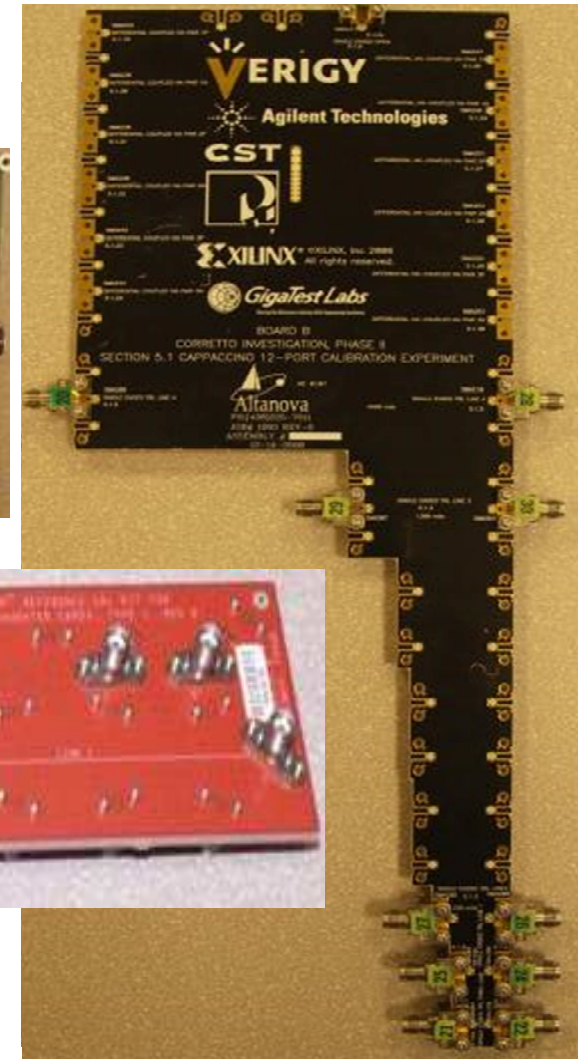
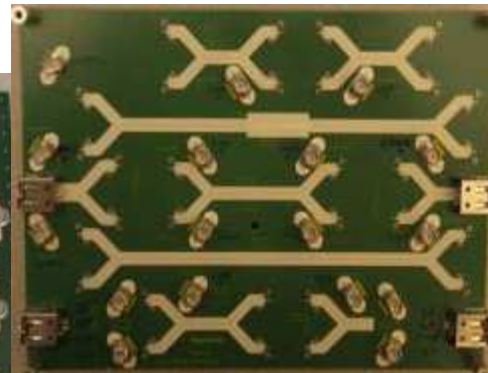
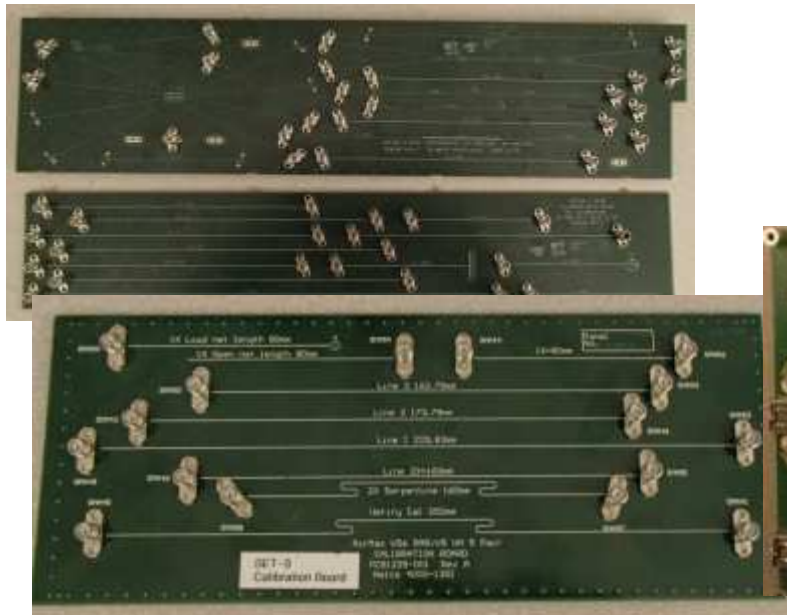


Design/ Verify in PLTS your TRL calkits



KEYSIGHT
TECHNOLOGIES

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Automatic Fixture Removal !!!



Unlocking Measurement Insights for 75 Years

New 5 Step Wizard makes it easy to define your fixture and remove it from your measurement.

Automatic Fixture Removal (AFR)

1. Describe Fixture 2. Specify Standards 3. Measure Standards 4. Remove Fixture 5. Save Fixture

This 5 step wizard characterizes and removes the fixture effects from your measurement.

My fixture inputs are:

☐ Single Ended

☒ Differential

My measurement is:

☐ 2 Port

☒ 4 Ports

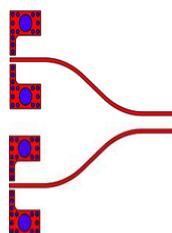
Current Fixture and DUT Assumptions

Fixture Match : A = B

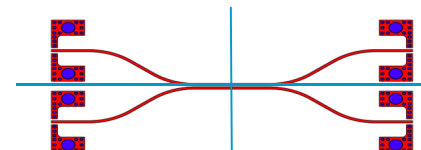
Fixture Length: A = B

DUT Z0: will be set to System Z0

Open or Short



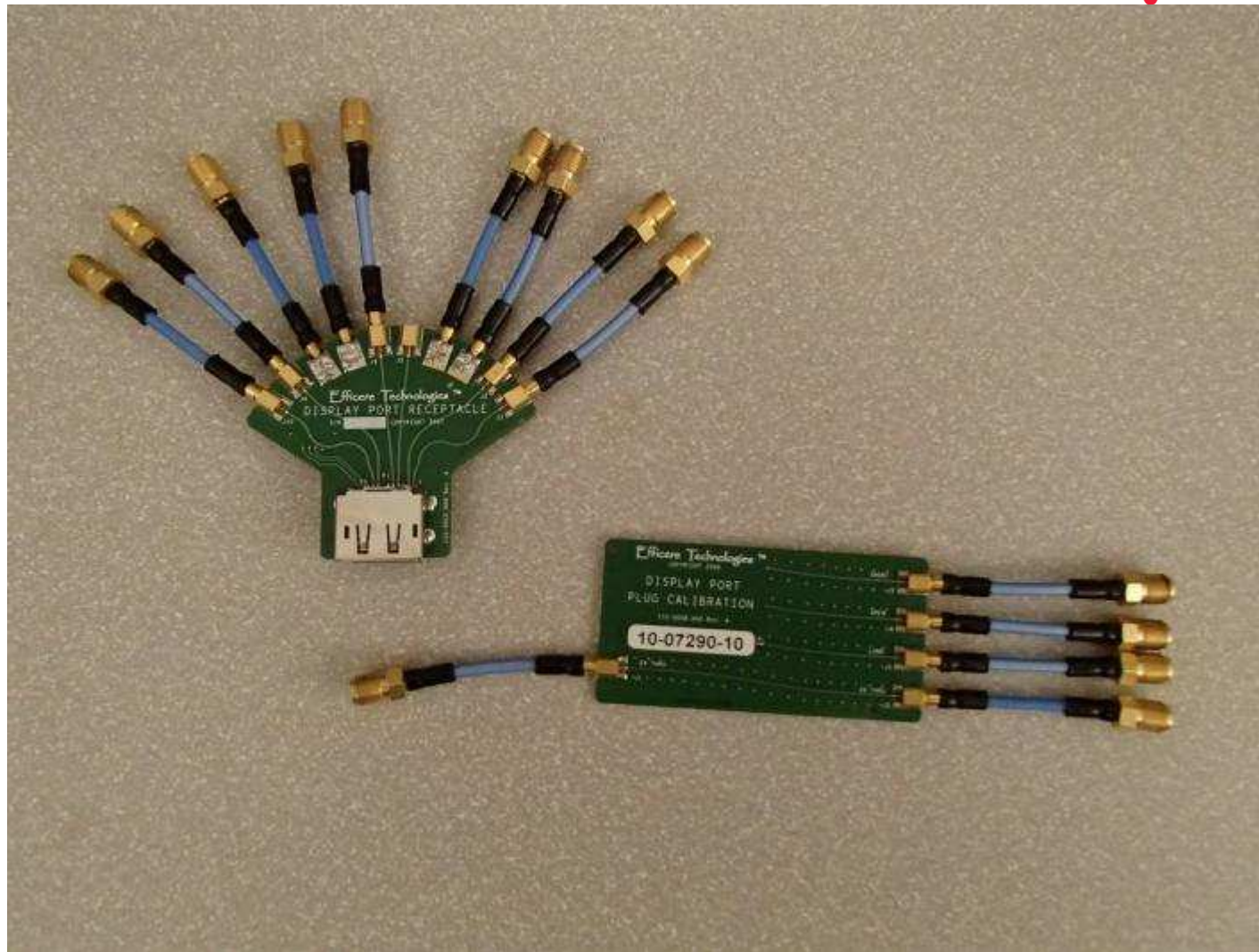
2xTHRU



Cable Fixtures – Display Port



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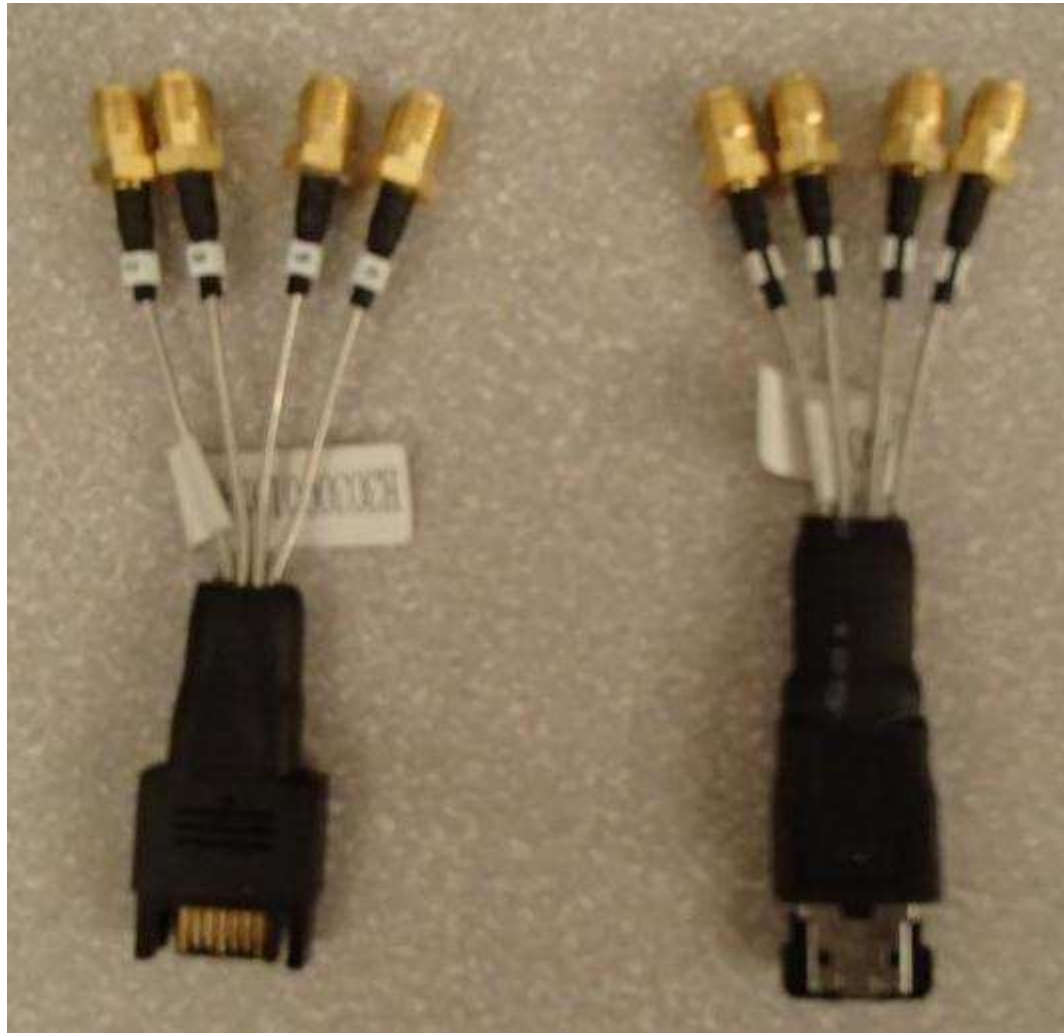


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Cable Fixtures – SATA



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Cable Fixtures – HDMI



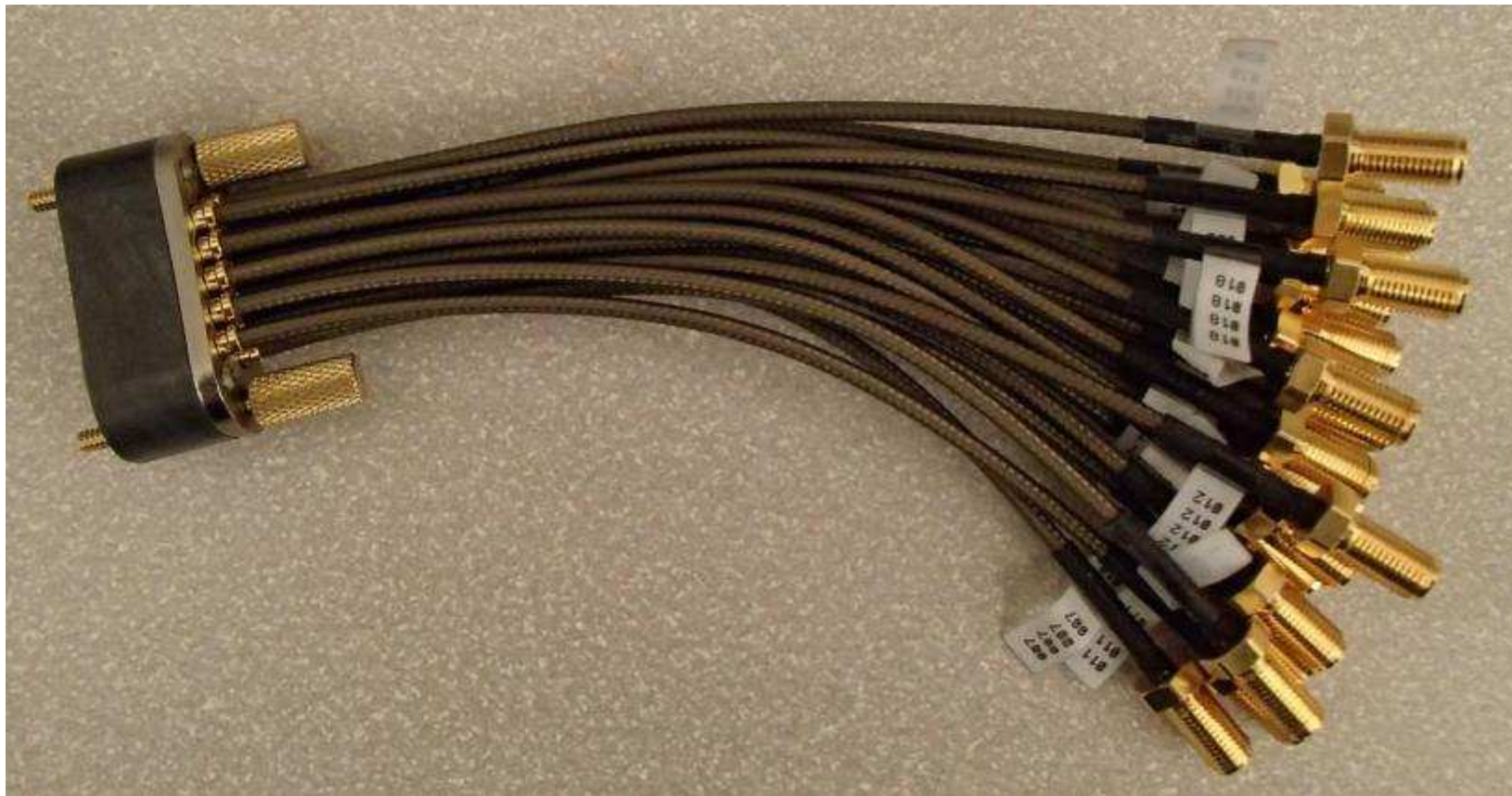
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Cable Fixtures – Bullseye Connector Fixture



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Demo: PLTS-AFR



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One-Port Automatic Fixture Removal

