

# INTEGRIDAD DE SEÑAL

TDR/TDT basados en Analizador Vectorial de Redes



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91 631 3300

# AGENDA



Unlocking Measurement Insights for 75 Years

- TDR based on VNAs
- Advanced TDR for Signal Integrity
- Stressed Eye Diagram Analysis
- Hot TDR Measurements
- Compliance Support: MOIs
- Correlation Data among VNA and Sampling Scopes



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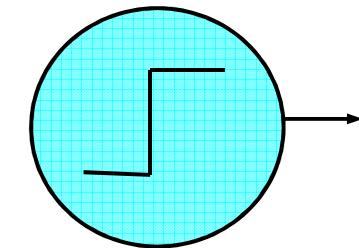


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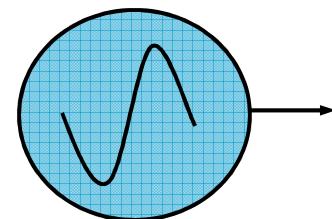
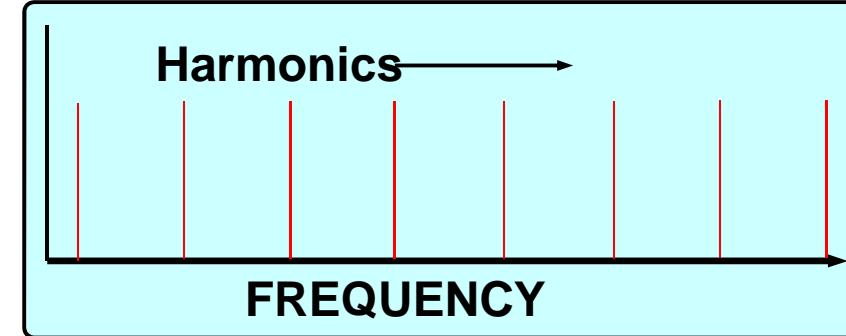
# TDR vs Network Analyzer Sources



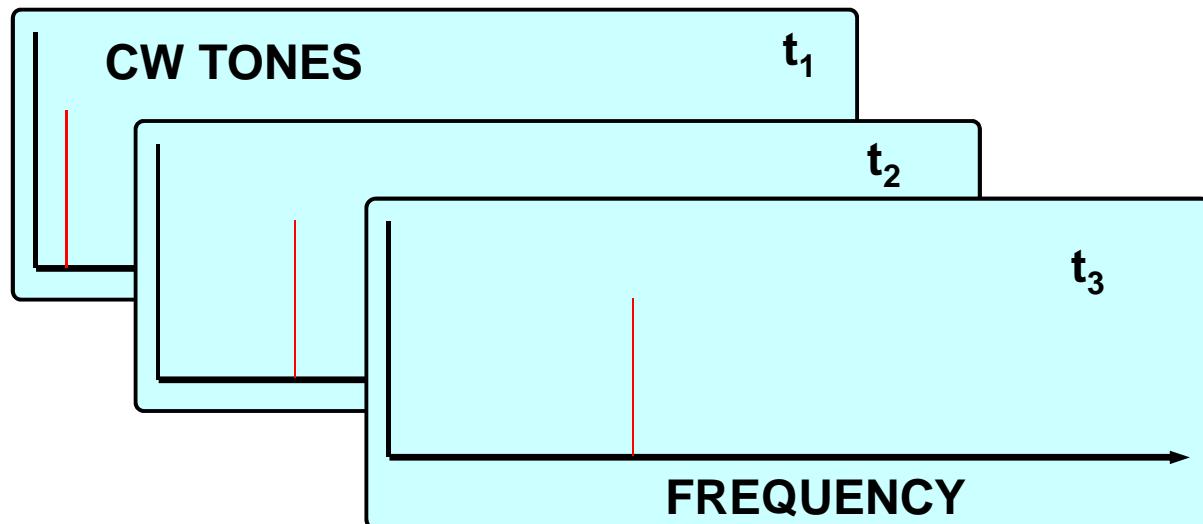
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**STEP / SNAP  
GENERATOR**



**SYNTHESIZED  
VNASOURCE**



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# How the VNA measure the time domain ?



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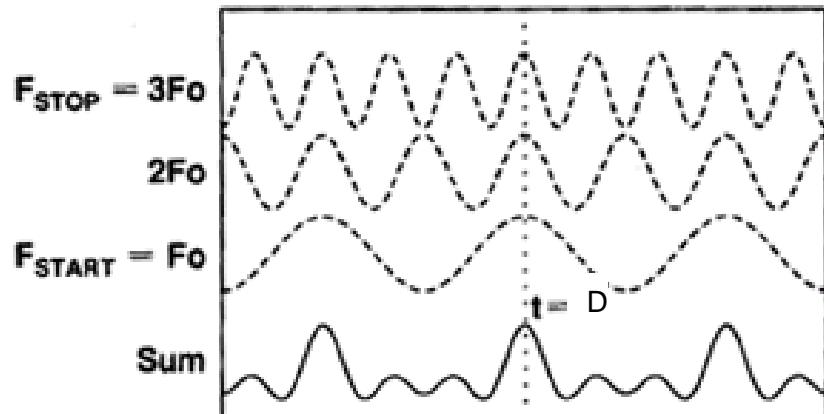


Fig.1

Open

Infinite frequency component create an impulse!

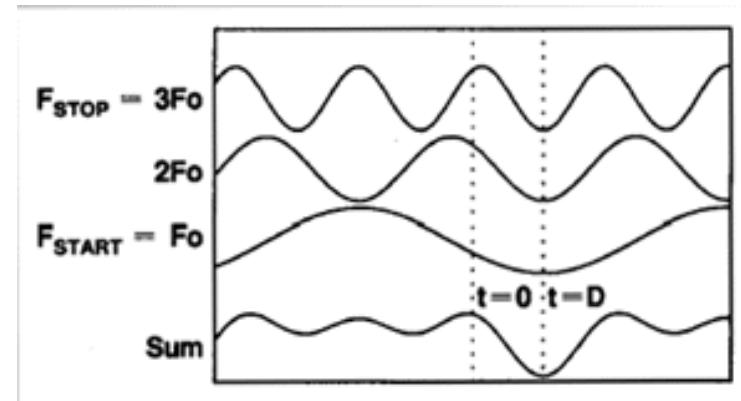
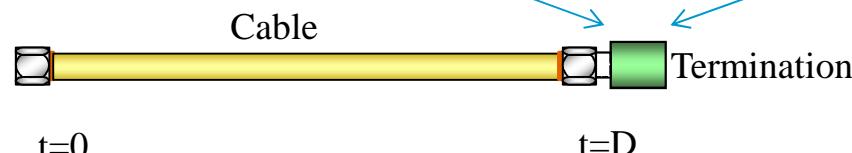


Fig.3 Short



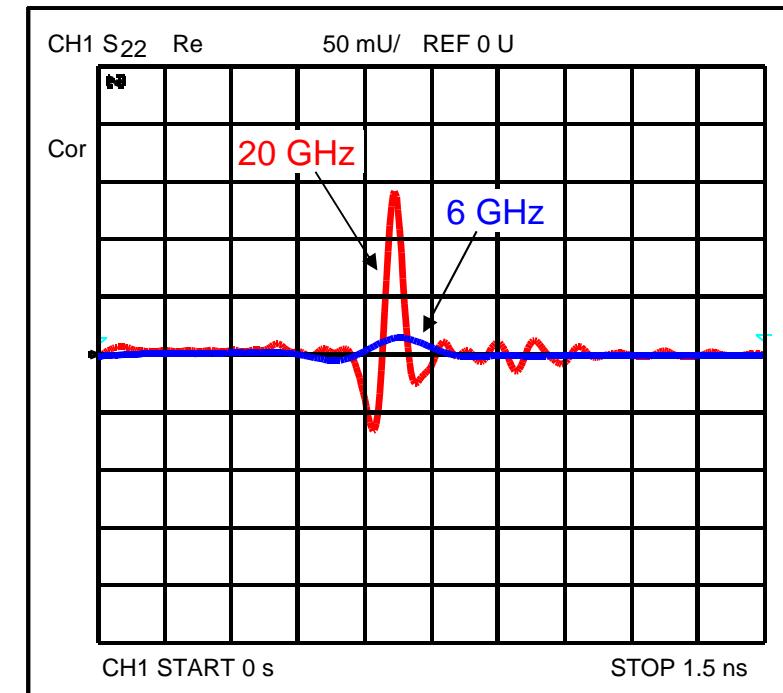
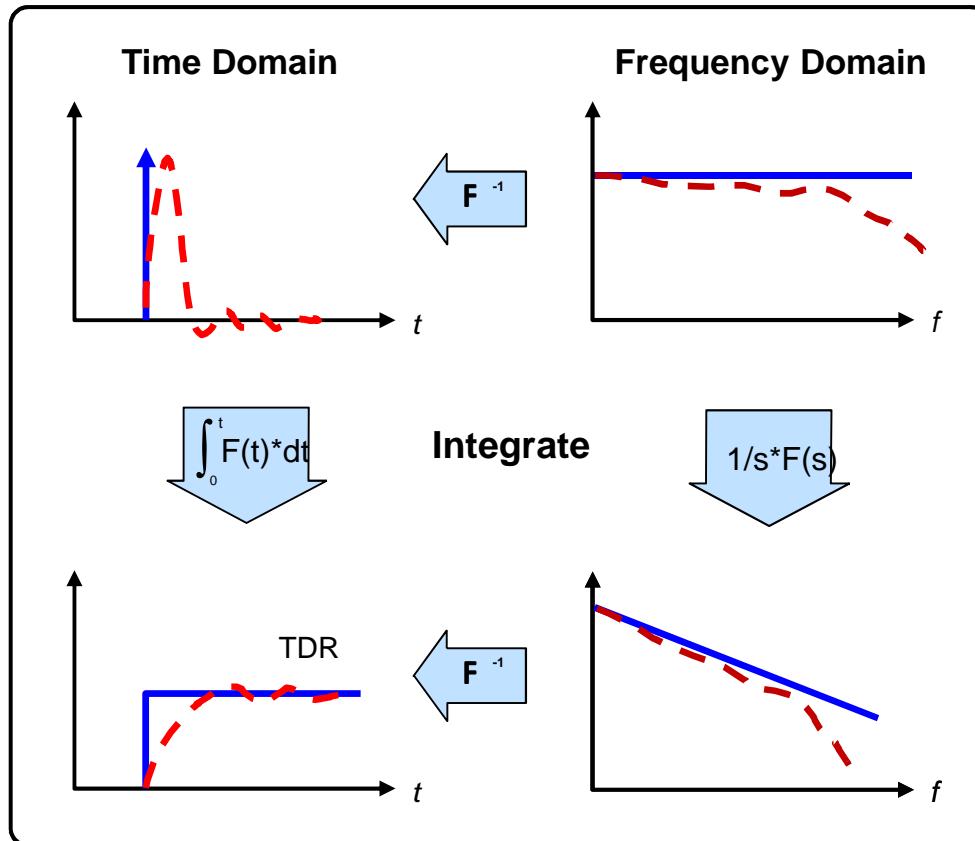
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# TDR Basics Using a Network Analyzer



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- DUT is stimulated by one “harmonic” at a time
- use inverse-Fourier transform to compute time-domain
- resolution inversely proportionate to frequency span



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# Analyzing Low Pass Reflections



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Impedance	Low Pass Step Response	Low Pass Impulse Response
Short		
Open		
$R > Z_0$		
$R < Z_0$		
Shunt C		
Series L		
Series C		
Shunt L		



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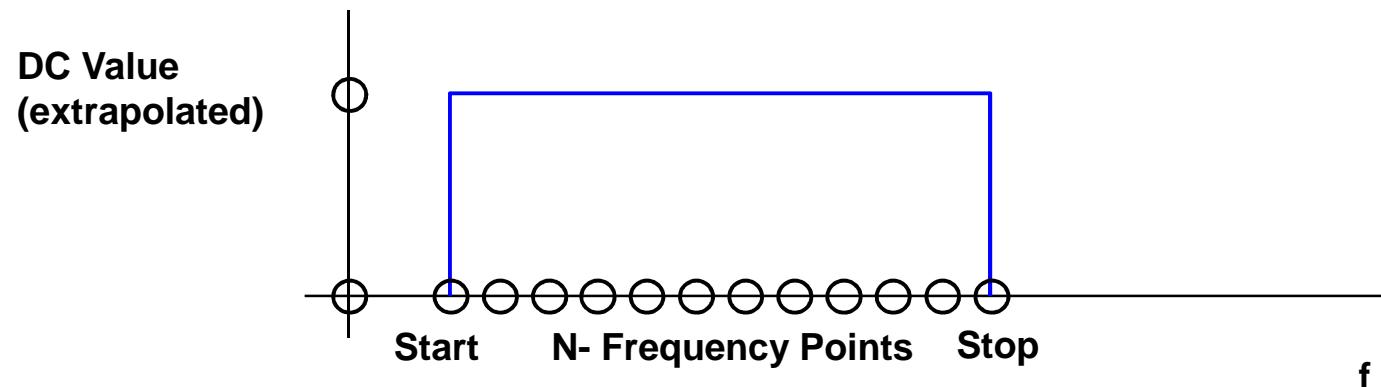
# Low Pass Stimulus



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Require equally spaced points

$$F_{\text{stop}} = N * F_{\text{start}}$$



To insure that these criteria are met, press the “**set frequency low pass**”



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# Time Domain Resolution



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## Response resolution (see presentation\_1)

- Ability to Resolve Closely Spaced Responses
- Dependent Upon Step Rise Time (10-90%) and Impulse Width (50%)

## Range Resolution

- The Ability to Locate a Single Response in Time

$$\text{Range Resolution} = \frac{\text{Time Span}}{\text{Points} - 1}$$



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# To Increase Alias Free Range



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$$\text{AFR} = (\text{Number Points} - 1) / \text{Span}$$

- Increase the number of points
- Decrease frequency span



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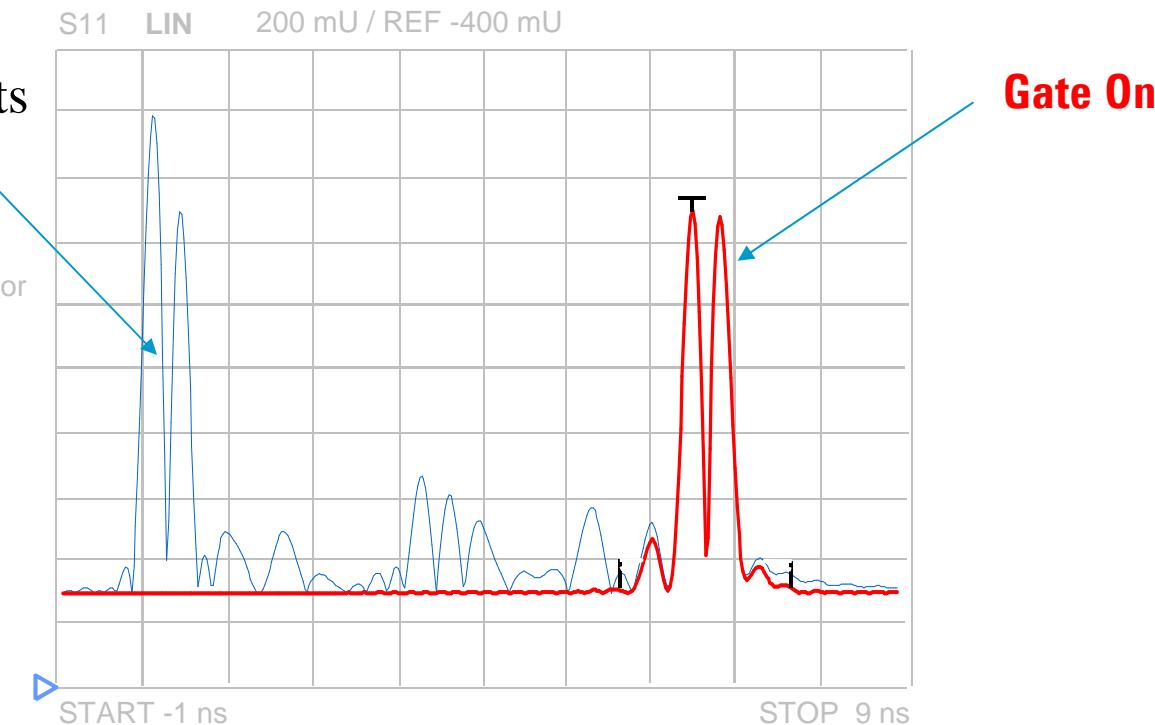
# Gating : Time Domain



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Remove the effects  
of the Input  
Connector

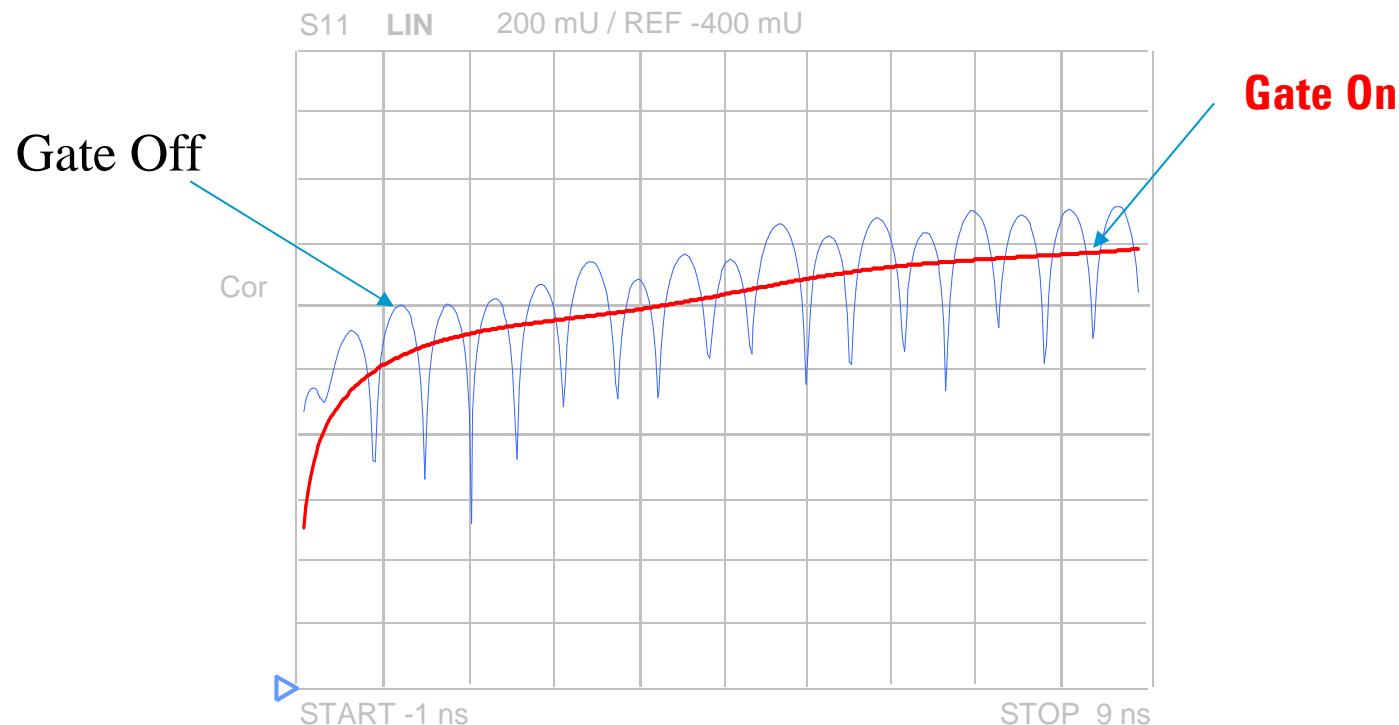


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# Gating : Frequency Domain



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*Use Gating to show the frequency response of the output connector & termination only*

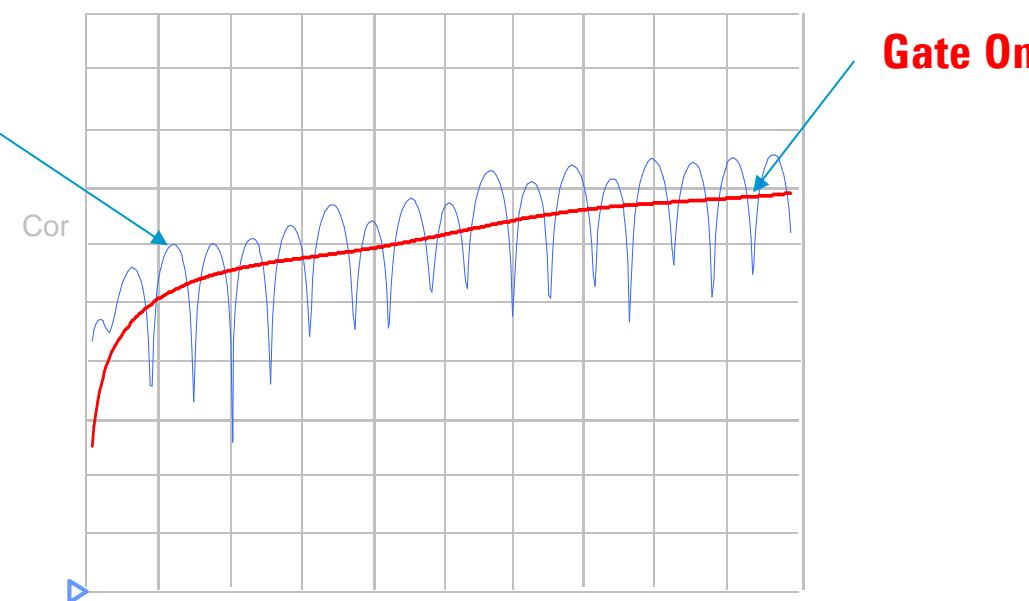


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# Demo: TDR based on VNA



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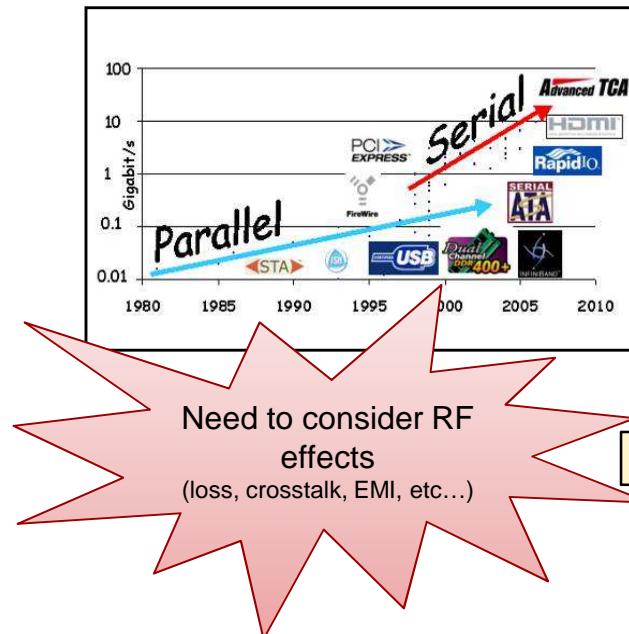
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# Technology Trends

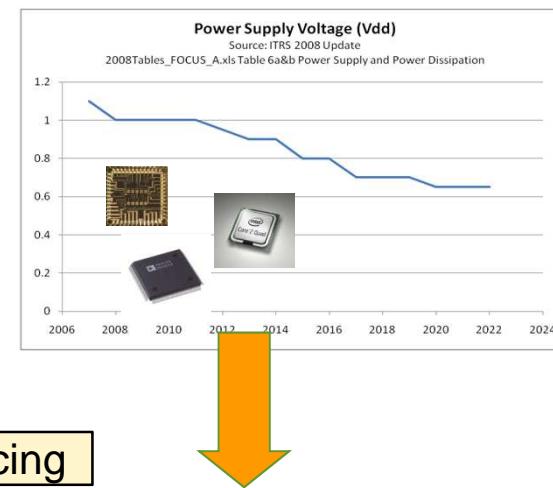


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## Data Rates Increase (>1Gbps)



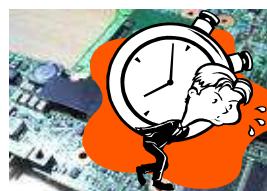
## Lower Power Supplies



SNR Degradation

**Need for Fast, high dynamic range and Accurate measurements**

Shorter design cycles



**Simple and Intuitive** operation

Lower cost of ownership



**ESD Robustness**

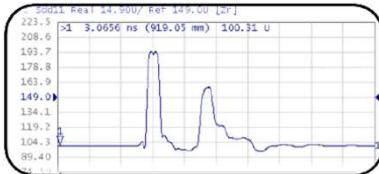


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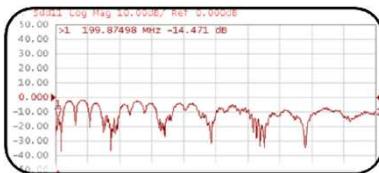
# One-Box Solution for Signal Integrity



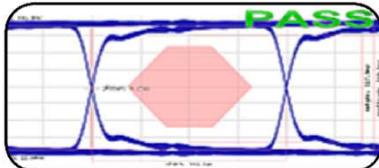
Time domain



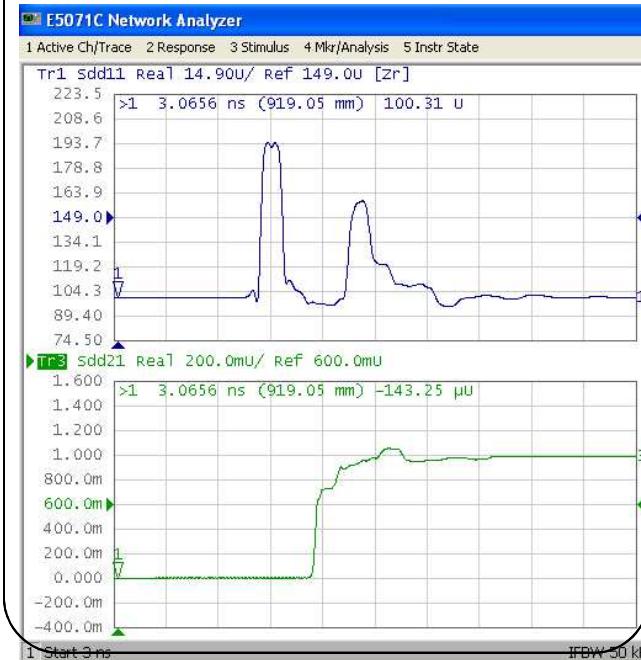
Frequency domain



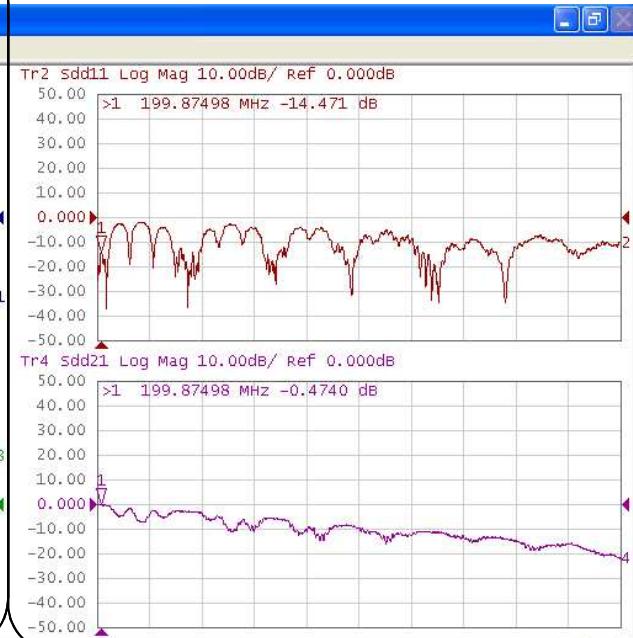
Eye diagram



Time domain



Frequency domain



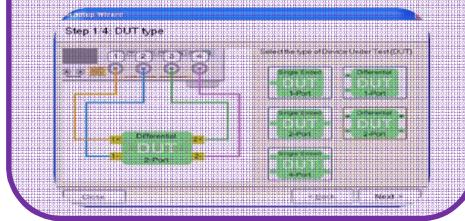
5 years

# Signal Integrity Design & Verification

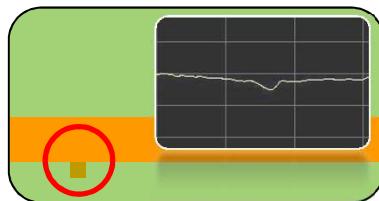


Unlocking Measurement Insights for 75 Years

Simple & Intuitive



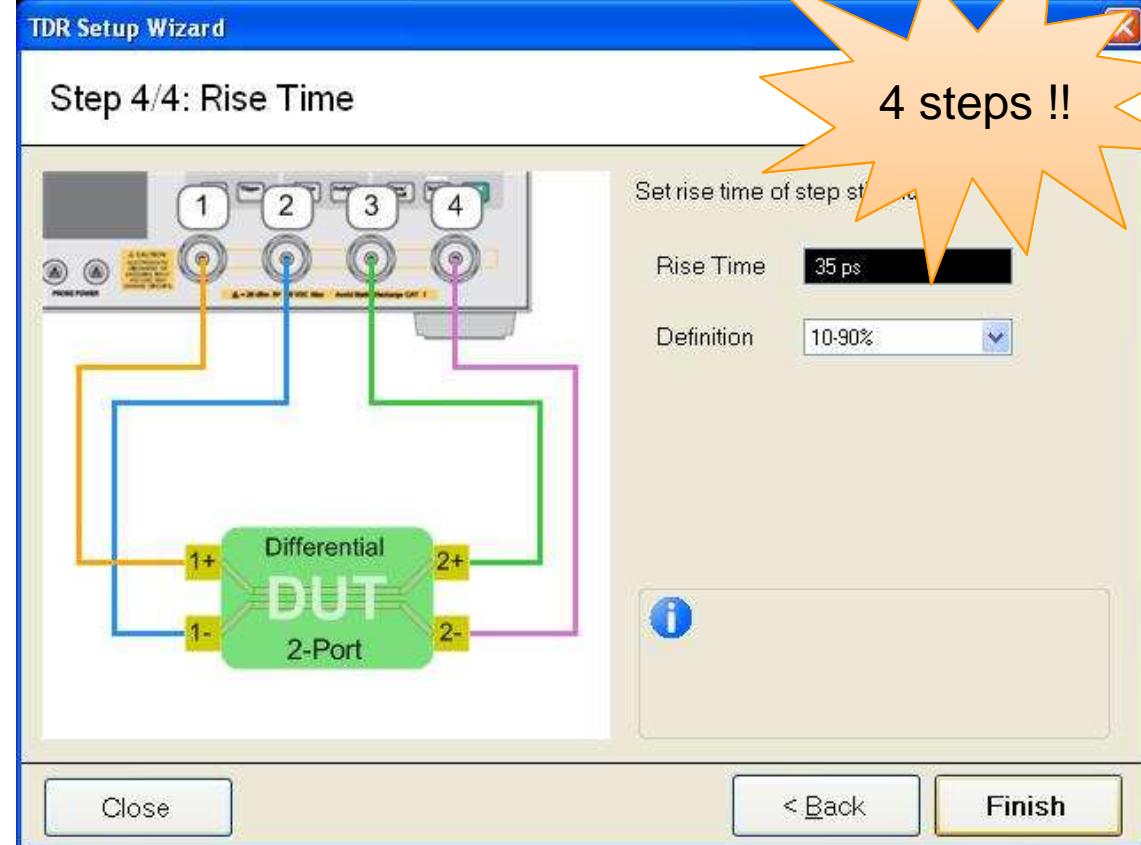
Fast & Accurate



ESD Robustness



## TDR Setup Wizard



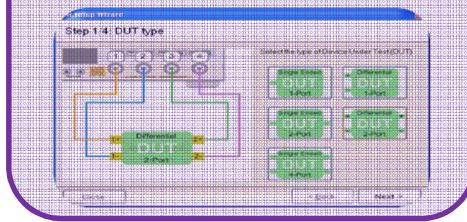
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# Signal Integrity Design & Verification

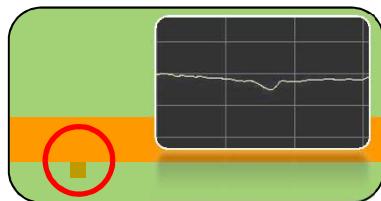


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Simple & Intuitive



Fast & Accurate

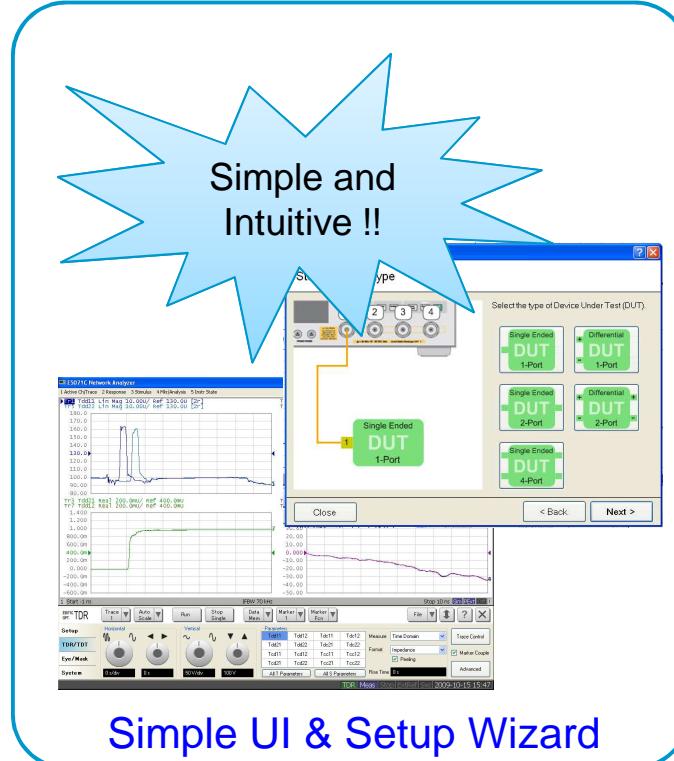


ESD Robustness



ENA Option TDR

Simple and  
Intuitive !!



Simple UI & Setup Wizard



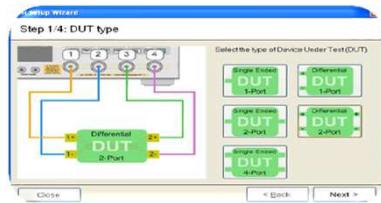
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# Signal Integrity Design & Verification

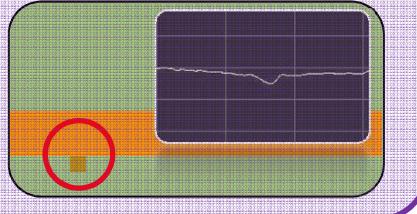


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Simple & Intuitive



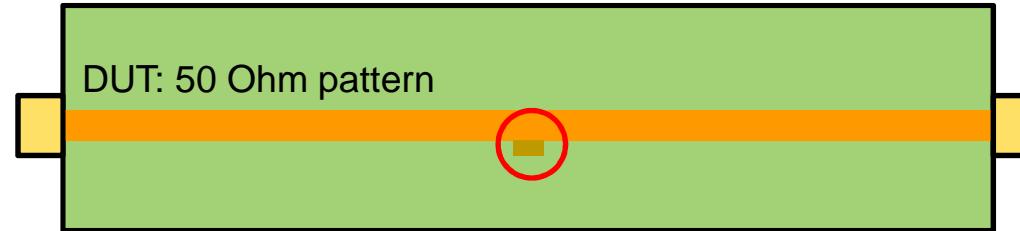
Fast & Accurate



ESD Robustness



DUT: 50 Ohm pattern



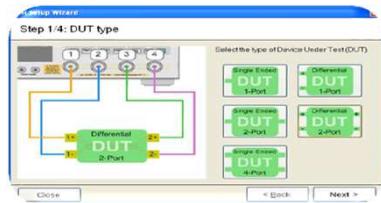
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# Signal Integrity Design & Verification

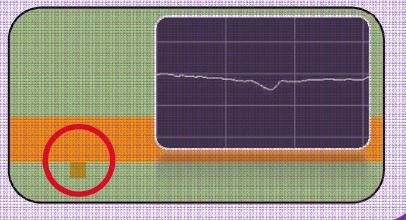


Unlocking Measurement Insights for 75 Years

## Simple & Intuitive



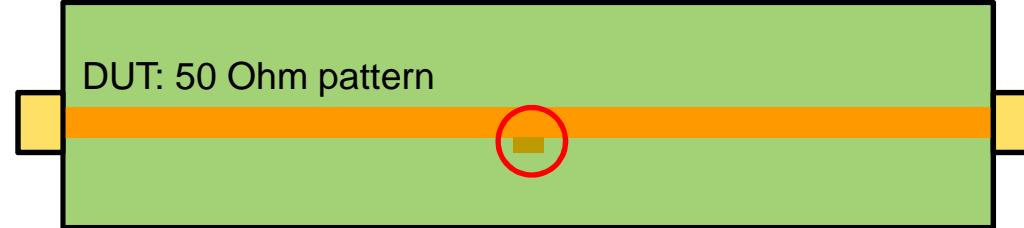
## Fast & Accurate



## ESD Robustness



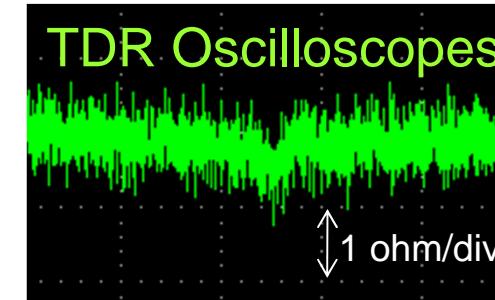
DUT: 50 Ohm pattern



ENA Option TDR



TDR Oscilloscopes



VNA Based TDR measurements  
= Low Noise



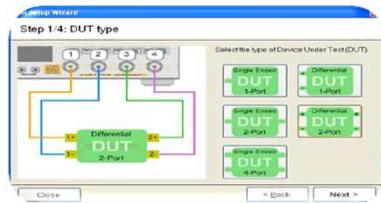
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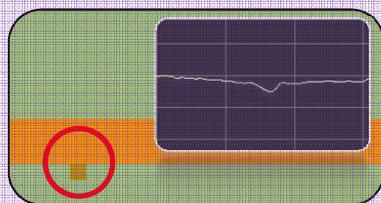


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Simple & Intuitive



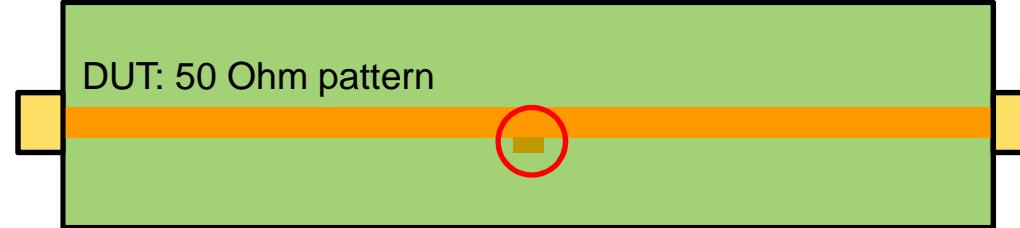
Fast & Accurate



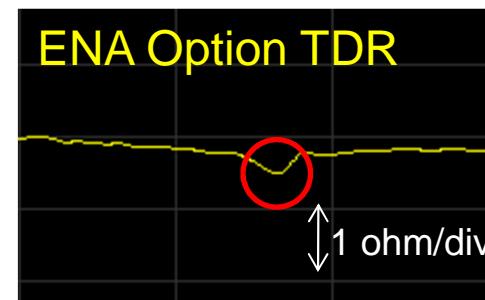
ESD Robustness



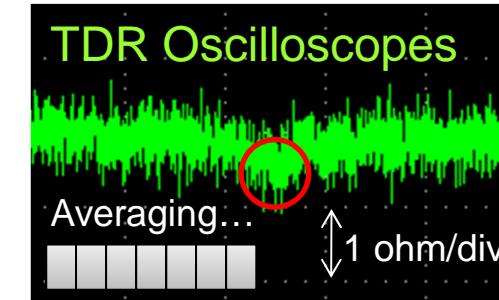
DUT: 50 Ohm pattern



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TDR Oscilloscopes



Averaging  
gives precise measurement

BUT...



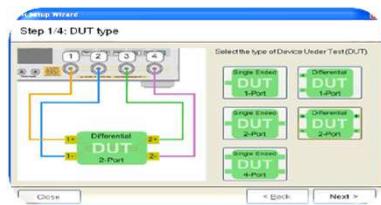
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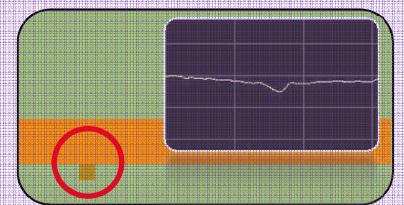


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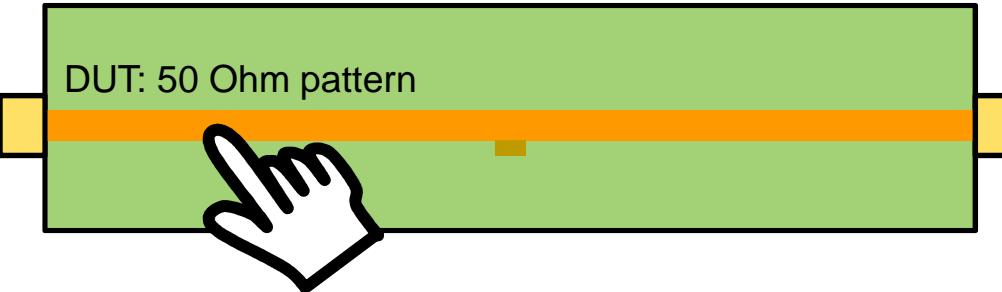
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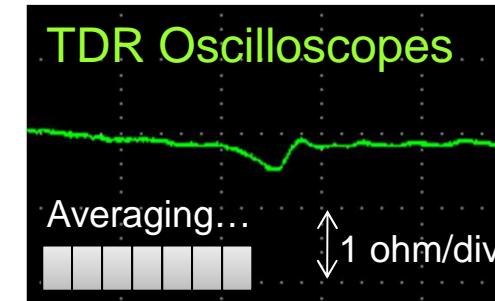
ESD Robustness



ENA Option TDR



TDR Oscilloscopes



Real-Time Analysis



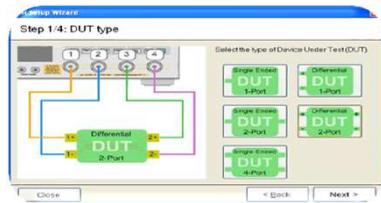
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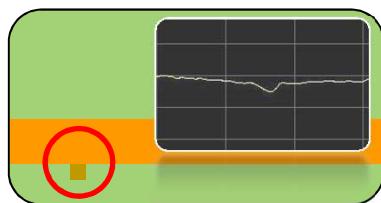


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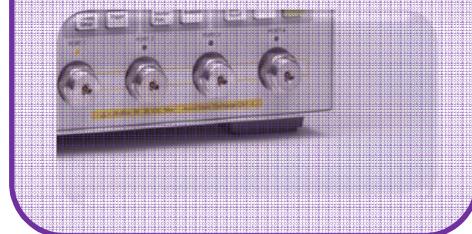
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ESD Robustness



## ESD Robustness



TDR oscilloscope is sensitive to ESD



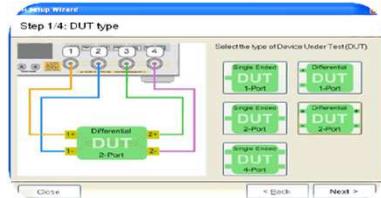
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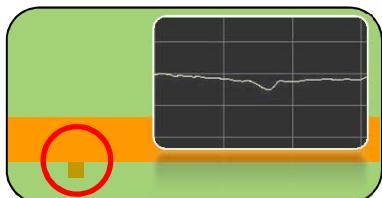


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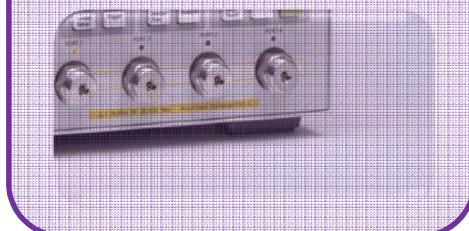
Simple & Intuitive



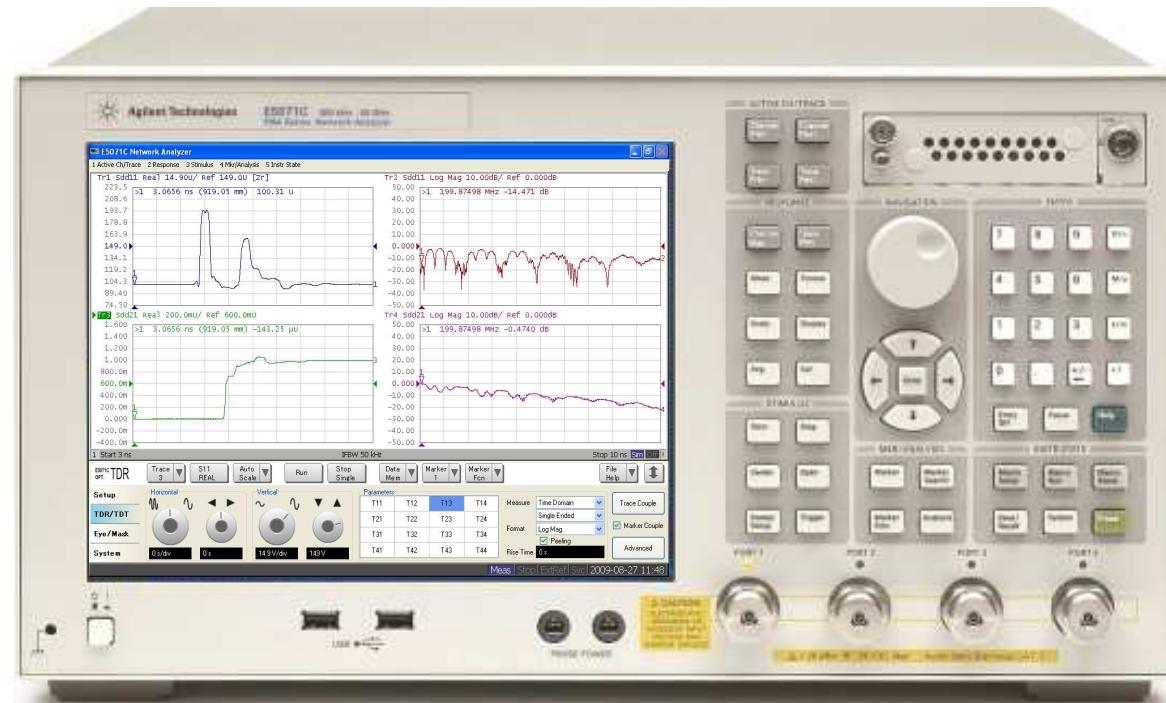
Fast & Accurate



ESD Robustness



## ESD Robustness



↑ ↑ ↑ ↑  
ESD protection circuit inside



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# Demo: Advanced TDR



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# AGENDA



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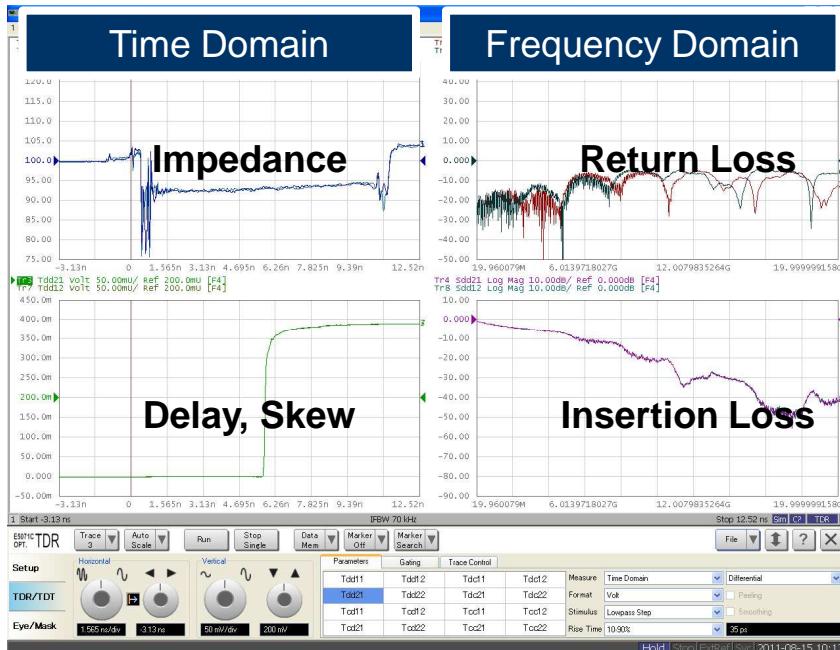
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# Parametric Characteristic are enough?

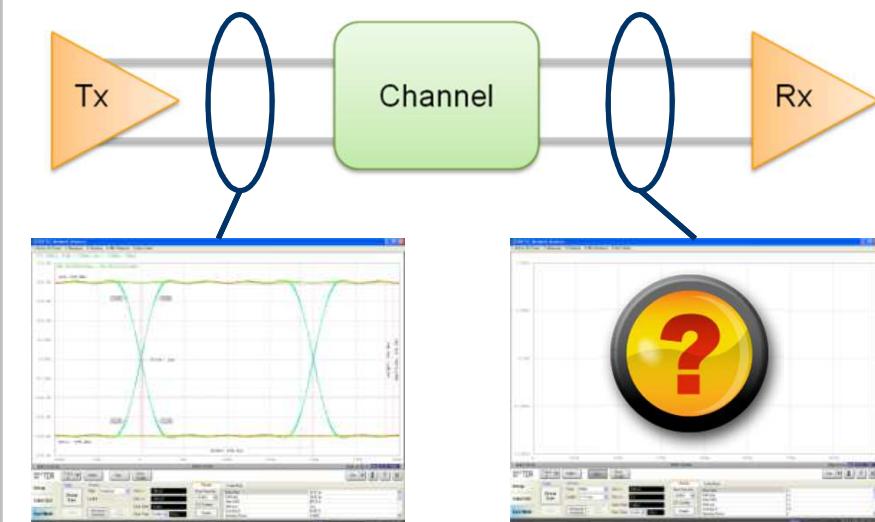


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Interconnects have traditionally been characterized by measuring parametric characteristics such as insertion loss and impedance.



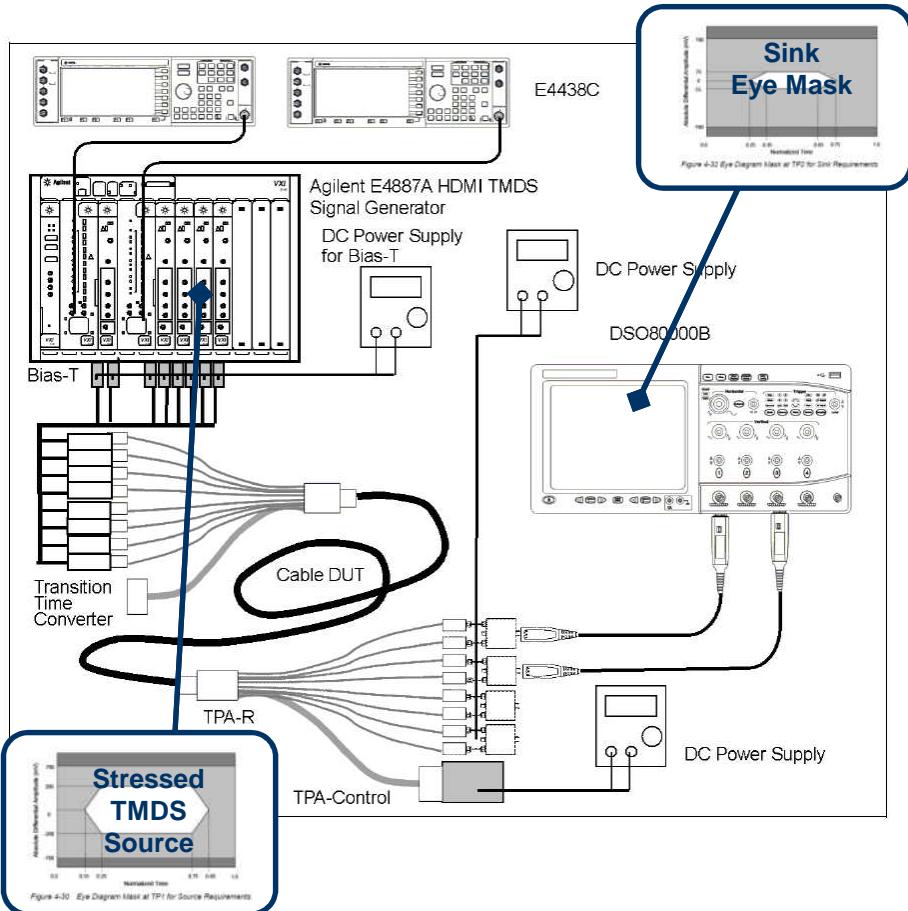
One challenge with such characterization is how to translate the measurements into what the eye diagram will look like at the end of a link....



# Traditional eye diagram



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## Many instruments...



How to setup for proper measurements?



Total solution cost?

## Only eye diagram measurements available...



How to troubleshoot and isolate root cause upon device failure?



# “Stressed” eye diagram testing on VNA

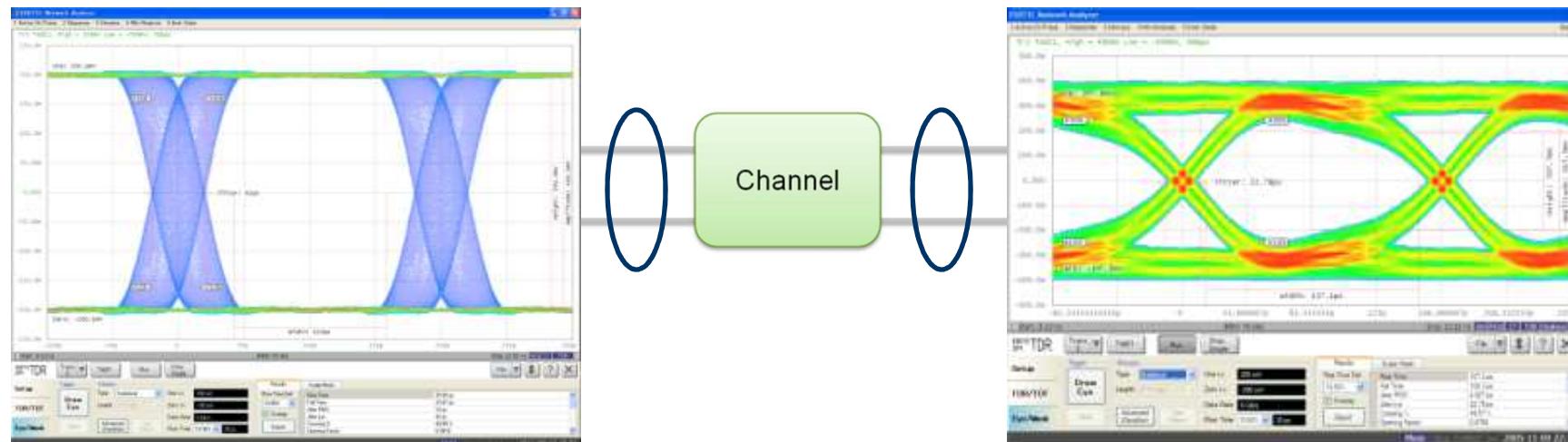


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Another approach is to characterize the interconnect using the eye diagram. This has the advantage of allowing direct measurement of eye characteristics at the end of the link. This process is called **“stressed” eye diagram testing**.

Input the expected worst case performance of the transmitter as the “stressed” signal to the interconnect...

... and evaluate the eye diagram at the output of the interconnect.

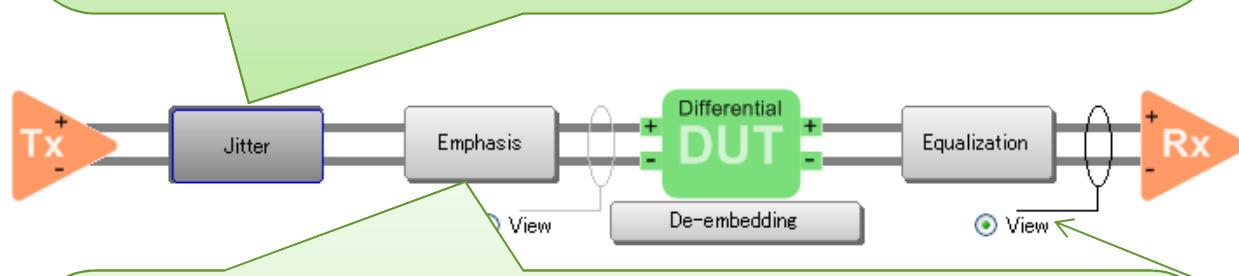
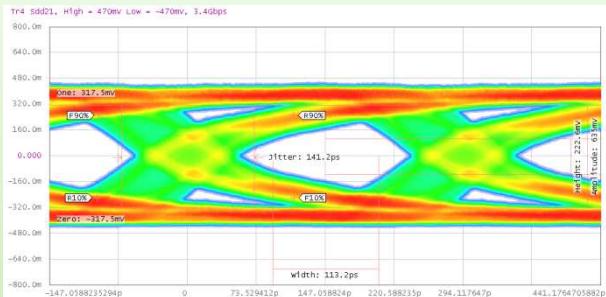


# Advanced Waveform Analysis

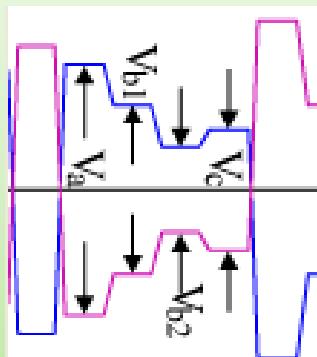


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**Jitter Injection** feature provides eye diagram test with a condition similar to the real implementation.



**Emphasis** is the intentional amplitude alteration of data signal to improve eye opening. The amplitude alterations are determined by the previous bits.



**Equalizer** is used for the same purpose as emphasis. It amplifies a particular frequency band to compensate the attenuation of DUT.

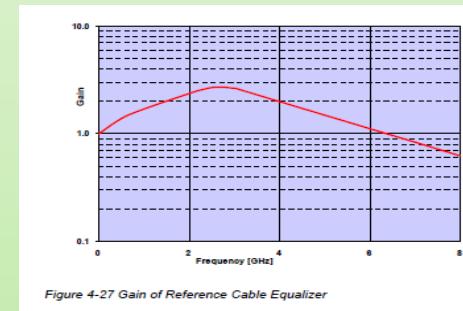


Figure 4-27 Gain of Reference Cable Equalizer



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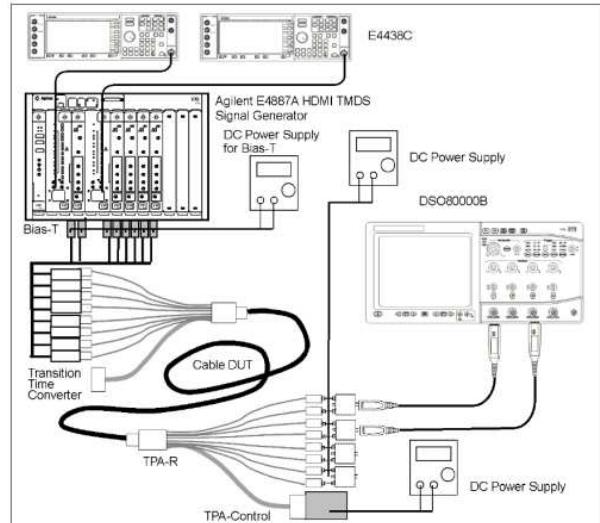
# Complete Characterization



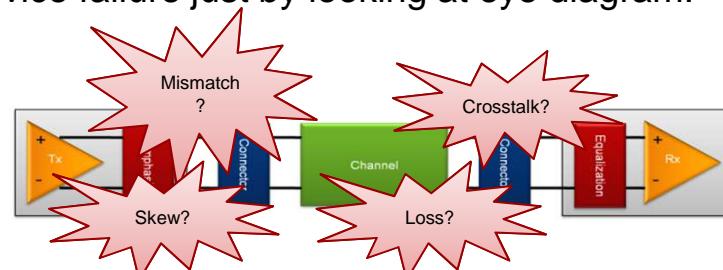
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## Traditional Solution

Only **stressed eye diagram** analysis available.

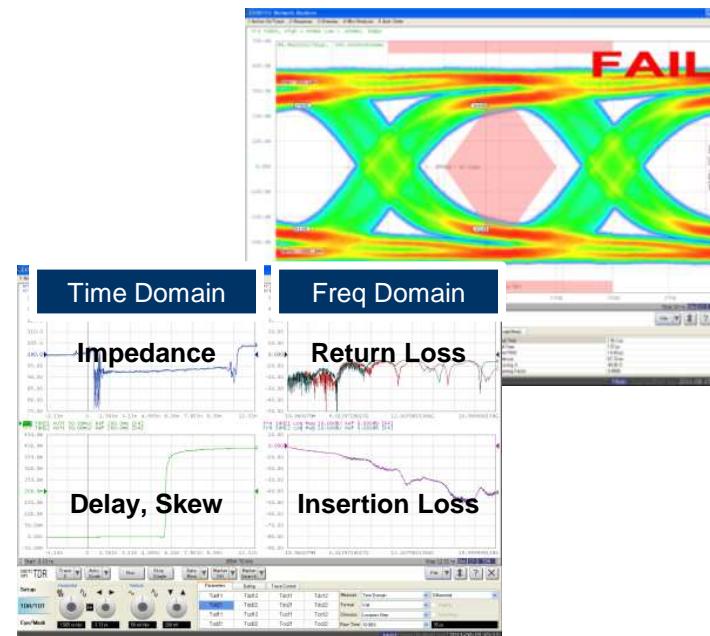


Difficult to troubleshoot and isolate root cause upon device failure just by looking at eye diagram.



## ENA Option TDR

Both **stressed eye diagram** and **parametric** analysis available.



Parametric tests provide insight into root cause of device failure.

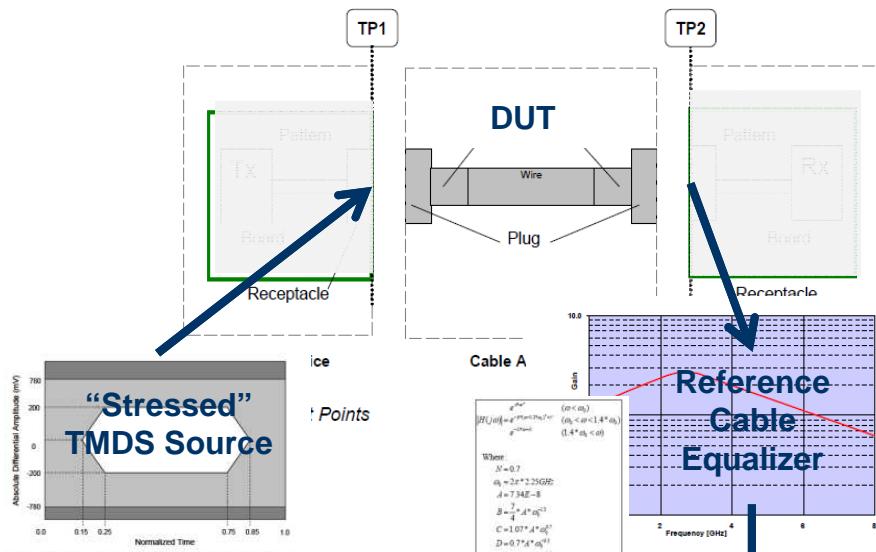
# Demo: HDMI1.4b



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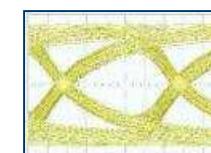
For HDMI Cable Assembly compliance test, there is the option of testing with either **parametric parameters**, or **stressed eye diagram (recommended)**.

## Stressed Eye Diagram Measurement Overview



1. Apply “stressed” source to DUT

2. Apply equalizer to DUT output.



3. Set eye mask and perform mask test

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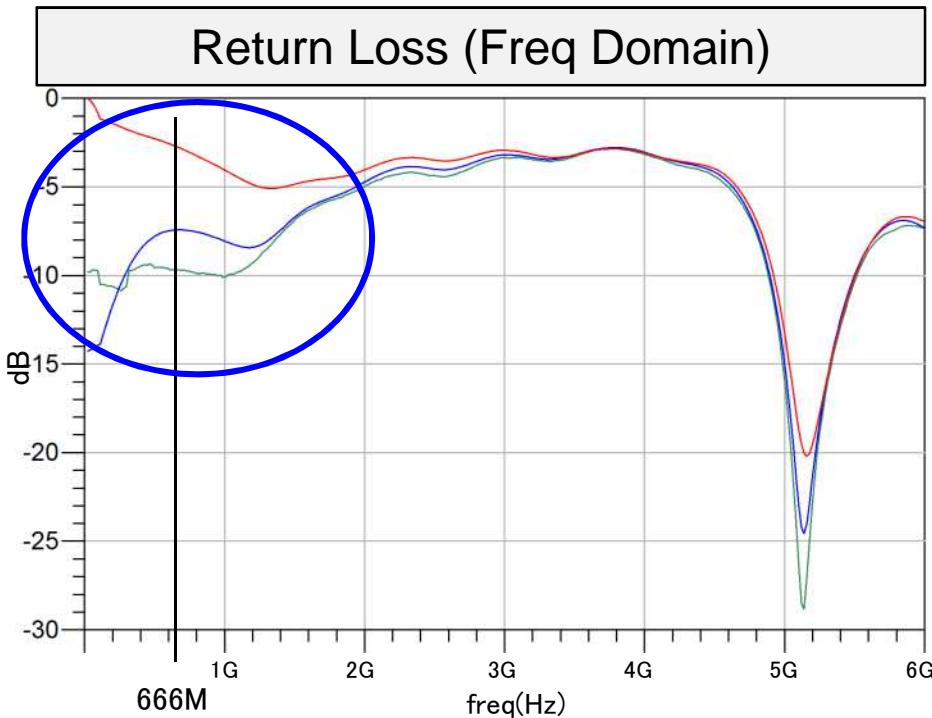
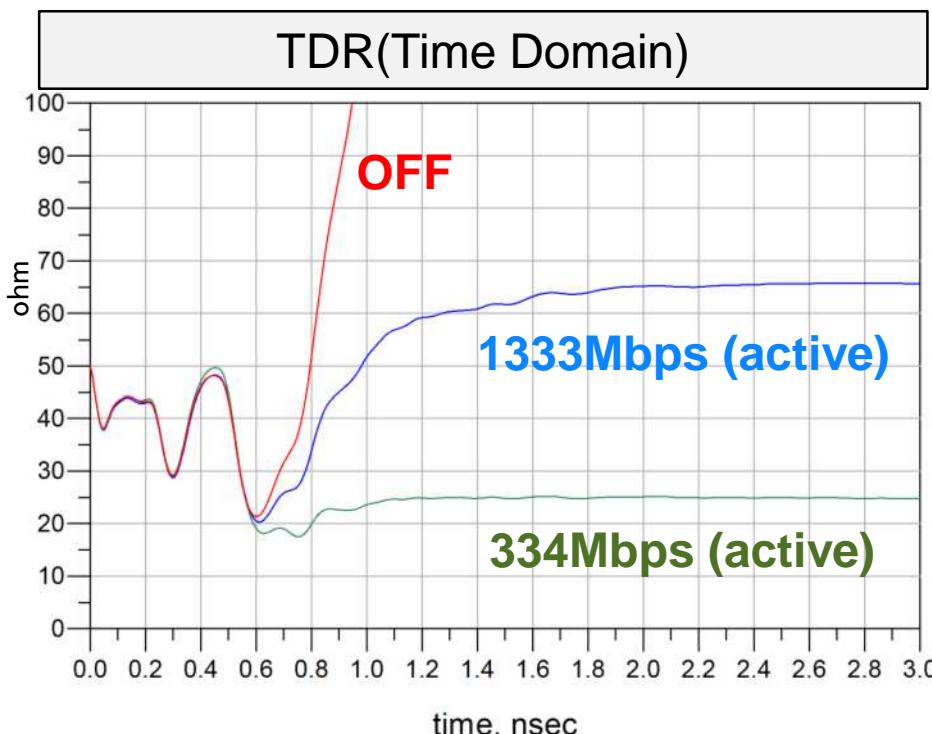
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# Why Measure Hot TDR?



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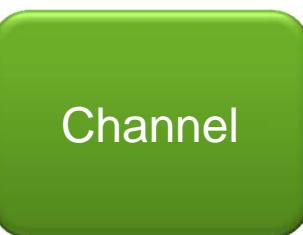
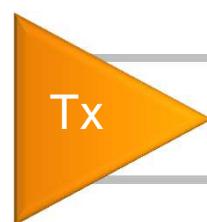
- Hot TDR measurement is the impedance analysis of active devices under actual operation conditions.
- Typically, impedance of the device in the OFF state and ON state (Hot TDR) is significantly different. Impedance may vary with the data rate as well.



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# Multiple Reflections

1. Signal transmitted from Tx ...



3. Re-reflection  
from Tx due to  
impedance  
mismatches ...

2. Partial reflection  
from Rx due to  
impedance  
mismatches ...

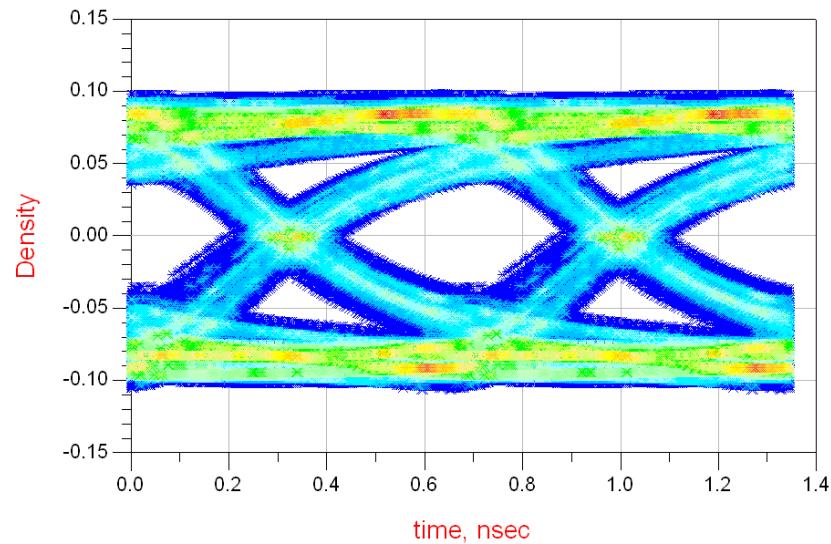


# Source Termination Effects

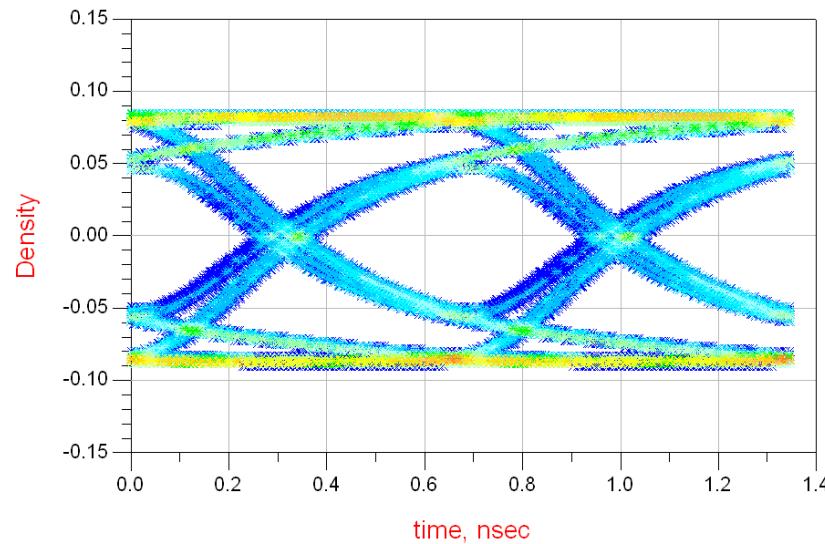


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Source Impedance **NOT** Matched



Source Impedance Matched



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# Many Standards Require Hot TDR



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## 7.4.13 Return Loss and Impedance Balance

### Transmitters (Tx):

When measuring output impedance of transmitters the operating condition shall be during transmission of **MFTP**. This is to assure the measurement is performed during a mode of operation that represents normal operation.

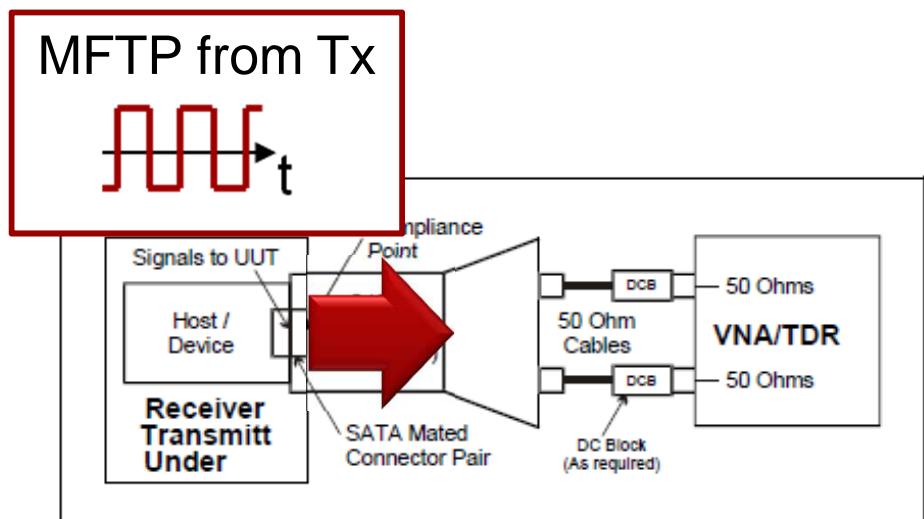


Figure 164 – Return Loss Test



### Measurement Challenge

How to avoid effects of the transmitter signal on measurements?

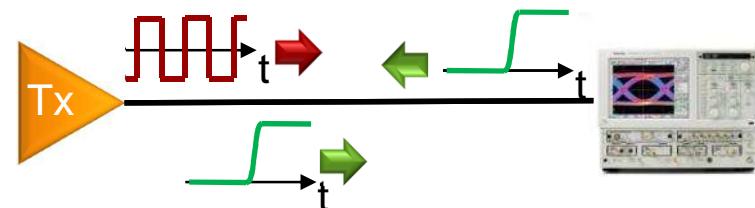


# Minimizing Errors from the Tx

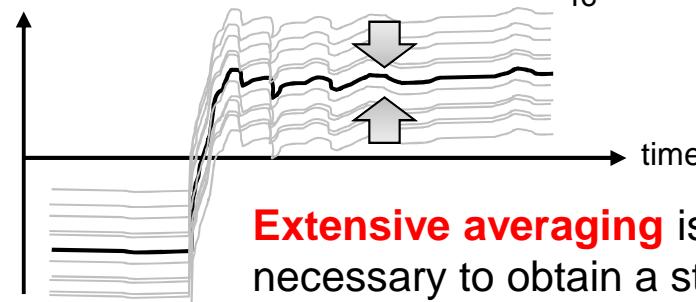
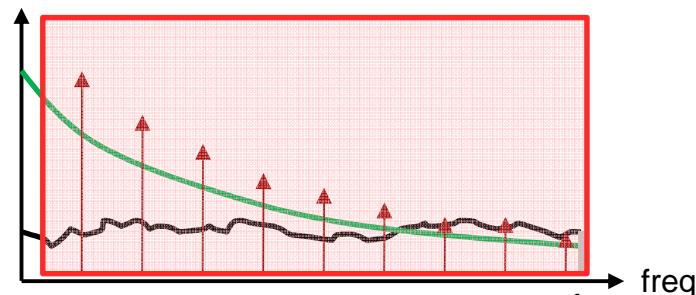


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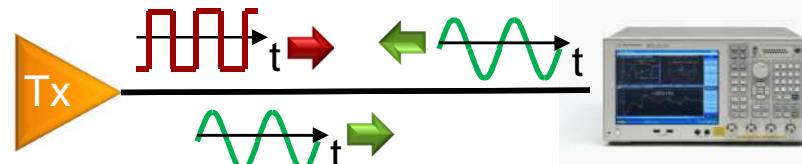
## TDR Scopes



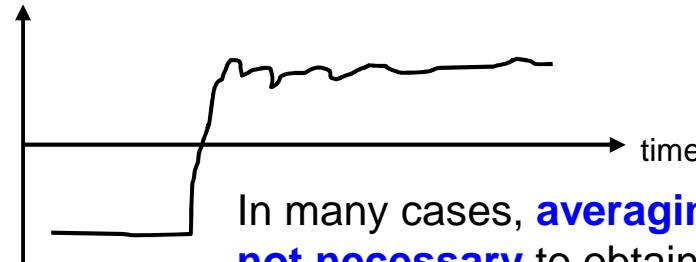
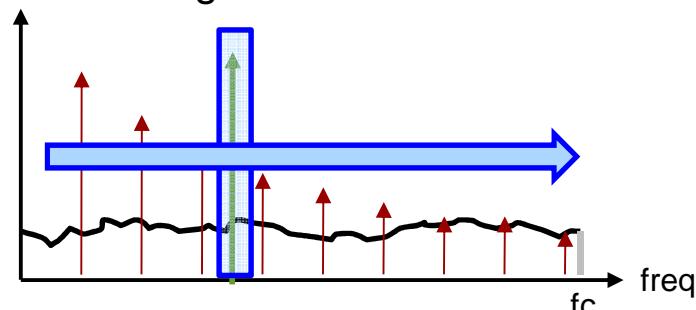
- **wideband receiver** captures all of the signal energy from the transmitter



## VNA



- **narrowband receiver** minimizes the effects of the data signal from the transmitter

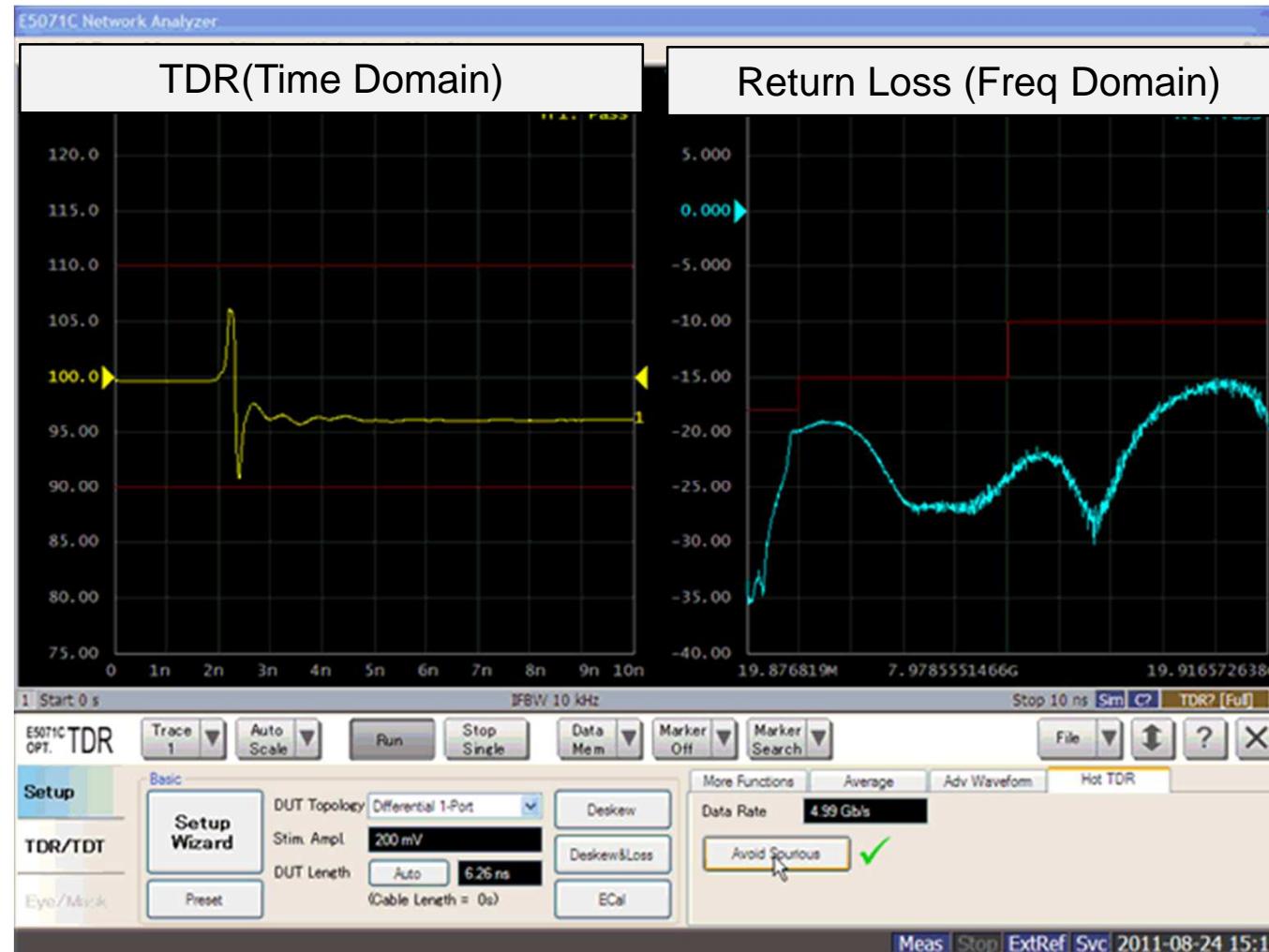


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# Demo: Hot TDR



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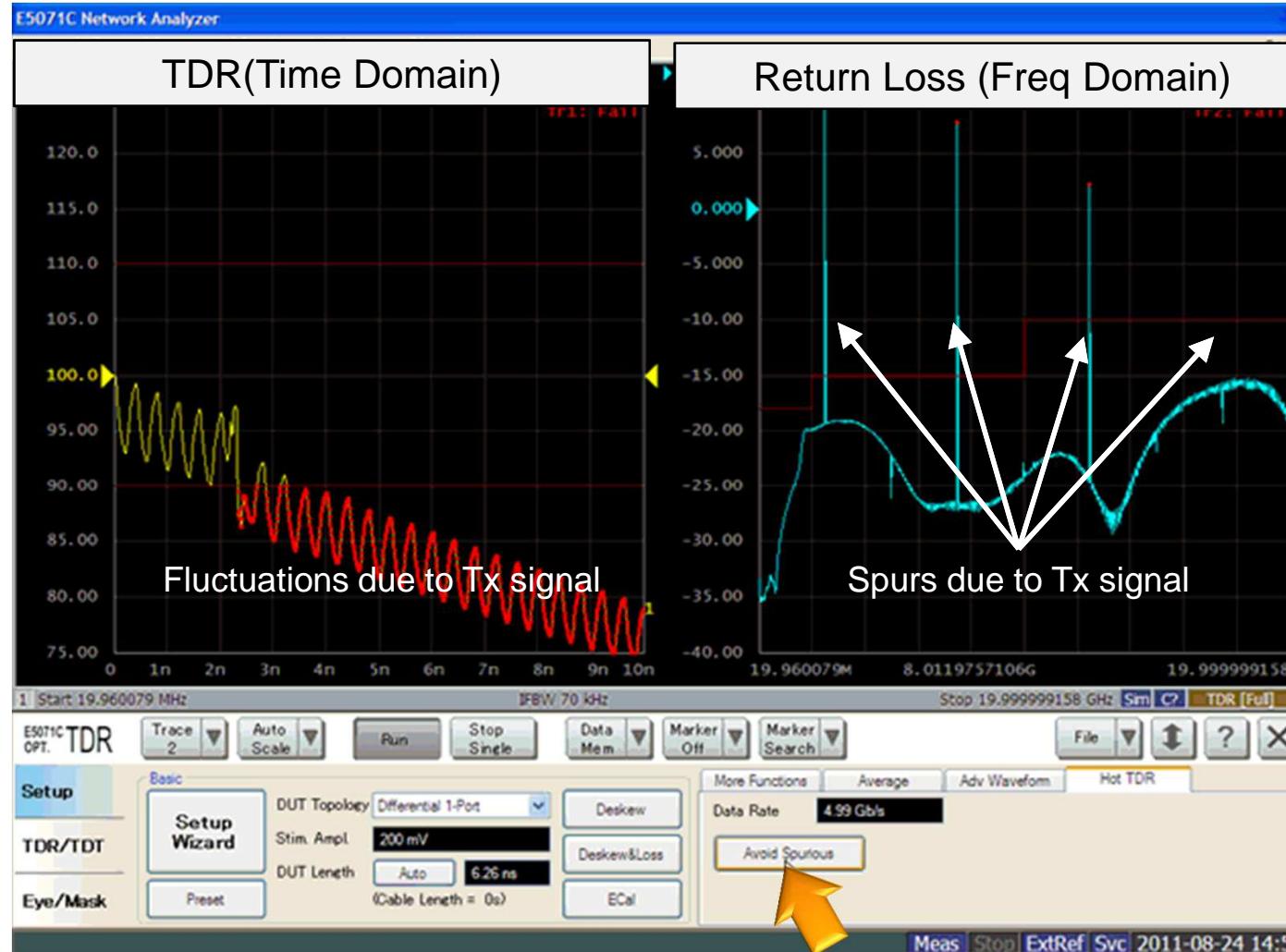


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# Avoid Spurious Feature



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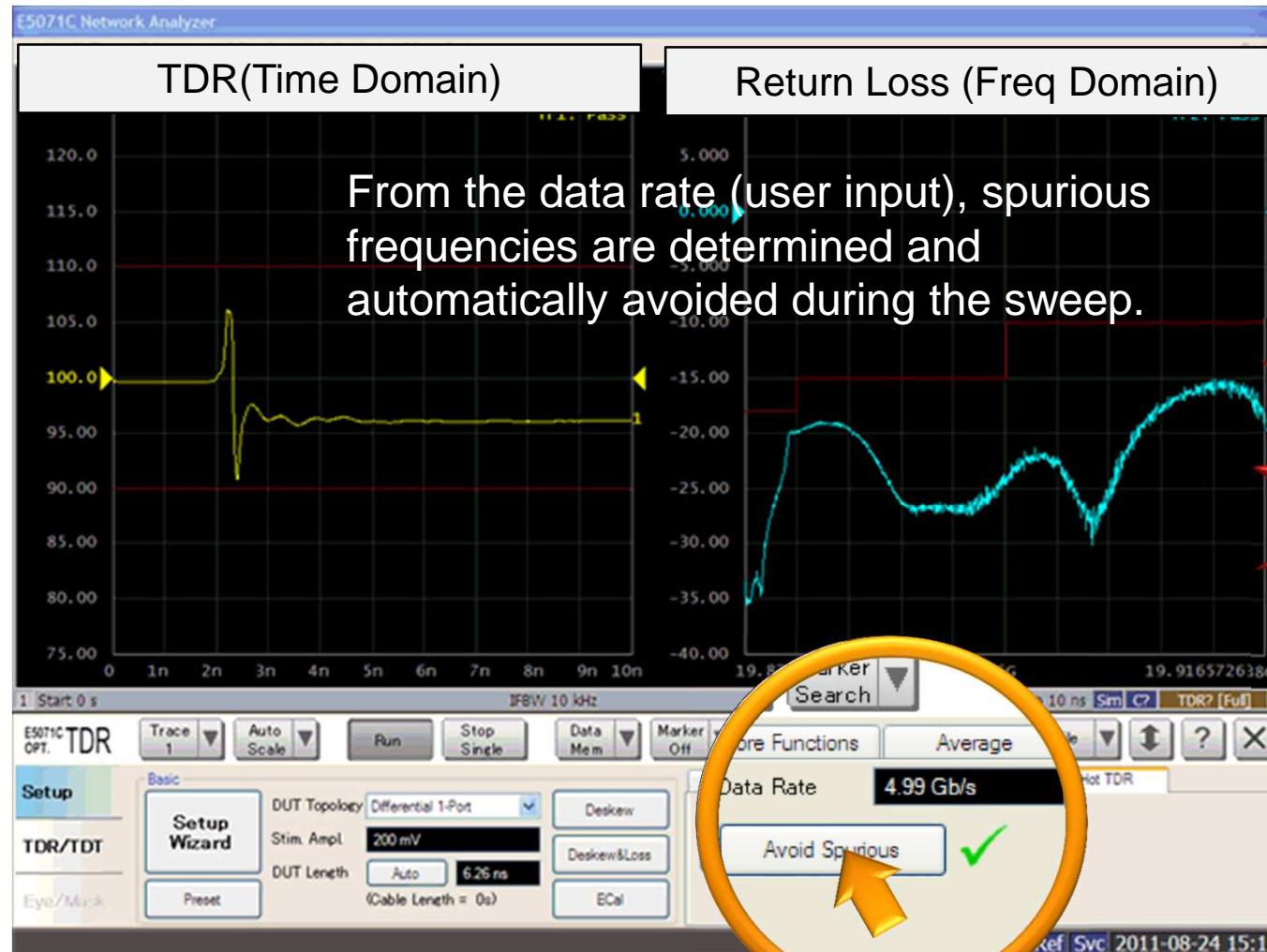


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# Avoid Spurious Feature



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# AGENDA



Unlocking Measurement Insights for 75 Years

- TDR based on VNAs
- Advanced TDR for Signal Integrity
- Stressed Eye Diagram Analysis
- Hot TDR Measurements
- **Compliance Support: MOIs**
- Correlation Data among VNA and Sampling Scopes



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# Compliance Support



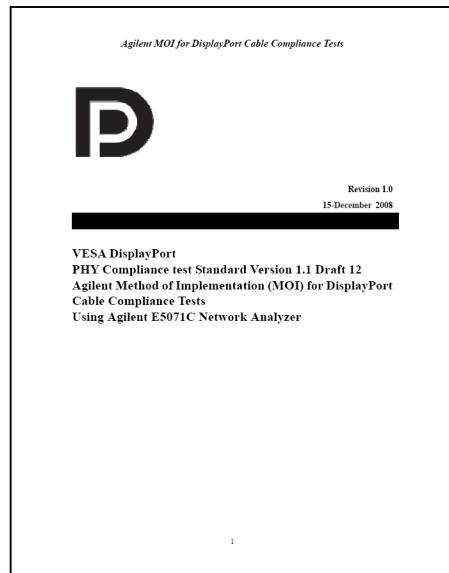
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→ Examples:



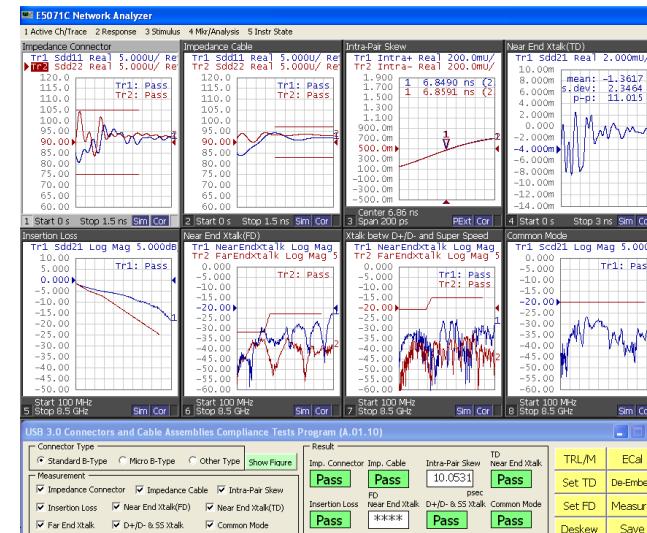
- E5071C Method of Implementation (MOI)

[Example] [Display Port](#) Cable Compliance Test



- VBA program and operation guide, mask tests, limits, states...

[Example] [USB3.0](#) Cable measurement using the VBA program



# Compliance Support

Standards supported by E5071C-TDR

Standards		MOIs & State Files		Test Solution Overview
		Cable-Connector Assembly	Source-Sink	
USB	USB3.0	Available	-	Available
	USB3.1	Coming soon...	-	Coming soon...
HDMI	HDMI 1.4b	Available	-	Available
	HDMI 2.0	(*2)	Coming soon...	Coming soon...
SATA		Available	Available	Available
DisplayPort		Available	-	Available
MIPI™	D-PHY	-	Available	Available
	M-PHY	-	Available	Available
Ethernet	100BASE-TX	Available	-	Available
	10GBASE-T	Available	-	Available
MHL		Available	Coming soon...	Available
PCIe®		Available	-	Available
Thunderbolt®		-	Available (*1)	Available
BroadR-Reach®		Available (*1)	-	Available

\*1: Contact Agilent sales representative for more detail.

\*2: HDMI 2.0 uses the same cable as HDMI 1.4b.



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Refer to following link for further information:

<http://www.home.agilent.com/agilent/editorial.jspx?cc=US&lc=eng&ckey=2022953&nid=-11143.0.00&id=2022953>



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# AGENDA



Unlocking Measurement Insights for 75 Years

- TDR based on VNAs
- Advanced TDR for Signal Integrity
- Stressed Eye Diagram Analysis
- Hot TDR Measurements
- Compliance Support: MOIs
- **Correlation Data among VNA and Sampling Scopes**



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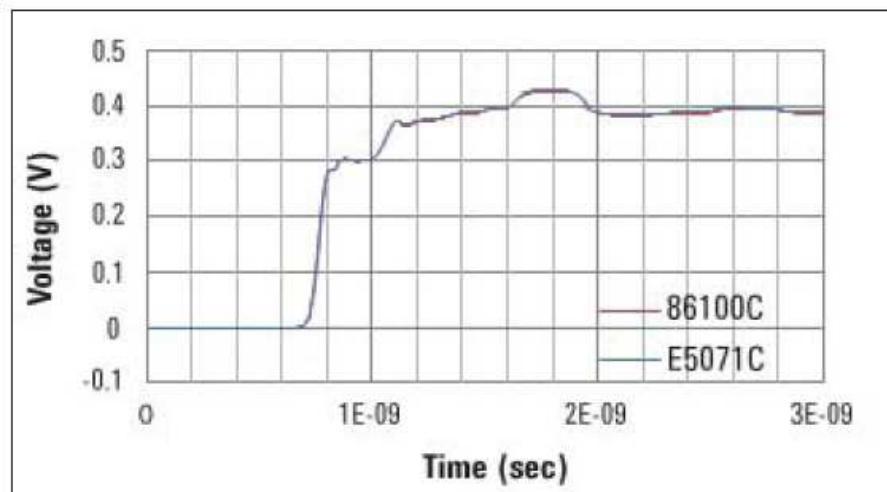
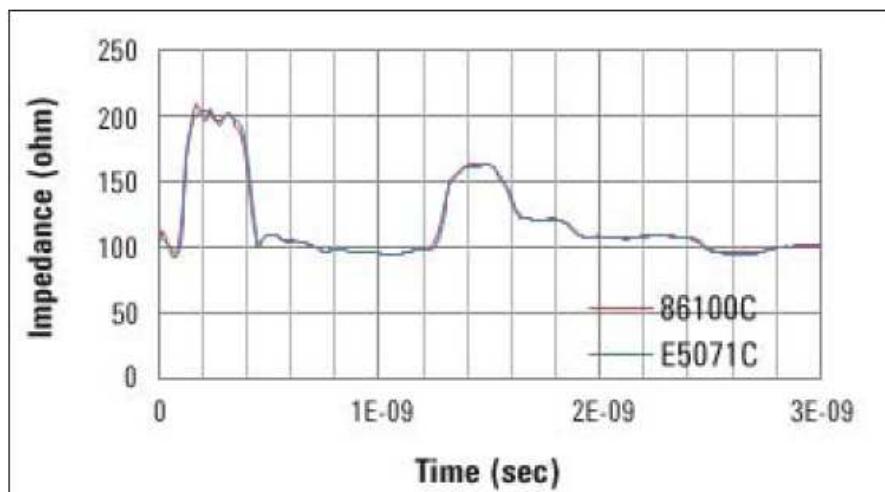
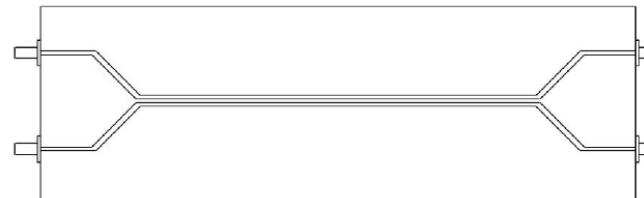
# Measurement Correlation

## TDR/TDT



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- DUT: Differential PCB trace
- 35 ps rise time (10-90%)



NOTE: For further details, refer to Application Note, "Correlation between TDR oscilloscope and VNA generated time domain waveform" (5990-5238EN)



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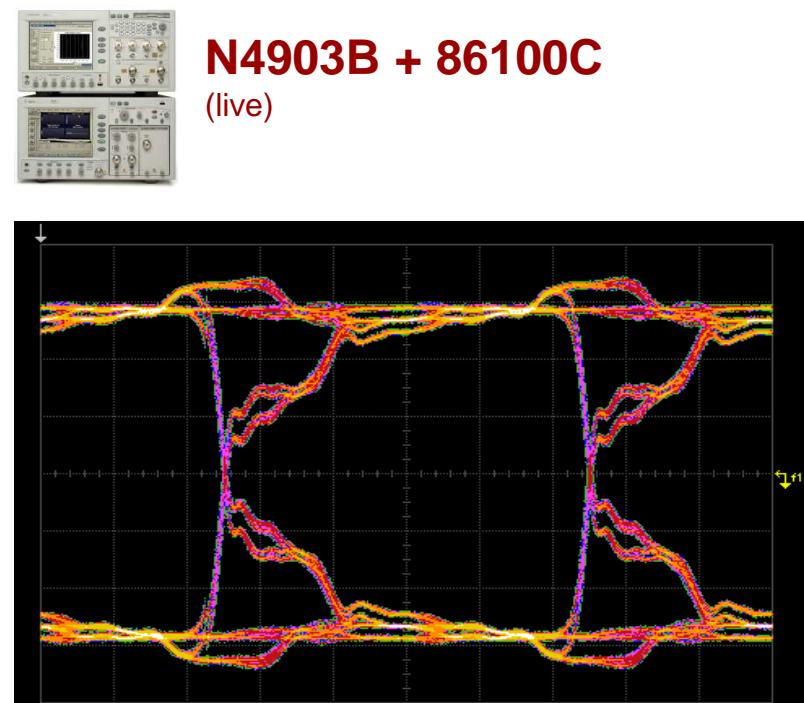
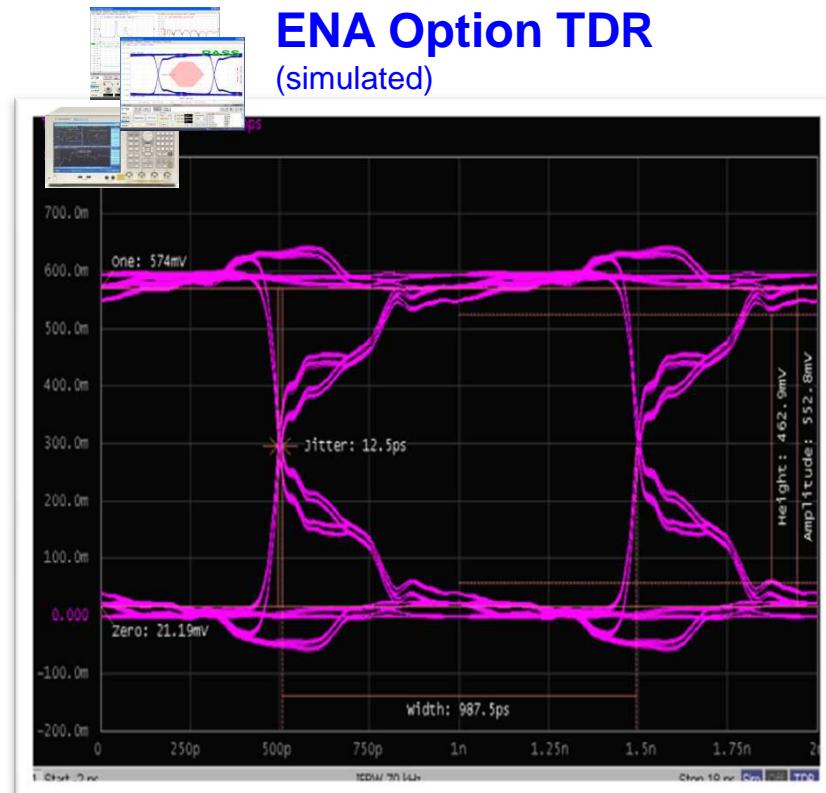
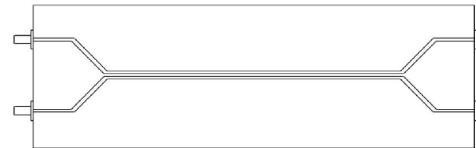
# Measurement Correlation

## Eye Diagram

- DUT: differential PCB trace
- PRBS (2<sup>7</sup>-1) @ 1 Gbps



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NOTE: For further details, refer to Application Note, "Correlation between TDR oscilloscope and VNA generated time domain waveform" (5990-5238EN)



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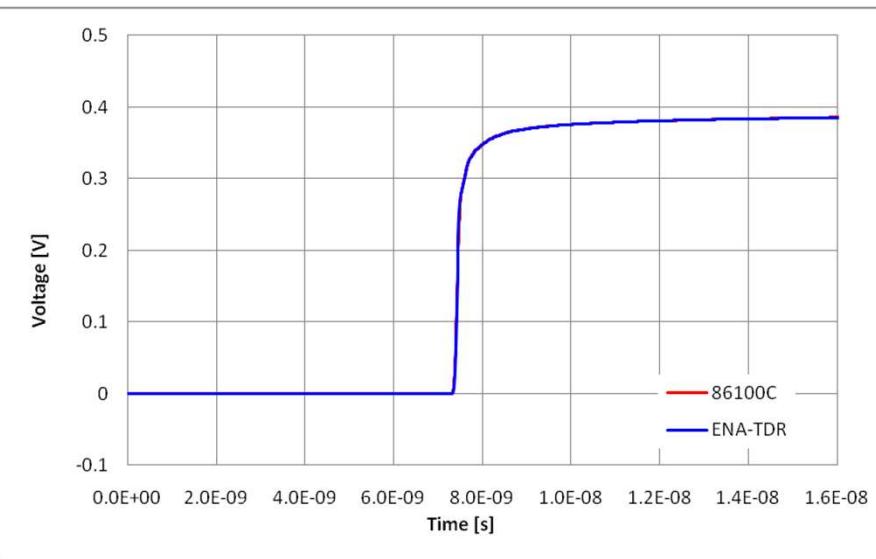
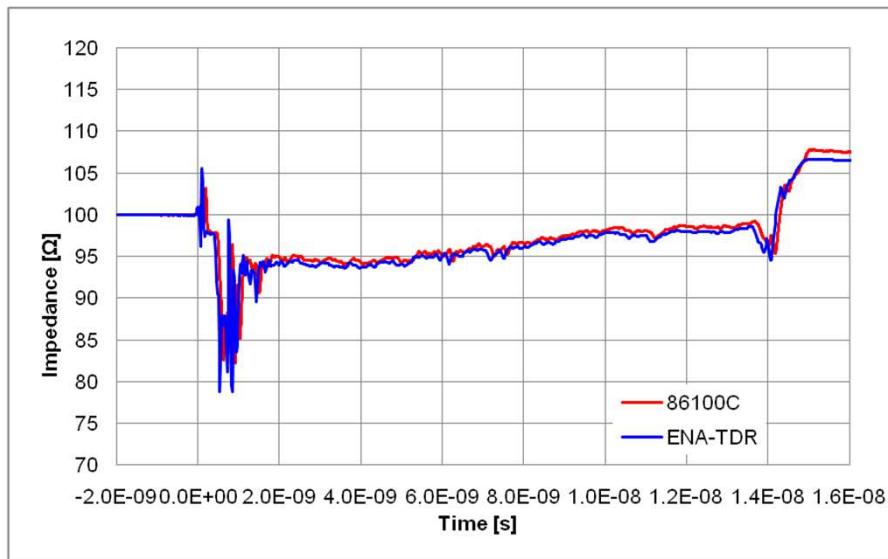
# Measurement Correlation

## TDR/TDT



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- DUT: USB3.0 Cable
- 50 ps rise time (20-80%)

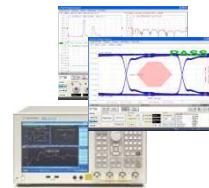


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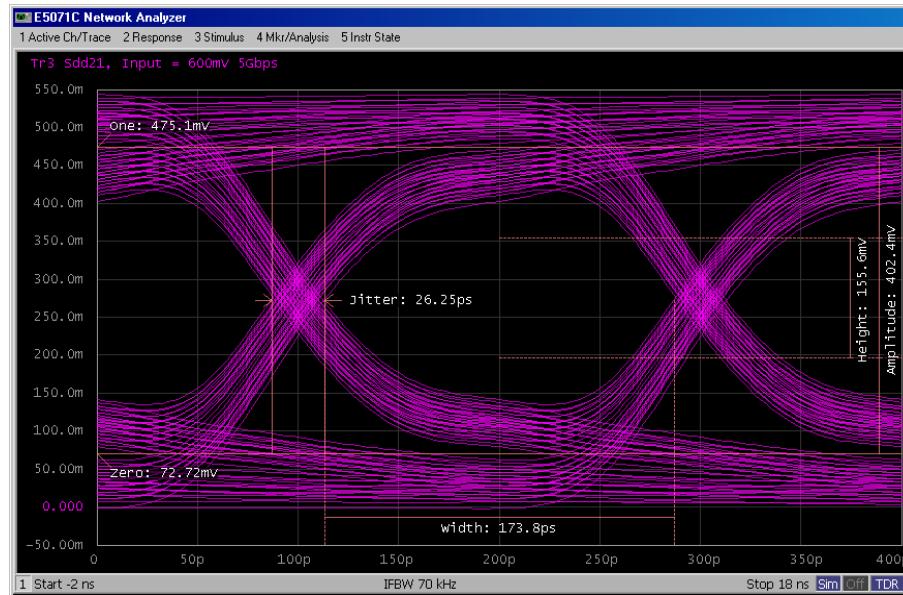
# Measurement Correlation

## Eye Diagram

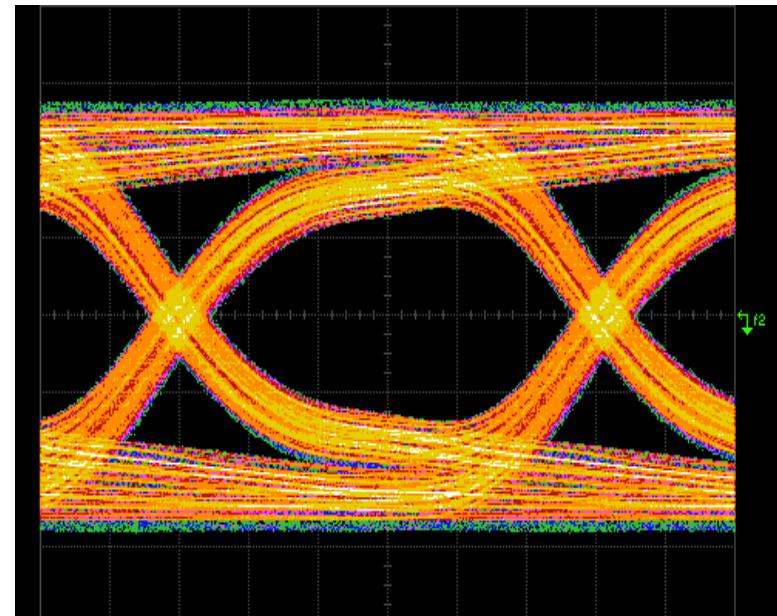
- DUT: USB3.0 Cable
- PRBS (2<sup>7</sup>-1) @ 5 Gbps



**ENA Option TDR**  
(simulated)



**N4903B + 86100C**  
(live)



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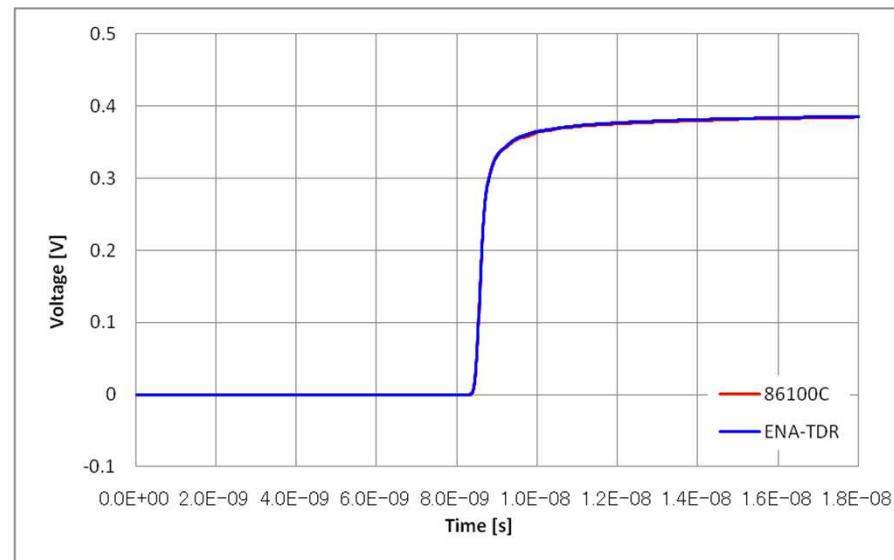
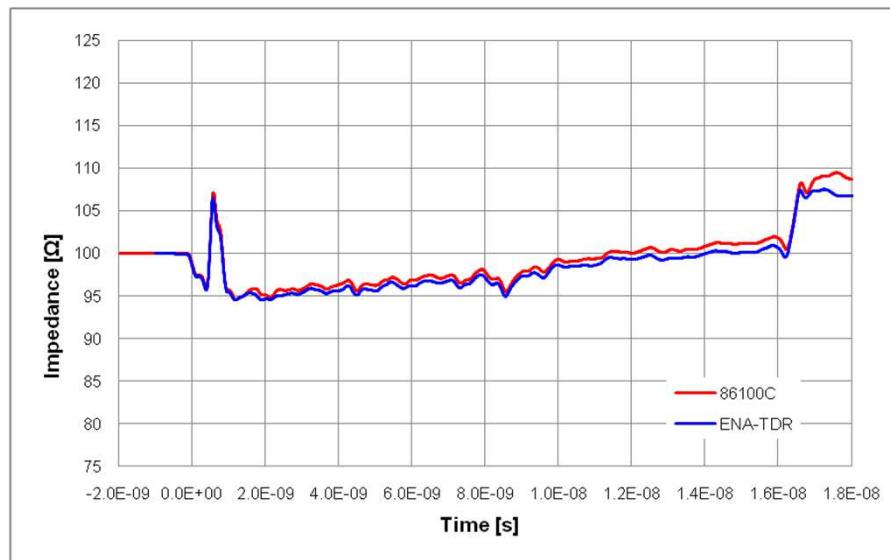
# Measurement Correlation

## TDR/TDT



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- DUT: DisplayPort Cable
- 130 ps rise time (20-80%)

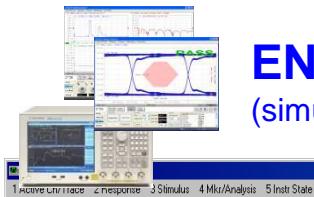


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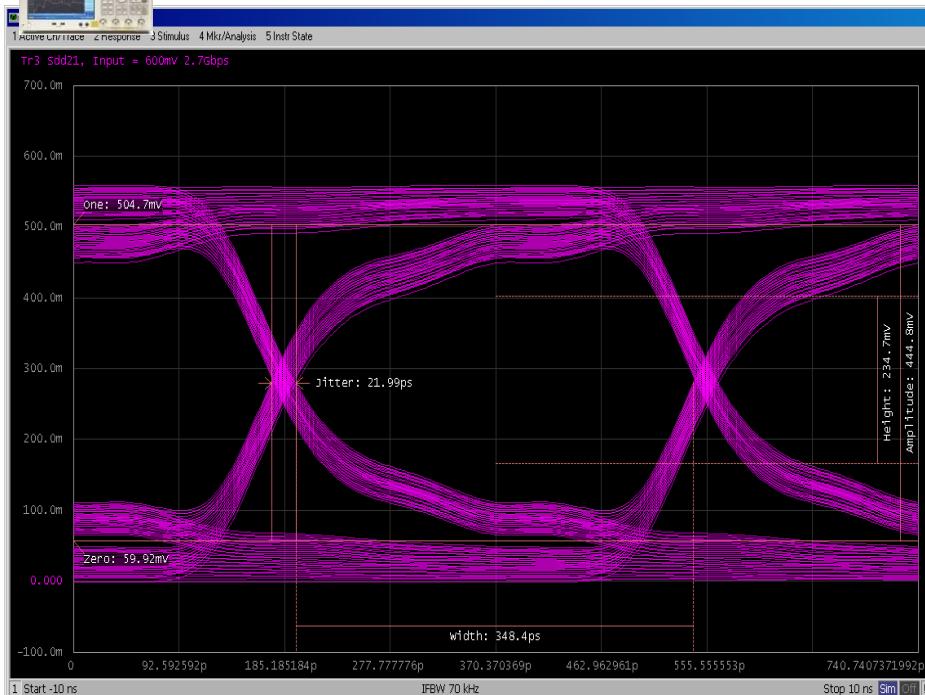
# Measurement Correlation

## Eye Diagram

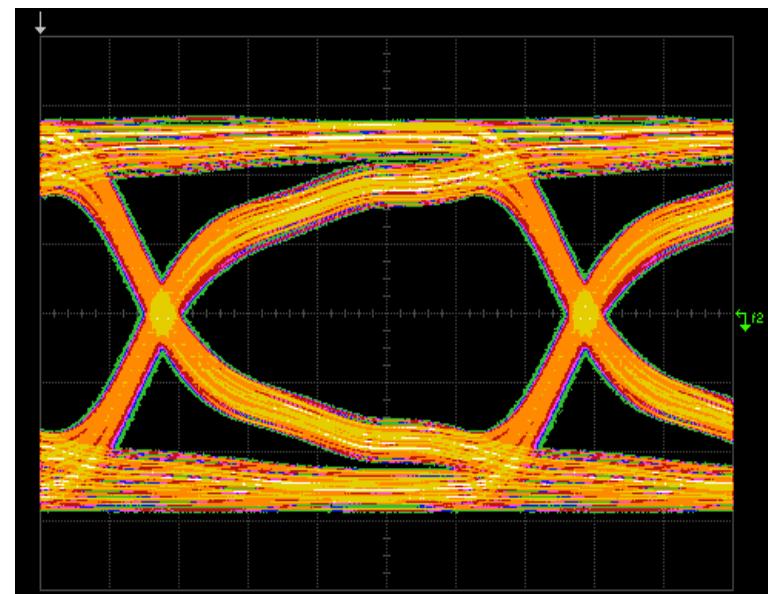
- DUT: DisplayPort Cable
- PRBS (2<sup>7</sup>-1) @ 2.7 Gbps



**ENA Option TDR**  
(simulated)



**N4903B + 86100C**  
(live)



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# Measurement Correlation

## TDR/TDT

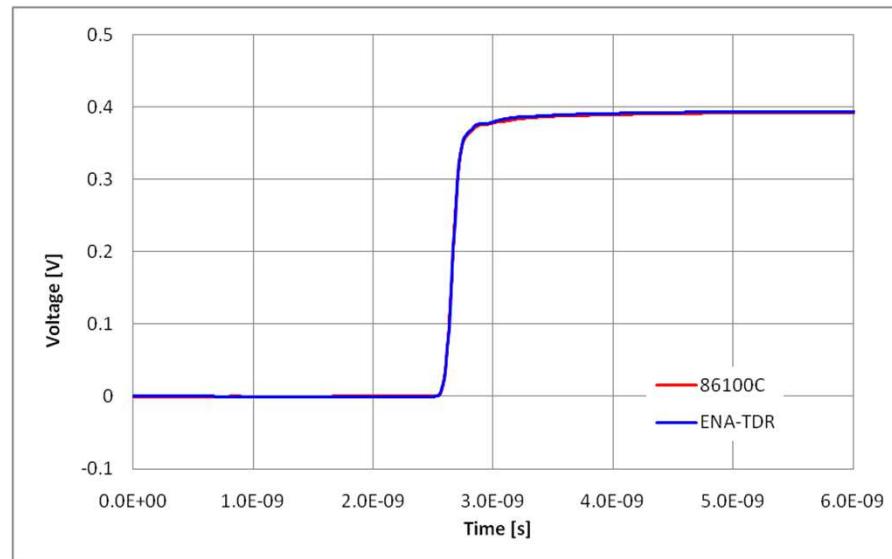
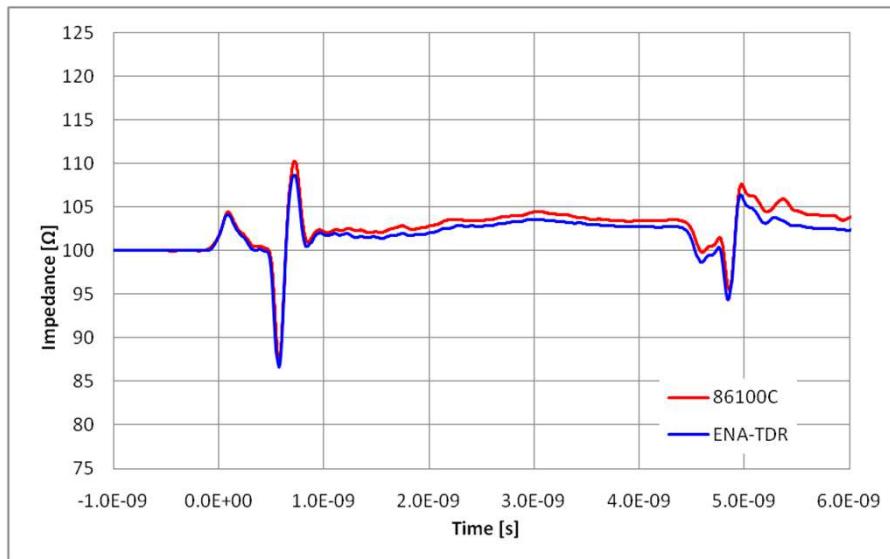


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- DUT: SATA Cable
- 70 ps rise time (20-80%)



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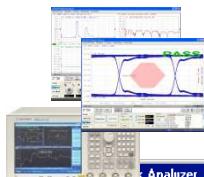
# Measurement Correlation

## Eye Diagram

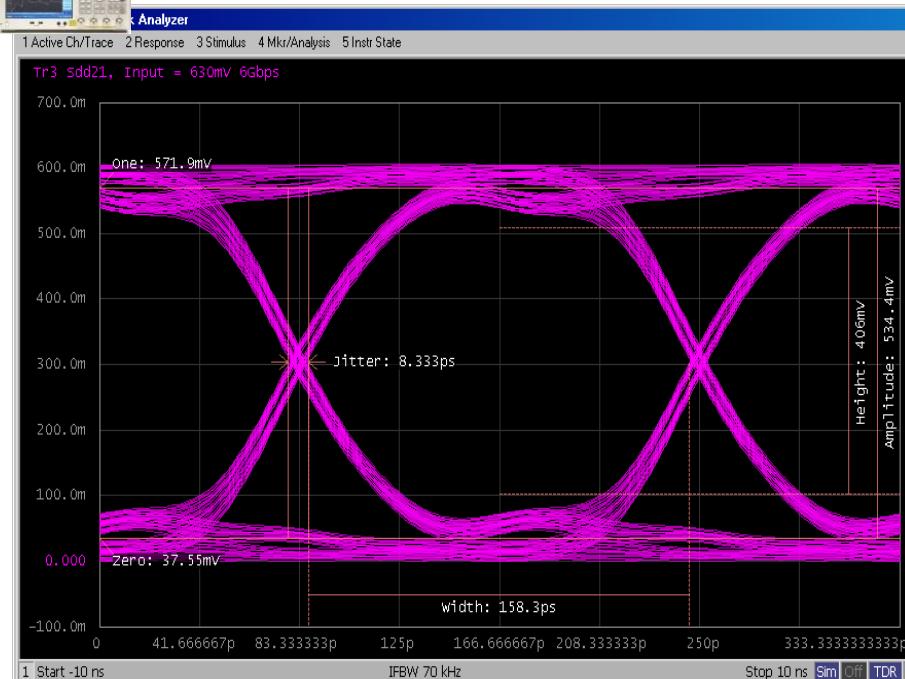
- DUT: SATA Cable
- PRBS (2<sup>7</sup>-1) @ 6 Gbps



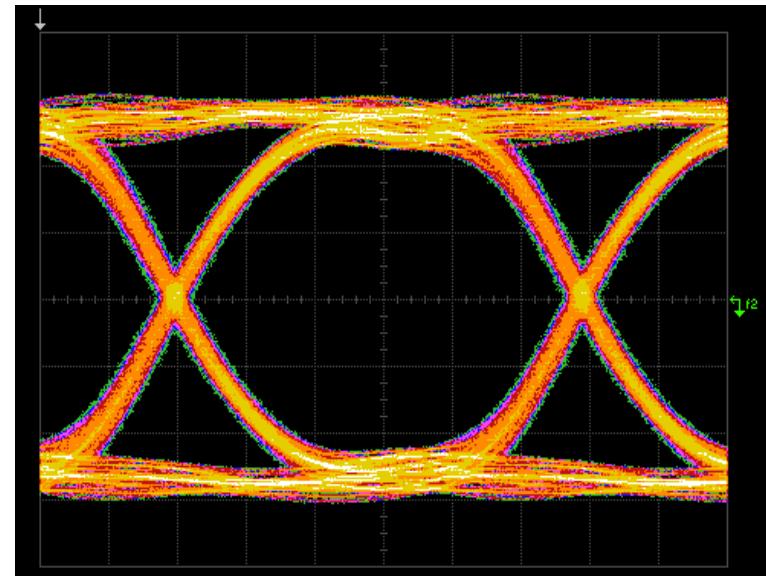
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**ENA Option TDR**  
(simulated)



**N4903B + 86100C**  
(live)



Application Note: <http://cp.literature.agilent.com/litweb/pdf/5990-5238EN.pdf>



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