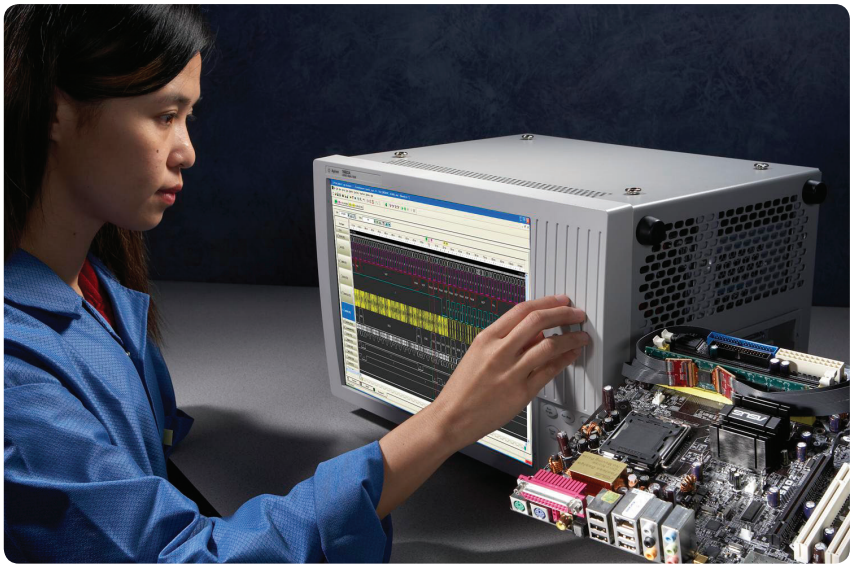
Agilent B4622B DDR/2/3/4 and LPDDR/2/3 Protocol Compliance and Analysis Toolset

Data Sheet

Features

- Automated real-time and post process DDR/2/3/4 or LPDDR/2/3 protocol compliance measurements.
- Identifies DDR/2/3/4 or LPDDR/2/3 state machine, protocol compliance, and protocol level bus cycle timing violations.
- Customizable real-time compliance tests.
- DDR standard preset tests allow user to edit parameters.
- Provides a quick overview of the DDR/2/3/4 or LPDDR/2/3 bus performance with statistical and histogram views for bus optimization purposes.
- Enables fast physical address trigger setup with trigger tool.



Achieve greater insight faster using the B4622B Protocol Compliance and Analysis toolset for DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, or LPDDR3.

DDR Memory measurement and debug work has become more complex and time consuming over the years as data rates increase and the architecture becomes more advanced. The B4622B provides four software tools in one toolset covering:

- Automated real-time compliance violation capture
- Post process compliance violation detection on captured traces
- Performance measurements
- Physical address trigger creation

These four tools help to quickly identify protocol problem areas and also give an overview of system performance.

Real-Time DDR/2/3/4 or LPDDR/2/3 Compliance ApplicationTool

The B4622B offers a new automated Real-Time Compliance Application tool to detect and capture state machine, protocol compliance, and protocol level bus cycle timing violations for DDR/2/3/4 or LPDDR/2/3. Real-time violation detection is an important advancement in DDR memory debug and validation. Monitoring your DDR bus real-time means the Agilent Logic Analyzer will trigger if the violation being checked ever occurs in the time specified in the software tool.

Beyond monitoring your DDR/2/3/4, or LPDDR/2/3 system real-time for elusive violations, designers can also monitor other digital system continuously for elusive, intermittent violations in protocol compliance or bus level timing.

Real-time testing enables:

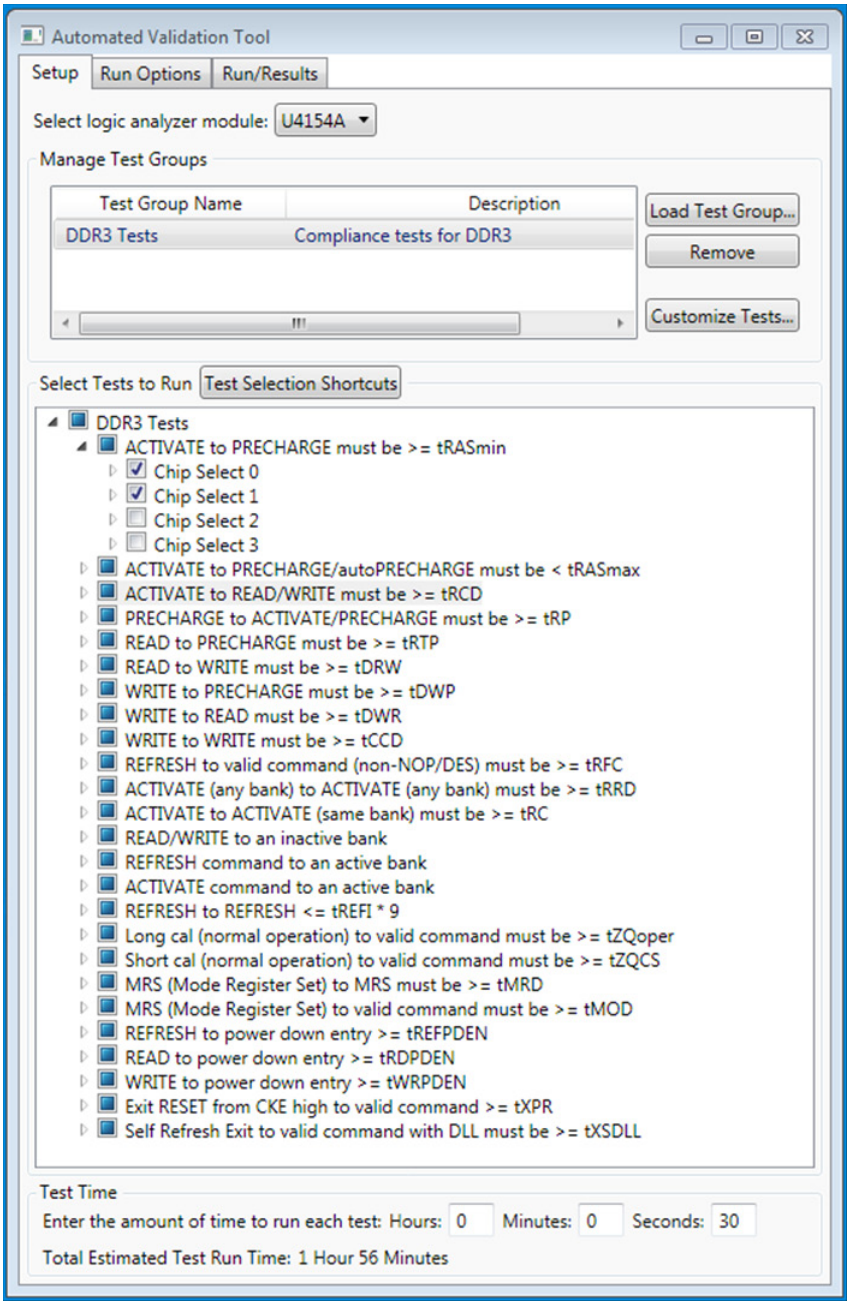
- Parts per million error detection
- Monitoring for compliance violations while running specific routines on the system under test.
- Editing of DDR standard compliance test parameters.
- Creation of custom regression test suites (using valid logic analyzer triggers) for any digital system that can be probed by the Agilent logic analyzer.

Real-Time Violations

State machine violations common to DDR, DDR2, DDR3, DDR4 and LPDDR, LPDDR2, LPDDR3	
READ or WRITE to an inactive row	
REFRESH to an active bank	
ACTIVATE to an active bank	
Compliance parameter	**Real-time compliance tests**
DDR and DDR2 and LPDDR	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= REFI*9
tMRD	MRS (MODE Register Set) to MRS must be >= tMRD

Compliance parameter	Real-time compliance tests
DDR3	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= REFI*9
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration (normal operation) to any valid command must be > tZQCS
tMRD	MRS (MODE Register Set) to MRS must be >= tMRD
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL
DDR4	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD_L	WRITE to WRITE (same group) must be >= tCCD_L
tRFC	REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC
tRRD_L	ACTIVATE to ACTIVATE (different banks) must be >= tRRD_L
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH to REFRESH <= REFI*9
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration (normal operation) to any valid command must be > tZQCS
tMRD	MRS (MODE Register Set) to MRS must be >= tMRD
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL

Compliance parameter	Real-time compliance tests
LPDDR2 and LPDDR3	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tRC	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tZQCL	Long calibration command to any valid command (or CKE low) must be > tZQCL
tZQCS	Short calibration command to any valid command (or CKE low) must be > tZQCS
tZQINIT	Init calibration command to any valid command (or CKE low) must be > tZQINIT
tZQRESET	Reset calibration command to any valid command (or CKE low) must be > tZQRESET
tMRW	MRW command to any valid command (or CKE low) must be > tMRW
tMRR	MRR command to any valid command (or CKE low) must be > tMRR
tRFCab	REFRESH (all banks) to Active or Refresh must be > tRFCab
tRFCpb	REFRESH (per bank) to Activate (same bank) or REFRESH must be > tRFCpb
tRPab	PRECHARGE (all banks) to ACTIVE (any bank) must be >= tRPab
tRPpb	PRECHARGE (per bank) to ACTIVE (same bank) must be >= tRPpb
tCKE	Duration of CKE high/low >= tCKE



New B4622B Real-Time Violation Tool – DDR3 example.

Post Process DDR/2/3/4 or LPDDR/2/3 Compliance Application tool

The Post Process Compliance Application tool automates state machine, protocol compliance, and protocol level bus cycle timing violation detection across Agilent logic analyzer traces. The tool provides the test results with details of the test failure in HTML format for reporting purposes.

Use the Post Process Compliance Application tool to:

- Spot check logic analyzer traces for violations.
- Check logic analyzer trace captures leading up to system crashes for possible violations before the crash.

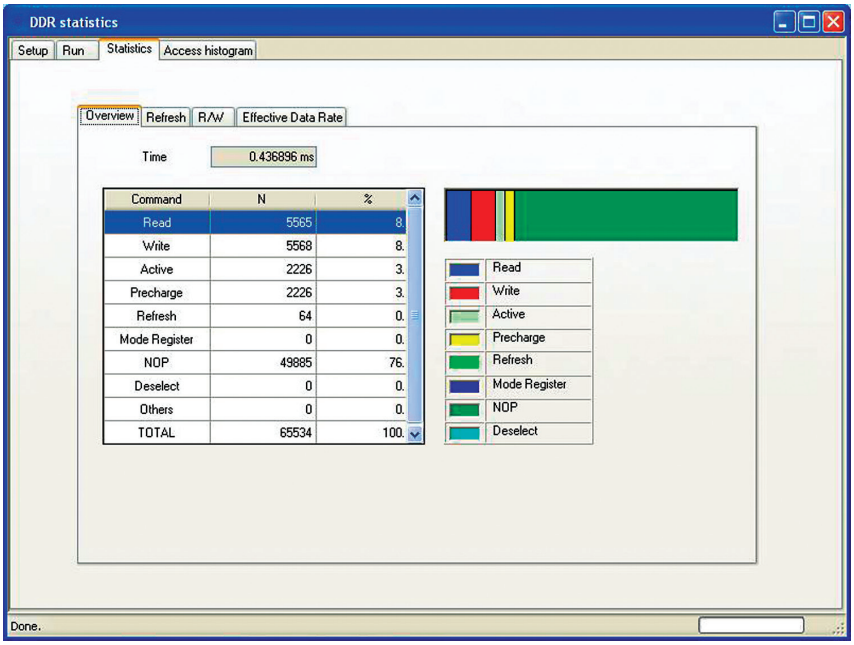
Post Process Compliance Tests

State machine violations common to DDR, DDR2, DDR3, DDR4 and LPDDR, LPDDR2, LPDDR3	
READ to WRITE to an inactive row	
REFRESH to an active bank	
ACTIVATE to an active bank	
Compliance parameter	**Post process / Compliance tests**
DDR and DDR2 and LPDDR	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRFC	REFRESH to non-NOP/DES must be >= tRFC
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tFAW	Four ACTIVATE window (different banks) must be >= tFAW
tRCD	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH command to REFRESH command must be <= tREFI*9
tMRD	Mode Register Set command to Mode Register Set Command >= tMRD
DDR3	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRP	PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRFC	REFRESH to non-NOP/DESELECT must be >= tRFC
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tFAW	Four ACTIVATE window (different banks) must be >= tFAW

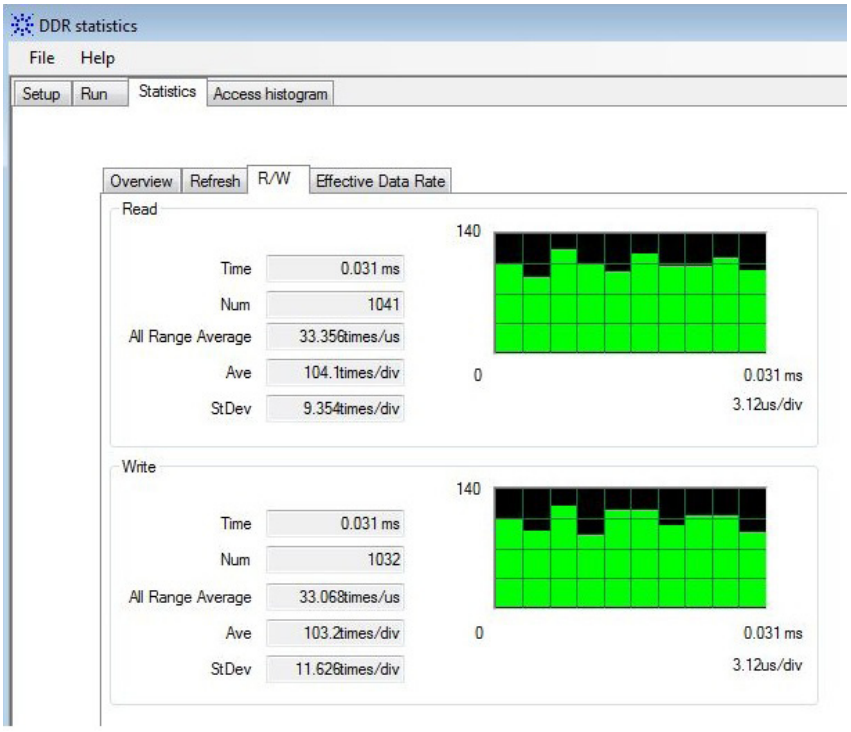
Compliance parameter	Post process / Compliance tests
DDR3 (continued)	
tRCD	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tREFI	REFRESH command to REFRESH command must be <= tREFI*9
tZQoper	Long cal (normal operation) to valid command must be >= tZQoper
tZQCS	Short calibration command to any valid command (or CKE low) must be > tZQCS
tMRD	Mode Register Set command to Mode Register Set command >= tMRD
tMOD	MRS (MODE Register Set) to valid command must be >= tMOD
tREFPDEN	REFRESH to power down entry >= tREFPDEN
tRDPDEN	READ to power down entry >= tRDPDEN
tWRPDEN	WRITE to power down entry >= tWRPDEN
tXPR	Exit RESET from CKE high to valid command >= tXPR
tXSDLL	Self refresh exit to valid command with DLL must be >= tXSDLL
tXPDLL	Exit precharge power down with DLL to any valid command < tXPDLL
LPDDR2 and LPDDR3	
tRASmax	ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax
tRASmin	ACTIVATE to PRECHARGE must be >= tRASmin
tRCD	ACTIVATE to READ/WRITE must be >= tRCD
tRTP	READ to PRECHARGE must be >= tRTP
tDRW	READ to WRITE must be >= tDRW
tDWP	WRITE to PRECHARGE must be >= tDWP
tDWR	WRITE to READ must be >= tDWR
tCCD	WRITE to WRITE, READ to READ must be >= tCCD
tRRD	ACTIVATE to ACTIVATE (different banks) must be >= tRRD
tFAW	Four ACTIVATE window (different banks) must be >= tFAW
tRCD	ACTIVATE to ACTIVATE (same bank) must be >= tRC
tZQCL	MRW long calibration command to any valid command (or CKE low) must be > tZQCL
tZQCS	MRW short calibration command to any valid command (or CKE low) must be > tZQCS
tZQINIT	MRW init calibration command to any valid command (or CKE low) must be > tZQINIT
tZQRESET	MRW reset calibration command to any valid command (or CKE low) must be > tZQRESET
tMRW	MRW command to any valid command (or CKE low) must be > tMRW
tMRR	MRR command to any valid command (or CKE low) must be > tMRR
tRPab	PRECHARGE (all banks) to ACTIVE must be >= tRPab
tRPpb	PRECHARGE (per bank) to ACTIVE must be >= tRPb
tCKE	Duration of CKE high/low >= tCKE
tCKESR	Duration of self-refresh >= tCKESR
tDPD	Duration of power down to valid command >= tDPD
tXSR	Exit self-refresh to valid command >= tXSR
tXP	Exit power down to valid command >= tXP
tREFBW	Greater than 8 REFRESH all bank commands in tREFBW
tREFW	Required number of refresh commands occur in time period <= tREFW
tRFCab	REFRESH (all banks) to Active or Refresh must be > tRFCab
tRFCpb	REFRESH (per bank) to Activate (same bank) or REFRESH must be > tRFCpb

DDR/2/3/4 and LPDDR/2/3 Performance Analysis Tool

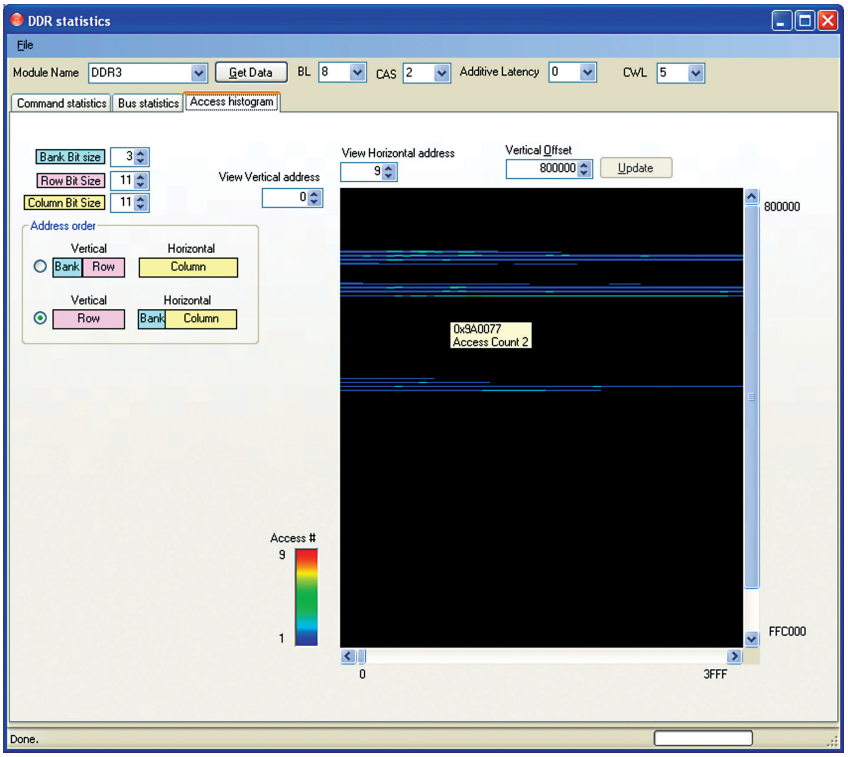
Another key feature of the B4622B is the ability to view the performance of your DDR bus through bus statistic report and histogram. The bus statistic report gives you an overview of the DDR bus utilization for a specific trace to help you analyze the behavior and activity of your DDR bus. The histogram view reports the number of access in specific memory location to help you improve optimization by controlling the number of access across the address bus.



DDR bus statistic view for obtaining command cycles information in color-coded chart.



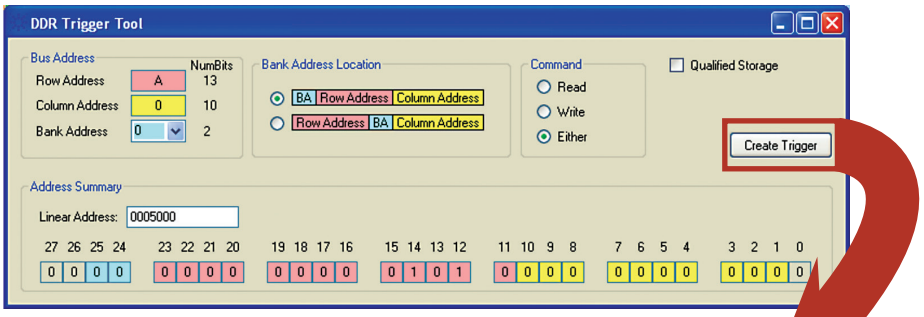
DDR bus statistic views for providing bus utilization information on read and write commands.



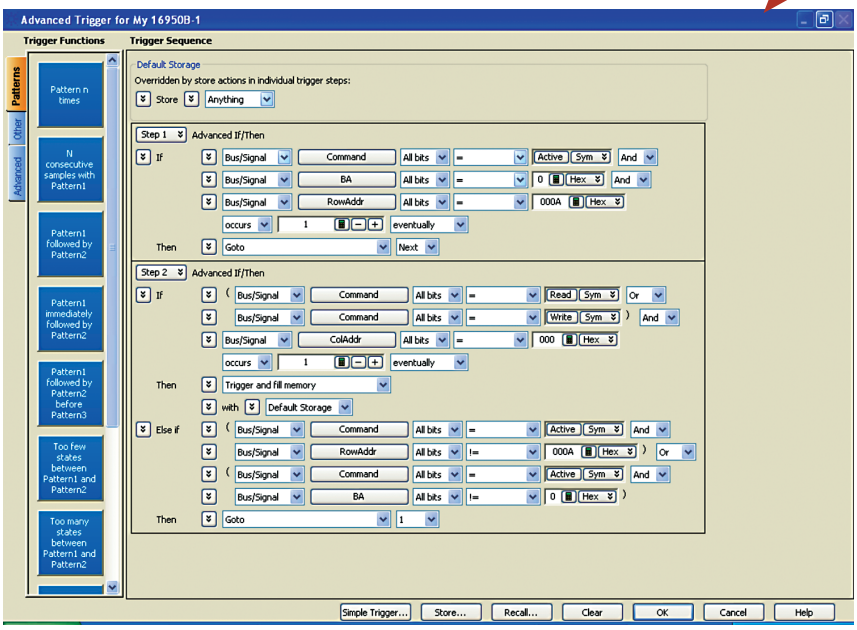
Access histogram view to enable overview of number of access at specific DDR address.

DDR/2/3/4 and LPDDR/2/3 Trigger Tool

Setting up a trigger on a specific physical address to obtain the corresponding data bus can be very tedious. The B4622B allows you to automatically create a trigger on a specific physical address without having to go through a step by step trigger add-in. The trigger setup tool incorporates a user-friendly interface to help you quickly setup the trigger.



User friendly interface to setup trigger on a physical address.



Resulting trigger for the Agilent logic analyzer created by the trigger tool.

Logic Analyzer Ordering Information

The B4622B operates with the following Logic Analyzers from Agilent Technologies. Logic analyzer selection criteria includes: logic analyzer specifications and characteristics, maximum DDR technology data rate, and minimum data valid windows of the data eyes at the logic analyzer probe point.

Product	Description
AXIe-based logic analyzers	
U4154A	U4154A 136-channel, 4 Gb/s state, AXIe-based logic analyzer module
16900 Series logic analyzers	
16900A	6-slot mainframe, requires external display
16901A	2-slot mainframe with 15-inch display with touch screen
16902B	6-slot mainframe with 15-inch display with touch screen
Logic analyzer modules	
16950B	68-channel 4 GHz timing, 667 MHz state logic analysis module
16962A	68- channel 2 GHz timing, 2 GT/s state logic analysis module
DDR2 BGA probes	
W2631A	DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2632A	DDR2 x16 BGA data probe for logic analyzer and oscilloscope – kit of 4 probes
W2633A	DDR2 x8 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2634A	DDR2 x8 BGA data probe for logic analyzer and oscilloscope – 4 probe set
Logic analyzer ZIF probes (used to connect W2630As Series DD2 BGA probes to 90 pin logic analyzer cables)	
E5384A	46-ch single-ended ZIF probe for x8/x16 DRAM BGA probe connect to 90-pin logic analyzer cable
E5826A	46-ch single-ended ZIF probe for x16 DRAM data only BGA probe connect to logic analyzer cable
E5827A	46-ch single-ended ZIF probe for 2 x8 DRAMs data only BGA probe connect to 90-pin logic analyzer
DDR3 BGA probes	
W3631A	DDR3 x16 BGA command and data probe for logic analyzer and oscilloscope
W3633A	DDR3 x4/x8 BGA command and data probe for logic analyzer and oscilloscope
Logic analyzer ZIF probes (used to connect W3630A Series DDR3 BGA probes to 90 pin logic analyzer cables)	
E5845A	46-ch single-ended ZIF probe for x16 DRAM BGA probe connect to 90-pin logic analyzer cable
E5847A	46-ch single-ended ZIF probe for x8 DRAM BGA probe connect to 90-pin logic analyzer cable
DDR3	
Required/recommended software	
Logic and protocol analyzer software (required)	
B4622B (required)	DDR/2/3/4 and LPDDR/2/3 Protocol Compliance and Analysis Toolset
B4621B (recommended for DDR/2/3/4)	Bus decoder for DDR2, DDR3, or DDR4 debug and validation
B4623B (recommended for LPDDR/2/3)	Bus decoder for LPDDR/2/3 debug and Validtation
DDR Setup Assistant and DDR Eyefinder (recommended)	

For additional DDR/2/3/4 and LPDDR/2/3 probing options, contact your local Agilent representative ***www.agilent.com/find/contactus*** *or refer to the U4154A logic analyzer data sheet, 5990-7513EN.*

Information on FuturePlus DIMM and SODIMM interposers for DDR2, DDR3, and DDR4 is available at ***http://www.futureplus.com/DDR3-Memory/agilent-la-support-overview.html***

For additional analysis software, refer to ***www.agilent.com/find/logic-sw-apps***

Related Literature

Publication title	Pub number
Agilent Technologies 16900 Series Logic Analysis Systems - Brochure	5989-0420EN
U4154A AXIe-based Logic Analyzer Module - Data Sheet	5990-7513EN
W2630A Series DDR2 BGA Probes for Logic Analyzers and Oscilloscopes - Data Sheet	5989-5964EN
W3630A Series DDR3 BGA Probe for Logic Analyzers and Oscilloscopes - Data Sheet	5990-3179EN

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