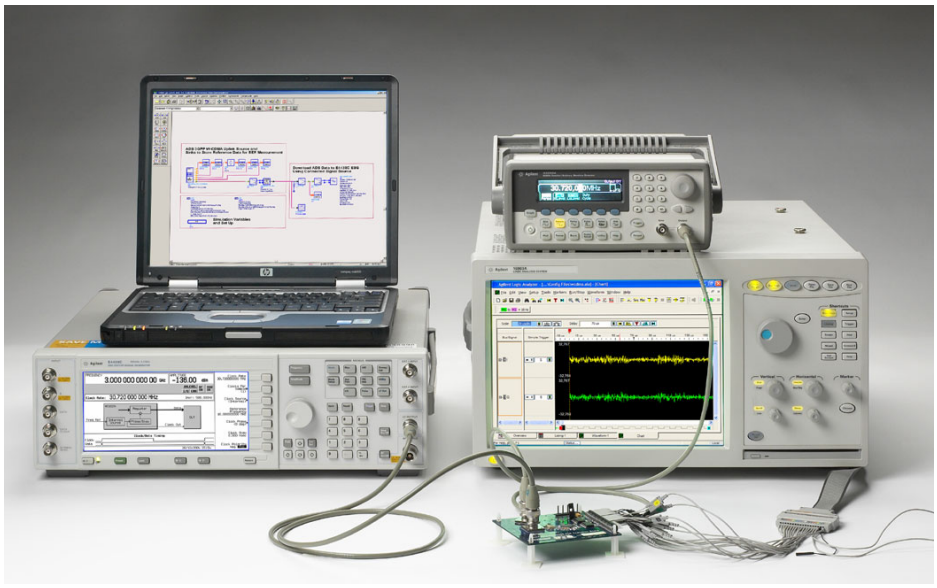
# Demo Instructions for Digital VSA
# (Logic Analyzers AND Vector Signal Analysis)

Updated August 24, 2006

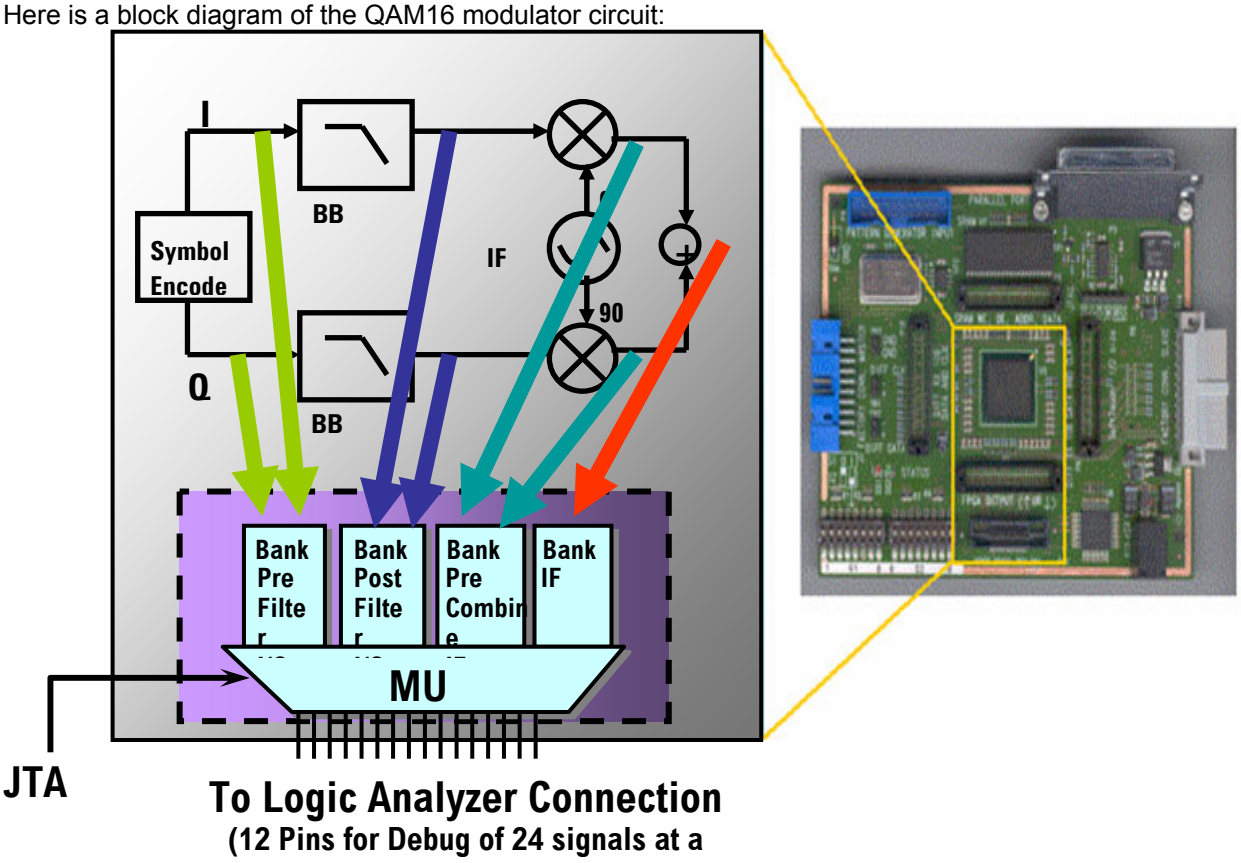


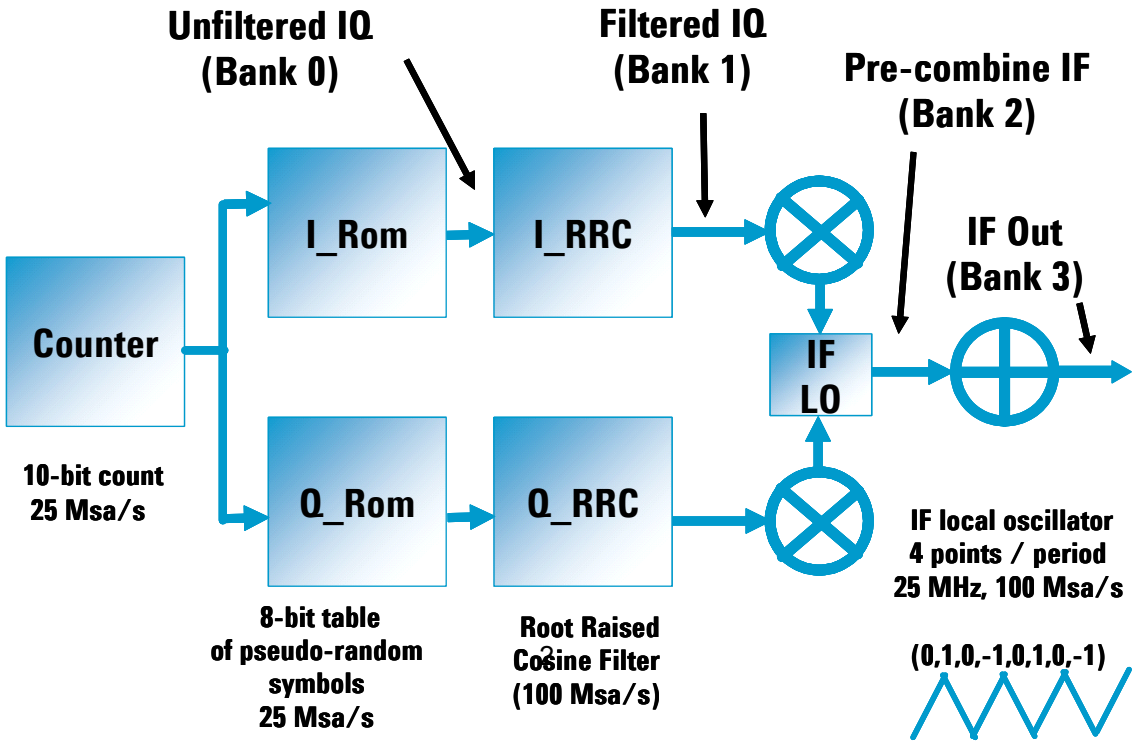
## *QAM16 Digital Radio in FPGA Demo Board*

This demo uses the Logic Analyzer FPGA Demo board and the B4655A FPGA Dynamic Probe to demonstrate VSA on digital Baseband and IF signals in a QAM16 transmitter.

### Demo Overview

Here is a block diagram of the QAM16 modulator circuit:



To simulate an incoming bit stream and symbol encoder, we actually use a 10-bit counter and a pair of ROM's which contain a pre-made array of IQ symbols. Those IQ symbols are 8-bit signed numbers, running at 25 MHz. Those IQ symbols are sent through an interpolating Root Raised Cosine filter (a kind of low-pass filter). The output is 24 bits in resolution, at 100 MHz (4 samples per symbol). This is the ***IQ Baseband*** data. This data is modulated by an IF LO (Intermediate Frequency Local Oscillator). This LO is a sine wave generator with two outputs, one 90 degrees out of phase from the other.

The IF LO is a bit crude in this example; there are 4 samples per IF period, effectively making the sine wave actually a triangle wave (0, 1, 0, -1, 0, etc). This is a common practice in DSP because it's a lot easier to implement this than a full direct digital synthesizer (sine wave generator).

Finally the two IF components are added back together to create the scalar "IF" signal.

All of these various signals are probed with the FPGA dynamic probe. We are using 24 pins, with the 2X mux option. So we can simultaneously see the I and Q Baseband 24-bit signals through one set of pins. Since the Baseband bus is running at 100 MHz, the muxed pins are running at 200 MHz.

## Demo Requirements

1. 16900 series logic analyzer mainframe with 3.6 LA software and 6.30 VSA software.
2. 16910A logic analyzer card

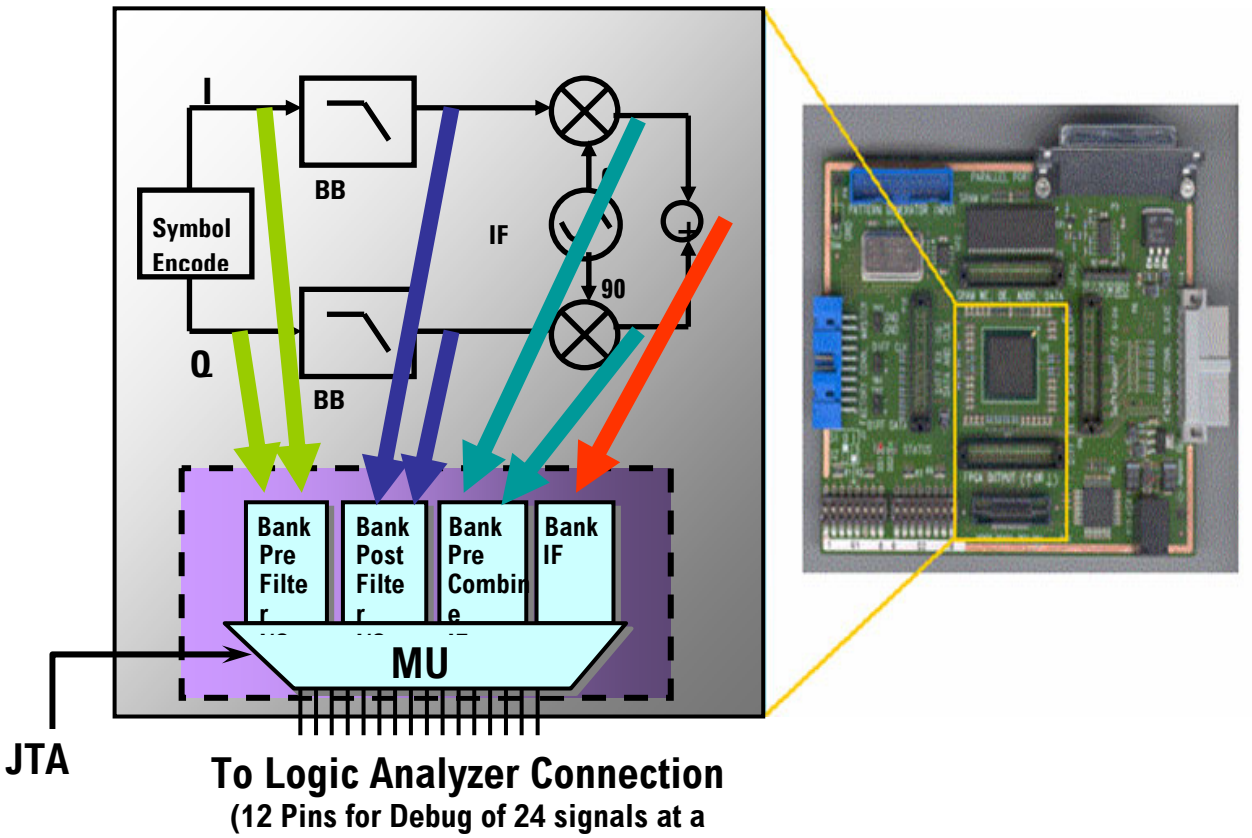
Or: 16800 Series logic analyzer with the same software requirements.

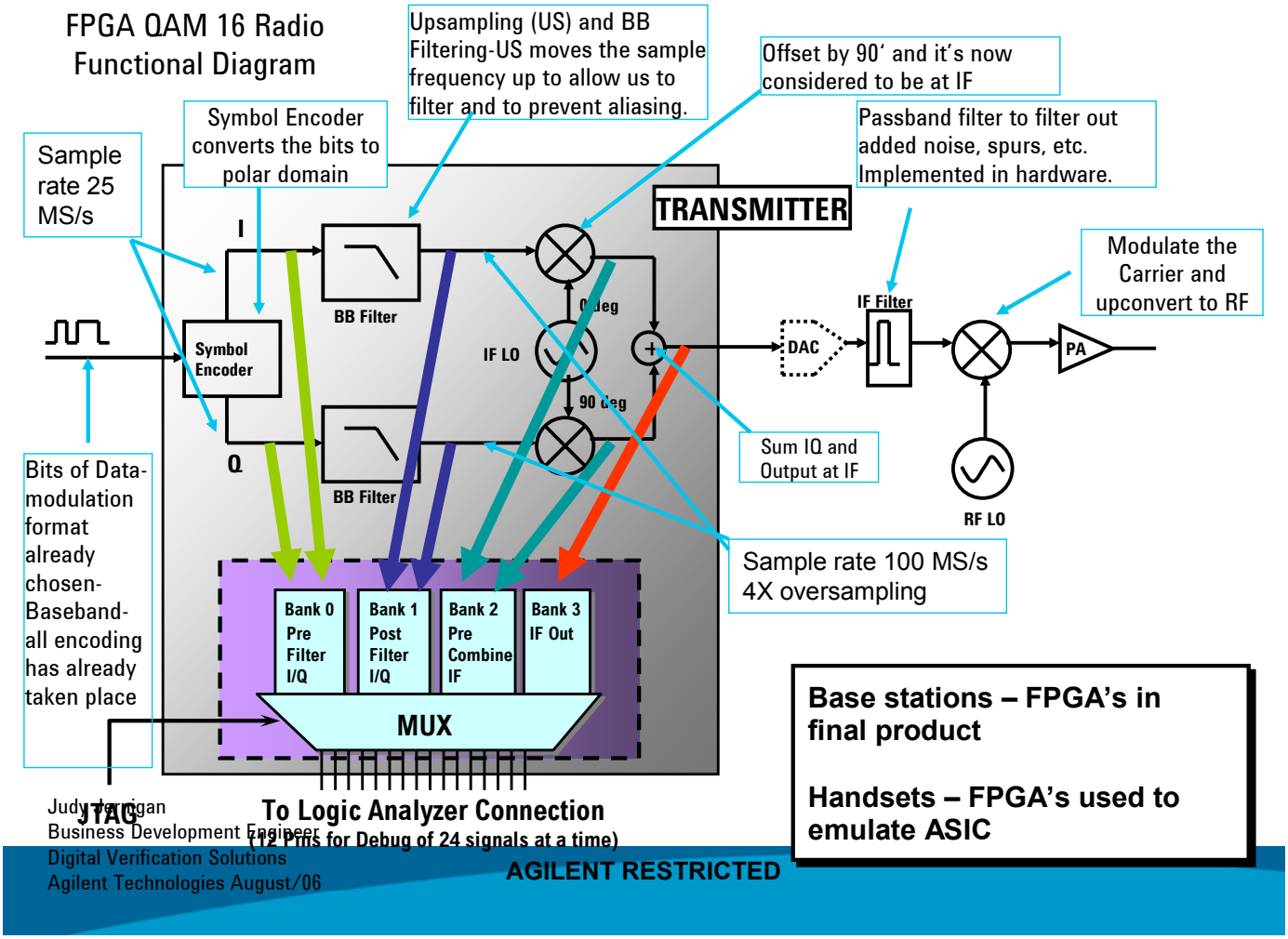
3. E5346A mictor probe
4. FPGA demo board
5. FPGA bitfile, CDC file, and configurations (in the "QAM16 FPGA Demo" folder of the share drive)

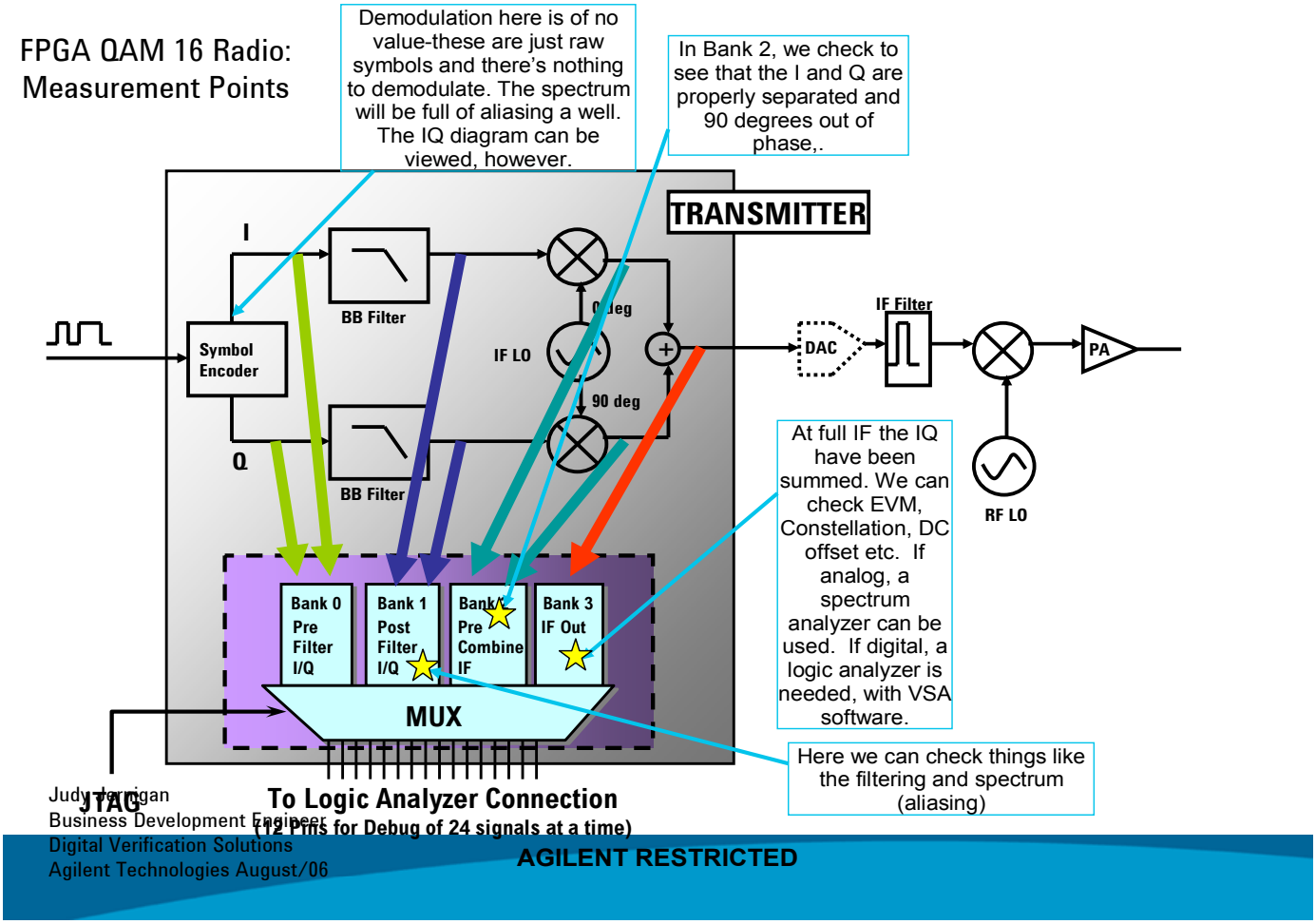
## Demo Instructions

1. If currently running, close the logic analyzer and 89601 VSA applications.
2. Connect the Logic Analyzer FPGA Demo board to **Pod 1** and **Pod 3** of the Logic Analyzer.
3. Start the logic analyzer application. Look in the lower right hand corner to make sure that the logic analyzer application is connected to the logic analyzer hardware. (The word 'Local' will be displayed in the lower right hand corner. If the logic analyzer application is not connected to the hardware it will say 'Offline'.)
4. Perform the following to download the correct bits into the demo board's FPGA.
    a. Go to the **Overview** tab of the logic analyzer (lower left corner). From the Module icon, use the pull down on the left and select **'New Probe', 'FPGA Dynamic Probe'**.
    b. Select Cable Connection. In the dialog make sure that **'Xilinx Cable', Parallel Auto detect, Speed = 200 KHz and Port LPT1** are selected. (Assumes you are using the parallel cable supplied with the demo board.) Click **OK**.
    c. Highlight the XC2V250 Row, and select "Configure Device."
    d. Recall the "qam16automap.bit" file and allow it to configure.
    e. Once that's done, select "Import Bus/Signals," and select the "qam16demo.cdc'" file.
    f. Tell it OK.
    g. Select '**Pin Mapping'** to have the FPGA Dynamic probe automatically assign the signals to the appropriate channel of the logic analyzer probes/pods. A dialog will appear stating **'Successfully mapped all ATC pins! Would you like to see a graphical view of how pins were mapped?** Select **Yes**. Select the first row to highlight it and then select **'Edit Probe…'** This shows that the names for the internal FPGA signals have been mapped to the appropriate channel of the logic analyzer. Typically a customer would have to spend a long time entering this information in manually. One of the benefits of the FPGA dynamic probe is that it sets up the logic analyzer in a matter of seconds automatically.

h. Click **OK** twice to close the Pin Mapping dialogs.
i. You are now looking at the **FPGA Dynamic Probe Bank Selection** dialog. This is where you can quickly change the which internal FPGA signals you're looking at by simply selecting a Bank and clicking OK.



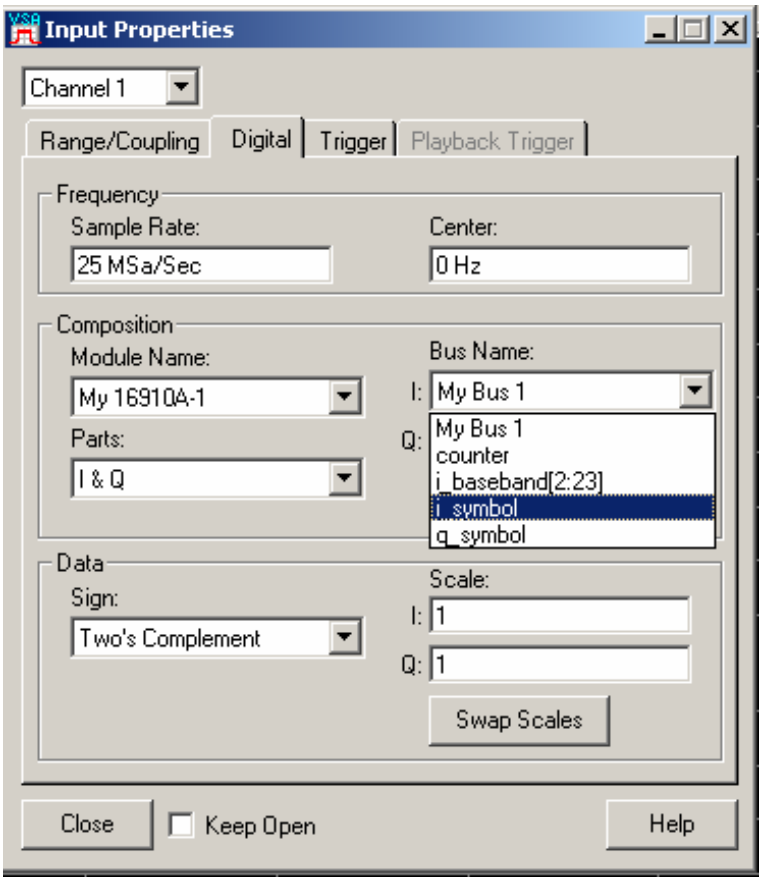

FPGA QAM 16 Radio Functional Diagram
Upsampling (US) and BB Filtering-US moves the sample frequency up to allow us to filter and to prevent aliasing.
Offset by 90' and it's now considered to be at IF
Symbol Encoder converts the bits to polar domain
Passband filter to filter out added noise, spurs, etc. Implemented in hardware.
Sample rate 25 MS/s
TRANSMITTER
Modulate the Carrier and upconvert to RF
I
BB Filter
IF Filter
Symbol Encoder
IF LO
DAC
PA
90 deg
Q
BB Filter
Sum IQ and Output at IF
RF LO
Bits of Data-modulation format already chosen-Baseband-all encoding has already taken place
Sample rate 100 MS/s 4X oversampling
Bank 0 Pre Filter I/Q
Bank 1 Post Filter I/Q
Bank 2 Pre Combine IF
Bank 3 IF Out
MUX
JTAG
To Logic Analyzer Connection
(12 Pins for Debug of 24 signals at a time)
Base stations – FPGA's in final product
Handsets – FPGA's used to emulate ASIC
Judy Flanigan
Business Development Engineer
Digital Verification Solutions
Agilent Technologies August/06
AGILENT RESTRICTED




Let's start looking at it now:

**BANK ZERO:**

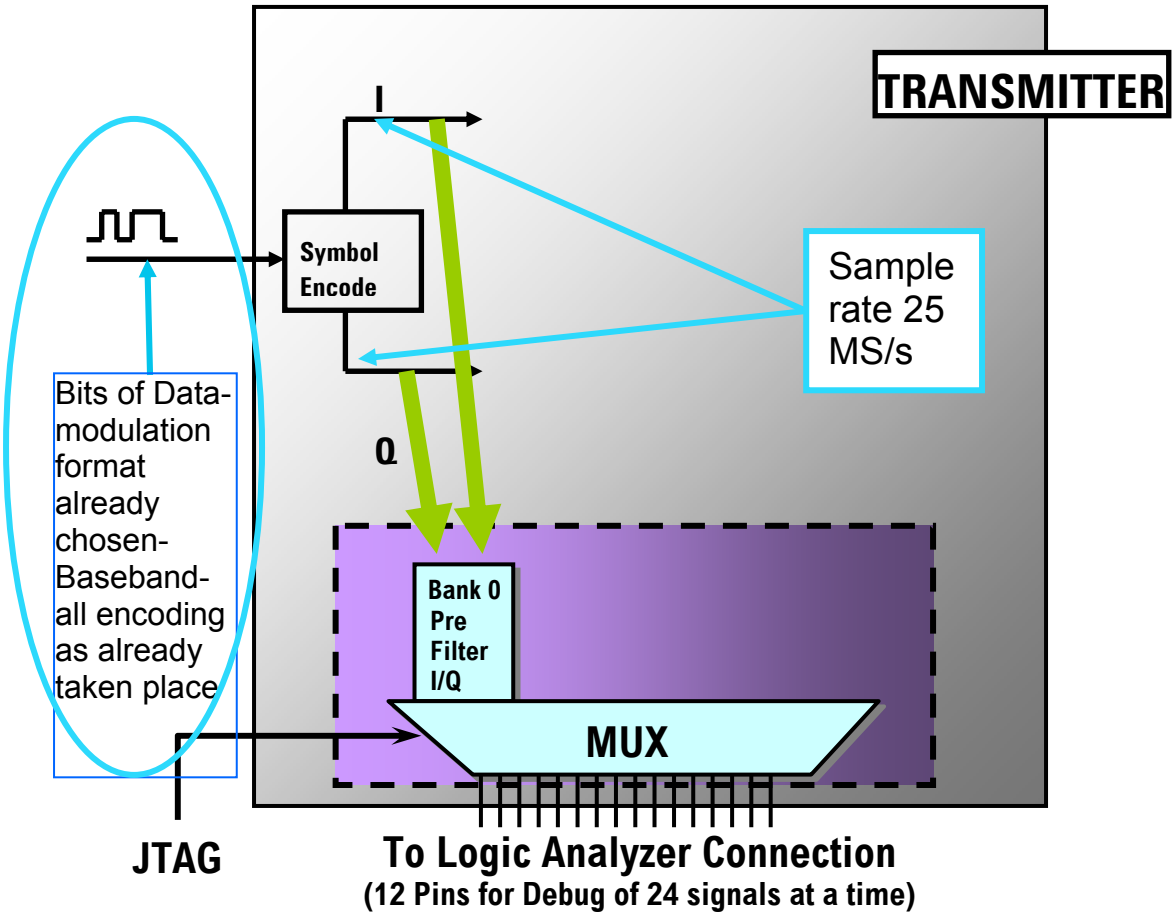
1. Click on Bank 0 and Run the Eyefinder.
2. If the 89601A software is not already running, go ahead and start it up. It will take a few seconds.
3. Once it's up, go to Input>Digital, and Select "Refresh Names."
4. Set the Sample Rate to 25 MSa/S (this is the sample rate prior to upsampling).
5. Pull down the Module Name window and select the logic analyzer.
6. Pull down the Parts window and select "I&Q."
7. Pull down the Bus name for I and select i_symbol, and do the same for the Q Bus Name. (q_symbol).



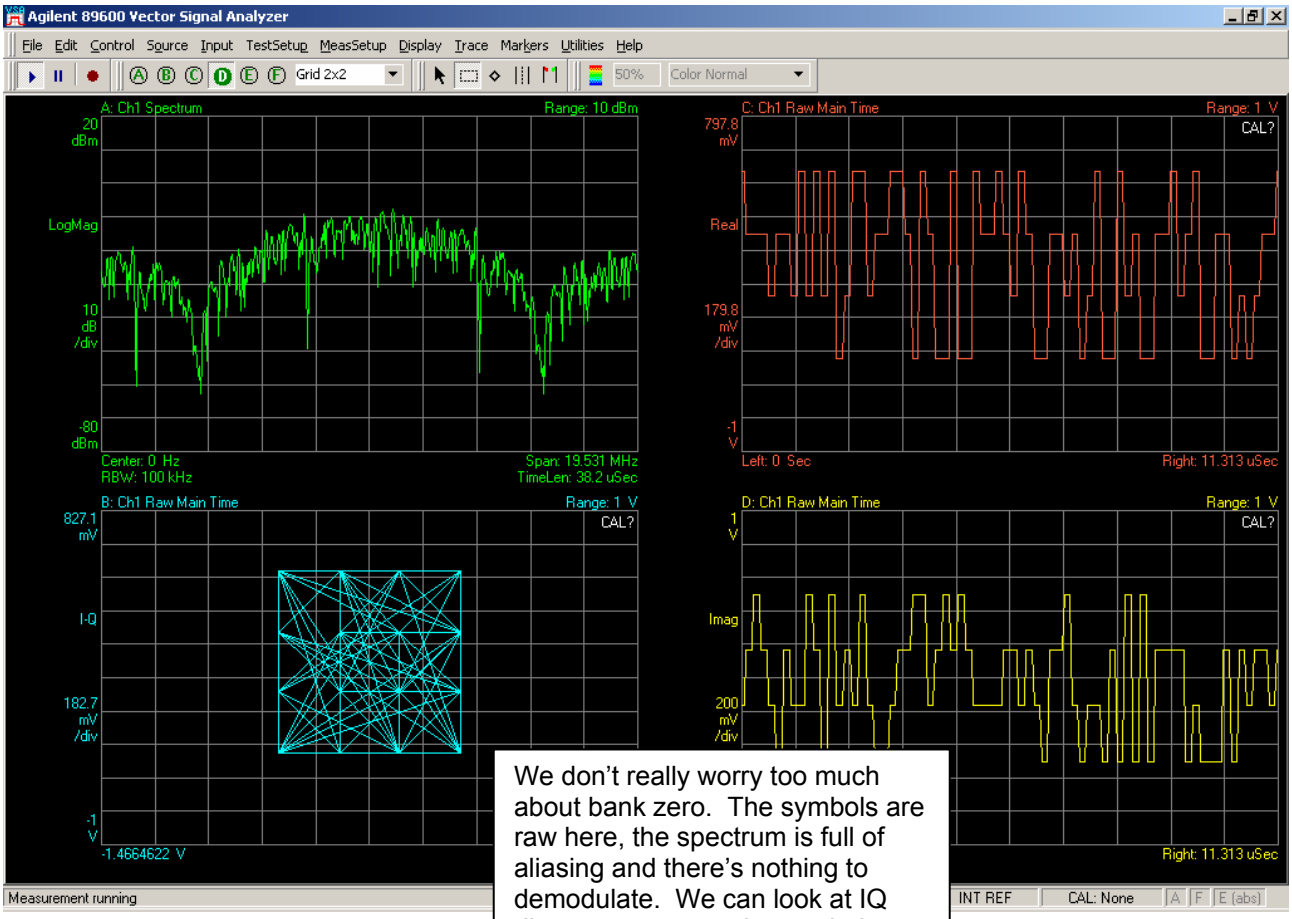

8. Close this window out and go to the main screen. Select the Run button on the 89601A software.
9. Trace A will be the spectrum. All though it looks much like a Sinx/X display, it's mostly just aliasing-folding in on itself etc.

Recall the setup file "Prefilter bank zero setup.set." (Go to File>Recall>Recall Setup).

# FPGA QAM 16 Radio Bank 0



# FPGA QAM 16 Radio Bank 0

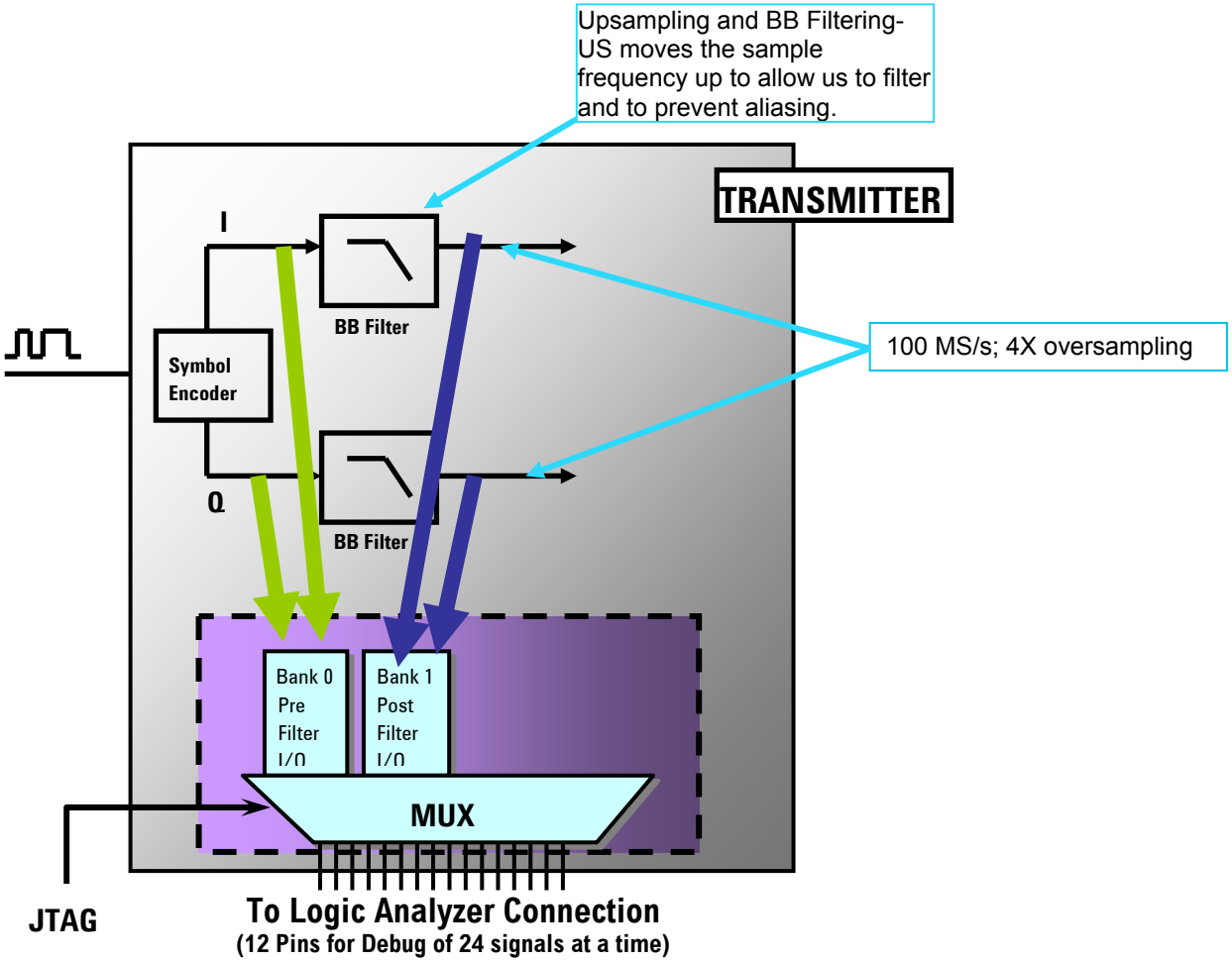



We don't really worry too much about bank zero. The symbols are raw here, the spectrum is full of aliasing and there's nothing to demodulate. We can look at IQ diagram to ensure the symbol encoder did it's job correctly. We can look at the raw symbols if we want.

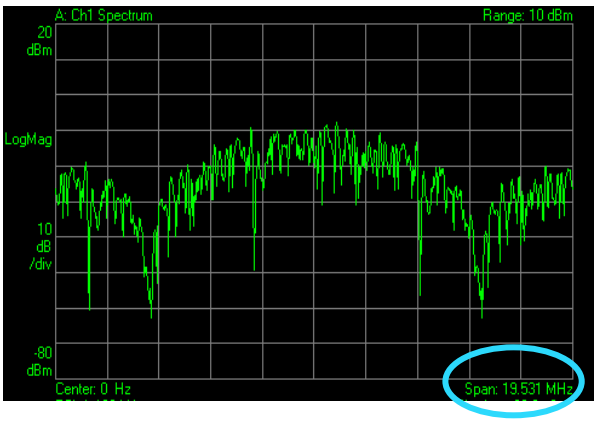
**BANK ONE:**

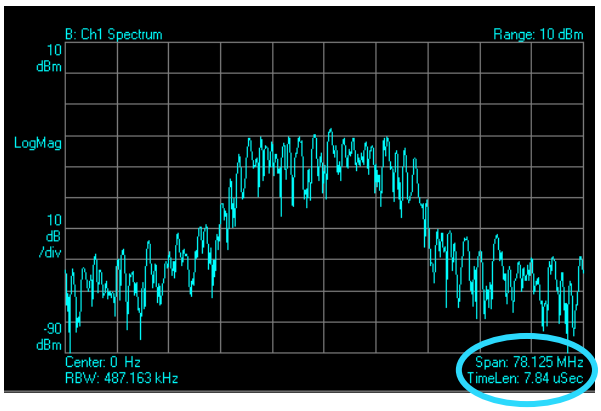
1. On the Logic Analyzer application, click "Cancel" on the screen that tells us it's being used by the 89600 VSA.
2. Under the Overview tab, select Bank One, and run the Eyefinder. Tell it OK, once it's finished.
3. Go back to the 89601A software and go to Input>Digital, and Select "Refresh Names."
4. Set the Sample Rate to 100 MSa/S . We have up-sampled between 4X at this point. Typically this is done by interleaving 0s. We have then filtered the signal with a Root Nyquist filter (filter Alpha is approximately 0.3), so we'll see a nice, clean spectrum.
5. Pull down the Module Name window and select the logic analyzer.
10. Pull down the Parts window and select "I&Q."
11. Pull down the Bus name for I and select i_basebandl, and do the same for the Q Bus Name. (q_baseband).
12. Select the run button on the 89601A Software.

# FPGA QAM 16 Radio
# Bank One



# FPGA Demo Bank 0 to Bank 1: 89601A



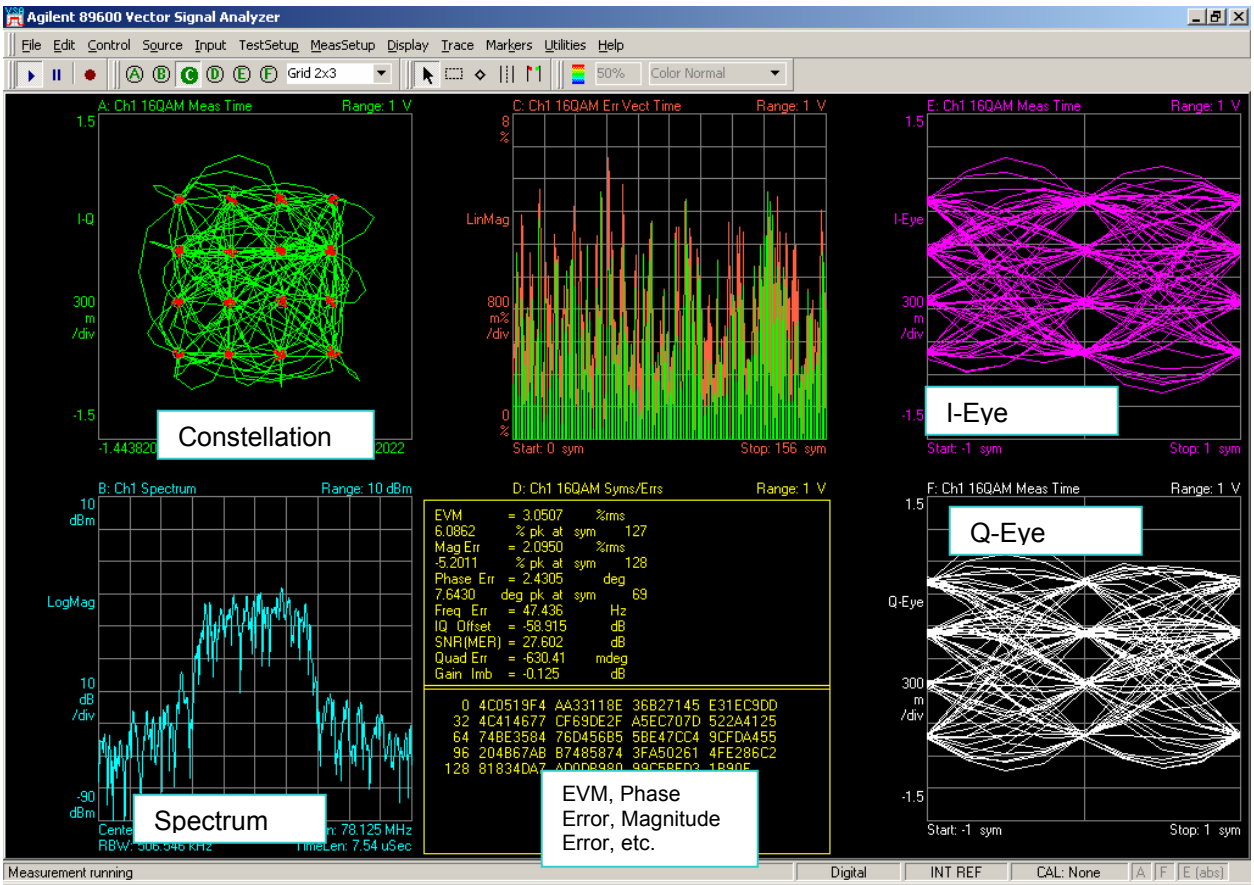

**Pre-filter**

- Notice the enormous difference in the spectrums!
- Applied filtering has removed the aliasing.
- The spans are different because we have applied 4X upsampling at Bank 1.

**Post-filter**

13. Recall the setup file for bank one: "Postfilter bane one setup.set"

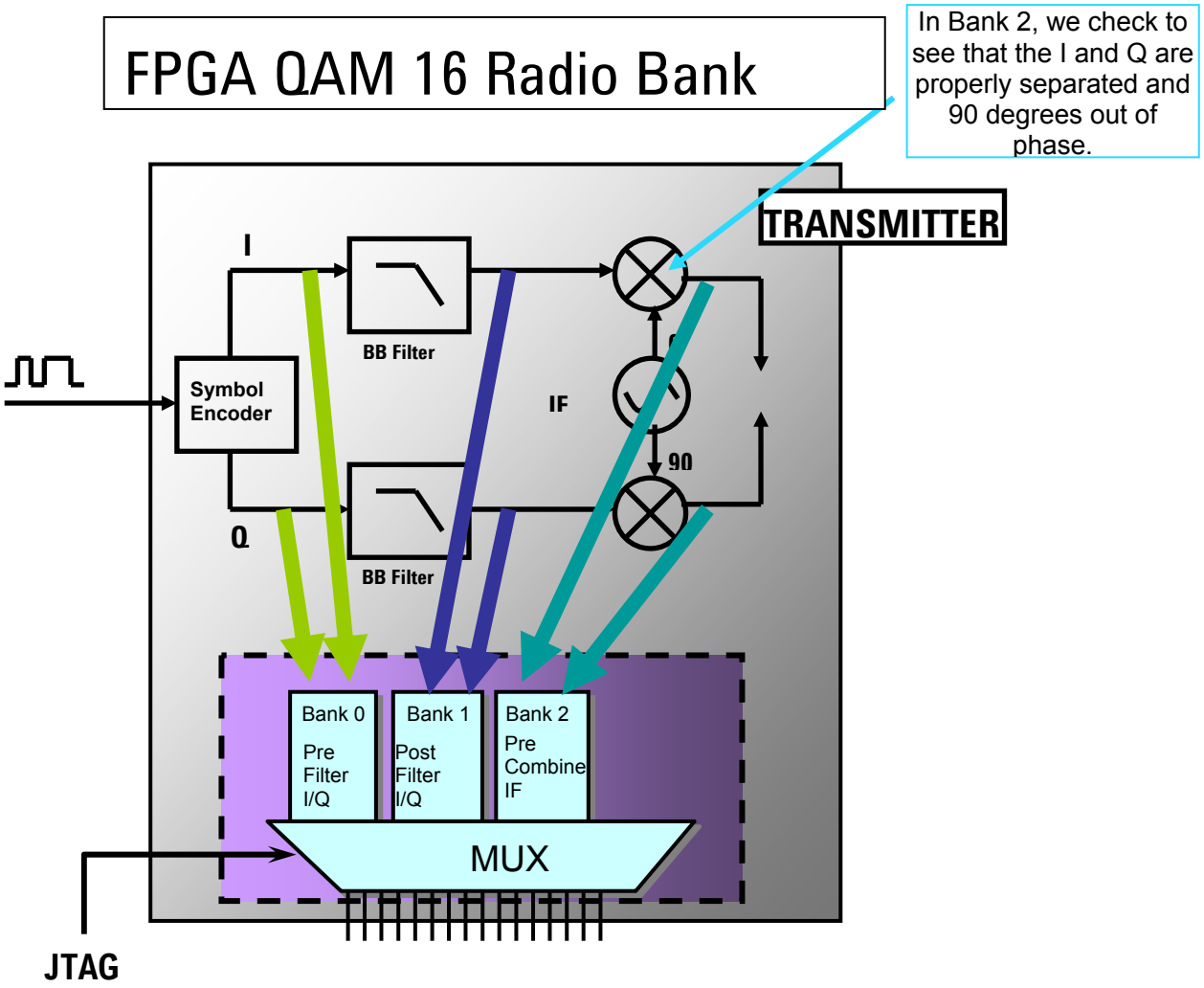
We can look at all the modulation quality measurements now. A wonderful application for the DVSA is in measurements for a digital receiver. You can use these mod quality values to tradeoff filter (BB Filters) designs.



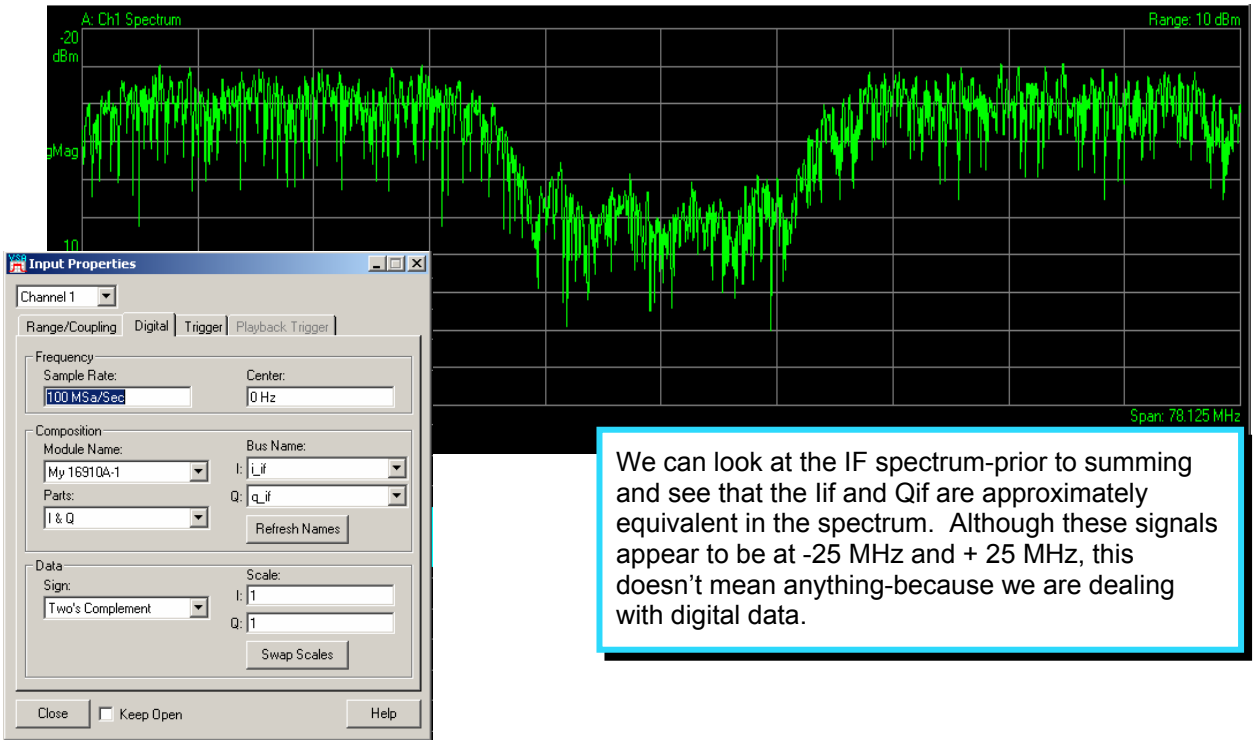
**BANK TWO:**

1. On the Logic Analyzer application, click “Cancel” on the screen that tells us it’s being used by the 89600 VSA.
2. Under the Overview tab, select Bank Two, and run the Eyefinder. Tell it OK, once it’s finished.
3. Go back to the 89601A software and go to Input>Digital, and Select “Refresh Names.”
4. Keep the Sample Rate at 100 MSa/S . This won’t change again.
5. Pull down the Module Name window and select the logic analyzer.
6. Pull down the Parts window and select “I&Q.”
7. Pull down the Bus name for I and select i_if, and do the same for the Q Bus Name. (q_if).
8. Recall the setup file, “Presum bank two part one.set.”

Select the run button on the 89601A Software.



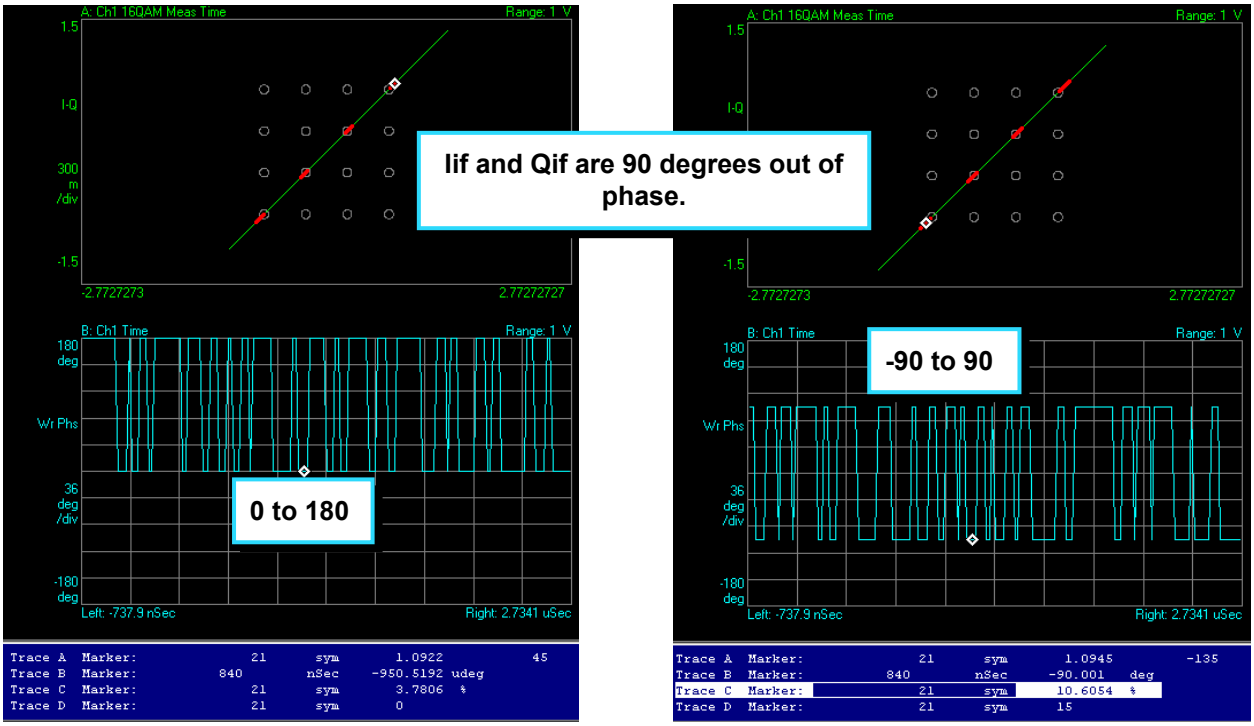
# FPGA QAM 16 Radio: Bank 2, Spectrum




We can look at the IF spectrum-prior to summing and see that the Iif and Qif are approximately equivalent in the spectrum. Although these signals appear to be at -25 MHz and + 25 MHz, this doesn't mean anything-because we are dealing with digital data.

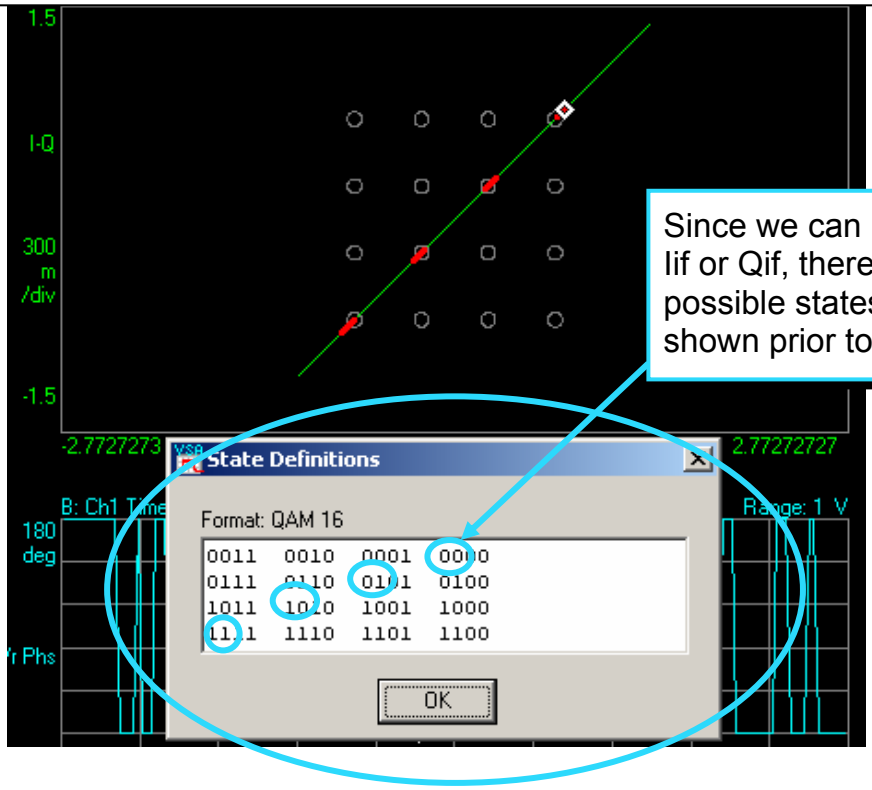
9. Recall the setup file : "Presum bank two part two demod.set"
10. The setup file also setup the digital input properties. Go to Input>Digital, and you'll see that we now have a real signal, i_if. You can change this to q_if if you like. Note that the center frequency is meaningless because this is a digital signal.
11. Notice in trace B that we have the phase if the I-if Signal wrapped. The marker should be reading out 180 degrees (Trace B offset).
12. Go the Input>Digital window and pull down the I bus name to select q_if. Now you'll find that the phase readout (Trace B offset) wraps between -09 to +90 degrees, and that i_if and q_if are 90 degrees out of phase with each other.

# FPGPA QAM 16 Radio: Bank 2, Phase




# FPGA QAM 16 Radio: Bank 2, Constellation States

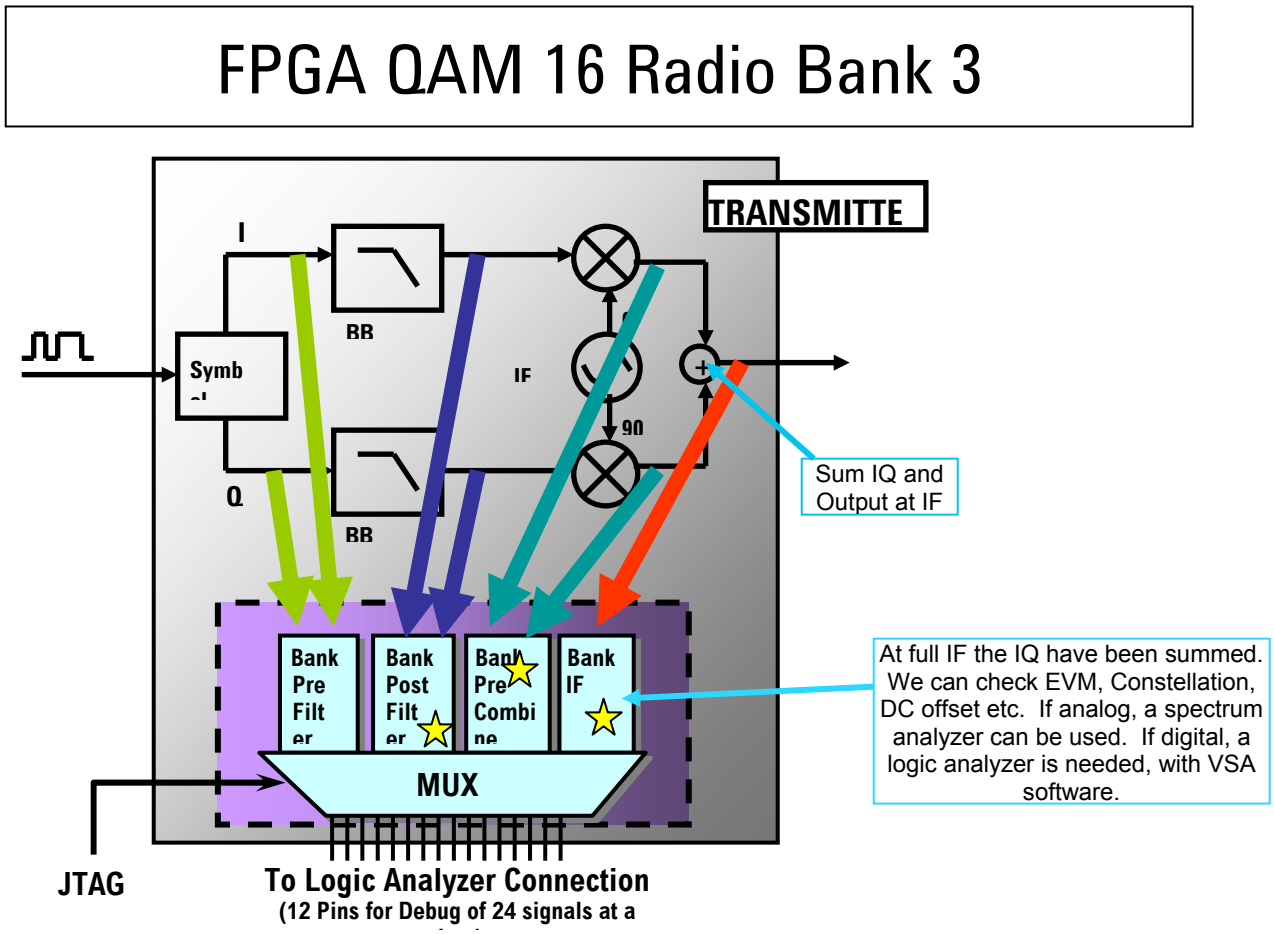
A typical 16 QAM signal has 16 different states



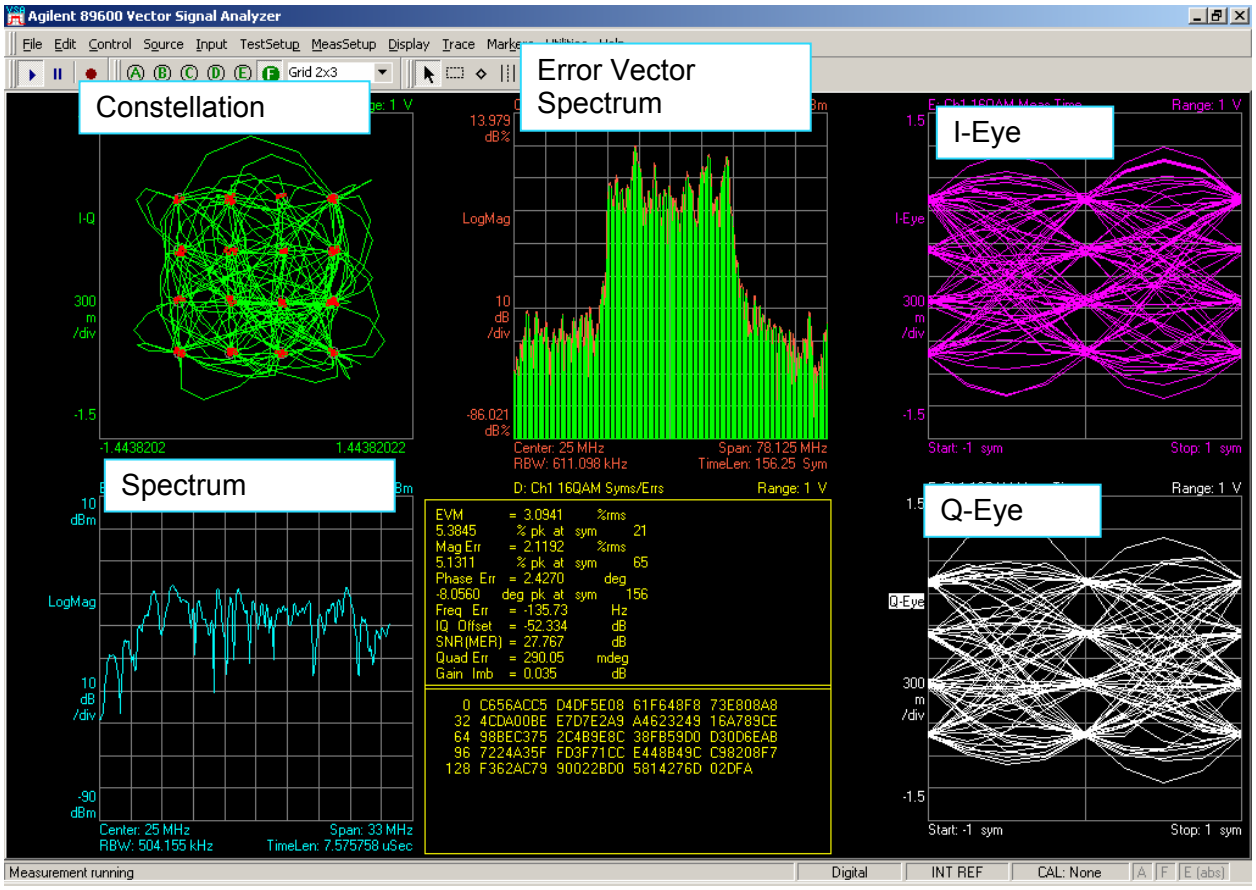

Since we can look only at lif or Qif, there are only 4 possible states that can be shown prior to summing.

**BANK THREE:**

1. On the Logic Analyzer application, click “Cancel” on the screen that tells us it’s being used by the 89600 VSA.
2. Under the Overview tab, select Bank Three, and run the Eyefinder. Tell it OK, once it’s finished.
3. Go back to the 89601A software and go to Input>Digital, and Select “Refresh Names.”
4. Keep the Sample Rate at 100 MSa/S .
5. Pull down the Module Name window and select the logic analyzer.
6. Pull down the Parts window and select “REAL.”
7. Pull down the Bus name for I and select Ifout
8. Go to File>Recall>Recall Setup and recall the setup “Full if demod no equalizer.set.”



# Digital Radios:  Bank 3 Final IF

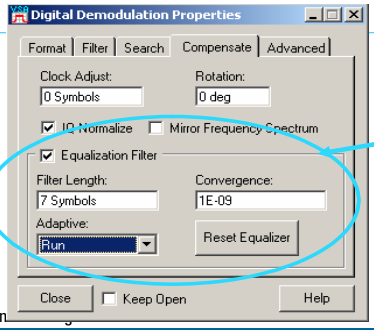



The final IF, center frequency is 25 MHz.  However, because this is a logic analyzer measurement-it's purely digital, the center frequency is irrelevant and is for display purposes only.
The center frequency and sample rate define the limits for the center frequency:
 (real data)
Minimum Center Frequency = 0
Maximum Center Frequency = Sample Rate / 2.56
(complex data
Minimum Center Frequency = Center - Sample Rate / 2.56
Maximum Center Frequency = Center + Sample Rate / 2.56

Think of the maximum center frequency as the highest frequency that can be displayed as well.  This is why Trace B shows the spectrum as being cut off on the upper side.

# The Advantages of Equalization

- Quadrature Amplitude Modulation, or QAM. is a combination of phase and amplitude modulation. and is used extensively in A/D applications, 3G systems, modems (cable TV), and Digital Video broadcasting because it is very robust and can carry high data rates.
- Filtering is typically Root Nyquist (Or Root-Raised Cosine).
- QAM has inherent linear errors (amplitude/magnitude) so quite often an Equalizer is used. An Equalizer smoothes out the linear errors to give a flatter frequency response. Most QAM receivers utilize some type of equalizer. This is also true with Orthogonal Frequency Division Multiplexing (OFDM) receivers (and with others).




**Agilent's 89601A VSA software provides a feed forward Equalizer to view your signal as your receiver would. This allows for more efficient design tradeoffs in the transmitter.**


Judy Jernigan
Business Develop
Digital Verification Solutions
Agilent Technologies August/06

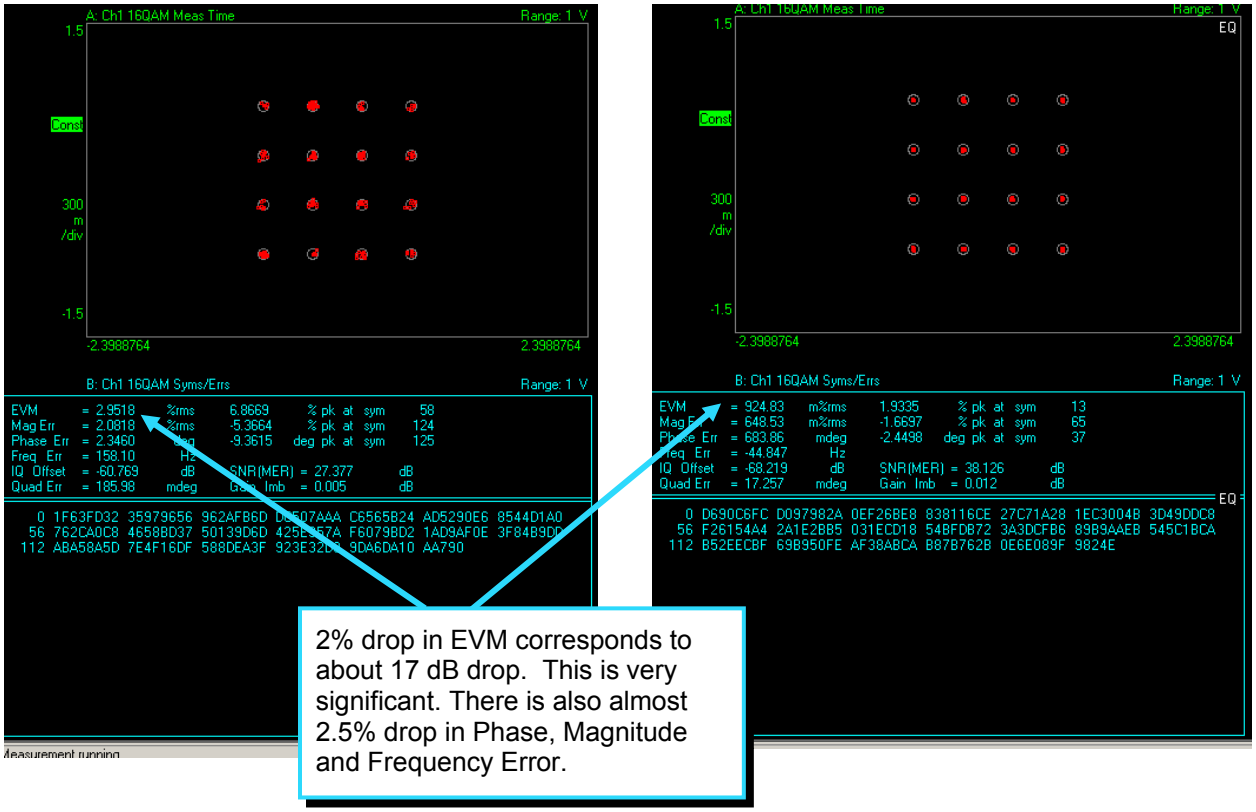



**BANK THREE, Cont.**

9. Recall (in the 89601A) the setup file "Full if demod Equalized.set."
10. Go to "MeasSetup>Demod Properties" and select the "Compensate Tab.
11. Pull down the Adaptive Window and select "Run."
12. Select the "Reset Equalizer" button, then while watching the EVM, pull down the Adaptive window again and hover over the "Hold" button until the EVM has gotten as good as it will get, then select it.
13. What happened to the two right hand windows?
    a. The length of the filter determines the position of the unit impulse response in the filter. The impulse is located in the center of the filter for short filter lengths. As the filter length increases, the impulse moves, proportionally, towards the start of the filter to handle channels with *large delay-spread*. This is the Trace E: Ch1 16QAM Eq Impls Resp trace. In this case it's pretty ideal. However, should there be any delay spread ( when a signal is transmitted over the air, it reflects and bounces off of things-the resulting fan out of the waves is called delay spread) it will show up here as various peaks outside of the central impulse response. The primary application of the equalizer's impulse-response display is for evaluating multi-path environments. Multi-path environments usually require longer filter lengths.

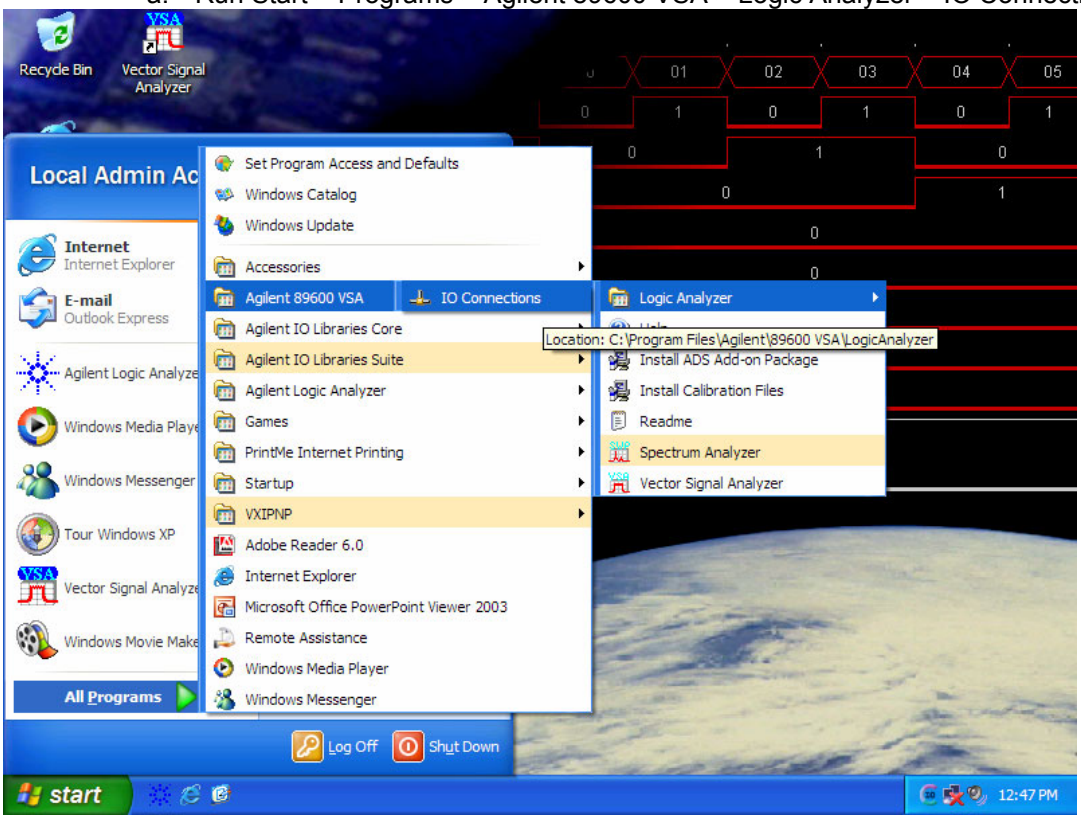
    b. If Adaptive is set to **hold**, the analyzer does not update the filter coefficients. Instead, the analyzer uses the last updated coefficients before selecting **hold**. However, in a very wideband signal (this 16QAM is quite wide), the equalizer can have a harder time converging, so we can simply allow it to perform it's calculations, and set it to hold for the best response.

c. Trace F shows the equalizer frequency response. The primary application of the equalizer's frequency-response display is for evaluating the transmitter or receiver signal-path for errors such as passband ripple and group-delay distortion. Short filter lengths usually work well for these types of measurements

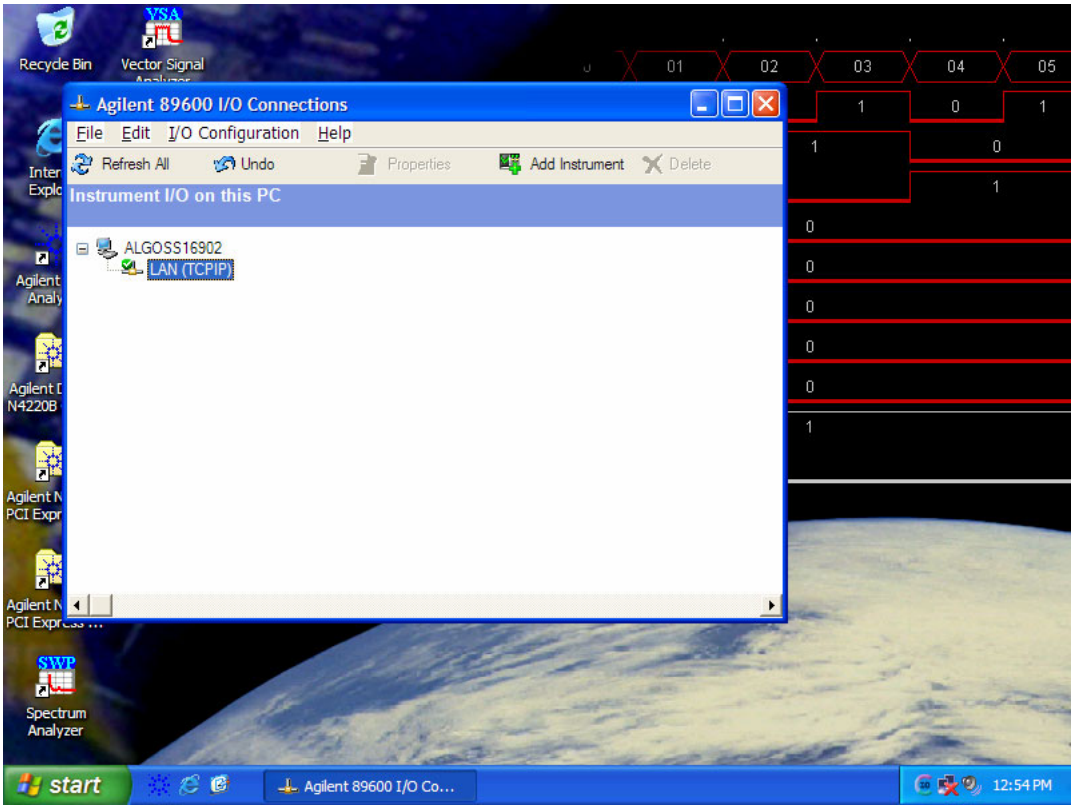


## Hardware Setup Steps

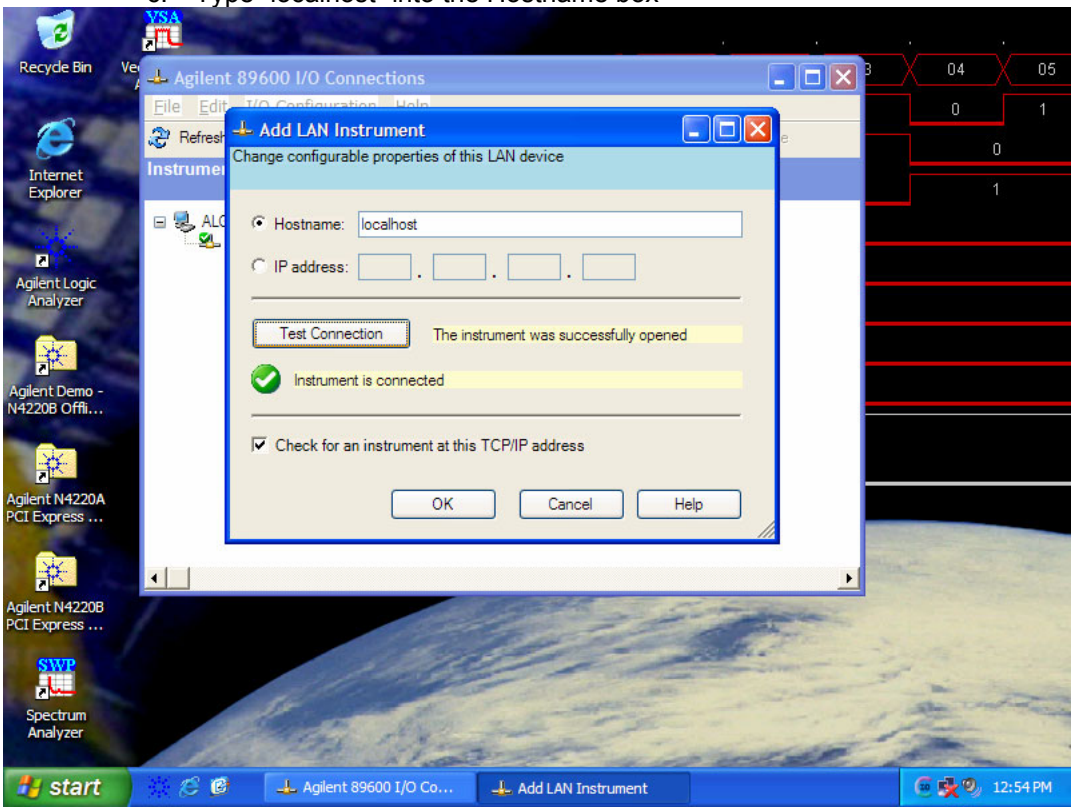
1. Install and license logic analyzer and VSA software.
2. Connect FPGA Demo Board to Pod 1 and Pod 3 of the LA.
3. Connect the VSA Software to the LA
    a. Run Start > Programs > Agilent 89600 VSA > Logic Analyzer > IO Connections




    b. Select LAN (TCPIP) and then click Add Instrument




c. Type “localhost” into the Hostname box




d. Press Test Connection to make sure the LA is connected

e. Confirm that the LA is added to the IO Connections (If LAN is not connected to the frame you will get an error on the connection even though the logic analyzer and VSA are connected.)