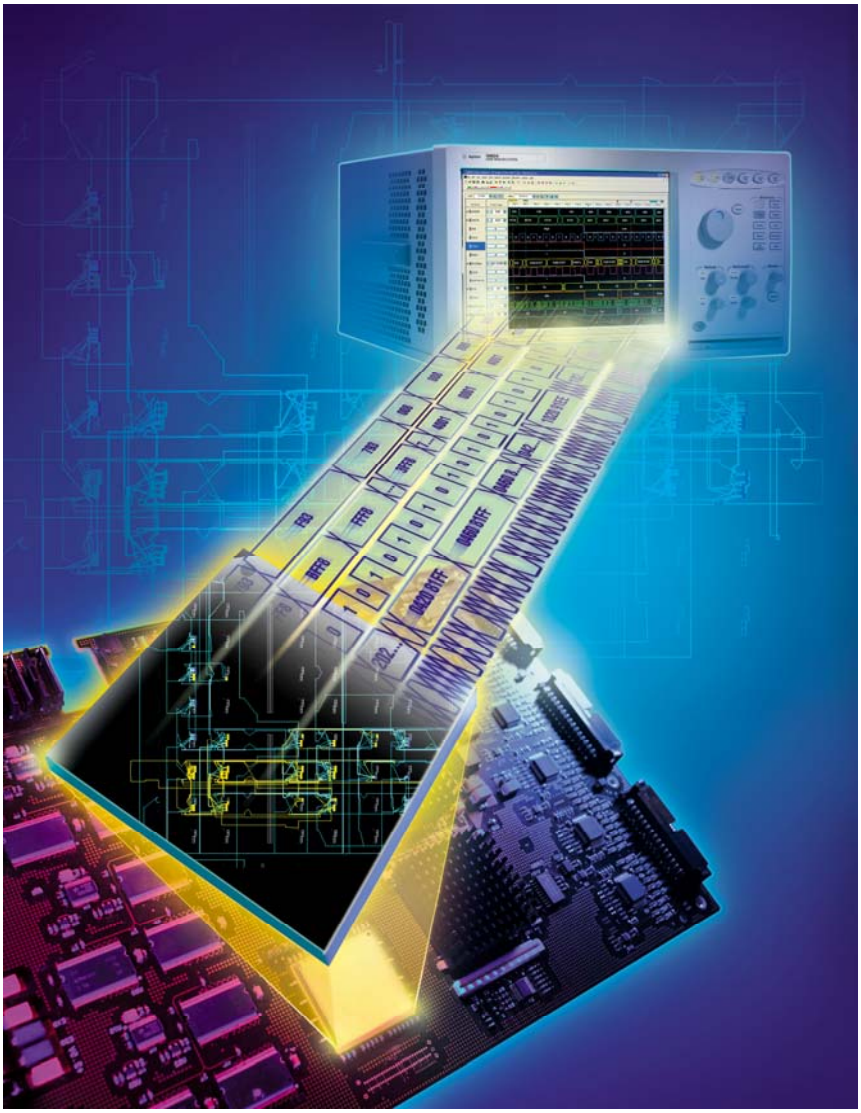


1 Altera FPGA Demo Quick Start

1.1 Download the updated B4656A Altera FPGA demo guide and files from the field portal http://field.cos.agilent.com/apps/fpga-debug/sales/#logic

1.2 The 'Files.zip' is included 2 folders and one setup file which are:

1.2.1 QProgrammer (Contains setup file named 'quartusii_60_sp1_programmer')

1.2.2 B4656A Altera FPGA Dynamic Probe Application software setup file named 'SetupProbeFPGAAltera03600002'

1.2.3 'Altera FPGA Demo Configuration Files' folder contains 4 configuration files named:

- ALTERA_FLYING_LEADS_50MHz.lai
- ALTERA_FLYING_LEADS_50MHz.sof
- ALTERA_MICTOR_LA.LAI
- ALTERA_MICTOR_LA.SOF

1.3 To run the Altera FPGA demo, first, you have to install the QProgrammer (refer to **2.QProgrammer Installation Guide**) or Quartus II software (refer to **3.Quartus II Software Installation Guide**) on the Logic Analyzer because the USB Blaster installer will only be shown after the QProgrammer or Quartus II software is installed.
Note: For a basic demo, you will never need to use the Quartus II software --- it is just an extraction step of the USB Blaster driver.

1.4 Install the USB Blaster driver to Logic Analyzer by following the '**4.USB Blaster (JTAG) Driver Installation Guide**'.

1.5 Follow the '**5.B4656A Altera FPGA Dynamic Probe Software Installation Guide**' to install the B4656A application software.

1.6 Now, you can start to demonstrate the Altera FPGA demo by follow the demo guide either using a Flying lead set (see **7. Demo Guide for Flying Leads Set**) or Mictor probe (see **8.Demo Guide for Mictor Probe**).

(Note: all software is contained on provided CDs, or downloadable at:

http://field.cos.agilent.com/apps/fpga-debug/sales/#logic

Since 16800 and 16900 logic analyzers do not have a CD-ROM, you will either need an external USB CD-ROM, or you will need to transfer files from the provided CDs to a USB thumb drive and then from the thumb drive to the logic analyzer)

Demo Requirements:

Hardware

1. 1680, 1690, 16800, 16900 Series software version 03.55 or greater
2. Altera Stratix demo board
3. Altera JTAG cable (with attached USB cable to Logic Analyzer)

Software

1. Altera JTAG driver software (QProgrammer.exe) installed on Logic Analyzer
2. Agilent FPGA dynamic probe application SW installed on Logic Analyzer
3. Altera .sof configuration file and .lai naming files
    a. ALTERA_FLYING_LEADS_50MHz.sof
    b. ALTERA_FLYING_LEADS_50MHz.lai or
    c. ALTERA_MICTOR_LA.sof
    d. ALTERA_MICTOR_LA.lai

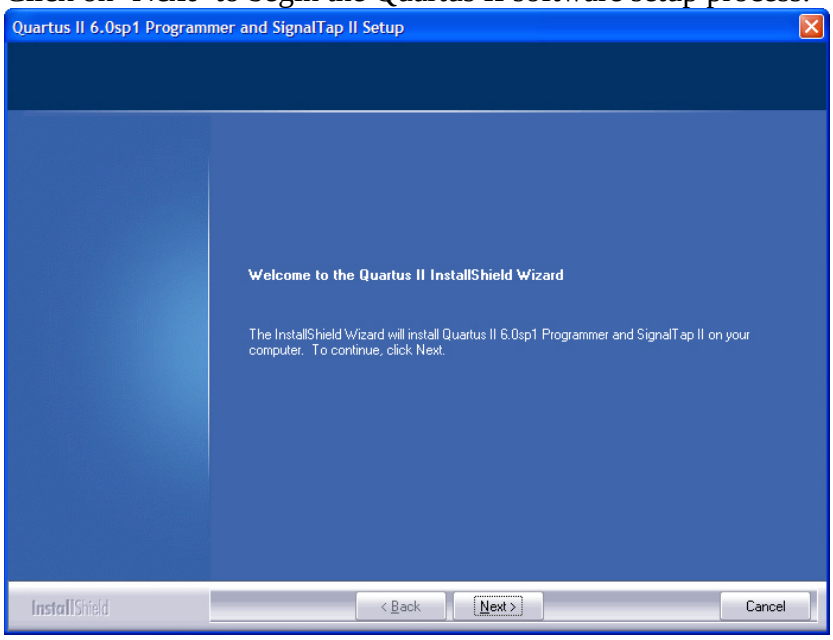
Probing

1. Flying Leads or Mictor Probe

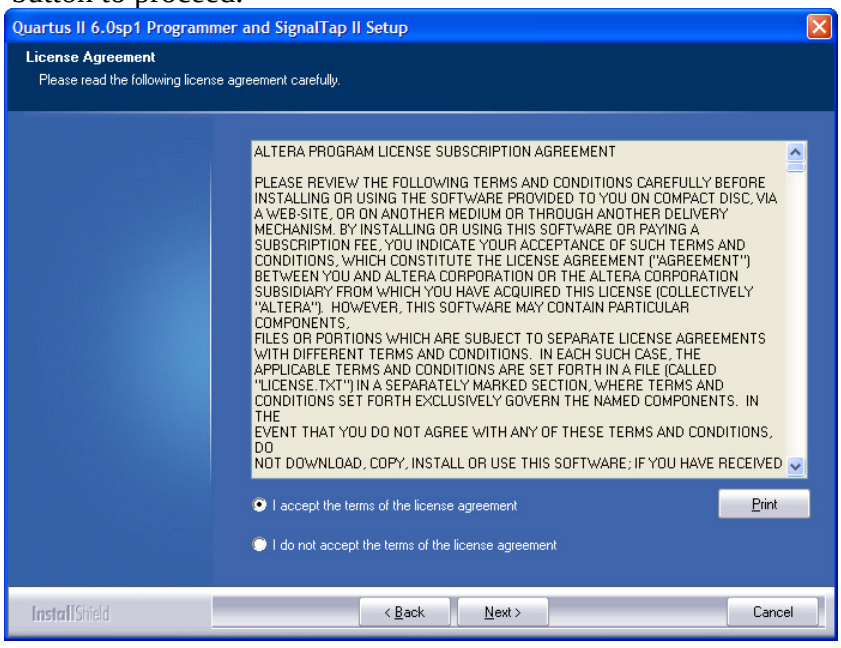
2 QProgrammer Installation Guide

2.1 Click on the '**quartusii_60_sp1_programmer.exe**' icon to begin the QProgrammer installation.

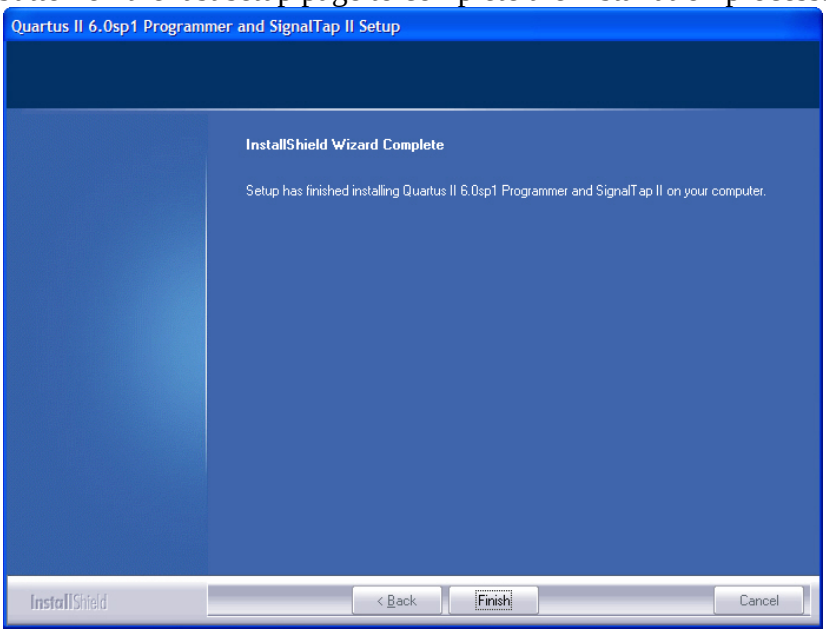
2.2 Click on '**Next**' to begin the Quartus II software setup process.



2.3 Select '**I accept the terms of the license agreement**' and click on the '**Next**' button to proceed.



2.4 Keep using the default setting in the following setup processes (you do have to provide some text in the Company Name text box) and click on the '**Finish**' button on the last setup page to complete the installation process.

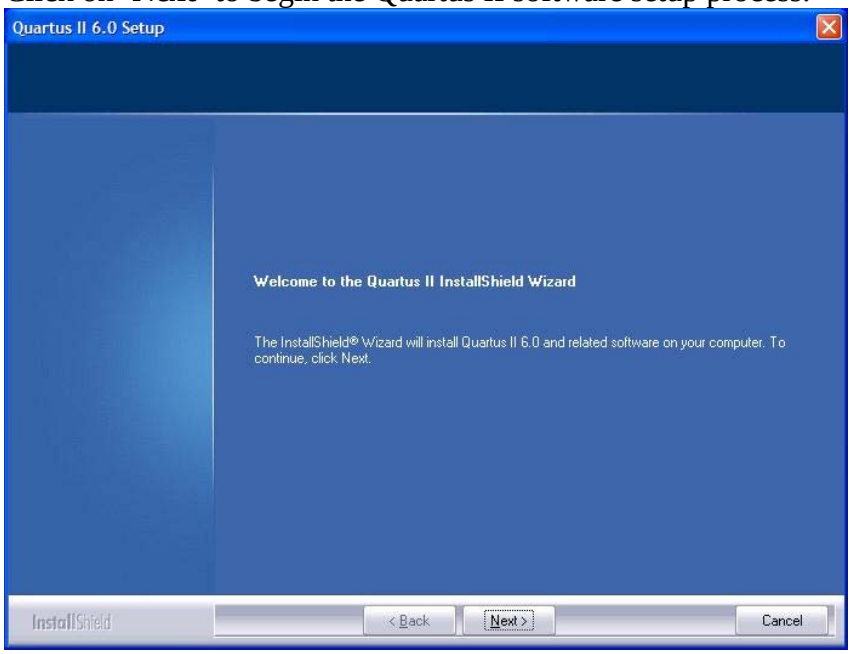


3 Quartus II Software Installation Guide

3.1 Install the Quartus II Design Software by using the provided 2 Setup disks named Quartus II Design Software for Windows.

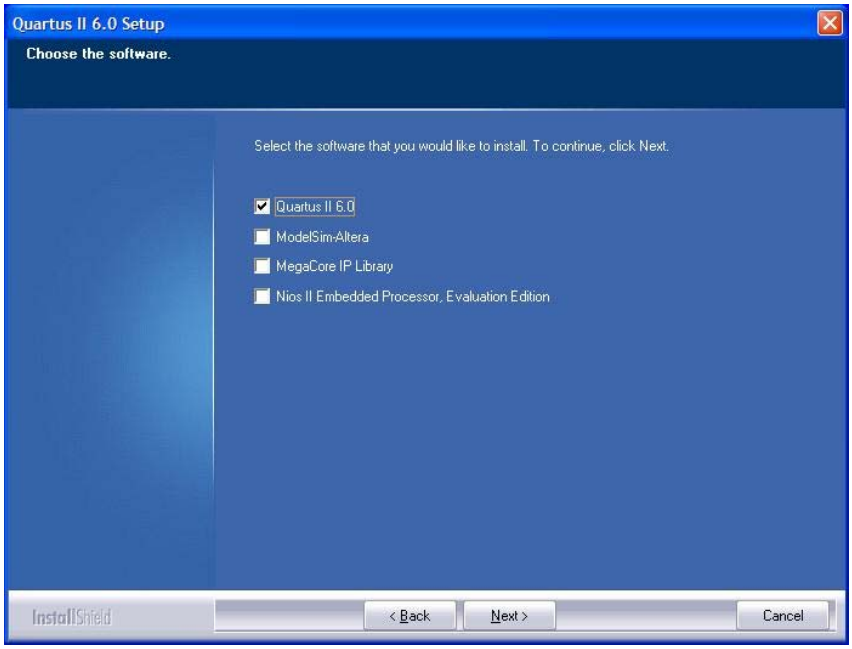
3.2 Click on the '**Install Quartus II and Related Software**' button on the installation beginning window.

3.3 Click on '**Next**' to begin the Quartus II software setup process.

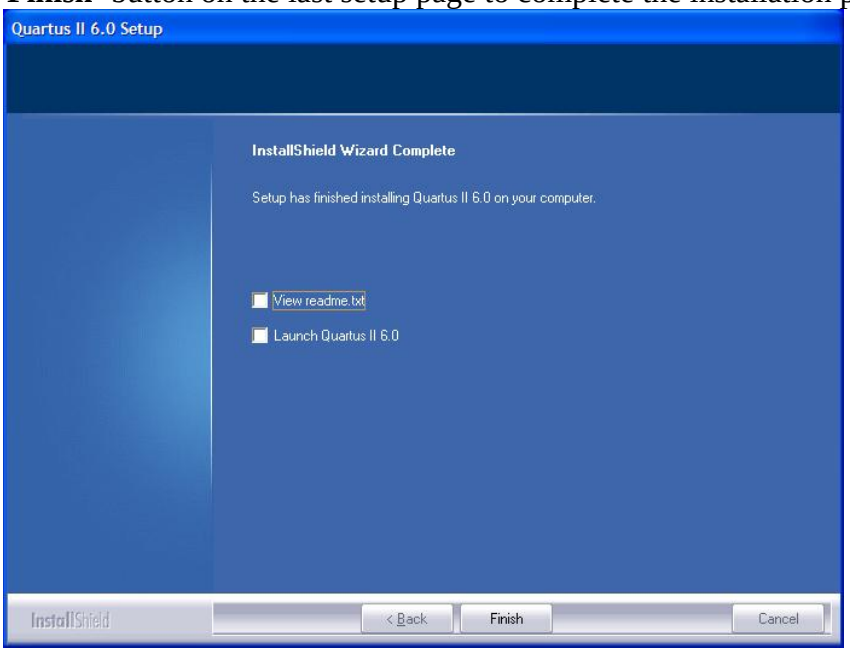


3.4 Checked the **Quartus II 6.0** and click on the '**Next**' button to proceed.

Note: You don't need to install the rest of the software if you just require to install the USB Blaster driver.



3.5 Keep using the default setting in the following setup processes and click on the '**Finish**' button on the last setup page to complete the installation process.



4 USB Blaster (JTAG) Driver Installation Guide

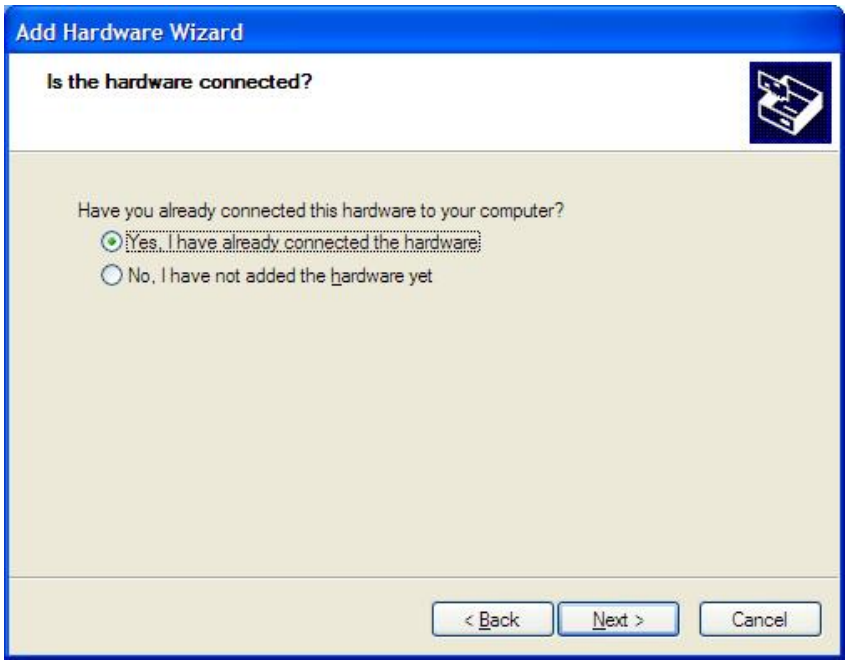
Remarks:

i. **Either the Quartus II development environment or QProgrammer must be first installed on the system.**
ii. **The user must have system administration (Administrator) privileges to install the USB Blaster download cable drivers**
iii. **Make sure the USB Blaster (JTAG) cable is connected between demo board and Logic Analyzer with demo board turned on.**

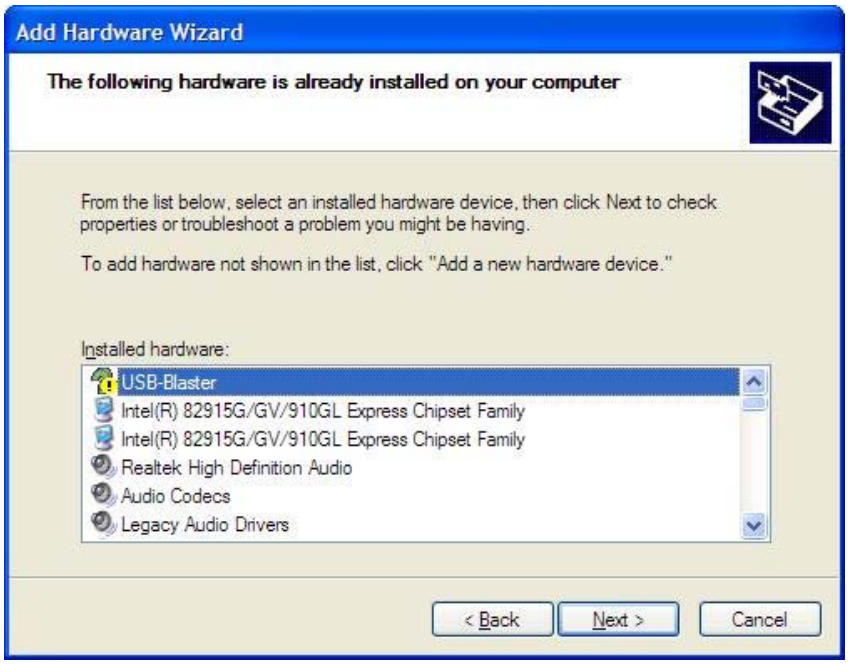
4.1 If this is the first attempt at install, you will be prompted with the Found New Hardware Wizard. If the wizard is canceled, the USB Blaster will be added to the Windows Device Manager as an Unknown Device. It may be necessary to go into Control Panel…System…Device Manager and uninstall the Unknown Device if this happens and then proceed with the following instructions. For Windows XP, click on the Start menu, and then select '**Control Panel**'.

4.2 Double-click the '**Add Hardware**' icon to start the Add Hardware Wizard and click on '**Next**' to continue.

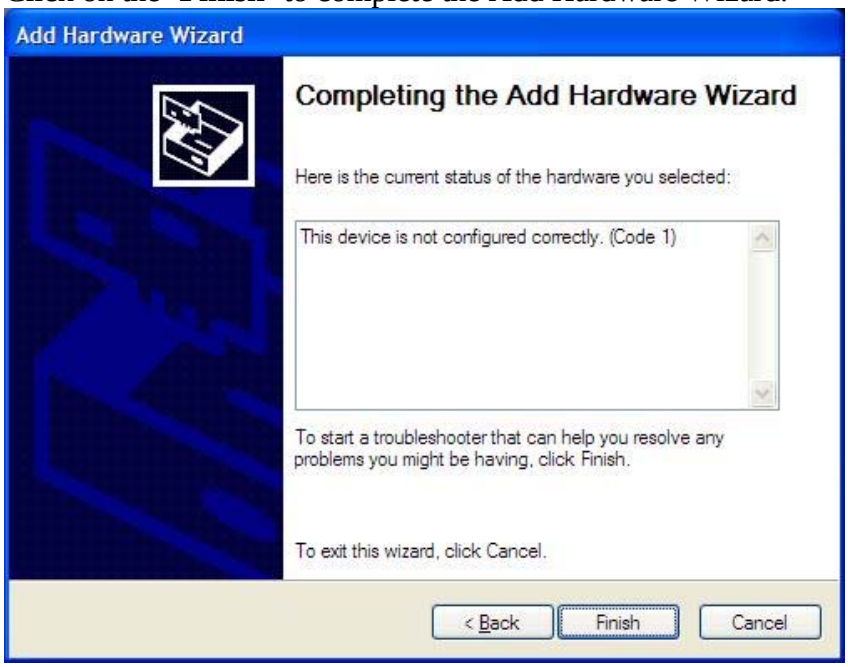
4.3 Select '**Yes, I have already connected the hardware**' and click on '**Next**' to continue.



4.4 Select '**USB-Blaster**' in the Installed hardware list, and click on '**Next**' to continue.



4.5 Click on the '**Finish**' to complete the Add Hardware Wizard.

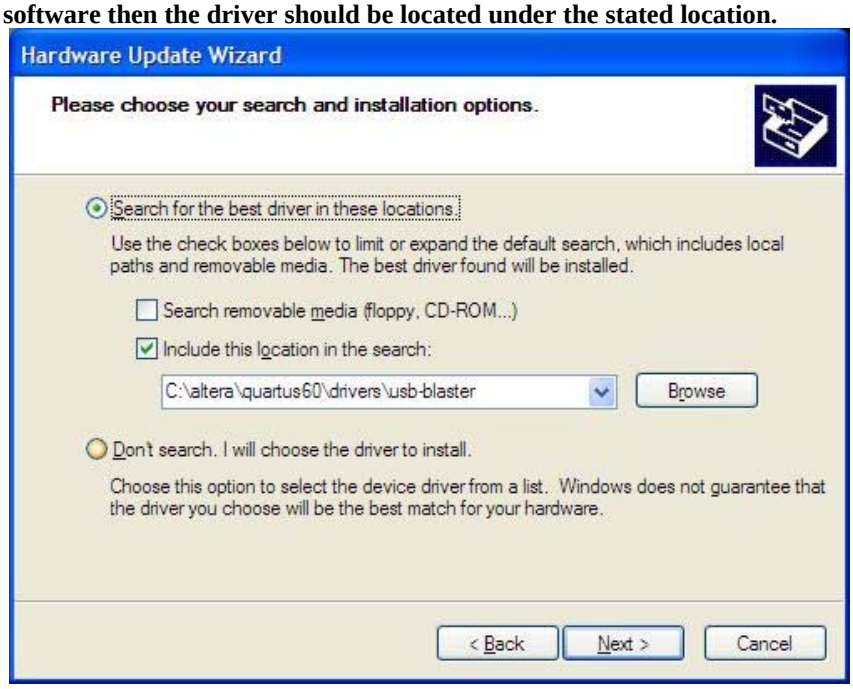


4.6 The '**Hardware Update Wizard**' will automatically show on the screen as per the figure shown below. Select '**No, not this time**' and click on '**Next**' to continue.

4.7 Select 'Install from a list or specific location (Advance)' and click on 'Next' to continue.

4.8 Select '**Search for the best driver in these locations**' and browse to the location of the driver directory of your QProgrammer (c:\altera\qprogrammer\drivers\usb-blaster) or Quartus II software (c:\altera\quartus60\drivers\usb-blaster) installation. Click on '**Next**' to continue.

Note: If you are using the default setting while installing the QProgrammer or Quartus II software then the driver should be located under the stated location.



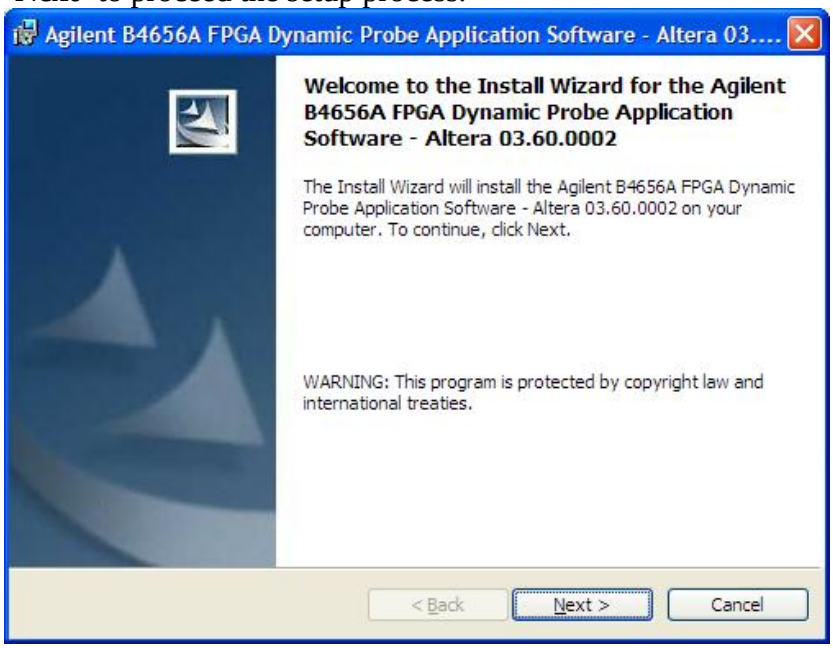
4.9 Select **Continue Anyway** when the hardware installation warning appears.

4.10 Select **Finish** in the Completing the Add/Remove Hardware Wizard window.

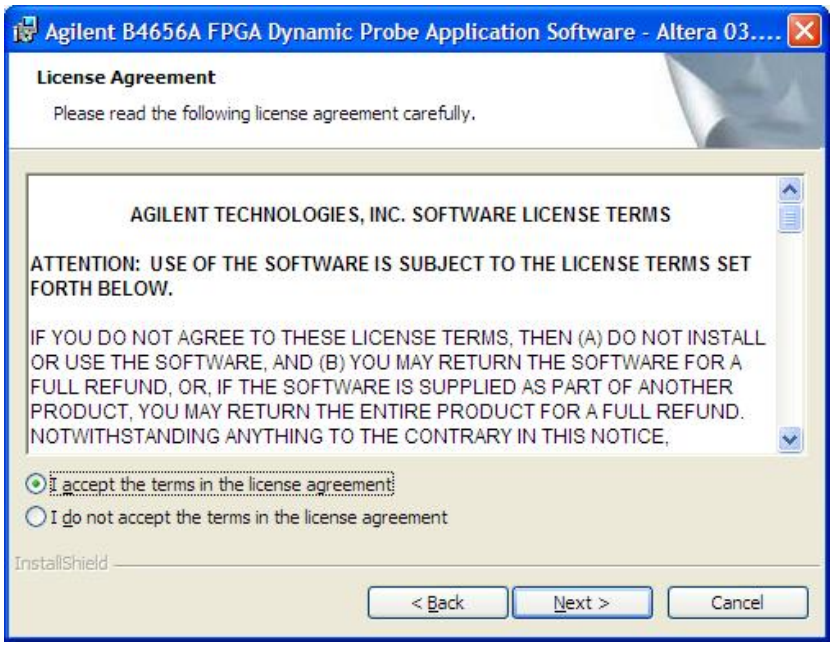
4.11 Reboot the computer.

5 B4656A Altera FPGA Dynamic Probe Software Installation Guide

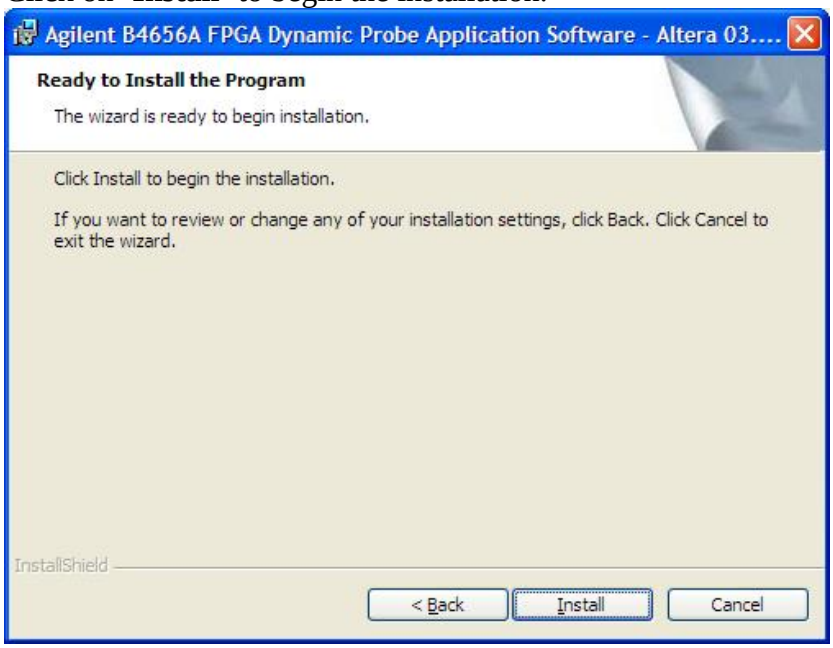
5.1 Double click on the '**SetupProbeFPGAAltera03600002**' setup file. Click on '**Next**' to proceed the setup process.



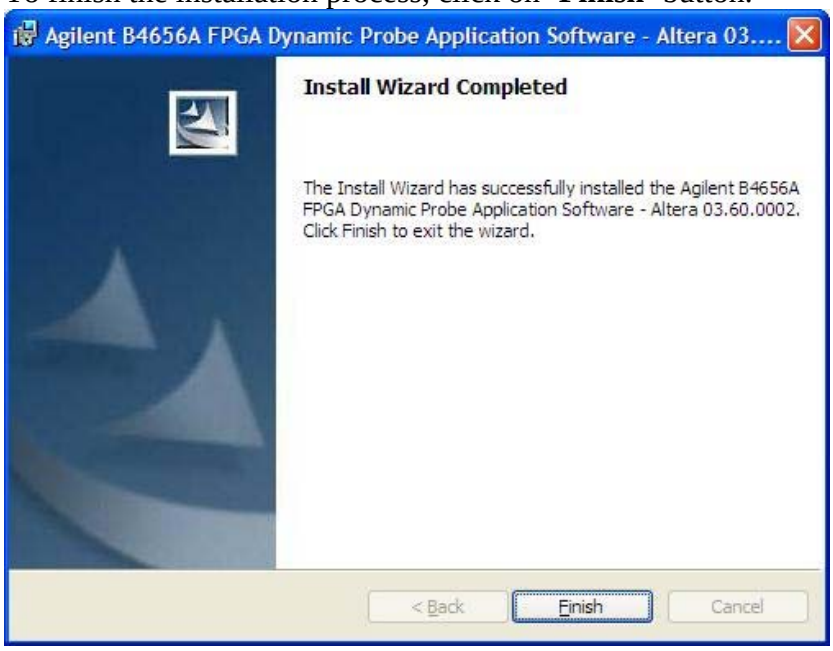
5.2 Select '**I accept the terms in the license agreement**' and click on '**Next**' to continue.



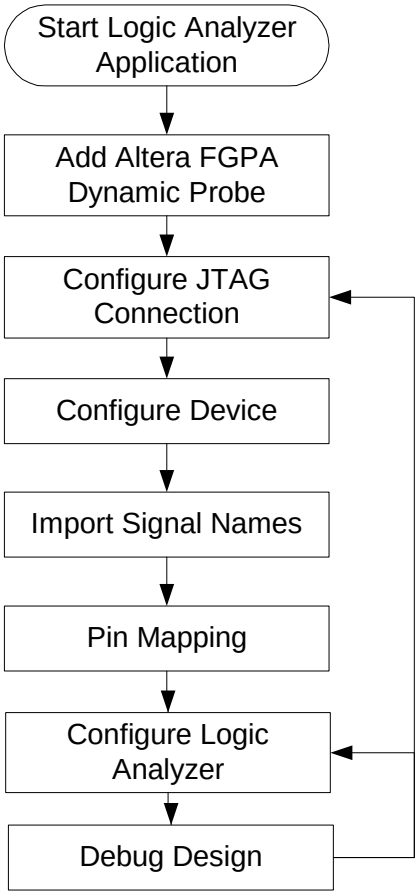
5.3 Click on '**Install**' to begin the installation.



5.4 To finish the installation process, click on '**Finish**' button.



6 Altera FPGA debugging Process flow



7 Demo Guide for Flying Leads Set

7.1 Connect the connections according to the figure shown below.

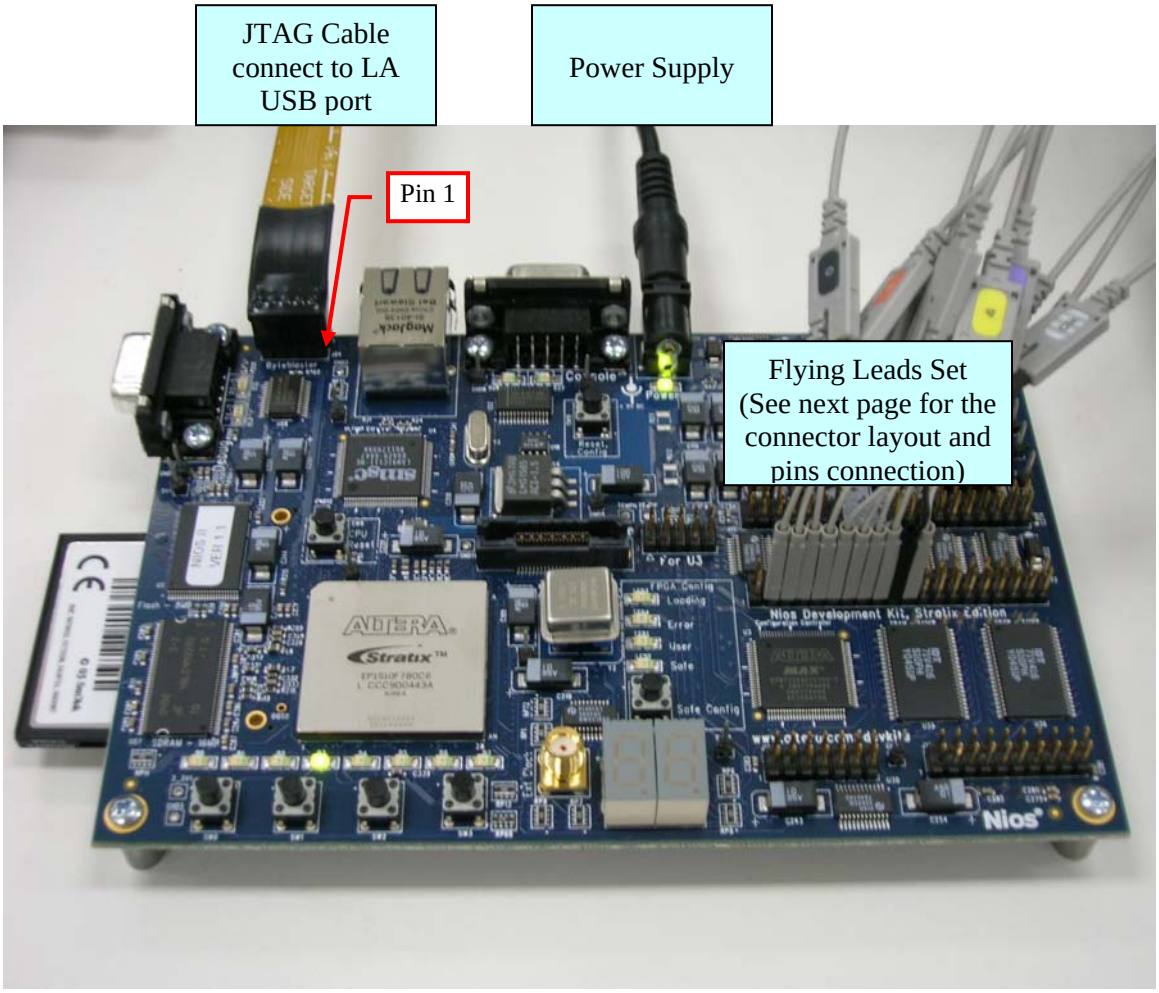
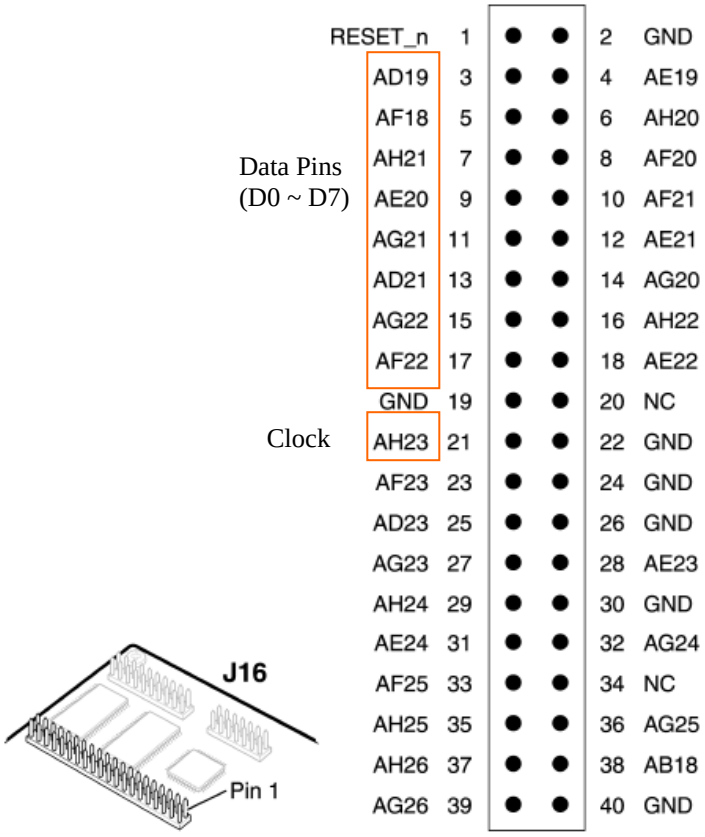


Figure 1–8. Expansion Prototype Connector - J16



LA Channel	Altera board pin location
Ch0	3
Ch1	5
Ch2	7
Ch3	9
Ch4	11
Ch5	13
Ch6	15
Ch7	17
Clock	21
Digital Grounds	2, 22

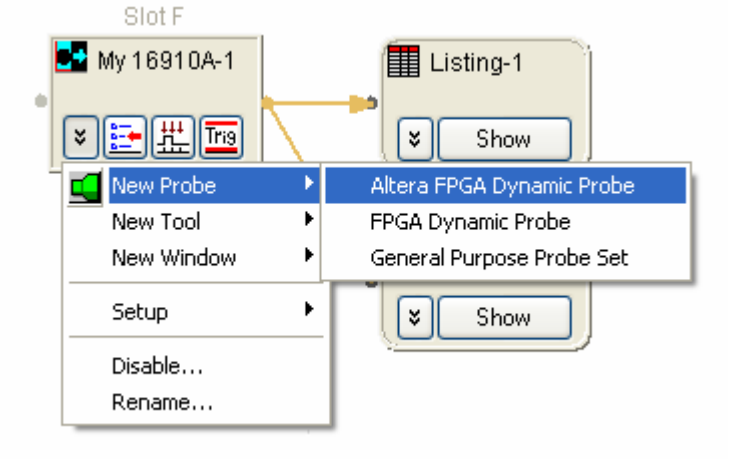
Remarks:

a) Connect the flying leads to pins 3, 5, 7, 9, 11, 13, 15 and 17 as your 8 data pins. The 50 MHz clock is on pin 21.

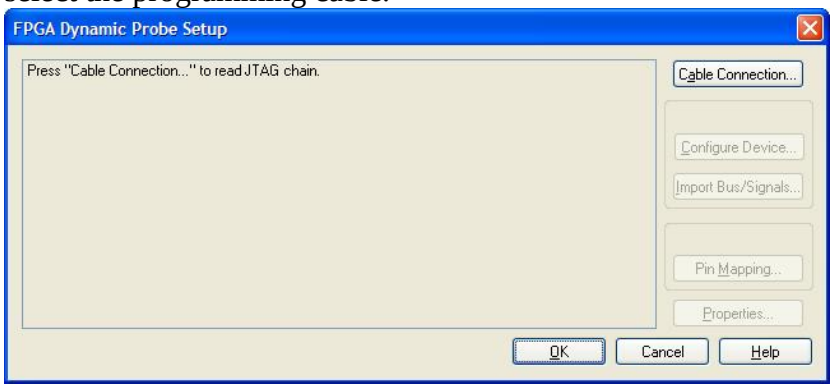
b) The demo contains of 4 Banks:

i. Bank0 – 8-bit up counter
ii. Bank1 – 8-bit down counter
iii. Bank2 – 3-bit state machine that cycles through sIdle(000), sReading(001), sWriting(010), and sWait(100). The machine is idle for 16 states, then writes one state, waits one state then is idle again for 16 states. Next it will read for two states, wait one and idle again. And repeat
iv. Bank3 – Loads 0x5555 and then performs a shift; kind of a pseudo PRBS.

7.2 To add the Altera FPGA Dynamic Probe the user will right click on the Logic Analyzer in the Overview tab. From the pop up select '**New Probe**' then '**Altera FPGA Dynamic Probe**'.



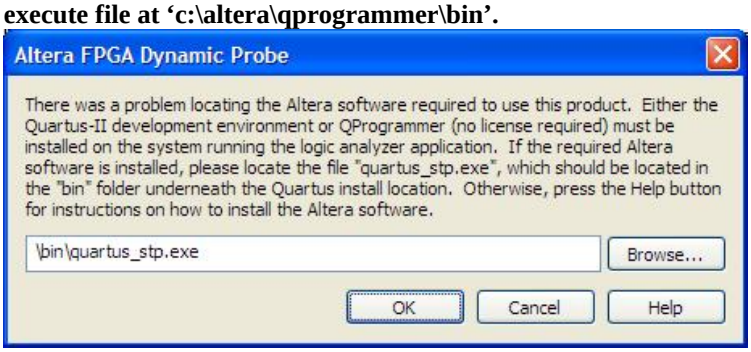
7.3 The FPGA Dynamic Probe Setup window will automatically appear on the screen as per the figure shown below. Click on the '**Cable Connection**' to select the programming cable.



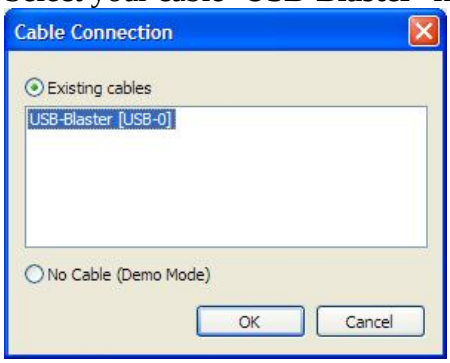
Note:

i. **The Altera FPGA Dynamic Probe can read the JTAG chain and identify devices on the chain.**

ii. **The message window as shown in figure below will be appeared if the user installed the USB Blaster by using QProgrammer. Browse the 'quartus_stp.exe' execute file at 'c:\altera\qprogrammer\bin'.**

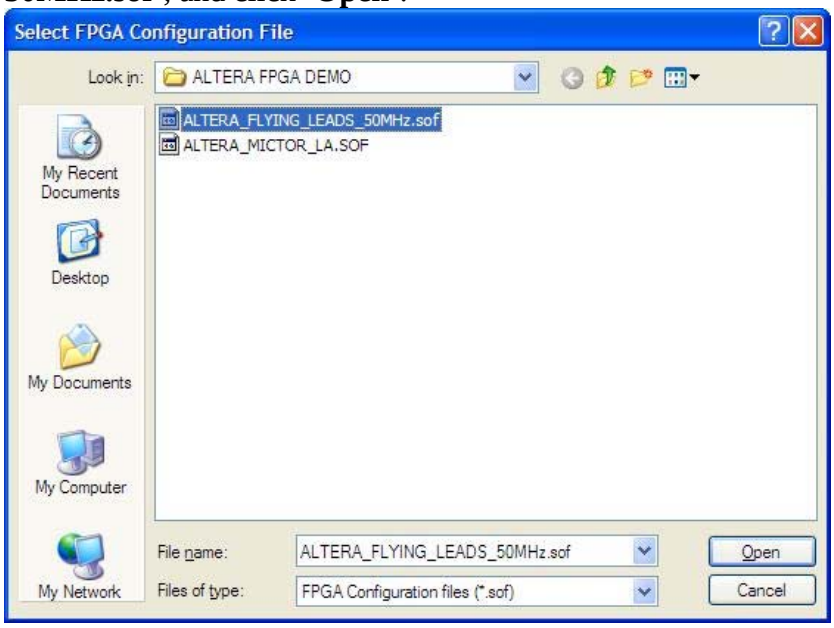


7.4 Select your cable '**USB-Blaster**' from the list of Existing cables and hit '**OK**'.

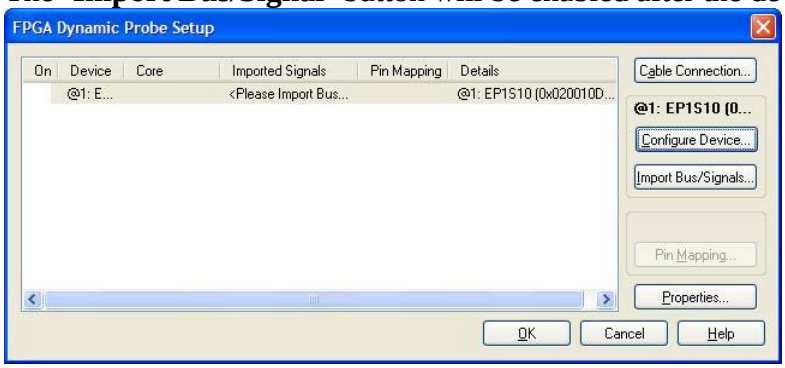


7.5 Devices on the JTAG chain will be displayed on the FPGA Dynamic Probe Setup window.

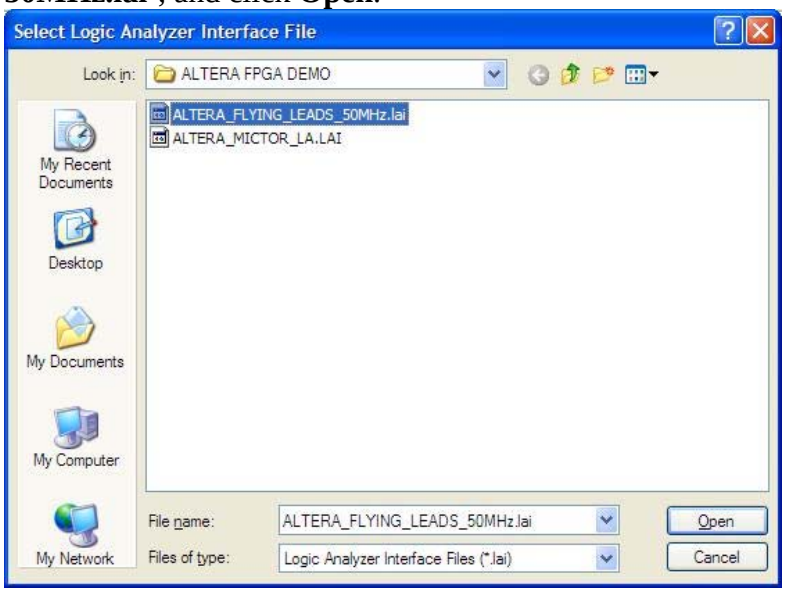
7.6 Click on '**Configure Device**' to select the FGPA configuration file. Navigate to the location of the .sof file, select '**ALTERA FLYING LEADS 50MHz.sof**', and click '**Open**'.



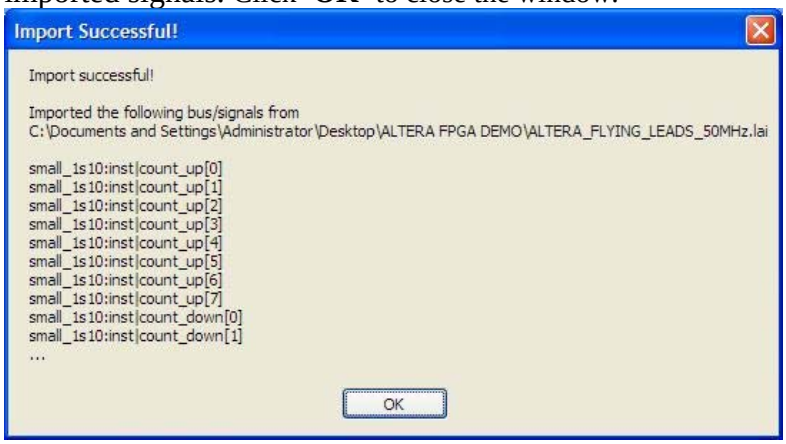
7.7 The '**Import Bus/Signal**' button will be enabled after the device is configured.



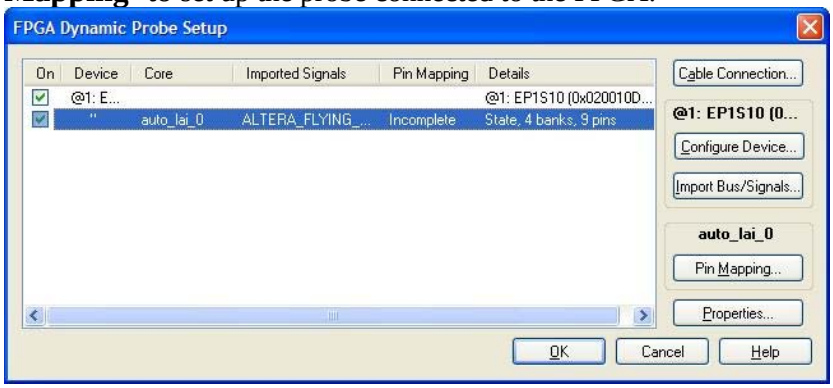
7.8 Click on **'Import Bus/Signals**' to select the Logic Analyzer Interface file. Navigate to the location of the .lai file, select '**ALTERA FLYING LEADS 50MHz.lai**', and click **Open**.



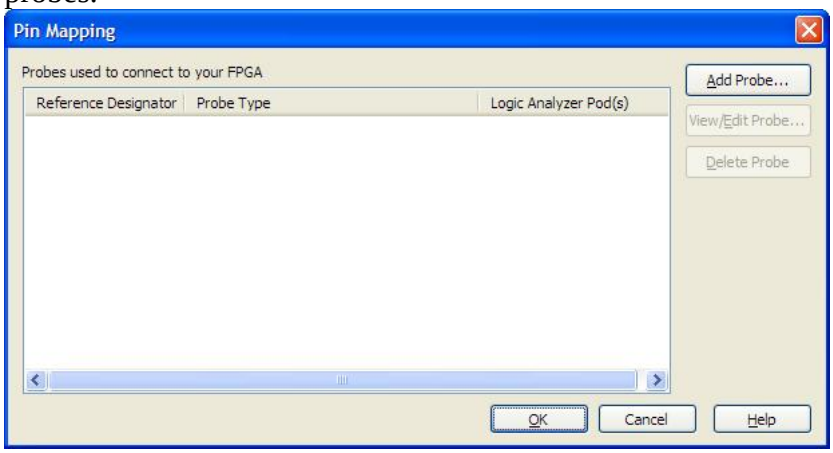
7.9 A pop-up window will show the import status and display a subset of the imported signals. Click '**OK**' to close the window.



7.10 The setup window will display the core details: number of pins, number of banks, and capture mode. Select the required core and click on the '**Pin Mapping**' to set up the probe connected to the FPGA.

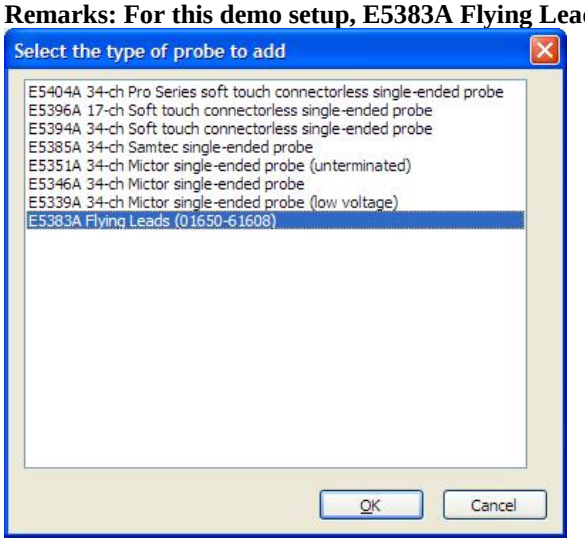


7.11 In the Pin Mapping window, click on '**Add Probe**' to define the type of the probes.

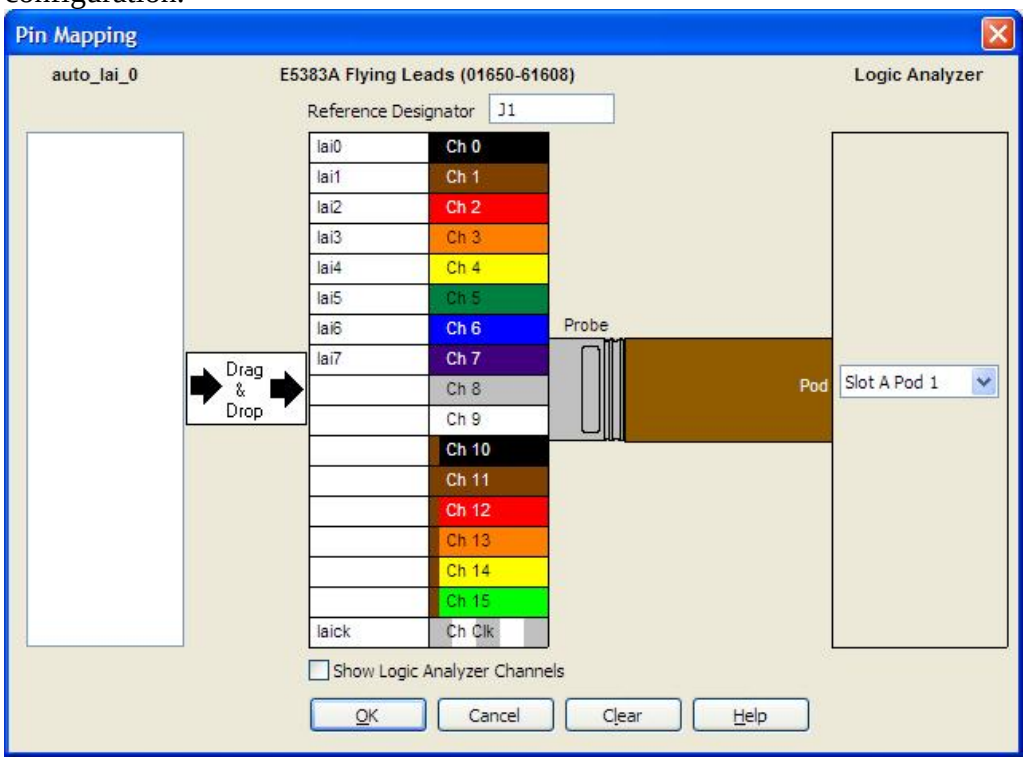


7.12 From the list, select the specific probe being used.

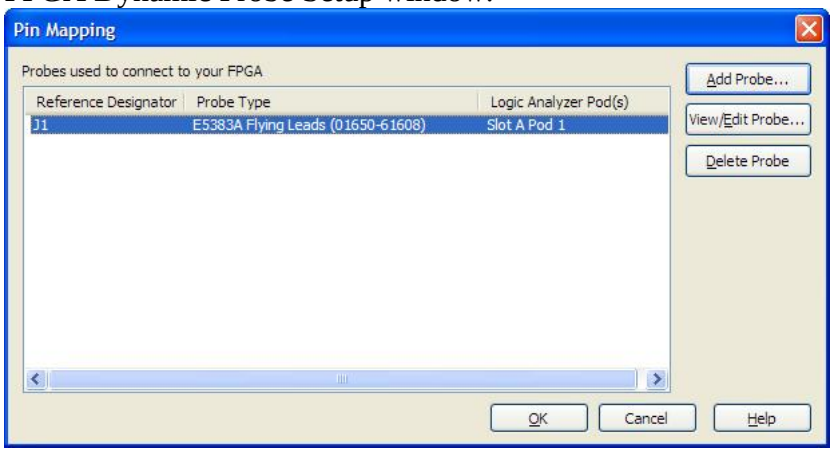
Remarks: For this demo setup, E5383A Flying Leads is being used.



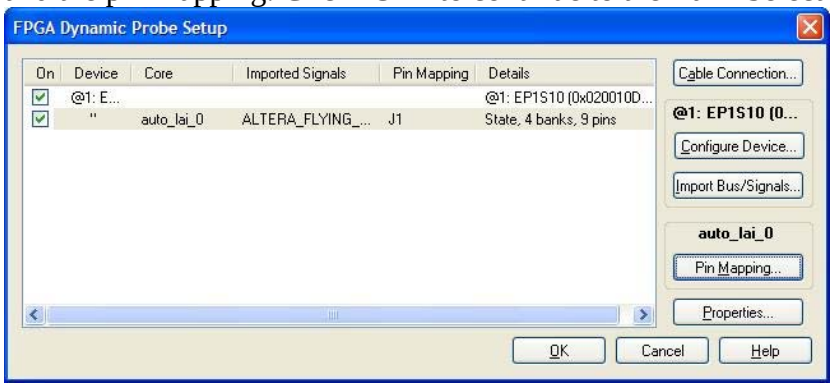
7.13 The Pin Mapping window will be shown after the selected the probe being used. Drag and drop LAI pins to Logic Analyzer channels and pods as per the configuration shown on the figure below. Click '**OK**' to confirm the configuration.



7.14 The Pin Mapping window should now display the selected Probe type and Logic Analyzer pod. Click '**OK**' to save the pin mapping and return to the FPGA Dynamic Probe Setup window.



7.15 The Setup window should now display the core details, the imported signals, and the pin mapping. Click '**OK**' to continue to the Bank Selection.



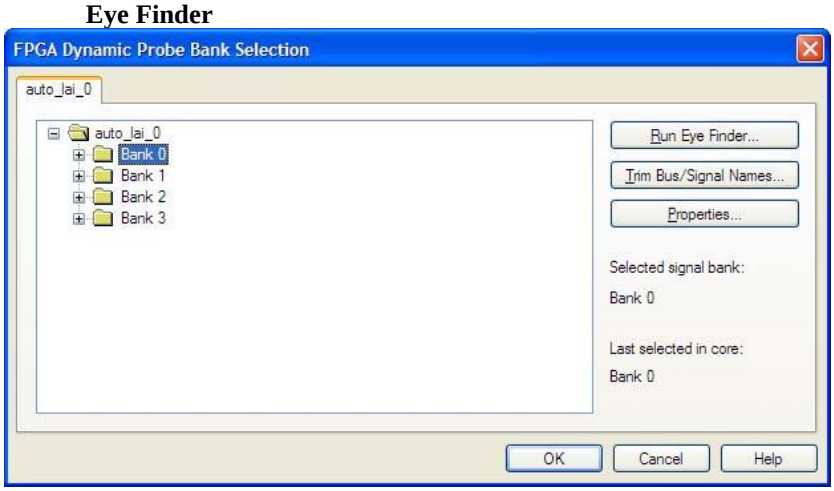
7.16 In the FPGA Dynamic Probe Bank Selection window, the user can select the bank to be probed.

Note:

i. **It is highly recommended to run eye finder (Auto sample position setup) on Bank 3 to ensure that the logic analyzer samples valid data before proceeding with a demo of the other banks.**

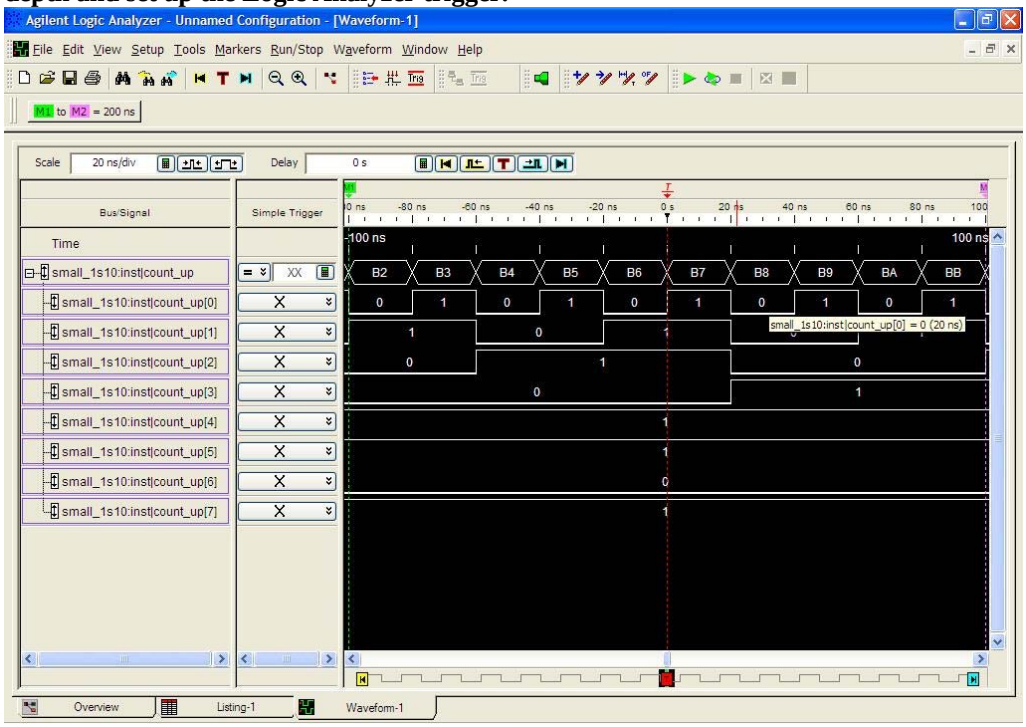
ii. **Recommended to demonstrate the capability by switching between Bank 0 (Count up) and Bank 1 (Count Down).**

iii. **This window displays the banks available and can be expanded to see individual signals. If the core is a state core the user may run Eye Finder by clicking Run Eye Finder**



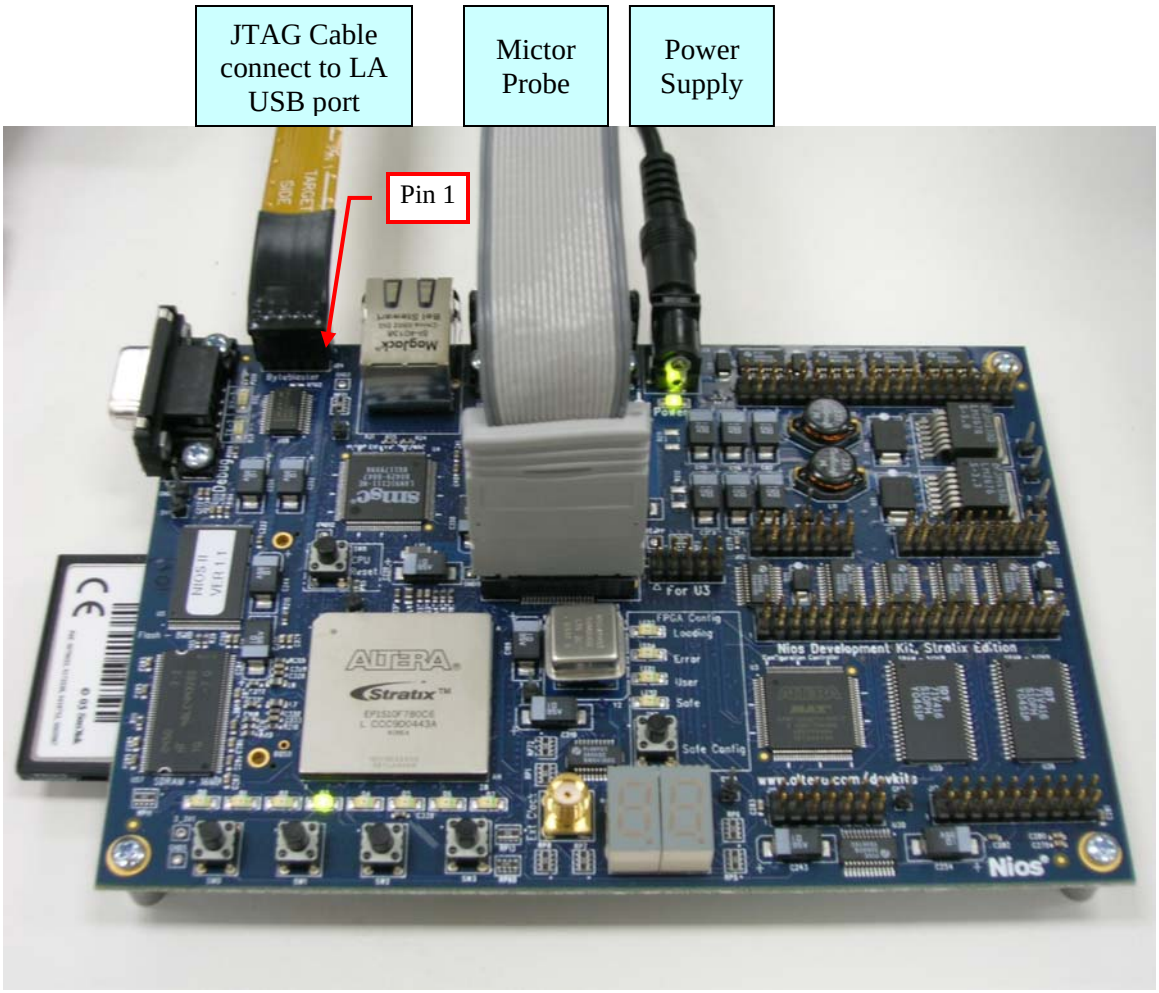
7.17 The system is now set up to debug the FPGA design.

Note: The Logic Analyzer will be setup according to parameters read from the LAI file. This included clocking, labels, and capture mode. The user can now modify acquisition depth and set up the Logic Analyzer trigger.



8 Demo Guide for Mictor Probe

8.1 Connect the connections according to the figure shown below. (Since there is no shroud on the Mictor, take care not to put force on the Mictor Probe Adapter in a way that might break the connector on the board)

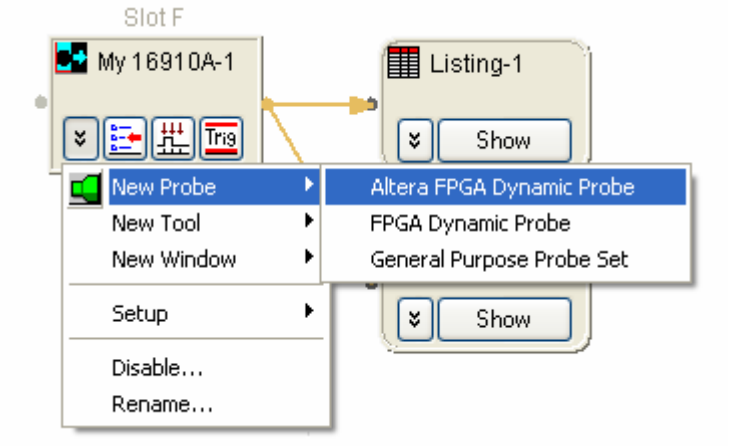


Remarks:

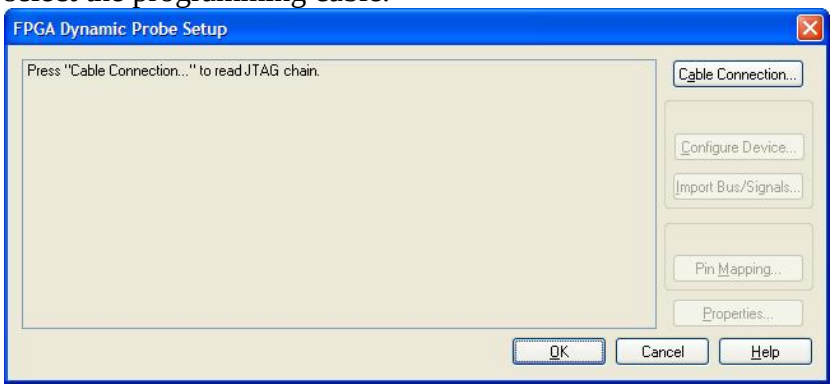
a) The demo contains of 4 Banks:

i. Bank0 – 8-bit up counter
ii. Bank1 – 8-bit down counter
iii. Bank2 – 3-bit state machine that cycles through sIdle(000), sReading(001), sWriting(010), and sWait(100). The machine is idle for 16 states, then writes one state, waits one state then is idle again for 16 states. Next it will read for two states, wait one and idle again. And repeat
iv. Bank3 – Loads 0x5555 and then performs a shift; kind of a pseudo PRBS.

8.2 To add the Altera FPGA Dynamic Probe the user will right click on the Logic Analyzer in the Overview tab. From the pop up select '**New Probe**' then '**Altera FPGA Dynamic Probe**'.



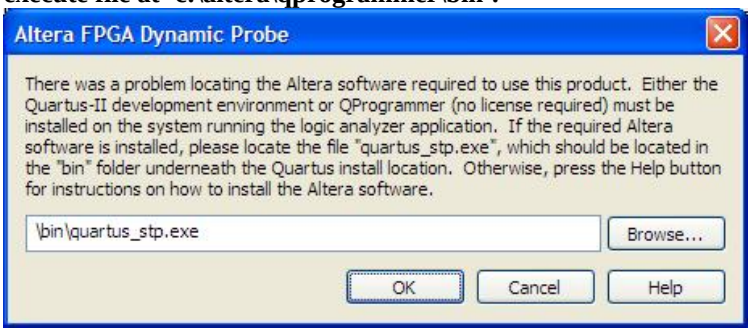
8.3 The FPGA Dynamic Probe Setup window will automatically appear on the screen as per the figure shown below. Click on the '**Cable Connection**' to select the programming cable.



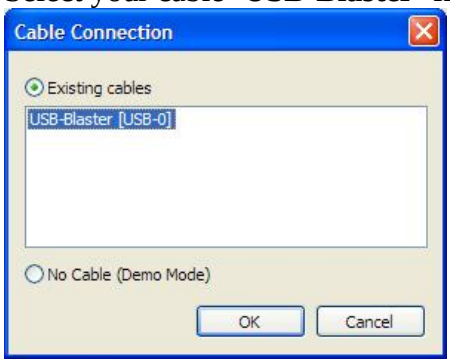
Note:

i. **The Altera FPGA Dynamic Probe can read the JTAG chain and identify devices on the chain.**

ii. **The message window as shown in figure below will be appeared if the user installed the USB Blaster by using QProgrammer. Browse the 'quartus_stp.exe' execute file at 'c:\altera\qprogrammer\bin'.**

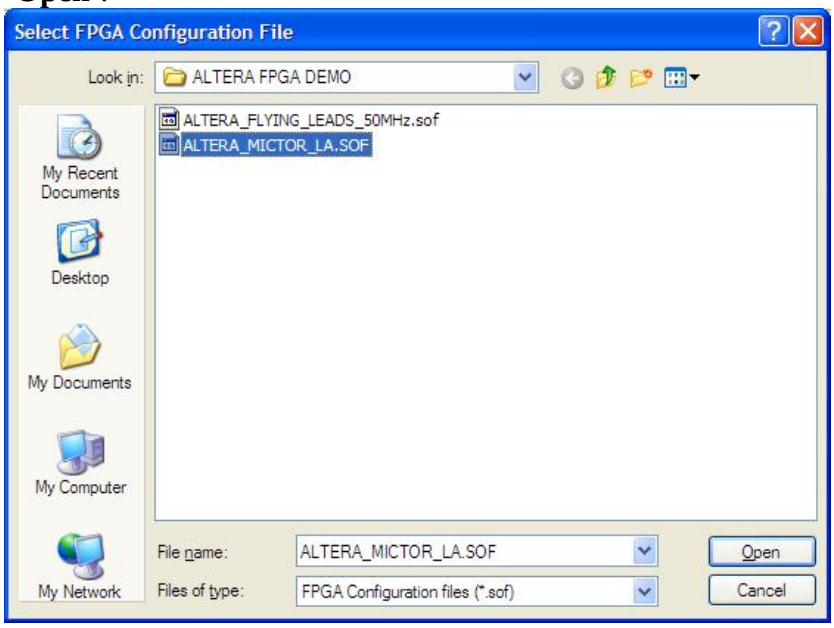


8.4 Select your cable '**USB-Blaster**' from the list of Existing cables and hit '**OK**'.

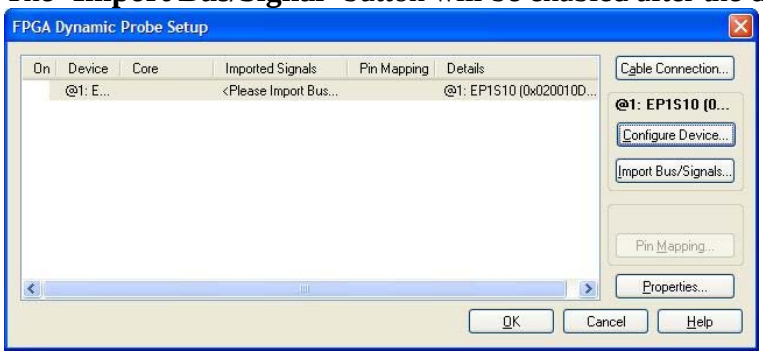


8.5 Devices on the JTAG chain will be displayed on the FPGA Dynamic Probe Setup window.

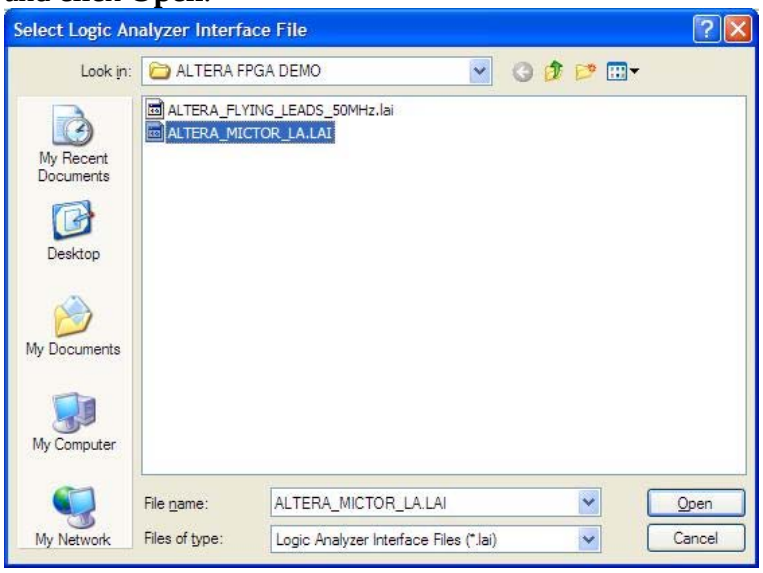
8.6 Click on '**Configure Device**' to select the FGPA configuration file. Navigate to the location of the .sof file, select '**ALTERA MICTOR LA.sof**', and click '**Open**'.



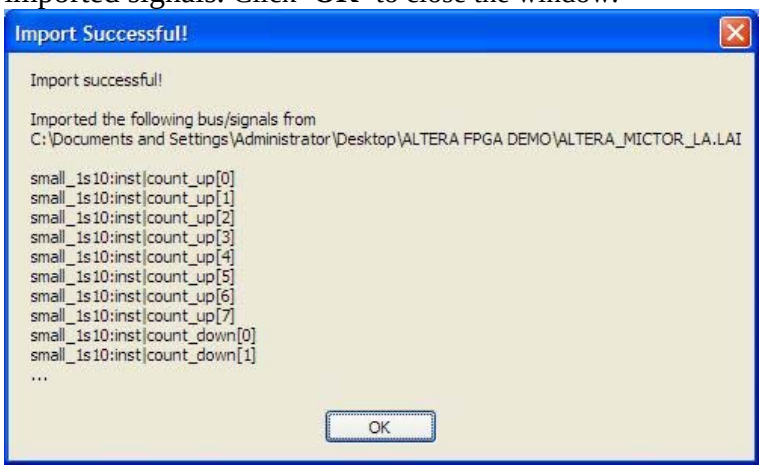
8.7 The '**Import Bus/Signal**' button will be enabled after the device is configured.



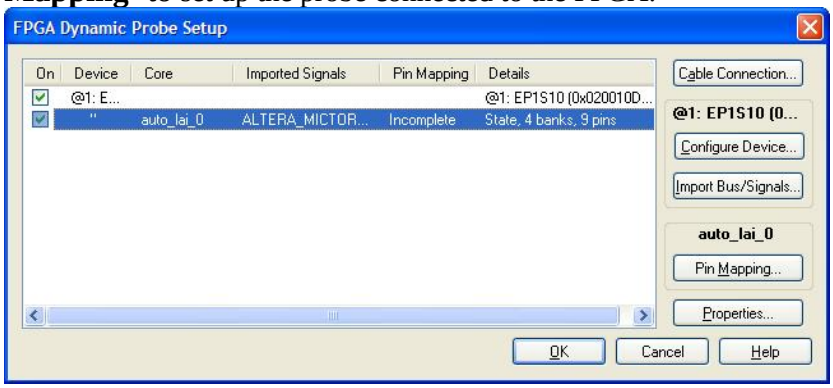
8.8 Click on **'Import Bus/Signals**' to select the Logic Analyzer Interface file. Navigate to the location of the .lai file, select '**ALTERA MICTOR LA.lai**', and click **Open**.



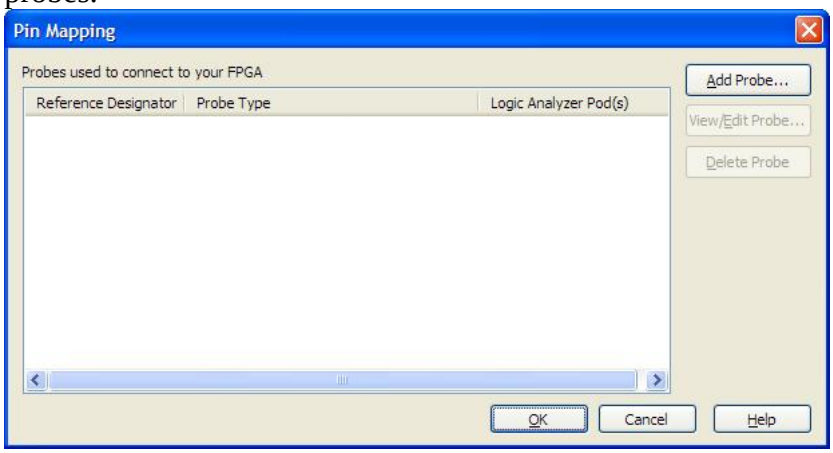
8.9 A pop-up window will show the import status and display a subset of the imported signals. Click '**OK**' to close the window.



8.10 The setup window will display the core details: number of pins, number of banks, and capture mode. Select the required core and click on the '**Pin Mapping**' to set up the probe connected to the FPGA.

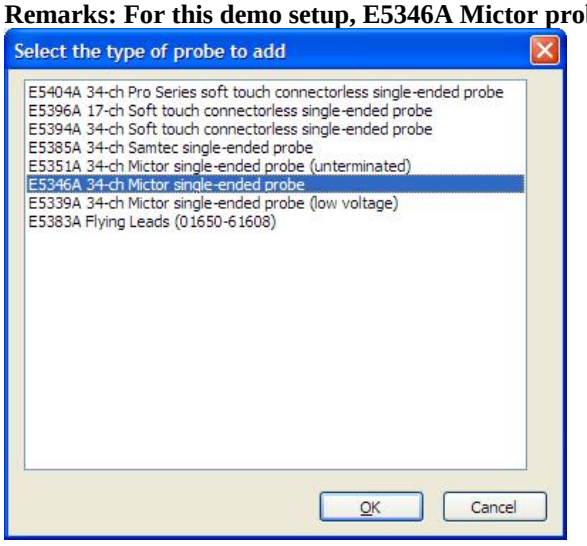


8.11 In the Pin Mapping window, click on '**Add Probe**' to define the type of the probes.

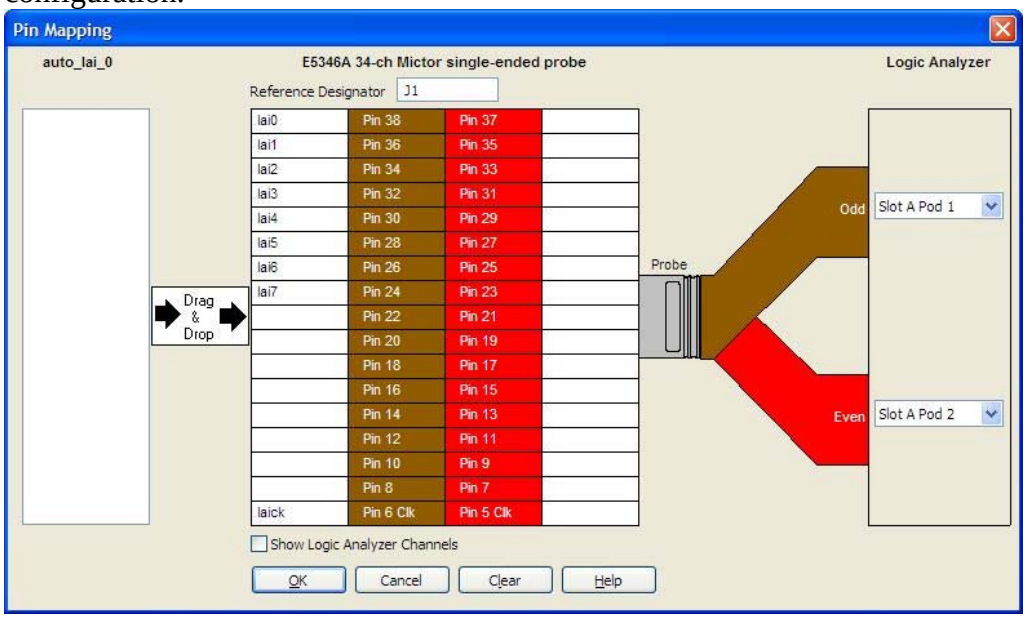


8.12 From the list, select the specific probe being used.

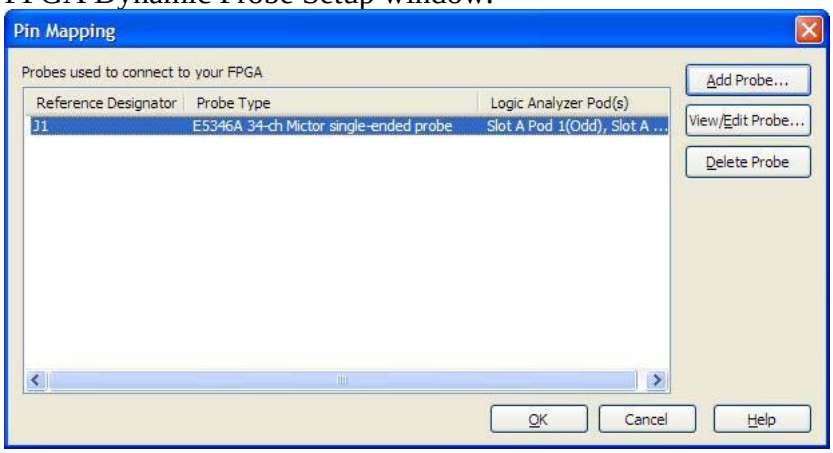
Remarks: For this demo setup, E5346A Mictor probe is being used.



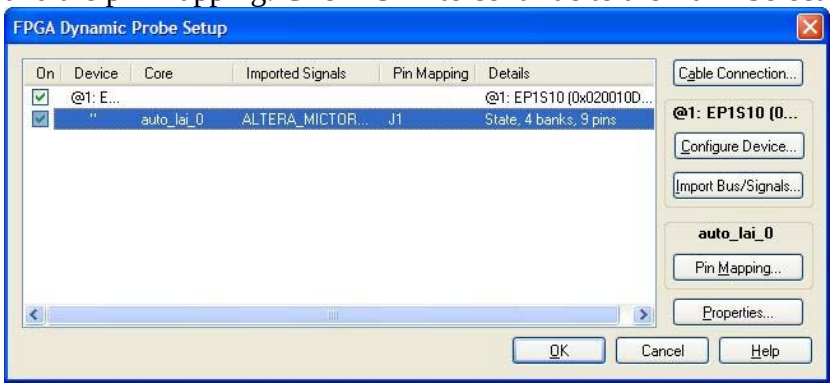
8.13 The Pin Mapping window will be shown after the selected the probe being used. Drag and drop LAI pins to Logic Analyzer channels and pods as per the configuration shown on the figure below. Click '**OK**' to confirm the configuration.



8.14 The Pin Mapping window should now display the selected Probe type and Logic Analyzer pod. Click '**OK**' to save the pin mapping and return to the FPGA Dynamic Probe Setup window.



8.15 The Setup window should now display the core details, the imported signals, and the pin mapping. Click '**OK**' to continue to the Bank Selection.

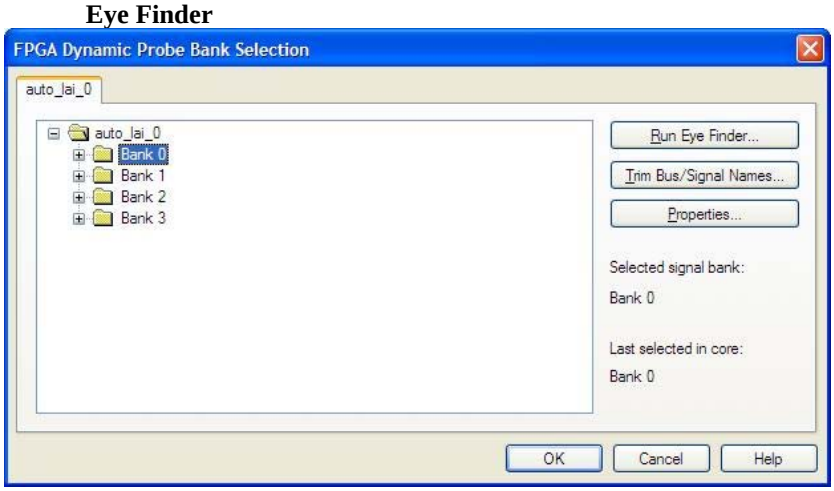


8.16 In the FPGA Dynamic Probe Bank Selection window, the user can select the bank to be probed.

Note:

i. **Recommended to demonstrate by switching between Bank 0 (Count up) and Bank 1 (Count Down).**

ii. **This window displays the banks available and can be expanded to see individual signals. If the core is a state core the user may run Eye Finder by clicking Run Eye Finder**



8.17 The system is now set up to debug the FPGA design.

Note: The Logic Analyzer will be setup according to parameters read from the LAI file. This included clocking, labels, and capture mode. The user can now modify acquisition depth and set up the Logic Analyzer trigger.