

Frequently Asked Questions

B4655A FPGA Dynamic Probe

March 15, 2004

This document addresses common questions whose answers are not found in FPGA dynamic probe datasheet available at www.agilent.com/find/FPGA.

Agilent's FPGA dynamic probe provides greater real-time measurement productivity for logic-analysis based validation of FPGAs and the surrounding system. The tool features:

- o Increased visibility -- Traditional logic analyzer probes limit engineers to measuring signals at the periphery of the FPGA. With Agilent's FPGA dynamic probe, engineers are able to measure up to 64 internal FPGA signals for each debug pin (external FPGA pin dedicated to debug).
- o Faster probing changes -- Agilent's FPGA dynamic probe enables design teams to move probe points internal to the FPGA in a mouse click--without any design changes, and without any changes to the timing of your design.
- o Automatic setup of the logic analyzer -- FPGA dynamic probe maps internal signal names from your FPGA design tool to your logic analyzer. The signal naming capability of the Agilent FPGA probe eliminates mistakes and the time needed to manually setup signal and bus names and logic analyzer connections, yielding a significant advantage over logic analyzers without this capability.

Q. How do I create an ATC2 core?

A. Xilinx ChipScope Pro provides this capability and is required for ATC2 core creation and merge with the design. ChipScope Pro includes Core Generator and Core Inserter. Using either of these tools, the user can specify the parameters of the ATC2 core and can also specify which design signals go to the ATC2 making them available for real-time measurement.

Q. How do I get an ATC2 core into my design?

A. Xilinx Core Inserter puts the core into your FPGA design post synthesis. Xilinx Core Generator is for use with synthesis tools, and instantiates your parameterized ATC2 as a black-box Verilog or VHDL file. The instantiated core is put into your design during the synthesis process.

Q. What synthesis tools can Xilinx use to get the ATC2 core into my design?

A. ATC2 cores produced by Core Generator are compatible with:

- Exemplar Leonardo Spectrum
- Synopsys Design Compiler
- Synopsys Design Compiler II
- Synopsys FPGA Express
- Synplicity Synplify
- Xilinx XST

Q. Are there advantages to using Core Inserter versus Core Generator?

Yes. Core Inserter additionally produces a .cdc file. This is a small file listing the signal inputs to the ATC2 core. This file is used to automatically synchronize design signal names

with logic analysis bus and signal names. Agilent recommends using Xilinx Core Inserter so you can take advantage of signal name mapping.

Xilinx has a stimulus core known as VIO. This core can only be created and placed in design exclusively using Core Generator. For a single design that contains both a VO core and an ATC2, Core Generator must be used.

Q. How big is the core? How much of my device does it take?

Each input signal adds roughly 1 FPGA slice to the size of the ATC2 core. The ATC2 cores have been designed to be as small as possible. A Xilinx XCV2000 part with an ATC2 core configured with 32 signal banks and 6 signals per bank consumes less than 2% of the device resources.

The specific answer depends on what FPGA device you are using and also on the parameters (state/timing, # of signal banks, pin compression, # of debug pins) of the ATC2 core you've selected. The ATC2 core consumes no BUFGs (global clocks), nor DCMs (digital clock manager), or any block RAM resources. A formula can be used to approximate resource utilization. **The formula will be forthcoming.**

Q. How many of my FPGA resources does it consume?

A. Yes. We can send the customer an equation to use if they would like a more specific answer for the configuration of the core they wish to use.

Q. Do I pay royalties for the use of the core?

A. No. ATC2 cores are distributed as part of Xilinx ChipScope Pro. There are no associated royalties.

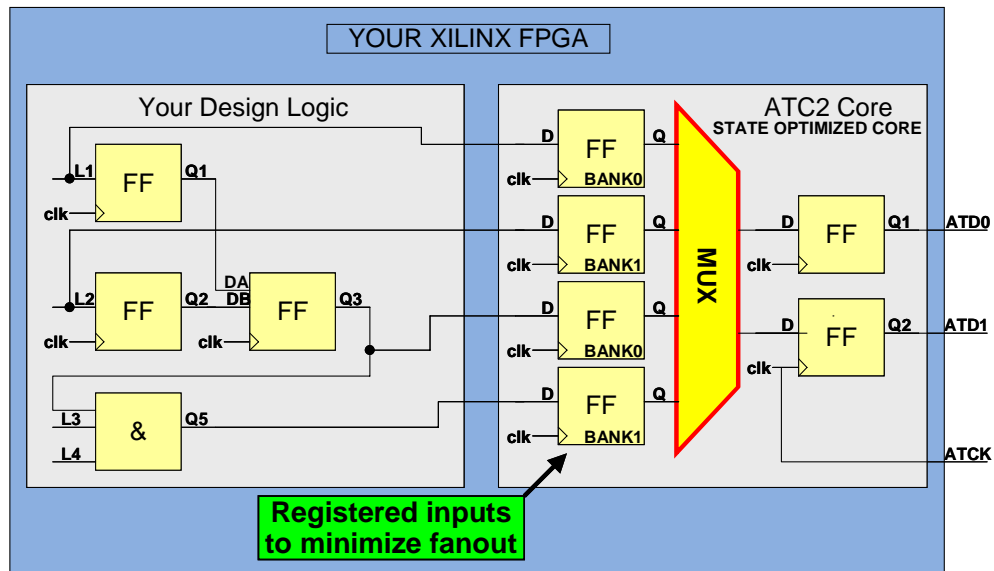
Q. Should I leave the ATC2 core in my design after validation is complete?

A. This decision is up to the user. A number of users prefer leaving debug cores in the design as removing the cores from the design will change design timing. The core can also be useful in doing debug once units are in the field, if needed. The ATC2 core is by default, "turned off" and wakes when communicated to from an Agilent logic analyzer. This feature saves power when the core remains in a shipping design.

Q. When would I want to use an ATC2 state core (synchronous) versus a timing (asynchronous) core?

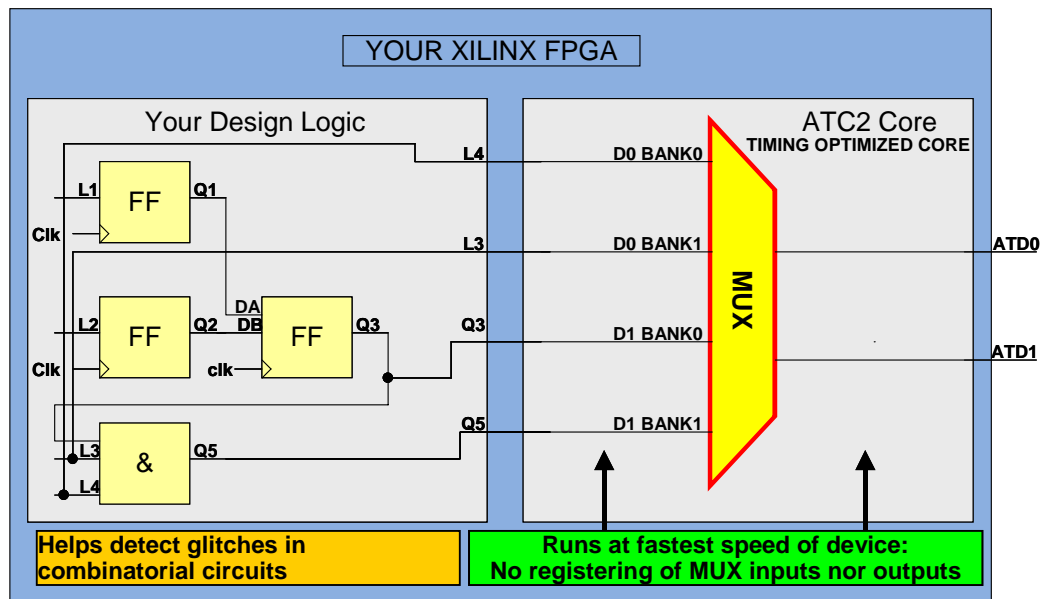
A. State cores:

- Provide most accurate measurement for functional debug in one time domain
- Register inputs to minimize fan out
- Support time division multiplexing for 2X pin reduction
- Support calibration for more accurate measurements on buses with narrow data valid windows



Timing cores:

- Are best for measurements across multiple time domains
- Run at fastest possible speed of device, no registering of MUX inputs nor outputs
- Have minimal impact on design timing



Q. What effect does the core have on my design's timing? After loading the ATC II, does it affect my signal routing?

A. The ATC2 core is a firm core. The core will not affect the synthesis of the design when the user creates and inserts the design using core inserter. The inclusion of ATC2 core in the design may affect the placement and routing of the overall FPGA design. In typical applications the

effect should be small. The effect on design timing will depend on how the core is configured (for example, the number of signals you choose per bank, and the total number of banks) and the number of resources available on the particular FPGA device being used.

State core: The ATC2 core adds one additional load (flop) on each signal probed. This load will affect the placement and routing to meet user-specified timing constraints. The ATC2 state core includes a flop that registers data. This flop helps the tools meet timing constraints for most types of designs. Internal to Agilent, we've created state cores for our FPGA designs that run @ 150MHz.

Timing core: The ATC2 timing core adds a wire load for each signal probed. This wireload is a false path that is ignored during place and route of the design. Hence, the timing core has minimal to no effect on design timing. Users can determine the skew between signals by viewing the delay file generated by the design tools to estimate this difference.

Once the ATC2 core (both state or timing core) is in the design, switching from signal bank to signal bank does not change design timing as all connections have been already made.

Q. What's the impact on FPGA performance?

A. The core will have some effect on performance, but it should not be significant. The effect on performance is directly related to timing constraints. The timing core is capable of running at the fastest internal FPGA speed of the device the customer is using. For the timing core, the sample rate on the logic analyzer will determine how often data is captured. For state cores, the maximum sample rate will be the lower of the speed of the FPGA time domain being measured or the maximum state speed of the logic analyzer. All supported logic analyzers have state speeds of 200Mhz and greater.

Q. How does the optional 2X pin compression technology work?

A. All signal inputs to the ATC2 state core are registered and clocked on the edge specified by the user. Internal to the core, the registered value of signal 1 is passed to the logic analyzer on the rising edge of the clock and the value of signal 2 is passed to the logic analyzer on the falling edge of the clock. The logic analyzer utilizes a de-multiplexing mode to decompress the information and preserve all triggering and analysis capabilities.

Q. If I have ATC2 signal banks with 64-bit width, how many pins and logic analyzer channels does it take with 2X pin compression turned on?

A. Simultaneous measurement of 64 signals requires 32 FPGA pins and 64 logic analysis channels. Only 32 of the logic analysis channels are physically connected to pins of the FPGA. The other 32 channels provide their acquisition memory and triggering resources for the measurement.

Q. Can I simulate the ATC2 core?

A. No. Agilent guarantees that the ATC2 core meets specifications and characteristics listed in our datasheet. The core has been debugged and tested by Agilent.

Q. What is the duration of the software license?

A. FPGA dynamic probe is licensed to a single logic analyzer (1680 series, 1690 series, or 16900 series). Specifically for 16900 Series mainframes or split 1680/90 Series analyzers, multiple instances of FPGA dynamic probe are provided so a single license can be used for all logic analysis modules in the mainframe.

Q. How will I be notified that my license is about to expire?

A. The 1 year license includes a 1 year software update service. This service includes free factory-pushed revisions to FPGA dynamic probe software and a notification service 60 days before the license expires. The notification will occur on the front panel of the Agilent logic analyzer where the application is installed. An email notification will also be sent to the address given at the time of software update service subscription.

Q. Who do I contact if I'm having problems?

A. Xilinx has ChipScope Pro expertise including inserting the core into your design. Agilent's expertise will be on the core and FPGA dynamic probe application. Agilent and Xilinx will work together on issues that cross company boundaries.

Q. What if I didn't assign all of the signals of interest early when I created the core?

A. You can still use Xilinx FPGA editor to route new input signals to the ATC2 core. However, a new .cdc file is not produced so signal name synchronization will need to be done manually. Alternatively, you can change input signals by recompiling the FPGA design with a new ATC2 core or new signal connections to the core.

Q. Can I use FPGA dynamic probe application to download configuration bits into my Xilinx FPGA?

A. Yes.

Q. What Xilinx JTAG cables work with FPGA dynamic probe?

A. Xilinx Parallel III cable, Parallel IV cable and Xilinx MultiLINUX cables.

Q. How does calibration work?

A. The core contains test generation circuitry to stimulate the signal banks and output pins. With this active data running, the logic analyzer invokes the eye finder feature to automatically adjust for variances in path delays through the core to the acquisition system on the logic analyzer.

Q. Do you use calibrate in timing mode?

A. No. Calibration works exclusively for ATC cores parameterized for state analysis.

Q. Can I use a different clock on each bank or do I need a clock with each bank?

A. Timing cores do not have a clock since information is sampled using the logic analyzer's internal clock. For state cores, the ATC2 core has a master clock that is used for all banks.

Q. Can multiple ATC2 cores be put in a single device?

A. Yes. FPGA dynamic probe application has been architected to support multiple cores in a single FPGA device. If the cores are state cores, each will need a clock from the design it is measuring.

Q. Does the tool also support Altera FPGAs?

A. No. Xilinx and Agilent collaboratively developed FPGA dynamic probe. It exclusively supports Xilinx Spartan-3, Virtex-II, and Virtex-II Pro FPGAs.

Q. I already design and use my own MUX structure to select signals for test. What advantage does FPGA dynamic probe and ATC2 core offer?

A. Agilent's ATC2 cores are optimized for use with Agilent logic analyzers (e.g. calibration for state cores) and are designed for minimal intrusion in your FPGA design. The integration with the logic analyzer for core control and signal naming are significant advantages that enhance your productivity. Other advantages include:

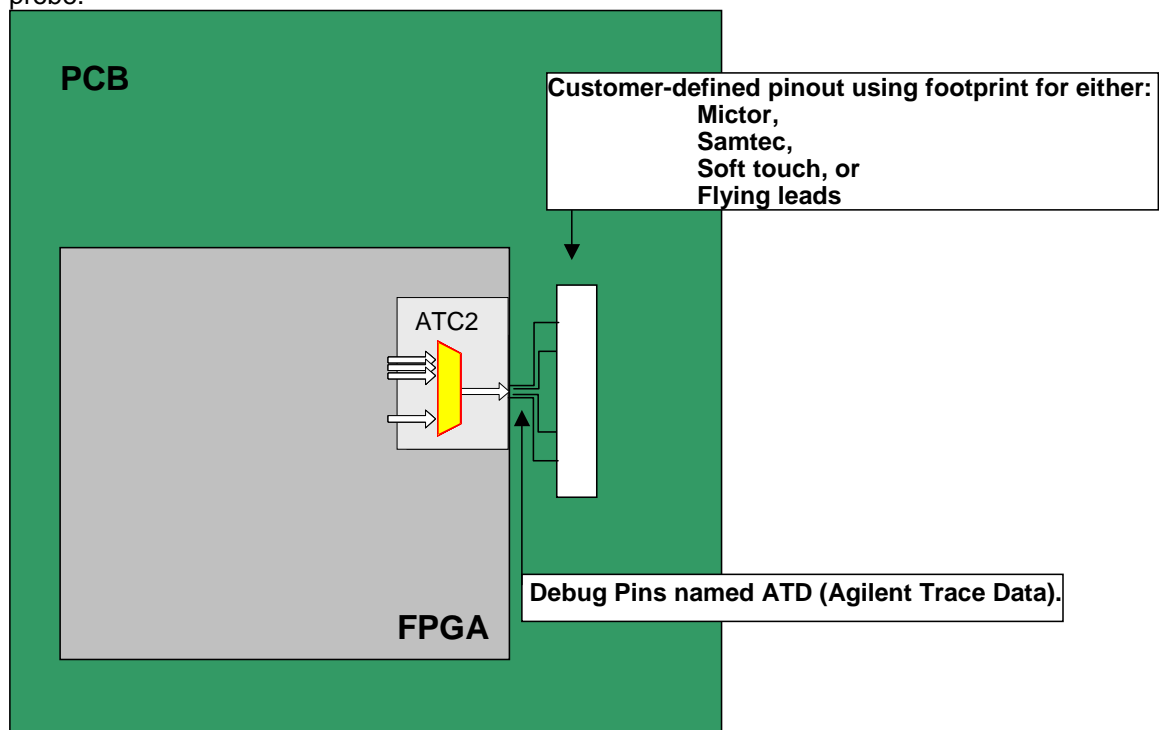
- Easier to create core and merge into design (less engineering resources)
- Automated pin mapping (faster, eliminate errors)
- Automatic signal naming synchronization (faster, eliminate errors)
- Easier to change core parameters (more flexible)
- Easier to control via JTAG (ease of use)
- Ability to download configuration bits via logic analyzer (flexibility)
- Core calibrated for more accurate state measurements (more accurate)

Q. What triggering resources are available with FPGA dynamic probe?

A. The full trigger resources of the Agilent logic analyzer being used are available.

Q. What special pinouts are required by FPGA dynamic probe?

A. No special pinouts are required. FPGA dynamic probe includes a graphical feature called pin mapping. This lets you visually tell the tool how FPGA physical pins that carry the MUX output (ATD (Agilent Trace Data)) are connected to the logic analyzer. If using a traditional probing connection such as a mictor or samtec connector, or a soft touch probe, the graphic lets you specify the location of each ATC2 output and which logic analysis cable is connected to this probe.



General Questions on Purchasing and Installing ChipScope Pro Tools

Q. What is ChipScope Pro?

A. ChipScope Pro is the on-chip verification and debug tool for Xilinx FPGAs including:

- ILA core and ChipScope Pro Analyzer (not used in FPGA dynamic probe application)
- Core Inserter
- Core Generator

Q. What Xilinx FPGA devices do ChipScope Pro tools support?

A. ChipScope Pro tools support; Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Spartan-II, Spartan-IIE, and Spartan-3.

Q. How do customers order ChipScope Pro tools?

A. ChipScope Pro can be ordered through the Xilinx sales channel (there will be an entry in the Xilinx sales book). Alternatively customers can purchase ChipScope Pro [on-line](#).

Q. How much do ChipScope Pro tools cost?

A. ChipScope Pro tools cost \$695.00.

Q. Is ChipScope Pro tools sold as a time based license agreement?

A. Yes, ChipScope Pro is sold under the standard Xilinx one-year time based license agreement.

Q. What do I get when I purchase ChipScope Pro tools?

A. Customers will receive a letter with a ChipScope Pro product ID and instructions on how to access ChipScope Pro tools including: The ChipScope Pro Core Generator and Core Inserter, ChipScope Pro Analyzer, and ChipScope Pro soft cores; ILA, IBA, VIO, as well as the Agilent ATC2 core.

Q. How can a customer get the latest version of ChipScope Pro tools?

A. Customers can get the latest version of ChipScope Pro cores on-line at http://www.xilinx.com/ise/verification/cs_pro_get.htm.

Q. Is there an evaluation version of ChipScope Pro tools?

A. Yes, there is a full-featured 90-day evaluation version of ChipScope Pro tools that is available for download at http://www.xilinx.com/ise/verification/cs_pro_get.htm.

Q. How do customers obtain ChipScope Pro registration IDs?

A. When a customer purchases ChipScope Pro tools they receive a product ID, the customer will need to register this product ID to obtain a valid registration ID.

Questions on Using ChipScope Pro Tools

Q. What is the ChipScope Pro Core Generator?

A. Similar to the ISE CoreGen tool, the ChipScope Pro Core Generator allows customers to define parameter for ChipScope Pro cores, and generates synthesizable HDL that can be combined within a users design.

Q. What is the ChipScope Pro Core Inserter?

A. The ChipScope Pro Core Inserter allows users to add ChipScope Pro cores after the design has been synthesized by merging design netlists.

Q. What is the ChipScope Pro Analyzer?

A. The ChipScope Pro Analyzer is the main interface that allows users to configure Xilinx FPGAs, find ChipScope Pro cores within a design, and setup and define trigger conditions. The

ChipScope Pro Analyzer is similar to a logic analyzer in that it allows user to view and interact with data captured for the purposes of debug and verification.

Q. What is ChipScope Pro ILA?

A. ChipScope Pro ILA (Integrated Logic Analyzer) allows users to view signals and nodes within the Virtex-II Pro FPGA design. Multiple trigger inputs, trigger sequencing and optional time stamping allow users to better utilize the available blockRAM within the device under test. The ILA cores communicate via JTAG with the ChipScope Pro Analyzer.

Q. What is ChipScope Pro IBA?

A. ChipScope Pro IBA (Integrated Bus Analyzer) is the industries first integrated bus analysis core. ChipScope Pro IBA is a CoreConnect specific bus analyzer that allows users to capture and display transaction and signal activity between the PPC405 processor and IP components in the FPGA fabric.

Q. Do the ChipScope Pro IBA cores support the IBM CoreConnect Interface?

A. Yes, the ChipScope Pro CoreConnect IBA has been predefined specifically for the IBM CoreConnect Interface. Two variations of the IBA core support the On-chip Peripheral Bus (OPB) and the Processor Local Bus (PLB). This core will allow users to view transactions and protocol violations specific to the CoreConnect interface.

Q. What is ChipScope Pro VIO?

A. ChipScope Pro VIO (Virtual Input Output) core allows users to define virtual inputs and outputs that are controlled via the ChipScope Pro Analyzer interface.

Questions on Xilinx and Agilent On-chip Debug Solutions

Q. What is the Agilent Xilinx relationship?

A. Teams within Agilent and Xilinx have worked closely together over the past several years to provide solutions for on-chip debug of Xilinx FPGAs. These solutions have become part of the Xilinx ChipScope Pro solution.

Q. What is the status of the Xilinx/ Agilent Trace Port Analyzer solution?

A. The Agilent FPGA Trace Port Analyzer solution, introduced just over a year ago, will be discontinued on October 30, 2004. The capabilities available in the Agilent FPGA Trace Port Analyzer solution have been improved and are now available in a new technology known as FPGA Dynamic Probing from Agilent.

Q. Will the Agilent Trace Port Analyzer continue to be supported?

A. Yes, ChipScope Pro tools and Agilent will continue to support the Agilent Trace Port Analyzer solution, although customers will no longer be able to purchase this solution.

Q. What is Agilent FPGA Dynamic Probing?

A. Agilent FPGA Dynamic Probing enables users to configure Xilinx FPGAs, find and set up ChipScope Pro ATC2 cores, and capture and display data directly on the new series of Agilent Logic Analyzer mainframes.

Q. What logic Agilent Logic Analyzers does this work with?

A. This new technology works with all Agilent logic analyzers that run Windows XP. This includes the 16900 Series, and the 1680/90 Series.

Q. How much does the Agilent FPGA Dynamic Probing Solution cost?

A. The Agilent FPGA Dynamic Probing technology costs \$995 for a 1 year license.

Q. Does the Agilent FPGA Dynamic Probing solution require Xilinx ChipScope Pro tools?

A. Yes. The solution requires the use of the ATC2 core, this core is delivered and inserted using ChipScope Pro Core Generator or ChipScope Pro core Inserter.

Q. Can I still use ChipScope Pro to configure the FPGA?

A. Yes, ChipScope Pro tools can be used to configure Virtex-II and Virtex-II Pro devices.