# Agilent Digital Test Console PCI Express® 3.0

Data Sheet

Version 1.1

The only comprehensive and integrated x1 through x16 protocol analyzer and LTSSM exerciser solution for PCI Express® 1.0, 2.0, and 3.0 with superior probing using ESP technology

Agilent Technologies

# Overview

Agilent Technologies' new Digital Test Console now includes support for all PCI Express 3.0 (PCIe 3.0) speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3) with x1 through x16 support on both the protocol analyzer and the link training sequencer state machine (LTSSM) exerciser.

With a protocol analyzer, LTSSM exerciser, as well as mid-bus and slot interposer probes using the equalizing snoop probe (ESP) technology, Agilent's Digital Test Console is the industry's most complete test solution for PCIe 3.0.

The Digital Test Console helps test engineers and validation labs address the challenges of transitioning to PCIe 3.0, such as the high speeds, the requirement to maintain the same electrical channel lengths and characteristics, and the completely new encoding scheme and advanced protocol features. The solutions-based approach of the Digital Test Console simplifies the PCIe 2.0 to PCIe 3.0 transition by providing stimulus to thoroughly test the link, and analysis and debug capabilities with accurate probing capabilities to help troubleshoot the systems under test.

## Digital Test Console – The Solution Approach

- Complete, modular, and scalable solution
- Two-in-one solution for stimulus and analysis

### Stimulus and test

- Support for Gen3 through Gen2, x1 through x16 link width
- Thorough testing of the link from x1 to x16, using automated LTSSM exerciser
- Industry's smallest form-factor, and scalable architecture

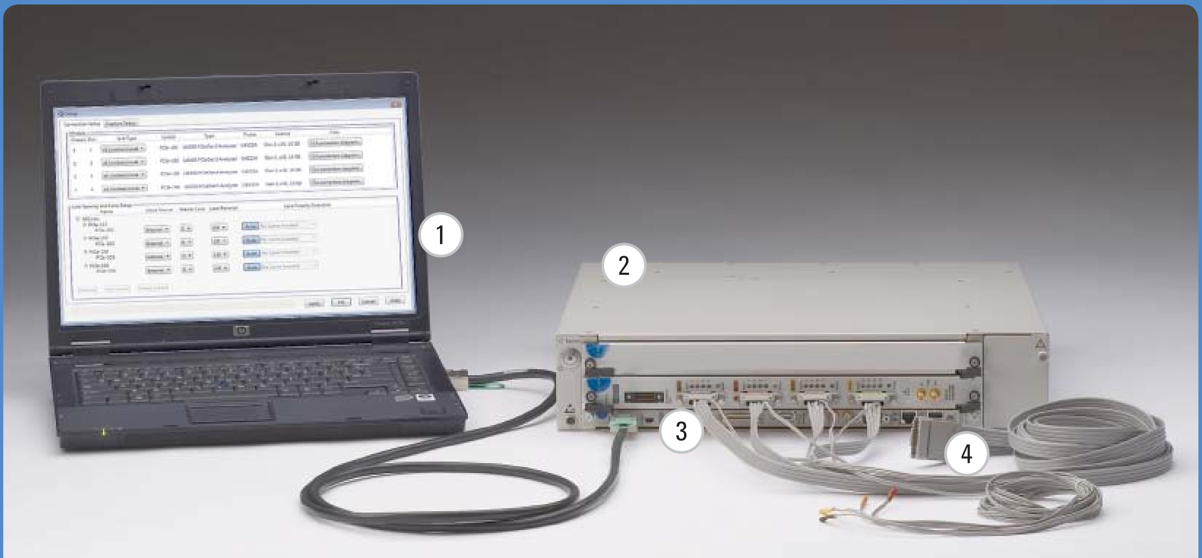
### Analysis and debug

- Support for Gen1 through Gen3, x1 through x16 link width
- Raw capture mode with lane triggering to ensure data visibility even in the face of significant PHY layer issues
- 4 GB of capture buffer per module (up to 8 GB of capture for x16 analyzer)

### Industry leading probes

- Both mid-bus and slot interposer probe, x1 to x16 support
- Non-intrusive probing that leverages ESP technology
- Automatically tuned equalization ASIC to ensure accurate data capture in all systems

# System Architecture Overview



1. PC controller to manage and interact with the system. Multiple connection options for the controller: USB 2.0 directly from the PC to the chassis or PCIe Gen1 x4 cable from the PC to the chassis
2. U4002A: Digital Test Console 2-slot chassis
3. U4301A protocol analyzer module controlled via PCIe x4 cable link from the PC controller
4. U4322A soft touch mid-bus probe 3.0

## Platform features and benefits

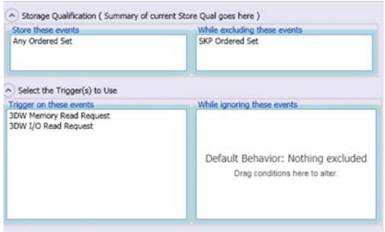
| Feature | Benefits |
|---|---|
| Modular and scalable system architecture | • Supports small and large-scale test environments<br>• Protects your financial investment for future needs, allowing you to split a x16 system into two x8 debug stations<br>• Multiple chassis can be connected together to form a large-scale analysis system<br>• Multiple exercisers can be controlled through a single PC via a USB hub for correlated large scale system testing |
| Cross bus analysis using the multi-frame capabilities | • Multiple protocols can be monitored at the same time (e.g. PCI Express to double date rate memory (DDR))<br>• Correlated views between the logic analyzer view and the protocol analyzer view<br>• Ping pong triggering between the logic analyzer and the PCI Express protocol analyzer |
| Test customization and automation with TCL | • Both the exerciser and protocol analyzer can be fully automated<br>• Automate repetitive tests for regression testing |

# Product Features and Benefits Overview

## Analyzer

### Effective presentation of protocol interactions from physical layer to transaction layer

- Raw capture mode with data presented in lane viewer to help debug low level PHY issues
- Lane view with packet highlighting to show the actual data on the bus
- Industry standard spreadsheet format protocol viewer with:
  - Highlighting by packet type or direction
  - Easy flow columns to better understand the stimulus and response nature of the protocols
  - Context sensitive columns to show only the relevant information, minimizing the need to scroll horizontally
- Transaction viewer groups all related packets and metrics for each transaction
- Flexible GUI configuration to meet debug needs, with pre-defined GUI layouts for Link Training debug, Config accesses and general I/O



Storage Qualification ( Summary of current Store Qual goes here )

Store these events: Any Ordered Set

While excluding these events: SKP Ordered Set

Select the Trigger(s) to Use

Trigger on these events: 3DW Memory Read Request, 3DW I/O Read Request

While ignoring these events: Default Behavior: Nothing excluded. Drag conditions here to alter.

### Simple and powerful state-based triggering

- New simple trigger mode makes it easy to setup single event triggers
- Powerful state-based triggering including:
  - Four states supported in trigger sequencer
  - Triggering on errors such as illegal sync characters, loss of framing, illegal block, etc.
  - Triggering on patterns (ordered set patterns or packet types)
  - Internal counters and timers
  - Triggering on an ordered set on a specific lane
- External trigger in/out

### Powerful hardware features ensure capture of important transition events

- Dual phase lock loops (PLLs) per direction ensuring that the analyzer will lock on speed change events quickly and not miss any critical data
- Large capture buffer, for long recording sessions up to 8 GB (x16 configuration)
- PCIe Gen1 x4 link to the host PC, provides up to 10 Gb/s of data download; the fastest in the industry
- LEDs to show lane status and speed for fast understanding of current link status

# Product Features and Benefits Overview

## Probing and LTSSM Exerciser

### Accurate data recovery with consistent representation of the signal

- Uses ESP technology to ensure accurate data recovery in all Gen3 platforms and all x1 through x16 link widths
- Slot interposer probe consistently represents signal, ensuring design problems can be reproduced
- Mechanical stabilization for the device under test's (DUT's) end point and to ensure firm PCIe slot connections

### Accurate data recovery with flexible use model

- Uses ESP technology to ensure accurate data recovery in all Gen3 platforms and all x1 through x16 link widths
- Micro spring-pin technology provides reliable contact to signal pads
- Spring-loaded cover on the probe tip ensures sensitive pins are protected when not in use
- To reduce cost of test, ensures that only one type of probe is required for:
  - x16 straight
  - x16 swizzled
  - x8 bi-directional
  - Bi-furcation support (one link as two logical links)
- Independent reference clock per four lanes for maximum layout flexibility

### Thorough link testing

- Pre-defined LTSSM tests to help validate the complex and hard to test state transitions of the DUT's LTSSM
  - Detailed reporting to clearly define source of problem for faster debug
  - Easy-to-use test architecture; single click to run all tests
- Automates testing with built-in API interface (backwards compatible with PCI Express Gen2 exerciser API)
- Flexible software architecture; start with LTSSM testing today and expand to other applications such as an exerciser through a simple software upgrade
- Self-contained, portable, and self-powered PCIe Gen3 backplane for end point testing eliminates the requirement for a motherboard
  - Two pairs of x16 slot connectors
  - Provides additional power for end point devices

# Typical Configurations

| LTSSM Exerciser sample configuration | |
|---|---|
| **Test cards** | |
| U4305A-E16 | Exerciser board x16 for PCIe 8 GT/s |
| **Software** | |
| U4305A-LTSSM | LTSSM software license |
| **Accessories** | |
| N5316A | Test backplane 3.0 for PCIe 8 GT/s |

| Analyzer sample configuration | |
|---|---|
| **Chassis** | |
| U4002A | Digital Test Console two-slot chassis |
| U4002A-EXP | PCI Express cable to express card adapter for laptop connections |
| U4002A-2MC | PCIe cable (2.0 m) |
| **Test blades** | |
| U4301A | Analyzer blade hardware |
| U4301A-A08 | Analyzer linkwidth x8 |
| **Software** | |
| U4301A-v07 | Analyzer software license for PCIe 8 GT/s, Spec version 0.7 |
| U4301U-v10 | Analyzer software license upgrade for PCIe 8 GT/s, specification version 0.7 to 1.0 |
| **Probes** | |
| U4321A-A08 | Slot interposer 3.0 for PCIe 8 GT/s x8 |

# Related Agilent Literature

| Publication title | Pub number |
|---|---|
| *Agilent E2960B Series for PCI EXPRESS® 2.0 Data Sheet* | 5989-5660EN |
| *Agilent Technologies PCI Express® Design and Test – From Electrical to Protocol Brochure* | 5989-5594EN |

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