Agilent Logic Analyzer Cheat Sheet

Considerations When Configuring a Logic Analyzer (App note: http://cp.literature.agilent.com/litweb/pdf/5989-5138EN.pdf)

Connect What is the best way to probe the target signals, given their unique characteristics?	Acquire What is the right combination of acquisition capabilities required to address the measurement needs?	View and Analyze What is the most efficient way to analyze the captured data?
Probing: Ensure the probe connection to the DUT supports the characteristics of the signals being probed (probe bandwidth to match the signal speeds, impact of probe loading on the target device and measurement accuracy, signal type – single-ended or differential, minimum signal amplitude, etc.). Also – will the customer be designing in probing connections or connecting to individual signals after the design is complete? Connection to the DUT can also be by done via analysis probe, interposer, etc. **NOTE:** Probes are ordered separately. Specify probes when ordering to ensure the correct connection between the logic analyzer and device under test. Recommend ordering enough probes for the number of channels selected unless other probing options are available (analysis probe, interposer, etc.)	**State & Timing Speeds:** Select a logic analyzer with a max state speed at least as high as the bus data rate and max timing rate at least 4 to 10 times the bus data rate. **Channels:** Each channel represents one signal. Select a system with enough channels for the application. Recommend getting additional channels to look at other buses or for future needs. **NOTE**: Channel count is not upgradeable in portable configurations – order enough channels for future needs. **Memory Depth:** Due to the complexity of today's digital buses, the logic analyzer must have enough acquisition memory to capture as much system activity as possible. For tight budgets, purchase the amount of memory needed for now and upgrade as needs evolve. **NOTE**: if all channels are used, memory depth is halved in state mode.	**Application and Analysis Tools:** Agilent and our partners provide an extensive range of FPGA, processor, bus and analysis tools. Analysis tools help rapidly consolidate data into displays that provide insight into the system's behavior – saving the customer time. **NOTE**: Use the logic analyzer configuration spreadsheet to determine if application support is available for the specific application, as well as logic analyzer compatibility. Agilent and its 3rd parties are available to develop custom solutions also.

Logic Analyzer Portfolio http://www.agilent.com/find/logic

Product Family	16800 Series Portable Logic Analyzers	16900 Series Modular Logic Analysis Systems	AXIe-based Logic Analyzers
Websites and Data Sheets	www.agielnt.com/find/16800 http://cp.literature.agilent.com/litweb/pdf/5989-5063EN.pdf	www.agilent.com/find/16900 Mainframes: http://cp.literture.agilent.com/litweb/pdf/5989-0421EN Measurement Modules: http://cp.literture.agilent.com/litweb/pdf/5989-0422EN	www.agilent.com/find/U4154A Chassis: http://cp.literature.agilent.com/litweb/pdf/5990-6584EN.pdf U4154A: http://cp.literature.agilent.com/litweb/pdf/5990-7513EN.pdf
	Benefits of a 16800 Series portable logic analyzer Delivers an exclusive combination of logic analysis, pattern generation, application software, and innovative probing – all at a price to fit limited budgets. • Built in 48-ch pattern generator available on select models • 8 models support a wide range of applications (34, 68, 102, 136, or 204 channels) • Affordable fixed configurations	**Benefits of a 16900 Series modular system** • Flexibility to configure the system for specific acquisition and stimulus needs • Long-term investment protection – upgrade or re-configure as needs evolve • Maximize measurement capability: highest channel counts, highest state (2 GHz) and timing (8 GHz) speeds, deepest memory depth (up to 256 M), single ended and differential signal support	**Benefits of an AXIe-based logic analyzer** • AXIe-based modular platform supported multiple buses including logic analyzer, HDMI & MHL Protocol Analyzer and Generator Module, PCIE Gen 3 analyzer module, and etc. • AXIe chassis provide a high-performance platform to compliment PXI-based systems • Long-term investment protection – upgrade or re-configure as needs evolve
	Features • 15″ display, Touch screen optional (option 103) • Logic analyzer cables egress from the side • External removable hard drive (option 109) • See details below 	**16901A feature differences relative to 16902B modular mainframe** • 2-slots for measurement modules • Logic analyzer cables egress from the side • External removable hard drive (option 109) • Same footprint as 16800 series portable logic analyzer  **16902B feature differences relative to 16901A modular mainframe** • 6-slots for measurement modules • Logic analyzer cables egress from the rear • Built-in removable hard drive (standard) • Largest footprint 	**U4154A features** • State capture up to 4 Gb/s on 68 channels, 2.5 Gb/s on 136 channels per module • Trigger Sequence Rate, 2.5GHz • 12.5 GHz Timing Zoom with 256 K sample memory • Reliable data capture on eye openings as small as 100 ps by 100 mV 

	16800 Series Portable Logic Analyzers					16900 Series Logic Analyzer Modules			U4154A Logic Analyzer Module	
Model	**16801A 16821A**	**16802A 16822A**	**16803A 16823A**	**16804A**	**16806A**	**16910A/16911A** (Entry Class)	**16950B/16951B** (Mid Range)	**16962A** (High End)	**U4154A-01G** (High End)	**U4154A-02G** (Ultra High End)
Logic Analyzer Channels	34	68	102	136	204	102 / 68	68	68	136	
Pattern Generator Channels	48	48	48	N/A	N/A	Requires 16720A module	Requires 16720A module	Requires 16720A module	N/A	
Max channels on single time base	34	68	102	136	204	340 / 510	340	340	272	
Number of analyzers (time bases)	1	2				2	2	1	1	
Maximum state clock rate	250 MHz	250 MHz (standard) 450 MHz with opt 500				250 MHz (standard) 450 MHz with opt 500	667 MHz	2 GHz	1.4 GHz	2.5 GHz
Max state data rate	250 Mb/s	250 Mb/s (standard) 500 Mb/s with opt 500				250 Mb/s (standard) 500 Mb/s with opt 500	667 Mb/s (DDR) 1066 Mb/s (Dual Sample)	2 Gb/s (DDR) 2.5 Gb/s (Dual Sample)	1.4 Gb/s (136 channels) 2.8 Gb/s (68 channels)	2.5 Gb/s (136 channels) 4 Gb/s (68 channels)
Minimum state clock rate	Low Hz					Low Hz	Low Hz	40 MHz	12.5 MHz (single edge), 6.25 MHz (both edges)	
High Speed Timing Zoom	4 GHz (250 ps) with 64k depth					4 GHz (250 ps) with 64k depth	4 GHz (250 ps) with 64k depth	N/A	12.5 GHz (80ps) with 256K depth	
Max timing sample rate (qtr/half/full ch)	500 MHz half ch / 1 GHz full ch					500 MHz half ch / 1 GHz full ch	600 MHz half ch / 1.2 GHz full ch	8 GHz quarter ch / 4 GHz half ch / 2 GHz full ch	5 GHz half ch / 2.5 GHz full ch	
Transitional timing	500 MHz (full ch)					500 MHz (full ch)	600 MHz (full ch)	8 GHz quarter ch / 4 GHz half ch / 2 GHz full ch	5 GHz half ch / 2.5 GHz full ch	
Memory depth	1 M standard 4 M, 16 M, 32 M optional					256 K standard 1 M, 4 M, 16 M, 32 M optional	16950B: 1 M stnd, 4 M, 16 M, 32 M, 64 M opt & 16951B: 256 M stnd	4 M standard 16 M, 32 M, 64 M, 100 M optional	2 M standard 4 M, 8 M, 16 M, 32 M, 64 M, 128 M, 200 M optional	
Supported signal types	Single-ended					Single-ended	Single-ended and Differential	Single-ended and Differential	Single-ended and Differential	
Probe compatibility	40-pin cable connector					40-pin cable connector	90-pin cable connector	90-pin cable connector	90-pin cable connector	

Pattern Generator (Standard with 16821A, 16822A, and 16823A portable logic analyzers; 16720A module for 16900 Series systems)			More differentiators between -01G and -02G		
Pattern Generator Configuration	**Half Channel**	**Full Channel**	**Max trigger sequencer rate**	1.4 GHz	2.5 GHz
Maximum Clock	300 MHz	180 MHz	**Minimum eye size**	160 ps x 160 mV	100 ps x 100 mV
Data Channels	24	48	**Sample position adjustment resolution**	20 ps	5 ps
Memory depth in vectors	16 M	8 M	**Threshold resolution**	20 mV	2 mV
Logic levels supported	5 V TTL, 3-state TTL, 3-state TTL/CMOS, 3-state 1.8 V, 3-state 2.5 V, 3-state 3.3 V, ECL, 5 V PECL, 3.3 V LVPECL, LVDS		**Upgrade availability**	U4154A-02G (Software license upgrade to 02G without any penalty cost)	
Data/Clock Pod Quantities	Must order at least one clock pod per pattern generator and at least one data pod for every 8 output channels.				

Logic Analyzer Probing and Accessory Solutions (http://www.agilent.com/find/logic_analyzer_probes)

	General Purpose Probes				DDR2/3 BGA Probes for Logic Analyzers and Oscilloscopes	
	Flying Lead	**Mictor**	**Samtec**	**Soft Touch Connectorless**	**DDR2/3 BGA Probes**	**ZIF Probes**
Key: SE = Single Ended DF or diff = Differential Classic = Original (larger) soft touch footprint Pro Series = narrower soft touch footprint, industry standard – also compatible with Tek logic analyzers	Measure individual signals physically far apart or where a probe connector has not been designed in. A wide variety of accessories provide the flexibility to connect to IC pins, traces, vias, and any signal that resides on the surface of the board.	This reliable and cost-effective connector solution supports data rates up to 600 Mb/s. The probe requires a 38-pin connector designed into the target system.	This high-performance connector solution supports data rates up to 1.5 Gb/s. The probe requires a 100-pin Samtec connector designed into the target system.	Reduce cost and shorten the design cycle by eliminating probing connectors. The proprietary micro spring-pin technology provides reliable contact to signal pads even when probing uneven or contaminated circuit board surfaces.	The W2630A and W3630A Series of BGA probes enable viewing of data traffic on industry standard DDR2/3 DIMMs with a 16900 Series logic analyzer or 9000/90000 Series oscilloscope. The probes provide a non-intrusive, electrical and mechanical connection to all signals of the DDR2/3 DRAM.	ZIF probes provide a connection between 90-pin logic analyzer cables and the wings of a compatible BGA probe.
40-pin probes (Compatible with 16800 Series portables and 16910A, 16911A modules)	E5383A: 17-ch (SE)	E5346A: 34-ch (SE)	E5385A: 34-ch (SE)	E5404A: 34-ch (SE, Pro Series) E5394A: 34-ch (SE, Classic) E5396A: 17-ch (SE, Half-size Classic)	N/A	N/A
90-pin probes (Compatible with U4154A, 16962A, 16950B, 16951B, and 16760A modules)	E5382A: 17-ch (SE) E5381A: 17-ch (DF)	E5380A: 34-ch (SE)	E5378A: 34-ch (SE) E5379A: 17-ch (DF)	E5406A: 34-ch (SE, Pro Series) E5402A: 34-ch (SE, low profile, Pro Series) E5405A: 17-ch (DF, Pro Series) E5390A: 34-ch (SE, Classic) E5398A: 17-ch (SE, half-size Classic) E5387A: 17-ch (DF, Classic)	**DDR2 BGA Probes** W2631A: 42 signals + 3 diff clocks* (UDQS, LDQS, CK) W2632A: 16 signals + 1 diff clock (LDQS) W2633A: 32 signals + 2 diff clocks (LDQS, CK) W2634A: 8 signals + 1 diff clock (LDQS) *UDQS/UDQS# are available on the oscilloscope probing pads on the rigid flex but do not go to the logic analyzer cable. **DDR3 BGA Probes** W3631A: DDR3 x16 command and data W3633A: DDR3 x4/x8 command and data (options specify quantity: 001 = qty 1, 002 = qty 2, 004 = qty 4)	**ZIF Probe: Access (for DDR 2 BGA probes)** E5384A: All x8 or x16 DRAM data buses E5326A: x16 DRAM data buses E5327A: two x8 DRAM data buses **ZIF Probes: Access (for DDR 3 BGA probes)** E5845A: for X16 DRAM E5847A: for x8 DRAM

Logic Analyzer Application Solutions (http://www.agilent.com/find/logic-sw-apps)

FPGA – This virtual probing method for Xilinx and Altera FPGAs provides access to as many as 256 internal FPGA signals for each FPGA pin dedicated to debug. Internal probe points can be moved is seconds without design changes. Automated pin mapping shortens measurement setup time and eliminates unintentional mistakes. http://www.agilent.com/find/fpga	B4655A FPGA Dynamic Probe for Xilinx B4656A FPGA Dynamic Probe for Altera E9524A Xilinx MicroBlaze trace core and inverse assembler
Memory (DDR) – the variety of BGA, interposer and mid-bus probes used in conjunction with the DDR 2/3 bus decoder and protocol compliance tool provides memory bus triggering, debug and compliance measurements. http://www.agilent.com/find/memory	B4621B DDR2/3/4 Bus Decoder B4622B DDR 2/3 Compliance and Analysis Tool (B4622A Protocol Compliance requires B4621A) B4623B LPDDR/2/3 Bus Decoder
ARM Cortex ETM and PTM Decoders – The ARM Cortex ETM/PTM Decoder, used with an Agilent Technologies logic analyzer, allows you to view instructions and messages that are executing in your target system.	E9528A ARM Cortex ETM Decoder E9529A ARM Cortex PTM Decoder
Analysis Tools – analysis tools help identify what is happening and why by rapidly consolidating data into displays that provide insight into the system's behavior. http://www.agilent.com/find/logic-sw-apps	B4601C Serial to parallel analysis tool B4602A Signal Extractor tool B4606A Advanced Customization Environment (Developer) B4607A Advanced Customization Environment (Runtime) B4610A Data Import Tool B4630A MATLAB Connectivity Tool
Digital VSA – provides the digital serial acquisition and stimulus capabilities required to independently debug and test new digital buses in RF designs. http://www.agilent.com/find/dvsa	89601A-200, 89601A-300
Low speed serial buses – analysis probes convert the low speed serial data into a parallel format enabling triggering and deep traces that cover a long period of system activity	I2C, CAN, SPI, RS-232 analysis probes with inverse assemblers are available from Advanced Logical Design, http://www.ald.com/
Microprocessors and Microcontrollers – Monitor processor execution relative to the rest of the system. http://www.agilent.com/find/pnbs	Refer to logic analyzer configuration tool for list of supported devices

Related DDS Application Solutions

http://www.agilent.com/find/pcie	http://www.agilent.com/find/mipi	http://www.agilent.com/find/hdmi http://www.agilent.com/find/MHL
PCI Express	**Mobile Computing (DigRF, D-PHY, M-PHY)**	**HDMI / MHL**
Agilent´s U4300 Digital Test Console PCI Express protocol test solution supports all speeds of PCIe, 2.5 GT/s (Gen1), 5.0 GT/s (Gen2) through PCIe 8GT/s (Gen3). The Digital Test Console is the industry´s most complete test solution for PCIe 3.0, with a PCIe analyzer, PCIe LTSSM exerciser and both mid-bus as well as slot interposer probes utilizing the ESP (Equalizing Snoop Probe) technology.	The Mobile Industry Processor Interface (MIPI) Alliance has defined standard interfaces for mobile terminals. As a contributor member of the MIPI Alliance and a world leader in test and measurement, Agilent is at the forefront in providing you with digital and RF test solutions for the MIPI test interfaces.	The Agilent U4998A protocol / audio / video analyzer and generator module enables you to test your devices to ensure they are compliant to the HDMI 1.4b as well as MHL (Mobile High-Definition Link) compliance test specification (CTS).

Additional Logic and Protocol Analyzer Resources

Field portal for Logic analyzer information (sales tools, competition, etc.)	http://fieldcom.cos.agilent.com/portal/Coll.php?cId=-536902443
Field portal for Protocol analyzer information (sales tools, competition, etc.)	http://fieldcom.cos.agilent.com/portal/Coll.php?cId=-536902450
Keep up-to-date on the latest **promotional offers** for logic analyzers	http://www.agilent.com/find/promotion
Copy logic analyzer **demo videos** to your PC or direct customers to the site for individual viewing	http://www.agilent.com/find/logicdemos
Download the latest **logic analyzer software updates**	http://www.agilent.com/find/la-sw-download