Dakar
F5 Carrier Board
Technical Reference

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Preface

Spectrum Signal Processing offers a complete line of DSP hardware, software and I/O products for the DSP Systems market based on the latest DSP microprocessors, bus interface standards, I/O standards and software development environments. By delivering quality products, and DSP expertise tailored to specific application requirements, Spectrum can consistently exceed the expectations of our customers. We pride ourselves in providing unrivaled pre and post sales support from our team of application engineers. Spectrum has excellent relationships with third party vendors which allows us to provide our customers with a more diverse and top quality product offering.

Spectrum achieved ISO 9001 quality certification in 1994.

As Spectrum's hardware products are static sensitive, please take precautions when handling and make sure they are protected against static discharge.

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1 Introduction

1.1. Purpose of This Manual

This manual describes the features, architecture, and specifications of the F5 Carrier Board. It will help you understand how the function libraries described in the *F5 Carrier Board User Guide* operate within the board. You can also use this information to program the board at a driver level, extend the standard hardware functionality, or obtain more information to do custom configurations.

The *F5 Carrier Board User Guide* also shows you how to install and configure the board, as well as loading and running some of the sample code provided with the board.

1.2. Reference Documents

In addition to the F5 Carrier Board Technical Reference, Programming Guide, and Installation Guide, you will also find the following documentation helpful.

- *Dakar F5 Carrier Board User Guide* from Spectrum
- *TMS320C4x User's Guide* available from Texas Instruments
- *PCI Local Bus Specification*, Revision 2.1, PCI Special Interest Group, June 1995.
- *PLX PCI 9060 Data Sheet*, PLX Technology 1996.
- *PLX PCI 9080 Data Sheet*, PLX Technology 1997.
- *TMS320C44 TIM-40 Module Specification*, Version 1.01
- *Addendum to the TIM-40 TMS320C4x Module Specification Version 1.01*.
- *DSP~LINK3 Specification* Revision 1 from Spectrum (available from Spectrum's internet website at http://www.spectrumsignal.com)

1.3. Definition of Key Terms

'C4x	TMS320C40 or TMS320C44 Texas Instruments Digital Signal Processor
COMM Port	8-Bit parallel communication port on TMS320C40 and TMS320C44 DSPs.
PEROM	Programmable Erasable Read-Only Memory. Can be erased and reprogrammed in-circuit.
JTAG	Joint Test Action Group. Serial boundary-scan interface used to control test and on-chip emulation functions of DSPs.

XDS510	A JTAG interface for controlling the on-chip emulation functions of the TMS320C44.
PCI Master	An intelligent controller that is granted the PCI bus, and can execute read/write cycles to other devices on the PCI bus.
PCI Target	A “slave” device that PCI Masters can read/write to. Target and Master functionality can be combined on one PCI card.
Global Shared Bus	A shared bus that all four CPU Nodes can gain Master control to read/write DSP~LINK3 directly, and Far Global SRAM via the PLX PCI Local Bus. CPU Node A can also access the PLX PCI chip internal registers, and become PCI bus master via the Global Shared Bus and PLX PCI Local Bus.
PLX PCI Local Bus	A shared bus that all four ‘C4x Nodes, and a PCI Master can become Master of to access the Far Global SRAM. Node A can also access the PLX PCI internal registers and become PCI master via the PLX PCI Local Bus.
PLX PCI	PLX PCI9060 chipset or PLX PCI9080 chipset
PCI Host	The System Processor that is responsible to run PCI configuration cycles, host software, and receives interrupts from the PCI bus, typically a Pentium processor
Slice	A window of time allotted to one of the 'C4x processor nodes on the Global Shared Bus and possibly PLX PCI Local Bus. The length of time of a “slice” is determined by the Arbiter’s Latency Timer.

2 General Description

The F5 Carrier Board is a TIM-40 carrier board for use within computers equipped with a PCI bus. The full-length PCI board features one embedded Texas Instruments TMS320C44 Digital Signal Processor (DSP) and three TIM-40 module sites. TIM-40 modules define a family of DSP modules, based on TMS320C4x processors, designed for use in multiple DSP systems. Spectrum offers a range of single and dual processor TIM-40 modules that can be used with the F5 Carrier Board.

2.1. Features

- Flexible architecture consisting of up to seven TMS320C4x-based processor nodes
- One embedded TMS320C44 (’C44) processor with associated memory devices to form a virtual TIM-40 site for Node A.
- Three TIM-40 sites supporting single or double width TIM-40 modules further nodes.
- Up to 420 MFLOPS performance can be achieved using three dual-processor TIM-40 modules and the embedded ’C44 for a total of seven 50/60 MHz TMS320C4x processors
- Internal TMS320C4x communication port (COMM Port) connections between processor nodes.
- Ten external COMM Port connectors from the processor nodes
- 132 MBytes/s peak transfer rates from 32-bit PCI (Master/Slave) Bus.
- One on-board DSP~LINK3 module site
- One external DSP~LINK3 connector
- Non-intrusive multi-processor debugging in real-time using JTAG interface
- External connector on end-plate provides access to TIM-40 Application Specific Pins for nodes B, C, and D
- Up to 512k x 32-bit 1 wait-state SRAM shared between all processor nodes
- Up to 1M x 32-bit 0 wait-state SRAM for the Node A embedded processor
- Programmable Erasable ROM (PEROM) for the Node A embedded processor provides TIM-40 compliant code boot-strapping and board identification

2.1.1. Scaleable Modular Architecture

With its embedded ’C44 processor and its three module sites that are compatible with Texas Instruments’ TIM-40 specification, the F5 Carrier Board can be configured with one to seven 'C4x DSPs. This results in an architecture that can be scaled from 60 to 420

MFLOPS of processing power with varying memory capacity. A wide range of modules are available from spectrum providing the flexibility of different memory and analog I/O combinations for each TIM-40 site. Single or double width TIM-40 modules can be accommodated.

2.1.2. PCI Interface

Any PCI master on the PCI bus can access the following devices on the F5 Carrier Board via the PCI slave interface

- Test Bus Controller
- PLX PCI interface chip registers
- Far Global SRAM (for shared memory communication)
- Interrupt registers
- Bus Control registers

The Node A embedded ’C44 can master the PCI bus through the DMA channels of the PLX PCI interface chip. This allows the F5 Carrier Board to access the resources on the host computer through DMA transfers initiated by Node A.

Note: The Intel® 430FX chipset does not support DMA Bus Mastering. If your computer is equipped with this chipset, The F5 Carrier Board cannot initiate a DMA transfer to the PCI bus as a PCI master.

2.1.3. TMS320C4x Communication Port Interfaces

The TMS320C4x communication ports (COMM Ports) are used for inter-processor communication both internally and externally to the F5 Carrier Board. The COMM Ports provide bi-directional asynchronous communication between TMS320C4x processors. They are ideal for passing large data sets between processors without loading any shared resource, such as the Far Global SRAM. All four nodes are connected to each other internally and there are 10 external COMM Port connections shared amongst the nodes.

2.1.4. Shared Memory Resources

The shared bus architecture allows the on-board DSP, the TIM-40 module sites, and the PCI interface to access a shared bank of on-board SRAM. The F5 Carrier Board will have either 0.5 MB or 2 MB of zero wait-state 20 ns SRAM.

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2.1.5. Node A Memory Resources

Node A memory resources consist of a local bus PEROM, local bus SRAM and global bus SRAM in accordance to the TIM-40 specification. These resources are only accessible from the Node A 'C4x. The PEROM device is a 32K x 8-bit device used for TIM-40 IDROM and, optionally, for loading of boot-code. The local and global busses of Node A contain either both 0.5 MB or both 2 MB zero wait-state 15 ns SRAM banks.

2.1.6. DSP~LINK3 Interface

DSP~LINK3 modules can be used with the F5 Carrier Board via the DSP~LINK3 interface. The DSP~LINK3 module site allows Spectrum DSP~LINK3 modules to be installed right on the F5 Carrier Board while the DSP~LINK3 ribbon cable connector allows external DSP~LINK3 modules to be connected to the F5 Carrier Board. The interface is directly accessible to all processors nodes.

Spectrum offers a range of modules with DSP~LINK3 interfaces that can be used with the F5 Carrier Board, including IndustryPack® modules.

The DSP~LINK3 interface is an open standard for Spectrum's I/O interface. It defines a 32-bit wide, 40 Mbyte-per-second I/O interface with low interrupt latency. The full DSP~LINK3 specification is available from Spectrum upon request. DSP~LINK3 is electrically compatible the DSP~LINK2 specification and may be used with DSP~LINK2 with the appropriate mechanical adapter available from Spectrum.

2.1.7. JTAG Interface Debug Support

An on-board JTAG Test Bus Controller (TBC) is mapped to the PCI Local Bus to provide multiprocessor, C source, debug capability in conjunction with support software applications. JTAG-based debugging uses the 'C4x's dedicated debug port to minimize the intrusiveness of the debugger on your application.

2.2. Board Layout

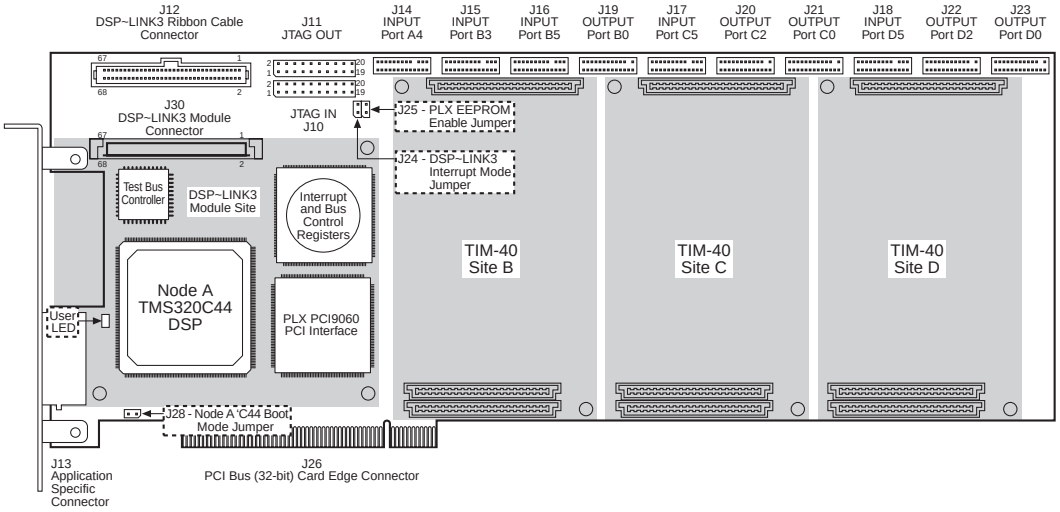

Figure 1 F5 Connector and Jumper Locations

Table 1 F5 Jumper Summary

Jumper	Description	Installed	Not Installed
J24	DSP~LINK3 Interrupt Mode	All DSP~LINK3 interrupts to Node A IIOF0	DSP~LINK3 interrupt IRQ0 to Node A IIOF0*
J25	PLX PCI EEPROM Enable	Enabled*	Disabled
J28	Node A 'C44 Boot Mode	Boot from PEROM*	Boot from COMM Port

*Default

2.3. Memory Configurations

The F5 Carrier Board is available in the memory configurations shown in the following table. Each SRAM bank consists of four 8-bit SRAM memory devices.

Table 2 Memory Device Sizes (in 32-bit words)

Total SRAM (Bytes)	Local SRAM Bank 1	Local SRAM Bank 0	Global SRAM Bank 1	Global SRAM Bank 0	Far Global SRAM
-	*15 ns*	*15 ns*	*15 ns*	*15 ns*	*20 ns*
1.5 Mbytes	empty	128K	empty	128K	128K
6 Mbytes	empty	512K	empty	512K	512K
10 Mbytes	512K	512K	512K	512K	512K

The locations of the memory devices on the back of the F5 Carrier Board are shown in the following figure..

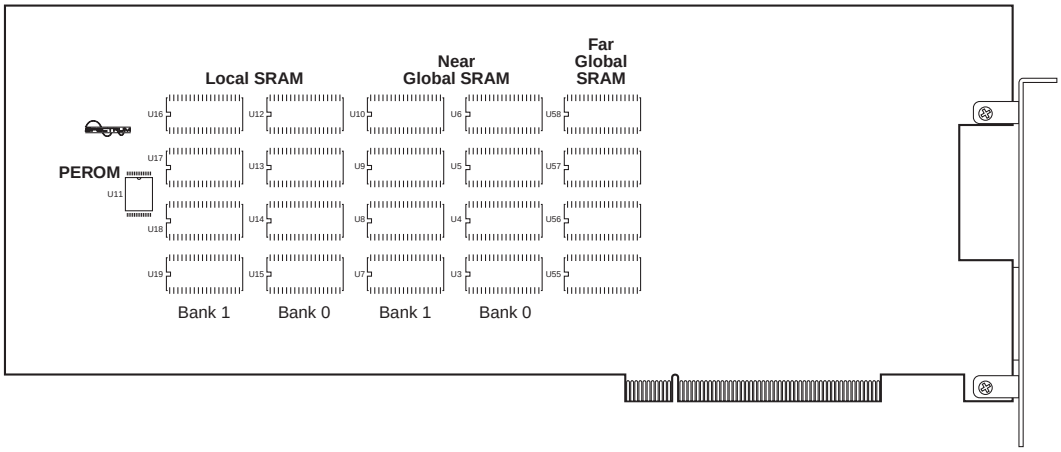

Figure 2 F5 Memory Device Locations

2.4. Bus Architecture

Several different communication buses are used on the F5 Carrier Board to connect the embedded ’C44 processor, TIM-40 sites, memory devices, and interface circuitry as shown in the following diagram.

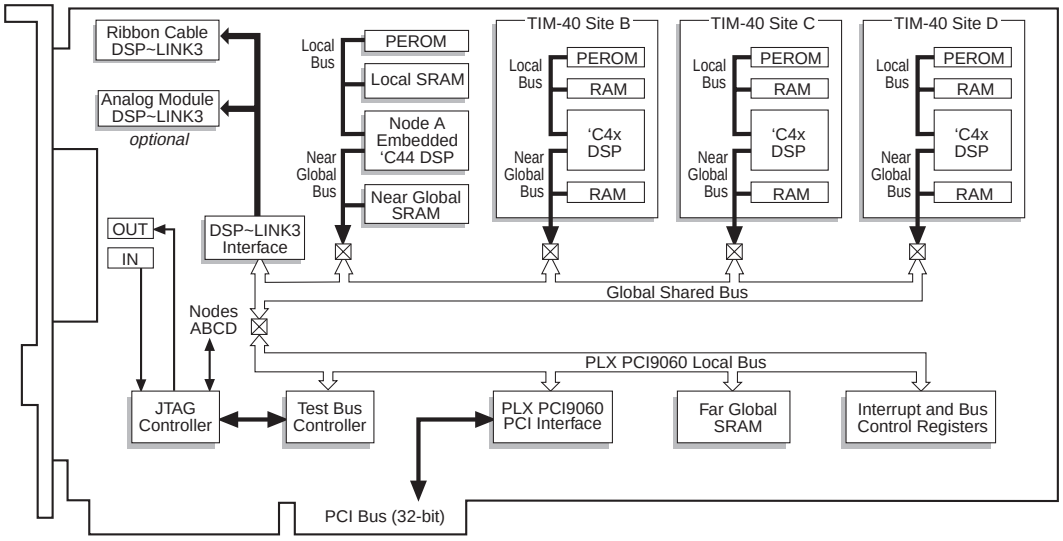

Figure 3 F5 Block Diagram

The internal busses of the F5 Carrier Board are described in the following passage.

Local Bus — The Local Bus address range is specific to a single ’C4x DSP, and is therefore not shared with other processors or nodes. It is a private memory bus of a particular’C4x.

Near Global Bus — The Near Global Bus refers to the Global Bus of each TIM-40 site and the embedded ’C4x node. The SRAM located on ’C44 Global Bus is zero wait state. The Near Global Bus SRAM of a node cannot be accessed by the DSPs of any other nodes.

Global Shared Bus

The Global Shared Bus interconnects the:

- Buffered Global Buses of each TIM-40 site via the Global Connectors
- Buffered Global Buses of the embedded ’C44 node A
- DSP~LINK3 Interface
- Interface between the PLX PCI Local Bus and the Global Shared Bus

32-bit buffers isolate the Global Shared Bus from the ’C4x node Global Buses. An analog quickswitch connects the data and address lines of the Interface between the PLX PCI Local Bus and the Global Shared Bus; the interface control lines are buffered.

PLX PCI Local Bus

The PLX PCI Local Bus of the PLX PCI chip is connected to the

- Global Shared Bus interface buffer
- Far Global SRAM
- Interrupt Controller
- Registers for the Interrupt Controller and Bus Arbitration
- JTAG Controller

2.5. ’C4x Communication Port Architecture

Routing of the ’C4x COMM ports to the 10 external COMM port connectors is shown in the following diagram. Arrows indicate the default port direction after the board is initialized.

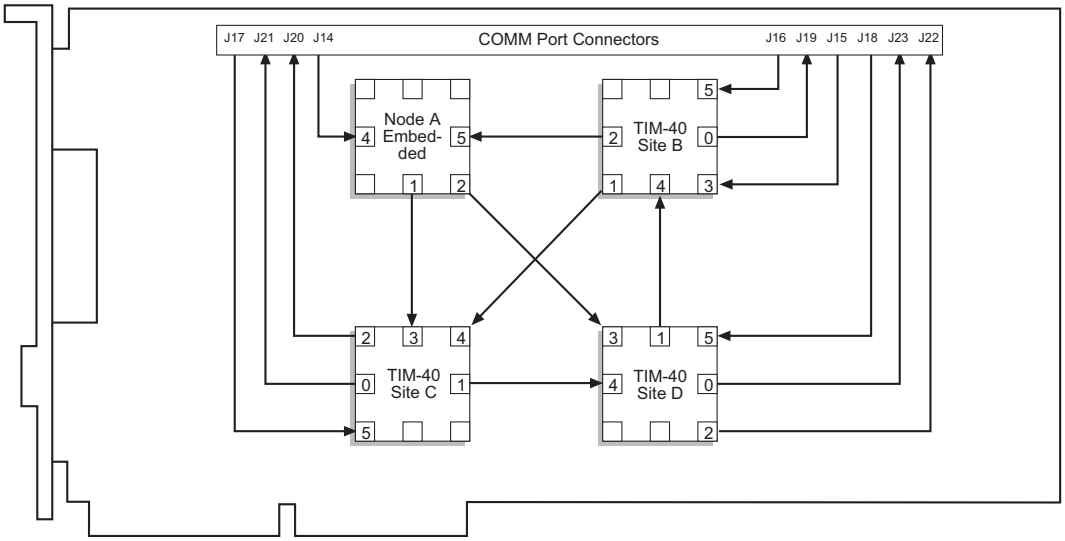

Figure 4 F5 COMM Port Architecture

2.6. Resetting the F5 Carrier Board

The F5 Carrier Board is reset upon system power up. Resets can also be performed from host software on the PCI bus and from JTAG. The following table shows which F5 Carrier Board hardware is initialized by each type of reset.

Table 3 Reset Summary

F5 Carrier Board Hardware Reset	Power Up	PCI Software	JTAG
All CPU Nodes	✓	✓	✓
DSP~LINK3 Slave Devices	✓	✓	
JTAG devices connected to the JTAG Out connector /GRESET pin (J11 pin 20)	✓	✓	✓
PCI bus Interface Logic	✓		
PCI Local Bus Logic	✓	✓	
Support Logic	✓	✓	✓

When the processor nodes are reset with any of the above methods, the ‘C4x processor IIOF lines are tristated as per the TIM-40 specification to allow the boot mode selection jumpers to be read by the C4X processor. To enable its IIOF signals a ‘C4x must then execute an IACK cycle.

2.6.1. Power Up Reset

The PCI bus RST# signal resets all F5 Carrier Board hardware when it is asserted. It is asserted upon system power up and typically when the operating system (such as Windows 95) is started.

The system must issue PCI bus configuration cycles after RST# to configure the F5 Carrier Board PCI bus interface. Usually the host BIOS or operating system (such as the Windows 95 Plug and Play component) will do this automatically.

The F5 Carrier Board remains in a reset state for a approximately 30 milliseconds after power on for on board initialization. Once this is complete, the on board reset logic is released.

2.6.2. PCI Software Reset

Any PCI master (usually the host) can reset all F5 Carrier Board hardware *except* the PCI bus interface logic, using the using the following procedure on the PLX PCI PCI interface chip.

1. Set the PCI Adapter Software Reset Bit (bit 30) in the PCI EEPROM control register (PCI offset 0x6C, local bus offset 0xEC) to “1”. This places the F5 Carrier Board in the reset state.

2. Set this same bit to “0”. This releases the F5 Carrier Board from reset.

3. Set the Reload Configuration Registers Bit (bit 29) in the PCI EEPROM control register (PCI offset 0x6C, local bus offset 0xEC) to “0”.

4. Set this same bit to “1”. This reloads the PCI configuration registers from EEPROM. The transition from 0 to 1 causes the reload to occur.

PCI bus configuration registers in the PCI are *not* affected by this reset, therefore PCI bus configuration cycles do not need to be issued.

After reset the PCI EEPROM needs to be reloaded as described above. The PCI EEPROM enable jumper J25 must be installed, and the EEPROM loaded with the correct values.

Note: Under Windows 95, the PLX PCI can be reset and then initialized from the EEPROM by using the **F5_Control** function with the F5_CTL_RESET action parameter. Refer to the function description in this guide and to the source code examples for complete details.

2.6.3. JTAG Reset

Setting the /GRESET input of the JTAG IN connector (J10 pin 20) to 0 volts resets

- All processor nodes
- JTAG Out
- Support logic

The /GRESET signal is a TRISTATE line that is shared across all F5 Carrier Board boards connected by a 20 pin JTAG connector. All F5 Carrier Boards that are connected together through a JTAG chain can be simultaneously reset by asserting this line. This ensures that all F5 Carrier Boards that are connected together via COMM PORT cables are reset simultaneously to avoid any damage due to contention on the COMM PORT direction settings.

To resume normal operation, the /GRESET signal must be tristated by an external driver. Pull up resistors on the board can then place the line at 5 volts.

3 Embedded ’C44 Node A

Node A consists of an embedded TMS320C44 operating at 60 MHz supporting the memory devices listed in the following table.

Table 4 Node A Memory

Memory	Type	Width	Size
C4x Local Bus	zero wait-state SRAM	32-bit	128k or 512k
C4x Near Global Bus	zero wait-state SRAM	32-bit	128k or 512k
Boot/IDROM	PEROM	8-bit	32k

The Node A embedded ’C44 uses only 24 external address lines. All Address locations are mapped within the 16M (longword) space. Therefore, the Node A embedded ’C44 does not use a TIM-40 style page register.

The global bus is buffered onto the Global Shared Bus allowing the processors to access the shared resources which are the Far Global SRAM, the DSP~LINK3and the PCI interface through the PLX PCI Local Bus. STRB0 is used to access the Near Global SRAM and STRB1 will be used to access any of the shared resources via the arbitrator circuitry.

3.1. Boot Source

Jumper J28 selects the boot mode of the embedded ’C44. When installed, the ’C44 boots from its PEROM; when removed, the the ’C44 boots from its COMM port.

3.2. Node A Memory Map

The following table shows the local and global memory map of the embedded ’C44. Although the ’C44 uses only 24 external address lines, all 32 are internally mapped to the local and global strobes by the CPU-Control Registers.

Table 5 Embedded 'C44 Memory Map

Bus	Strobe	C44 Address	Access
Local Bus		0000 0000h - 002F FFFFh	Reserved for internal 'C44 SRAM, Registers and Boot Loader
	LSTRB0	0030 0000h - 0037 FFFFh	Local SRAM (128K or 512kx32)
		0038 0000h - 3FFF FFFFh	Reserved
	LSTRB1	4000 0000h - 4000 7FFFh	PEROM _Boot-up address (read/write)
	(LSTRB0 on	4000 8000h - 6FFF FFFFh	Reflections
	boot up)	7000 0000h - 7000 7FFFh	PEROM_ID Location(read/write)
		7000 8000h - 7FFF FFFFh	Reflections
Global Bus	STRB0	8000 0000h - 8007 FFFFh	Near Global SRAM (128k or 512kx32)
		8008 0000h - BFFF FFFFh	Reserved
	STRB1	C000 0000h - C000 FFFFh	DSP~LINK3 A (Ready Control Access)
	(Global Shared Bus)	C001 0000h - C001 FFFFh	DSP~LINK3 B(Standard Access)
		C002 0000h - C002 FFFFh	DSP~LINK3 C(Fast Standard Access)
		C003 0000h - C003 FFFFh	DSP~LINK3 D(Address Strobe Control)
		C004 0000h -C01F FFFFh	Reflections
	STRB1	C020 0000h - C020 FFFFh	Arbiter Registers
		C021 0000h - C021 FFFFh	Reserved
		C022 0000 - C022 FFFFh	PLX PCI Internal Registers
		C023 0000h - C023 FFFFh	F5 IRQ Control/Status Registers
		C024 0000h -C02F FFFFh	Reflections
		C030 0000h - C037 FFFFh	Far Global SRAM (128k or 512k x32)
		C038 0000h -C03F FFFFh	Reserved
		C040 0000h -C07F FFFFh	PCI Master Window (4 Meg words)
		C080 0000h -FFFF FFFFh	Reserved

During boot-up, the entire local address bus is mapped to the LSTRB0. This allows the Node A 'C44 to have read and write access to the PEROM as well as its local SRAM. After booting, address range 4000 0000h to 7FFF FFFFh is mapped to LSTRB1 for read-only access to the PEROM.

3.3. 'C44 Memory Interface Control Registers

Local Memory Interface Control Register (LMICR) and Global Memory Interface Control Register (GMICR) values used by the Node A 'C44 are given in the following table.

Table 6 Node A Memory Control Register

	Local Memory Interface Control Register		Global Memory Interface Control Register	
Register Value	3D84 0000h		3D84 0000h	
Register Bits	Value	Description	Value	Description
STRB Switch	1	Inserts a cycle between STRB0 and STRB1 Reads	1	Inserts a cycle between STRB0 and STRB1 Reads
STRB Active	11101	LSTRB0: 0000 0000h - 3FFF FFFFh LSTRB1: 4000 0000h - 7FFF FFFFh	11101	LSTRB0: 8000 0000h - BFFF FFFFh LSTRB1: C000 0000h - FFFF FFFFh
LSTRB1 Pagesize	10000	128 kWords per bank	10000	128 kWords per bank
LSTRB0 Pagesize	10000	128 kWords per bank	10000	128 kWords per bank
STRB1 WTCNT	000	External RDY is used	000	External RDY is used
STRB0 WTCNT	000		000	
STRB1 SWW	00		00	
STRB0 SWW	00		00	

Note: In order to re-program the Node A PEROM, the LMICR must be programmed to the value **3E84 0000.** The Spectrum PEROM Programming Tool does this automatically.

3.4. Node A IIOF Lines

The four IIOF lines of the Node A 'C44 are assigned and configured according to the following table. User applications running on Node A must configure the 'C44's Interrupt Flag Register (IIF) accordingly for interrupts to be received.

Table 7 Node A IIOF Lines

Line	Source	Configuration	Comment
IIOF0	Application Specific Connector	Edge-triggered	Node A must determine the interrupt source externally.
	DSP~LINK3	Level-triggered	
IIOF1	Node B, C, or D	Level-triggered	via Interrupt Controller
IIOF2	Interrupt Control register	Level-triggered	Initially high if J28 is OUT (boot from COMM port; low if J28 is IN (boot from PEROM)
IIOF3	PLX PCI Chip	Level-triggered	PLX PCI LINT#0 or LSERR

4 TIM-40 Sites B, C, and D

The F5 Carrier Board accommodates single and double width TIM-40 modules on its three TIM-40 module sites (nodes B, C, and D). Each site has three 80-way connectors, supporting the top, bottom and optional Global Bus connectors.

The TIM-40 module specification was developed by Texas Instruments to deliver the full performance of TMS320C4x DSPs on a standardized parallel processing element. The standard provides physical, electrical interface, and system characteristics for module development. Modules are installed on TIM-40 carrier boards which connect the modules to each other and to the host system. Spectrum offers a variety of TIM-40 modules with various configurations including single and multiple TMS320C40, single and multiple TMS320C44 with SRAM, DRAM, or specialized I/O. Complete information on the TIM-40 specification can be found in the TIM-40 TMS320C4x Module Specification available from Texas Instruments.

Nodes can communicate with the PCI bus through Node A via the COMM Ports, or through the Far Global SRAM.

4.1. Communication Ports

Each node is connected to the others via COMM Ports. Each COMM Port can communicate at up to 20 Mbytes per second. Because ’C44 processors only have four COMM Ports, not all internal or external COMM Port from each node may be available, but a COMM Port link to Node A is always present from every other node regardless of which ’C4x processor is used on the node.

4.2. Clock Sources

TIM-40 clock input pins are supplied with a 60 MHz clock source. If a TIM-40 module requires a different clock speed, it will have to have its own on board clock source. The F5 Carrier Board can support TIM-40 modules with clock frequencies up to 60 Mhz.

Note: The F5 Carrier Board does not support TIM-40 modules with on board clock frequencies higher than 60 Mhz.

4.3. Global Bus

The global bus of each node is buffered onto the global shared bus to allow the access of the shared SRAM (Far Global SRAM) for each ’C4x processor. Each node can access the shared SRAM via STRB1. Access to the shared SRAM is granted to any of the TIM-40'C4x’s, the embedded 'C44, or the PCI host, by an arbitrator circuit.

The general global memory map for each TIM40 Node is shown in the following table.

Table 8 TIM-40 Global Memory Map

Strobe	C4x Address	Access
STRB0	8000 0000h - 9FFF FFFFh	Reserved for TIM-40 Module Global Memory
	A000 0000h - BFFF FFFFh	Reflections
STRB1 (Global Shared Bus)	C000 0000h - C000 FFFFh	DSP~LINK3-A (Ready Control Access)
	C001 0000h - C001 FFFFh	DSP~LINK3-B (Standard Access)
	C002 0000h - C002 FFFFh	DSP~LINK3-C (Fast Standard Access)
	C003 0000h - C003 FFFFh	DSP~LINK3-D (Address Strobe Control)
	C004 0000h - C01F FFFFh	Reflections
STRB1 (PLX Local Bus)	C020 0000h - C020 FFFFh	Arbiter Registers
	C021 0000 - C022 FFFFh	Reserved
	C023 0000h - C023 FFFFh	F5 IRQ Control/Status Registers
	C024 0000h -C02F FFFFh	Reflections
	C030 0000h - C037 FFFFh	Far Global SRAM (128k x 32 or 512k x 32)
	C038 0000h -C07F FFFFh	Reserved
	C080 0000h -FFFF FFFFh	Reflections

Note: The Global Memory Interface Control Register of the primary ’C4x on each TIM-40 site should be configured according to the preceding memory map.

5 PCI Bus Interface

The F5 Carrier Board is fully PCI revision 2.1 compliant through its card edge connector. The PLX PCI chip provides the interface between the F5 Carrier Board and the PCI bus. The PLX PCI is a *dual port* device with the PCI bus on one side and the PLX PCI Local Bus on the other. The PCI bus interface operates at a 33 MHz and can transfer data at up to 132 Mbytes per second into the internal FIFOs of the PLX PCI chip.

Refer to the *PLX PCI Data Sheet* for complete information on this chip.

The local bus operates at 40 MHz with 1 wait state (2 clock) cycles to the Far Global SRAM for a peak bandwidth of 80 Mbytes per second using 20 ns SRAM.

The following features are supported through the PLX PCI interface chip:

- Dual independent DMA controllers
- PCI bus access to the PLX PCI local bus via memory accesses
- Cx mode Local bus operation. *32-bit non-multiplexed address and data*
- PCI interrupts *Refer to the Interrupt Handling section for details*
- Serial EEPROM initialization on power up to default values
- Read/write access to PLX PCI registers from both the PCI bus and the Node A embedded ’C44
- 40 MHz crystal oscillator PLX PCI Local Bus clock
- 33 MHz CLK input from the PCI connector for the PCI bus clock
- Unaligned DMA transfers
- PLX PCI Burst Mode cycles to Far Global SRAM using 2 clock cycles
- Node A embedded ’C44 DMA bus master transfers on the PCI bus
- All node reset operation from the PLX PCI local bus reset pin LRESETo#
- PCI Bus Parity Error detection can be set to interrupt the Local Bus Host (Node A) or the PCI Bus Host

5.1. PCI Bus Memory Map

The memory map of the F5 Carrier Board from the PCI bus is shown in the following table. The addresses given are the offset addresses that must be added to the PCI Base address.

Table 9 PCI Bus Memory Map

Name	PCI Bus Address (PCI Base +)
Reserved/Reflections	0000 0000h - 007F FFFFh
Bus Control Registers	0080 0000h - 0083 FFFFh
Test Bus Controller Register	0084 0000h - 0087 FFFFh
PLX PCI Registers	0088 0000h - 008B FFFFh
Interrupt Registers	008C 0000h - 008F FFFFh
Reflections	0090 0000h - 00BF FFFFh
Far Global SRAM	00C0 0000h - 00DF FFFFh
Reserved	00E0 0000h - 00FF FFFFh

The PCI Host can access the far global SRAM, the Test Bus Controller, the interrupt registers and the arbiter registers via the PLX PCI local bus.

5.2. PLX PCI Implementation

The PLX PCI provides a compact high performance PCI bus master interface between the F5 Carrier Board and the PCI Bus. The PLX PCI allows the Node A embedded ’C44 to initiate DMA bus master transfers on the PCI bus.

The PLX PCI provides two independent bi-directional DMA channels with bi-directional FIFOs supporting one wait-state burst transfers between host and local memory. Each channel also supports full data chaining modes allowing concurrent operations. The chip also contains a bi-directional FIFO for efficient slave access.

A separate PCI memory space is setup by the PLX PCI to allow PCI access to the PLX PCI internal registers. The PCI host can only see a partial set of internal PLX PCI registers via normal PCI memory accesses. The PCI configuration registers and PLX PCI DMA registers are not visible to normal PCI address space.

Although the PLX PCI supports both I/O and Memory map capability, all devices are memory mapped on the F5 Carrier Board.

PCI Configuration Registers

The PLX PCI PCI Configuration Registers are available to the Embedded ’C44 processor, and to the PCI host in the PCI Configuration Address Space. The PCI host configures these registers during power up initialization.

The F5 Carrier Board uses these two Base Address Registers.

- PCI Base Address for Memory Mapped Runtime Registers
- PCI Base Address for Local Address Space 0

Local Configuration Registers

The PLX PCI Local Configuration Registers are available to the PCI host in PCI memory space at an offset from the F5 Carrier Board’s PCI Runtime Base Address. These registers are initialized from the PLX PCI’s EEPROM during power up initialization.

Shared Runtime Registers

The PLX PCI Shared Runtime Registers, and Local DMA Registers are also available to the PCI host in PCI memory space, at an offset from the F5 PCI Runtime Base Address. These registers are initialized from values in Node A’s PEROM during power up initialization.

Note: 'C4x processors addresses map to 32-bit words; PCI bus addresses map to 8-bit words.

5.3. User LED

The green LED near the Application Specific connector on the F5 Carrier Board is connected to the USERO output pin on the PLX PCI device. This pin is controlled by the General Purpose Output Register bit (bit 16) in the PLX PCI EEPROM Control Register. Refer to the *PLX PCI Data Sheet* for the location and description of this register.

- To turn the LED on, write a “0” to this register bit.
- To turn it off write a “1” to this register bit.

By default the LED is off after a power on reset.

6 Internal Architecture

6.1. PLX PCI Local Bus

This bus connects the current Global Shared Bus master to the Far Global SRAM, allows CPU Node A access to the PLX PCI internal registers. It also allows the current PCI master to access the Far Global SRAM via direct access. The CPU Node A can program the PLX PCI internal DMA controller to transfer data between Far Global SRAM and the PCI bus. Arbiter logic allows a CPU Node to run cycles to the DSP~LINK3 interface in parallel with the PLX PCI chip running cycles to the Far Global SRAM to allow improved performance.

The PCI bus master can make requests to access the PLX PCI Local Bus via the PLX PCI local bus. The PLX PCI Local Bus arbiter grants the PLX PCI Local Bus if the Local Bus is unused.

The PCI bus can hold the PLX PCI Local Bus indefinitely once it has been granted to the PCI bus. It is up to the applications software to prevent PCI accesses from clogging the Global Shared Bus.

The PLX PCI internal DMA is awarded the same access rights as PCI hosts because the arbiter cannot discriminate between the two cycle types. The Local Latency and Pause Timers in the PLX PCI can be used to prevent the PLX PCI DMA from clogging the PLX PCI Local Bus. These counters hold and release the PLX PCI Local Bus during PLX PCI DMA. The PLX PCI DMA hangs onto the bus until it is finished, or until the Local Latency timer times out. It then pauses until the Pause Timer counts down before re-acquiring the PLX PCI Local Bus. This allows the Global Shared Bus processors access to the PLX PCI Local Bus.

The ’C4x processors request the PLX PCI Local Bus by executing cycles within the longword address range from C020 0000 to FFFF FFFF of the Global Bus /STRB1 memory space. The ’C4x /STRB1 signal is sent to the Global Shared Bus arbiter to act as a bus request signal. Once the arbiter picks the next Global Shared Bus master, it grants the processor the bus by enabling the processor global bus signals onto the Global Shared Bus. If the address is also within PLX PCI Local Bus space, then the PLX PCI Local Bus arbiter will also be asked to grant the bus to the ’C4x processor.

6.2. Far Global Memory

The Far Global SRAM is a section of SRAM that can be accessed by the TIM-40 sites, the Embedded ’C44, and the PCI host via PLX PCI local bus cycles.

It contains a minimum of 128k by 32-bit ram, expandable to 512k by 32-bit and supports the following features:

- 1 wait state access speed by all nodes using a 30 MHz H1 clock.

- 1 wait state access speed by the PLX PCI local bus using a 40 MHz local bus clock.
- 8-, 16-, and 32-bit writes from the PCI Bus using PLX PCI LBE[3:0] outputs.

Peak bandwidth for the Far Global SRAM is given in the following table.

Table 10 Far Global SRAM Performance

Master	Read	Write
PCI to Far Global SRAM	20 M longwords per second (80 M bytes per second)	20 M longwords per second (80 M bytes per second)
Any C4x Node to Far Global SRAM (for 60 MHz DSPs)	15 M longwords per second (60 M bytes per second)	10 M longwords per second (40 M bytes per second)

6.3. Global Shared Bus

The Global Shared Bus connects the global busses of the four ’C4x processor nodes, the DSP~LINK3 interface, and the PLX PCI Local Bus interface. Not all devices on the Global Shared Bus can reach all memory locations. Access modes by the embedded ’C44 Node A, TIM-40 site Nodes B to D, a PCI master and a PLX PCI DMA transfer to the different memory locations are shown in the following table.

Table 11 Global Shared Bus Memory Access Modes

Memory Location	TIM-40	Embedded'C44	PCI Master	PLX PCI DMA
Near Local SRAM	R/W their own	R/W their own	-	-
Near Global SRAM	R/W their own	R/W their own	-	-
Far Global SRAM	R/W	R/W	R/W	R/W
PLX PCI Internal Registers	-	R/W	R/W	-
PCI Targets (PCI Slaves)	-	R/W (via DMA)	R/W	R/W
Test Bus Controller	-	-	R/W	-
DSP~LINK3	R/W	R/W	-	-

The Global Shared Bus can be mastered by any of the four processor nodes. Each node is given equal access rights to the Global Shared Bus via a round robin priority scheme. A programmable Latency Timer sets a minimum number of clocks on the bus for each processor (a “slice”). The number of clocks granted to each processor is controlled by the F5 Latency Timer register. Each processor is given the same number of clock cycles on the bus.

If a processor targets the Far Global SRAM then the Arbitration logic requests access to the PLX PCI Local Bus at the same time. The PLX PCI Local Bus arbiter can grant the PLX PCI Local Bus to any PCI master cycles, which can run concurrently to Global Shared Bus activity.

If PCI requests the PLX PCI Local Bus, the current 'C4x Node is allowed to finish it’s current cycle. The arbiter then grants the PLX PCI Local Bus to the PLX PCI chip. Once the PCI host releases the bus, the arbiter assigns the bus to the next processor in the queue, and restarts the Latency Timer.

After the Latency Timer terminates a round robin priority assigns the bus to the next processor on the list. Ownership is granted depending upon which processor makes the request and which processor last controlled the bus.

If a processor finishes its Global Shared Bus activity early, then as soon as the Arbitration logic can safely determine that the current bus owner has stopped running back to back cycles the next processor is granted the Global Shared Bus.

If there are no requesters, the current master retains ownership.

7 DSP~LINK3 Interface

The DSP~LINK3 interface allows external DSP~LINK3 I/O modules to be attached to the F5 Carrier Board through the ribbon cable connector or by the mezzanine connector. Both connectors can be used at the same time.

The F5 Carrier Board can support up to 4 slave DSP~LINK3 devices. If a DSP~LINK3 module is installed, up to 3 additional devices can be connected to the ribbon cable connector; otherwise, up to 4 devices can be connected to the ribbon cable connector. The ribbon cable can be up to 12 inches (30 cm) long.

Any ’C4x node can access the DSP~LINK3 interface from its global bus; but it cannot be accessed from the PCI bus.

The DSP~LINK3 reset line is controlled by the F5 Carrier Board DSP~LINK3 Reset Register. It is asserted by writing a “1” to the register or by a board reset condition. A DSP~LINK3 reset should be at least 1 µs long.

7.1. DSP~LINK3 Operating Modes

The F5 Carrier Board supports the three data transfer modes and the address page turn (/ASTRB) cycle of the DSP~LINK3 interface. The timing of the DSP~LINK3 interface for the F5 Carrier Board is based on multiples of the DSP’s H1 clock. For example, the length of a Standard Fast transfer DSP~LINK3 is 5 times the DSP’s H1 clock signal. If a H1 cycle is about 33 ns, for the 60 MHz DSP, then a Standard Fast transfer is about 165 ns. The following table describes the different transfer modes of the interface.

Standard	For slave boards that are similar to DSP~LINK1 slave boards and operate with a fixed, minimum 130 ns access time. Cycle time is 7 times H1.
Standard Fast	For DSP~LINK3 slave boards that have fast, fixed access times. Cycle time cycle is 5 times H1.
RDY Controlled	For DSP~LINK3 slave boards that require variable length access times. /DSTRB is active until the slave asserts the DSP~LINK3 ready signal (/RDY) to end the cycle.
/ASTRB Cycle	For slave boards that require more than the 16 KWords of addressing provided by the standard DSP~LINK3 address lines. The bus master uses the /ASTRB cycle to place the page address onto the DSP~LINK3 data lines. It determines which address page is accessed on the slave board. This allows access to up to 2^{14} address pages with each address page having an address depth of 2^{14}. The /ASTRB Cycle has the same timing as the Standard Fast transfer cycle.

Each mode occupies its own 64K address space on the Global Shared Bus. The following table shows how the F5 Carrier Board supports the different DSP~LINK3 operating modes.

Table 12 DSP~LINK3 Operating Modes

Mode	Base Address	Read Performance	Write Performance
Ready Control Access*	C000 0000h	7 Mbytes/sec	7 Mbytes/sec
Standard Access	C001 0000h	16 Mbytes/sec	14 Mbytes/sec
Fast Standard Access	C002 0000h	22 Mbytes/sec	22 Mbytes/sec
Address Strobe Control	C003 0000h	not applicable	not applicable

*Best Case

7.2. Interface Signals

The DSP~LINK3 interface consists of two 16-bit bi-directional buffers for data, a16-bit address latch, and a control signal buffer. The control signals are terminated via a SCSI terminator. The DSP~LINK3 interface signals are:

- 32 data I/O lines: D[31..0]
- 16 address outputs: A[15..0] A15 and A14 are used for slave device (board) selection.
- Read (/RD), write (/WR), and reset (/RST) outputs
- Tri-state ready (/RDY) input
- 4 interrupt inputs (IRQ0 to IRQ3). Each interrupt is routed to the IIOF0 line of a specific ’C4x node; IRQ0 to Node A, IRQ1 to Node B, and so on. By installing jumper J24, all IRQs can also be routed to the IIOF0 line of Node A’s embedded 'C44 through an OR gate.

Refer to *DSP~LINK3 specification* for details (available from Spectrum’s internet web site at http://www.spectrumsignal.com)

7.3. DSP~LINK3 Reset

The DSP~LINK3 reset (/RST) output can be used to reset any DSPLINK3 module connected to the F5 Carrier Board. The DSP~LINK3 reset (/RST) output is asserted during a power up reset from the RST# of the PCI bus and during a PCI software reset of the PLX PCI chip.

It can also be asserted under software control by any of the processor nodes or a host on the PCI bus through the DSP~LINK3 Reset register. This register is accessible on the ‘C4x Global Bus at address C020 0004h, or address 80 0010h offset from the PCI base address on the PCI bus. Reset is asserted by writing a “1” to the LSB of this register and released by writing a “0” to the LSB.

8 JTAG Interface and Debug Capability

The F5 Carrier Board supports JTAG in-circuit emulation from a built in Test Bus Controller and a Windows 95 debug monitor. JTAG in-circuit emulation is fed by the PCI host via the Test Bus Controller, or C Source Debugging can be done through the JTAG connectors to an emulator board running a debug monitor on an adjacent PC.

Each of the ’C4x processors has a JTAG interface for debug purposes. JTAG data lines are routed to each available ’C4x node in turn. The Test Bus Controller permits the PCI interface to operate the JTAG chain. Additionally, there are two JTAG connectors, JTAG IN and JTAG OUT, which can route the JTAG chain off-board. If a JTAG IN connection with a clock signal is present the Test Bus Controller is automatically disabled.

Note: The initialization code loaded into the PLX PCI chip from its EEPROM disables the chip’s Memory Space 0 Prefetch feature. This ensures that the PCI bus can properly access the Test Bus Controller for debugging purposes. Refer to the *PLX PCI Data Sheet* for more information.

8.1. JTAG Chain

The full JTAG chain is shown in the following diagram. Unoccupied TIM-40 sites are bypassed. For multiple processor TIM-40 modules, refer to the TIM-40 module documentation for information on the order in which the processors are connected in the JTAG scan path.

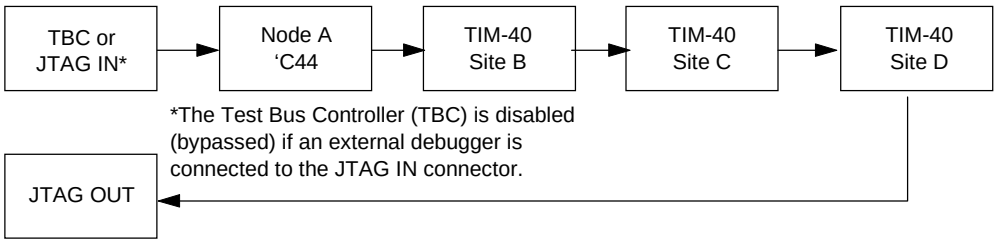

Figure 5 JTAG Chain

The JTAG IN input is buffered to reduce the load on an external JTAG device. The JTAG OUT output is buffered to guarantee enough drive to external JTAG loads.

8.2. Debugging Multiple Boards Using JTAG

Up to three F5 Carrier Boards can be daisy-chained together through their JTAG connectors for multi-board debugging. The JTAG cable of the external debugger should only be connected to the JTAG IN of the first board. The JTAG OUT of the first board should be connected to the JTAG IN of second board. The JTAG OUT of the second board should be connected to the JTAG IN of third board and so on. See the following figure.

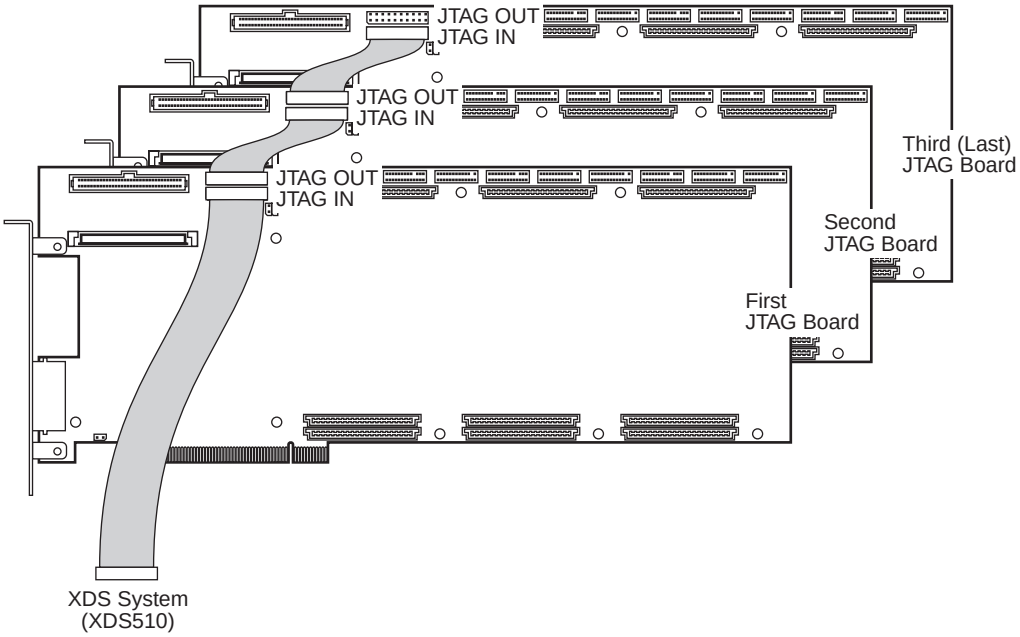

Figure 6 Multi-Board JTAG Connections

Note: All hardware must be powered off before the JTAG cable are connected and the JTAG chain is set up.

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9 Interrupt Handling

An Interrupt Controller addressed on the PLX PCI Local Bus handles interrupts on the F5 Carrier Board. A set of registers addressed in this controller is used to monitor and control the interrupts. Interrupt sources and destinations are shown in the following list.

Interrupt Sources	Interrupt Destinations
• IIOF1 on ’C4x nodes B, C, and D	• IIOF1 on ’C4x node A
• DSP~LINK3 IRQ0 to IRQ3	• IIOF0 and IIOF2 on any ’C4x node
• PCI host	• IIOF3 on ’C4x node A
• PLX PCI chip	• PCI host
• Application Specific Interrupt	

Note: The IIOF lines of all the ’C4x nodes are tri-stated during ’C4x bootup. Each DSP must perform an IACK command to enable its own interrupt signals.

Interrupt routing on the F5 Carrier Board is shown in the following diagram and is described in the following subsections. For complete details on the Interrupt Controller registers, see the *Registers* section.

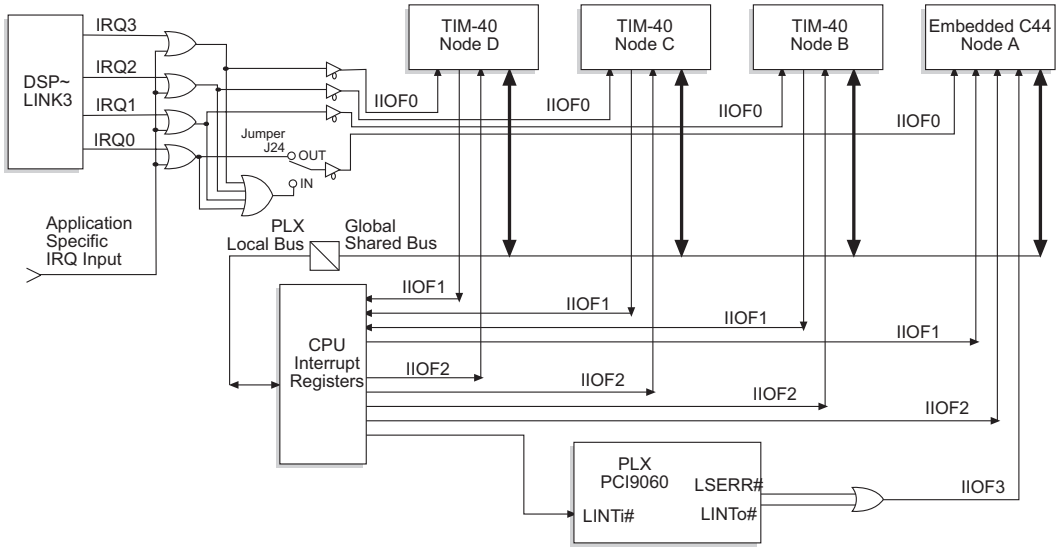


Figure 7 F5 Interrupt Routing

9.1. PLX PCI Interrupts

The Interrupt Controller performs a logical OR of the PLX PCI chip LSERRo# and LINTo# outputs and routes the result to the IIOF3 input of the embedded Node A ’C44. The cause of the IIOF3 interrupt is identified by reading the appropriate status registers in the PLX PCI chip.

Refer to the *PLX PCI Data Sheet* for further information on these PLX PCI registers.

9.2. PCI to Node X Interrupts

The PCI host can interrupt any of the four ’C4x nodes by writing to the appropriate *PCI to Node* x *IRQ* registers, where “x” indicates the node to be interrupted. This causes the IIOF2 input on the corresponding C4X to be asserted. The 'C4x processor can clear this by performing an IACK cycle.

9.3. Node X to PCI Interrupts

Each CPU Node can interrupt the PCI host by writing a “1” to the appropriate *Node* x *to PCI IRQ* register, where *x* indicates the interrupting node. The PCI host can clear these interrupts by writing a “0” to the same register(s). The *Node X to PCI IRQ Status* register allows the PCI host to identify which node(s) are asserting a PCI interrupt. Multiple nodes can interrupt the PCI at the same time; it is up to the application software to handle these simultaneous interrupts.

9.4. Node B, C, and D to Node A Interrupts

TIM-40 sites B, C, and D can interrupt the embedded 'C44 of Node A by asserting, and then negating, their IIOF1 outputs. The outputs are latched in the Interrupt Controller and then routed to IIOF1 on Node A. The embedded 'C44 can identify the source of the interrupt by reading the *Node BCD to A IRQ Status* register. This interrupt can then be cleared by writing a “0” to the appropriate *Node* x *to Node A IRQ Clear* register, where *x* is the node that caused the interrupt to Node A.

9.5. DSP~LINK3 Interrupts

Four DSP~LINK3 active-low, level-sensitive interrupts are individually mapped to the IIOF0 inputs of the four 'C4x nodes. Additionally, jumper J24 can configure all of these interrupts to be routed to the IIOF0 of the Node A embedded 'C44 through a quad-input OR gate. During 'C4x node configuration, these inputs are routed through tri-state buffers on the F5 Carrier Board to prevent any interference with the 'C4x node boot mode selection during power up initialization. All four DSP~LINK3 interrupts are driven by open collector drivers so that more than one device on DSP~LINK3 can drive the same IRQ line. The IIOF outputs to the TIM-40 sites are tri-stated until the IACK input for each TIM-40 is asserted to indicate the boot period is finished.

The default routing for the DSP~LINK3 (J24 not installed) is shown in the following table.

Table 13 DSP~LINK3 Interrupt Routing

DSP~LINK3 Interrupt Source	C4x IIOF0 Input Interrupt Destination
IRQ3	TIM-40 site D
IRQ2	TIM-40 site C
IRQ1	TIM-40 site B
IRQ0	Embedded 'C44 Node A

The F5 Carrier Board does not latch the DSP~LINK3 interrupts. Refer to the documentation on each module for information on acknowledging and clearing DSP~LINK3 interrupts.

9.6. Application Specific Interrupt

The negative edge-triggered Application Specific interrupt input is internally latched on the F5 Carrier Board. This interrupt is simultaneously OR'ed with each of the four DSP~LINK3 interrupts. The 'C4x cannot distinguish between DSP~LINK3 and Application Specific interrupts on IIOF0. Any 'C4x node can clear an Application Specific interrupt by writing a "0" to the *Application Specific IRQ* register.

Note: If the source of a Application Specific interrupt asserts the signal too long, the 'C4x may not be able to clear it. Ensure that the interrupt source releases the interrupt before the 'C4x Interrupt Service Routine begins to clear the interrupt.

10 Registers

The 32-bit Bus Arbitration and Interrupt Control registers can be accessed from the Global Bus of any ’C4x node (A, B, C, or D) and also from the PCI bus. Register addresses are absolute for ’C4x access, but are an offset from the PCI base address of the F5 Carrier Board.

Note: The registers are sequentially addressed from the Global Bus, but are addressed at every fourth address from the PCI bus. This is because the registers are 32-bit, and the PCI data bus is byte addressed.

Table 14 Register Addresses

Register	‘C4x Global Bus Address	PCI bus Address
Latency Count	C020 0000h	PCI Base + 80 0000h
CPU ID	C020 0001h	PCI Base + 80 0004h
/CONFIG	C020 0002h	PCI Base + 80 0008h
Node A /CONFIG	C020 0003h	PCI Base + 80 000Ch
DSP~LINK3 Reset	C020 0004h	PCI Base + 80 0010h
PCI to Node A IRQ	C023 0000h	PCI Base + 8C 0000h
PCI to Node B IRQ	C023 0001h	PCI Base + 8C 0004h
PCI to Node C IRQ	C023 0002h	PCI Base + 8C 0008h
PCI to Node D IRQ	C023 0003h	PCI Base + 8C 000Ch
Node A to PCI IRQ	C023 0004h	PCI Base + 8C 0010h
Node B to PCI IRQ	C023 0005h	PCI Base + 8C 0014h
Node C to PCI IRQ	C023 0006h	PCI Base + 8C 0018h
Node D to PCI IRQ	C023 0007h	PCI Base + 8C 001Ch
Node X to PCI IRQ Status	C023 0008h	PCI Base + 8C 0020h
Node B to Node A IRQ Clear	C023 0009h	PCI Base + 8C 0024h
Node C to Node A IRQ Clear	C023 000Ah	PCI Base + 8C 0028h
Node D to Node A IRQ Clear	C023 000Bh	PCI Base + 8C 002Ch
Node BCD to A IRQ Status	C023 000Ch	PCI Base + 8C 0030h
Application Specific IRQ	C023 000Dh	PCI Base + 8C 0034h

Latency Count Register

'C4x Global Bus Address	C020 0000h
PCI bus Address	PCI Base + 80 0000h

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Latency Count Value			

The 4-bit Latency Count register sets the amount of time that each processor can use the Global Shared Bus. The amount of time is based on the number of cycles from Node A's H1 clock. The 4-bit value written to the Latency Count register is used to calculate the number of H1 clock cycles allocated to each processor from between 2 to 62.

Each time a processor is granted the bus, the value in the Latency Counter register is multiplied by four (4) and loaded into a latency timer which then counts down to zero. Upon reaching zero, the Global Shared Bus is assigned to the next processor waiting to access it.

Upon reset, the Latency Count register is assigned the value "1111".

CPU ID Register

'C4x Global Bus Address	C020 0001h
PCI bus Address	PCI Base + 80 0004h

D31..							..D8
Reserved							

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						CPU ID	

This read-only register allows a 'C4x to identify itself. The value in the register is determined by the node that is currently granted access to the bus. For example, if the node A 'C4x reads this register, it will see a value that indicates that it is node A; if the node B 'C4x reads it, it will see a value indicating that it is node B.

Values for the register are:

Node	D1	D0
A	0	0
B	0	1
C	1	0
D	1	1

/CONFIG Register

'C4x Global Bus Address	C020 0002h
PCI bus Address	PCI Base + 80 0008h

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							/CONFIG

The read-only /CONFIG register indicates the state of the TIM-40 /CONFIG line. The PCI host can use this to determine when all the installed 'C4x processors have finished booting.

- 1 = All installed 'C4x processors have finished their boot sequences
- 0 = Boot sequences are still in progress

Node A /CONFIG Register

'C4x Global Bus Address	C020 0003h
PCI bus Address	PCI Base + 80 000Ch

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							/CONFIG

The Node A /CONFIG register is used by the Node A embedded 'C44 to indicate its /CONFIG status. Node A should write a "0" to this register at the start of its configuration, and write a "1" to the register when it has finished its configuration. The value of this register is combined with the /CONFIG lines of nodes B, C, and D to provide the board-level /CONFIG signal. The board-level /CONFIG signal can be read from the /CONFIG register.

- 1 = The Node A 'C44 has finished its boot sequences
- 0 = The Node A 'C44 Boot sequence is still in progress

DSP~LINK3 Reset Register

'C4x Global Bus Address	C020 0004h
PCI bus Address	PCI Base + 80 0010h

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							Reset

This register allows the DSP~LINK3 interface to be reset.

- To reset the DSP~LINK3 interface, write a "1" to bit D0.
- To clear the reset, write a "0" to bit D0.

PCI to Node x *IRQ Registers*

Register	'C4x Global Bus Address	PCI bus Address
PCI to Node A IRQ	C023 0000h	PCI Base + 8C 0000h
PCI to Node B IRQ	C023 0001h	PCI Base + 8C 0004h
PCI to Node C IRQ	C023 0002h	PCI Base + 8C 0008h
PCI to Node D IRQ	C023 0003h	PCI Base + 8C 000Ch

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							IRQ

These registers are used by the PCI host to cause interrupts to each 'C4x processor. The output of each of these registers are sent to the appropriate IIOF2 input of each CPU Node.

- To cause an interrupt on a target node, the PCI host writes a "1" to the appropriate register.
- The interrupt is cleared by the 'C4x processor performing an IACK cycle.

Each 'C4x processor knows the IIOF2 source is the PCI host, by definition.

Node x *to PCI IRQ Registers*

Register	'C4x Global Bus Address	PCI bus Address
Node A to PCI IRQ	C023 0004h	PCI Base + 8C 0010h
Node B to PCI IRQ	C023 0005h	PCI Base + 8C 0014h
Node C to PCI IRQ	C023 0006h	PCI Base + 8C 0018h
Node D to PCI IRQ	C023 0007h	PCI Base + 8C 001Ch

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							IRQ

These registers are used by the 'C4x nodes to cause an interrupt to the PCI bus Host.

- A 'C4x processor can interrupt the PCI host by writing a 1 to the appropriate *Node* x *to PCI IRQ* register.
- The PCI host can clear the interrupt by writing a 0 to the appropriate *Node* x *to PCI IRQ* IRQ register.

The 'C4x node should **only** use the IRQ register assigned to it. The 'C4x node can identify itself by reading the CPU ID register. The CPU ID register is one of the Bus Arbitration registers.

Node X to PCI IRQ Status Register

'C4x Global Bus Address	C023 0008h
PCI bus Address	PCI Base + 80 0020h

D31..	..D8
Reserved	

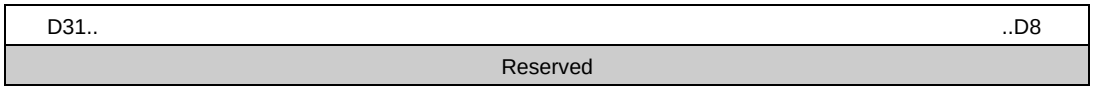
D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Node A

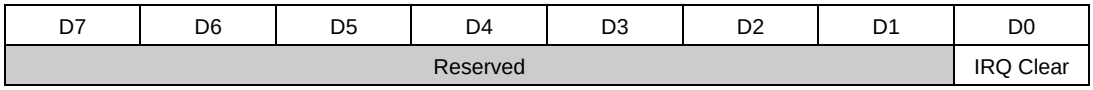
This read-only register allows the PCI Host to identify all possible sources of 'C4x Node X to PCI interrupts in one read cycle.

- If a node has generated a pending IRQ, a "1" will be placed in the appropriate bit of this register.

Node x *to Node A IRQ Clear Registers*

Register	'C4x Global Bus Address	PCI bus Address
Node A to Node A IRQ Clear	C023 0009h	PCI Base + 8C 0024h
Node B to Node A IRQ Clear	C023 000Ah	PCI Base + 8C 0028h
Node C to Node A IRQ Clear	C023 000Bh	PCI Base + 8C 002Ch





These registers allow the Node A embedded 'C44 to clear an interrupt generated to its IIOF1 pin by a TIM-40 sites (Nodes B, C, or D).

Each register corresponds to one of the three TIM-40 sites which can generate an IIOF1 interrupt on Node A. When Node A receives an IIOF1 interrupt it can read the *BCD to A IRQ Status* register to determine which of the TIM-40 sites generated the interrupt.

- To clear a IIOF1 interrupt on Node A, write a "0" to the *Node* x *to Node A IRQ Clear* register corresponding to the node that generated the interrupt.

Node BCD to A IRQ Status Register

'C4x Global Bus Address	C023 000Ch
PCI bus Address	PCI Base + 80 0030h

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Reserved

This read-only register allows the Node A embedded 'C44 to identify all possible sources of a IIOF1 interrupt on Node A in one read cycle.

- If a node has generated an pending interrupt on the IIOF1 pin of Node A, a "1" will be placed in the appropriate bit of this register.

Application Specific IRQ Register

'C4x Global Bus Address	C023 000Dh
PCI bus Address	PCI Base + 80 0034h

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							IRQ

This register allows a node to clear an Application Specific interrupt.

- To clear an IIOF0 interrupt caused by an Application Specific interrupt, write a "0" to bit D0.

11 Specifications

The F5 Carrier Board is electrically compliant with PCI Specification Rev 2.1 for 5 Volt cards.

Table 15 F5 Specifications

Supply Voltage	+5 Volts
Current Consumption (no TIM-40 modules)	1.8 Amperes
Power (*typical*)	9 Watts
Height	122.56 mm
Width	312 mm
Operating Temperature	0ºC to 50ºC

Mechanical Size Exceptions

The F5 Carrier Board conforms to the PCI Rev 2.1 Mechanical Specification for 5 volt ISA Slot Full Length card with the following exceptions:

- The F5 board height is 122.56 mm tall. This exceeds the PCI maximum height of 106.68 mm tall. Note that it is as tall as a standard ISA board, so that it can fit into a system that has room for full height ISA cards.

- The F5 board exceeds the PCI slot back side maximum component height due to the height of the SRAM SOJ packages on the back of the F5 board.

PCI slot back side maximum component height	2.67 mm
F5 Carrier Board with SOJ SRAM back side height	3.5 mm
Exceeds PCI slot back side maximum component height by	0.83 mm

12 External Interface Connectors

The F5 Carrier Board has the following external connectors:

- PCI card edge
- DSP~LINK3 ribbon cable
- DSP~LINK3 module
- ’C4x COMM Ports (10)
- Application Specific Pins
- JTAG IN
- JTAG OUT.

The locations for these connectors on the F5 Carrier Board are shown in the following diagram.

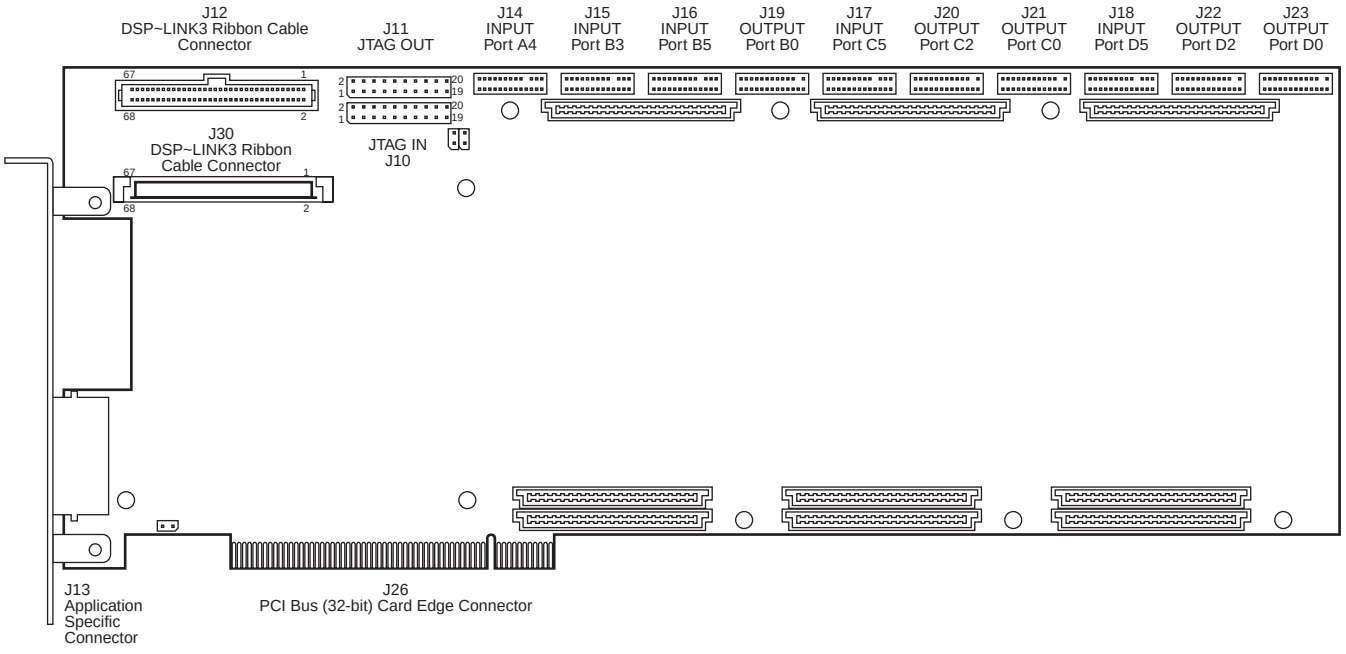


Figure 8 F5 Connector Locations

Note: Refer to the TIM-40 Specification for a description of the TIM-40 connectors.

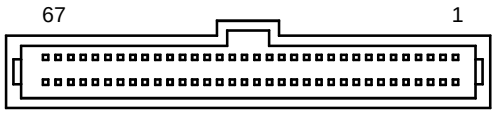
12.1. PCI Card Edge Connector

A standard 120 pin Card Edge Connector provides the interface to the PCI bus. It is keyed as a 5 Volt, 32-bit PCI card. The pin assignment is fully compliant with the *PCI Local Bus Specification*.

12.2. DSP~LINK3 Connector

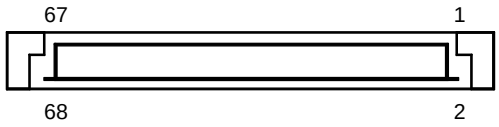
Connector pinouts for the DSP~LINK3 module and ribbon cable connectors are given in the following tables. Refer to the *DSP~LINK3 Specification* for complete information.

Table 16 DSP~LINK3 Ribbon Cable Connector Pinout



Pin Number	Signal	Pin Number	Signal
1	VCC 1	2	A15
3	A14	4	A13
5	A12	6	A11
7	A10	8	A9
9	A8	10	A7
11	A6	12	A5
13	A4	14	A3
15	A2	16	A1
17	A0	18	R/W_
19	/RESET	20	GND
21	/DSTRB	22	GND
23	/ASTRB	24	GND
25	/RDY	26	GND
27	/INT0	28	GND
29	/INT1	30	GND
31	/INT2	32	GND
33	/INT3	34	GND
35	D31	36	D30
37	D29	38	D28
39	D27	40	D26
41	D25	42	D24
43	D23	44	D22
45	D21	46	D20
47	D19	48	D18
49	D17	50	D16
51	D15	52	D14
53	D13	54	D12
55	D11	56	D10
57	D9	58	D8
59	D7	60	D6
61	D5	62	D4
63	D3	64	D2
65	D1	66	D0
67	GND	68	RSVD

Table 17 DSP~LINK3 Module Connector Pinout

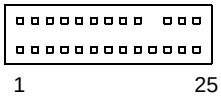
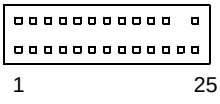


Pin Number	Signal	Pin Number	Signal
1	VCC (+5 V)	35	A15
2	A14	36	A13
3	A12	37	A11
4	A10	38	A9
5	A8	39	A7
6	A6	40	A5
7	A4	41	A3
8	A2	42	A1
9	A0	43	R/W_
10	/RESET	44	GND
11	/DSTRB	45	GND
12	/ASTRB	46	GND
13	/RDY	47	GND
14	/INT0	48	/INT2
15	/INT1	49	/INT3
16	D31	50	D30
17	D29	51	D28
18	D27	52	D26
19	D25	53	D24
20	D23	54	D22
21	D21	55	D20
22	D19	56	D18
23	D17	57	D16
24	D15	58	D14
25	D13	59	D12
26	D11	60	D10
27	D9	61	D8
28	D7	62	D6
29	D5	63	D4
30	D3	64	D2
31	D1	65	D0
32	RSVD	66	RSVD
33	VCC (+5 V)	67	VCC (+5 V)
34	+12 V (unfiltered)	68	-12 V (unfiltered)

12.3. 'C4x COMM Port Connections

Ten high-density 26-pin .050" x .100" (1.27mm x 2.54mm) pitch headers provide un-buffered connections to COMM ports of the Node A embedded 'C44 and the Node B, C, and D TIM-40 sites. The connectors are polarized (keyed) to prevent accidental connection of inputs to outputs.

Table 18 COMM Port Connector Pinouts

J14: Node A COMM Port 4 INPUT J15: Node B COMM Port 3 INPUT J16: Node B COMM Port 5 INPUT J17: Node C COMM Port 5 INPUT J18: Node D COMM Port 5 INPUT				J19: Node B COMM Port 0 OUTPUT J20: Node C COMM Port 2 OUTPUT J21: Node C COMM Port 0 OUTPUT J22: Node D COMM Port 2 OUTPUT J23: Node D COMM Port 0 OUTPUT			
							
Pin Number	Top Row	Pin Number	Bottom Row	Pin Number	Top Row	Pin Number	Bottom Row
1	CD0	2	GND	1	CD0	2	GND
3	CD1	4	GND	3	CD1	4	GND
5	CD2	6	GND	5	CD2	6	GND
7	CD3	8	GND	7	CD3	8	GND
9	CD4	10	GND	9	CD4	10	GND
11	CD5	12	GND	11	CD5	12	GND
13	CD6	14	GND	13	CD6	14	GND
15	CD7	16	GND	15	CD7	16	GND
17	/CREQ	18	GND	17	/CREQ	18	GND
19	/CACK	20	Key	19	/CACK	20	GND
21	/CSTRB	22	GND	21	/CSTRB	22	GND
23	/CRDY	24	GND	23	/CRDY	24	Key
25	DIRIN	26	DIROUT	25	DIRIN	26	DIROUT

12.4. Application Specific Connector

A 40-pin right angle header (SAMTEC TMS-120-01-G-D-RA) with 0.05” x 0.10” grid pin spacing is used for Application Specific connector. It presents the 12 user defined pins of each TIM-40 site (Nodes B, C, and D), as well as an application specific interrupt request line to the F5 Carrier Board end plate.

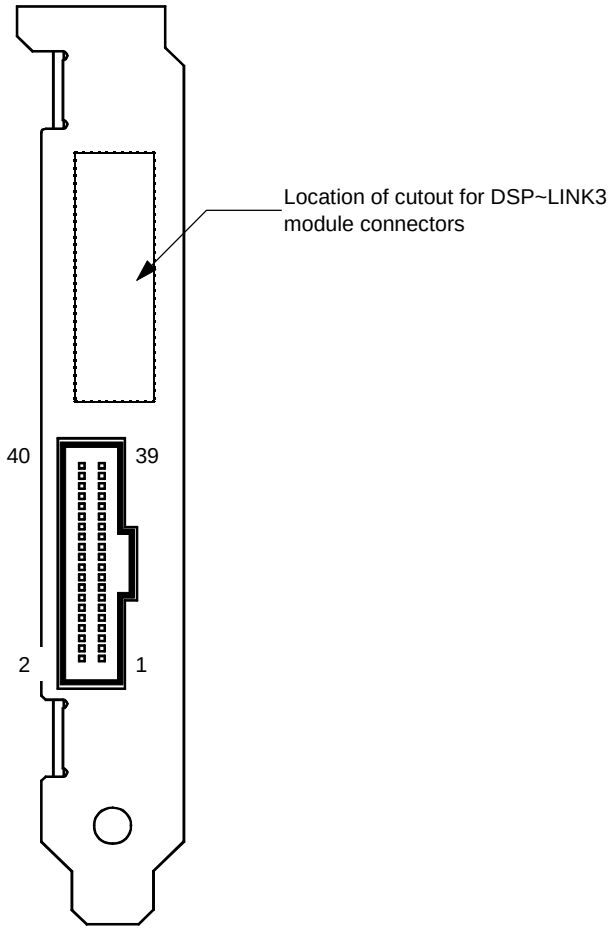


Figure 9 Application Specific Connector

The following table shows the pinout for the Application Specific connector. The TIM-40 application specific pin corresponding to the connector pin is indicated by two characters; the node followed by the pin. For example, “B1” indicates the application specific pin of the Node B TIM-40 site.

Table 19 Application Specific Connector Pinout

Pin Number	Top Row	Pin Number	Bottom Row
1*	B1	2	B2
3	B3	4*	B4
5*	B5	6	B6
7	B7	8*	B8
9*	B9	10	B10
11	B11	12*	B12
13*	C1	14	C2
15	C3	16*	C4
17*	C5	18	C6
19	C7	20*	C8
21*	C9	22	C10
23	C11	24*	C12
25*	D1	26	D2
27	D3	28*	D4
29*	D5	30	D6
31	D7	32*	D8
33*	D9	34	D10
35	D11	36*	D12
37*	GND	38	Interrupt**
39	GND	40*	GND

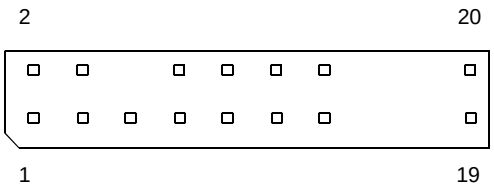
*Wide PCB traces
**refer to Interrupt Handling section

Note: For better transition of high integrity analog signals, alternate traces for this connector are wider than those for the other pins. This allows applications to use the wide traces as ground shields for the other traces.

12.5. JTAG Connectors

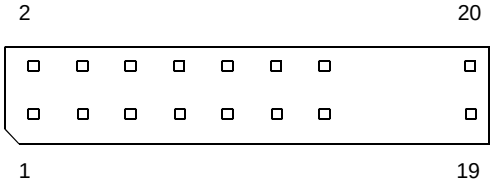
JTAG connection is provided by a pair of 0.1” by 0.1” grid 20-pin header connectors (AMP 103186-10). One for JTAG out, and one for the JTAG in which are located on the F5 Carrier Board.

Table 20 JTAG IN Connector



Pin Number	Top Row	Pin Number	Bottom Row
1	TMS	2	/TRST
3	TDI	4	GND
5	Presence Detect (+5V)	6	Key
7	TDO	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1
15	Key	16	Key
17	Key	18	Key
19	/CONFIG	20	/GRESET

Table 21 JTAG OUT Connector



Pin Number	Top Row	Pin Number	Bottom Row
1	TMS	2	/TRST
3	TDO	4	GND
5	SENSE	6	N/C
7	TDI	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1
15	Key	16	Key
17	Key	18	Key
19	/CONFIG	20	/GRESET

Appendix A: PLX PCI Implementation

The following values loaded into the PCI from EEPROM during power on and reset of the F5 Carrier Board.

Note: The PLX PCI does not support Direct Bus Mastering on the F5 Carrier Board. However, register settings for this function are shown for possible future PLX PCI-compatible chips.

Table 22 PLX PCI PCI9060 EEPROM Contents

Offset	Value	Register Notes
000h	00F512FB	Vendor ID =12FB (Spectrum Signal Processing Inc.) Device ID = 00F5
004h	06800000	Revision ID = 00 Class Code= =068000 60 = Bridge Device 80 = Other Bridge Device 00 = Interface
008h	00000109	Interrupt Line Routing Value= =09 Interrupt Pin = 01 Minimum Latency = 00 Maximum Latency = 00
00Ch	00000000	Mailbox 0
010h	00000000	Mailbox 1
014h	FF000000	Local Configuration Register PCI 00h, Local 80h Local Address Space 0 Range Register (bits 31:4) = FF00000 Prefetchable? (bit 3) = 0 (no prefetch) Location (bits 2:1) = 00 IO/Memory Map (bit 1) = 0 (memory map local address space 0)
018h	00000001	Offset 018 Local Configuration Register PCI 04h, Local 84h Space 0 Re-Map (bits 31:4) = 000000 Unused (bits 3:1) = 000 Space 0 Enable (bit 0) = 1
01Ch	00000000	Local Configuration Register PCI 08, Local 88h Reserved (bits 31:0) = 00000000 *(This register is different for PCI9080 see table below)*
020h	00000000	Local Configuration Register PCI 0Ch, Local 8Ch Reserved (bits 31:0) = 00000000 *(This register is different for PCI9080 see table below)*
024h	00000000	Local Configuration Register PCI 10h, Local 90h ROM Range (bits 31:11) = 00000000000000000000 binary Unused (bits 10:0) = 00000000000 binary

Table 22 PLX PCI PCI9060 EEPROM Contents

Offset	Value	Register Notes
028h	0000001F	Offset 028 Local Configuration Register PCI 14h, Local 94h Expansion ROM Re-map (bits 31:11) = 0 Not Used (bits 10:5) = 0 BREQo Enable (bit 4) = 1 BREQ Delay (bits 3:0) = F NOTE: Direct bus mastering not supported on F5 with PCI
02Ch	F0030143	Offset 02c Local Configuration Register PCI 18h, Local 98h PCI Target Retry Delay Clocks (bits 31:28) = 1111 binary Direct Slave PCI write mode (bit 27) = 0 binary Exp. ROM Burst Enable (bit 26) = 0 binary Not Used (bit 25) = 0 binary Mem Space 0 Burst Enable (bit 24) = 0 binary Exp. ROM Bterm Enable (bit 23) = 0 binary Exp. ROM RDY Enable (bit 22) = 0 binary Exp. ROM Wait States (bits 21:18) = 0000 binary Exp. ROM Width (bits 17:16) = 11 binary Not Used (bits 15:10) = 000000 binary Exp. ROM Prefetch Disable (bit 9) = 0 binary Mem Space 0 Prefetch Disable (bit 8) = 1 binary Mem Space 0 Bterm Enable (bit 7) = 0 binary Mem Space 0 RDY Enable (bit 6) = 1 binary Mem Space 0 Wait States (bits 5:2) = 0000 binary Mem Space 0 Width (bits 1:0) = 11 binary
030h	FF000000	Local Configuration Register PCI 1Ch, Local 9Ch Local Range Direct Master to PCI (bits 31:16) = FF00 Not Used (bits 15:0) = 0000
034h	FD000000	Local Configuration Register PCI 20h, Local A0h Local Base Address Register for Direct Master to PCI (bits 31:16) = fd00 Not Used (bits 15:0) = 0000
038h	E0000000	Local Configuration Register PCI 24h, Local A4h Local Base Address Register for Direct Master to PCI IO/CFG (bits 31:16) = e000 Not Used (bits 15:0) = 0000
03Ch	FD000001	Local Configuration Register PCI 28h, Local A8h Remap Local to PCI Space (bits 31:16) = fd00 (arbitrary value) Not Used (bits 15:8) = 0 Almost Full Flag (bits 7:5) = 000 binary Direct Master PCI Read Mode (bit 4) = 0 binary Direct Master Read Prefetch Size Control (bit 3) = 0 binary Lock Input Enable (bit 2) = 0 binary Direct Master I/O Access Enable (bit 1) = 0 binary Direct Master Memory Access Enable (bit 0) = 1 binary

Table 22 PLX PCI PCI9060 EEPROM Contents

Offset	Value	Register Notes
040h	00000000	Local Configuration Register PCI 2Ch, Local Ach Configuration Cycle Information (bits 31:0) = 00000000
044h	00000000	Unused
048h	00000000	Unused
04Ch	00000000	Unused
050h	00000000	Unused

Register values are the same for both the PCI9060 chipset and the PCI9080 chipset except those listed in the table below.

Table 23 PLX PCI PCI9080 EEPROM Contents

Offset	Value	Register Notes
01Ch	00000000	Local Configuration Register PCI 08, Local 88h PCI Rev. 2.1 Mode (bit 24) = 1 PCI Request Mode (bit 23) = 1 Local Bus Direct Slave Give up Bus Mode (bit 21) =1
020h	00000000	Local Configuration Register PCI 0Ch, Local 8Ch Reserved (bits 31:8) = 000000 Big/Little Endian Descriptor Register (bits7:0) 00000000