A Digital Signal Processing Approach to Analog-to-Digital Conversion

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I. Introduction

In modern time and frequency domain measurement systems, it is imperative that the ADC accurately estimates analog voltages that are supplied to it. In today's highly cluttered RF environment, signals of interest are constantly competing for available frequency bandwidth. An ADC that generates high-order, nonlinear errors such as harmonic and intermodulation distortion can introduce a whole host of spurious signals into a spectrum that can easily confuse system operators and various automatic screening algorithms. This is particularly true for devices designed to work the HF communications bands where the concentration of signals is very high. It is desirable to design the ADC sections of RF frequency monitoring systems with great care, as the capabilities of these systems will, to a large extent, depend heavily on the quality of the samples coming out of the ADC. This article focuss on a new technology for improving the linearity of ADCs targeted at a nominal sample rate of 10Msamples per second, often used in applications such as underwater & airborne acoustics, ELF/VLF/RF communications, SONAR, and RADAR/EW systems.

II. Error Sources

The primary error sources found in ADCs are listed in Figure-2. The cumulative effect of these errors often results in designs that yield digitized data with extraneous signals and an unfaithful estimation of the original analog signal, *x(t)*.

High-order distortion has always been the most difficult ADC error to deal with. High-order distortion is typically associated with nonlinear behavior of the digital circuitry in an ADC. *Harmonic* and *intermodulation*

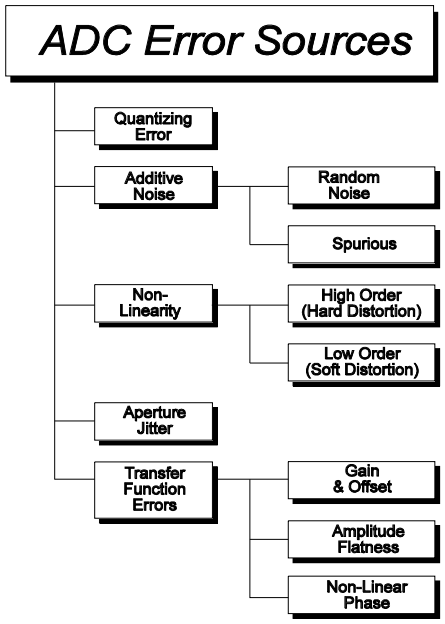

Figure-2. ADC Error Sources

distortion are typical manifestations of this kind of distortion. High-order distortion has the troubling characteristic of not diminishing as the signal level being presented to the ADC is reduced. This characteristic greatly reduces the effectiveness of notch filters and other frequency management devices that are used to reduce the levels of fixed, high amplitude signals that mix with lower level SOIs to produce a variety of intermod products. The intermod products can be so severe as to control the background noise of the measurement. Mercifully, harmonic distortion often falls outside of the measurement band, especially in narrowband monitoring systems.

III. High-order Distortion

In a high performance ADC, much of the high-order distortion can be traced to imperfections in the analog-to-digital transfer function. The transfer function of an ideal ADC with finite resolution is shown in Figure-3.

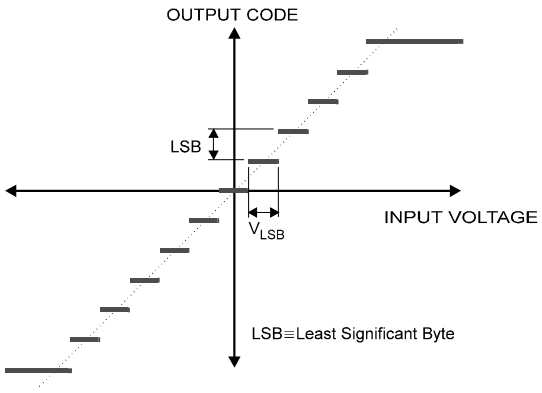

Figure-3. Ideal ADC transfer function.

A key characteristic of an "ideal" ADC with finite resolution is the uniform width of each "tread" of the "staircase". Crafting actual circuitry to implement this function is quite difficult. Manufacturing tolerances on the components used to build the circuits are such that the tread widths vary not only within each individual ADC, but between ADCs with the same part number.

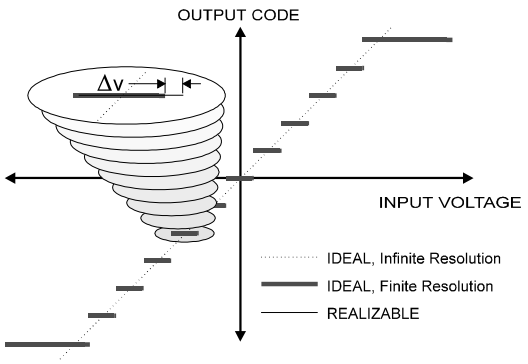

Figure-4. Quantizer differential nonlinearity.

The error associated with this irregularity in the ADC's transfer function is called a differential nonlinearity. The variations in the tread width Δv are fixed within the context of an individual ADC. Figure-4 shows the variation for just one of the treads; each tread will have a unique Δv. Once the ADC is built, the set of Δv's will be subject to the drift and aging specifications for the components in the part. Errors caused by nonlinear distortion are shown in Figure-5. The error voltage transfer function will have a random characteristic. It is important to note that this function can be curve fit using a very "high order" fitting function. In actual monitoring systems, implementing correction algorithms based on curve fitting would prove impractical because of the complexity of the resulting equations and the characteristic that each ADC would require a unique correction algorithm.

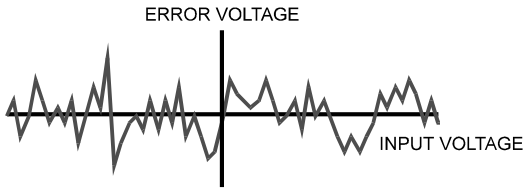

Figure-5. High-order error transfer function.

IV. High-order Distortion Reduction

A new approach towards reducing high-order distortion effects in ADCs is now possible due in part to the availability of custom, high-speed, signal processing-capable integrated circuits. When configured with appropriate correction algorithms, designs can be developed to do real-time error correction at speeds high enough to be useful in signal monitoring systems.

The process that was used to implement this approach began with a traditional, high-performance ADC design. Signal processing algorithms were added to calibrate out the nonlinear distortion.

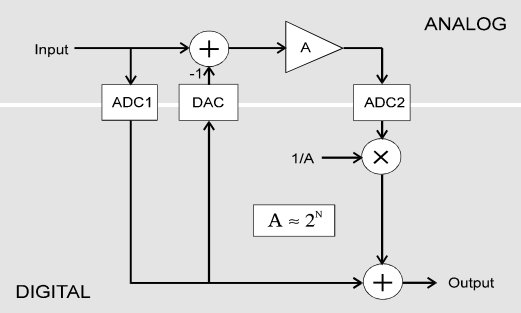

Figure-6. A subranging, 2-pass converter.

As shown in Figure-6, a subranging converter was used as the starting point for this investigation. A voltage supplied by an external track or sample and hold is estimated by ADC1, forming the most significant bits of the final output value. This estimate is then passed through a digital-to-analog converter (DAC) where it is subtracted from the original voltage. The residual is amplified by gain A, then estimated by a second converter, ADC2. After correction by the amount of gain used, the second estimate now represents the least-significant bits of the final output value. The first and second estimates are then combined to form a digital word representing the original input voltage. The number of bits used to represent the voltage has traditionally not exceeded 16 in high sample rate devices.

An error model can be formulated that clearly illustrates the tendency of this design to produce errors that are not zero-mean Gaussian in nature. As shown in Figure-7, if the amplifier gain A is not precisely calibrated out, nonlinear distortion errors from ADC1 and the DAC will contaminate the output word.

X - Input from track & hold
Y - Output sample
E_1 - ADC1 quantization error
E_2 - ADC2 quantization error
E_d - DAC error

$$Y = X + E_1(1 - A2^{-N}) + E_dA2^{-N} + E_22^{-N}$$

Figure-7. Subranging converter error model.

The investigation team for this effort decided to attack the error generation mechanisms by first designing an algorithm which was capable of exactly calibrating out the amplifier gain A. They then designed a second algorithm which would calibrate out the remaining DAC errors.

V. Statistical Gain Calibration

The algorithm used to calibrate out the amplifier gain A is essentially a control loop that adjusts the coefficient used to calibrate the amplifier gain on a sample-by-sample basis. The additional circuitry is shown in Figure-8. The idea is to inject a pseudorandom sequence into the residue path, and observe how the path (including the amplifier) modifies the sequence. A gain coefficient G, will always be set to whatever value is necessary to force perfect calibration.

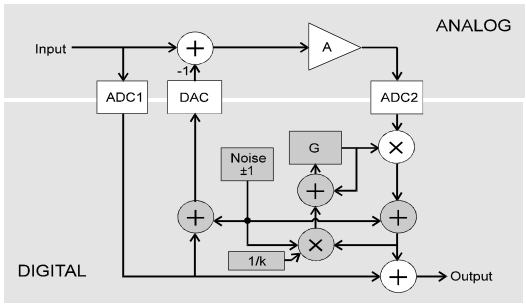

Figure-8. Amplifier gain calibration loop.

An examination of the loop equations in Figure-9 reveals that the new circuitry is capable of tracking changes in the amplifier gain on a sample-by-sample basis. As long as a physical circuit could be constructed to do the calculations fast enough, this looked like a very promising approach.

X_n - Input from track & hold
G_n - Gain value
N_n - Random ± 1 sequence
D_n - Output of ADC1
A - Residue amplifier gain

Closed-loop system tracks changes in residue amp gain!

$$G_\infty = \frac{1}{A}$$

$$G_{n+1} = G_n + \frac{N_n}{k}\,(AG_n(X_n - D_n - N_n) + N_n)$$

$$G_{n+1} = G_n + \frac{1}{k}(1 - AG_n) \quad \text{Difference equation}$$

$$G_n = \frac{1}{A} + \left(1 - \frac{A}{k}\right)^n \left(G_0 - \frac{1}{A}\right) \quad \text{Exponential Average}$$

Figure-9. Amplifier calibration loop equations and convergence.

A new error model is readily derivable and clearly shows the elimination of ADC1 errors. As shown in Figure-10, the new error model is still subject to DAC errors and ADC2 errors (Note: ADC2 errors are still reduced by the amplifier gain, A).

X_n - Input from track & hold
G_n - Gain value
N_n - Random ± 1 sequence
D_n - Output of ADC1
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Figure-10. Error model after residue amplifier gain calibration.

VI. DAC Calibration Loop

A similar approach was taken to reduce the errors caused by the DAC. Unfortunately, the complexity of the required circuitry increased dramatically. The loop equations required matrix and vector math operations to be run on a sample-by-sample basis. The DAC calibration loop is shown in Figure-11.

An interesting attribute of this loop is the addition of two additional DACs and two additional pseudorandom noise generators. The noise generators in this loop and in the gain calibration loops were configured to emit sequences of {-1,1} instead of {0,1}. This was done to simplify the math and the resulting circuitry.

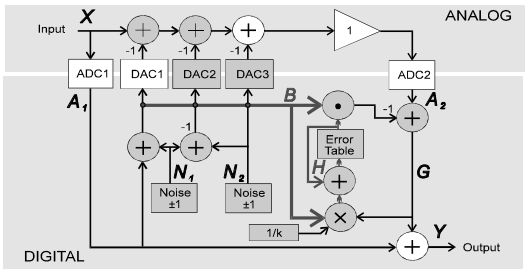

Figure-11. DAC calibration loop.

The loop equations are shown in Figure-12. Convergence of the equations convinced the investigation team that it was possible to calibrate out the DAC errors.

B - Vector of DAC bit line states
b_n - MSB of DAC1
C - Vector with DAC bit weights w/errors
H - Vector with corrections for DAC bit errors
W - Vector, Expected Value($C + H_n$)
D - Vector, Expected Value($B_n b_n$)
F - Matrix, Expected Value($B_n B_n^T$)

Closed-loop system tracks and cancels DAC bit current errors!

$$W_\infty = -F^{-1}D$$

$$G_n = X - b_n - B_n \bullet C + B_n \bullet H_n$$

$$H_{n+1} = H_n + \frac{B_n}{k}(X - b_n - B_n^T(C + H_n))$$

$$W_n = -F_{-1}D + (I - \frac{1}{k}F)^n(W_0 + F^{-1}D)$$

Figure-12. DAC calibration loop equations and convergence.

The net effect of the calibration loop is to force the DAC error E_d, to converge to zero. A quick examination of the error model shown in Figure-10 with a zero substituted in for E_d shows that the error model now is dependent only upon ADC2 errors. The noise generator circuits provide approximately 1/2 scale dither at the input of ADC2, which causes quantization errors to become small even for relatively inexpensive ADC2 parts. Figure-13 illustrates the final error model for the circuit.

$$Y_n = X_n + noise_n$$

Figure-13. Final error model for the enhanced 2-pass ADC.

The enhanced 2-pass ADC mathematically was able to make a dramatic advancement in the state-of-the-art in ADC design. The challenge left was to actually build one.

revealed that none existed that could do the massive amount of processing required to implement these correction loops at the speeds required. A compounding factor was cost. This investigation was tasked to develop a commercially viable ADC system, not a one-of-a-kind research project.

VII. ABACUS

A close examination of available off-the-shelf digital signal processing chips
With these thoughts in mind, the investigation team decided to build an *application specific integrated circuit* (ASIC) to implement as much of the correction loop circuitry as possible.

The chip is capable of performing more than 1.5 billion math operations per second, and was designed to be operated at conversion rates up to 25 million samples-per-second (MSPS). The ASIC was built into a 144-pin surface mount package.

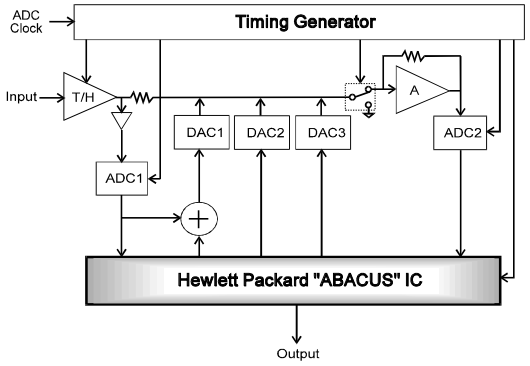

Figure-14. Enhanced 2-pass ADC.

The ASIC, code named ABACUS by the investigation team, is capable of handling ADC1s of up to 9 bits and ADC2s of up to
12 bits. Each output sample of ABACUS has 23 bits of resolution. This far exceeds the maximum number of raw bits available in preceding devices. The final configuration of the enhanced ADC is shown in Figure-14.

IX. Summary

This article has described the approach taken to create a continuously-calibrating ADC system based on the real-time signal processing of each digitized data point. The hardware implementation of this approach (see Figure-15) has been able to achieve
18-bits of linearity with 23-bits of resolution. High-order distortion higher than -110dBfs is converted into low order distortion. These performance figures are for the entire "front end", which includes signal conditioning, alias filtering, the ADC, zoom and decimation filtering. The current VXI module has a maximum sample rate of 10.24MSPS and an information bandwidth of 4MHz. An investigation in under way into the design of a second VXI module that would maintain or improve upon all of the E1430A's specifications and would have double the sample rate and bandwidth.

Figure-18 shows a 2-tone intermodulation distortion measurement made with the E1430A. The spectrum shown was measured with an input range of +4dBm, a baseband frequency

span of 4MHz, 50 rms averages, a Hanning window and a 32ksample FFT yielding 12800 lines of resolution. The frequency bandwidth was 312.5Hz. The only measureable intermod product was more than 90dB below the amplitude of either of the test tones. A small signal visible at 269.7kHz came from the test signal generator.

Figure-18. 2-Tone intermodulation distortion test using the E1430A enhanced ADC.

X. Acknowledgments

This paper is a compendium of information drawn from several papers and articles written by the team leader and principal investigator for the project, Howard Hilton. Howard and his team at Hewlett-Parkard's Lake Stevens Division in the state of Washington spent countless hours running simulations and verifications on the design. His unique insight into the signal processing required to produce ABACUS guaranteed that the project would be successful.

XI. References

1. Howard E. Hilton,"A 10-Megasample-per-Second Analog-to-Digital Converter with Filter and Memory", *Hewlett-Packard Journal, Vol. 44, no. 5, October 1993, pp. 100-104.*

2. Howard E. Hilton,"A 10-MHz Analog-to-Digital Converter with 110-dB Linearity", *Hewlett-Packard Journal, Vol. 44, no. 5, October 1993, pp. 105-112.*

3. *Statistically Based Continuous Autocalibration Method and Apparatus, U.S. Patent 4,996,530, United States Patent Office, February 1991.*

4. S.R. Broadstone, *"Summary of the Hewlett-Packard E1430A ADC Performance Tests", Lincoln Laboratory, Massachusetts Institute of Technology, 17 March 1994.*

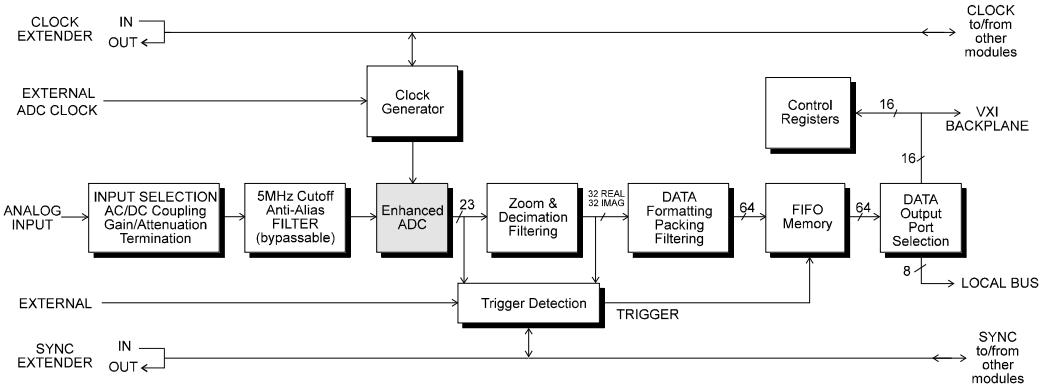

Figure-15. Enhanced ADC-based VXI module w/23-bits of resolution.