HEWLETT PACKARD

# HP E6500A
# VXI Tuner

Users Guide

HP part number: E6500-90013
Printed in USA
October 1999

Revision 1.0

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# What You'll Find in This Manual…

### HP E6500A System-Level Information

**Chapter 1**

- Getting Started
  - System and module descriptions
  - System configurations and cabling
  - System accessories
  - Preparation for use

**Chapter 2**

- Using the Driver
  - Driver information
  - Source code information

**Chapter 3**

- Theory of Operation
  - Theory of operation
  - System tuning equations
  - System block diagram

**Chapter 4**

- Register-Based Programming
  - Module EEPROM information
  - Register functions
  - Register control illustrations

**Chapter 5**

- Specifications
  - System specifications

# Warranty

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# Safety and Regulatory Information

Review this product and related documentation to familiarize yourself with safety markings and instructions before you operate the instrument. This product has been designed and tested in accordance with international standards.

**WARNING**

**The WARNING notice denotes a hazard. It calls attention to a procedure, practice, or the like, that, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.**

**CAUTION**

The **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

## Instrument Markings

| | |
|---|---|
|  | When you see this symbol on your instrument, you should refer to the instrument's instruction manual for important information. |
|  | This symbol indicates hazardous voltages. |
|  | The laser radiation symbol is marked on products that have a laser output. |
|  | This symbol indicates that the instrument requires alternating current (ac) input. |
|  | The CE mark is a registered trademark of the European Community. If it is accompanied by a year, it indicates the year the design was proven. |
|  | The CSA mark is a registered trademark of the Canadian Standards Association. |
| 1SM1-A | This text indicates that the instrument is an Industrial Scientific and Medical Group 1 Class A product (CISPER 11, Clause 4). |
|  | This symbol indicates that the power line switch is ON. |
|  | This symbol indicates that the power line switch is OFF or in STANDBY position. |

## Safety Earth Ground

This is a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and secured against any unintended operation.

## Before Applying Power

Verify that the product is configured to match the available main power source as described in the input power configuration instructions in this manual. If this product is to be powered by autotransformer, make sure the common terminal is connected to the neutral (grounded) side of the ac power supply.

# DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

| | |
|---|---|
| **Manufacturer's Name:** | Hewlett-Packard Co. |
| **Manufacturer's Address:** | Santa Rosa Systems Division<br>1400 Fountaingrove Parkway<br>Santa Rosa, CA 95403-1799<br>USA |

declares that the products

| | |
|---|---|
| **Product Names:** | 20 MHz to 1000 MHz VXI Tuner,<br>Downconverter VXI module,<br>Local Oscillator VXI module,<br>Block Downconverter VXI module |
| **Model Numbers:** | HP E6500A, HP E6401A, HP E6402A,<br>HP E6403A |
| **Product Options:** | This declaration covers all options of the above products. |

conform to the following Product specifications:

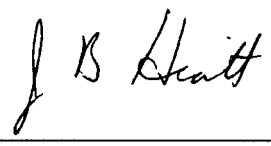
Safety: IEC 1010-1:1990+A1 / EN 61010-1:1993
CAN/CSA-C22.2 No. 1010.1-92

EMC: CISPR 11:1990/EN 55011:1991 Group 1, Class A
IEC 801-2:1984/EN 50082-1:1992 4 kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1:1992 3 V/m, 27-500 MHz
IEC 801-4:1988/EN 50082-1:1992 0.5 kV Sig. Lines, 1 kV Power Lines

**Supplementary Information:**
The products herewith comply with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and are marked accordingly.

The HP E6500A consists of HP E6401A, HP E6402A and HP E6403A modules. The system was tested in an HP E1401B mainframe.

Santa Rosa, California, USA 30 Oct. 1996



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European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH, Department HQ-TRE, Herrenberger Strasse 130, D-71034 Böblingen, Germany (FAX +49-7031-14-3143)

# Typeface Conventions

*Italics*

- Used to emphasize important information:
  Use this software *only* with the HP xxxxxX system.
- Used for the title of a publication:
  Refer to the *HP xxxxxX System-Level User's Guide*.
- Used to indicate a variable:
  Type `LOAD BIN` *filename.*

**`Instrument Display`**

- Used to show on-screen prompts and messages that you will see on the display of an instrument:
  The HP xxxxxX will display the message **`CAL1 SAVED`**.

**[Keycap]**

- Used for labeled keys on the front panel of an instrument or on a computer keyboard:
  Press **[Return]**.

***{Softkey}***

- Used for simulated keys that appear on an instrument display:
  Press ***{Prior Menu}***.

`User Entry`

- Used to indicate text that you will enter using the computer keyboard; text shown in this typeface must be typed *exactly* as printed:
  Type `LOAD PARMFILE`
- Used for examples of programming code:

```
#endif // ifndef NO_CLASS
```

*`Path Name`*

- Used for a subdirectory name or file path:
  Edit the file *`usr/local/bin/sample.txt`*

**Computer Display**

- Used to show messages, prompts, and window labels that appear on a computer monitor:
  The **Edit Parameters** window will appear on the screen.
- Used for menus, lists, dialog boxes, and button boxes on a computer monitor from which you make selections using the mouse or keyboard:
  Double-click **EXIT** to quit the program.

# Contents


Notice . . . . . ii
What You'll Find in This Manual. . . . . iii
Warranty . . . . . iv
Certification . . . . . iv
Warranty . . . . . iv
Assistance . . . . . v
Service and Support . . . . . vi
Safety and Regulatory Information . . . . . vii
Safety Earth Ground . . . . . viii
Before Applying Power . . . . . viii
Typeface Conventions . . . . . x

**1. Getting Started**

Introducing the HP E6500A VXI Tuner System . . . . . 1-1
Initial Inspection . . . . . 1-2
HP E6500A VXI Tuner System Module Front-Panel Features . . . . . 1-3
HP E6401A 20–1000 MHz Downconverter . . . . . 1-4
*Figure 1-1. HP E6401A 20–1000 MHz Downconverter Module* . . . 1-5
HP E6401A Option 001 20–1000 MHz Downconverter with Baseband Output . . . . . 1-6
*Figure 1-2. HP E6401A Option 001 20–1000 MHz Downconverter with Baseband Output Module* . . . . . 1-7
HP E6402A Local Oscillator . . . . . 1-8
*Figure 1-3. HP E6402A Local Oscillator Module* . . . . . 1-9
HP E6402A Option 002 Local Oscillator with Dual Outputs . . . . . 1-10
*Figure 1-4. HP E6402A Option 002 Local Oscillator with Dual Outputs Module* . . . . . 1-11
HP E6403A 1000–3000 MHz Block Downconverter . . . . . 1-12
*Figure 1-5. HP E6403A 1000–3000 MHz Block Downconverter Module* 1-13
Typical Tuner System Configurations . . . . . 1-14
HP E6500A Tuner System and System Options . . . . . 1-14
HP E6500A Mainframe Options . . . . . 1-14
HP E6500A . . . . . 1-15
*Figure 1-6. HP E6500A System Configuration* . . . . . 1-15
HP E6500A Option 001 . . . . . 1-16
*Figure 1-7. HP E6500A Option 001 System Configuration* . . . . . 1-16
HP E6500A Option 003 . . . . . 1-17
*Figure 1-8. HP E6500A Option 003 System Configuration* . . . . . 1-17
HP E6500A Option 001, 003 . . . . . 1-18
*Figure 1-9. HP E6500A Option 001, 003 System Configuration* . . 1-18

*Figure 1-10. HP E3238S System with HP E6500A Option 001, 003 Configuration* . . . . . 1-19
HP E6500A Option 006 . . . . . 1-20
*Figure 1-11. HP E6500A Option 006 System with Mainframe Configuration* . . . . . 1-20
HP E6500A Option 013 . . . . . 1-21
*Figure 1-12. HP E6500A Option 013 System with Mainframe Configuration* . . . . . 1-21
Accessories Supplied . . . . . 1-22
*Table 1-1. HP E6401A 20–1000 MHz Downconverter Accessories* 1-22
*Table 1-2. HP E6401A Option 001 20–1000 MHz Downconverter Accessories* . . . . . 1-22
*Table 1-3. HP E6402A Local Oscillator Accessories* . . . . . 1-22
*Table 1-4. HP E6402A Option 002 Local Oscillator Accessories* . 1-22
*Table 1-5. HP E6403A 1000–3000 MHz Block Downconverter Accessories* . . . . . 1-22
Electrostatic Discharge . . . . . 1-23
Preparing a Static-Safe Work Station . . . . . 1-23
*Figure 1-13. Example of a Static-Safe Work Station* . . . . . 1-23
Reducing ESD Damage . . . . . 1-24
*Table 1-6. Static-Safe Accessories* . . . . . 1-24
Preparation for Use . . . . . 1-25
Setting the Logical Address Switches . . . . . 1-26
*Table 1-7. Address Settings* . . . . . 1-26
*Figure 1-14. HP 640xA Side Cover with Logical Address Switch Location and Address Switch Configurations for each Model of Module* . . . . . 1-27
Installing the Tuner . . . . . 1-28
Cabling the Tuner . . . . . 1-28
HP E6500A Operator's Check . . . . . 1-29
*Table 1-8. Test Equipment Needed* . . . . . 1-29
Procedure . . . . . 1-29
*Table 1-9. Frequency Points Measured for Operator's Check Procedure* 1-30

**2. Using the Driver and Demonstration GUI**

About the Driver . . . . . 2-1
*Figure 2-1. HP E6500A Source and Header Files* . . . . . 2-1
Driver Functions . . . . . 2-3
Configuration and Initialization . . . . . 2-3
. . . . . Common Use Functions 2-5
Miscellaneous Functions . . . . . 2-7
VXIplug&play Required Functions . . . . . 2-8
Error Codes . . . . . 2-10
Using the Demonstration GUI . . . . . 2-12
*Figure 2-2. Configuration Form Window* . . . . . 2-12
*Figure 2-3. Error Message Window Example* . . . . . 2-13

*Figure 2-4. Driver Errors Window Example* . . . . . 2-14
*Figure 2-5. Shared LO Box Configuration Window* . . . . . 2-15
*Figure 2-6. Operational Tuner GUI Window* . . . . . 2-16
*Figure 2-7. Operational Tuner (Shared LO) GUI Window* . . . . . 2-17
Demonstration GUI Controls . . . . . 2-18
General . . . . . 2-18
Frequency . . . . . 2-18
Step Size . . . . . 2-18
Input Attenuation . . . . . 2-18
10 MHz Ref . . . . . 2-18
IF Output Freq . . . . . 2-18
Preset . . . . . 2-19
Temp . . . . . 2-19
Tuner Active . . . . . 2-19
Shared LO . . . . . 2-19
Driver Revision . . . . . 2-19
Reset All . . . . . 2-19
Close . . . . . 2-19

**3. HP E6500A VXI Tuner System Description**

Tuning an HP E6500A System . . . . . 3-2
Tuning Equations . . . . . 3-2
Definition of Terms . . . . . 3-3
Preselector Bands . . . . . 3-5
*Table 3-1. HP E6500A Preselector Bands* . . . . . 3-5
Calibration Factors . . . . . 3-5
Optimizing Dynamic Range . . . . . 3-5
HP E6401A 20 to 1000 MHz Downconverter Operation . . . . . 3-7
Functions . . . . . 3-7
Description . . . . . 3-7
HP E6401A Option 001 Module . . . . . 3-8
Inputs and Outputs . . . . . 3-9
HP E6402A Local Oscillator Operation . . . . . 3-10
Functions . . . . . 3-10
Description . . . . . 3-10
HP E6402A Option 002 Module . . . . . 3-12
Inputs and Outputs . . . . . 3-12
HP E6403A 1000 to 3000 MHz Block Downconverter Operation . . . . 3-13
Functions . . . . . 3-13
Description . . . . . 3-13
*Table 3-2. Frequency Translations* . . . . . 3-14
Inputs and Outputs . . . . . 3-14

**4. Register-Based Programming**

Addressing the Registers . . . . . 4-2
*Figure 4-1. Registers within A16 Address Space* . . . . . 4-2
*Figure 4-2. Registers within HP E1406A A16 Address Space* . . . . . 4-3
Base Address . . . . . 4-3

Address Space Outside the Command Module . . . . . 4-3
Address Space Inside the Command Module . . . . . 4-4
Register Offset . . . . . 4-4
HP E6500A System Initialization . . . . . 4-5
Initialization Procedure . . . . . 4-5
Overview of the Registers . . . . . 4-6
Conventions . . . . . 4-6
Reading and Writing to the Registers . . . . . 4-6
Registers Common to Most VXI Modules . . . . . 4-7
*Table 4-1. Manufacturer's Identification Register* . . . . . 4-7
*Table 4-2. Device Identification Register* . . . . . 4-7
*Table 4-3. Status Register* . . . . . 4-7
Registers Specific to the HP E6500A Tuner . . . . . 4-8
*Table 4-4. HP E6500A Tuner Systems' Registers* . . . . . 4-8
Using the HP E6500A EEPROM Data . . . . . 4-9
*Table 4-5. Information Stored in Each EEPROM* . . . . . 4-9
Reading from the EEPROMs . . . . . 4-9
*Table 4-6. EEPROM Control Lines* . . . . . 4-9
*Table 4-7. Clock Cycles Needed to Retrieve Data from the EEPROM* . 4-10
*Table 4-8. Module Specific EEPROM Control Line to Register Mapping* 4-10
Data Stored in the Serial EEPROMS . . . . . 4-11
*Table 4-9. Format for HP E6401A, HP E6402A, and HP E6403A EEPROM Data* . . . . . 4-12
*Table 4-10. HP E6402A EEPROM Address and Data Sequence* . . 4-13
*Table 4-11. Example Data Read Sequence Starting at Address 0* . 4-14
HP E6401A 20 to 1000 MHz Downconverter Module Registers and Functions . . . . . 4-15
Controlling the HP E6401A Downconverter . . . . . 4-15
*Table 4-12. HP E6401A Control Interface Registers and Functions* . . . 4-17
Programming the Serial-to-Parallel Converter . . . . . 4-18
*Table 4-13. Serial-to-Parallel Settings Controlled By Register 38 Bit 7* 4-18
*Table 4-14. Optimum Settings for Unused Paths* . . . . . 4-18
HP E6402A Local Oscillator Module Registers and Functions . . . . . 4-19
Initializing and Controlling the HP E6402A LO Module . . . . . 4-19
*Table 4-15. HP E6402A Serial Data Input Using Parallel-to-Serial Conversion* . . . . . 4-20
*Table 4-16. HP E6402A Programming Sequence Example* . . . . . 4-21
*Table 4-17. Setting the VCO1 Bias and the Internal 10 MHz Reference Offset* . . . . . 4-22
*Table 4-18. HP E6402A VCO1 Programming Sequence Example* 4-22
*Table 4-19. HP E6402A Control Interface Registers and Functions* . . . 4-23

HP E6403A 1000 to 3000 MHz Block Downconverter Module Registers and Functions . . . . . 4-24
Controlling the HP E6403A Block Downconverter . . . . . 4-24
*Table 4-20. HP E6403A Register and HP E6401A Serial-to-Parallel Converter Settings* . . . . . 4-25
*Table 4-21. HP E6403A Attenuator Settings* . . . . . 4-25
*Table 4-22. HP E6403A Control Interface Registers and Functions* . . . 4-27
Changing the Tuned Frequency . . . . . 4-28
10 MHz Internal Reference Timebase Adjustment . . . . . 4-29
Adjustment Procedure . . . . . 4-29
*Figure 4-3. Register Control of the HP E6401A 20 to 1000 MHz Downconverter Module* . . . . . 4-31
*Figure 4-4. Register Control of the HP E6402A Local Oscillator Module and the HP E6401A Mixing Path* . . . . . 4-33
*Figure 4-5. Register Control of the HP E6403A 1000 - 3000 MHz Block Downconverter Module* . . . . . 4-35

**5. Specifications**

Definition of Terms . . . . . 5-1
Frequency-Related Specifications . . . . . 5-2
Amplitude-Related Specifications . . . . . 5-3
Physical Characteristics . . . . . 5-5
*Figure 5-1. Dimensions of the HP E640xA Modules Comprising the HP E6500A VXI Tuner System* . . . . . 5-6
General Information . . . . . 5-7
Environmental Information . . . . . 5-8
VXI Information . . . . . 5-9

# 1 Getting Started

## Introducing the HP E6500A VXI Tuner System

The HP E6500A VXI tuner system provides high dynamic range downconversion to a fixed-bandwidth intermediate frequency (IF) output. The tuner is implemented in the VXI platform to provide the flexibility needed to address different system requirements. The basic HP E6500A tuner systems described in this manual consist of two to three C-size modules, each with a register-based interface.

The following basic HP E6500A VXI tuner system configurations are covered in this manual. The standard HP E6500A tuner system consists of an HP E6401A 20–1000 MHz downconverter module and an HP E6402A local oscillator (LO) module. This configuration provides 20 to 1000 MHz of specified input frequency coverage and is tunable down to 2 MHz. The HP E6401A translates the input signal to a 21.4 MHz IF output signal. The HP E6402A provides the LO signals to the HP E6401A module.

The HP E6500A Option 001 tuner system is similar to the standard HP E6500A except that it uses an HP E6401A Option 001 module in place of the HP E6401A to provide a baseband output from approximately 2.5 to 9.5 MHz.

The HP E6500A Option 003 tuner system extends the input frequency range of the HP E6500A system to provide continuous frequency coverage from 20 to 3000 MHz with the addition of an HP E6403A 1000–3000 MHz block downconverter module. The HP E6403A translates the 1000 to 3000 MHz range, in four preselector bands, into the frequency range of the HP E6401A 20–1000 MHz downconverter module. The HP E6402A provides the block downconverter LO signal to the HP E6403A module.

The HP E6500A Option 001, 003 tuner system combines the 20 to 3000 MHz input frequency capability of the HP E6500A Option 003 system with the baseband output capability of the HP E6500A Option 001 system.

Controlling the tuner requires a controller card, MXI card or an embedded VXI computer in slot zero of the VXI mainframe and software to control the registers. A driver and a demonstration GUI are included with this product that enable the user to control the tuner with high-level commands rather than programming individual registers.

# Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, keep it until you have verified that the contents are complete and you have tested the module(s) mechanically and electrically.

Table 1-1 through Table 1-5 contain the accessories shipped with each module. If the contents are incomplete or if the modules do not pass the "HP E6500A Operator's Check" procedure found at the end of this chapter, notify the nearest Hewlett-Packard Support and Service office. A listing of Hewlett-Packard Support and Service offices is located at the front of this manual. If the shipping container is damaged or the cushioning material shows signs of stress, also notify the carrier. Keep the shipping materials for inspection by the carrier. The HP office will arrange for repair or replacement without waiting for a claim settlement.

If the shipping materials are in good condition, retain them for possible future use. You may wish to ship the module(s) to another location or return it to Hewlett-Packard for service.

# HP E6500A VXI Tuner System Module Front-Panel Features

In this section, the front-panel features will be described for each of the five modules used to create, in combinations of two to three modules, the four basic system configurations described in this manual. An illustration of each module and its position in a basic tuner system is included. The modules are:

- HP E6401A 20–1000 MHz Downconverter
- HP E6401A Option 001 20–1000 MHz Downconverter with Baseband Output
- HP E6402A Local Oscillator
- HP E6402A Option 002 Local Oscillator with Dual LO Outputs
- HP E6403A 1000–3000 MHz Block Downconverter

# HP E6401A 20–1000 MHz Downconverter

**Access** LED flashes whenever the module is being accessed via the VXI backplane.

**21.4 MHz IF Output** is the tuner output signal port. The output has approximately +5 dB of gain when the correction table is used.

**2nd LO Input** is the port for the HP E6402A 2nd LO output signal of approximately 1200 MHz.

**1st LO Input** is the port for the HP E6402A 1st LO output signal that ranges from approximately 1241.4 to 2221.4 MHz.

**Block Downconv Input** is the port for the HP E6403A block downconverter output signal that ranges, in bands, from approximately 250 to 900 MHz (when the HP E6403A is present).

**20–1000 MHz Input** is the port for the HP E6403A 20–1000 MHz output signal (when the HP E6403A is present), or for an antenna (when the HP E6403A is not present).

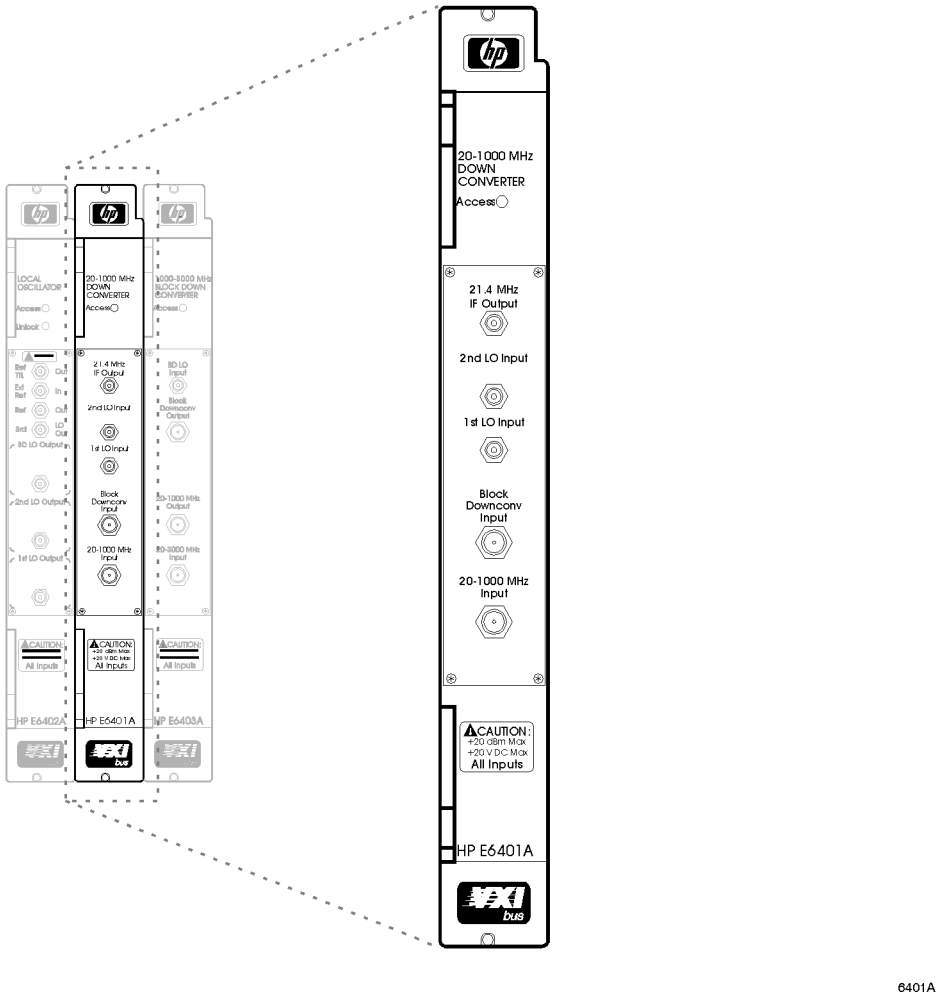


***Figure 1-1 HP E6401A 20–1000 MHz Downconverter Module***

## HP E6401A Option 001 20–1000 MHz Downconverter with Baseband Output

**IF Output** is the tuner output signal port. Its signal ranges from approximately 2.5 to 9.5 MHz and has approximately +15 dB of gain when the correction table is used.

**3rd LO Input** is the port for the HP E6402A 3rd LO output signal of 30 MHz.

**Access** LED flashes whenever the module is being accessed via the VXI backplane.

**2nd LO Input** is the port for the HP E6402A 2nd LO output signal of approximately 1200 MHz.

**1st LO Input** is the port for the HP E6402A 1st LO output signal that ranges from approximately 1241.4 to 2221.4 MHz.

**Blk Downconv Input** is the port for the HP E6403A block downconverter output signal that ranges, in bands, from approximately 250 to 900 MHz (when the HP E6403A is present).

**20–1000 MHz Input** is the port for the HP E6403A 20–1000 MHz output signal (when the HP E6403A is present), or for an antenna (when the HP E6403A is not present).

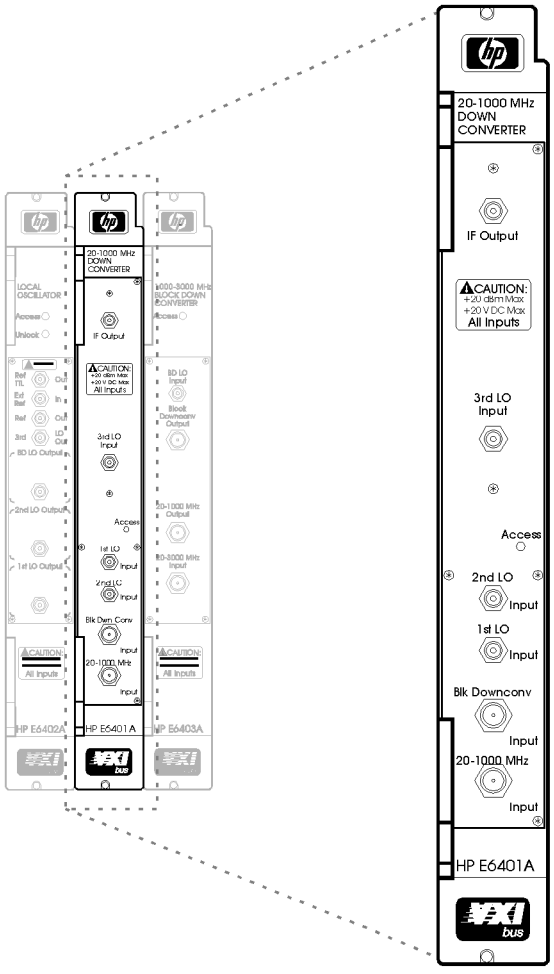


***Figure 1-2 HP E6401A Option 001 20–1000 MHz Downconverter with Baseband Output Module***

## HP E6402A Local Oscillator

**Access** LED flashes whenever the module is being accessed via the VXI backplane.

**Unlock** LED lights when the 1st LO or 2nd LO is unlocked.

**Ref TTL Out** is the port for the reference 10 MHz TTL-level output signal.

**Ext Ref In** is the port for the external reference 10 MHz input signal (if used).

**Ref Out** is the port for the reference 10 MHz output signal.

**3rd LO Out** is the port for the 30 MHz signal going to the HP E6401A Option 001 3rd LO Input port (when the HP E6401A Option 001 is present).

**BD LO Output** is the port for the signal of approximately 1200 MHz going to the HP E6403A BD LO Input port (when the HP E6403A is present).

**2nd LO Output** is the port for the signal of approximately 1200 MHz going to the HP E6401A 2nd LO Input port.

**1st LO Output** is the port for the signal that ranges from approximately 1241.4 to 2221.4 MHz going to the HP E6401A 1st LO Input port.

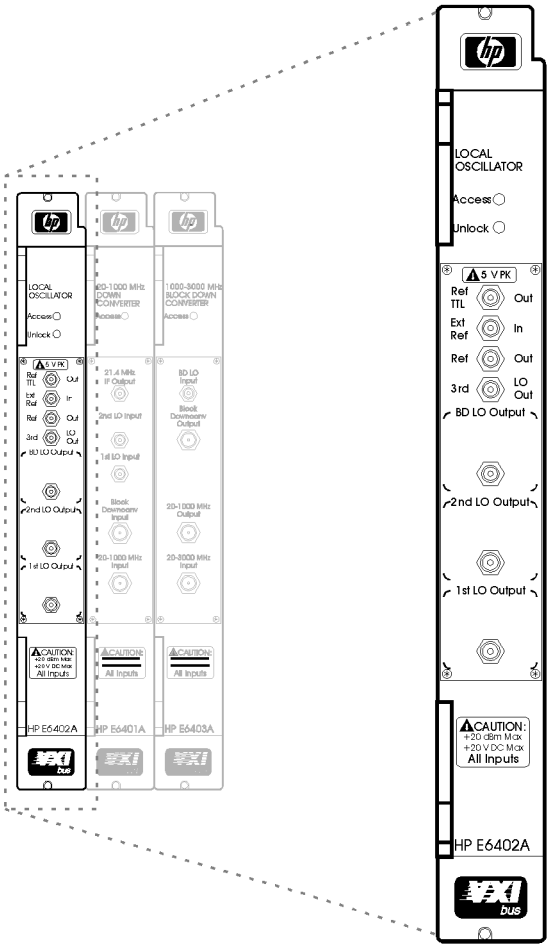


***Figure 1-3 HP E6402A Local Oscillator Module***

## HP E6402A Option 002 Local Oscillator with Dual Outputs

**Access** LED flashes whenever the module is being accessed via the VXI backplane.

**Unlock** LED lights when the 1st LO or 2nd LO is unlocked.

**Ref TTL Out** is the port for the reference 10 MHz TTL-level output signal.

**Ext Ref In** is the port for the external reference 10 MHz input signal (if used).

**Ref Out** is the port for the reference 10 MHz output signal.

**3rd LO Out** is the port for the 30 MHz signal going to the HP E6401A Option 001 3rd LO Input port (when the HP E6401A Option 001 is present).

**BD LO Output** are the ports (2) for the signal of approximately 1200 MHz going to the HP E6403A BD LO Input port (when the HP E6403A is present).

**2nd LO Output** are the ports (2) for the signal of approximately 1200 MHz going to the HP E6401A 2nd LO Input port.

**1st LO Output** are the ports (2) for the signal that ranges from approximately 1241.4 to 2221.4 MHz going to the HP E6401A 1st LO Input port.

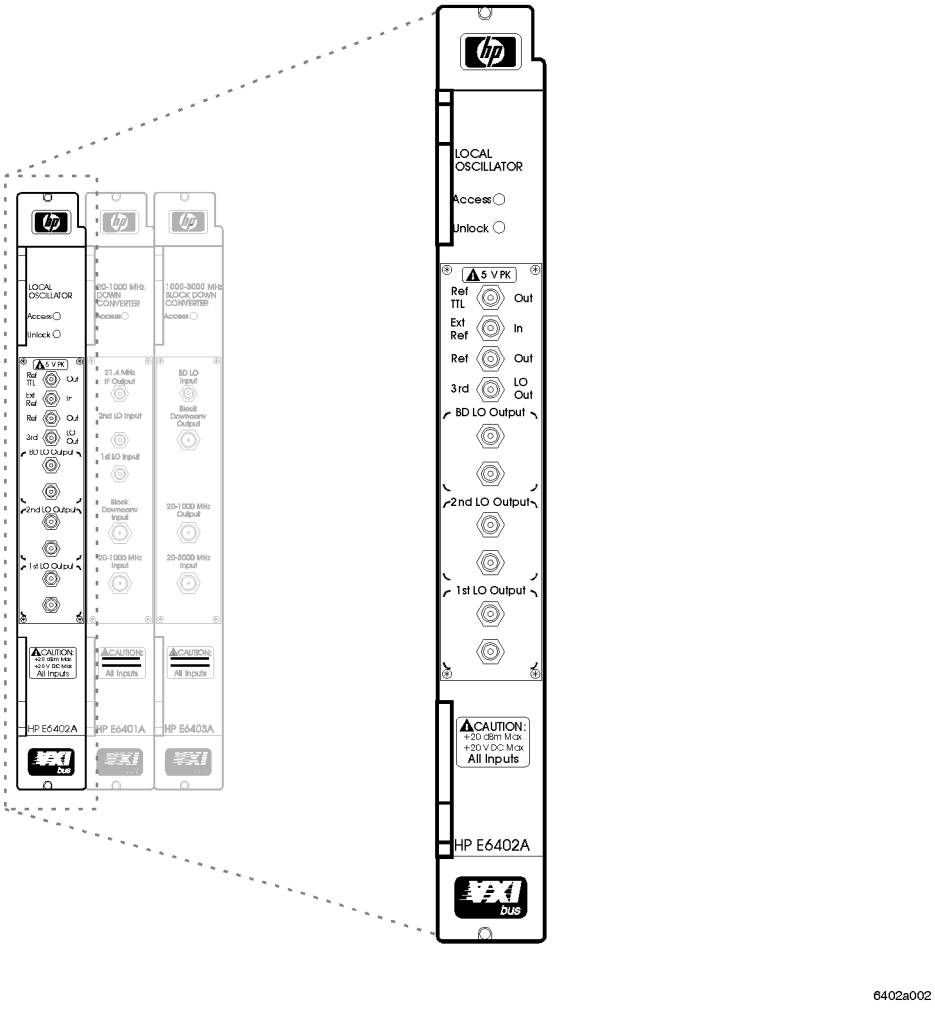


***Figure 1-4 HP E6402A Option 002 Local Oscillator with Dual Outputs Module***

## HP E6403A 1000–3000 MHz Block Downconverter

**Access** LED flashes whenever the module is being accessed via the VXI backplane.

**BD LO Input** is the port for the HP E6402A block downconverter LO output signal of approximately 1200 MHz.

**Block Downconv Output** is the port for the signal that ranges in bands from approximately 250 to 900 MHz going to the HP E6401A Block Downconv Input port.

**20–1000 MHz Output** is the port for the signal going to the HP E6401A 20–1000 MHz Input port.

**20–3000 MHz Input** is the port for the signal from an antenna.

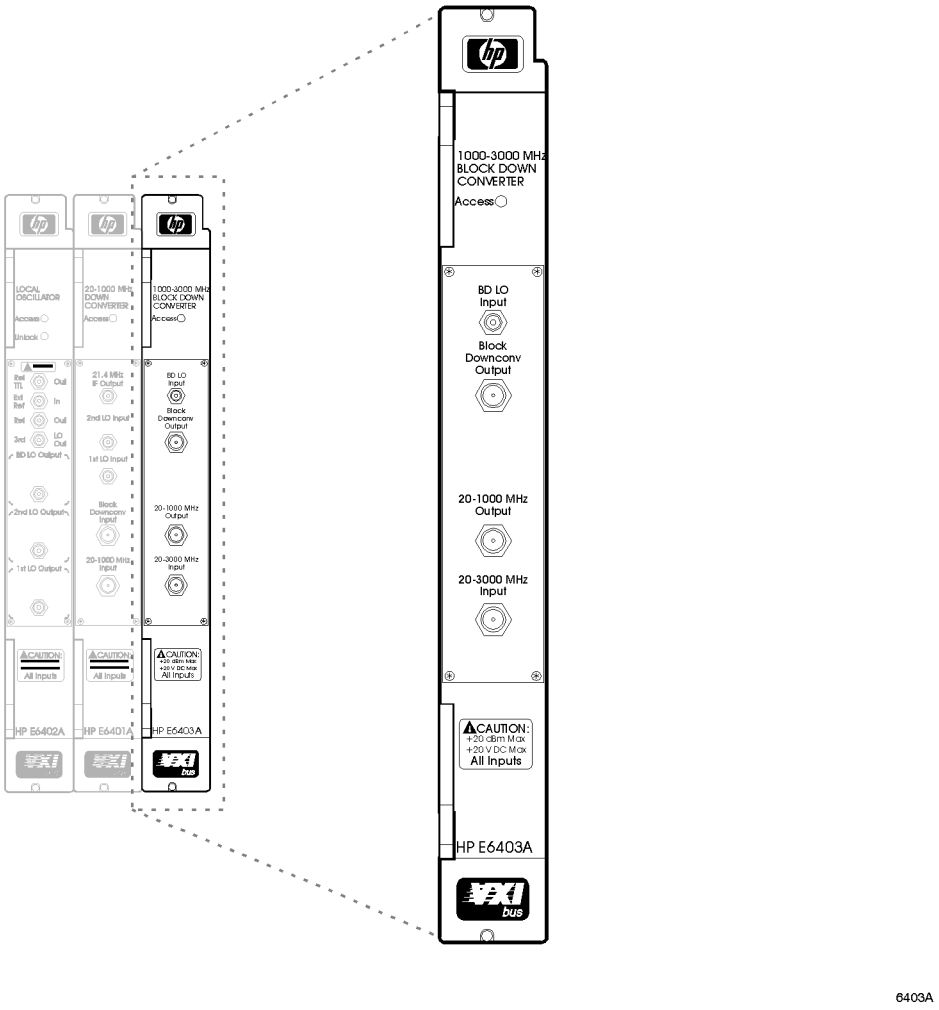


***Figure 1-5 HP E6403A 1000–3000 MHz Block Downconverter Module***

# Typical Tuner System Configurations

In this section, a front-panel illustration and brief description is given for each of the four basic tuner systems and the two mainframe options described in this manual. Also included is an illustration of an HP E6500A tuner used in an HP E3238S signals development system. Each front panel illustration depicts the module position in the system, the system cabling configuration, and the cable part numbers. The HP E6500A VXI tuner and system options are listed below:

## HP E6500A Tuner System and System Options

- HP E6500A
- HP E6500A Option 001
- HP E6500A Option 003
- HP E6500A Option 001, 003

### HP E3238S Example Application

- HP E3238S signals development system using an HP E6500A Option 001, 003

## HP E6500A Mainframe Options

- HP E6500A Option 006
- HP E6500A Option 013

**NOTE**

- Systems will *not* arrive cabled.
- HP E6500A mainframe options 006 and 013 may be configured with any of the system options listed above. The mainframes are illustrated with the standard HP E6500A system.

## HP E6500A

The HP E6500A tuner consists of two single-slot C-size VXI modules: the HP E6401A 20–1000 MHz downconverter and the HP E6402A local oscillator.

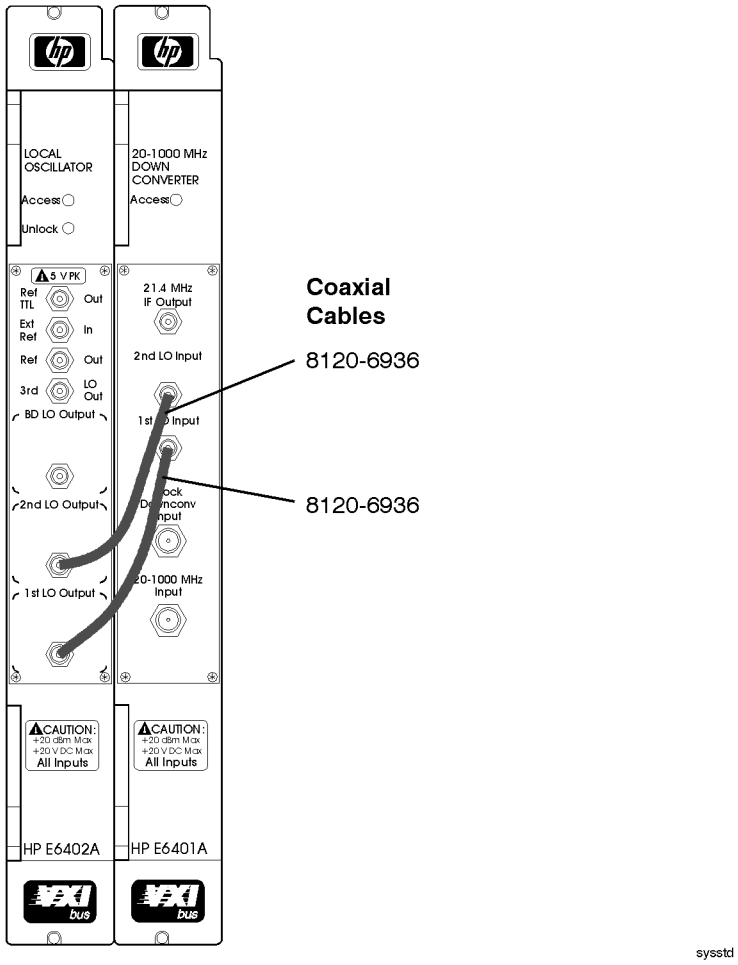


***Figure 1-6 HP E6500A System Configuration***

## HP E6500A Option 001

The HP E6500A Option 001 tuner consists of two single-slot C-size VXI modules: the HP E6401A Option 001 baseband output (2.5 to 9.5 MHz) and the HP E6402A local oscillator.

**NOTE**

Option 001 is required when the HP E6500A tuner is used with the HP E3238S signals development system, the HP E1430A ADC module, the HP E1437A ADC module, or the HP 89410A vector signal analyzer.

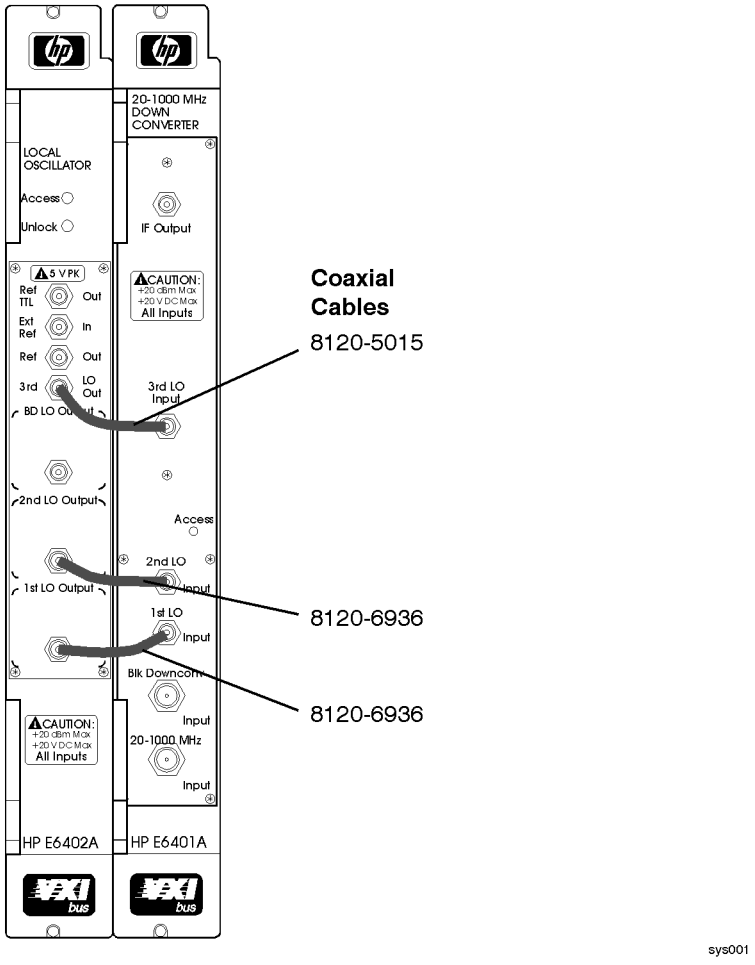


***Figure 1-7 HP E6500A Option 001 System Configuration***

## HP E6500A Option 003

The HP E6500A Option 003 tuner consists of three single-slot C-size VXI modules: the HP E6401A 20–1000 MHz downconverter, the HP E6403A 1000–3000 MHz block downconverter, and the HP E6402A local oscillator.

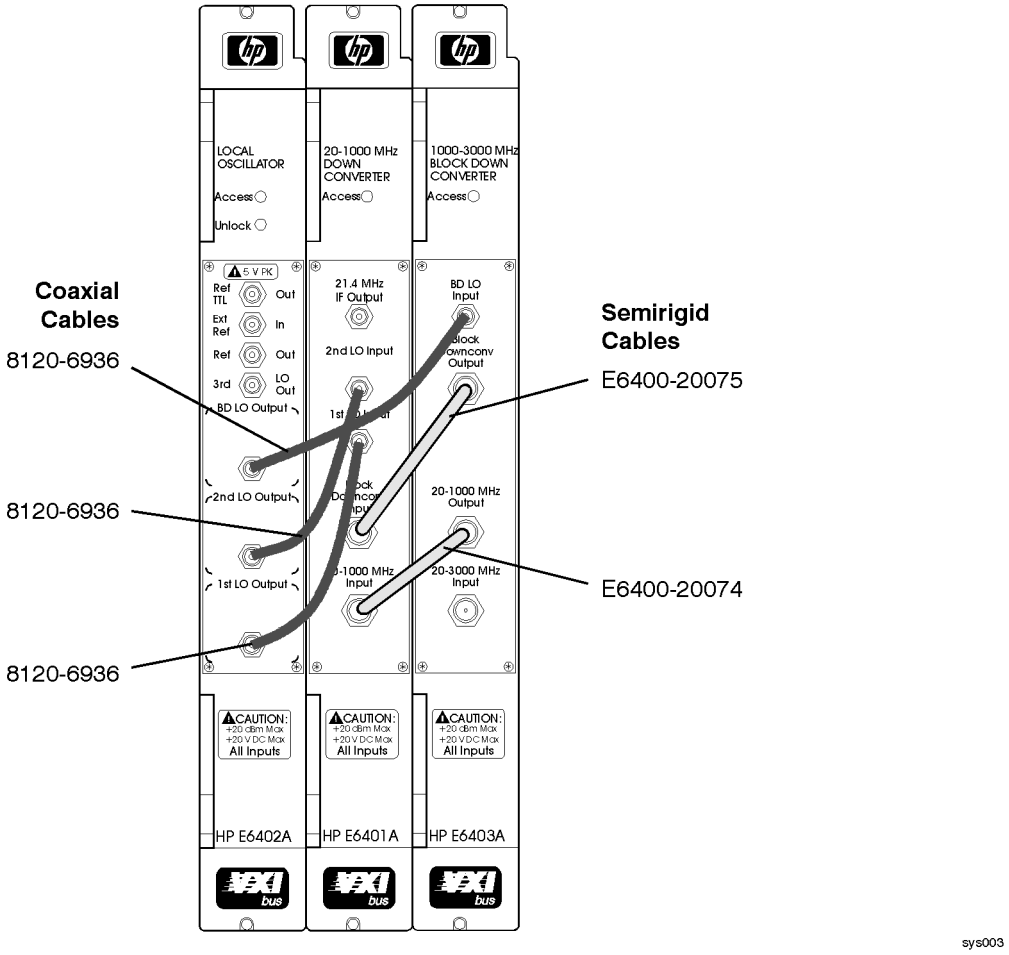


*Figure 1-8 HP E6500A Option 003 System Configuration*

## HP E6500A Option 001, 003

The HP E6500A Option 001, 003 tuner consists of three single-slot C-size VXI modules: the HP E6401A Option 001 baseband output (2.5 to 9.5 MHz), the HP E6403A 1000–3000 MHz block downconverter, and the HP E6402A local oscillator.

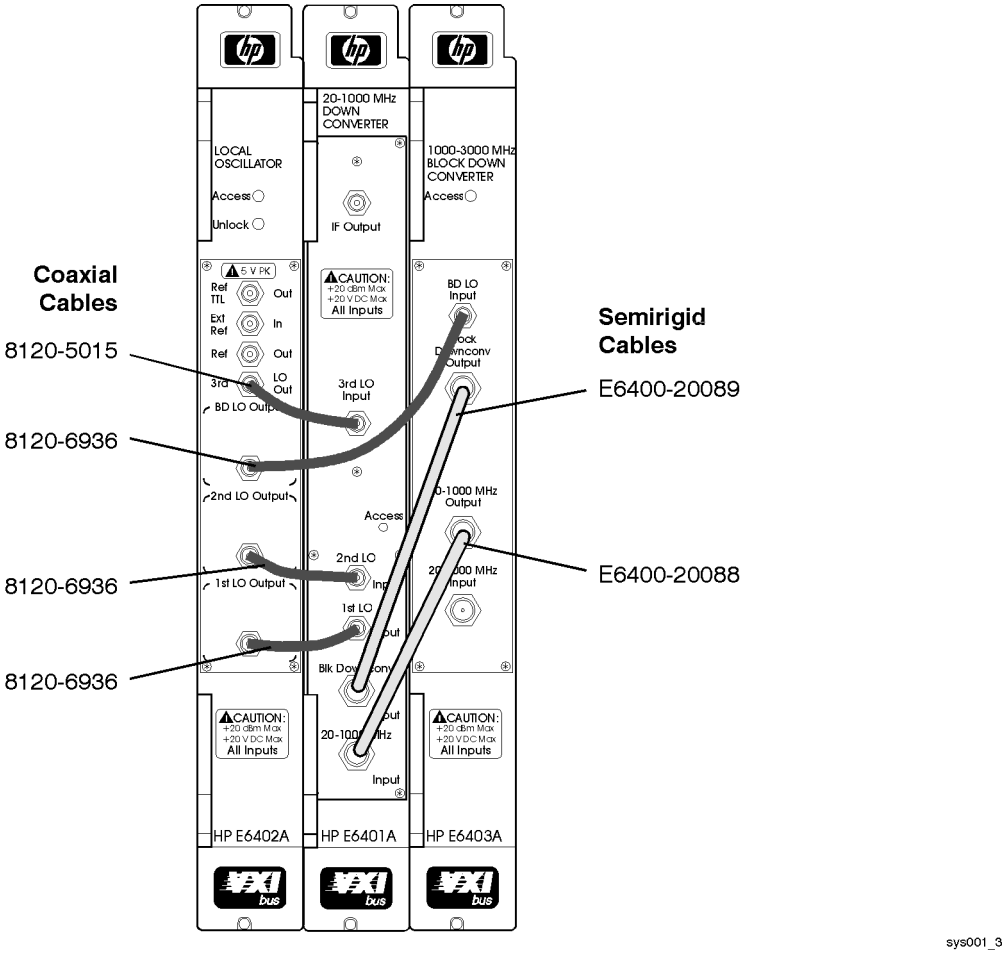


***Figure 1-9 HP E6500A Option 001, 003 System Configuration***

## HP E3238S with the HP E6500A Option 001, 003 Configuration

This is an example of how an HP E6500A Option 001, 003 may be configured as a tuner for the HP 3238S signals development system.

The Option 001 feature of the HP E6500A Option 001, 003 configuration provides a baseband (IF) signal to the HP E1437A or HP E1430A digitizer module where it is filtered and digitized. Then, the HP E1485A DSP module and the HP 1498A V743 controller module digitally process the signals to provide a spectral display on the color monitor.

For more information on this system, refer to the *HP E3238S Signals Development System Operator's Reference*.

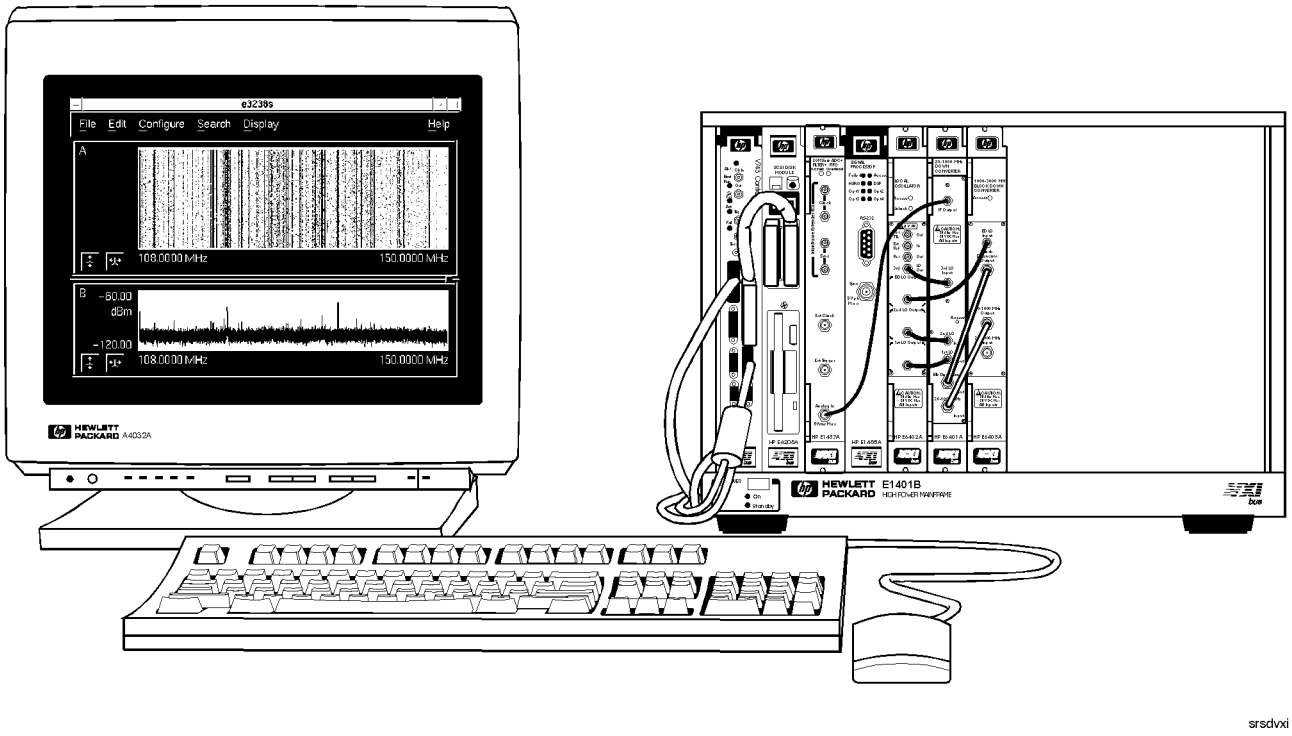


***Figure 1-10 HP E3238S System with HP E6500A Option 001, 003 Configuration***

## HP E6500A Option 006

The HP E6500A Option 006 tuner consists of the HP E6500A and the HP E1421B high-power VXI mainframe with six C-size slots for plug-in modules.

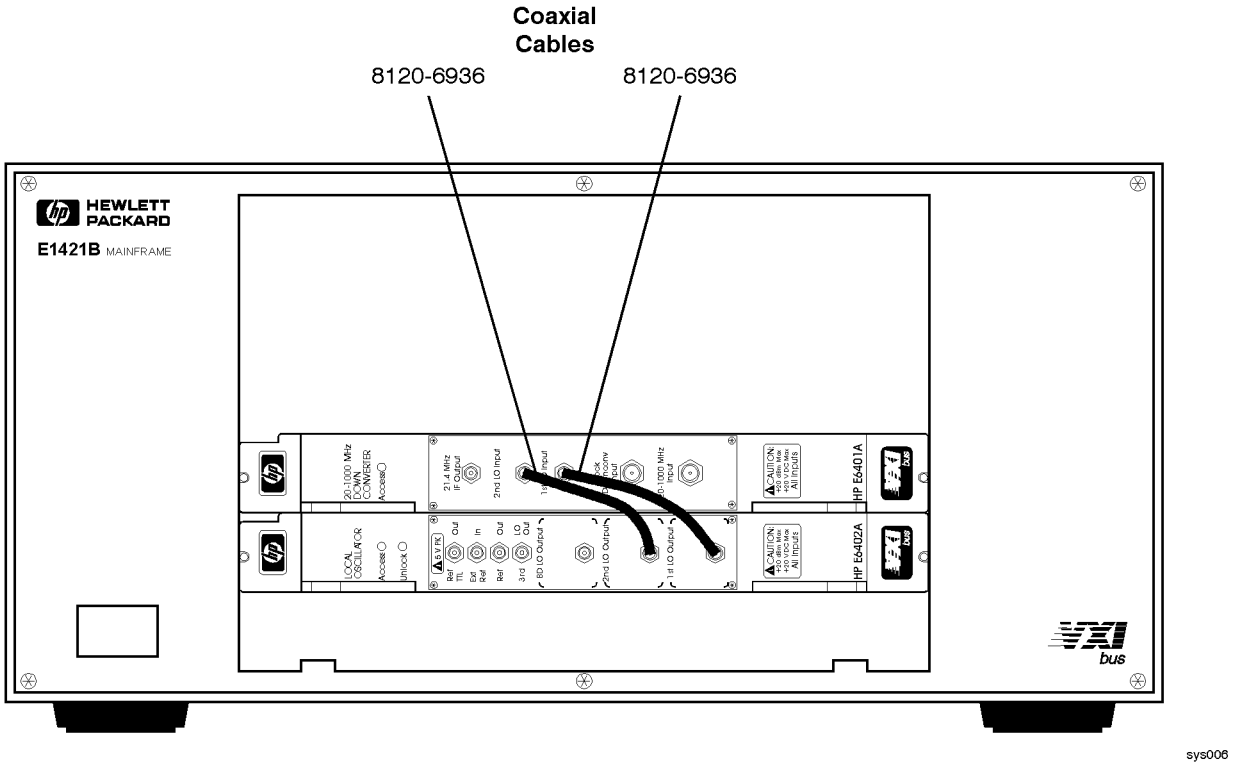


***Figure 1-11 HP E6500A Option 006 System with Mainframe Configuration***

## HP E6500A Option 013

The HP E6500A Option 013 tuner consists of the HP E6500A and the HP E1401B high-power VXI mainframe with 13 C-size slots for plug-in modules.

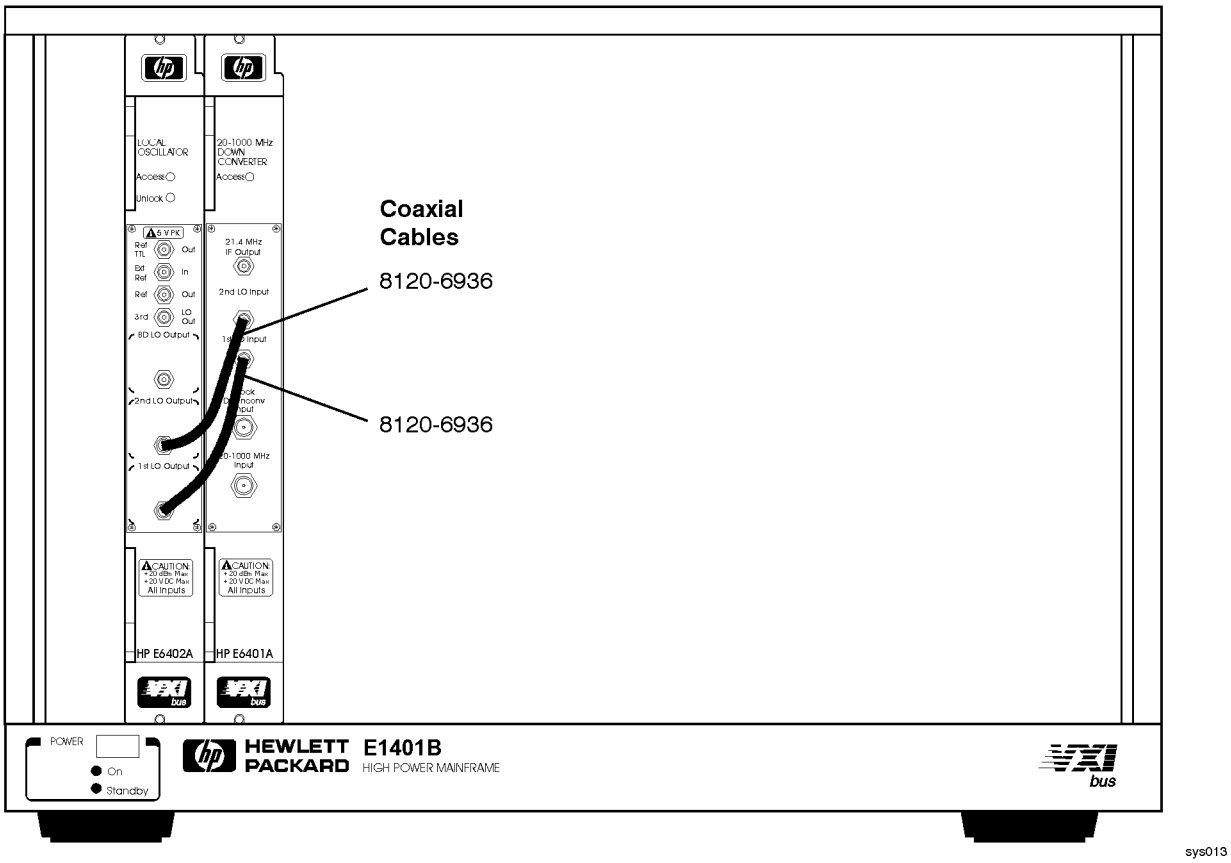


***Figure 1-12 HP E6500A Option 013 System with Mainframe Configuration***

# Accessories Supplied

***Table 1-1 HP E6401A 20–1000 MHz Downconverter Accessories***

| Description | Quantity | Part Number |
|---|---|---|
| Coaxial cable, SMC (f)/SMC (f), 120 mm | 2 | 8120-6936 |

***Table 1-2 HP E6401A Option 001 20–1000 MHz Downconverter Accessories***

| Description | Quantity | Part Number |
|---|---|---|
| Coaxial cable, SMC (f)/SMC (f), 120 mm | 2 | 8120-6936 |
| Coaxial cable, SMB (f)/SMB (f), 120 mm | 1 | 8120-5015 |
| Coaxial cable, SMB (f)/BNC (m), 600 mm | 1 | 8120-6269 |

***Table 1-3 HP E6402A Local Oscillator Accessories***

| Description | Quantity | Part Number |
|---|---|---|
| *HP E6500A VXI Tuner User's Guide* | 1 | E6500-90001 |
| Driver software | 1 | E6500-10005 |
| Coaxial cable[1],SMB (f)/SMB (f), 205 mm | 1 | 8120-5017 |

1. This cable connects the Ref TTL Out connector to the slot 0 controller. This connection is optional.

***Table 1-4 HP E6402A Option 002 Local Oscillator Accessories***

| Description | Quantity | Part Number |
|---|---|---|
| *HP E6500A VXI Tuner User's Guide* | 1 | E6500-90001 |
| Driver software | 1 | E6500-10005 |
| Coaxial cable[1], SMB (f)/SMB (f), 205 mm | 1 | 8120-5017 |

1. This cable connects the Ref TTL Out connector to the slot 0 controller. This connection is optional.

***Table 1-5 HP E6403A 1000–3000 MHz Block Downconverter Accessories***

| Description | Quantity | Part Number |
|---|---|---|
| Coaxial cable, SMC (f)/SMC (f), 120 mm | 1 | 8120-6936 |
| Semirigid cable, SMA (m)/SMA (m) | 1 | E6400-20074 |
| Semirigid cable, SMA (m)/SMA (m) | 1 | E6400-20075 |
| Semirigid cable, SMA (m)/SMA (m) | 1 | E6400-20088 |
| Semirigid cable,SMA (m)/SMA (m) | 1 | E6400-20089 |

# Electrostatic Discharge

## Preparing a Static-Safe Work Station

Electrostatic discharge (ESD) can damage or destroy electronic components. Therefore, all work performed on assemblies consisting of electronic components should be done at a static-safe work station. See Figure 1-13. Two types of ESD protection are shown:

- a conductive table mat and wrist strap combination
- a conductive floor mat and heel strap combination

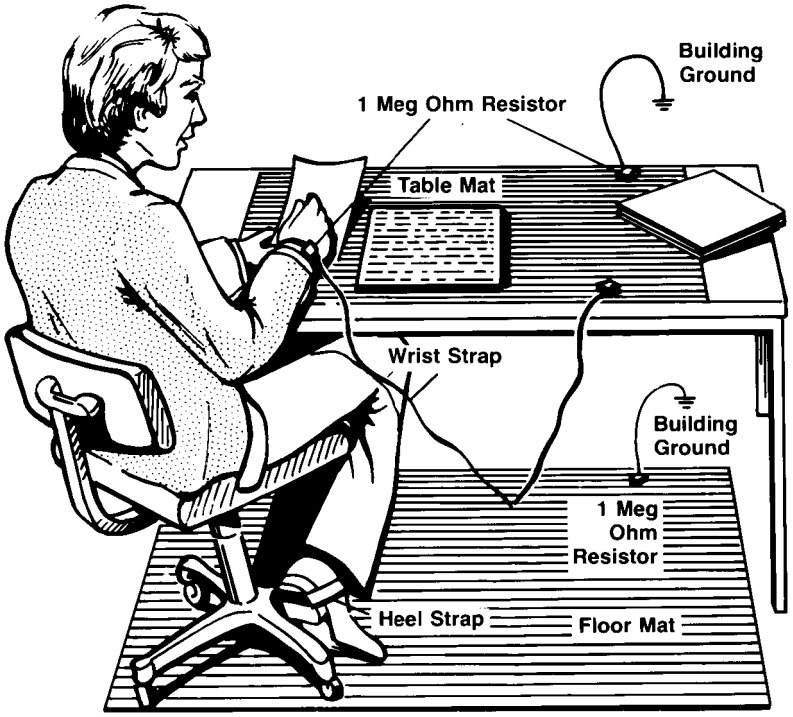


***Figure 1-13 Example of a Static-Safe Work Station***

**CAUTION**

- Do not touch the edge-connector contacts or trace surfaces with bare hands. Always handle board assemblies by the edges.
- Do not use erasers to clean the edge-connector contacts. Erasers generate static electricity and degrade the electrical quality of the contacts by removing the thin gold plating.
- Do not use paper of any kind to clean the edge-connector contacts. Paper or lint particles left on the contact surface can cause intermittent electrical connections.

## Reducing ESD Damage

To help reduce the amount of ESD damage that occurs during testing and servicing, use the following guidelines:

- Be sure that all instruments are properly earth-grounded to prevent buildup of static charge.
- Personnel should be grounded with a resister-isolated wrist strap before touching the center pin of any connector and before removing any assembly from a piece of equipment.
  Use a resister-isolated wrist strap that is connected to the mainframe's chassis. If you do not have a resistor-isolated wrist strap, touch the chassis frequently to equalize any static charge.
- Before connecting any coaxial cable to an instrument connector for the first time each day, *momentarily* short the center and outer conductors of the cable together.
- Handle all PC board assemblies and electronic components only at static-safe work stations.
- Store or transport PC board assemblies and electronic components in static-shielding containers.
- PC board assembly edge-connector contacts may be cleaned by using a lint free cloth with a solution of 80% electronics-grade isopropyl alcohol and 20% deionized water. This procedure should be performed at a static-safe work station.

***Table 1-6 Static-Safe Accessories***

| HP Part Number | Description |
|---|---|
| 9300-0797 | Set includes: 3M static control mat 0.6 m × 1.2 m (2 ft × 4 ft) and 4.6 m (15 ft) ground wire. (The wrist strap and wrist strap cord are not included. They must be ordered separately.) |
| 9300-0865 | Ground wire, 4.6 m (15 ft) |
| 9300-0980 | Wrist strap cord 1.5 m (5 ft) |
| 9300-1383 | Wrist strap, color black, stainless steel, without cord, has four adjustable links and a 7 mm post-type connection. |
| 9300-1169 | ESD heel strap (reusable 6 to 12 months.) |
| Order the above by calling HP DIRECT at (800) 538-8787 or through any Hewlett-Packard Sales and Service Office. | |

# Preparation for Use

This procedure describes how to configure and install C-size VXI modules into a C-size VXIbus mainframe by using the following steps:

1. Setting the logical address switches
2. Installing the tuner
3. Cabling the tuner

**WARNING**

**SHOCK HAZARD. Only service-trained personnel who are aware of the hazards involved should install, remove, or configure the system. Before you perform any procedures in this guide, disconnect AC power and field wiring from the mainframe.**

**To avoid electrical shock, always cover unused slots with the faceplate panels that came with the mainframe**

**CAUTION**

- STATIC ELECTRICITY. Static electricity is a major cause of component failure. To prevent damage to the electrical components in the mainframe and plug-in modules, observe anti-static techniques whenever handling a module.
- It is your responsibility to ensure that adequate cooling is supplied to all modules installed in the mainframe. Section B.7.2.4 of the VXIbus Specification (Revision 1.3) discusses module cooling requirements. Section B.7.3.5 discusses mainframe cooling requirements.

## Setting the Logical Address Switches

Each module is shipped with a factory-set logical address as shown in the following table. Each module installed in a mainframe must have a unique logical address. If there is more than one module with the same factory-set logical address (for example, more than one module of the same model), you must change the logical address of each additional module. This can be accomplished by incrementing the factory-set logical address number by five for each additional module of the same model.

***Table 1-7 Address Settings***

| Model | Factory-Set Logical Address | Secondary Address Setting |
|---|---|---|
| HP E6401A | 42 | 47 |
| HP E6401A Option 001 | 42 | 47 |
| HP E6402A | 41 | 46 |
| HP E6402A Option 002 | 41 | 46 |
| HP E6403A | 40 | 45 |

### Procedure

Follow the steps and refer to Table 1-7 below to set each module's logical address:

1. Locate the logical address switch on each module.
2. Set the module's logical address using the following guidelines:
    a. Use the factory-set logical address. If you have modules with the same logical address, change the address of one or more of those modules until all modules have different logical addresses.
    b. If multiple mainframes are connected via MXIbus, make sure the logical addresses of the modules in a mainframe are within the logical address window for that mainframe.
    c. Valid logical addresses are 1 through 255. Most Hewlett-Packard modules are statically configured modules, which means that you have to physically set the address on a switch. A dynamically configured module's address is set programmatically by the resource manager. To dynamically configure a module which supports dynamic configuration, its logical address must be set to 255. Note, however, if a statically configured module is set to 255, the resource manager will not dynamically configure any module.

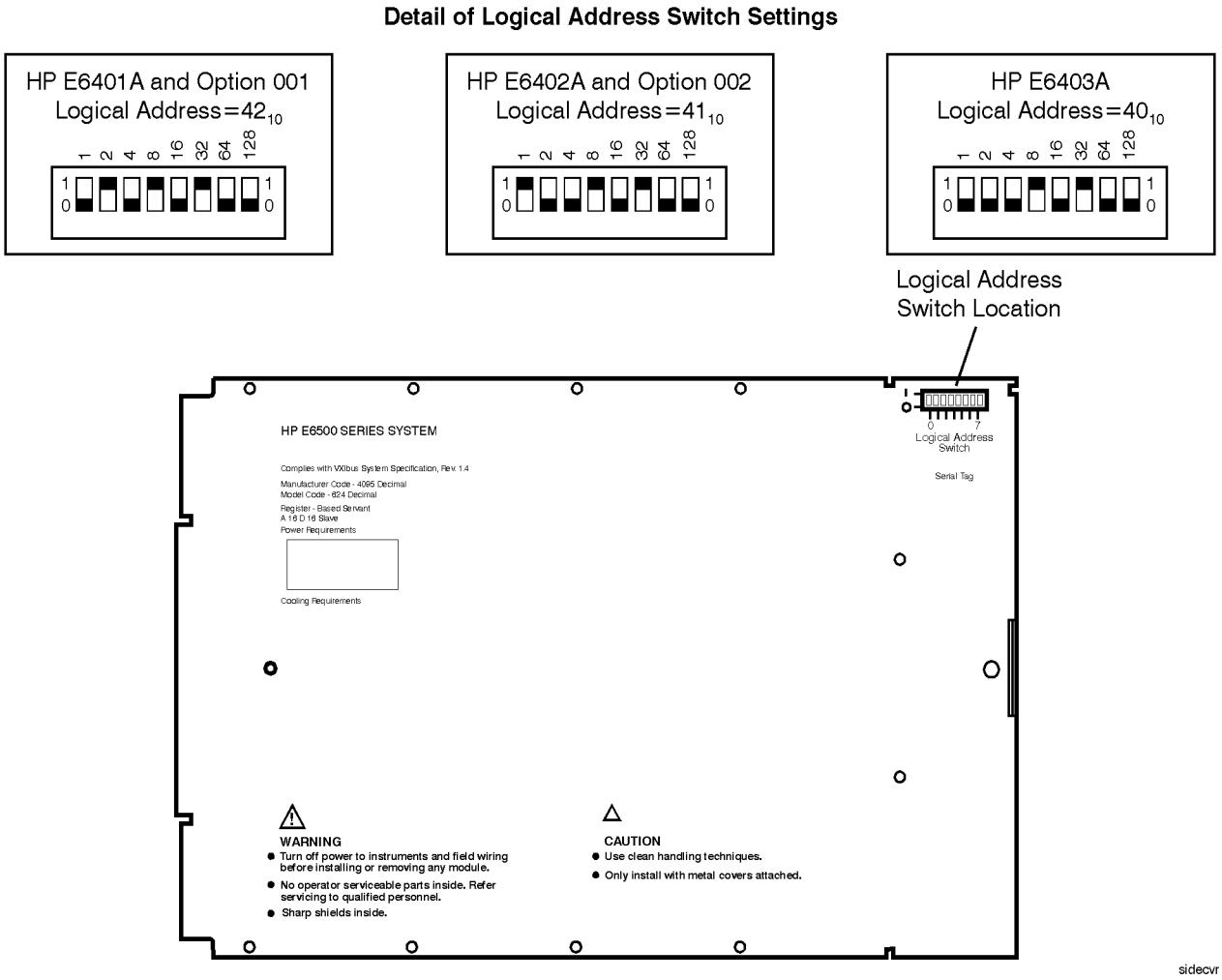


***Figure 1-14 HP 640xA Side Cover with Logical Address Switch Location and Address Switch Configurations for each Model of Module***

## Installing the Tuner

The modules can be installed in any slot except 0. The modules should be installed in the order shown for that system configuration so the cables can be correctly connected between the modules.

Use the following steps to install the tuner:

1. Set up the VXI mainframe. See the installation guide for your C-size VXIbus mainframe. If the mainframe is turned on, turn it off by pressing the button in the lower-left front corner.
2. Select the correct slot for each module. See the systems illustrations in the section “Typical Tuner System Configurations” beginning on page 1-14.
3. With the extractor handles lifted, insert each module into the mainframe by aligning the top and bottom of the module with the card guides inside the mainframe. Slowly push the module straight into the slot until it seats in the backplane connectors. When installing modules in the HP E1421B mainframe, the “top” of a module will be on the left when it is installed horizontally.
4. Secure the modules to the mainframe by pushing the extractor handles in until they lock in place.

## Cabling the Tuner

Refer to the section “Typical Tuner System Configurations” beginning on page 1-14 for cabling configuration illustrations.

### 10 MHz Reference

We recommend that:

- any external reference used for the HP E6500A have good phase noise and stability
- the slot 0 controller use the HP E6402A ref TTL out signal to eliminate the possibility of spurious responses caused by different references

# HP E6500A Operator's Check

This check procedure applies only to system-level configurations. There is *no* procedure for verifying individual module operation.

To verify the correct operation of the HP E6500A tuner system configurations you will need the following test equipment and adapters:

***Table 1-8 Test Equipment Needed***

| Equipment and Accessories | Critical Specification for Test Equipment | Recommended Model |
|---|---|---|
| Signal source | Frequency range: 20–1000 MHz<br>or to 3000 MHz (if Option 003 is present)<br>Amplitude accuracy: 1.5 dB | HP 8648C |
| Power meter | Power range: -30 to 0 dBm<br>Power accuracy: 0.1 dB | HP 437B |
| Power sensor | Power range: -30 to +20 dBm | HP 8482A |
| Adapter | Type-N (f) to BNC (f) | HP 1250-1474 |
| Adapter | Type-N (m) to BNC (f) | HP 1250-0780 |
| Adapter | BNC (f) to SMA (m) | HP 1250-1200 |
| Cable | BNC (m) to (m) | HP 10501A |

## Procedure

1. Turn on the VXI mainframe.
2. Run the VXI controller initialization software.
3. Install the software.

   To install the HP E6500A software, insert the supplied CD into your CD drive and run the `Setup.exe` executable program. After following the setup instructions, the driver, demonstration GUI, source code, and necessary components will be installed on your computer. The default location for the GUI executable and all source files is `C:\Program Files\hpe6500a`. The `hpe6500.dll` components will reside in the `C:\winnt\system32` folder. As stated in the installation procedure, the host computer must be restarted prior to using the HP E6500A software.

**NOTE**

It is assumed that the user has installed the VISA drivers for their VXI interface prior to installing and running the HP E6500A software.

4. Start the HP E6500A demonstration GUI. This will program the local oscillator synthesizers and turn on the internal 10 MHz reference. Allow 30 minutes of warm-up time to ensure frequency accuracy.

**NOTE**

The driver supplied with this product works only on Windows NT, 4.0 (with Service Pack 3.0 or higher).

5. Set the signal source to -20 dBm while measuring with the power sensor through the BNC cable.
6. Connect the signal source to the HP E6401A 20–1000 MHz Input port or, if Option 003 is present, to the HP E6403A 20–3000 MHz Input port.
7. Verify that the amplitudes are correct for each frequency listed in the following table by entering the frequency value in the **TuneFrequency** window. The signal source should be set to each frequency and have an amplitude of -20 dBm. The 21.4 MHz IF out gain should be 5 dB, measuring -15 dBm +/-4 dB. If Option 001 is present, the gain should be 15 dB measuring -5 dBm +/-5 dB.
8. Repeat steps 4 through 6 for each frequency listed in Table 1-9 on page 1-30

***Table 1-9 Frequency Points Measured for Operator's Check Procedure***

| System Type | Preselector Band | Frequency (MHz) |
|---|---|---|
| HP E6500A without Option 003 | 1 | 30 |
| | 2 | 50 |
| | 3 | 70 |
| | 4 | 100 |
| | 5 | 130 |
| | 6 | 180 |
| | 7 | 300 |
| | 8 | 400 |
| | 9 | 600 |
| | 10 | 800 |
| HP E6500A with Option 003 | 11 | 1100 |
| | 12 | 1500 |
| | 13 | 2000 |
| | 14 | 2800 |

# 2 Using the Driver and Demonstration GUI

The HP E6500A tuner is a register based VXI instrument and thus requires externally running software for control. The HP E6500A is supplied with a CD which contains the compiled driver (*hpe6500.dll*), a demonstration GUI that is used to configure and control up to four HP E6500A tuners, and the components necessary to operate both the driver and the demonstration GUI on a computer running Windows NT 4.0. The source code for both the driver and the demonstration GUI are also provided.

## About the Driver

In order to be VXIplug&play compatible, the driver is written in C. It was created and built using Microsoft Visual C++ Developer Studio, Version 6.0. A listing of the driver source and header files is shown below.

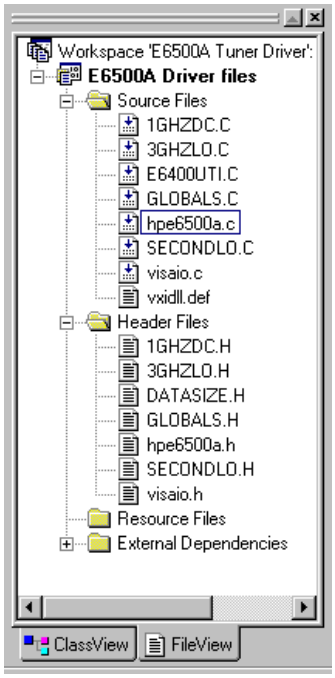


***Figure 2-1 HP E6500A Source and Header Files***

The software layer for all user interface tuner functionality is in the *hpe6500a.c* source file. Communications with the hardware are passed through this source file, with low level hardware communication being handled by the *hwRead* and/or *hwWrite* functions in the *visaio.c* file.

The HP E6500A driver is somewhat unique in that a standard VXIplug&play driver normally controls a single instrument. In the case of the HP E6500A, a single driver simultaneously controls three different VXI modules. Thus, many of the required VXIplug&play function prototypes do not make sense for the architecture of the HP E6500A. This is explained in greater detail with the listing of each function prototype.

# Driver Functions

The driver functions listed in this document are those functions in the *vxidll.def* file and thus are exported for external use. There are many functions internal to the driver which are not detailed.

The first three prototypes listed are configuration and initialization functions and should be used in the order listed.

## Configuration and Initialization

The driver performs the following configuration and initialization functions:

### Collect system information:

```
ViStatus _VI_FUNC hpe6500_sys_info(ViUInt16 number_of_tuners,
ViUInt16 SharedLO)
```

This function receives the number of tuners and the shared LO status from the user interface. A value of zero indicates a system with a non-shared LO and a value of one indicates a system with a shared LO. The driver and GUI are constructed such that if the LO is shared, it is strongly recommended that it should be shared across all tuners and the shared LO set with a value of one. This is not a requirement, but can lead to confusion if the user attempts to use a single LO to tune independent tuners to different frequencies.

### Receive logical addresses, IF output frequency information, and establish session ID numbers:

```
ViStatus _VI_FUNC hpe6500_setup_sessions(ViUInt16
tuner_number, ViUInt16 Opt001, ViUInt16 LO_log_add, ViUInt16
OneGHz_log_add, ViUInt16 ThreeGHz_log_add, ViUInt32
*LO_session_id, ViUInt32 *OneGHz_session_id, ViUInt32
*ThreeGHz_session_id)
```

This function is used to establish session IDs with each of the tuner modules. Note that this is done on a per tuner basis. This function must be called with the corresponding tuner number and logical addresses for each tuner. If the HP E6403A is not used, its logical address should be passed as a zero. The driver and GUI are constructed to handle up to four tuners, with the parameter *tuner_number* running from 0 to 3. To increase the number of tuners, change the defined constant MAX_TUNERS from four to the desired number in both the driver and the GUI. The pointers to the session IDs are not actually required as passed parameters for driver functionality, but are included should a user wish to debug custom driver enhancements from the

GUI side. Other functions performed by the *hpe6500_setup_sessions* function are model number checking, opening a master session, error checking, and receipt of Opt001 status. Opt001 status relates to the HP E6401A downconverter IF output frequency. A status of zero will cause the IF output to be set to a center frequency of 21.4 MHz, and a status of one will cause the IF output to be set to a center frequency of 5.6 MHz. Since HP E6401A's are available that can provide either output frequency, option checking is not possible and it remains for the user to correctly match the output frequency choice with the HP E6401A downconverter hardware configuration.

If the shared LO flag has been set, the shared LO will receive only one session ID. This session ID is automatically used with each tuner grouping since the logical address for the LO is identical for all tuners.

## Initialize tuners:

*ViStatus _VI_FUNC hpe6500_init_tuners(short tuner_num)*

This function sets up the LOs, the preselection, the internal 10 MHz reference, the attenuators, correction factors, and the initial frequency for each tuner referenced by *tuner_num*. Unless absolutely necessary, it is strongly recommended not to alter any of the functions called by *hpe6500_init_tuners.* The driver and GUI are constructed such that *tuner_num* runs from 0 to 3.

**The Defaults are:**

| | |
|---|---|
| 10 MHz Reference | Internal |
| Input Attenuation | 0 dB |
| Initial Frequency | 20 MHz |

# Common Use Functions

### Set the 10 MHz reference:

```
ViStatus _VI_FUNC hpe6500_set_reference(ViUInt16 tuner_num,
ViUInt16 Source)
```

The 10 MHz reference is set on a per tuner basis. `Source=0` corresponds to internal reference and `Source=1` corresponds to external reference. A clean external reference is required to meet tuner phase noise characteristics.

### Set the frequency:

```
ViStatus _VI_FUNC hpe6500_set_frequency(ViUInt16 tuner_num,
ViReal64 frequency)
```

The frequency is set on a per tuner basis with tuner numbers running from 0 to 3. Driver allowable tuning range is a function of the tuner configuration. A tuner configuration of an HP E6402A LO and an HP E6401A 20 MHz to 1000 MHz downconverter will allow tuning from 2 MHz to 1000 MHz. Addition of an HP E6403A 1 GHz to 3 GHz downconverter will cause the driver to extend tuning up to 3 GHz.

**NOTE**

The tuner performance is unspecified below 20 MHz.

### Set the input attenuation:

```
ViStatus _VI_FUNC hpe6500_set_input_attenuation(ViUInt16
tuner_num, ViUInt16 attenuation)
```

This function sets the input attenuation to the tuner. Attenuation is set on a per tuner basis with tuner numbers running from 0 to 3. Possible attenuation values are: 0, 10, 20, and 30. Receipt by the driver of any other values will generate an error.

### Set the output attenuation:

```
ViStatus _VI_FUNC hpe6500_set_output_attenuation(ViUInt16
tuner_num, ViUInt16 attenuation)
```

This function sets the output attenuation of the tuner. Attenuation is set on a per tuner basis with tuner numbers running from 0 to 3. Possible attenuation values are integers running from 0 to 15. These correspond to sixteen 1 dB steps of the output attenuator. The settings of the output attenuator are

preprogrammed and are used to flatten the frequency response of the tuner. Thus, the attenuation setting is a function of frequency. Changing these values will cause the flatness of the tuner to degrade. For this reason, the *hpe6500_set_output_attenuation* entry point is provided in the driver for those who really need its functionality, but is not exposed for immediate use in the GUI.

**NOTE**

If the output attenuator is set by the user via this function call, and then the tuner frequency is changed, the output attenuator setting will be set to the preprogrammed value for the new frequency.

### Get the output attenuation:

```
ViStatus _VI_FUNC hpe6500_get_output_attenuation(ViUInt16
tuner_num, ViUInt16 *attenuation)
```

This function gets the output attenuation of the tuner. Attenuation is requested on a per tuner basis with tuner numbers running from 0 to 3. Possible attenuation values are integers running from 0 to 15. These correspond to sixteen 1 dB steps of the output attenuator. The settings of the output attenuator are preprogrammed and are used to flatten the frequency response of the tuner. Thus, the attenuation setting is a function of frequency. Changing these values will cause the flatness of the tuner to degrade. Although exercising this function does not change the output attenuator setting, to mirror the use of the *hpe6500_set_output_attenuation*, the *hpe6500_get_output_attenuation* entry point is provided in the driver for those who really need its functionality, but is not exposed for immediate use in the GUI.

# Miscellaneous Functions

### Get the driver revision:

```
ViStatus _VI_FUNC hpe6500_driver_rev(ViChar _VI_FAR
driver_rev[])
```

This function retrieves the revision of the tuner driver. The driver revision is located in the driver itself, so no hardware communication is required.

### Close all session ID's and master session ID:

```
ViStatus _VI_FUNC hpe6500_close_all(void)
```

This function closes all open instrument sessions and the master session ID. This is *not* on a per tuner basis. The driver will check all possible tuners for open sessions and will close them all with this single command.

### Get the HP E6401A temperature:

```
ViStatus _VI_FUNC hpe6500_get_temp(ViUInt16 tuner_num, float
*temperature)
```

This function reads the HP E6401A temperature in degrees Celsius. A nominal operating temperature is around 30 $^{o}$C. The temperature is requested on a per tuner basis, with **tuner_num** running from 0 to 3.

### Reset tuners:

```
ViStatus _VI_FUNC hpe6500_tuner_reset(short number_of_tuners)
```

This function can be used to reset all active tuners. The parameter `number_of_tuners` runs from 0 to 3. Note that the tuners must be configured in a continuous manner to use this function. For example, if three tuners are used, they must be configured as tuners 0, 1, and 2 (which corresponds to 1, 2, and 3 on the GUI), and not 0, 1, and 3. The `hpe6500_tuner_reset function` calls the `hpe6500_init_tuners` function. See the `hpe6500_init_tuners` function for further information.

# VXIplug&play Required Functions

### Provides the VXIplug&play prototype for init:

```
ViStatus _VI_FUNC hpe6500_init(ViRsrc rsrcName, ViBoolean
id_query, ViBoolean reset_instr, ViPSession vi)
```

Since the HP E6500A tuners function as a grouping of modules, this required function prototype is not useful for controlling a tuner. It is included to meet the VXIplug&play standard and can be used to open a session with a card. Due to the use of tuner groupings, this function is not recommended to be used for opening any sessions or for tuner control.

### Provides the VXIplug&play prototype for reset:

```
ViStatus _VI_FUNC hpe6500_reset(ViSession vi)
```

This function is included to meet the VXIplug&play standard. Since the HP E6500A tuners function as a grouping of modules, resetting a single module is not useful and not recommended to be used. Use of this function will return: **VI_WARN_NSUP_RESET.**

### Provides the VXIplug&play prototype for self_test:

```
ViStatus _VI_FUNC hpe6500_self_test(ViSession vi, ViPInt16
test_result, ViChar _VI_FAR test_message[])
```

This function is included to meet the VXIplug&play standard. The HP E6500A is register based and thus does not support self test. Use of this function will return: **VI_WARN_NSUP_SELF_TEST.**

### Provides the VXIplug&play prototype for error_query:

```
ViStatus _VI_FUNC hpe6500_error_query(ViSession vi, ViPInt32
error_code, ViChar _VI_FAR error_message[])
```

This function is included to meet the VXIplug&play standard. The HP E6500A is register based and thus does not support error query. Use of this function will return: **VI_WARN_NSUP_ERROR_QUERY.**

### Provides the VXIplug&play prototype for error_message:

```
ViStatus _VI_FUNC hpe6500_error_message(ViSession vi, ViStatus
status_code, ViChar _VI_FAR message[])
```

This function is used to retrieve an error message that is based on an error return value which in the prototype is called: *status_code.* When a driver error is generated, a return value is received in the user interface. The GUI can have its own error table or it can call the function *hpe6500_error_message* to retrieve the error message that corresponds with the error number. The complete error listing is given in a later section.

### Provides the VXIplug&play prototype for revision_query:

```
ViStatus _VI_FUNC hpe6500_revision_query(ViSession vi, ViChar
_VI_FAR driver_rev[], ViChar _VI_FAR instr_rev[])
```

This function is included to meet the VXIplug&play standard. The HP E6500A contains no firmware and thus can only return a driver revision. The driver revision is not associated with a particular piece of hardware or session ID. Use of this function will return: **VI_WARN_NSUP_REV_QUERY.** Use the function: *hpe6500_driver_rev* to read the driver revision.

### Provides the VXIplug&play prototype for close:

```
ViStatus _VI_FUNC hpe6500_close(ViSession vi)
```

This function is included to meet the VXIplug&play standard. Since the HP E6500A tuners function as a grouping of modules, closing the session for a single module is not recommended, but it is supported by the driver. To end a period of instrument usage, use: *hpe6500_close_all.*

# Error Codes

The introduction of error codes was performed at a fairly high hardware level so as not to hinder the hardware speed. For example, to initialize the HP E6402A LO module, over 100 writes to the hardware take place. If each of those writes was monitored for errors with a corresponding error code, hardware performance could be compromised. The error codes have been placed in such a way that each function call is monitored for at least one read or write to the hardware. Other than hardware end-performance, there is no way of checking whether the hardware actually received the correct bits or performed the requested function.

The *hpe6500.dll* error codes, along with their corresponding numeric integer and hexadecimal values are given below:

```
#define ERROR_INITIALIZING_1GHZ_LO                    -100      /*  FFFFFF9C  */
#define ERROR_INITIALIZING_1GHZ_DC                    -101      /*  FFFFFF9B  */
#define ERROR_INITIALIZING_3GHZ_DC                    -102      /*  FFFFFF9A  */
#define ERROR_SETTING_FREQUENCY_DURING_INITIALIZATION  -103      /*  FFFFFF99  */
#define ERROR_NO_LO_MODULE                            -104      /*  FFFFFF98  */
#define ERROR_NO_1GHZ_MODULE                          -105      /*  FFFFFF97  */
#define ERROR_OPENING_LO_SESSION                      -106      /*  FFFFFF96  */
#define ERROR_OPENING_1GHZ_SESSION                    -107      /*  FFFFFF95  */
#defineERROR_OPENING_3GHZ_SESSION                     -108      /*  FFFFFF94  */
#defineERROR_OPENING_MAIN_VI_SESSION                  -109      /*  FFFFFF93  */
#defineERROR_READING_LO_MOD_NUM                       -110      /*  FFFFFF92  */
#defineERROR_READING_1GHZ_MOD_NUM                     -111      /*  FFFFFF91  */
#defineERROR_READING_3GHZ_MOD_NUM                     -112      /*  FFFFFF90  */
#defineERROR_CLOSING_VI_SESSIONS                      -113      /*  FFFFFF8F */
#defineERROR_NO_ACTIVE_TUNERS                         -114      /*  FFFFFF8E */
#defineERROR_RESETTING_TUNER                          -115      /*  FFFFFF8D */
#defineERROR_SETTING_INPUT_ATTEN                      -116      /*  FFFFFF8C */
#defineERROR_SETTING_INTERNAL_REF                     -117      /*  FFFFFF8B */
#defineERROR_SETTING_EXTERNAL_REF                     -118      /*  FFFFFF8A */
#defineERROR_SETTING_FREQUENCY                        -119      /*  FFFFFF89 */
```

```
#define ERROR_READING_TEMPERATURE                    -120     /*  FFFFFF88 */
#define ERROR_INVALID_FREQUENCY                      -121     /*  FFFFFF87 */
#define ERROR_INVALID_INPUT_ATTENUATION_VALUE        -122     /*  FFFFFF86 */
#define ERROR_INVALID_OUTPUT_ATTENUATION_VALUE       -123     /*  FFFFFF85 */
#define ERROR_SETTING_OUTPUT_ATTENUATION             -124     /*  FFFFFF84 */
#define ERROR_READING_OUTPUT_ATTENUATION             -125     /*  FFFFFF83 */
```

# Using the Demonstration GUI

The HP E6500A is supplied with a demonstration GUI written in Microsoft Visual Basic 5.0. The demonstration GUI contains two forms: a configuration form which allows the configuration of up to four tuners, and the tuner form which allows easy access to normal tuner functionality.

The configuration form is shown in the following figure.

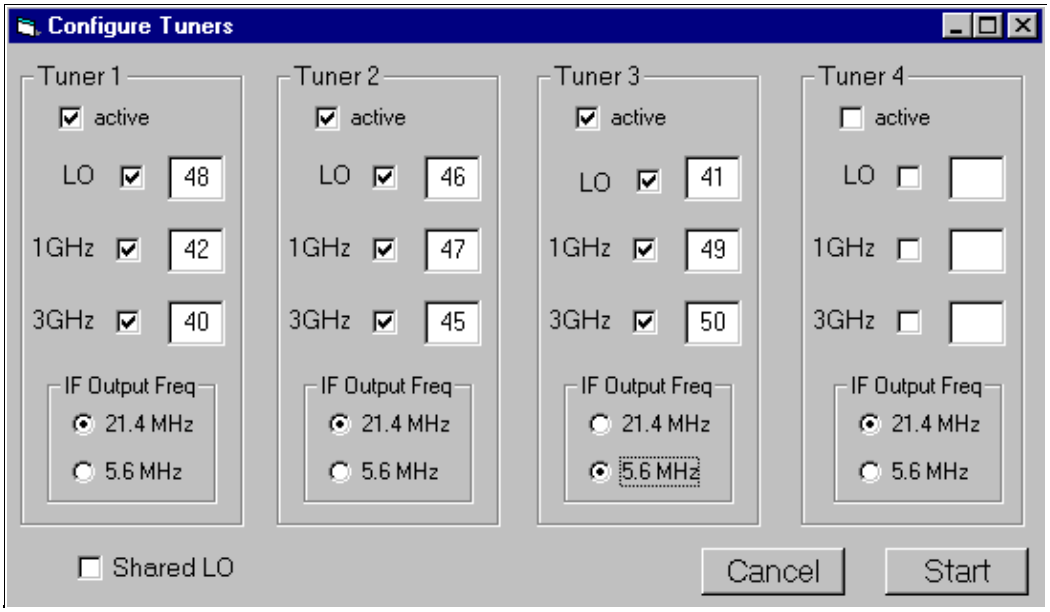


***Figure 2-2 Configuration Form Window***

To be usable, each configured tuner must be checked active and must contain an LO and a 1 GHz module. The 3 GHz module is optional.

GUI setups that will generate errors:

- Failure to select any active tuners will generate a GUI error.
- Failure to check both the LO and 1 GHz checkboxes for any active tuners will generate a GUI error.
- Failure to enter a logical address for a checked module will generate a GUI error.
- Entering the same logical address for multiple LOs, or 1 GHz modules, or 3 GHz modules will generate a GUI error.

- Entering a logical address for an incorrect card type will generate a driver error. For example, entering 46 for tuner 1 LO when 46 is the logical address of a 1 GHz downconverter will generate an error.

It is up to the user to set up the configuration GUI such that it corresponds to the hardware connectivity. No checking or assumptions are made based on slot position in the mainframe. Note that in Figure 2-2 on page 2-12, the 5.6 MHz baseband output has been selected for tuner 3. It is up to the user to be sure that the HP E6401A for tuner 3 is an Option 001 or has had its hardware set up for baseband operation.

If the configuration form is set up so as to generate an error, clicking on the Start button will activate error checking. Errors are presented in the form of dialog boxes. When the user clicks the **OK** button, most errors disappear and the user is returned to the configuration form in order to correct any entry problems. GUI errors are in lower case as shown in the following figure.

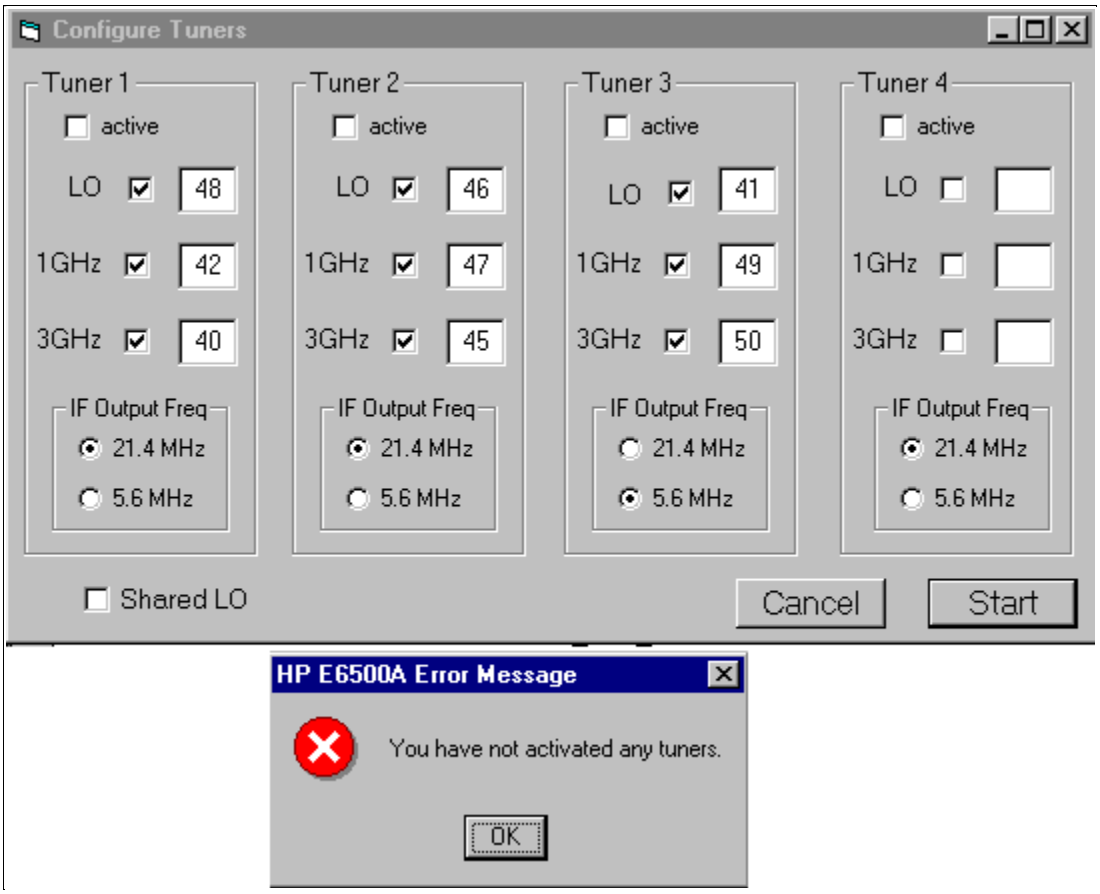


***Figure 2-3 Error Message Window Example***

Driver Errors are in uppercase and return an error number as shown in the following figure.

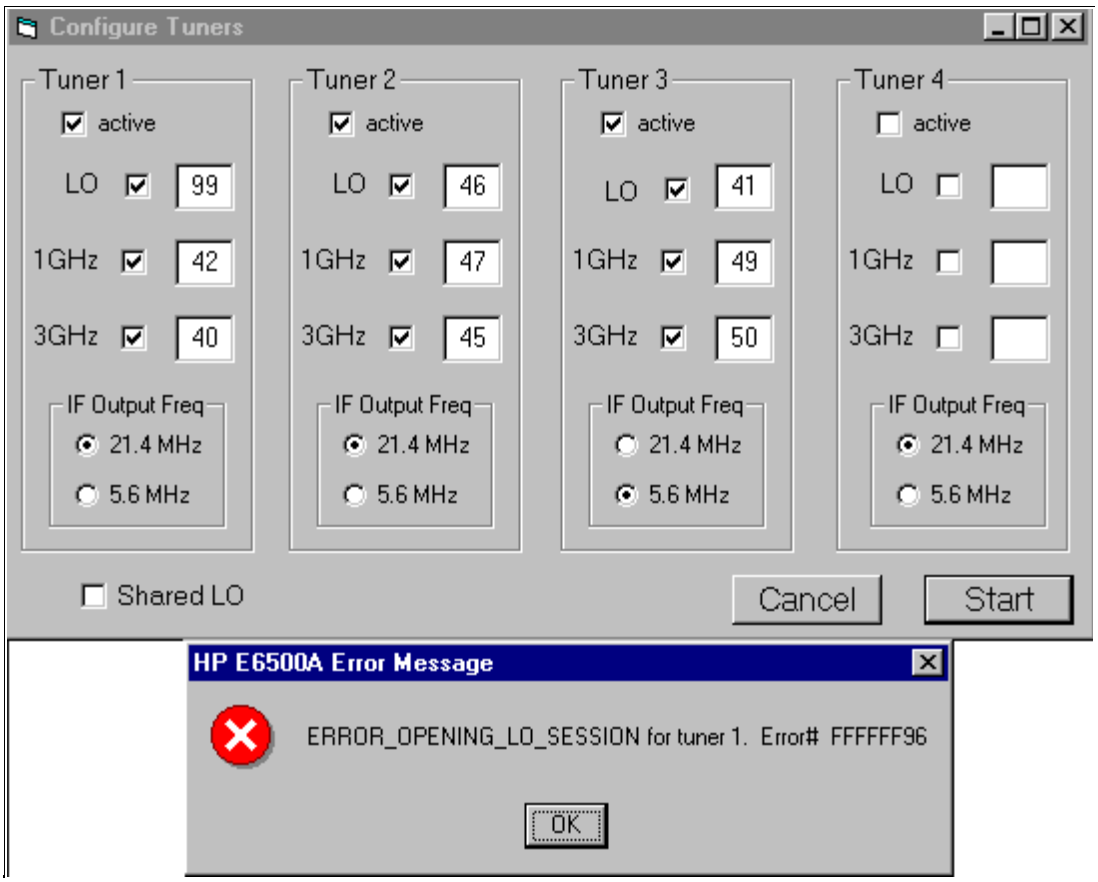


***Figure 2-4 Driver Errors Window Example***

When the Start button is clicked, the configuration is saved in the computer's registry.When the configuration form is run for the first time, the user must make the necessary entries for their system. Thereafter, the configuration will be remembered each time that the system is started.

If the **Shared LO** box is checked the configuration form behaves as shown in the following figure.

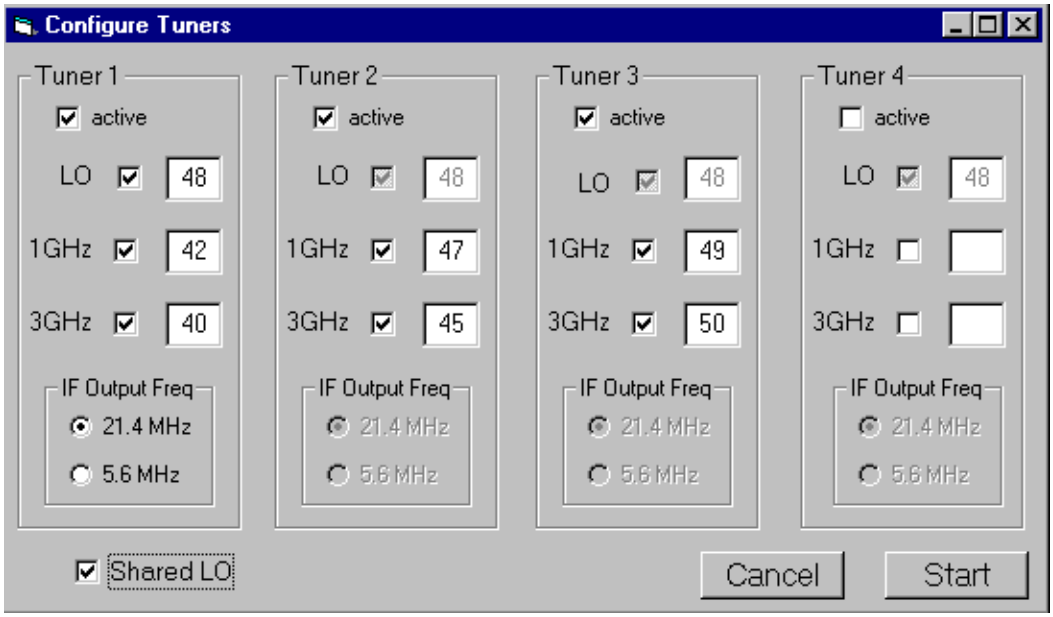


***Figure 2-5 Shared LO Box Configuration Window***

**NOTE**

The **LO** checkboxes and logical address text boxes are automatically filled in and grayed out for tuners 2, 3, and 4. Also note that since the LO is shared, all the IF output frequencies must be the same, so the **IF Output Freq** is only selectable for tuner 1. All the remaining tuners track the tuner 1 selection.

The operational tuner GUI is shown in the following figure.

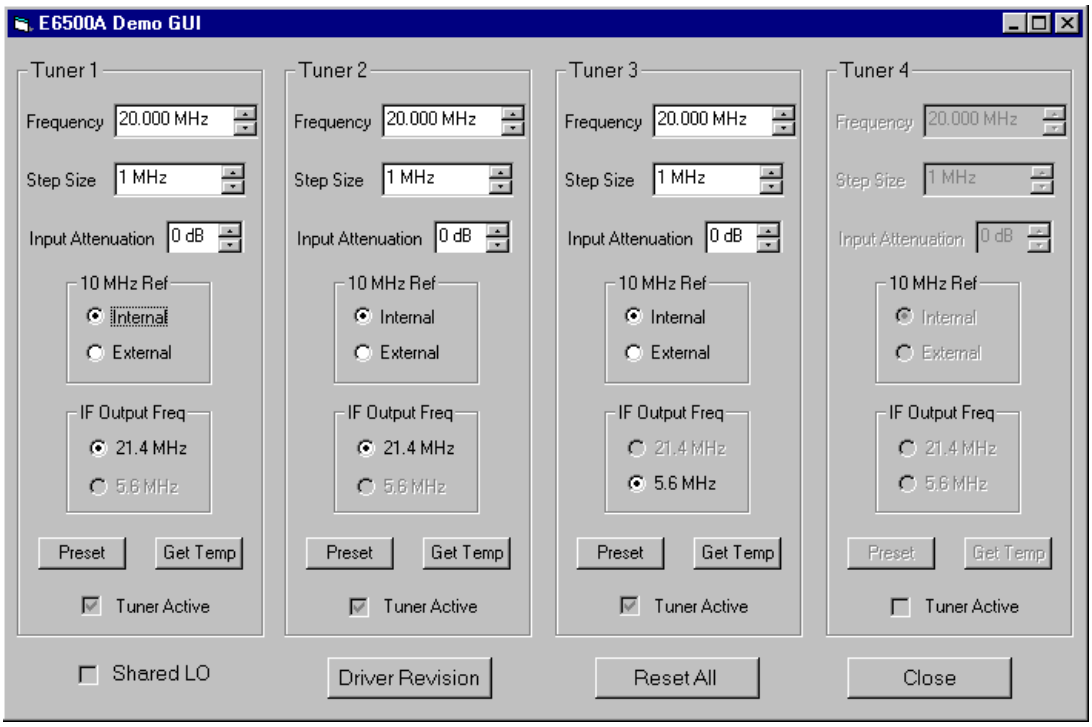


***Figure 2-6 Operational Tuner GUI Window***

Based on the previous configuration form settings from Figure 2-2 on page 2-12, three independent, active tuners are controllable from the E6500A Demo GUI. Frequency ranges are a function of the tuner configuration. Tunable frequency range for each tuner is 2-1000 MHz without an HP E6403A, 3 GHz downconverter, and 2-3000 MHz if tuner N's configuration included a 3 GHz downconverter.

**NOTE**

The tuner specifications do not apply *below* 20 MHz.

The operational tuner GUI for a shared LO configuration is shown in the following figure.

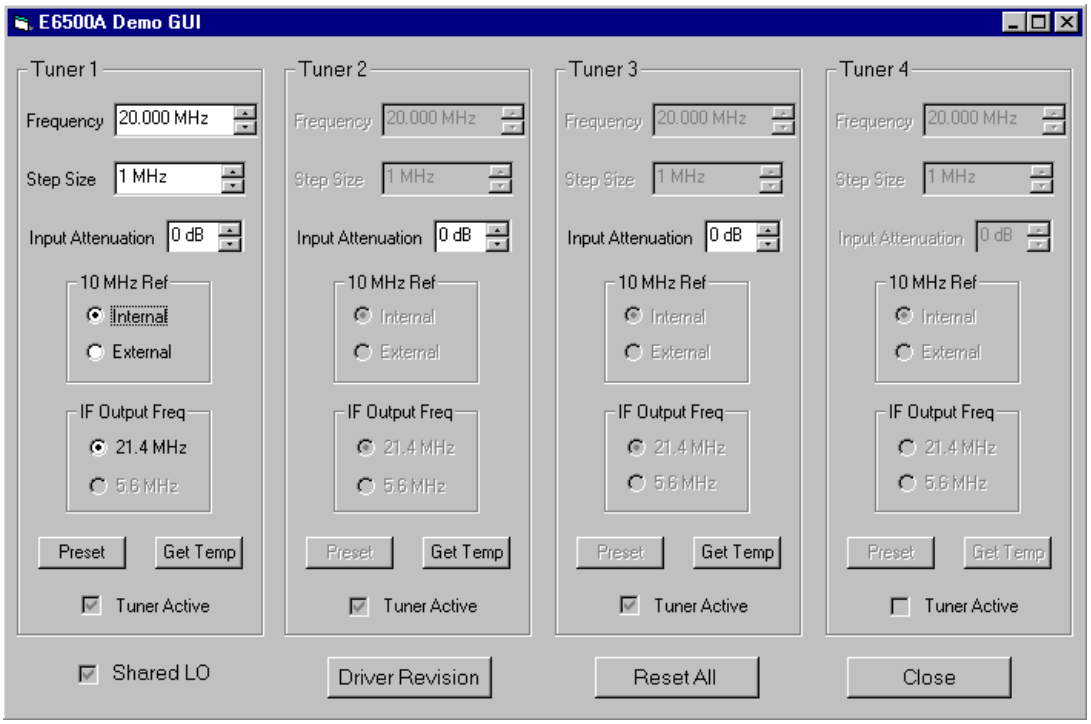


***Figure 2-7 Operational Tuner (Shared LO) GUI Window***

Based on the configuration form settings from Figure 2-5 on page 2-15 using a **Shared LO**, three active tuners are controllable from the E6500A Demonstration GUI.

# Demonstration GUI Controls

## General

The numeric control spin buttons are HP proprietary Active X controls. A tuner customer is licensed to use the controls in the GUI, but cannot use them for further software development work. Standard up/down or Microsoft Active X spin button controls can be used in their place for modification of the design.

## *Frequency*

Frequency ranges are a function of the tuner configuration. Tunable frequency range for each tuner is 2-1000 MHz without an HP E6403A, 3 GHz downconverter, and 2-3000 MHz if tuner N's configuration included a 3 GHz downconverter.

**NOTE**

The tuner specifications do not apply *below* 20 MHz. Although the readout resolution is 1 kHz, resolution down to 1 Hz is possible by numeric entry or step sizes smaller than 1 kHz. Tuning to a resolution smaller than 1 kHz will occur, but will not be displayed in the frequency text box.

## Step Size

**Step Size** is settable from 1 Hz to 10 MHz using the HP E6500A Demo GUI. The simplest method of entering a step size is to enter the desired number, followed by the first letter of the frequency suffix. For example, to enter 125 kHz, type `125k`.

## Input Attenuation

**Input Attenuation** is settable to either 0, 10, 20, or 30 dB. It can be set either by entering the desired number or using the up/down buttons. For a shared LO configuration, the Input Attenuation does not track that of tuner 1 and remains adjustable on a per tuner basis.

## *10 MHz Ref*

The **10 MHz ref** is settable to either the internal reference or an external reference. The default is internal reference. For a shared LO configuration, the 10 MHz reference is only settable for tuner 1. The remaining active tuners will track tuner 1. Note that tuner phase noise characteristics are only valid while using a clean external 10 MHz reference.

## IF Output Freq

The **IF Output Freq** is selected as per the configuration form. It is settable to either 21.4 MHz or 5.6 MHz. For a shared LO configuration, the IF Output Frequency is displayed as active on tuner 1. The remaining active tuners will track tuner 1. The IF Output Frequency is displayed only, and cannot be toggled from the HP E6500A Demo GUI.

## Preset

The **Preset** button presets the frequency, step size, and attenuation for its associated tuner. 10 MHz reference and IF Output Frequency are unaffected. For a Shared LO configuration, the Preset control is only settable for tuner 1, but controls all active tuners.

## Temp

Clicking on the **Temp** button will display a dialog box which gives the temperature for the HP E6401A of the associated tuner. The **Temp** button is active on a per tuner basis for both Shared or non-Shared LO status.

## Tuner Active

The **Tuner Active** checkbox will be grayed out, but checked for all active tuners. This is a convenience item that prevents the user from having to remember which tuners are active. This is especially useful in the Shared LO mode.

## Shared LO

The **Shared LO** checkbox will always be grayed out, but checked when the system was configured using a Shared LO.

## Driver Revision

Clicking on the **Driver Revision** button will display a dialog box which gives the current driver revision.

## Reset All

Clicking on the **Reset All** button will close all open VXI sessions, reopen new VXI sessions, and set up all tuners as configured in the Configuration Form. All normal default settings as per the Configuration Form will be applied.

## Close

Clicking on the **Close** button will close all open VXI sessions and exit the current tuner user interface. To restart an instrument session, the user would have to restart the software and set up the configuration form.

# 3 HP E6500A VXI Tuner System Description

See the “HP E6500A Simplified Block Diagram” located at the end of this chapter for a quick overview of the tuner.

The standard HP E6500A VXI tuner system consists of an HP E6401A 20 to 1000 MHz downconverter module and an HP E6402A local oscillator module. This configuration covers a specified input frequency range from 20 to 1000 MHz and is tunable down to 2 MHz. The HP E6401A translates this input signal to a 21.4 MHz IF output signal. The IF output signal has approximately 16 MHz of bandwidth. The HP E6402A module provides the 1st and 2nd LO signals for the HP E6401A module.

The HP E6500A Option 001 tuner system is similar to the standard HP E6500A except that it uses an HP E6401A Option 001 module in place of the HP E6401A module to provide a baseband output from approximately 2.5 to 9.5 MHz.

The HP E6500A Option 003 tuner system extends the input frequency range of the HP E6500A system, with the addition of an HP E6403A 1000 to 3000 MHz block downconverter (BD) module, to provide continuous frequency coverage from 20 to 3000 MHz. The HP E6403A module translates the 1000 to 3000 MHz band into the frequency range of the HP E6401A 20 to 1000 MHz downconverter module. The HP E6402A module provides the block downconverter LO signal to the HP E6403A module.

The HP E6500A Option 001, 003 tuner system combines the 20 to 3000 MHz input frequency capability of the HP E6500A Option 003 system with the baseband output capability of the HP E6500A Option 001 system.

# Tuning an HP E6500A System

When tuning an HP E6500A, usually only the frequency of the HP E6402A 1st LO is changed. If, after setting the 1st LO, it is desirable to have the IF frequency at a value other than 21.4 MHz or desirable to move the IF frequency away from filter edges, the 2nd LO frequency may be changed.

When the HP E6401A Option 001 is being used, the 2nd LO may also be changed to achieve the desired 3rd IF output.

## Tuning Equations

Listed below are the tuning equations and definition of terms used to calculate the 1st and 2nd LO frequencies to achieve the desired tuned frequency. For the HP E6500A Option 001 operation, the IF output frequency may also be calculated.

- HP E6500A System
  - 1st LO = RF + 2nd LO + 2nd IF
- HP E6500A Option 001 System
  - 1st LO = RF + Option 001 1st IF
  - 2nd LO = Option 001 1st IF - 3rd LO + 3rd IF
- HP E6500A Option 003 System
  - 1st LO
    - 1000 to 1250 MHz tuned frequency
      1st LO = $LO_{low}$ - RF + 2nd LO + 2nd IF
    - 1250 to 1800 MHz tuned frequency
      1st LO = $LO_{high}$ - RF + 2nd LO + 2nd IF
    - 1800 to 2400 MHz tuned frequency
      1st LO = RF - $LO_{low}$ + 2nd LO + 2nd IF
    - 2400 to 3000 MHz tuned frequency
      1st LO = RF - $LO_{high}$ + 2nd LO + 2nd IF

- HP E6500A Option 001, 003 System
  - 1st LO
    - 1000 to 1250 MHz tuned frequency
      1st LO = $LO_{low}$ - RF + Option 001 1st IF
    - 1250 to 1800 MHz tuned frequency
      1st LO = $LO_{high}$ - RF + Option 001 1st IF
    - 1800 to 2400 MHz tuned frequency
      1st LO = RF - $LO_{low}$ + Option 001 1st IF
    - 2400 to 3000 MHz tuned frequency
      1st LO = RF - $LO_{high}$ + Option 001 1st IF
  - 2nd LO
    - 1000 to 3000 MHz tuned frequency
      2nd LO = Option 001 1st IF - 3rd LO + 3rd IF

## Definition of Terms

**RF** is the tuned input frequency.

**1st LO** is the (approximately) 1241.4 to 2221.4 MHz output from the HP E6402A module.

**2nd LO** is the 1200 MHz +/- 5 MHz output from the HP E6402A module.

**3rd LO** is the 30 MHz output from the HP E6402A module and is used by the HP E6401A Option 001 module.

**IF output** is the 3rd IF output from the HP E6401A Option 001 module.

**1st IF** is at 1221.4 MHz and is internal to the HP E6401A module.

**Option 001 1st IF** is at approximately 1225.4 MHz and is internal to the HP E6401A Option 001 module.

**2nd IF** is at approximately 21.4 MHz and labeled as the 21.4 MHz IF Output on the HP E6401A module's front panel.

**Option 001 2nd IF** ranges from 20.5 to 27.5 MHz and is internal to the HP E6401A Option 001 module.

**3rd IF** can be tuned from 2.5 to 9.5 MHz and is the IF output from the HP E6401A Option 001 module.

**21.4 MHz** output is from the HP E6401A module and is the 2nd IF.

**BD LO freq** is the 2nd LO frequency with power adjusted for the HP E6403A block downconverter.

**$LO_{low}$** is equal to 1.25 × BD LO $_{freq}$ (approximately 1500 MHz) and is generated in the HP E6403A module.

**$LO_{high}$** is equal to 1.75 × BD LO $_{freq}$ (approximately 2100 MHz) and is generated in the HP E6403A module.

## Example: Using the Tuning Equations

Given:

3rd IF (IF output desired) = 5.6 MHz

RF = 2000 MHz

1st LO = RF - $LO_{low}$ + Option 001 1st IF

2nd LO = Option 001 1st IF - 3rd LO + 3rd IF

Solution:

2nd LO = Option 001 1st IF - 3rd LO + 3rd IF

2nd LO = 1225.4 - 30.0 + 5.6

2nd LO = 1201.0 MHz

1st LO = RF - $LO_{low}$ + Option 001 1st IF

1st LO = 2000.0 - (1.25 × 1201.0) + 1225.4

1st LO = 1724.15 MHz

## Preselector Bands

There are ten preselector bands defined for the HP E6401A downconverter module and an additional four bands defined for the HP E6403A block downconverter module.

***Table 3-1 HP E6500A Preselector Bands***

| Module | Preselector Band | Characteristic Frequency Range and Band Switching Points (MHz) |
|---|---|---|
| HP E6401A Downconverter | 1 | 40 (Low-pass filter) |
| | 2 | 40 to 60 |
| | 3 | 60 to 84 |
| | 4 | 84 to 118 |
| | 5 | 118 to 170 |
| | 6 | 170 to 230 |
| | 7 | 230 to 350 |
| | 8 | 350 to 450 |
| | 9 | 450 to 750 |
| | 10 | 750 to 1000 |
| HP E6403A Block Downconverter | 11 | 1000 to 1250 |
| | 12 | 1250 to 1800 |
| | 13 | 1800 to 2400 |
| | 14 | 2400 to 3000 |

Note: All preselector bands except 11 and 12 are frequency inverted. If HP E6401A Option 001 is present, only preselector bands 11 and 12 are frequency inverted

Each preselector band (except band 1) is suboctave, ranging in frequency by less than two-to-one from highest to lowest frequency. Using suboctave preselection decreases the chance of the second harmonic of a strong signal (at half the desired frequency) from appearing as the desired signal. Suboctave preselection also increases the second-order spurious-free dynamic range of the HP E6500A tuner.

## Calibration Factors

Each module contains an EEPROM where calibration factors are stored. These stored factors must be used by the controlling program for the tuner to meet its specifications.

## Optimizing Dynamic Range

Although internally generated spurious signals (spurs) have been minimized, it is not possible to completely eliminate them. These spurs are produced whenever harmonics of the 1st and 2nd LOs are separated in frequency by

one of the IF frequencies. Careful layout and shielding have reduced these spurs to a level well below the specifications. Although, in some cases, the spurs are still measurable.

The HP E6500A tuner has the ability to move these spurs outside of a specified subset of the maximum IF bandwidth. The spurs are relocated by moving both the 1st LO and the 2nd LO the appropriate amount so that the desired signal is centered at the IF frequency, but the spurious signal is moved off center by greater than the specified bandwidth. This procedure gives a much lower spurious level.

Equations were developed to predict which LO, IF, and tuned frequencies would produce undesired products in the pass band. To simplify their use, tables for 3 IFs were generated: 21.4 MHz for the HP E6500A; and 3.25 MHz and 5.6 MHz for the HP E6500A Option 001 systems. Three *README~x.TXT* files, stored in the *E6500/SpurTables* subdirectory on the disk, explain how the tables can be used. For the lowest spurious level possible refer to this table, located on the 3.5” disk at the front of this manual, to determine the correct setting of the 2nd LO necessary to push the spurs outside of the specified bandwidth.

In normal operation, for a desired input frequency, the 1st LO is set to the frequency dictated by the tuning equation while the 2nd LO is set to a fixed frequency. This would yield spurious levels that are lower than the specifications but still measurable.

# HP E6401A 20 to 1000 MHz Downconverter Operation

## Functions

- Attenuation
- Preselection
- Preamplification
- Upconversion
- Image filtering
- Downconversion
- Gain control

## Description

The HP E6401A 20 to 1000 MHz downconverter module converts input signals in the frequency range of 20 to 1000 MHz to a 21.4 MHz IF output frequency.

The 20 to 1000 MHz input signal path splits into two main paths, each having a solid-state 0 to 30 dB input attenuator (adjustable in 10 dB steps) to allow increased signal handling capability. Signals below 450 MHz are switched to the path that splits into eight preselector band paths (preselector bands 1 through 8). Signals above 450 MHz are switched to the path that splits into two preselector band paths (preselector bands 9 and 10). Nine of the ten preselector paths each have a filter to allow for suboctave preselection. Band 1 is not suboctave. After preselector filtering, the signal passes through a 550 MHz low-pass filter in preselector bands 1 through 8 path or a 1 GHz low-pass filter in the preselector bands 9 and 10 path. These low-pass filters offer added rejection of the 1st LO and IF signals. The two signal paths are switched into one common signal path.

**NOTE**

For the unused input path (*low path* or *high path*), the input attenuator is set to 30 dB of attenuation and the preselector switches are set for optimum isolation. (For an example of how the HP E6401A switches are set to optimize isolation, refer to the illustration “Register Control of the HP E6401A 20 to 1000 MHz Downconverter Module” at the end of Chapter 4.)

The common signal path passes through a preamplifier which compensates for losses in the preselector switches and filters. An additional 1 GHz low-pass filter follows for more LO and IF rejection. The signal is then upconverted in the first mixer to a 1st IF frequency of 1221.4 MHz. Bandpass filters provide image rejection at the 1st IF frequency. Two amplifiers in the 1st IF path compensate for loss in these filters. The 1st IF signal is downconverted to the 2nd IF frequency of 21.4 MHz in the 2nd

mixer. The signal passes through a 30 MHz low-pass filter and a final amplifier stage. Before the 21.4 MHz IF output, a solid-state 0 to 15 dB variable output attenuator, adjustable in 1 dB steps, sets the gain of the HP E6401A module to approximately +5 dB. This gain may vary over the frequency range of the IF output.

Output attenuator values for several frequencies in each preselector band are stored by the factory in each module's EEPROM. These values should be read once and stored as a table in the computer's memory. Any routine that sets the frequency should refer to this table for the correct attenuator setting.

The block downconverter input path accepts the output signal from the optional HP E6403A 1000–3000 MHz block downconverter module. This signal path has two switched filters. These filters prevent undesired mixing products from mixing with the input signal and giving the appearance of degraded IF rejection. After passing through one of the two filters, the signal is switched into the path used by preselector bands 9 and 10 just before the 1 GHz low-pass filter.

The system bandwidth is set to approximately 16 MHz by the 1st IF bandpass filters centered at 1221.4 MHz. However, other filters in the signal path can also affect the overall bandwidth. In the lower preselector bands, if the tuned frequency is near the edge of a preselector band, the stopband skirts of the preselector filter will contribute to a narrowing of the overall bandwidth. If the 1st LO is moved to a point that does not center the 1st IF at 1221.4 MHz, then the bandwidth will be lowered. Moving the 2nd LO to a frequency where the 2nd IF is closer to the edge of the 30 MHz low-pass filter will cause a narrower bandwidth.

The LO signals for the first and second mixers come from the HP E6402A. Each of the two LO signals goes through automatic level control loops to control the power at the LO port of each mixer.

## HP E6401A Option 001 Module

The HP E6401A Option 001 baseband output module converts input signals in the frequency range of 20 to 1000 MHz to a baseband IF output signal ranging from approximately 2.5 to 9.5 MHz.

To generate the baseband IF output, the 10 MHz reference in the HP E6402A LO module is tripled to create the 30 MHz 3rd LO signal. The 2nd IF in the HP E6401A Option 001 is set to an appropriate frequency to be mixed with the 3rd LO generating the desired baseband IF output.

The frequency range of the baseband IF output is limited by a high-pass and a low-pass filter. The lower 3 dB limit for the baseband IF output is set to approximately 2.5 MHz by requirements for image rejection. The upper 3 dB frequency limit is set to 9.5 MHz by a high-pass filter at the input to the third downconverter.

Image rejection is provided by the steep low-pass filter in front of the third mixer. Moving the 1st IF frequency to 1225.4 MHz gives additional rejection

at the input of the third downconverter by moving the signal closer to the edge of the 1st IF 1221.4 MHz bandpass filter. The high-pass filter at the input to the third downconverter limits exposure to signals that may cause in-band spurious responses to be generated in the mixer. The output of the mixer is amplified and sent through a 12 MHz low-pass filter to limit the 30 MHz LO signal at the output.

Gain through the Option 001 tuner system is approximately 15 dB when the correct output attenuator values are applied.

## Inputs and Outputs

### HP E6401A

- 20–1000 MHz input
- Block downconverter input (Block downconv Input), 250 to 900 MHz
- 1st LO input, approximately 1241.4 to 2221.4 MHz
- 2nd LO input 120 MHz
- 21.4 MHz IF output with +5 dB of gain

### HP E6401A Option 001

- 20–1000 MHz input
- Block downconverter input (Blk Downconv Input), 250 to 900 MHz
- 1st LO input, approximately 1241.4 to 2221.4 MHz
- 2nd LO input, approximately 1200 MHz
- 3rd LO input, 30 MHz
- IF output, approximately 2.5 to 9.5 MHz with +15 dB of gain

# HP E6402A Local Oscillator Operation

## Functions

- Synthesize 1st LO and 2nd LO
- Filtering
- Ovenized reference
- LO distribution

## Description

The HP E6402A local oscillator module provides the LO signals needed by the HP E6401A 20 to 1000 MHz downconverter, the HP E6401A Option 001 baseband output, and the HP E6403A 1000 to 3000 MHz block downconverter. The LOs are phase-locked to the 10 MHz reference. The HP E6402A module also provides reference distribution circuitry and a built-in oven-controlled crystal oscillator (OCXO).

### 2nd Local Oscillator

Synthesis starts with a narrowband voltage-controlled oscillator (VCO) tuned over a frequency range of 1200 MHz +/-5 MHz. The VCO signal is buffered and sent to one of two output signal paths. One path goes to the 2nd LO Output port: its signal drives the HP E6401A. The other path goes to the BD LO Output port: its signal drives the HP E6403A. The only difference between the 2nd LO and BD LO output signals is the power level.

### 10 MHz Reference

An internal 10 MHz OCXO is available as the frequency reference for the HP E6402A. This oscillator is *only* powered up when it is providing the 10 MHz reference (internal reference mode) for the LO module. Selection of the internal versus external reference is achieved through register control. When the internal oscillator is active, the external reference path is disabled and all the reference signals of the module will come from the internal OCXO. The oscillator is guaranteed to meet specified frequency accuracy only after it has been selected and allowed at least thirty minutes to stabilize. The output frequency of the OCXO is controlled by a digital-to-analog (DAC). The value for this DAC is generated at the factory and stored in the module's EEPROM.

The external reference input goes through a limiter and is buffered. Then the reference switched in, external or internal, is split into four paths leading to the:

- Ref TTL Out port used to lock the VXI backplane 10 MHz signal to the system reference
- Ref Out port with an attenuated version of the 10 MHz reference approximately at 0 dBm
- BD LO Output and 2nd LO Output ports
- 3rd LO Out port

The 3rd LO output is created by tripler circuitry, which takes the 10 MHz reference signal through a series of amplifiers and bandpass filters, and yields a 30 MHz fundamental signal with very low subharmonics. The 30 MHz signal is used by the HP E6401A Option 001 baseband output module.

If either of the LOs is in an unlocked state, an indicator light on the HP E6402A front panel will illuminate. Individual LO unlock information is available over the VXI bus.

## First Local Oscillator

The 1st LO provides a synthesized leveled signal from 1241.4 to 2221.4 MHz (settable to 1 Hz), nonvolatile storage (EEPROM) of calibration data, and a 10 MHz output at 0 dBm.

The VCO, labeled VCO1, produces a signal in the range of 620.7 to 1110.7 MHz. Bias of the VCO, controlled by a DAC, is aligned at the factory. Its value is stored in the EEPROM. The VCO is temperature compensated.

The VCO signal is buffered and then switched to one of three bands. Each band has an amplifier, frequency doubler, bandpass filters and three-to-one band switches. The first band ranges from approximately 1200 to 1350 MHz. The bandpass filters and amplifier in this band are used to filter out the fundamental VCO signal and submultiples of the desired signals. The amplifier helps maintain a low noise floor. The 2nd band ranges from approximately 1350 to 1675 MHz; it also needs filtering of the fundamental and submultiples of the desired signal. In addition, the bandpass filter must attenuate the noise at 1221.4 MHz (the 1st IF frequency of the HP E6401A 20 to 1000 MHz downconverter). The third band ranges from approximately 1675 to 2300 MHz; its filtering characteristics are similar to those of the second band.

After the three-to-one bandswitch, the signal is amplified and passed through an automatic leveling control (ALC) modulator. The signal then passes through a directional coupler and a splitter. A range of leveling, greater than 10 dB, compensates for changes in power versus frequency and temperature.

## HP E6402A Option 002 Module

The HP E6402A Option 002 offers dual LO output signals for two 20 to 1000 MHz downconverter modules and two 1000 to 3000 MHz block downconverter modules.

## Inputs and Outputs

### HP E6402A

- External reference input (Ext Ref In), 10 MHz
- Reference TTL output (Ref TTL Out)
- Reference output (Ref Out), 10 MHz
- Block downconverter LO output (BD LO Output), approximately 1200 MHz
- 1st LO output, approximately 1241.4 to 2221.4 MHz
- 2nd LO output, approximately 1200 MHz
- 3rd LO output, 30 MHz

### HP E6402A Option 002

- External reference input (Ext Ref In), 10 MHz
- Reference TTL output (Ref TTL Out)
- Reference output (Ref Out), 10 MHz
- Block downconverter LO output (BD LO Output), approximately 1200 MHz (dual outputs)
- 1st LO output, approximately 1241.4 to 2221.4 MHz (dual outputs)
- 2nd LO output, approximately 1200 MHz (dual outputs)
- 3rd LO output, 30 MHz

# HP E6403A 1000 to 3000 MHz Block Downconverter Operation

## Functions

- Attenuation
- Preselection
- Preamplification
- Downconversion
- Image filtering
- Gain control

## Description

The HP E6403A 1000 to 3000 MHz block downconverter module is a frequency extension module for the HP E6500A tuner system. It converts input signals in the range of 1000 to 3000 MHz down to the range of 250 to 900 MHz. This puts the signals within the tuning range of the HP E6401A downconverter module.

The 20 to 3000 MHz input path goes though a solid-state input switch. When the HP E6500A is tuned to a signal below 1000 MHz, the switch routes the input signal to the 20 to 1000 MHz Input port of the HP E6401A downconverter. When the HP E6500A is tuned to an input signal above 1000 MHz, the switch routes the signal to the HP E6403A block downconverter (BD) path.

After the input switch in the block downconverter path, there is a programmable solid-state attenuator. The attenuator can be set to 0, 10, 20, or 30 dB of attenuation. The attenuator improves the dynamic range of the receiver when large signals are present at the input. Without attenuation, large signals can overload the receiver and cause spurious responses.

After the attenuator, the signal is routed through a bank of four preselector filters (preselector bands 11 through 14), a preamplifier, and a second, identical bank of preselector filters. These filters not only provide preselection, but image rejection for the mixer, and they prevent leakage of the LO signal from the mixer out the RF input connector. Two banks of filters are used to provide the isolation necessary to achieve good image rejection and LO emissions. The preamplifier compensates for loss in the preselectors, switches, and mixer, achieving good sensitivity.

The 2nd LO signal, provided by the HP E6402A module, is routed to the HP E6403A module's BD LO input port. The HP E6403A manipulates the 2nd LO input signal of approximately 1200 MHz, generating an LO frequency of 1.25 times ($LO_{low}$) or 1.75 times ($LO_{high}$) the 2nd LO. The value of the LO frequency depends on the frequency of the input signal as follows:

***Table 3-2 Frequency Translations***

| Tuned Frequency (MHz) | HP E6403A Generated LO Frequency (Approximate) (MHz) | Block Downconverter Output Frequency (MHz) | HP E6401A Block Downconv Input Filter [1] |
|---|---|---|---|
| **1000–1250** | 1500 ($LO_{low}$) | 500–250 | BP |
| **1250**–1500 | 2100 ($LO_{high}$) | 850–600 | HP |
| 1500–**1800** | | 600–300 | BP |
| **1800**–2100 | 1500 ($LO_{low}$) | 300–600 [2] | BP |
| 2100–**2400** | | 600–900 [2] | HP |
| **2400**–2700 | 2100 ($LO_{high}$) | 300–600 [2] | BP |
| 2700–**3000** | | 600–900 [2] | HP |

**Boldface** numbers indicate preselector range

BP = bandpass, HP =high-pass

1. Refer to the illustration, "Register Control of the HP E6401A 20–1000 MHz Downconverter Module."
2. A reversed frequency spectrum exists at the block downconverter output and the 21.4 MHz output for these ranges. If the Option 001 is present, these output frequencies are the only ones not reversed.

After the second bank of filters, the input signal is downconverted in the mixer, using the HP E6403A generated LO frequency, to produce the IF output.

The IF output from the mixer is amplified and filtered to remove the image frequencies and the LO signal from the output of the mixer. The IF output goes through a programmable solid-state attenuator which corrects for the frequency response of the block downconverter. The IF output is then referred to as the block downconverter output. The attenuator settings are calibrated at the factory and stored in the module's EEPROM.

## Inputs and Outputs

- Block downconverter LO input (BD LO Input), approximately 1200 MHz
- 20 to 3000 MHz input
- Block downconverter output (Block Downconv Output), 250 to 900 MHz
- 20 to 1000 MHz output

# 4 Register-Based Programming

The information in this chapter and the HP E6500A source code provided should be used if you need to modify the driver for your application.

The HP E6500A VXI tuner system and system options consist of register-based modules. The modules use VXI A16/D16 register-based interfaces. All module functions are controlled by writing to registers located within each module. All module control registers are within VXI A16 space. While the modules use a D16 data interface, only the VXI configuration registers use the upper eight bits (data lines 8 through 15). Tuning and downconverting operations are controlled by the lower eight bits (data lines 0 through 7).

Module function is controlled directly by register outputs, by additional logic circuitry (such as serial-to-parallel converters) accessed through the registers, or by manipulating bits to emulate a serial interface. Multiple register accesses are necessary to complete module operational changes. Some of the functions are RF attenuation, preselector band selection, LO band selection, internal or external reference selection, LO frequency, LO power on or off, and IF level.

Each module incorporates an EEPROM which contains calibration data. This data must be used in order to meet specified performance. Calibrated functions include such parameters as signal gain and VCO bias.

An access LED on the front panel of each module indicates when the module is being accessed from the VXI backplane.

Register-based programming consists of reads and writes to the module registers. Writing directly to the registers can increase throughput since it eliminates the time necessary to parse commands.

**CAUTION**

Before taking direct control of the registers, review Chapter 2, “Using the Driver” in this guide. Some parts of the driver should not be modified. The source code contains sections commented with `“DO NOT MODIFY.”` Changes to these sections will invalidate support for register programming.

# Addressing the Registers

Register addresses for register-based modules are located in the upper 25% of VXI A16 address space. Every VXI module (up to 256 devices) is allocated a 32-word (64-byte) block of addresses.

Figure 4-1 shows the register address location within A16 as it might be mapped by an embedded controller. Figure 4-2 on page 4-3 shows the location of A16 address space in the HP 1406A command module.

When reading or writing to a module register, a register address may need to be specified. This address consists of a base address plus a register offset:

**Register Address = Base Address + Register Offset**

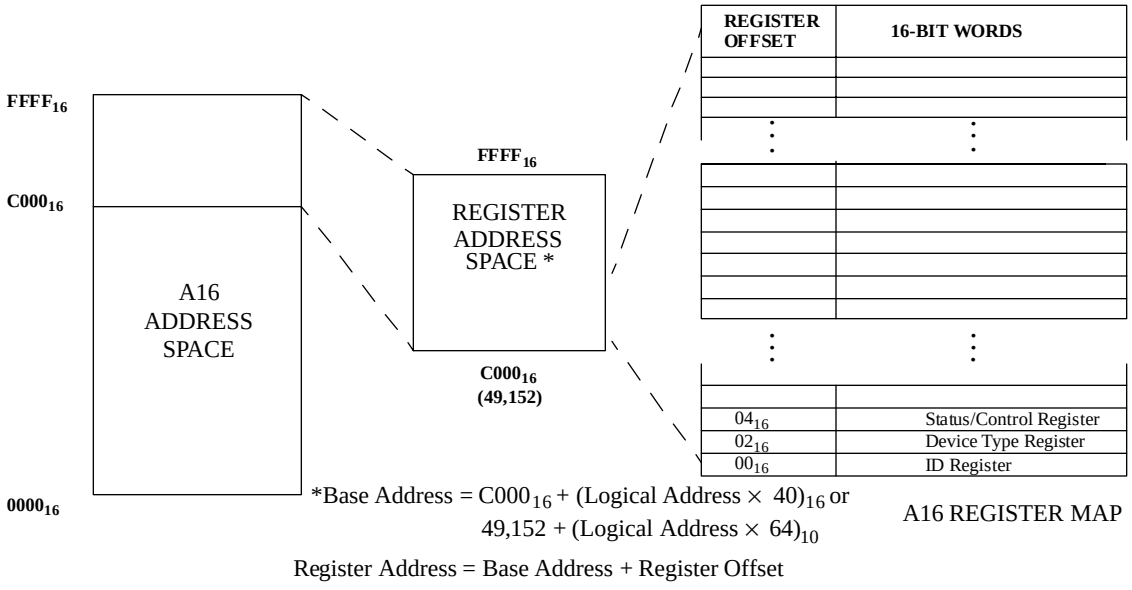


***Figure 4-1 Registers within A16 Address Space***

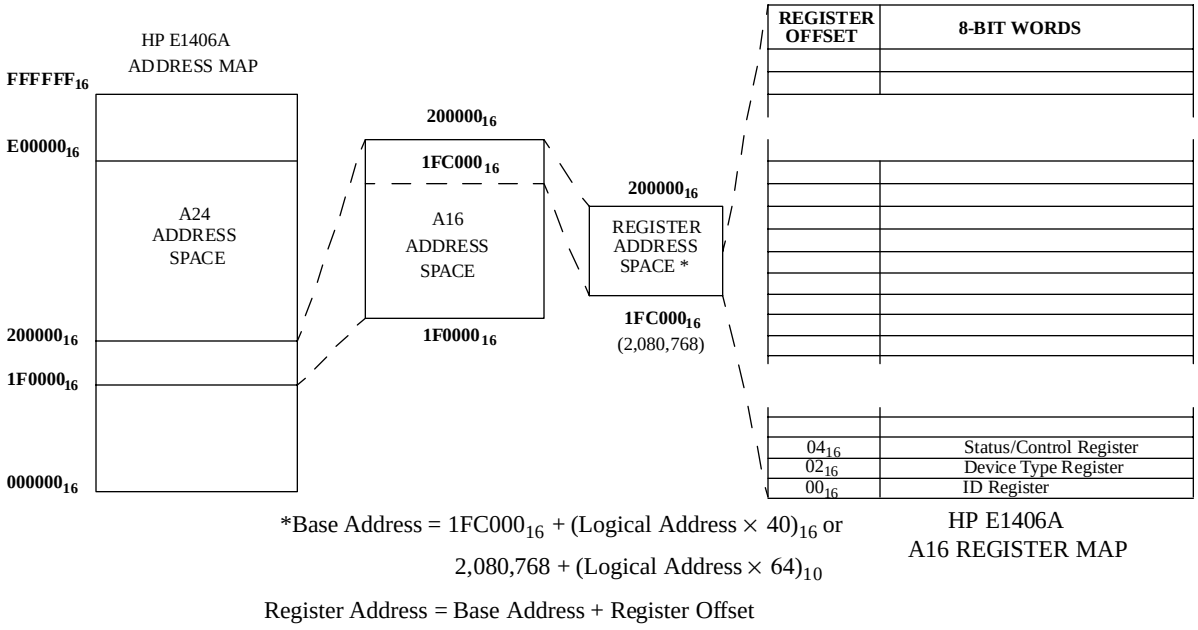


***Figure 4-2 Registers within HP E1406A A16 Address Space***

## Base Address

The base address used in register-based programming depends on whether the A16 address space is outside or inside the HP E1406A command module.

## Address Space Outside the Command Module

When the command module is not part of the VXIbus system (Figure 4-1), the module's base address depends on the command module used:

Command module address + $C000_{16}$ + $(LADDR \times 40)_{16}$ *or*

Command module address + 49,152 + $(LADDR \times 64)_{10}$

**Where:** $C000_{16}$ (49,152) is the starting location of the VXI A16 addresses

LADDR is the module's logical address

64 is the number of address bytes per register-based module.

## Address Space Inside the Command Module

When the A16 address space is inside the command module (Figure 4-2), the module's base address is calculated as follows:

$1FC000_{16} + (LADDR \times 40)_{16}$ *or*

$2{,}080{,}768 + (LADDR \times 64)_{10}$

**Where:** $1FC000_{16}$ (2,080,768) is the starting location of the register addresses

LADDR is the module's logical address

64 is the number of address bytes per VXI module.

Again, the module's factory-set logical address is 120. If the address is not changed, the module will have the following base address:

$1FC000_{16} + (120 \times 40)_{16} = 1FDE00_{16}$ *or*

$2{,}080{,}768 + (120 \times 64)_{10} = 2{,}088{,}448_{10}$

## Register Offset

The register offset is the register's location in the block of 64 address bytes. For example, if you want to read from the module's status register, you would add a register offset of $04_{16}$ (see "Overview of the Registers" in this chapter). When writing a command to this register, the offset is added to the base address to form the following register address:

$1FDE00_{16} + 04_{16} = 1FDE04_{16}$ *or*

$2{,}088{,}448_{10} + 04_{10} = 2{,}088{,}452_{10}$

# HP E6500A System Initialization

The HP E6500A system needs to be initialized before normal operation can begin. The initialization sequence involves setting each module's registers to a known state, reading calibration data specific to each module, downloading the HP E6402A instructions, and setting the LOs.

## Initialization Procedure

1. Set each module's applicable registers to the *initial register states* as shown in Table 4-4, "HP E6500A Tuner Systems' Registers," on page 4-8.
2. Read the data from each module's EEPROM. Refer to the section "Using the HP E6500A EEPROM Data" on page 4-9.
3. Download the required HP E6402A instructions into the 1st and 2nd LO synthesizers. This step is *performed by the driver only* and must not be modified.
4. Set the LOs for a tuned frequency of 100 MHz. Check for LO phase lock by reading register 44. See Table 4-19, "HP E6402A Control Interface Registers and Functions," on page 4-23.

The tuner is now ready for normal operation.

# Overview of the Registers

This section offers an overview of the registers used by the HP E6500A tuner system and optional system modules. There are three registers that are common to VXI modules and eighteen registers that are specific to the HP E6500A tuner systems.

## Conventions

- Each HP E6500A specific register is referred to by its offset from the base address and has eight data bits. For example, the register at offset 38 is referred to as register 38.
- Bit position zero represents the least significant bit (LSB).
- Basic HP E6500A tuner *systems* refer to the:
  - standard HP E6500A,
  - HP E6500A Option 001,
  - HP E6500A Option 003, and
  - HP E6500A Option 001, 003 systems

## Reading and Writing to the Registers

You can read or write to the following registers:

- Registers common to VXI modules–these are 16-bit registers
  - Manufacturer's identification register (read only)
  - Device type register (read only)
  - Status register (read only)
- Registers specific to the HP E6500A tuner systems referred to by model of module in the system–these are 8-bit registers
  - HP E6401A and HP E6401A Option 001 registers (read or write)
  - HP E6402A and HP E6402A Option 002 registers (read or write)
  - HP E6403A registers (read or write)

Each of the registers is discussed in more detail later in this chapter.

## Registers Common to Most VXI Modules

Four registers are listed in this section that are common to most VXI modules:

- Manufacturer's Identification Register
- Device Identification Register
- Status Register
- Control Register (Although common to most VXI modules, this register is *not* used by the HP E6500A tuner systems' modules.)

The manufacturer's identification (read-only) register is at offset address $00_{16}$. The return value of $FFFF_{16}$ shows Hewlett-Packard as the manufacturer and the module as an A16 register-based module.

***Table 4-1 Manufacturer's Identification Register***

| Register $00_{16}$ | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $FFFF_{16}$ | | | | | | | | | | | | | | | |

The device identification (read-only) register is at offset address $02_{16}$. To determine which module you have, you must read the device identification register which returns one of the following values:

- HP E6401A (and Option 001): $270_{16}$ or $624_{10}$
- HP E6402A (and Option 002): $271_{16}$ or $625_{10}$
- HP E6403A: $272_{16}$ or $626_{10}$

***Table 4-2 Device Identification Register***

| Register $02_{16}$ | 15–12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Unused | $270_{16}$ | | | | | | | | | | | |

The status register is at offset address $04_{16}$ and informs the user about the module's status and configuration.

***Table 4-3 Status Register***

| Register $04_{16}$ | 15 | 14 | 13–4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Read | Unused | MODID | Unused | Ready | Passed | Unused | |

## Registers Specific to the HP E6500A Tuner

Registers for the HP E6500A tuner systems are grouped by the module to which they belong.

***Table 4-4 HP E6500A Tuner Systems' Registers***

| Module | Logical Address | Register | General Function(s) | Initial Register State |
|---|---|---|---|---|
| HP E6401A 20 to 1000 MHz Downconverter and HP E6401A Option 001 Baseband Output | 42 | 8 | Enables or disables registers 32–38 | 0x00 |
| | | 32 | IF gain and EEPROM control | 0x77 |
| | | 34 | EE_data_out | NA |
| | | 36 | Switching for preselector bands 1–10 | 0xEF |
| | | 38 | Attenuation; data clock, word strobe, data input for serial-to-parallel converter (switching for preselector bands 9–14) | 0x1F |
| HP E6402A Local Oscillator and HP E6402A Option 002 Dual Outputs | 41 | 8 | Enables or disables registers 36–48 | 0x00 |
| | | 12 | Number of bits to send from the parallel-to-serial converter | NA |
| | | 14 | Starts parallel-to-serial conversion | NA |
| | | 36 | Parallel-to-serial converter | NA |
| | | 38 | Parallel-to-serial converter | NA |
| | | 40 | Parallel-to-serial converter | NA |
| | | 42 | Parallel-to-serial converter | NA |
| | | 44 | Synthesizer unlock and EEPROM data | NA |
| | | 46 | Switching for external or internal reference, switching for 1st LO bands | 0x00 |
| | | 48 | Serial shift, load, and reset | 0x30 |
| HP E6403A 1000 to 3000 MHz Block Downconverter | 40 | 8 | Enables or disables registers 40 and 42 | 0x00 |
| | | 40 | Input switching, attenuation, BD LO control | 0x04 |
| | | 42 | Preselector band switching, EEPROM clocking and negated or asserted, IF levels (gain attenuation), EE_data_in | 0x08 |

NA = initial state not applicable for the register

# Using the HP E6500A EEPROM Data

HP E6500A system data is stored in the EEPROM of each module comprising the system. This section describes the stored data and how to read the EEPROMs.

General EEPROM address and data information for the HP E6401A, HP E6402A, and HP E6403 modules is given in Table 4-5.

***Table 4-5 Information Stored in Each EEPROM***

| Starting at Address | Description | Number of Bytes | How Stored |
|---|---|---|---|
| 0 | Serial number | 10 | ASCII |
| 5 | Model number | 6 | |
| 8 | Model options | Up to 30 (End of file denoted by asterisks) | |
| 23 | Table ID | 2, Indicating the table title | |
| 24 | Table size | 2, Indicating the # of table entries | |
| 25+ | Correction table | Format is specific to each module | |

## Reading from the EEPROMs

Listed in Table 4-6 are the control lines used in retrieving EEPROM data for the HP E6401A, HP E6402A, and HP E6403 modules.

***Table 4-6 EEPROM Control Lines***

| Control Line | Active State | Description |
|---|---|---|
| EEPROM_CS[1] | 1 | Enables the EEPROM |
| EE_clk | ↑ | Clocks data in or out |
| EE_data_in | data | Inputs data to the EEPROM |
| EE_data_out | data | Outputs data from the EEPROM |

1. EEPROM_CS must be high before a rising edge on the EE_clk line occurs.

### To Initiate a Read

1. Preset the EEPROM_CS and EE_clk lines low before starting the read sequence.
2. Set the EEPROM_CS line high.
3. Send the read command ($110_2$) followed by the 8-bit address to start the read operation.
4. After the 11 bits of command and address are sent, as shown in Table 4-7 below, each rising edge on the EE_clk outputs a bit on the EE_data_out line. The first bit (during cycle 12) is a dummy bit (logical 0). The next bit is the MSB. Continued strobing of the EE_clk outputs the rest of the 16-bit word. Each word *must* be specifically addressed. Continued strobing of the EE_clk does not output the next word.

***Table 4-7 Clock Cycles Needed to Retrieve Data from the EEPROM***

| **EEPROM Clock Strobe on Rising Edge** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | … | **28** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Serial Data In/Out** | 1 | 1 | 0 | a | a | a | a | a | a | a | a | 0 | MSB | … | LSB |
| **Action** | Read command | | | Read from address | | | | | | | | | Word at address | | |
| **Data In/Out** | Serial data in | | | | | | | | | | | Serial data out | | | |
| a = address | | | | | | | | | | | | | | | |

Table 4-8 shows the EEPROM control lines and how the registers in each module map to them.

***Table 4-8 Module Specific EEPROM Control Line to Register Mapping***

| **Control Line** | **HP E6401A** | | **HP E6402A** | | **HP E6403A** | |
|---|---|---|---|---|---|---|
| | **Register** | **Data Bit Position** | **Register** | **Data Bit Position** | **Register** | **Data Bit Position** |
| EEPROM_CS | 32 | 7 | 46 | 3 | 42 | 5 |
| EE_clk | 32 | 6 | 48 | 1 | 42 | 4 |
| EE_data_in | 32 | 0 | 48 | 0 | 42 | 6 |
| EE_data_out | 34 | 0 | 44 | 7 | 40 | 0 |

## Data Stored in the Serial EEPROMS

### HP E6401A Gain Correction Data

Two gain correction tables, G1 and G2, are stored in the HP E6401A EEPROM. Table G1 contains correction values for the 20 to 1000 MHz input. Table G2 contains correction values for the block downconverter input.

Each table entry for G1 and G2 consists of four bytes. The first two bytes designate the frequency (in MHz) with the LSB indicating the start of a new preselector band. The second two bytes contain the gain correction value (in dB) at a given frequency, although only the four lower bits are used. The HP E6401A gain attenuator, used for gain correction, has 15 dB of range in 1 dB steps. The value read equals the actual attenuator setting.

#### Example: Reading the Values

- Setting the tuned frequency to 230 MHz (at the beginning of preselector band 7), the first word read is 0000000111001101:
  - LSB = 1, indicating the start of a new preselector band
  - Removing the LSB -> 000000011100110 = 230 MHz
- If the second word (gain correction value) read is 0000000000000101:
  - The value represents the actual attenuator setting of 5 dB.

### HP E6402A Calibration Data

There is one calibration table, LO, stored in the HP E6402A EEPROM which contains two pieces of calibration data for the module. This data is the VCO1 bias correction value and the 10 MHz reference offset value. See Table 4-10, “HP E6402A EEPROM Address and Data Sequence,” on page 4-13 for the HP E6402A address and data sequence.

### HP E6403A Gain Correction Data

There is one gain correction table, G3, stored in the HP E6403A EEPROM. This table contains correction values for the 1000–3000 MHz input signal range. Each entry is four bytes long. The first two bytes contain frequency (in MHz) information, with the LSB indicating if it is the start of a new preselector band. The second two bytes contain the gain correction value with only the two lower bits being used.

#### Example: Reading the Values

- Setting the tuned frequency to 2400 MHz (at the beginning of preselector band 14), the first word read is 0001001011000001:
  - LSB = 1, indicating the start of a new preselector band
  - Removing the LSB -> 000100101100000 = 2400 MHz
- The second word (gain correction value) read is 1111111111111110.

***Table 4-9 Format for HP E6401A, HP E6402A, and HP E6403A EEPROM Data***

| Table | Address | Parameter | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HP E6401A** | | | | | | | | | | | | | | | | | | |
| | 23 | Table ID (G1) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | 24 | Table size (50) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| G1 | 25 | Frequency | f | f | f | f | f | f | f | f | f | f | f | f | f | f | f | s |
| | 26 | Gain correction | x | x | x | x | x | x | x | x | x | x | x | x | g | g | g | g |
| | 27..124 | Repeat frequency and gain data | | | | | | | | | | | | | | | | |
| | 125 | Table ID (G2) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | 126 | Table size (50) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| G2 | 127 | Frequency | f | f | f | f | f | f | f | f | f | f | f | f | f | f | f | s |
| | 128 | Gain correction | x | x | x | x | x | x | x | x | x | x | x | x | g | g | g | g |
| | 129..226 | Repeat frequency and gain data | | | | | | | | | | | | | | | | |
| **HP E6402A** | | | | | | | | | | | | | | | | | | |
| | 23 | Table ID (LO) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | 24 | Table size (2) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| LO | 25 | VCO1 bias | x | x | x | x | MSB | b | b | b | b | b | b | b | b | b | b | LSB |
| | 26 | 10 MHz Ref offset | x | x | x | x | MSB | b | b | b | b | b | b | b | b | b | b | LSB |
| **HP E6403A** | | | | | | | | | | | | | | | | | | |
| | 23 | Table ID (G3) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | 24 | Table size (56) | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| G3 | 25 | Frequency | f | f | f | f | f | f | f | f | f | f | f | f | f | f | f | s |
| | 26 | Gain correction | x | x | x | x | x | x | x | x | x | x | x | x | x | x | G | G |
| | 27..136 | Repeat frequency and gain data | | | | | | | | | | | | | | | | |

Note: All available space in the HP E6401A, HP E6402A, and HP E6403A tables may not be in use.

A = decode for ASCII

b = binary decode to decimal for the number of table entries

f = binary decode to decimal for frequency

g = gain value in binary to be sent to HP E6401A AT3

G = gain value in binary to be sent to HP E6403A AT5

LSB = least significant bit

MSB = most significant bit

s = bit used for start of new preselector band: 1 indicates true

x = unused bits

The sequence for setting the HP E6402A EEPROM address and for reading module data is shown in Table 4-10. Refer to Table 4-5, “Information Stored in Each EEPROM,” on page 4-9.

***Table 4-10 HP E6402A EEPROM Address and Data Sequence***

| State | EEPROM Clock Cycle | Register | Data | Description | |
|---|---|---|---|---|---|
| Setting the EEPROM Address | Preclock condition | 48 | 0xF0 | Set to default state | |
| | | 46 | 0x08 | Enable EEPROM | |
| | | 48 | 0xF1 | Set EE_data_in = 1 | |
| | 1 | 48 | 0xF3 | Transition EE_clk, latch data | Read command |
| | | 48 | 0xF1 | EE_data = 1 | |
| | 2 | 48 | 0xF3 | Transition EE_clk, latch data | |
| | | 48 | 0xF0 | EE_data = 0 | |
| | 3 | 48 | 0xF2 | Transition EE_clk, latch data | |
| | | 48 | 0xF3 | EE_data = 0, first bit of address | |
| | 4 ..11 | (Repeat until addressing is complete) | | | |
| | **After the address is latched in:** | | | | |
| Reading Module Data | | 48 | 0xF0 | EE_data = 0 | |
| | 12 | 48 | 0xF2 | Transition EE_clk, latch data | |
| | | 44 | | Read bit 7, first read is a dummy bit, always = 0 | |
| | | 48 | 0xF0 | EE_data = 0 | |
| | 13 | 48 | 0xF2 | Transition EE_clk, latch data | |
| | | 44 | | Read bit 7, MSB of 16-bit word | |
| | | 48 | 0xF0 | EE_data = 0 | |
| | 14 | 48 | 0xF2 | Transition EE_clk, latch data | |
| | | 44 | | Read bit 7 | |
| | ..28 | (Repeat until 16 bits are read) | | | |

## Example: Reading the Module Serial Number

*Table 4-11 Example Data Read Sequence Starting at Address 0*

| Data | ASCII |
|---|---|
| 0x55 | U |
| 0x53 | S |
| 0x33 | 3 |
| 0x36 | 6 |
| 0x34 | 4 |
| 0x33 | 3 |
| 0x30 | 0 |
| 0x31 | 1 |
| 0x30 | 0 |
| 0x31 | 1 |

The data in Table 4-11 decodes to the prefix and serial number, US36430101, located on the module.

# HP E6401A 20 to 1000 MHz Downconverter Module Registers and Functions

This section includes address, function, and bit information needed to set the registers for the HP E6401A module and is HP E6401A Option 001 inclusive. For other HP E6401A details, refer to the section, "HP E6401A 20 to 1000 MHz Downconverter Operation" on page 3-7.

The "Register Control of the HP E6401A 20–1000 MHz Downconverter Module (125 MHz Frequency Shown)" illustration (Figure 4-3 on page 4-31) provides an example of the register settings necessary to activate the 125 MHz path. Register settings and logic levels required to activate other HP E6401A paths are also shown.

The factory-set logical address for the HP E6401A module, including Option 001, is 42.

## Controlling the HP E6401A Downconverter

There are ten switches and three attenuators in the HP E6401A module that are controlled through registers. The HP E6401A illustration depicts signal flow through the switches and attenuators.

Three main paths in the HP E6401A provide coverage from 20 to 1000 MHz. After passing through a number of switches and attenuators, all paths are routed through a common mixing path. The mixers and their filters are shown in the illustration "Register Control of the HP E6402A Local Oscillator Module and the HP E6401A Mixing Path (125 MHz Tuned Frequency Shown)," located at the end of this chapter.

The three paths are:

**Low path** covers the 20 to 450 MHz range using preselector bands 1 through 8 and the low path attenuator.

**High path** covers the 450 to 1000 MHz range using preselector bands 9 and 10 and the high path attenuator.

**Block downconverter path** covers the 250 to 900 MHz range using preselector bands 11 through 14. This is the path for the signal from the Block Downconverter Output port of the HP E6403A module through the HP E6401A module. This path provides additional filtering of the block downconverter output signal.

All paths share one gain attenuator and require the use of registers 32, 34, 36, and 38. Gain correction values are set through register 32. When a path is chosen, out-of-path switches and attenuators are set to optimize isolation in the unused paths.

### Low Path

The low path uses switches S7, S8, and S10 and attenuators AT2 and AT3. Switch S8 switches the signal to the low path. The signal then passes through an input attenuator AT2. A 3-to-8 multiplexer switches in one of the eight preselector band filters in the low path. After passing through the preselector band filter, the signal passes through switch S7.

### High Path

The high path uses switches S1, S2, S3, S6, and S9 and attenuators AT1 and AT3. Switch S9 switches the signal to the high path. The signal then passes through an input attenuator AT1. Switches S1, S2, and S3 direct the signal through preselector band 9 or 10, depending upon the frequency. The signal then passes through switch S6 and on to the mixing path.

### Block Downconverter Path

The block downconverter path uses switches S0, S4, S5, and S6 and attenuator AT3. The block downconverter signal passes through one of two filters, determined by S4 and S5 settings. Refer to the section, “HP E6403A 1000 to 3000 MHz Block Downconverter Module Registers and Functions” on page 4-24, for a functional description of these filters. Switch S0 is closed when using the block downconverter path and open when the low path or high path is active. Switch S6 is closed when the block downconverter path or the high path is active.

*Table 4-12 HP E6401A Control Interface Registers and Functions*

| Register and Type | Data Bit Position(s) | Active State | Label | Description | Active Input Port |
|---|---|---|---|---|---|
| 8 | | 0x00 | | Enables registers 32–38 | 20–1000 MHz or Block Downconv |
| | | 0xFF | | Disables registers 32–38 | |
| 32, Write | 0 | 1 | IF OUT (gain) | Selects 1 dB of attenuation or EE_data_in | 20–1000 MHz or Block Downconv |
| | 1 | 1 | IF OUT (gain) | Selects 2 dB of attenuation | |
| | 2 | 1 | IF OUT (gain) | Selects 4 dB of attenuation | |
| | 3 | 1 | IF OUT (gain) | Selects 8 dB of attenuation | |
| | 5,4 | | | Unused bits | |
| | 6 | ↑ | EE_clk | EEPROM control line | |
| | 7 | 1 | EEPROM_CS | EEPROM control line | |
| 34, Read | 0 | | EE_data_out | EEPROM data out | |
| | 7–1 | | | Unused bits | |
| 36, Write | 2–0 | 111 | Preselector band 1 | Selects 10–40 MHz path | 20–1000 MHz |
| | 2–0 | 000 | Preselector band 2 | Selects 40–60 MHz path | |
| | 2–0 | 001 | Preselector band 3 | Selects 60–84 MHz path | |
| | 2–0 | 010 | Preselector band 4 | Selects 84–118 MHz path | |
| | 2–0 | 011 | Preselector band 5 | Selects 118–170 MHz path | |
| | 2–0 | 110 | Preselector band 6 | Selects 170–230 MHz path | |
| | 2–0 | 101 | Preselector band 7 | Selects 230–350 MHz path | |
| | 2–0 | 100 | Preselector band 8 | Selects 350–450 MHz path | |
| | 4 | 0 | HIGH PATH | Selects high path | |
| | 5 | 0 | LOW PATH | Selects low path | |
| | 7,6,3 | | | Unused bits | |
| 38[1], Write | 0 | | | Unused bit | |
| | 1 | 1 | 20 dB HIGH PATH | Selects 20 dB of attenuation in the high path | 20–1000 MHz |
| | 2 | 1 | 10 dB HIGH PATH | Selects 10 dB of attenuation in the high path | |
| | 3 | 1 | 20 dB LOW PATH | Selects 20 dB of attenuation in the low path | |
| | 4 | 1 | 10 dB LOW PATH | Selects 10 dB of attenuation in the low path | |
| | 5 | 1 | DATA CLOCK | Rising edge clock for serial-to-parallel converter | 20–1000 MHz or Block Downconv |
| | 6 | 1 | WORD STROBE | Strobe for serial-to-parallel converter | |
| | 7 | 1 | SERIAL DATA[2] | Data bit for serial-to-parallel converter | |

1. The three most significant bits are used to program a serial register. The five least significant bits are used for other functions and must be preserved while writing to the serial-to-parallel register.

2. See the following table for functions controlled by the serial-to-parallel converter. These functions are set by a data string sent to bit 7 of register 2.

## Programming the Serial-to-Parallel Converter

Switches S0 through S7 are controlled by an 8-bit serial-to-parallel converter driven by register 38. The three lines used by register 38 for this conversion are:

- **D5, data clock:** Data is loaded on the rising edge and should be present before D5 is set to high. The clock bit should always be left in the low state.
- **D6, word strobe:** After eight bits of data are loaded, a rising edge latches the data to the switches. The word strobe bit should always be left in the low state.
- **D7, data in:** The most significant bit (MSB) is loaded first.

The states of bits 0 through 4 should be preserved while writing to the serial-to-parallel converter.

***Table 4-13 Serial-to-Parallel Settings Controlled By Register 38 Bit 7***

| Function[1] | Switches (Serial Bit) | Active State | Description | Active Input Port |
|---|---|---|---|---|
| BLOCK DOWN | 5,4,0 | 010 | BP filter (refer to HP E6403A for usage) | Block Downconv |
| | | 100 | HP filter (refer to HP E6403A for usage) | Block Downconv |
| | | 111 | Settings for isolating block downconv input from 20–1000 MHz input | 20–1000 MHz |
| HIGH PATH PRESEL | 3,2,1 | 101 | Preselector band 9 path selected (Also set *path select* bits 7 and 6, below, to $10_2$) | 20–1000 MHz |
| | | 010 | Preselector band 10 path selected (Also set *path select* bits 7 and 6, below, to $10_2$) | 20–1000 MHz |
| | | 011 | To isolate block downconv input from 20–1000 MHz input | Block Downconv |
| PATH SELECT | 7,6 | 01 | Low path selected | 20–1000 MHz |
| | | 10 | High path or block downconverter path selected | 20–1000 MHz or Block Downconv |

1. Three to four functions need to be set in registers 36 and 38 to activate any one of the frequency dependent paths.

These register settings, used to control switches in the unused paths, are provided to optimize isolation.

***Table 4-14 Optimum Settings for Unused Paths***

| Path Selected | Register | | |
|---|---|---|---|
| | 36 | 38 | Serial |
| Low | 11011ppp | sssaa111 | 01110011 |
| High | 11101011 | sss11aa1 | 1011ppp1 |
| Block Downconverter | 11101011 | sss11111 | 10bb0010 |
| p = preselector band choice | | s = control bits for serial mux | |
| a = attenuator for chosen band | | b = control bits for block downconverter filters | |

# HP E6402A Local Oscillator Module Registers and Functions

This section includes address, function, and bit information needed to set the registers for the HP E6402A and is HP E6402A Option 002 inclusive. It also includes the 1st and 2nd LO initialization procedures. Details on programming the synthesizers are not provided as these sections of the driver should not be modified. For other HP E6402A details, refer to the section, "HP E6402A Local Oscillator Operation" on page 3-10.

The "Register Control of the HP E6402A Local Oscillator Module and the HP E6401A Mixing Path (125 MHz Tuned Frequency Shown)" illustration, located at the end of this chapter, provides an example of the register settings necessary to attain the tuned frequency of 125 MHz. The 1st LO filter setting of 1350 to 1675 MHz was derived by using the tuning equations provided in "Tuning an HP E6500A System" on page 3-2. Register settings and logic levels required to activate other HP E6402A paths are also shown in the illustration.

The factory-set logical address for the HP E6402A module, including Option 002, is 41.

## Initializing and Controlling the HP E6402A LO Module

Before normal operation can begin, the HP E6402A module needs to be initialized. The procedure, below, includes reading EEPROM data, setting the VCO1 bias, and initializing the two LO synthesizers. Detailed information about the steps is given following the procedure.

The 1st LO requires a bias voltage to be set on its VCO. The bias voltage value is stored in the module's EEPROM and must be set before initializing the 1st LO. The 2nd LO does not require an independent bias setting due to its narrower operating range.

The HP E6500A tuner system uses microcontrollers to synthesize the 1st and 2nd LOs in the HP E6402A module. Before setting the two synthesizers, each must first be loaded with its respective microcode. The synthesizers are programmed serially with up to a 36-bit word. To speed synthesizer loading, data is fed to the HP E6402A eight bits at a time using up to five 8-bit parallel-to-serial registers. After the registers are loaded, the length of the word is sent to register 12. Writing 0xFF to register 14 starts the parallel-to-serial conversion.

**Module Initialization**

**Procedure**1. Set the reference to the internal or external 10 MHz reference.

2. Read the calibration information from the EEPROM for the VCO1 bias and internal reference adjust.
3. Using the EEPROM values from step 2, bias VCO1 and the offset of the internal 10 MHz reference.
4. Initialize the 1st and 2nd LOs. Refer to Chapter 2, "Using the Driver."

In normal operation, the 1st LO frequency and the 2nd LO frequency (which usually stays constant at approximately 1200 MHz) are determined by the tuned frequency. Refer to "Changing the Tuned Frequency" on page 4-28.

## Parallel-to-Serial Conversion

There are two types of devices in the HP E6402A that require serial inputs to perform their functions: the DAC which controls the oven-controlled crystal oscillator (OCXO) frequency and the VCO1 bias; and the synthesizers for the 1st and 2nd LOs. Registers 46 and 48 determine which device latches in the serial word.

To aid in sending a serial word to the devices, a parallel-to-serial converter is used. The converter consists of five 8-bit parallel-to-serial converters, which are loaded by addressing registers 36, 38, 40, 42, and the lower four bits of register 48 allowing up to a 36-bit word to be sent. Register 36 contains the most significant bit. The least significant bit depends on the word length.

When register 42 is addressed, the lower four bits of register 48 are also latched into the parallel-to-serial converter. Therefore, when inputting a 36-bit word, register 48 must be addressed before register 42 or the four bits of data from register 48 will not be latched.

The four most significant bits of register 48 control the parallel-to-serial converters and the DAC strobe, and must be set high to prevent data transfers before the data is loaded.

After the bits are fed into the parallel-to-serial converter, the device to which they will be sent is selected. The conversion process is started by sending the number of bits to register 12, then sending 0xFF to register 14.

***Table 4-15 HP E6402A Serial Data Input Using Parallel-to-Serial Conversion***

| Shift Registers Used | Number of Bits To Send To Register 12 | | | | |
|---|---|---|---|---|---|
| | **16** | **20** | **24** | **32** | **36** |
| **36** | MSB | MSB | MSB | MSB | MSB |
| **38** | LSB | ⋮ | ⋮ | ⋮ | ⋮ |

***Table 4-15 HP E6402A Serial Data Input Using Parallel-to-Serial Conversion***

| Shift Registers Used | Number of Bits To Send To Register 12 | | | | |
|---|---|---|---|---|---|
| | **16** | **20** | **24** | **32** | **36** |
| **40** | | LSB (4) | LSB | | |
| **42** | | | | LSB | |
| **48 (DB3–0)** | | | | | LSB (0) |

## Example: Programming Sequence

If the word 0x1DC851116 is sent to synthesizer1, the programming sequence of the registers would look like this:

***Table 4-16 HP E6402A Programming Sequence Example***

| Address | Data | Description |
|---|---|---|
| 48 | 0x80 | Clears serial register |
| 48 | 0x86 | Enables 36-bit transfer mode |
| 36 | 0x1D | Loads data into converter |
| 38 | 0xC8 | Loads data into converter |
| 40 | 0x51 | Loads data into converter |
| 42[1] | 0x11 | Loads data into converter |
| 48 | 0xC6 | Loads serial register from parallel input |
| 12 | 0x24 | Provides parallel input bit count |
| 14 | 0xFF | Starts parallel-to-serial conversion |
| 46 | 0x80 | Strobes serial data to synthesizer1 |
| 46 | 0x00 | Strobes serial data to synthesizer1 |

1. When addressing register 42, it will latch its data and latch in the four least significant bits of register 48.

The VCO1 bias and the internal reference offset are controlled by a DAC. The DAC requires a 16-bit serial word. Bits 0 through 2 select the DAC output, bit 3 is always low (0), and bits 4 through 15 represent the value. The word is sent using a parallel-to-serial converter. Only DAC outputs1 and 2 are used.

The VCO in the 1st LO synthesizer requires a bias voltage to be set before it will oscillate. The value for this bias is stored in the EEPROM. This value must be sent to the DAC before any synthesizer1 programming is performed. The VCO1 bias uses DAC output2.

In order for the internal reference to meet the published specification, the value in EEPROM must be sent to the reference offset DAC. The internal reference offset uses DAC output1.

VCO1 bias and reference offset are programmed only during initialization, after turning on the tuner.

***Table 4-17 Setting the VCO1 Bias and the Internal 10 MHz Reference Offset***

| Parameter | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Internal Reference | MSB | d | d | d | d | d | d | d | d | d | d | LSB | 0 | 0 | 0 | 1 |
| VCO1 Bias | MSB | d | d | d | d | d | d | d | d | d | d | LSB | 0 | 0 | 1 | 0 |

## Example: Sending the Value

As an example, a typical value for the VCO1 bias is 3610. It would be sent as follows:

***Table 4-18 HP E6402A VCO1 Programming Sequence Example***

| Register | Data | Description |
|---|---|---|
| 48 | 0xB6 | Sets up parallel-to-serial converter |
| 36 | 0xE1 | Sends MSB, 3610 = 0xE1A |
| 38 | 0xA2 | Sends least significant 4 bits, selects VCO1 bias DAC output to program |
| 12 | 0x10 | Provides parallel input bit count |
| 48 | 0xA6 | Loads serial register from parallel input |
| 48 | 0xE6 | Loads serial register from parallel input |
| 14 | 0xFF | Starts parallel-to-serial conversion |
| 48 | 0xF6 | Loads DAC serial word to its analog output |
| 48 | 0xD6 | Loads DAC serial word to its analog output |
| 48 | 0xF6 | Completes Load DAC |

## Initializing the 1st LO

The following is a listing of the registers and their data needed to start the LO synthesizer1. In general, the programming process:

1. Resets the serial outputs
2. Loads the parallel-to-serial registers
3. Shifts the parallel data to the serial registers
4. Tells the module how many bits to send to the synthesizer
5. Sends the bits

6. Strobes the synthesizer
7. Run the synthesizer

## Initializing the 2nd LO

The same process used for the 1st LO is also used for the 2nd LO. However, the values are different due to the smaller operating range of the 2nd LO.

***Table 4-19 HP E6402A Control Interface Registers and Functions***

| Register and Type | Data Bit Position(s) | Active State | Label | Description |
|---|---|---|---|---|
| 8 | | 0xFF | | Enables registers 36–48 |
| | | 0x00 | | Disables registers 36–48 |
| 12 | | | | Number of bits to send from the parallel-to-serial converter |
| 14 | | 0xFF | | Starts parallel-to-serial conversion |
| 36,38,40,42, (48) | | | | For parallel-to-serial converter |
| 44, Read | 1 | 1 | LO2 unlock | PLL unlock indicator, unlocked |
| | 5 | 1 | LO1 unlock | PLL unlock indicator, unlocked |
| | 6, 4, 3, 2, 0 | | | Unused bits |
| | 7 | | EE_data_out | Serial data from EEPROM |
| 46, Write | 0 | 1 | Run#2 | Execute command Synthesizer2 |
| | 1 | 1 | Com_strobe#2 | Serial word into Synthesizer2 |
| | 2 | 0 | HEXT | Internal reference active |
| | 2 | 1 | HEXT | Turns off internal reference, enables external reference |
| | 3 | 1 | EEPROM_CS | Enable EEPROM for read |
| | 5,4 | 00 | LO1 filter | 1st LO band < 1350 MHz |
| | 5,4 | 10 | LO1 filter | 1st LO band < 1675 MHz |
| | 5,4 | 01 | LO1 filter | 1st LO band < 2300 MHz |
| | 6 | 1 | Run#1 | Run Synthesizer1 |
| | 7 | 1 | Com_strobe#1 | Serial word into Synthesizer1 |
| 48, Write | 0 | | DB0/EE_data_in | EEPROM command and address input |
| | 1 | | DB1/EE_clk | DB3–DB0 loads into parallel-to-serial register when register 42 is addressed<br>EE_clk latches data on the rising edge |
| | 2 | | DB2 | |
| | 3 | | DB3 | |
| | 4 | 0 | LDAC_Strobe | Allows data to be clocked in. Low while serial data is being written to the DAC |
| | 5 | 0 | LLoad_dac | Outputs the value |
| | 6 | 0 | LShift | Loads serial registers from parallel inputs |
| | 7 | 0 | LReset | Clears the serial registers |

# HP E6403A 1000 to 3000 MHz Block Downconverter Module Registers and Functions

This section includes address, function, and bit information needed to set the registers for the HP E6403A module. For other HP E6403A details, refer to the section, "HP E6403A 1000 to 3000 MHz Block Downconverter Operation" on page 3-13.

The "Register Control of the HP E6403A 1000 to 3000 MHz Block Downconverter Module (1350 MHz Tuned Frequency Shown)" illustration, located at the end of this chapter, provides an example of the register settings necessary for a tuned frequency of 1350 MHz. Register settings and logic levels required to activate other HP E6403A paths are also shown.

The factory-set logical address for the HP E6403A module is 40.

## Controlling the HP E6403A Block Downconverter

The HP E6403A downconverts a 1000 to 3000 MHz input signal producing an output signal ranging from 250 MHz to 900 MHz. The HP E6401A downconverts this HP E6403A output to produce an output IF frequency. The HP E6403A provides suboctave preselection of the tuned frequency.

Registers 40 and 42 control the HP E6403A switches and attenuators. The input signal passes through S18 which switches the signal to either the HP E6401A (for 20 to 1000 MHz input signals) or the input attenuator AT4 in the HP E6403A (for 1000 to 3000 MHz input signals). The attenuator provides 30 dB of attenuation in 10 dB steps. Each step is independent of the others and should not be combined to give values other than those listed.

Register 42 controls the preselector and sets the HP E6403A gain. The output of AT4 passes through the preselector and is fed into the mixer. The mixer uses an LO of either 1500 or 2100 MHz. See Table 4-20, "HP E6403A Register and HP E6401A Serial-to-Parallel Converter Settings," on page 4-25. The mixer output signal passes through the gain attenuator AT5 and becomes the HP E6403A block downconverter output signal.

***Table 4-20 HP E6403A Register and HP E6401A Serial-to-Parallel Converter Settings***

| Tuned Frequency (MHz) | Block Downconverter Output (MHz) | HP E6403A Mixing LO (MHz) | HP E6403A Register 40 | HP E6403A Register 42 | HP E6401A Block Downconv Input Filter (MHz) | HP E6401A Serial-to-Parallel Converter |
|---|---|---|---|---|---|---|
| < 1000 | none | out | 11111111 | 00001111 | out | nn11nnn1 |
| 1000–1250 | 500–250 | 1500– | 10tt0t01 | gg000111 | (BP) 250–650 | 10101110 |
| 1250–1500 | 850–600 | 2100– | 00tt0t10 | gg001011 | (HP) 500 | 10011110 |
| 1500–1800 | 600–300 | | | | (BP) 250–650 | 10101110 |
| 1800–2100 | 300–600 | –1500 | 10tt0t01 | gg001101 | (BP) 250–650 | 10101110 |
| 2100–2400 | 600–900 | | | | (HP) 500 | 10011110 |
| 2400–2700 | 300–600 | –2100 | 00tt0t10 | gg001110 | (BP) 250–650 | 10101110 |
| 2700–3000 | 600–900 | | | | (HP) 500 | 10011110 |

t = bit settings for AT4 attenuation

n = settings for HP E6401A tuned frequency

g = bit settings for AT5 gain correction values read from EEPROM

Table 4-21 shows the bits that need to be set to change attenuator settings for AT4 and AT5.

***Table 4-21 HP E6403A Attenuator Settings***

| Attenuation | AT4 | AT5 |
|---|---|---|
| 0 dB | pp01s1pp | |
| 10 dB | pp10s0pp | |
| 20 dB | pp11s0pp | |
| 30 dB | pp11s1pp | |
| Read from EEPROM | | gg00pppp |

p = previous state

g = bit settings for AT5 gain correction values read from EEPROM

s = switch S18

## Procedure for Applying HP E6401A and HP E6403A Correction Data

When using the HP E6401A and HP E6403A in the 1000 to 3000 MHz range, correction values for both modules must be used. In the HP E6401A, table G2 is used when the block downconverter is active. Table G2 values refer to the block downconverter output frequency, *not* the tuned frequency.

1. Look up the correction value for the tuned frequency from table G3 data stored in the HP E6403A module's EEPROM.
2. Send the correction value to HP E6403A AT5.
3. Calculate the block downconverter output frequency by subtracting the tuned frequency from the HP E6403A mixing LO frequency (found in the HP E6403A register settings table above).

## Example: Applying Correction Data

Tuned frequency = 1400 MHz

Block downconverter output frequency is

2100 to 1400 = 700 MHz

4. Look up the correction value, unique to each module, for the block downconverter output frequency in the HP E6401A module's table G2.
5. Send the correction value to HP E6401A AT3.

***Table 4-22 HP E6403A Control Interface Registers and Functions***

| Register and Type | Data Bit Position(s) | Active State | Label | Description |
|---|---|---|---|---|
| 8 | | 0x00 | | Enables registers 40 and 42 |
| | | 0xFF | | Disables registers 40 and 42 |
| 40, Write | 3 | 1 | S18 | Input switch, 20–1000 MHz |
| | 3 | 0 | S18 | Input switch, 1000–3000 MHz |
| | 5,4,2 | 011 | AT4 | Selects 0 dB of attenuation |
| | **5**,4,2[1] | 100 | AT4 | Selects 10 dB of attenuation |
| | 5,**4**,2 | 110 | AT4 | Selects 20 dB of attenuation |
| | 5,4,**2** | 111 | AT4 | Selects 30 dB of attenuation |
| | 6 | 0 | S17 | LO power on |
| | 6 | 1 | S17 | LO power 0ff |
| | 7,1,0 | 101 | S14, S16, S15 | LO band 1.25 × LO, (BP) 1500 MHz, (BP) 2100 MHz[2] |
| | 7,1,0 | 010 | S14, S16, S15 | LO band 1.75 × LO, (BP) 1500 MHz, (BP) 2100 MHz[2] |
| 42, Write | 3–0 | 1111 | S19–S22 (Open) | Preselector band < 1000 MHz |
| | 3–0 | **0**111 | S19 | Preselector band 11 |
| | 3–0 | 1**0**11 | S20 | Preselector band 12 |
| | 3–0 | 11**0**1 | S21 | Preselector band 13 |
| | 3–0 | 111**0** | S22 | Preselector band 14 |
| | 4 | ↑ | EE_clk | EEPROM clock high |
| | 5 | 1 | EEPROM_CS | EEPROM_CS asserted |
| | 7,6 | 00 | AT5 | IF level[3] (minimum attenuation) |
| | 7,6 | 01 | AT5 | IF level |
| | 7,6 | 10 | AT5 | IF level |
| | 7,6 | 11 | AT5 | IF level (maximum attenuation) |

1. Bit in bold is associated with that specific switch or attenuator step.

2. For a 1000 to 3000 MHz tuned frequency either the 1500 MHz or the 2100 MHz filter is used. (Refer to the table in this section entitled “HP E6403A Register and HP E6401A Serial-to-Parallel Converter Settings.”) For a tuned frequency of less than 1000 MHz neither filter is used.

3. For correct operation, the IF level values should be read from the EEPROM.

# Changing the Tuned Frequency

In general, the frequencies for the 1st and 2nd LOs in the HP E6402 LO module should be set before any other module is addressed. The other modules may be programmed while the LOs are settling. When the tuned frequency is changed, the gain attenuator(s) may need to be reprogrammed.

To change the tuned frequency, the following events must occur:

- Using the "Tuning Equations" on page 3-2 and page 3-3, calculate the 1st LO frequency and possibly the 2nd LO frequency generated in the HP E6402A module.

  First LO and 2nd LO frequencies are calculated.

  In most cases, the 2nd LO's frequency is not changed when setting the tuned frequency and so will not need reprogramming after initialization. The 2nd LO is retuned only for minimization of internally generated spurious responses.
- Program the 1st LO (2nd LO if necessary)
- Change the preselector path settings

  If the new tuned frequency is out of range of the preselector path previously chosen, select a new preselector path.
- Maintain system gain

  Within a preselector range, gain changes are typically less than 4 dB. Small changes in frequency may not require the gain value to be rewritten. There are between three and seventeen gain correction values per preselector path.
- Set the input attenuators, according to the path selected, to maintain desired attenuation and isolation for the tuner system.

  When changing paths, a different input attenuator may be used. Input attenuation for the unused paths should be set to 30 dB. Input attenuation in the active path should be set to minimize spurious responses.

# 10 MHz Internal Reference Timebase Adjustment

The 10 MHz internal reference can be adjusted to compensate for long-term drift. It is recommended that the internal reference be on for at least 24 hours before changing the offset from the factory value. Refer to Table 4-18 on page 4-22 for the register programming sequence.

## Adjustment Procedure

1. Set the tuner for an input frequency of 1000 MHz. This will set the 1st LO to 2221.4 MHz. If your system includes Option 001, you will need to calculate the frequency of the 1st LO based on the final IF out, and any offset to the 2nd LO. Refer to the “Definition of Terms” and “Tuning Equations” sections in this chapter.
2. Measure the frequency of the 1st LO using an instrument with better than $1 \times 10^{-8}$ accuracy.
3. Change the value of the reference offset DAC until the 1st LO frequency is within the specification. Generally, a DAC value change of 1000 gives a frequency change of 25 ppm.
4. Record the final DAC value. If you are using the driver provided, enter the value in the `E6500.ini` file. If you are not using the driver provided, send the value whenever the system is powered up.

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FOLD OUT

bde6401

***Figure 4-3 Register Control of the HP E6401A 20 to 1000 MHz Downconverter Module***

BACK OF FOLD OUT

FOLD OUT

bde6402

***Figure 4-4 Register Control of the HP E6402A Local Oscillator Module and the HP E6401A Mixing Path***

BACK OF FOLD OUT

FOLD OUT

bde6403

***Figure 4-5 Register Control of the HP E6403A 1000 - 3000 MHz Block Downconverter Module***

# 5 Specifications

This chapter contains specifications, characteristics, and typical performance parameters for the HP E6500A VXI tuner, the HP E6500A Option 001 (baseband output) VXI tuner, and the HP E6500A Option 003 (3000 MHz extension) VXI tuner.

Specifications apply only to the HP E6500A *system-level* configuration. A minimum system consists of the two-module set: the HP E6401A downconverter and the HP E6402A local oscillator. Values given are specifications unless labeled as characteristic or typical.

Specifications are not available at the individual HP E6400-series VXI *module* level.

## Definition of Terms

**Specifications** describe warranted performance over the temperature range of 0 °C to 55 °C after a 30-minute warmup from ambient conditions.

**Typical** refers to test data at the 50th percentile (averaged over the frequency range) and 25 °C. Typical indicates non-warranted performance parameters.

**Characteristics** describe product performance for parameters that are not subject to variation, not measurable, verifiable through functional pass or fail tests, or are not routinely measured. Characteristic performance parameters are non-warranted.

**NOTE**

Specifications are valid *only* if the modules are housed in an Hewlett-Packard VXI mainframe. (HP E1421B and HP E1401B mainframes are recommended.)

# Frequency-Related Specifications

| | |
|---|---|
| **Frequency Range** [1] | 20 to 1000 MHz (HP E6500A)<br>20 to 3000 MHz (HP E6500A Option 003) |
| **Tuning Resolution** | 1 Hz |
| **Synthesizer Tuning Speed**<br>(Characteristic) | 1 ms (10 kHz settling)<br>2 ms (1 kHz settling)<br>4 ms (100 Hz settling)<br>[Data derived from register-based programming] |
| **Tuning Accuracy (Center frequency × reference accuracy)** | |
| Internal OCXO Reference Accuracy | $1 \times 10^{-6}$/yr [2] |
| External Reference Input | Requires 10 MHz reference signal with level 0 dBm +/-3 dB |

1. The HP E6500A is tunable down to 2 MHz. Specifications, characteristics, and typicals do not apply below 20 MHz.

2. A procedure for the "10 MHz Internal Reference Timebase Adjustment" is given on page 4-29.

**RF Preselection**

| **Preselector Band** | **Frequency Range (MHz)**<br>Characteristic |
|---|---|
| **1** | 40 (Low-pass filter) |
| **2** | 40 to 60 |
| **3** | 60 to 84 |
| **4** | 84 to 118 |
| **5** | 118 to 170 |
| **6** | 170 to 230 |
| **7** | 230 to 350 |
| **8** | 350 to 450 |
| **9** | 450 to 750 |
| **10** | 750 to 1000 |
| **11** | 1000 to 1250 |
| **12** | 1250 to 1800 |
| **13** | 1800 to 2400 |
| **14** | 2400 to 3000 |

# Amplitude-Related Specifications

| Input Parameters | |
|---|---|
| **RF Input Impedance** (Characteristic) | 50 ohms |
| **RF Input Connector** | SMA |
| **Input VSWR** (Typical) | 2:1 |
| **Maximum Input without Damage** (Characteristic) | |
| Average Continuous RF Power | +20 dBm |
| DC Voltage | 20 volts |
| **RF Input Attenuation** (Characteristic) | 0 dB to 30 dB in 10 dB steps |

| Dynamic Range Parameters | |
|---|---|
| **Noise Figure** (Typical) | 10 dB (20 to 1000 MHz) [1]<br>14 dB (1000 to 3000 MHz) [1] |
| **Intermodulation: Second Order** | |
| Second Order Intercept (SOI) | +40 dBm |
| **Intermodulation: Third Order** (Typical) | |
| Third Order Intercept (TOI) | +15 dBm, 20 MHz spacing |
| Narrowband Intermodulation (For 2 signals at -20 dBm and 125 kHz spacing) | -64 dBc |
| **Image Rejection** | 95 dB |
| **IF Rejection** | 90 dB |
| **Phase Noise at 20 kHz Offset** (Characteristic) | -100 dBc/Hz |
| **Internally Generated Spurious (Typical)** | <-100 dBm, equivalent input |
| **LO Emissions** | -110 dBm (HP E6500A)<br>-100 dBm (HP E6500A Option 003) |

1. The HP E6500A Option 001 noise figure values are also 10 dB and 14 dB, but are considered characteristic.

| IF Output Parameters | |
|---|---|
| **21.4 MHz IF Output** [1] | |
| Bandwidth, 3 dB (Characteristic) | 16 MHz, BW will be reduced at preselector band switching points |
| RF-to-IF Gain (Typical) | 5 dB [2] |
| **Baseband Output (HP E6500A Option 001)** [3] | |
| Bandwidth, 3 dB (Characteristic) | 2.5 to 9.5 MHz |
| RF-to-IF Gain (Typical) | 15 dB [2] |

**Note: The HP E6500A Option 001 does not include a 21.4 MHz output.**

1. Spectral information is inverted for signals in all bands except bands 11 and 12. See the “RF Preselection” table in this chapter.
2. This parameter is valid when correction factors are applied. The table is read from the HP E6401A and HP E6403A (if using the HP E6500A Option 003) modules.
3. Spectral information is inverted only for signals in bands 11 and 12. See the “RF Preselection” table in this chapter.

# Physical Characteristics

| Front Panel Connectors | |
|---|---|
| **HP E6401A 20–1000 MHz Downconverter Module** | 20–1000 MHz Input, SMA female<br>Block Downconv Input, SMA female<br>1st LO Input, SMC male<br>2nd LO Input, SMC male<br>21.4 MHz IF Output, SMB male |
| **HP E6401A Option 001 (Baseband Output) Module** | 20–1000 MHz Input, SMA female<br>Block Downconv Input, SMA female<br>1st LO Input, SMC male<br>2nd LO Input, SMC male<br>3rd LO Input, SMB male<br>IF Output [1], SMB male |
| **HP E6402A Local Oscillator Module** | Ext Ref In, SMB male<br>Ref TTL Out, SMB male<br>Ref Out, SMB male<br>BD LO Output, SMC male<br>1st LO Output, SMC male<br>2nd LO Output, SMC male<br>3rd LO Output, SMB male |
| **HP E6402A Option 002 (Dual LO Output) Module** | Ext Ref In, SMB male<br>Ref TTL Out, SMB male<br>Ref Out, SMB male<br>BD LO Output, SMC male (2)<br>1st LO Output, SMC male (2)<br>2nd LO Output, SMC male (2)<br>3rd LO Output, SMB male |
| **HP E6403A 1000–3000 MHz Block Downconverter Module** | BD LO Input, SMC male<br>20–3000 MHz Input, SMA female<br>Block Downconv Output, SMA female<br>20–1000 MHz Output, SMA female |

1. IF Output refers to the 2.5 to 9.5 MHz baseband output.

| | Weight (Characteristic) |
|---|---|
| **HP E6500A Tuner System** | 12 lb 10 oz (5.8 kg) |
| **HP E6500A Option 003 Tuner System** | 18 lb 8 oz (8.5 kg) |
| **HP E6401A Module** | 5 lb 14 oz (2.7 kg) |
| **HP E6401A Option 001 Module** | 6 lb 7 oz (2.9 kg) |
| **HP E6402A Module** | 6 lb 12 oz (3.1 kg) |
| **HP E6402A Option 002 Module** | 6 lb 12 oz (3.1 kg) |
| **HP E6403A Module** | 5 lb 14 oz (2.7 kg) |

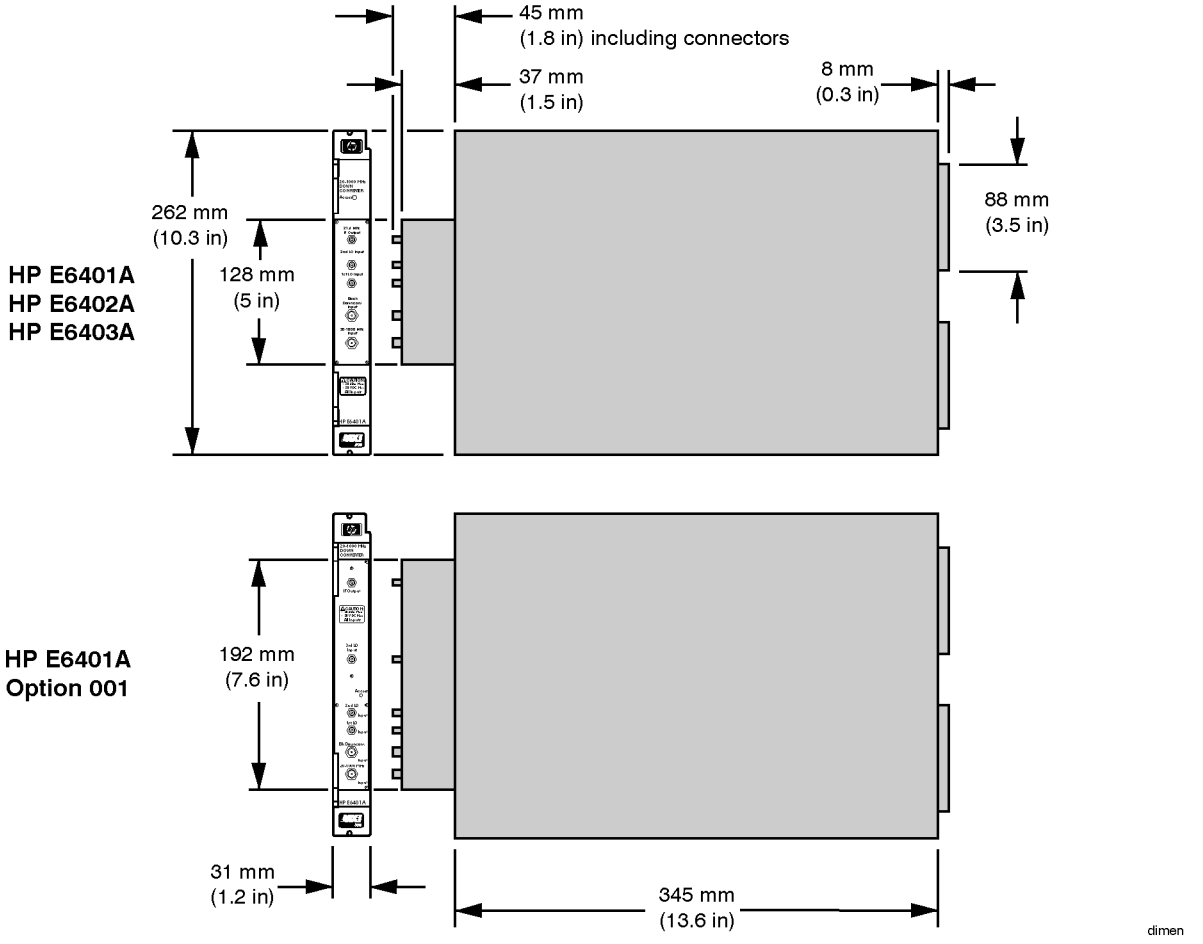


***Figure 5-1 Dimensions of the HP E640xA Modules Comprising the HP E6500A VXI Tuner System***

# General Information

**Power Requirements**

(Characteristic)

| | |
|---|---|
| **HP E6500A Tuner System** | 36 watts |
| **HP E6500A Option 003 Tuner System** | 50 watts |

HP E6500A Option 001 power consumption of 1.5 watts is included in the values listed in this table.

**Power Requirements**

(Characteristic)

| Module | +5 Vdc | –5.2 Vdc | +24 Vdc | –24 Vdc |
|---|---|---|---|---|
| **HP E6401A** | | | | |
| DC Current | 0.48 A | 0.34 A | 0.58 A | 0.022 A |
| Dynamic Current | 0.10 A | 0.07 A | 0.10 A | 0.00 A |
| **HP E6401A Option 001** | | | | |
| DC Current | 0.74 A | 0.39 A | 0.58 A | 0.021 A |
| Dynamic Current | 0.16 A | 0.09 A | 0.10 A | 0.00 A |
| **HP E6402A** | | | | |
| DC Current | 0.75 A | 0.012 A | 1.035 A | 0.124 A |
| Dynamic Current | 0.17 A | 0.00 A | 0.19 A | 0.02 A |
| **HP E6403A** | | | | |
| DC Current | 0.935 A | 0.341 A | 0.361 A | 0.161 A |
| Dynamic Current | 0.21 A | 0.08 A | 0.06 A | 0.03 A |

# Environmental Information

| | |
|---|---|
| **System Operating Temperature** | 0 ° C to 55 ° C |
| **System Calibration Interval** | Two years |

**Cooling/Slot**
**For 10 ° C Rise**
(Characteristic)

| **Module** | **Air Flow** (liters/second) | **DeltaP** (mm $H_2O$) |
|---|---|---|
| **HP E6401A** | 0.33 | 1.40 |
| **HP E6401A Option 001** | 0.30 | 1.25 |
| **HP E6402A** | 0.64 | 1.18 |
| **HP E6403A** | 0.32 | 1.39 |

# VXI Information

| | |
|---|---|
| **VXI Control** | Register-based commands<br>(Windows NT driver examples are also provided. VXI plug-and-play drivers are not available.) |
| **Module Size** | VXI C-size |
| **Slots Used** | Two slots (HP E6500A)<br>Three slots (HP E6500A Option 003) |
| **VXI Interface** | Requires a slot zero controller, such as a command module or MXI module. (Not included) |

# Index


**A**

accessories supplied, 1-22
address switches. See logical address switches
addressing registers, 4-2

**B**

baseband output (HP E6500A Option 001)
  defined, 1-1
  specification, 5-4
BD LO freq
  defined, 3-3

**C**

cables. See accessories supplied
calibration factors
  EEPROMs, 3-5
characteristics
  definition, 5-1
command module, 4-3
controlling
  registers, 4-15, 4-19, 4-24
  requirements, 1-1
cooling/slot, 5-8

**D**

driver
  part number, 1-22
dynamic range
  1st and 2nd LO settings, 3-5
  internally generated spurious signals, 3-5
  optimization, 3-5
  README.TXT files, 3-5

**E**

EEPROMs
  calibration factors, 3-5
  clock cycles, 4-10
  control lines, 4-10
  data, 4-9
  format, 4-12
  HP E6402A address and data sequence, 4-13
  internal reference offset, 4-21
  reading, 4-9, 4-10
  use of, 4-1
  VCO1 bias, 4-21
electrostatic discharge (ESD)
  preventing, 1-23
  static-safe accessories, 1-24
external 10 MHz reference
  switching, 3-10

**F**

first (1st) IF
  defined, 3-3
first (1st) LO
  defined, 3-3
  description, 3-11
  initializing, 4-22
  unlock, 4-23
frequency range specification, 5-2

**H**

HP E3238S with HP E6500A Option 001, 003
  configuration, 1-19
  information, 1-19
HP E6401A
  accessories, 1-22
  attenuation, 3-7, 4-15
  cables, 1-22
  controlling, 4-15
  description, 3-7
  factory-set logical address, 4-15
  front panel features, 1-4
  functions, 3-7
  gain correction data, 4-11
  inputs and outputs, 3-9, 3-12
  preselector filtering, 3-7
  registers and functions, 4-15
  serial-to-parallel conversion, 4-18
  signal flow, 3-7
  switching, 3-7, 4-15, 4-18
HP E6401A Option 001
  accessories, 1-22
  baseband output, 3-8
  cables, 1-22
  description, 3-8
  factory-set logical address, 4-15
  filtering, 3-8
  front panel features, 1-6
  registers and functions, 4-15
HP E6402A
  accessories, 1-22
  cables, 1-22
  calibration data, 4-11
  controlling, 4-19

description, 3-10
factory-set logical address, 4-19
front panel features, 1-8
functions, 3-10
initializing, 4-19, 4-22, 4-23
inputs and outputs, 3-12
internal 10 MHz reference, 3-10
parallel-to-serial conversion, 4-20
preselector filtering, 3-11
signal flow, 3-10
switching, 4-23
voltage-controlled oscillator (VCO) 1st LO, 3-11, 4-21
voltage-controlled oscillator (VCO) 2nd LO, 3-10
HP E6402A Option 002
accessories, 1-22
cables, 1-22
factory-set logical address, 4-19
front panel features, 1-10
HP E6403A
accessories, 1-22
attenuation, 3-13, 4-24, 4-25, 4-27
block downconverter output, 3-14
cables, 1-22
controlling, 4-24
correction data procedure, 4-26
description, 3-13
factory-set logical address, 4-24
front panel features, 1-12
functions, 3-13
gain correction data, 4-11
inputs and outputs, 3-14
mixing LO, 4-25
preselector filtering, 3-13
signal flow, 3-13
switching, 3-13, 4-24, 4-27
HP E6500A
cable part numbers, 1-15
cabling configuration, 1-15
controlling, 1-1
defined, 1-1, 3-1
EEPROM data, 4-9
initialization, 4-5
input (tuned) frequency, 1-1
installation, 1-28
operator's check, 1-29
options, 1-14
output frequency, 1-1
preparation for use, 1-25
registers, 4-8
slot zero, 1-1
system configuration, 1-15
tuning equations, 3-2
HP E6500A Operator's Check
procedure, 1-29
test equipment required, 1-29
HP E6500A Option 001
baseband output, 1-1
cable part numbers, 1-16
cabling configuration, 1-16
defined, 1-1, 3-1
input (tuned) frequency, 1-1
output frequency, 1-1
system configuration, 1-16
tuning equations, 3-2
HP E6500A Option 001, 003
defined, 1-1, 3-1
input (tuned) frequency, 1-1
output frequency, 1-1
tuning equations, 3-3
HP E6500A Option 003
cable part numbers, 1-17
cabling configuration, 1-17
defined, 1-1
input (tuned) frequency, 1-1
output frequency, 1-1
system configuration, 1-17
tuning equations, 3-2
HP E6500A Option 006
configuration, 1-20
HP E6500A Option 013
configuration, 1-21
HP E6500A VXI Tuner User's Guide
part number, 1-22

**I**

IF output
defined, 3-3
IF rejection, 5-3
image rejection, 5-3
initial inspection
damage, 1-2
instructions, 1-2
shipping container, 1-2
input VSWR (typical), 5-3
installation
module, 1-28
system, 1-28
intermodulation
second order, 5-3
third order, 5-3
internal 10 MHz reference
bias, 3-10
offset, 4-21
offset value, 4-11
oven-controlled crystal oscillator, 3-10
powered on, 3-10
timebase adjustment, 4-29
internally generated spurious, 5-3

**L**

LO emissions, 5-3
logical address switches
  illustrated, 1-27
  setting, 1-26

**M**

mainframes
  HP E1401B, 1-21
  HP E1421B, 1-20
maximum input without damage (characteristic), 5-3
module size, 5-9

**N**

noise figure (typical), 5-3

**O**

option 001 1st IF
  defined, 3-3
option 001 2nd IF
  defined, 3-3
options
  module, 1-3
  system, 1-14

**P**

phase noise at 20 kHz offset (characteristic), 5-3
power requirements (characteristic), 5-7
preselector bands
  defined, 3-5
  HP E6401A, 3-7
  suboctave, 3-5

**R**

registers
  addressing, 4-2
  attenuation, 4-17
  base address, 4-3
  control, 4-7
  device identification, 4-7
  manufacturer's identification, 4-7
  offset, 4-4, 4-6
  parallel-to-serial conversion, 4-20
  preselector bands, 4-17
  reading and writing, 4-6
  serial-to-parallel conversion, 4-18
  status, 4-7
  switching, 4-17
RF
  defined, 3-3
RF input attenuation (characteristic), 5-3
RF input connector, 5-3
RF input impedance (characteristic), 5-3

**S**

second (2nd IF)
  defined, 3-3
second (2nd) LO
  defined, 3-3
  description, 3-10
  initializing, 4-23
  unlock, 4-23
slot 0, 1-28
slots used, 5-9
specifications
  definition, 5-1
spurious signals. See dynamic range
synthesizer tuning speed (characteristic), 5-2
system bandwidth, 3-8
system calibration interval, 5-8
system operating temperature, 5-8
system, tuner. See HP E6500A system and options

**T**

third (3rd) IF
  defined, 3-3
third (3rd) LO
  defined, 3-3
  described, 3-11
tuned frequency, changing, 4-28
tuner system. See HP E6500A system and options
tuning accuracy, 5-2
tuning equations. See HP E6500A system and options
tuning resolution specification, 5-2
typical
  definition, 5-1

**V**

voltage-controlled oscillator (VCO). See HP E6402A voltage-controlled oscillator (VCO)
VXI control, 5-9
VXI interface, 5-9

**W**

weight (characteristic), 5-6