Porting E1430A software to the E1437A

The E1437A library was designed for compliance to the VXI Plug & Play standard. Because of this and some functional hardware differences between the modules, the library interfaces are different. Some of the key differences are:

1. The E1437 register level interface is not documented for direct end user access. The only direct access is to the status register via hpe1437_status_get.

2. The E1437 library does not manage modules in groups. To program multiple modules, a separate I/O session must be opened for each module. The programmer may establish his/her own ID array for controlling a set of modules as a group. The programmer is responsible for looping through the array with function calls intended for multiple modules. This approach provides substantially more flexibility than the approach used in the E1430 library. It also allows for consistency with the VXI Plug&Play specification, and allows programming with environments such as HP-VEE.

3. Explicit "try-recover" error trapping is not supported. Instead the VXI Plug & Play error reporting scheme is used. This does not include bus error trapping.

4. Some of the more obscure E1430 functions were dropped in the E1437. One of these is concurrent output of multiple digital filter outputs, the multipass mode. A second is the ability to reread the same data a second time from the output FIFO. A third is to set the magnitude trigger bandwidth independently from the signal bandwidth. A fourth is the ability to program the input DC offset.

5. The E1437 added substantially more flexibility in the generation and sharing of the ADC clock, and synchronizing multiple module local oscillators and decimation filters.

6. The post-processing functions for re-filtering and resampling data have been moved to a separate hpdsp library. This library includes additional useful functions for filter synthesis and FFT processing.

The first step in porting E1430A software to the E1437A is to replace the existing function calls with the corresponding one from the following table. Check the library documentation to adjust the function parameters accordingly. If the target system uses multiple modules, the code must then be modified to explicitly handle the initialization and management of the modules. Read the documentation on the use of the hpe1437_filter_sync and hpe1437_frequency_sync functions to manage the synchronization of multiple modules.

e1430_abort_meas	hpe1437_meas_control
e1430_arm_module	hpe1437_meas_start
e1430_autozero	hpe1437_input_autozero
e1430_auto_range	hpe1437_input_range_auto
e1430_create_module_group	hpe1437_init
e1430_debug_level	
e1430_delete_all_module_groups	hpe1437_close
e1430_diagnostics	hpe1437_self_test
e1430_display_module_state	hpe1437_
e1430_display_register	hpe1437_
e1430_get_adc_clock	hpe1437_clock_source_get
e1430_get_anti_alias_filter	hpe1437_input_alias_filter_get
e1430_get_append_status	hpe1437_data_append_status_get
e1430_get_blocksize	hpe1437_data_blocksize_get
e1430_get_center_frequency	hpe1437_frequency_center_get
e1430_get_coupling	hpe1437_input_coupling_get
e1430_get_data_mode	hpe1437_data_mode_get

e1430_get_data_port	hpe1437_data_port_get
e1430_get_data_reread	
e1430_get_data_size	hpe1437_data_resolution_get
e1430_get_data_type	hpe1437_data_type_get
e1430_get_decimation_bandwidth	hpe1437_filter_bw_get
e1430_get_decimation_output	
e1430_get_decimation_passtag	
e1430_get_decimation_state	hpe1437_filter_decimate_get
e1430_get_dsp_clock	hpe1437_clock_dsp_get
e1430_get_error_string	hpe1437_error_message
e1430_get_fifo_block_data_size	
e1430_get_fifo_data_point_size	
e1430_get_fifo_max_blocksize	
e1430_get_fifo_size	hpe1437_data_memsize_get
e1430_get_filter	hpdsp_fir
e1430_get_input_high	hpe1437_input_signal
e1430_get_input_low	hpe1437_input_float
e1430_get_input_offset	
e1430_get_interrupt_mask	hpe1437_interrupt_mask_get
e1430_get_interrupt_priority	hpe1437_interrupt_priority_get
e1430_get_lbus_mode	hpe1437_lbus_mode_get
e1430_get_module_state	
e1430_get_multi_sync	hpe1437_clock_multi_sync_get
e1430_get_range	hpe1437_input_range_get
e1430_get_range_la	hpe1437_input_range_get
e1430_get_register_address	hpe1437_attrib_get
e1430_get_resample	hpdsp_resample
e1430_get_sample_clock_freq_la	hpe1437_clock_fs_get
e1430_get_scale_la	hpe1437_data_scale_get
e1430_get_span	hpe1437_filter_bw_get
e1430_get_timeout	
e1430_get_trigger_bandwidth	hpe1437_filter_bw_get
e1430_get_trigger_delay	hpe1437_trigger_delay_get
e1430_get_trigger_level_adc	hpe1437_trigger_adclevel_get
e1430_get_trigger_level_mag	hpe1437_trigger_maglevel_get
e1430_get_trigger_phase	hpe1437_trigger_delay_actual_get
e1430_get_trigger_slope	hpe1437_trigger_slope_get
e1430_get_trigger_source	hpe1437_trigger_type_get
e1430_init_io_driver	hpe1437_init
e1430_print_errors	hpe1437_error_query
e1430_read_float32_data	hpe1437_read
e1430_read_raw_data	hpe1437_read_raw
e1430_read_register_card	hpe1437_status_get
e1430_read_register_image	hpe1437_status_get
e1430_reset_dsp	hpe1437_filter_sync
e1430_reset_lbus	hpe1437_lbus_reset
e1430_reset_module	hpe1437_reset
e1430_set_adc_clock	hpe1437_clock_source
e1430_set_analog_input	hpe1437_input_setup
e1430_set_anti_alias_filter	hpe1437_input_alias_filter
e1430_set_append_status	hpe1437_data_append_status
e1430_set_blocksize	hpe1437_data_blocksize
e1430_set_center_frequency	hpe1437_frequency_center
e1430_set_clock_master_mode	hpe1437_clock_master
e1430_set_clock_mode	hpe1437_clock_setup

e1430_set_coupling	hpe1437_input_coupling
e1430_set_data_format	hpe1437_data_setup
e1430_set_data_mode	hpe1437_data_mode
e1430_set_data_port	hpe1437_data_port
e1430_set_data_reread	
e1430_set_data_size	hpe1437_data_resolution
e1430_set_data_type	hpe1437_data_type
e1430_set_decimation_bandwidth	hpe1437_filter_bw
e1430_set_decimation_filter	hpe1437_filter_setup
e1430_set_decimation_output	
e1430_set_decimation_passtag	
e1430_set_decimation_state	hpe1437_filter_decimate
e1430_set_dsp_clock	hpe1437_clock_dsp
e1430_set_input_high	hpe1437_input_signal
e1430_set_input_low	hpe1437_input_float
e1430_set_input_offset	
e1430_set_interrupt	hpe1437_interrupt_setup
e1430_set_interrupt_mask	hpe1437_interrupt_setup
e1430_set_interrupt_priority	hpe1437_interrupt_setup
e1430_set_lbus_mode	hpe1437_lbus_mode
e1430_set_multi_sync	hpe1437_clock_multi_sync
e1430_set_range	hpe1437_input_range
e1430_set_range_la	hpe1437_input_range
e1430_set_sample_clock_freq_la	hpe1437_clock_fs
e1430_set_span_zoom	hpe1437_filter_setup, hpe1437_frequency_setup
e1430_set_timeout	
e1430_set_trigger_delay	hpe1437_trigger_delay
e1430_set_trigger_level_adc	hpe1437_trigger_adclevel
e1430_set_trigger_level_mag	hpe1437_trigger_maglevel
e1430_set_trigger_mode	hpe1437_trigger_setup
e1430_set_trigger_slope	hpe1437_trigger_slope
e1430_set_trigger_source	hpe1437_trigger_type
e1430_set_try_recover	
e1430_test_data_collection	hpe1437_self_test
e1430_test_fifo_memory	hpe1437_self_test
e1430_test_interrupts	hpe1437_self_test
e1430_test_logical_address	hpe1437_self_test
e1430_test_meas_control	hpe1437_self_test
e1430_test_register_access	hpe1437_self_test
e1430_test_timing_setup	hpe1437_self_test
e1430_test_trigger	hpe1437_self_test
e1430_trigger_module	hpe1437_meas_control
E1430_TRY	
E1430_RECOVER	
e1430_write_register	
e1430_write_register_card	
e1430_write_register_image	