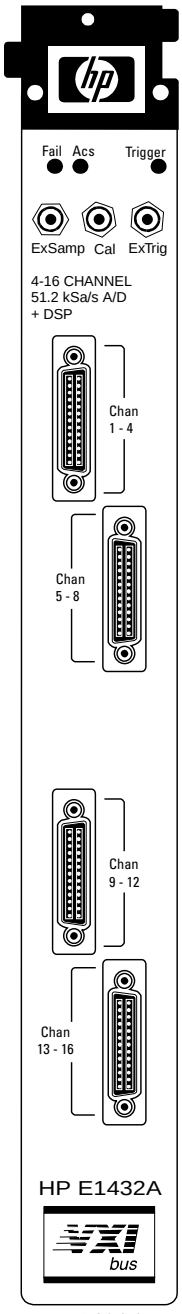
HEWLETT® PACKARD

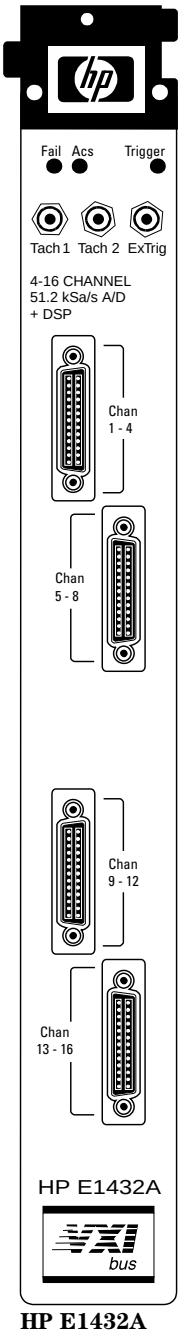
HP E1432A

Technical Specifications

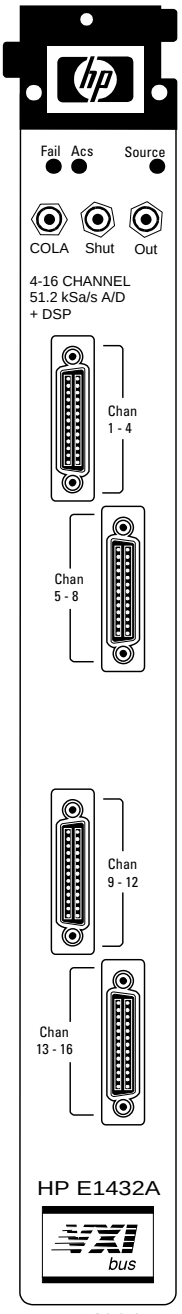
4-16 Channel 51.2 kSa/s Digitizer plus DSP
Rev. November 1995



HP E1432A



HP E1432A with Tachometer Option AYF



HP E1432A with Arbitary Source Option 1D4

Future revisions of the HP E1432A software will enhance its functionality. Please contact your local Hewlett-Packard sales representative for the most current product information.

Specifications describe warranted performance over the temperature range of 0° to 50°C, after a 15-minute warm-up from ambient conditions. Supplemental characteristics identified as "typical" or "characteristic," provide useful information by giving non-warranted performance parameters. Typical performance is applicable from 20° to 30°C.

Abbreviations

dBfs = dB relative to full scale amplitude range.

dBc = dB relative to carrier amplitude.

Typical = typical, non-warranted, performance specification included to provide general product information.

Frequency

Bandwidth (Hz) [1]	Sample Rate (samples/second)	Bandwidth (Hz) [1]	Sample Rate (samples/second)
23000 [2]	51200	488.2813	1250
20000	51200	468.75	1200
19531.25	50000	400	1024
18750	48000	390.625	1000
16000	40960	320	819.2
15625	40000	312.5	800
12800	32768	305.1758	781.25
10000	25600	292.9688	750R 640
9765.625	25000	250	625
9375	24000	244.1406	600
8000	20480	234.375	512
7812.5	20000	200	500
6400	16384	195.3125	409.6
5000	12800	160	400
4882.8125	12500	156.25	390.625
4687.5	12000	152.5879	375
4000	10240	146.4844	320
3906.25	10000	125	312.5
3750	9600	122.07031	300
3200	8192	117.1875	256
3125	8000	100	250
2560	6553.6	97.65625	~ 204.8
2500	6400	80	200
2441.4063	6250	78.125	195.3125
2343.75	6000	76.293945	187.5
2000	5120	73.242188	160
1953.125	5000	62.5	156. 25
1875	4800	61.035156	150
1600	4096	58.59375	128
1562.5	4000	50	125
1280	3276.8	48.828125	1 02.4
1250	3200	40	80
1220.7031	3125	31.25	78.125
1171.875	3000	30.517578	75
1000	2560	29.296875	64
976.5625	2500	25	62.5
937.5	2400	24.414063	51.2
800	2048	20	40
781.25	2000	15.625	39.0625
640	1638.4	15.258789	37.5
625	1600	14.648438	32
610.3516	1562.5	12. 5	31.25
585.9375	1500	12.207031	25.6
500	1280	10	

Frequency Accuracy ± 0.012% (120 ppm)

[1] Bandwidth is 400 lines of 512 line FFT spectrum unless noted otherwise.

[2] Bandwidth is 460 lines of 512 line FFT spectrum.

Input

Full Scale Input Ranges (in volts peak)	100 mV, 200 mV, 500 mV, 1 V, 2 V, 5 V, 10 V, 20 V [3] Add 23% to include over-range capability.
Maximum Input Level	42 Vp
Input Impedance (dc coupled or ac coupled above 10 Hz**)**	
Differential	1 MΩ nominal
Either side-to-chassis	500 kΩ, 35 pF nominal
Input Resistance (measured at dc while ac coupled)	
Either side-to-chassis	350 kΩ nominal
AC Coupling 3 dB Corner Frequency	< 1 Hz
Common Mode Rejection Ratio	
dc coupled, dc to 1 kHz	> 50 dB
ac coupled, 40 Hz to 1 kHz	> 45 dB
Maximum signal, either side-to-chassis	± 20 Vpk
Amplitude Over-Range Detection	
Over-range indication after:	
Common mode overload	± 22.5 V (typical)
Differential overload	± 130% of range (typical)
Residual DC	≤ ±1% of range, ±10 mV

Amplitude

Amplitude Accuracy at 1 kHz	± 0.7% of reading, ± 0.01% of full scale
Flatness (relative to 1 kHz, at full scale)	± 1% (0.09 dB)
Amplitude Resolution	16 bits, less 2.3 dB over-range

Cross Channel Matching (any HP E1432A module in the same mainframe)

Cross Channel Amplitude Match (full-scale signal, input ranges equal, frequency above 10 Hz if ac coupled)	± 0.1 dB
Cross Channel Phase Match (full-scale signal, input ranges equal)	
20 kHz	± 2.5° (or ± 350 ns)
F_{HZ} = 800 Hz to 20 kHz	$\pm (F_{HZ} \times 125 \times 10^{-6})°$
100 Hz to 800 Hz	± 0.1°
dc to 100 Hz, dc couple	± 0.1°
50 Hz to 100 Hz, ac couple	± 0.2°

[3] The 20 V range is not specified for dynamic range.

Dynamic Range

Resolution	16 bits
Spurious Free Dynamic Range (includes spurs, harmonic distortion, intermodulation distortion, alias products) (source impedance = 50 Ω)	< – 80 dBfs (0.01%fs), – 90 dBfs (typical)
Spurious and Residual Responses	< – 80 dBfs
Harmonic Distortion	< – 80 dBfs, – 90 dBfs (typical)
Aliased Responses (≤ 0 dBfs, ≤ 1 MHz)	< – 80 dBfs
Crosstalk (receiving channel source impedance = 50 Ω, low side grounded, full scale, < 10 kHz signal on other channels, input ranges within 20 dB)	< – 80 dBfs (typical)
Noise (input terminated with 50 Ω, 100 mV range)	
Noise density above 100 Hz	< 300 nVrms/$\sqrt{Hz}$
Noise density at 10 Hz	< 1000 nVrms/$\sqrt{Hz}$
Total rms noise, 23 kHz span	< 45 μVrms

Trigger

Trigger Detection	Digital
Trigger Modes	Input, external, source, TTL, TRG, RPM (requires option AYF)

Option 1D4 Arbitrary Source Specifications

General	
Output Modes	Sine and pseudo random with burst and band translation, arbitrary waveform with loop or continuous output
Frequency Bands	
Sine, noise modes	
Reconstruction filter bandwidth	0 to 25.6 kHz
DSP data rate (Fs)	48.00 kHz to 65.536 kHz
Data word size	16 bits
Arb modes	
Reconstruction filter bandwidth	0 to 6.4 kHz
Data word size	20 bits
Frequency Accuracy	± 0.012% (120 ppm)

Signal Output	
Number of Output Channels	1
Maximum Amplitude	10 Vp nominal
Output Impedance	< 0.5 Ω (typical)
Maximum Output Current	100 mA (typical)
Maximum Capacitive Load	0.01 μF (typical)
Amplitude Control (signal amplitude = range × scale factor)	
Maximum amplitude	10 Vp nominal
Amplitude ranges	79 mVp to 10 Vp in 0.375 dB steps
Amplitude scale factor	0.0 to 1.0, with 20-bit resolution
Residual Output Noise Voltage (Freq > 500 Hz)	< 500 nV/$\sqrt{\text{Hz}}$
Residual DC Offset	
Offset after autozero	± 2 mV
Offset after shutdown	± 20 mV
Zeroing resolution	100 μV
Output Overload Trip	> 17 V
Amplitude Ramp-down Time (Programmable)	0 to 30 seconds
Shutdown	
Shutdown input	TTL levels
Shutdown time	< 5 s
Shutdown time, ac fail	< 4 ms

Sine Output Mode

Sine Frequency (65536 Hz Fs)	
Frequency range	0 to 25.6 kHz
Frequency resolution	244 μHz
Amplitude Accuracy (1 kHz sine wave, into ≥ 200 Ω)	
10 Vp to 0.158 Vp ranges	± 0.20 dB (2.3 %)
0.152 Vp to 79 mVp ranges	± 0.40 dB (4.7 %)
Flatness (relative to 1 kHz)	± 0.5 dB
Harmonic and Aliased-harmonic Distortion (≥ 1 kΩ load)	
1 Vp range, 1.0 scale factor, 0 to 6.4 kHz	< – 80 dBc
2 to 10 Vp range, 0.05 to 1.0 scale factor, 0 to 25.6 kHz	< – 70 dBc
Spurious responses	< – 60 dBVp

Constant Level Output	
Output Level (after 1 second settling, DAC level > – 60 dBfs)	1 Vp (nominal)
Output Impedance	1.2 kΩ (typical)
Flatness, 10 Hz to 25.6 kHz	± 1 dB (typical)
Sine Wave Distortion	– 40 dBc (typical)
Residual dc Offset	< 1 mV (typical)

Summer Input	
Maximum Input Level	10 Vp
Gain, Summer Input to Signal Output	0 ± 0.5 dB at 1 kHz
Input Impedance	> 10 kΩ (typical)
Flatness, dc to 25.6 kHz	± 0.5 dB (typical)
Sine Wave Distortion	– 80 dBc (typical)
Residual dc Offset	1 mV (typical)

Option AYF Tachometer Input Specifications

General

Option AYF, Tachometer Input, provides two tachometer inputs. When this option is installed, 2 of the 3 SMB connectors on the VXI module are used for tachometer inputs. When this option is not installed, these connectors are normally used for "External Sample" and "Trigger."

Each tachometer input has a programmable trigger level. Each tach pulse causes a "Tach Edge Time" to be recorded in a 16384-word FIFO. A "Tach Edge Time" is the instantaneous value of the 32-bit "Tach Counter". A "Decimate" number can be set to ignore a number of tach pulses before recording each Tach Edge Time. A "Holdoff" time can be set to avoid false triggering due to ringing.

One of the tachometer inputs can be programmed for use as a trigger input rather than a tachometer input. In this mode, the tachometer option can trigger the system and measure the time between the trigger and the next sample clock edge.

The analog signal from either of the Tachometer inputs can be routed to an input channel using the internal calibration path.

Tach Counter	32-bit counter with roll-over detector bit
Decimate Counter	16-bit counter
Input Signal Trigger Level (typical)	
Voltage Range	– 25 V to + 25 V
Resolution, levels < ± 5V	40 mV
Resolution, levels > ± 5V	200 mV
Hysteresis	Programmable, 0 to 250 mV
Slope	Programmable, positive or negative
Input Signal Timing	
Minimum pulse width	5 μs
Maximum pulse rate	100 kHz
Trigger holdoff	1 to 65536 clock periods
Input Impedance	20 kΩ (typical)

Features	
VXI Standard Information	Conforms to VXI revision 1.4 C-size, single slot width Register-based programming "Slave" Data Transfer Bus functionality A24 address capability D32 data capability Optional Local Bus capability SUMBUS driver and receiver Requires 2 or 4 TTLTRG_ lines for multi-module synchronization
Signal Processing	33 MHz Motorola 96002 DSP 2 banks of 128 K word static RAM 4 M bytes dynamic RAM (32 M bytes with option ANC) 128 K bytes Flash ROM Direct Memory Access (DMA) data transfer

Software Drivers	
Driver Type	C libraries with source code
Supported Operating Systems	HP-UX 9.05
Supply Media	DAT tape
Plug & Play Compliance	C libraries support the preliminary Plug & Play standard for HP-UX, but will be updated later to full Plug & Play compliance when the HP-UX Plug & Play specification has been finalized. Plug & Play support for MS Windows will be added at that time. There will be no charge for driver upgrades.

Regulatory Compliance

Safety Standards	Designed for compliance to: UL 1244, 4th Edition IEC 348, 2nd Edition, 1978 CSA C22.2, No. 231
Radiated Emissions (tested in a "typical" system configuration, consisting of an HP E1401B Mainframe, HP V743 Controller, and HP E1432A module with option 1D4 or AYF)	CISPR 11: 1990, Group 1, Class A (requires connector shields HP E1400-80920 or HP E1421-80920) Tested for compliance to the European Economic Area's EMC directive
Electrostatic Discharge	Tested for compliance to the European Economic Area's EMC directive
Radiated Immunity	Tested for compliance to the European Economic Area's EMC directive

Environmental

Operating Restrictions	
Ambient Temperature	0° to 55°C
Humidity, Non-condensing	20% RH to 90% RH at 40°C
Maximum Altitude	4600 meters (15,000 feet)
Storage and Transport Restrictions	
Ambient Temperature	– 20° to 65°C
Humidity, Non-condensing	20% RH to 90% RH at 40°C
Maximum Altitude	4600 meters (15,000 feet)

General Characteristics

VXI Power Requirements

dc Current	**16 Channels**	**12 Channels**	**8 Channels**	**4 Channels**
Source option installed				
+5 V	5.20 A	4.93 A	4.66 A	4.39 A
+12 V	0.38 A	0.38 A	0.38 A	0.38 A
–12 V	0.23 A	0.23 A	0.23 A	0.23 A
+24 V	0.85 A	0.84 A	0.83 A	0.82 A
– 24 V	0.50 A	0.49 A	0.48 A	0.47 A
– 5.2 V	0.28 A	0.28 A	0.28 A	0.28 A
– 2 V	0.03 A	0.03 A	0.03 A	0.03 A
Tachometer option installed				
+5 V	4.80 A	4.53 A	4.26 A	3.99 A
+12 V	0.30 A	0.30 A	0.30 A	0.30 A
–12 V	0.09 A	0.09 A	0.09 A	0.09 A
+24 V	0.56 A	0.55 A	0.54 A	0.53 A
– 24 V	0.21 A	0.20 A	0.19 A	0.18 A
– 5.2 V	0.28 A	0.28 A	0.28 A	0.28 A
– 2 V	0.03 A	0.03 A	0.03 A	0.03 A
No options installed				
+5 V	4.60 A	4.33 A	4.06 A	3.79 A
+12 V	0.30 A	0.30 A	0.30 A	0.30 A
–12 V	0.09 A	0.09 A	0.09 A	0.09 A
+24 V	0.55 A	0.54 A	0.53 A	0.52 A
– 24 V	0.20 A	0.19 A	0.18 A	0.17 A
– 5.2 V	0.28 A	0.28 A	0.28 A	0.28 A
– 2 V	0.03 A	0.03 A	0.03 A	0.03 A
Dynamic Current				
+5 V	0.10 A			
+12 V	0.02 A			
–12 V	0.01 A			
+24 V	0.01 A			
– 24 V	0.01 A			
– 5.2 V	0.01 A			
– 2 V	0.01 A			

VXI Cooling Requirements	5.2 liters/second 0.46 mm H_2O
Warm-up Time	15 minutes

Performance Benchmarks
Because these performance benchmarks depend on the software and hardware configuration, they are included as supplemental, non-warranted characteristics.

VXI Data Transfer Rate (P1 connector)	
From HP E1432 DRAM to VXI Controller, during continuous acquisition, D32 data transfer size	4 M Bytes/s
From VXI Controller to HP E1432 DRAM (or to Option 1D4 Arb Source)	4 M Bytes/s
Maximum number of input channels for continuous throughput to HP E1562A at 51.2 kHz sample rate, 32 bits/sample	32 Channels
Local Bus Data Transfer Rate	
From HP E1432 DRAM, one block, during continuous acquisition	32 M Bytes/s
Maximum number of input channels for continuous throughput at 51.2 kHz sample rate	96 Channels
FIFO Memory (Maximum FIFO size, 4M Bytes DRAM installed)	4 MBytes/number active channels