Association of Old Crows

31st Annual AOC EW Technical Symposium

A Digital Signal Processing Approach to Analog-to-Digital Conversion

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Washington, DC

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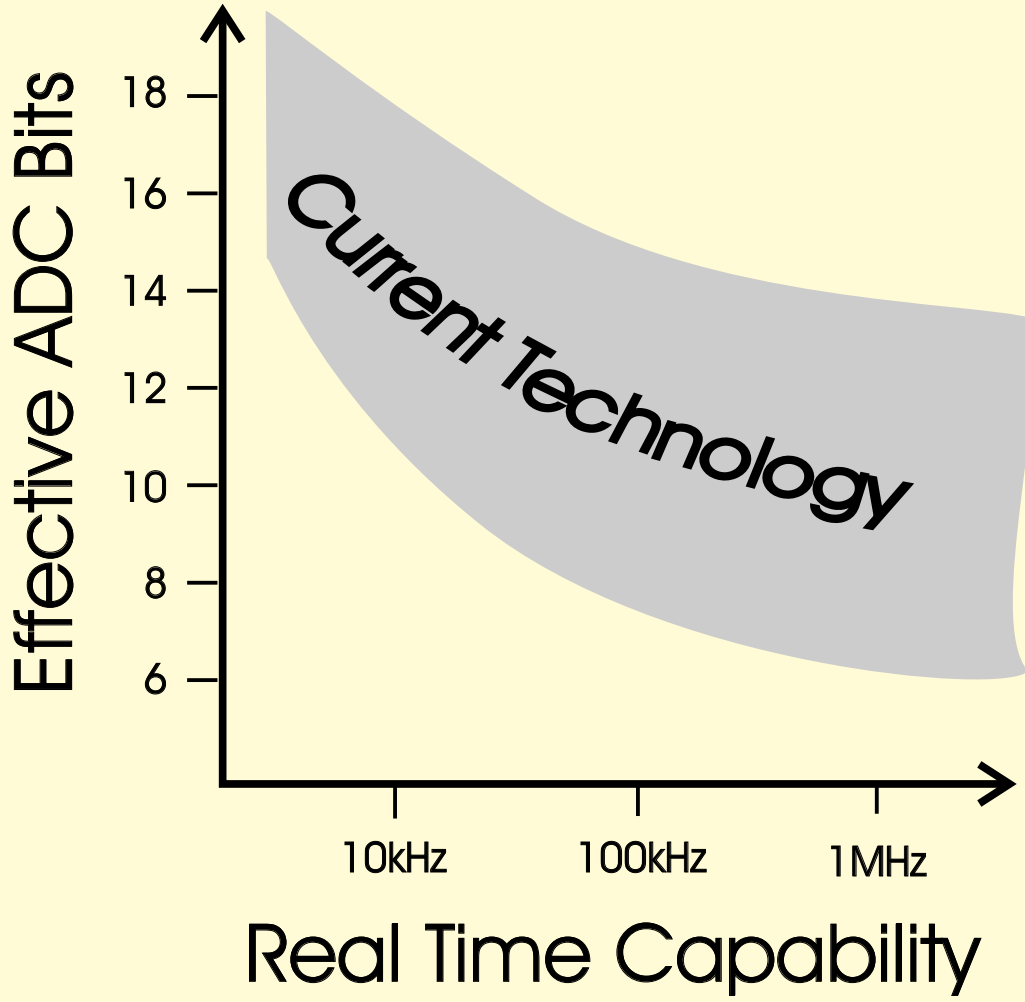
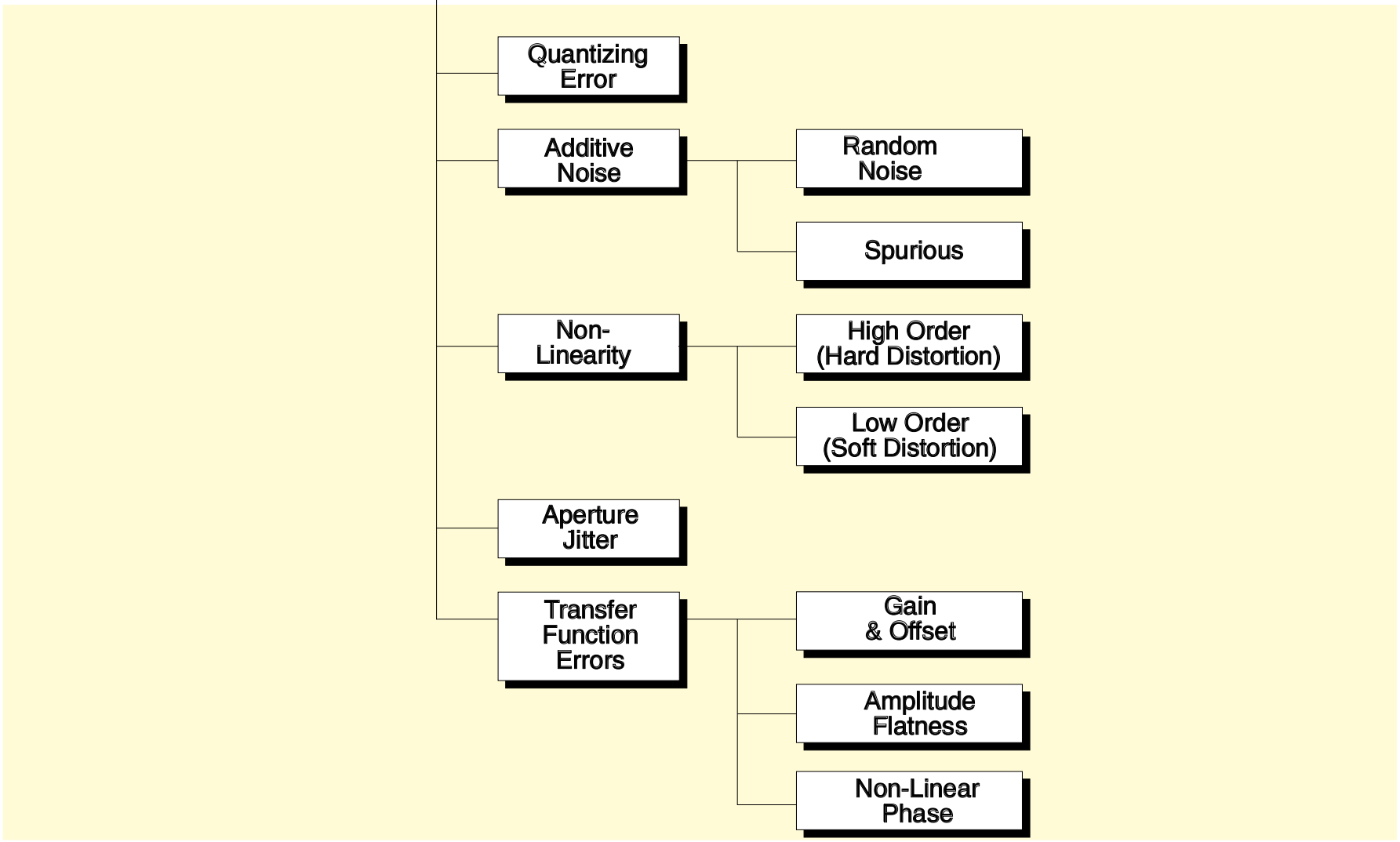
ADC Effective Bit Performance



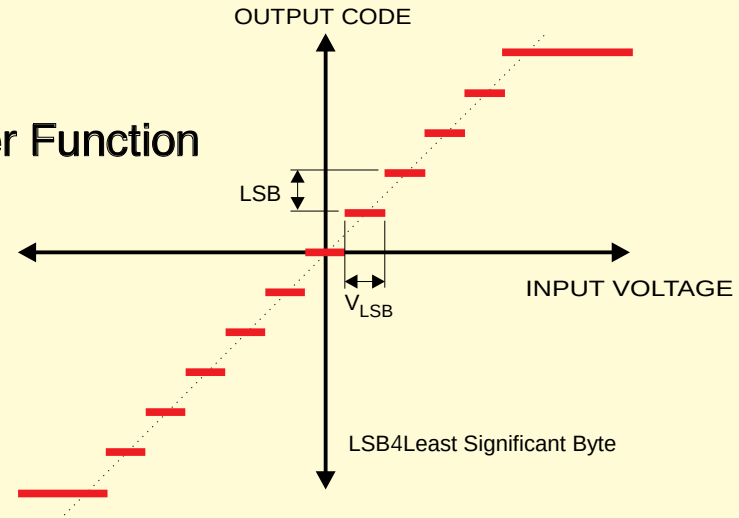
ADC Error Sources



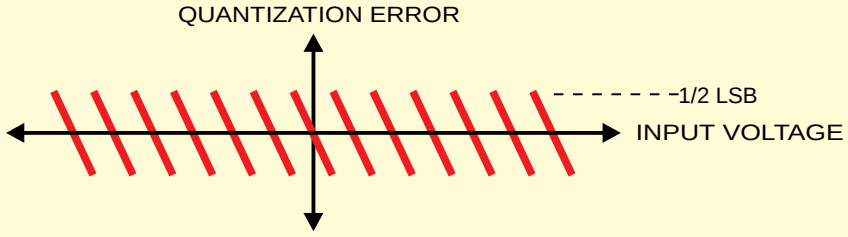
ADC Error Sources

Quantizing Error

Ideal Quantizer Transfer Function



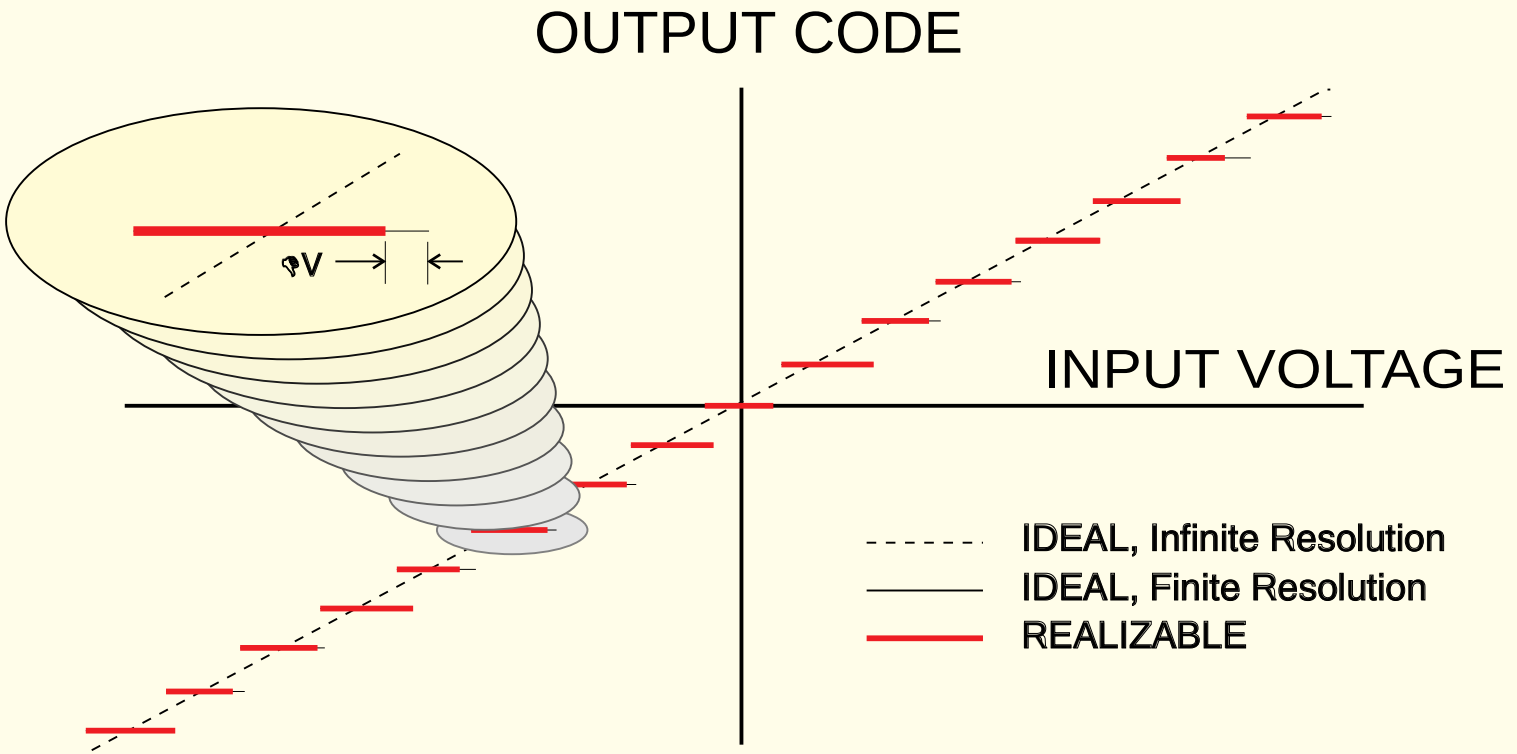
Quantizing Error for an Ideal ADC



ADC Error Sources

Non-Linearity

Quantizer Differential Non-Linearity

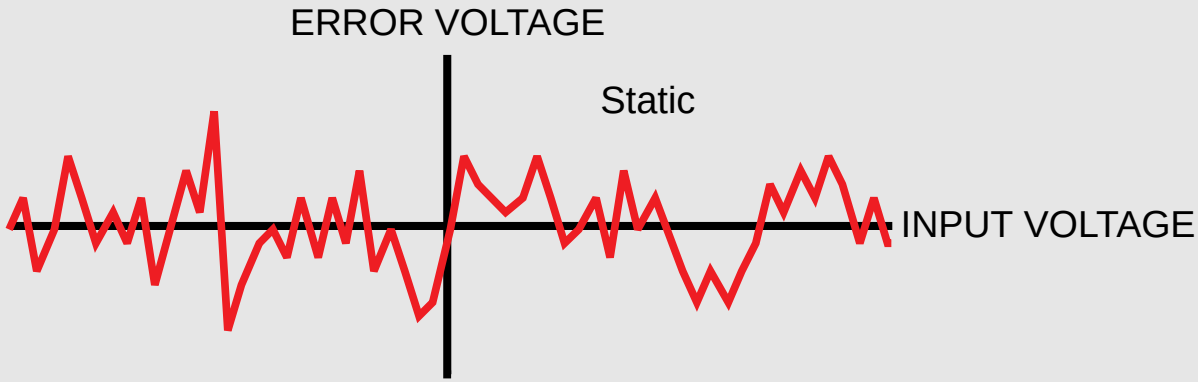


ADC Error Sources

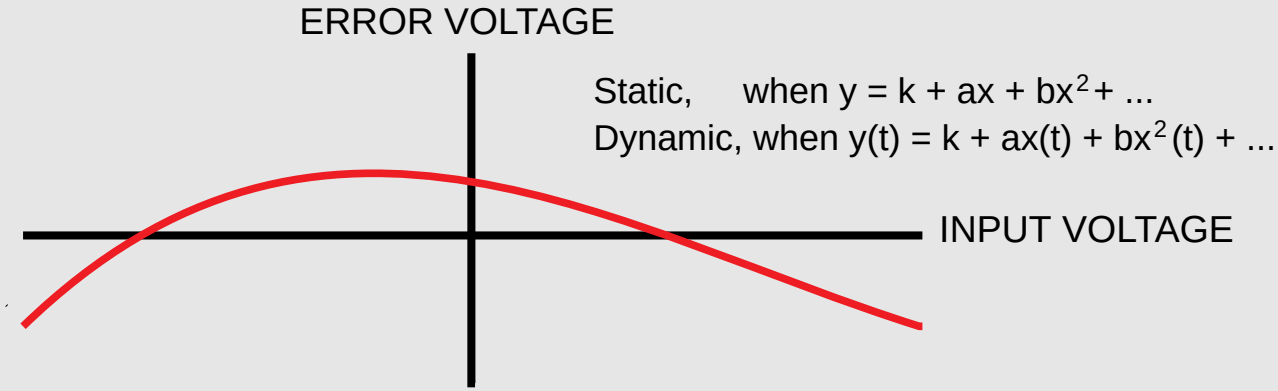
Non-Linearity

NON-LINEARITIES

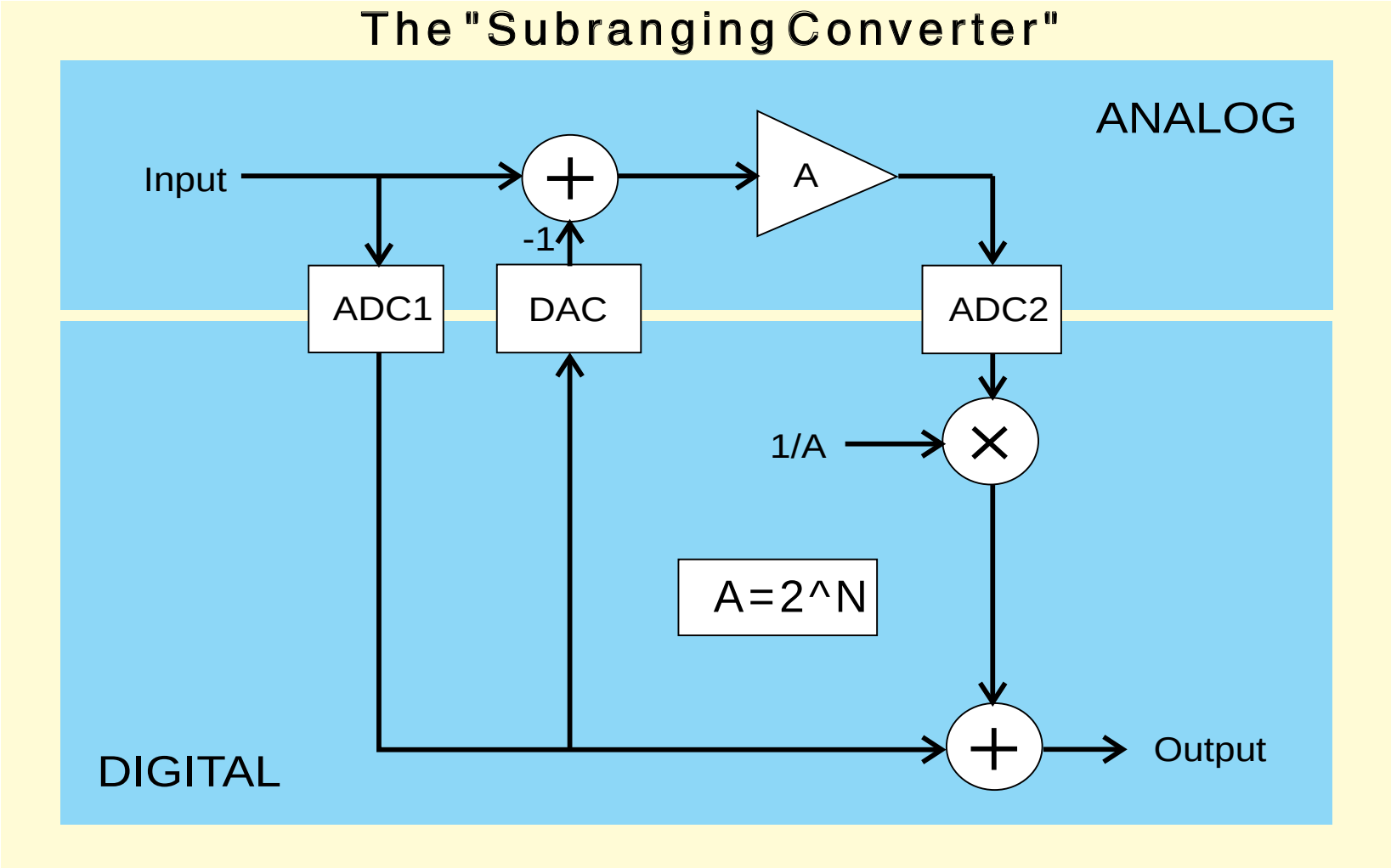
"Hard" Distortion
(HIGH ORDER)



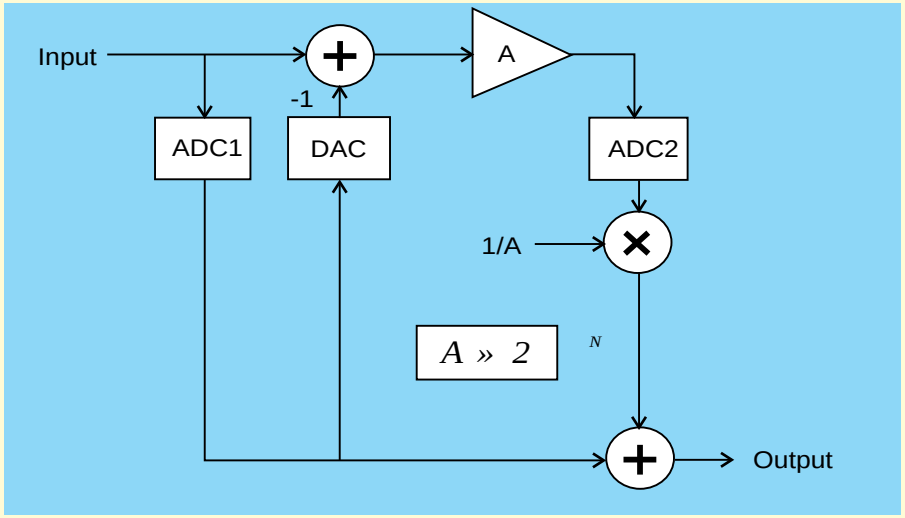
"Soft" Distortion
(LOW ORDER)



Standard 2-Pass ADC



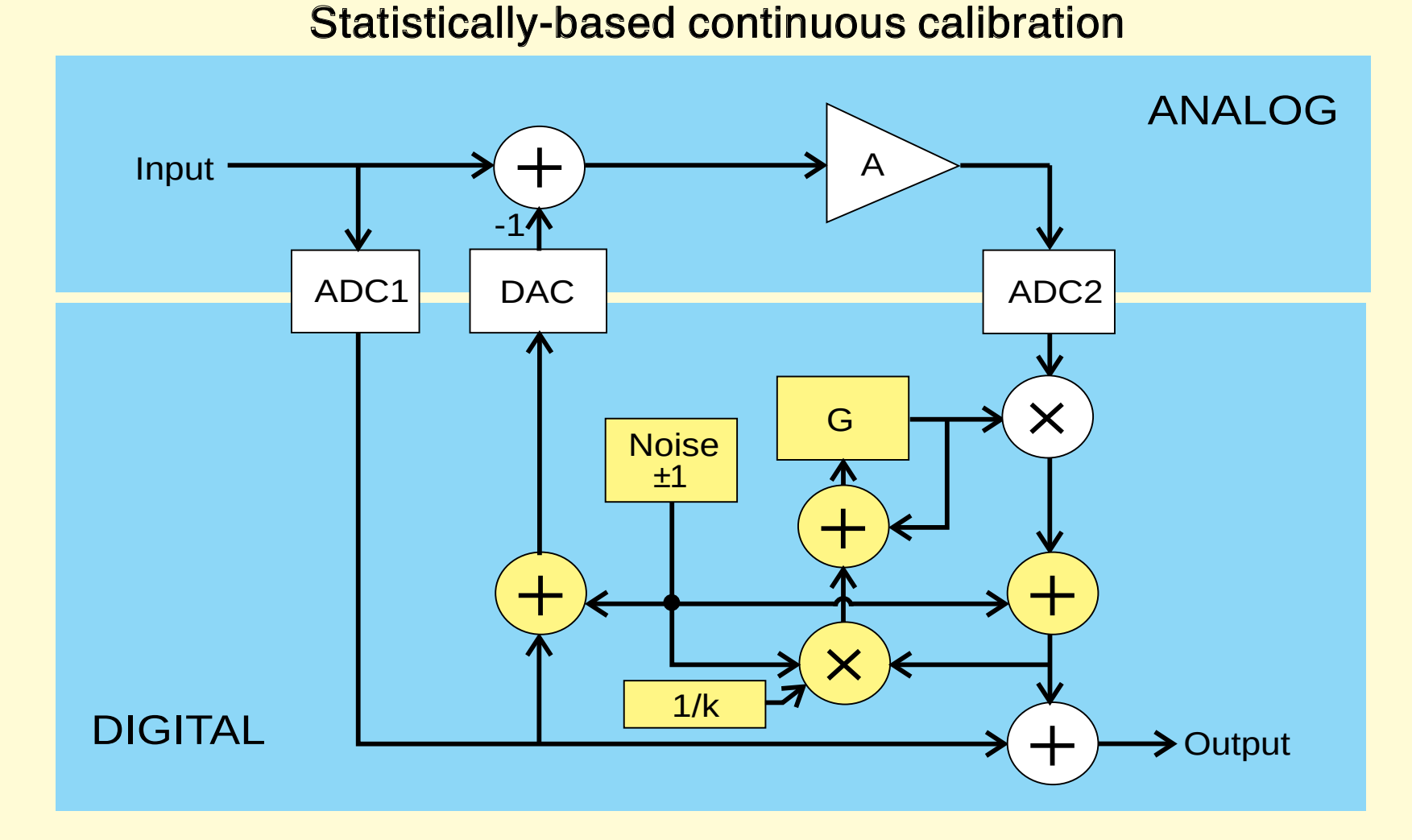
Standard 2-Pass ADC



X - Input from track & hold
Y - Output sample
E_1 - ADC1 quantization error
E_2 - ADC2 quantization error
E_d - DAC error

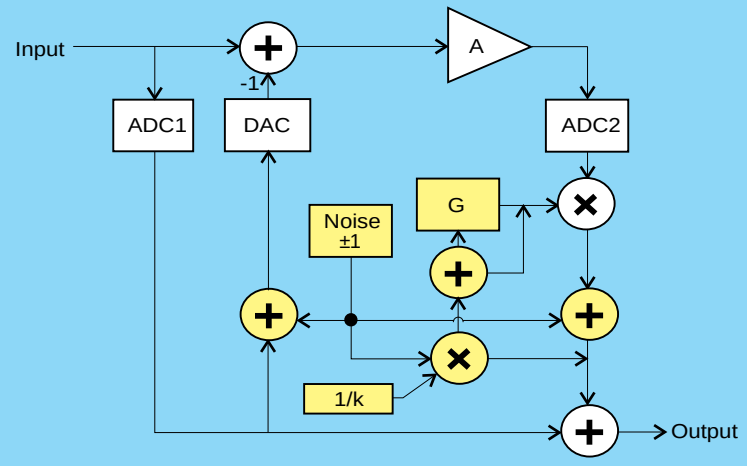
$$Y \equiv X + E_1(1 - A2^{-N}) + E_dA2^{-N} + E_22^{-N}$$

Enhanced 2-Pass ADC



Enhanced 2-Pass ADC

Calibration of Residue Gain



X_n - Input from track & hold
G_n - Gain value
N_n - Random ± 1 sequence
D_n - Output of ADC1
A - Residue amplifier gain

$$G_{n+1} \equiv G_n + \frac{N_n}{k}\left(AG_n(X_n - D_n - N_n) + N_n\right)$$

$$G_{n+1} \equiv G_n + \frac{1}{k}(1 - AG_n)$$ Difference equation

$$G_n \equiv \frac{1}{A} + \left(1 - \frac{A}{k}\right)^n \left(G_0 - \frac{1}{A}\right)$$ Exponential Average

Closed-loop system tracks changes in residue amp gain!

$$G_\infty \equiv \frac{1}{A}$$

Enhanced 2-Pass ADC

Standard 2-Pass Error Model

$$Y = X + E_1(1 - AG) + E_dAG + E_2G$$

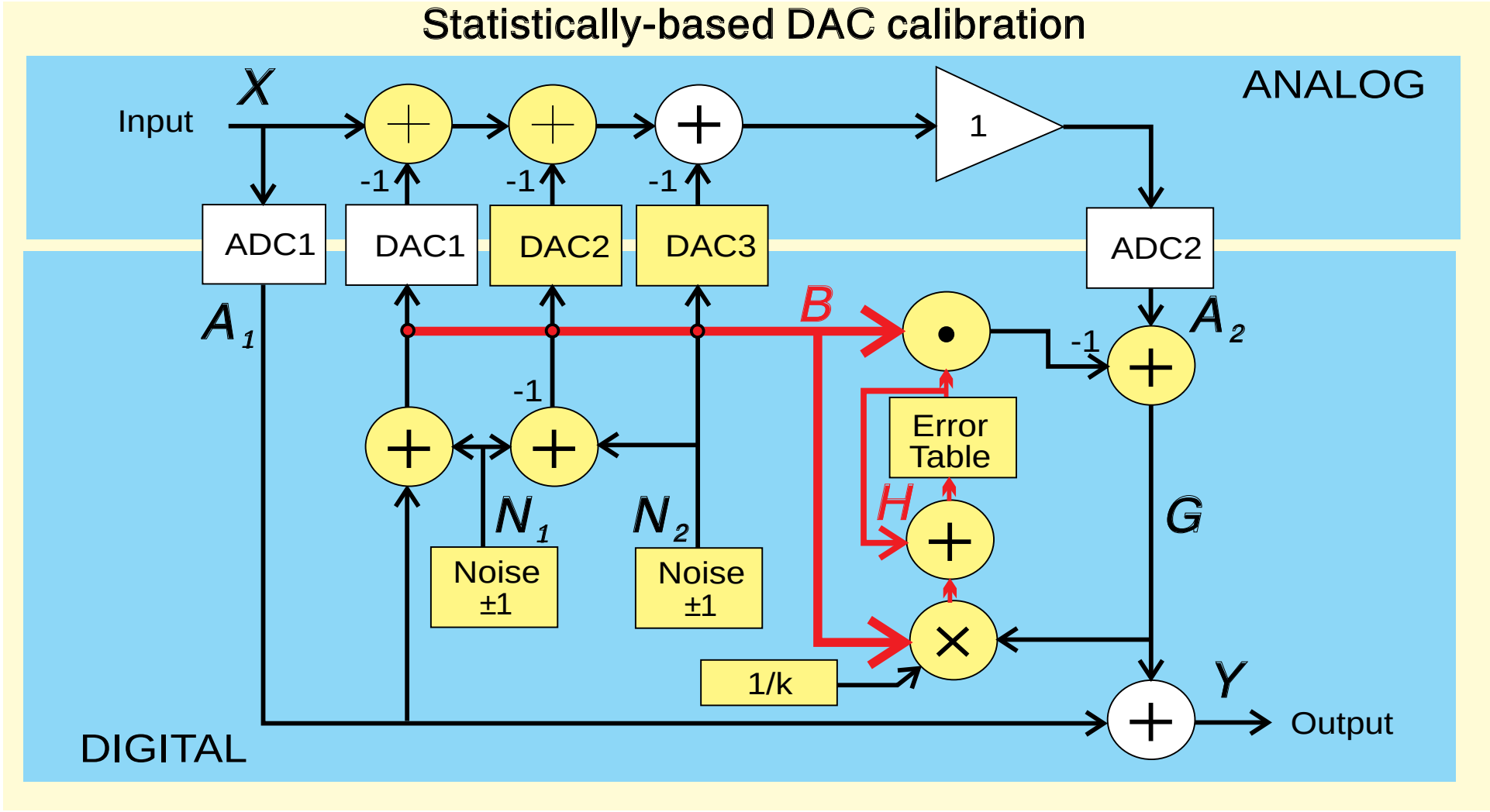
Contribution of Gain Calibration

$$G = \frac{1}{A}$$

New Error Model

$$Y = X + E_d + \frac{E_2}{A}$$

Enhanced 2-Pass ADC



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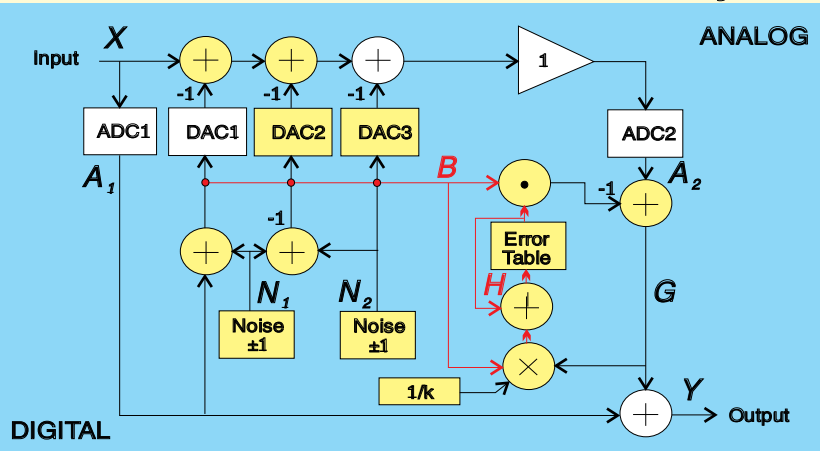
Enhanced 2-Pass ADC

Statistically-based DAC calibration



B - Vector of DAC bit line states

b_n - MSB of DAC1

C - Vector with DAC bit weights w/errors

H - Vector with corrections for DAC bit errors

W - Vector, Expected Value($C + H_n$)

D - Vector, Expected Value($B_n b_n$)

F - Matrix, Expected Value($B_n B^T_n$)

$$G_n \equiv X - b_n - B_n \odot C + B_n \odot H_n$$

$$H_{n+1} \equiv H_n + \frac{B_n}{k}(X - b_n - B_n^T(C + H_n))$$

$$W_n \equiv -F_{-1}D + (I - \frac{1}{k}F)^n(W_0 + F^{-1}D)$$

Closed-loop system tracks and cancels DAC bit current errors!

$$W_\infty \equiv -F^{-1}D$$

Enhanced 2-Pass ADC

Dac calibration zeroes out the DAC error term E_d.

Model for ADC error after DAC calibration becomes:

$$Y = X + \frac{E_2}{A}$$

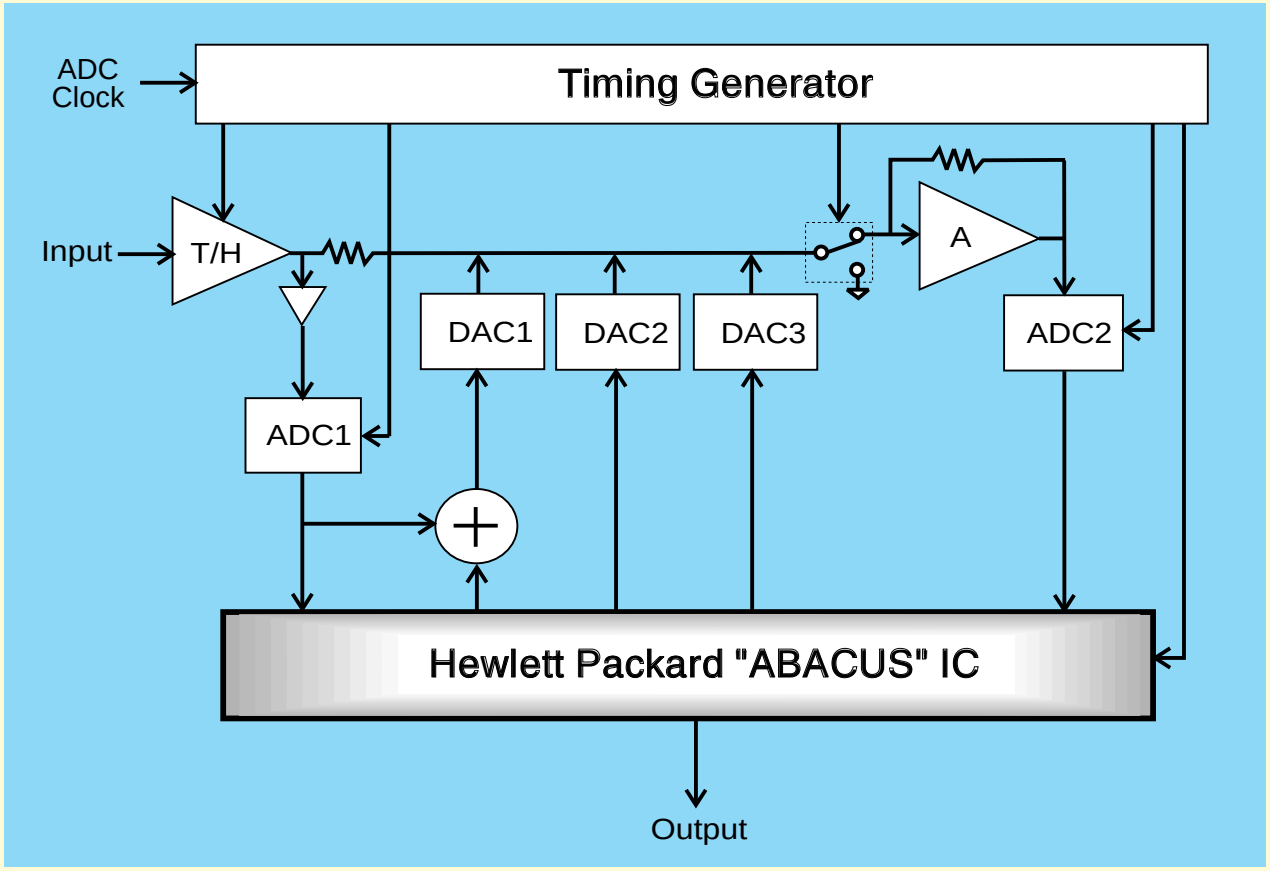
Analog dither at input of ADC2 and intentionally generated random errors from DAC3 cause 1/2 scale dither at input of ADC2. Remaining quantization noise goes away!

The Bottom Line!

$$Y_n \equiv X_n + noise_n$$

Enhanced 2-Pass ADC Implementation

Enhanced ADC with 23-bit resolution



The "ABACUS" IC

144-pin SM
CMOS-26 (≤.9 micron)
≥200K transistors
REAL TIME up to 25MHz
Up to 9-bit ADC1, 12-bit ADC2
≥1.5G math ops/sec

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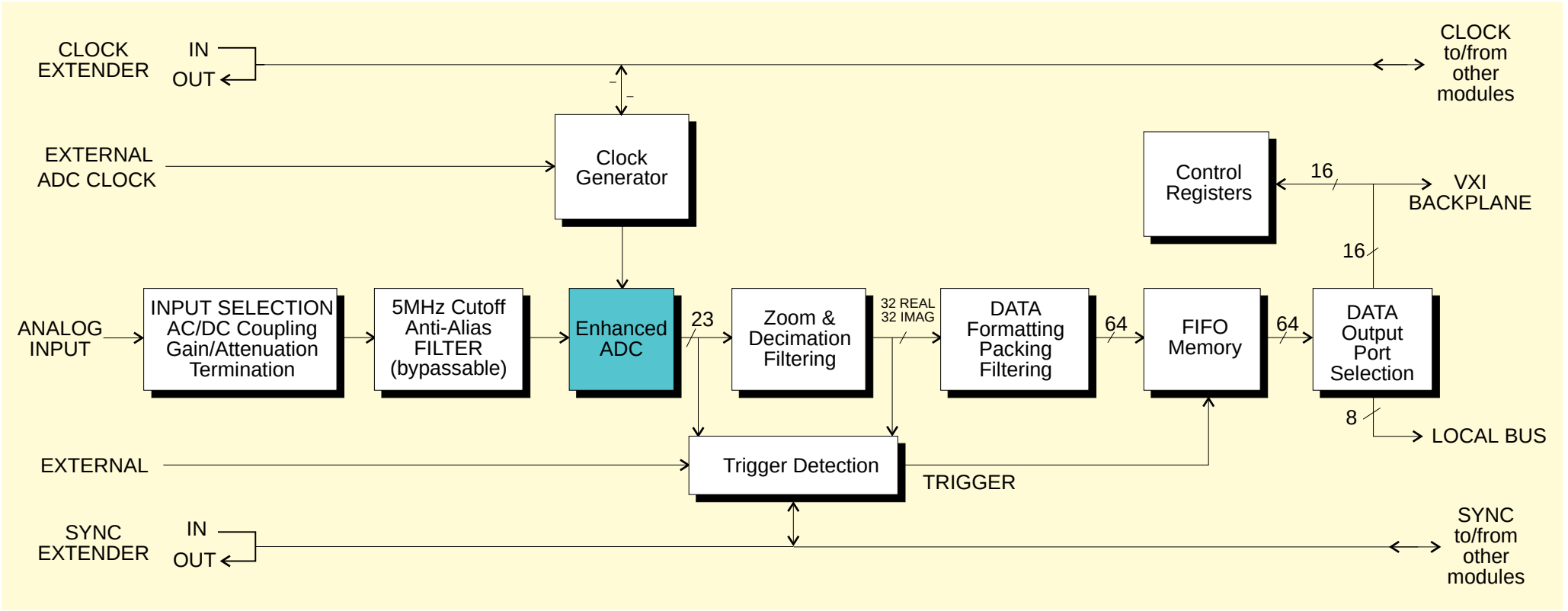
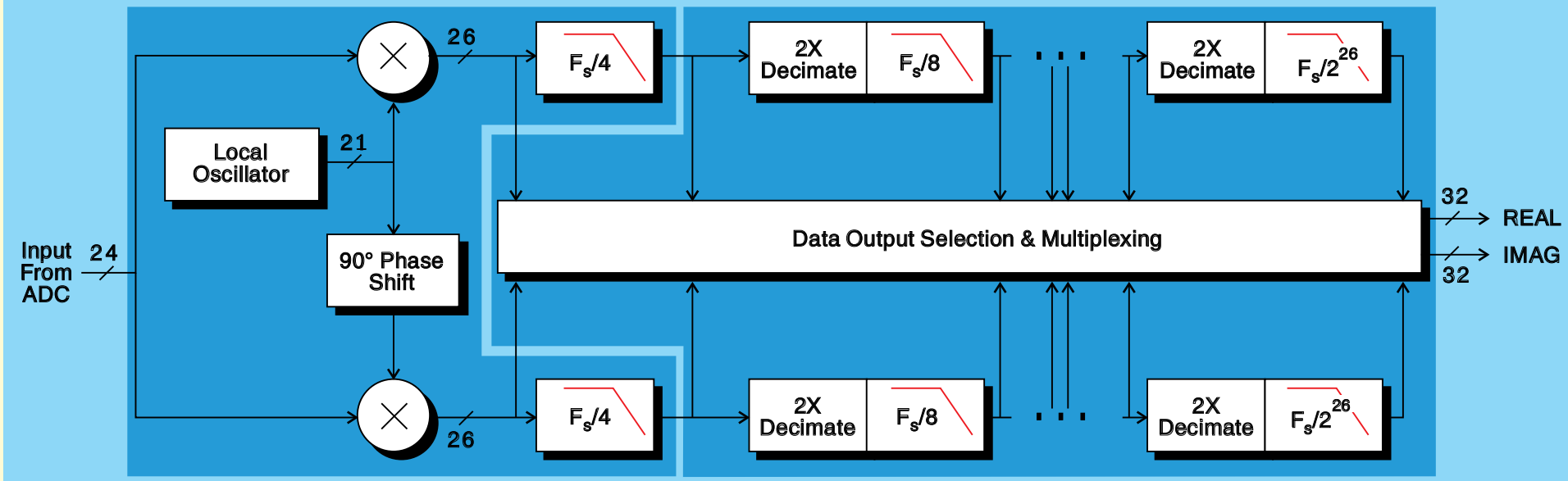
Enhanced ADC-Based Front End



Design GOALS: 10MHz Sample Rate, -110dBSFDR, 23-bit Resolution

4MHz Bandwidth, 70dB SNR @ 10MSa/s

Zoom & Decimation Filtering



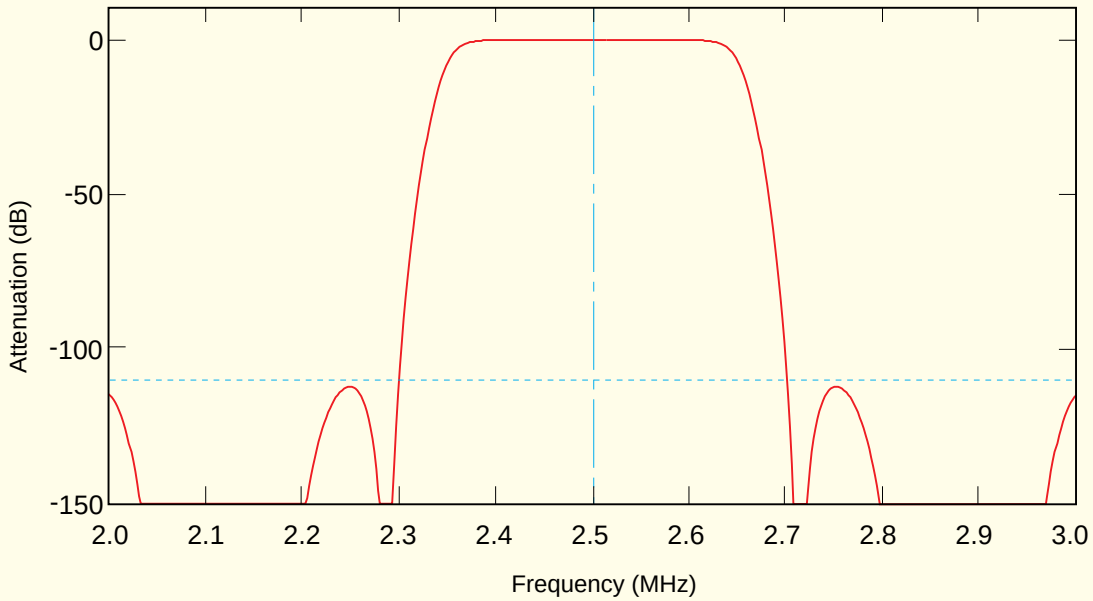
"Kestrel"

CMOS-26
26MSa/s max REAL TIME rate
42 adds & 4 multiplies in parallel
1.196G ops/sec
Typical spurs ⩽-125dBc

"Osprey"

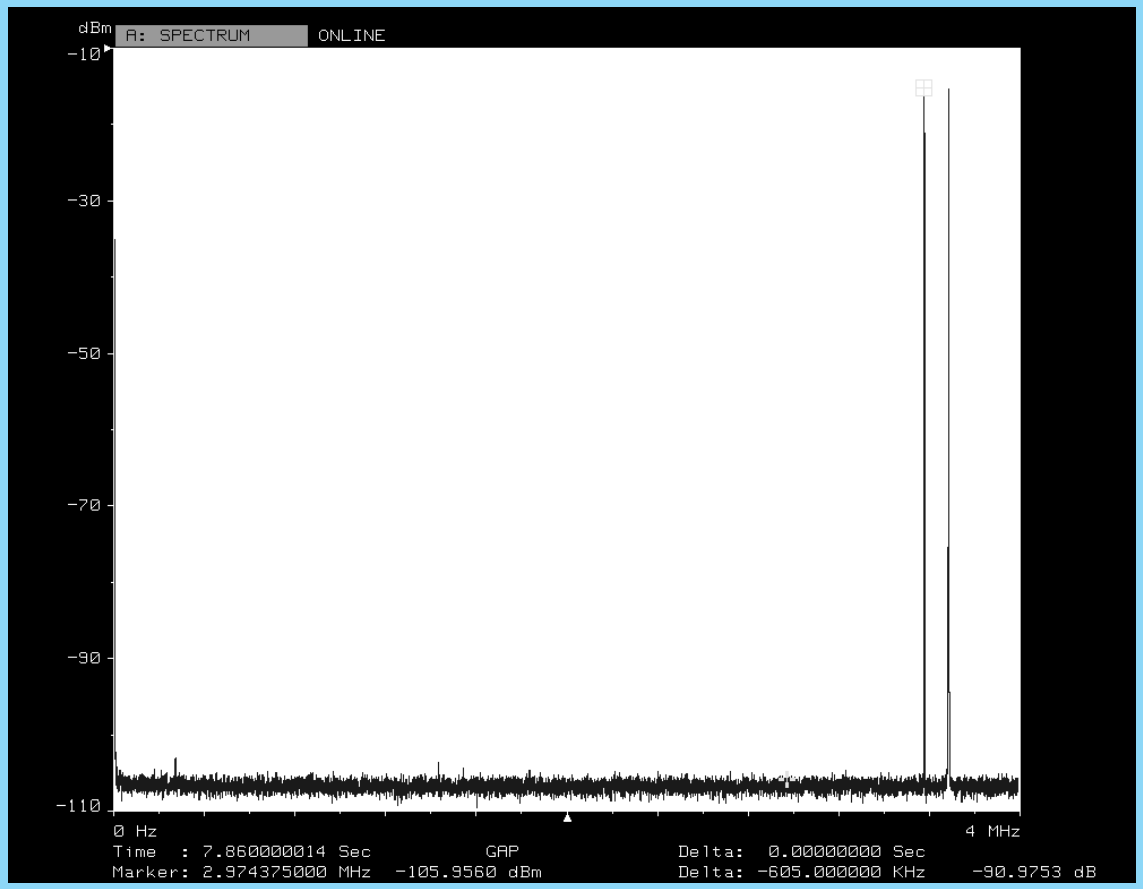
CMOS-26
26MSa/s max REAL TIME rate
24x 15th order filters
520M ops/sec
Typical spurs ⩽-125dBc

Digital Filter Magnitude Response



Magnitude Response of E1430A Digital Filter
(Zoom Mode, 5 Decimations)

2-Tone Intermodulation Example



Input Range:	+4dBm
Span:	4.00 MHz
Averages:	50 rms
Window:	Hanning
Block Size:	32K sample
# Bins:	12800
Bin Spacing:	312.5 Hz

ADC Error Sources

Non-Linearity

SPECTRUM OF HIGH ORDER NON-LINEARITIES

OUTPUT FROM 10MHz, 70dB SNR ADC

8192 POINT FFT WITH P400 WINDOW