MDC44ST
Super SRAM Dual C44
User Guide

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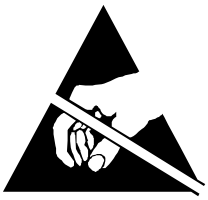

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1. INTRODUCTION

1.1. Purpose of This Manual

This manual provides the information you need to use Spectrum's MDC44ST Twin TMS320C44 ('C44) module. It describes the module's features, architecture, and specifications; and shows you how to install and configure it for your applications.

1.2. If You Need Help

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- The name and version number of all Spectrum software components
- The minimum amount of code that demonstrates the problem
- The version number of all software packages, including compilers and operating systems

1.3. Basic MDC44ST Overview

Spectrum's MDC44ST module is a single-width TIM-40 module equipped with two TMS320C44 DSPs, two 32K PEROMs, and up to 8 megabytes of SRAM. It is intended as a general use, parallel processing, expansion card for applications using two 'C44 DSPs.

The MDC44ST module is available in a variety of memory and processor speed configurations. These configurations are summarized in Table 1.

Table 1 MDC44ST Configurations

Model	RAM Size	Process Speed
MDC44ST3-50	2 MB	50 MHz
MDC44ST3.5-50	5 MB	50 MHz
MDC44ST4-50	8 MB	50 MHz
MDC44ST3-60	2 MB	60 MHz

1.4. Feature Summary

- Single-width TIM-40 module
- Two TMS320C44 DSPs (Refer to the TMS320C4x User's Guide for details)
- One 32K PEROM for each 'C44
- One bank of local bus SRAM (0.5 MB or 2 MB) for each 'C44
- One bank of global bus SRAM (0.5 MB or 2 MB) for each 'C44
- Global bus connector for the first 'C44
- 50 MHz or 60 MHz processor speed options
- Six communication ports available via the TIM-40 connectors (Three from each 'C44)
- Inter-processor interface provided by connecting a communication port from each 'C44 together.

1.5. TIM-40 Module Specification

The MDC44ST is a single-width TIM-40 module with three 80-way connectors. The TIM-40 standard provides physical, electrical interface, and system characteristics for module development. Modules are installed on TIM-40 carrier

boards which connect the modules to each other and to the host system. Spectrum offers a variety of TIM-40 carrier boards for use in PCI, PC-ISA, VMEbus, VXI, and other host systems.

For more information about the TIM-40 module, refer to the TIM-40 TMS320C4x Module Specification Version 1.01 available from Texas Instruments.

2. INSTALLATION

2.1. Setting the Module's Switches

Several MDC44ST features are configured through switches. Configure the features according to the following sections, using the information provided in Figure 1 and Table 2 for reference.

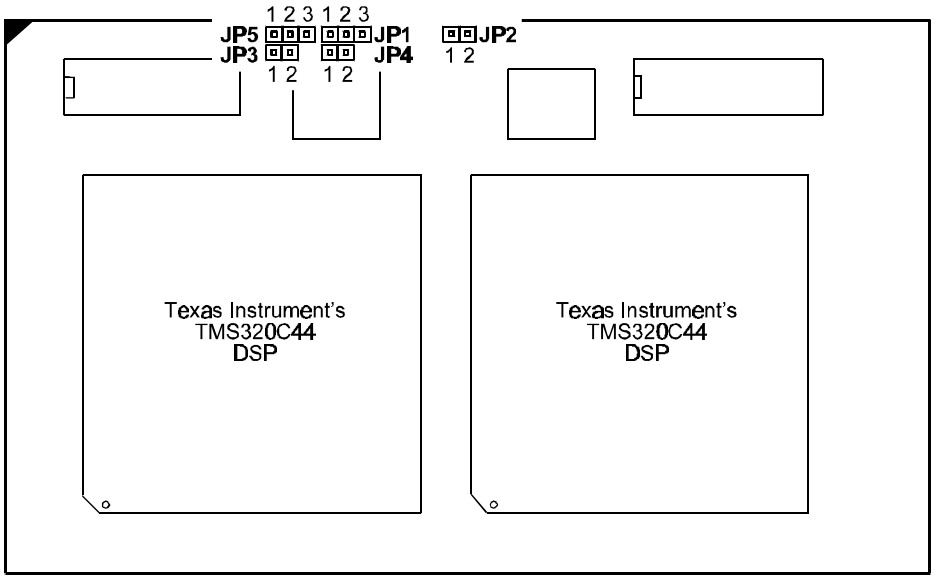

Figure 1 MDC44ST Board Layout and Jumper Locations

Table 2 MDC44ST Jumper Settings

Jumper	C44	Pins	Function
JP1	A+B	1-2	Use External Clock for C44-A and B
		2-3 *	Use Internal Clock for C44-A and B
JP2	A	OUT*	C44-A Boot data from first active communication port
		IN	C44-A Boot data from PEROM at address 0x4000 0000
JP3	B	OUT*	C44-B Boot data from first active communication port
		IN	C44-B Boot data from PEROM at address 0x4000 0000
JP4	B	OUT*	C44-B Disable NMI
		IN	C44-B Enable NMI
JP5	A+B	1-2*	Enable IIOF0 for C44-A
		2-3	Enable IIOF0 for C44-B

* Default

2.1.1.Clock Source

The module's clock signal (for both 'C44s) can be taken from its own internal oscillator or an external source depending upon jumper JP1.

- Set JP1 to select the internal or an external clock source.

2.1.2.Boot Data Source

Upon power up or reset, each 'C44 DSP must load its boot program into memory. The source of this data will either be the 'C44's on-board PEROM or a communication port. When set to boot from its PEROM, the IIOF2 interrupt line is pulled low which causes the 'C44 to start loading from address 0x4000 0000. When set to boot from a communication port, IIOF2 is pulled high which causes the 'C44 to load data from the first TIM-40 communication port that it sees active.

1. Set JP2 to select the boot data source for 'C44-A as either the on-board PEROM or to the first active communication port.

2. Set JP3 to select the boot data source for 'C44-B as either the on-board PEROM or to the first active communication port.

2.1.3.C44-B Non-Maskable Interrupt (NMI) Enable

The NMI pin from each 'C44 is connected to the TIM-40 connector. The NMI from 'C44-A cannot be disabled, but the NMI from 'C44-B can be enabled and disabled by jumper JP4.

- Set JP4 to either enable or disable the NMI from 'C44-B.

2.1.4.Interrupt IIOF0 Selection

The IIOF0 signal on the primary TIM-40 connector can be connected to the IIOF0 pin of either C44-A or 'C44-B by jumper JP5.

- Set JP5 to connect the II0F0 pin of the TIM-40 connector to either 'C44-A or to 'C44-B.

2.2. Installing the module on to the Carrier Board

1. Locate the TIM-40 site on the carrier board in which the module will be installed.

2. Align the module over its TIM-40 site on the carrier board so that the triangle printed on the top right corner of the module PCB is adjacent to the top primary connector of the carrier board.

3. Ensure that the connectors are properly aligned and gently push the module on to the connectors.

4. Fasten the module to the carrier board with the spacers provided with the module. There are two holes for these spacers at diagonal corners of the TIM-40 site. Screw the spacers between the module and the carrier board at these two holes. Do **not** overtighten.

3. MODULE ARCHITECTURE

The single-width MDC44ST TIM-40 module hosts two TMS320C44 digital signal processors: ‘C44-A and ‘C44-B. Each ‘C44 has a 32K PEROM, up 2 MB of local SRAM, and up to 2 MB of global SRAM. The Global Page Register on ‘C44-A allows it to access the full address range on the Global Connector. The general architecture of the module is shown in Figure 2 MDC44ST Block Diagram.

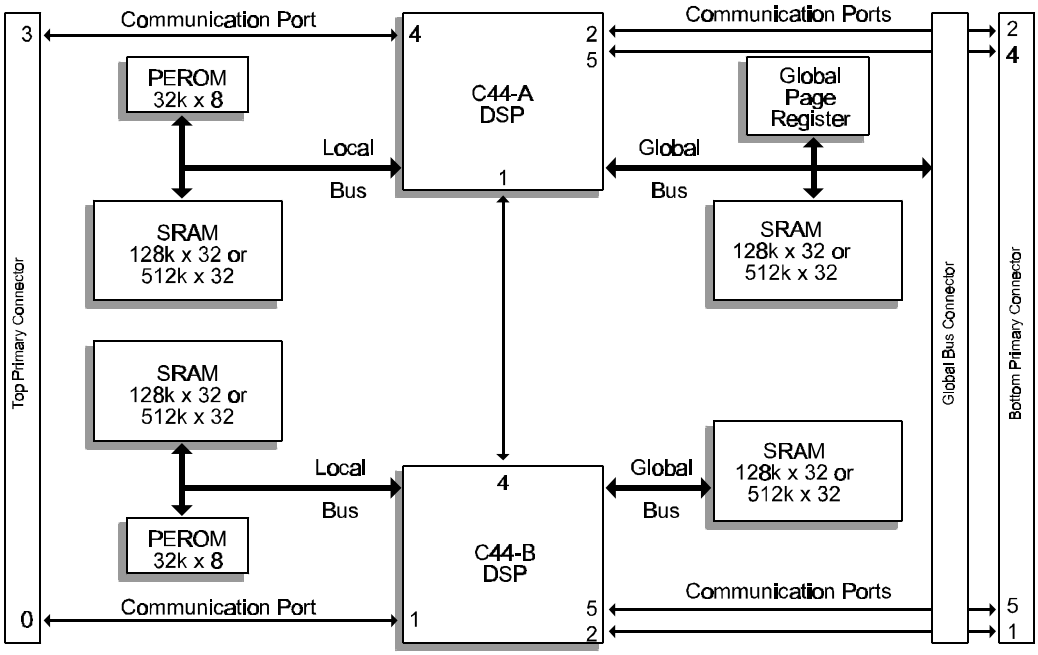

Figure 2 MDC44ST Block Diagram

3.1. Digital Signal Processors

Each TMS320C44 DSP (‘C44) has four 20 Mbps parallel communication ports, a local and global memory bus, and a set of interrupt and control lines. Complete information on the C44 can be found in Texas Instrument’s TMS320C44 User Guide.

An on-board clock circuit provides the clock signal for the module, but can be disconnected from both ‘C44s via a jumper to allow an external clock source to be used by that ‘C44.

Communication port 1 from ‘C44-A is connected to communication port 4 of ‘C44-B to enable inter-processor communication. The three remainging communication ports from each ‘C44 are assigned to ports on the TIM-40 connectors.

3.2. Optimizing DSP Performance

The *TMS320C4x User's Guide* provides several suggestions for optimizing performance, including:

- Enabling the 'C40's internal instruction cache
- Using DMA to transfer data in memory
- Isolating code and data on separate busses (global and local)
- Placing time-critical code and data into the 2 internal memory banks

3.3. Memory Interface

On each 'C44 the local memory is addressed from 0x0000 0000 to 0x7FFF FFFF, and global memory from 0x8000 0000 to 0xFFFF FFFF. Memory interface registers in the local address bus configure the busses for wait states, page size, and strobe line activation. Complete details about the 'C44 busses and the their interface control registers can be found in Chapter 7 of the *TMS320C4x User's Guide.*

The following table shows the memory devices and I/O functions located on the local and global busses of the 'C44.

Local Bus	Global Bus
• Internal Boot Loader ROM	• Global SRAM
• Internal Peripherals	• 'C44-A Global Page Register ('C44-A only)
• Local SRAM	• Global Expansion Bus ('C44-A only)
• PEROM	

The global and local memory address busses each have one bank of external memory. Each bank consists of four memory devices. Table 3 shows which banks are used for the different configurations of the MDC44ST.

Table 3 MDC44ST RAM Configurations

Model	DSP Speed	Total RAM on Module	Local RAM per 'C44	Global RAM per 'C44
MDC44ST3-50	50 MHz	2 MB	128K x 32	128K x 32
MDC44ST3.5-50	50 MHz	5 MB	512K x 32	128K x 32
MDC44ST4-50	50 MHz	8 MB	512K x 32	512K x 32
MDC44ST3-60	60 MHz	2 MB	128K x 32	128K x 32

3.3.1.Global Page Register

The TIM-40 specification defines a 31-bit address (A[0..30]) on the Global Connector. The 24-bit global address bus available on the C44-A is extended to meet this specification with a 7- bit Global Page Register. Figure 3 shows how this page register extends the bus.

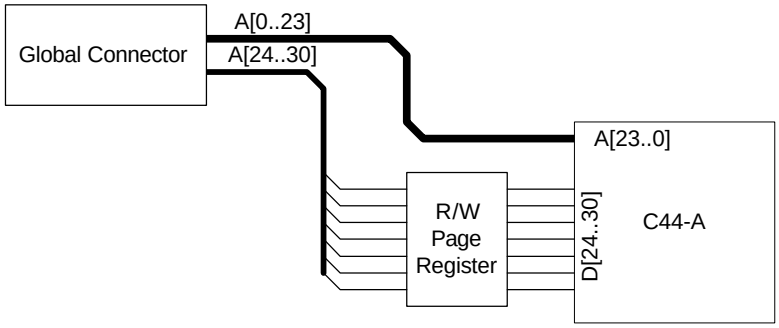

Figure 3 Page Register Functional Block Diagram

The page register is memory mapped to address 0x8010 0000 of C44-A, and is aliased through address 0x801F FFFF. On C44-B, this address space is reserved. Bits 0 to 6 of the global page register output are connected to bits 24 to 30 of the global address bus. When writing to the page register, the data lines D[24..30] correspond to the page to be accessed on the global bus. During a read from the page register, only D[24..30] are defined, the remaining bits, D31 and D[23..0] remain undefined.

Note: This register is accessed via /STRB0. Therefore, the Global Memory Interface Control Register value must reflect this fact, or else the Global Page Register will be unavailable.

Upon reset, the Global Page Register is set to all 1's; this covers addresses 0xFF00 0000 to 0xFFFF FFFF. To access an address outside this range, change the value of the Global Page Register to present the appropriate upper 7 bits to the global address bus.

3.3.2.Memory Maps

Each configuration of the MDC44ST has a slightly different memory map due to their different memory sizes. The following figures show the memory maps for the four MDC44ST configurations. In addition to addressing, the memory maps also show the number of wait states and strobe lines used for each address range

assignment. The memory map represents both ‘C44-A and ‘C44-B on the module.

	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	Peripherals (Internal)	0	-
	0x0010 0000 - 0x002F F7FF	Reserved	-	-
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0031 FFFF	External Local SRAM (128K x 32)	0	LSTRB0
	0x0032 0000 - 0x3FFF FFFF	RESERVED	-	LSTRB0
	0x4000 0000 - 0x4000 7FFF	PEROM	5	LSTRB1 LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED		-
	0x7000 0000 0x7000 7FFF	ID ROM	5	LSTRB1 LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	-
Global Bus	0x8000 0000 - 0x8001 FFFF	Global SRAM (128K × 32)	0	STRB0
	0x8002 0000 - 0x800F FFFF	Reserved	-	STRB0
	0x8010 0000 - 0x801F FFFF	C44-A: Global Page Register C44-B: Reserved	0	STRB0
	0x8020 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 4 MDC44ST3-50 Memory Map

	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	Peripherals (Internal)	0	-
	0x0010 0000 - 0x002F F7FF	Reserved	-	-
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0037 FFFF	External Local SRAM (512K x 32)	0	LSTRB0
	0x0038 0000 - 0x3FFF FFFF	RESERVED	-	LSTRB0
	0x4000 0000 - 0x4000 7FFF	PEROM	5	LSTRB1 LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED	-	-
	0x7000 0000 - 0x7000 7FFF	ID ROM	5	LSTRB1 LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	-
Global Bus	0x8000 0000 - 0x8001 FFFF	Global SRAM (128K × 32)	0	STRB0
	0x8002 0000 - 0x800F FFFF	Reserved	-	STRB0
	0x8010 0000 - 0x801F FFFF	C44-A: Global Page Register C44-B: Reserved	0	STRB0
	0x8020 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 5 MDC44ST3.5-50 Memory Map

	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	Peripherals (Internal)	0	-
	0x0010 0000 - 0x002F F7FF	Reserved	-	-
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0037 FFFF	External Local SRAM (512K x 32)	0	LSTRB0
	0x0038 0000 - 0x3FFF FFFF	RESERVED	-	LSTRB0
	0x4000 0000 - 0x4000 7FFF	PEROM	5	LSTRB1 LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED	-	-
	0x7000 0000 - 0x7000 7FFF	ID ROM	5	LSTRB1 LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	-
Global Bus	0x8000 0000 - 0x8007 FFFF	Global SRAM (512K × 32)	0	STRB0
	0x8008 0000 - 0x800F FFFF	Reserved	-	STRB0
	0x8010 0000 - 0x801F FFFF	C44-A: Global Page Register C44-B: Reserved	0	STRB0
	0x8020 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 6 MDC44ST4-50 Memory Map

	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	Peripherals (Internal)	0	-
	0x0010 0000 - 0x002F F7FF	Reserved	-	-
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0031 FFFF	External Local SRAM (128K x 32)	0	LSTRB0
	0x0032 0000 - 0x3FFF FFFF	RESERVED	-	LSTRB0
	0x4000 0000 - 0x4000 7FFF	PEROM	5	LSTRB1 LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED		-
	0x7000 0000 0x7000 7FFF	ID ROM	5	LSTRB1 LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	-
Global Bus	0x8000 0000 - 0x8001 FFFF	Global SRAM (128K × 32)	0	STRB0
	0x8002 0000 - 0x800F FFFF	Reserved	-	STRB0
	0x8010 0000 - 0x801F FFFF	C44-A: Global Page Register C44-B: Reserved	0	STRB0
	0x8020 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 7 MDC44ST3-60 Memory Map

3.3.3.Local Memory Interface Control Register

The value programmed into the Local Memory Interface Control Register (located at address 0x0010 0004h) of both 'C44s is **0x3D74 A850**. This value is used for all MDC44ST configurations, except if the PEROM is being programmed.

During PEROM programming, this value is changed to 0x3E74 AD50 by the PEROM programming code. Spectrum's PEROM Utility automatically sets this value, so this value does not have to be entered when the utility is used.

The following table is a brief description of each set of values in the Control Register. A more detailed explanation of each register may be found in the *TMS320C40 User's Guide.*

Table 4 Local Memory Interface Control Register Value

Bit	Register	Default Value
3..0	RESERVED	Read only - Write '0000' Consult C4x User Guide for details
5..4	LSTRB0 SWW	'01' - Internal wait states
7..6	LSTRB1 SWW	'01' - Internal wait states
10..8	LSTRB0 WTCNT	'000' - Zero wait states for RAM *'101' - Five wait states for PEROM write*
13..11	LSTRB1 WTCNT	'101' - Five wait states for PEROM
18..14	LSTRB0 PAGESIZE	'10010' - 512K page size
23..19	LSTRB1 PAGESIZE	'01110' - 32K page size
28..24	LSTRB0 ACTIVE	'11101' /LSTRB0 active from 0x0030 0000 to 0x3FFF FFFF /LSTRB1 active from 0x4000 0000 to 0x7FFF FFFF *'11110' /LSTRB0 active from 0x0030 0000 to 0x7FFF FFFF* *for PEROM writes only*
29	LSTRB0 SWITCH	'1' insert cycle between accesses on different pages to provide address decode timing requirements
31..30	RESERVED	Read only - Write '00' Consult C4x User Guide for details

3.4. Global Memory Interface Control Register

Although the global bus of C44-A and C44-B do not contain the same devices, they are configured with the same Global Memory Interface Control Register value. The value programmed into the Global Memory Interface Control Register (located at address 0x0010 0000h) of both 'C44s is **0x344C 8010**. This value is used for all MDC44ST configurations. This value can be changed to accommodate the actual memory map of the carrier board being used.

On C44-A, the /STRB0 line is used to access one bank of SRAM and the global page register, both of which are zero wait state operations. /STRB1 of the C44-A global bus is connected to the global TIM-40 connector for operations on the carrier board. There is only one bank of zero wait state SRAM on the C44-B global bus.

Note: Ensure that /STRB0 is used with the Global Page Register, or the register will be unavailable.

Table 5 Global Memory Interface Control Register Value

Bit	Register	Default Value
3..0	RESERVED	Read only - Write '0000' Consult C4x User Guide for details
5..4	STRB0 SWW	'01' - Internal wait states
7..6	STRB1 SWW	'00' - External wait states
10..8	STRB0 WTCNT	'000' - Zero wait states for RAM
13..11	STRB1 WTCNT	'000' - Zero - externally controlled
18..14	STRB0 PAGESIZE	'10010' - 512K page size
23..19	STRB1 PAGESIZE	'01001' - 1K page size - Carrier Board Dependent
28..24	STRB0 ACTIVE	'10100' /STRB0 active from 0x8000 0000 to 0x801F FFFF /STRB1 active from 0x8020 0000 to 0xFFFF FFFF
29	STRB0 SWITCH	'1' insert cycle between accesses on different pages to provide address decode timing requirements
31..30	RESERVED	Read only - Write '00' Consult C4x User Guide for details

3.5. Interrupts

Because the TIM-40 connector accommodates only the first three IIOF lines from only one C4x DSP, not all IIOF lines are assigned to the connector. IIOF0 on the connector can be assigned to either 'C44-A or 'C44-B, depending upon jumper JP5. IIOF1 and IIOF2 on the connector are only assigned to 'C44-A. The IIOF3 lines from both 'C44s are logically AND'd to generate the /CONFIG signal, which goes off-module to the carrier board.

3.6. 32K PEROM

Each 32K PEROM is programmed as an ID ROM according to the TIM-40 specifications. They can, however, be reprogrammed with user code using the DB40 debugger and the PEROM Utility programs included in the MDC44ST Developer's Kit software. Instructions on programming the PEROMs used on Spectrum TIM-40 modules can be found in the PEROM Utility Guide.

The Atmel AT29C256 Flash Programmable and Erasable Read Only Memory (PEROM) is used as the PEROM device. It is an 8-bit wide device using data bits

LD0 to LD7 and occupying addresses 0x4000 0000 to 0x4000 7FFF on the local bus, and is also aliased from 0x7000 0000 to 0x7000 7FFF for IDROM accesses.

3.7. JTAG Emulation Interface

The TMS320C44 integrates the IEEE 1149.1 JTAG interface for test, emulation, and programming the 32K PEROM. All seven lines of the JTAG interface are supported on the top primary connector of the TIM-40 module. To accommodate both 'C44s on the MDC44ST the serial data for JTAG is routed as shown in Figure 8.

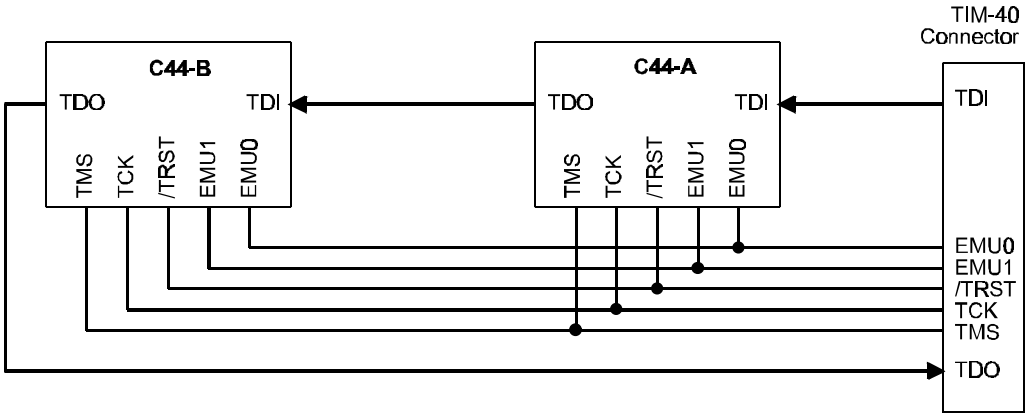

Figure 8 JTAG Connection

The JTAG Test Data Input and Output signals (TDI and TDO) are daisy-chained through C44-A and C44-B. The TDI signal from the module's TIM-40 connector is routed first to the TDI pin of C44-A. It is then passed out of the C44-A TDO pin to the TDI pin of C44-B. The TDO pin of C44-B is connected to the TDO pin of top primary connector. The remaining JTAG signals are connected in parallel to the two 'C44s.

Note: Although TDI from the top primary connector is connected to C44-A, JTAG views C44-A as the last in the JTAG scan chain. Therefore, C44-A should be placed after the entry for C44-B in any chain descriptor file, such as `board.cfg` for TI's DB40 utility.

In order to use the JTAG facility, a Texas Instruments' Test Bus Controller device (SN74ACT8990) is required either on the motherboard or via Texas Instruments' XDS510 emulation system board.

3.8. Communication Ports

The four communication ports from each 'C44 are assigned to the six communication ports on the TIM-40 as shown in Figure 9 and Table 6.

Communication port 1 from C44-A is connected to communication port 4 of C44-B for inter-processor communication.

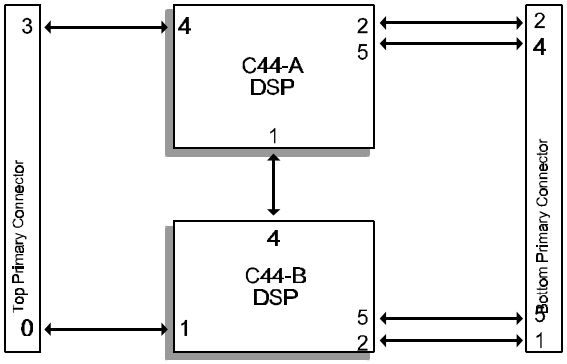

Figure 9 Communication Port Assignment

Table 6 Communication Port Assignment

TIM-40 Connector	C44 Communication Port
Communication Port 0	C44-B Port 1
Communication Port 1	C44-B Port 2
Communication Port 2	C44-A Port 2
Communication Port 3	C44-A Port 4
Communication Port 4	C44-A Port 5
Communication Port 5	C44-B Port 5

3.9. Power Up and Reset

After power up, the ‘C44s are reset and run the boot loader programs from their internal ROM. The boot loader takes source program data from either the 8-bit PEROM at address 0x4000 0000 or from the first communication port to go active. This source of boot data is configurable for each DSP with jumpers as described in the Installation chapter.

If the PEROM is used to bootstrap the DSP, it cannot be used as an ID ROM and vice versa. The boards are shipped with PEROM programmed to be the ID ROM. Refer to the TIM-40 specification for more information regarding the ID ROM.

The source program data specifies the width of the memory device, values for the local and global memory interface control registers, pointers to the interrupt and trap vector tables, as well as blocks of program data. Refer to the *TMS320C4x User’s Guide* for details.

4. SPECIFICATIONS

4.1. Functional Specifications

Model	MDC44ST3-50	MDC44ST3.5-50	MDC44ST4-50	MDC44ST3-60
DSPs (Two)	TMS320C44	TMS320C44	TMS320C44	TMS320C44
Clock Speed	50 MHz	50 MHz	50 MHz	60 MHz
RAM	2 MB	5 MB	8 MB	2 MB
PEROM	32 kB	32 kB	32 kB	32 kB
MFLOPS	100	100	100	120

4.2. Electrical Specifications

Supply Voltage +5.0V ± 5% at 1.0 A typical

4.3. Mechanical Specifications

Single-width TIM-40 module.

Length 4.2” (106.7 mm)

Width 2.5” (64.2 mm)

Component and mated connector height limits:

Top 0.210” (5.33 mm)

Bottom: 0.150” (3.81 mm)

4.4. Environmental Specifications

Operating Temperature with Forced Air 0 to 40° C

Storage Temperature: -25 to 80° C

Operational Humidity: 10% to 80% non-condensing

It is assumed that there will be forced air cooling within the product chassis. A high air velocity is required for proper cooling of this module.

4.5. TIM-40 Interface Connectors

Three 80-pin Hirose Electric FX-4 TIM-40 connectors provide the interface between the module and the carrier board according to Texas Instruments TIM-40 TMS320C4x Module Specification Version 1.01. Table 7 shows how the different functions on the primary TIM-40 connectors are assigned to the MDC44ST. The global connector fully supports the TIM-40 specification and is therefore not described.

Table 7 TIM-40 Interface Function Assignment

TIM-40 Interface Function	Primary Connectors
Communication Port 0	C44-B Port 1
Communication Port 1	C44-B Port 2
Communication Port 2	C44-A Port 2
Communication Port 3	C44-A Port 4
Communication Port 4	C44-A Port 5
Communication Port 5	C44-B Port 5
JTAG	C44-A and C44-B
/RESET	C44-A and C44-B
IIOF0	C44-A or C44-B
IIOF1	C44-A Only
IIOF2	C44-A Only
IACK	C44-A Only
NMI	C44-A Only or (C44-A and C44-B)
CONFIG	Logically AND'd from IIOF3 of both 'C44s
TCLK0	C44-A Only
TCLK1	C44-A Only
Clock Output H1	C44-A Only
Clock Output H3	C44-A Only
User Defined Pins	NC
Power (+5 V)	1.0 A typical
Power (+12 V)	NC
Power (-12 V)	NC