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**HP 75000 SERIES C**

# **HP E1451/E1452 20MHz Pattern I/O Modules**

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## **Hardware Manual**



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E1451-90002  
E0294

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## Declaration of Conformity

*According to ISO/IEC Guide 22 and EN 45014*

The Hewlett-Packard Company declares that the HP 75000 Model D20 E145xA Series modules and pods conforms to the following Product Specifications.

Safety: IEC 1010-1 (1990) Incl. Amend 1 (1992)/EN61010 (1993)  
CSA C22.2 #1010.1 (1992)  
UL 1244

EMC: CISPR 11:1990/EN 55011 (1991): Group 1 Class A  
IEC 801-2:1991/EN 50082-1 (1992): 4kVCD, 8kVAD  
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m  
IEC 801-4:1988/EN 50082-1 (1992): 1kV Power Line

Supplementary Information: The product herewith complies with the requirements of the low voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Tested in a typical configuration in an HP C-size VXI mainframe.

  
Q.A. Manager  
February 1994

Hewlett-Packard Company  
P.O. Box 301  
815 14th Street S.W.  
Loveland, Colorado 80539 U.S.A.

## Printing History

The Printing History shown below lists all Editions and Updates of this manual and the printing date(s). The first printing of the manual is Edition 1. The Edition number increments by 1 whenever the manual is revised. Updates, which are issued between Editions, contain replacement pages to correct the current Edition of the manual. Updates are numbered sequentially starting with Update 1. When a new Edition is created, it contains all the Update information for the previous Edition. Each new Edition or Update also includes a revised copy of this printing history page. Many product updates or revisions do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

Edition 1 (Part Number E1451-90001) ..... June 1991

Edition 2 (Part Number E1451-90002) ..... February 1994

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## Safety Symbols



Instruction manual symbol affixed to product. Indicates that the user must refer to the manual for specific Warning or Caution information to avoid personal injury or damage to the product.



Indicates the field wiring terminal that must be connected to earth ground before operating the equipment—protects against electrical shock in case of fault.



OR



Frame or chassis ground terminal—typically connects to the equipment's metal frame.



Alternating current (AC).



Direct current (DC).



Indicates hazardous voltages.

### WARNING

Calls attention to a procedure, practice, or condition that could cause bodily injury or death.

### CAUTION

Calls attention to a procedure, practice, or condition that could possibly cause damage to equipment or permanent loss of data.

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## WARNINGS

The following general safety precautions must be observed during all phases of operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the product. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

**Ground the equipment:** For Safety Class I equipment (equipment having a protective earth terminal), an uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

**DO NOT operate the product in an explosive atmosphere or in the presence of flammable gases or fumes.**

For continued protection against fire, replace the line fuse(s) only with fuse(s) of the same voltage and current rating and type. DO NOT use repaired fuses or short-circuited fuse holders.

**Keep away from live circuits:** Operating personnel must not remove equipment covers or shields. Procedures involving the removal of covers or shields are for use by service-trained personnel only. Under certain conditions, dangerous voltages may exist even with the equipment switched off. To avoid dangerous electrical shock, DO NOT perform procedures involving cover or shield removal unless you are qualified to do so.

**DO NOT operate damaged equipment:** Whenever it is possible that the safety protection features built into this product have been impaired, either through physical damage, excessive moisture, or any other reason, REMOVE POWER and do not use the product until safe operation can be verified by service-trained personnel. If necessary, return the product to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

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**DO NOT substitute parts or modify equipment:** Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

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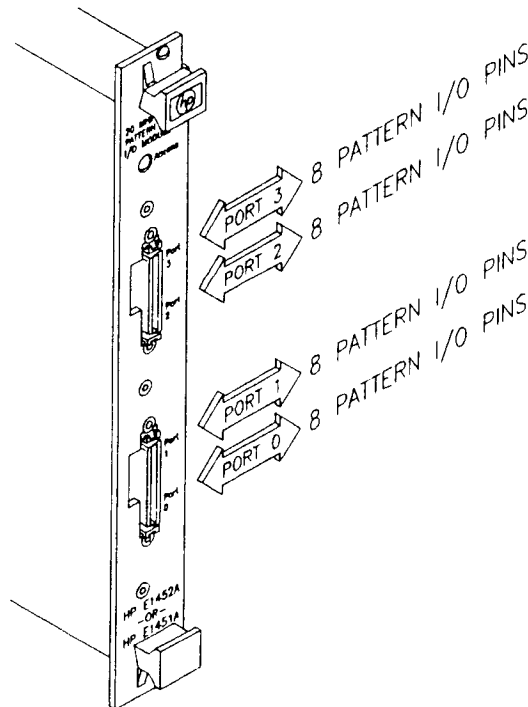
**Hardware Descriptions**

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# HP E1451/E1452 Pattern I/O Hardware Description

The HP E1451 and HP E1452 are identical except that the HP E1451 passes along the Local Bus pattern clocks to the next module whereas the HP E1452 terminates the pattern clock lines. The HP E1452 Terminating Pattern I/O Module must be the last module of the Pattern I/O module set so the Local Bus is properly terminated when the HP E1450 Timing Module is used. If external timing is used in lieu of the timing module, then only the HP E1451 Pattern I/O module is required.



**Figure 1-1. HP E1451/E1452 Pattern I/O Module**



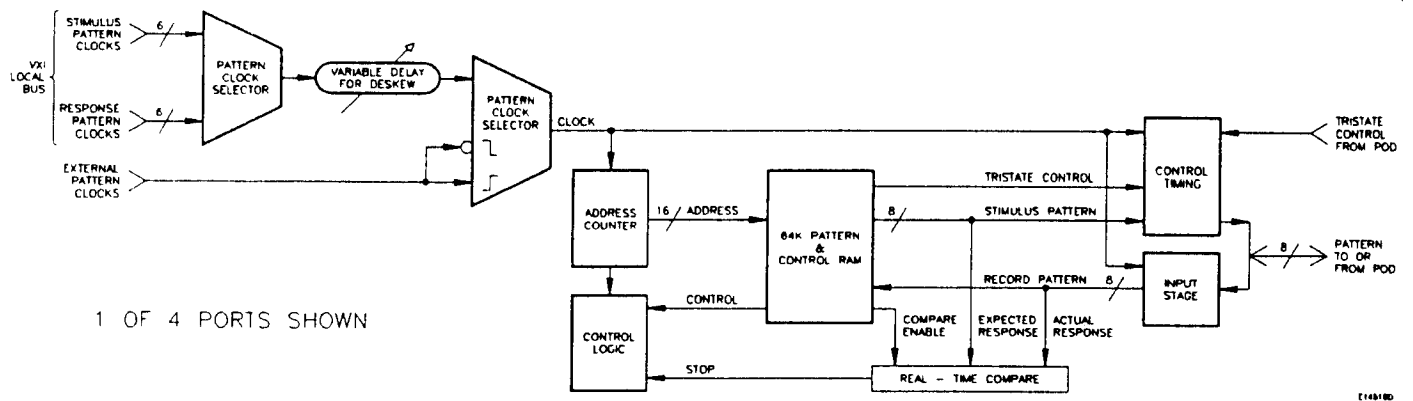


Figure 1-2. Pattern I/O Block Diagram

## HP E1454 Pattern I/O Pod Description

The optional HP E1454 Pattern I/O Pod (Figure 1-3) extends measurement accuracy to a DUT located up to two meters from the front panel of the Model D20. The pods buffer the input and output signals for two of the four HP E1451/E1452 I/O ports. This improves the Model D20's ability to drive DUT inputs and minimizes loading on DUT outputs. Response pattern clocks are delayed relative to the stimulus pattern clocks by the Timing Module so that timing is correct at the DUT. And pin-to-pin skew on the pattern I/O lines is compensated, based on constants stored in the pod's calibration memory. The pattern I/O pods also provide inputs for tri-state control and external clock. The HP E1454 is supplied with a 2.1-meter cable. Two HP E1454 pods are required for each HP E1451/E1452 in the Model D20.

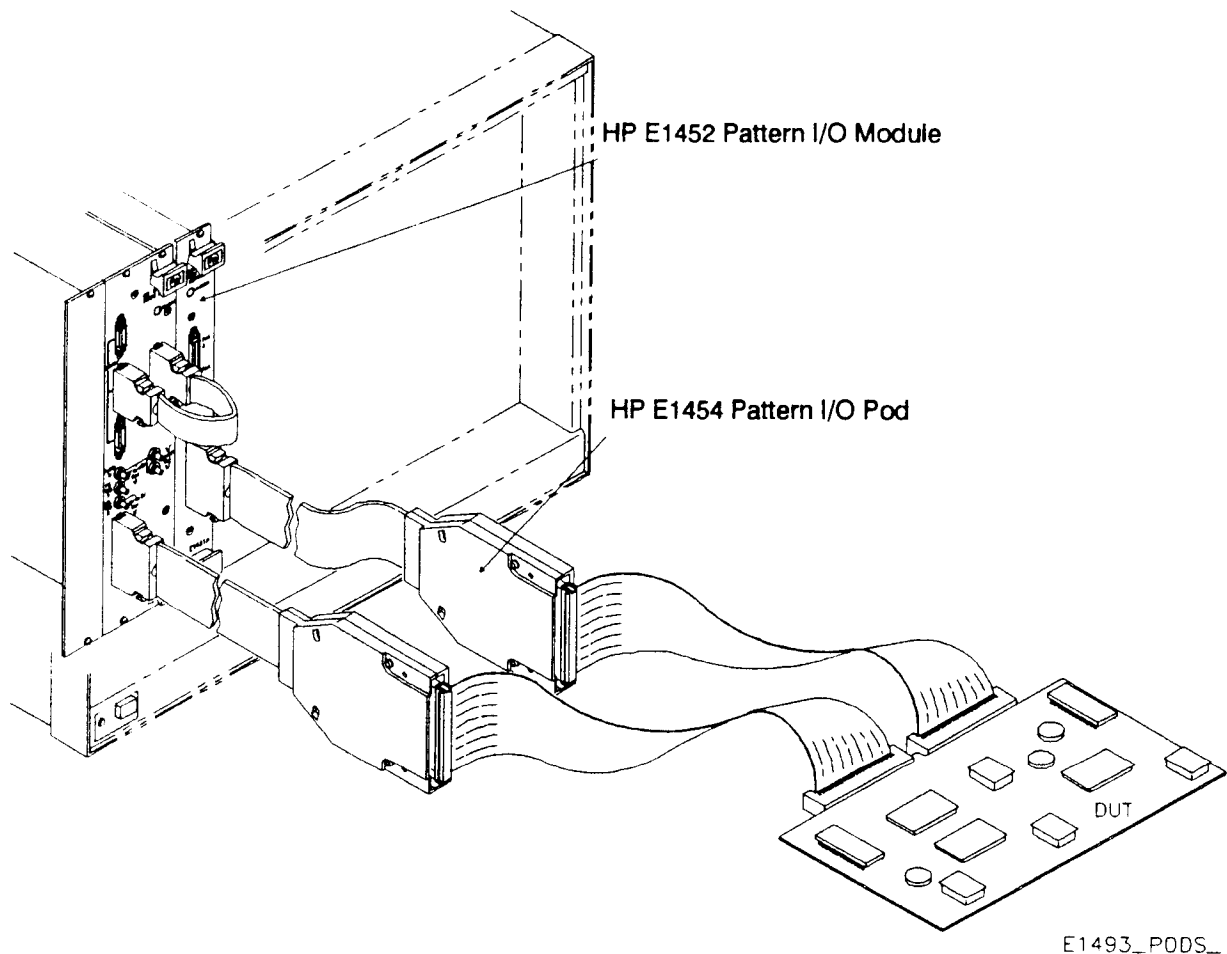


Figure 1-3. Pattern I/O Module/Pod

## Using the HP E1451/E1452 as a Stand-Alone Instrument

You can use the pattern module as a stand-alone digital I/O instrument without the need for an HP E1450 Timing Module. In this configuration, the pattern module must have a logical address that is a direct multiple of 8 (i.e., 8, 16, 24, 32, . . . 240). You must also use an external clock source since the Timing Module is not present (refer to "Using External Clocks" in chapter 3 of the Model D20 Task and Command Reference). When used as a stand-alone instrument, the pattern module is capable of executing only those commands shown in Table 1-1. Refer to the Command Reference, chapter 4 of the Model D20 Task and Command Reference Manual for details about these commands.

→ PN E1493 - 90030  
includes this manual

**Table 1-1. Stand-Alone Pattern Module Command Set**

**DIGital Subsystem**

**:GROup**

```
:CATalog?
:DEFine <name>,<port_list>
:DEFine? <group_name>
:DELetE:ALL
:DELetE[:NAME] <group_name>
:MODE RESPonse|STIMulus
:MODE?
[:SElect] <group_name>|NONE
[:SElect]?

```

**:RESPonse**

```
:COMParE
:ENABle
:SEquence
[:FULL] <boolean_block>
[:FULL]?
:PARTial <start_vector>,<count>|ON|OFF{,<start_vector>,<count>}
:PARTial? <start_vector>,<count>
:REPeat <start_vector>,<count>,<count>,<count>|ON|OFF
[:STATe] 1|0|ON|OFF
[:STATe]?
:ERRor?
:MASK[:VALue] <pattern_value>
:MASK[:VALue]?
:PATtern
:SEquence
[:FULL] <pattern_block>
[:FULL]?
:PARTial <start_vector>,<pattern_value>
{,<pattern_value>}
:PARTial? <start_vector>,<count>
:REPeat <start_vector>,<count>,<pattern_value>
[:VALue]?
:CLOCK
:EXTernal:SLOPe POSitive|NEGative
:EXTernal:SLOPe?
:SOURce HOLD|EXTernal
:SOURce?

```

**:SEquence**

```
:CATalog?
:DEFine <name>,<#_vectors>
:DEFine? <seq_name>
:DELetE:ALL
:DELetE[:NAME] <seq_name>
:POSition?
[:SElect] <seq_name>|NONE
[:SElect]?
:WINDow
:BOUNDary <start_vector>,<stop_vector>
:BOUNDary?
[:STATe] 1|0|ON|OFF
[:STATe]?

```

**:STIMulus**

```
:ENABle
:SEquence
[:FULL] <boolean_block>
[:FULL]?
:PARTial <start_vector>,<count>|ON|OFF{,<start_vector>,<count>}
:PARTial? <start_vector>,<count>
:REPeat <start_vector>,<count>,<count>,<count>|ON|OFF

```

```
[:VALue] 1|0|ON|OFF
[:VALue]?
:PATtern
:SEquence
[:FULL] <pattern_block>
[:FULL]?
:PARTial <start_vector>,<pattern_value>
{,<pattern_value>}
:PARTial? <start_vector>,<count>
:REPeat <start_vector>,<count>,<pattern_valu>
[:VALue] <pattern_value>
[:VALue]?
:CLOCK
:EXTernal:SLOPe POSitive|NEGative
:EXTernal:SLOPe?
:SOURce HOLD|EXTernal
:SOURce?

```

**System Operation Commands**

```
RUN
STOP

```

**System Status, Management, and Test Commands**

**STATus**

```
:OPERation
[:EVENT]?
:CONDition?
:ENABle <pattern_value>
:ENABle?
:NTRansition <pattern_value>
:NTRansition?
:PTRansition <pattern_value>
:PTRansition?
:PRESet
:QUESTionable
[:EVENT]?
:CONDition?
:ENABle <pattern_value>
:ENABle?
:NTRansition <pattern_value>
:NTRansition?
:PTRansition <pattern_value>
:PTRansition?

```

**SYSTem**

```
:ERRor?
:PRESet
:VERSion?

```

**TEST**

```
[:ALL]?
:MODule? <module_#>

```

**Query Data Format Commands**

**FORMat**

```
[:DATA] ASCii|HEXadecimal|OCTal|BINary
[:DATA]?

```



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## Chapter 2

# Configuration and Wiring

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### Using this Chapter

This chapter contains configuration and wiring information for the HP E1451/E1452 Pattern I/O Modules, the optional HP E1454 Pattern I/O Pods, and the optional module to DUT interface cables. For complete details on installing this equipment in a C-Size mainframe, refer to the "HP 75000 Model D20 Hardware Installation Guide" and the "C-Size VXIbus Systems Installation and Getting Started Guide".

---

#### **WARNING**

**SHOCK HAZARD.** Only service-trained personnel who are aware of the hazards involved should install, remove, or configure the system. Before you perform any procedures in this guide, disconnect AC power and field wiring from the mainframe.

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#### **Caution**

**STATIC ELECTRICITY.** Static electricity is a major cause of component failure. To prevent damage to the electrical components in the mainframe and plug-in modules, observe anti-static techniques whenever handling a module.

---



# Configuration Information

This section shows you how to set the module's logical address switch.

## Logical Address Guidelines

- The HP E1450 Timing Module must have a Logical Address that is an Instrument Identifier. An Instrument Identifier is a Logical Address that is an exact multiple of 8 (i.e., 8, 16, 24, 32, . . . 240).
- HP E1451 Pattern I/O and E1452 Terminating I/O modules must have successive Logical Addresses beginning with the address of the Instrument Identifier. The HP E1452 Terminating I/O Module must have the highest Logical Address (last in the list).

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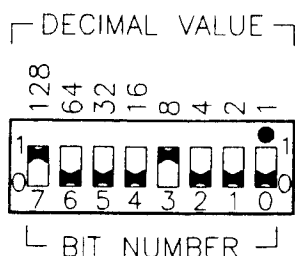
### NOTE

*When using an HP E1451 or E1452 as a stand-alone instrument (no other modules involved), it must have a Logical Address that is an Instrument Identifier (an exact multiple of 8).*

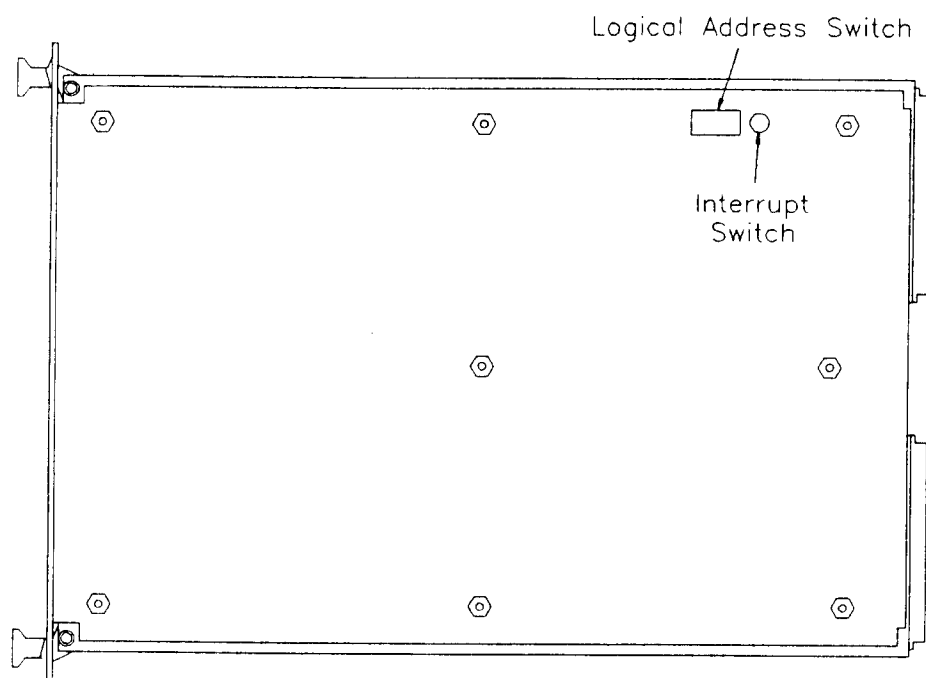
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## Logical Address Switch

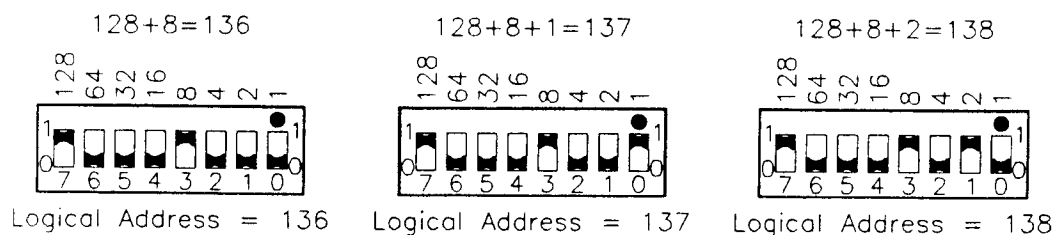
Figure 2-1 shows a Logical Address Switch. Notice that the switch is made up of 8 switches each having a decimal value. To determine the Logical Address, add the decimal values of all set switches. For example, if you set switches 7 and 3 to "1" (see Figure 2-1), the logical address is  $128 + 8 = 136$ . The HP-IB Secondary Address is determined by dividing the Instrument Identifier by 8. For example, if the Instrument Identifier logical address is 136, the Secondary Address is  $136 / 8 = 17$ . Figure 2-2 shows how to set the Logical Address switch.



**Figure 2-1. Logical Address Switch**



EXAMPLES:



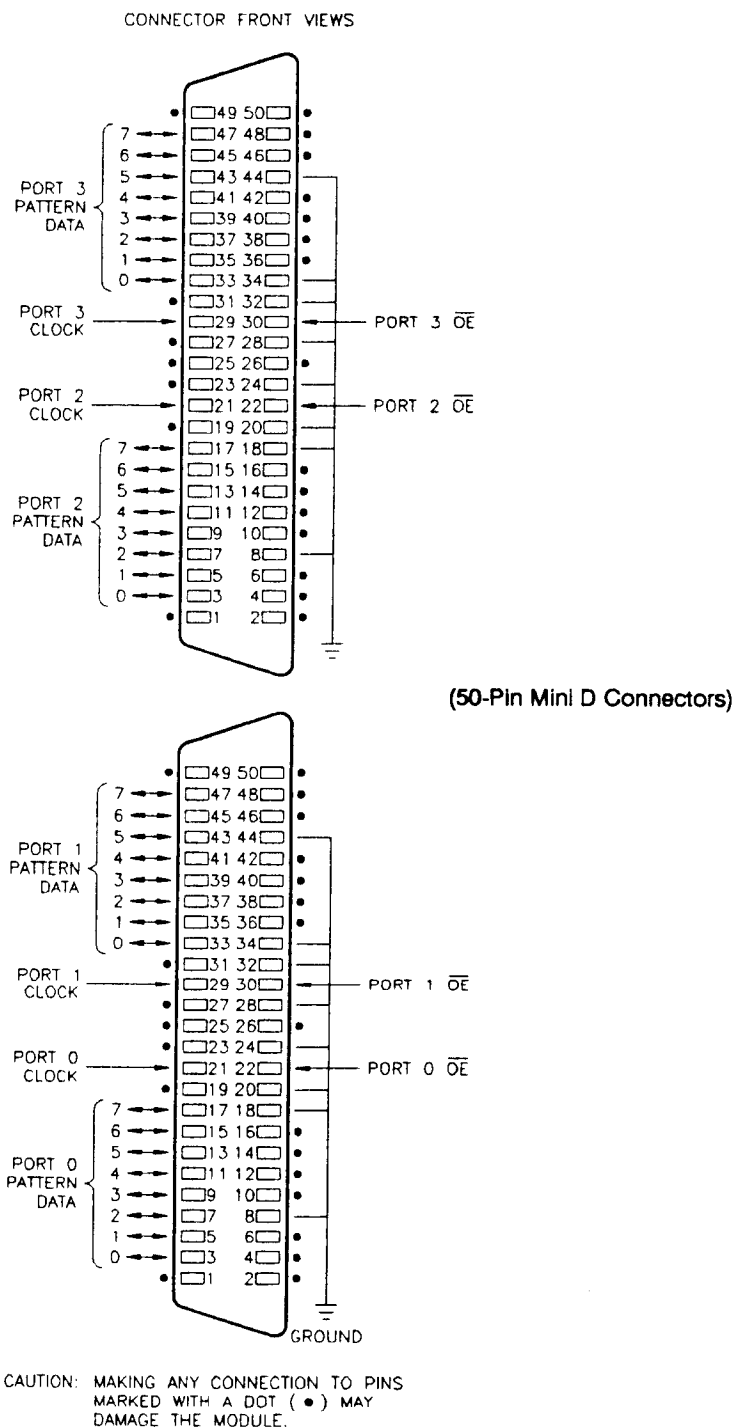
**Figure 2-2. Setting a Logical Address Switch**

## NOTE

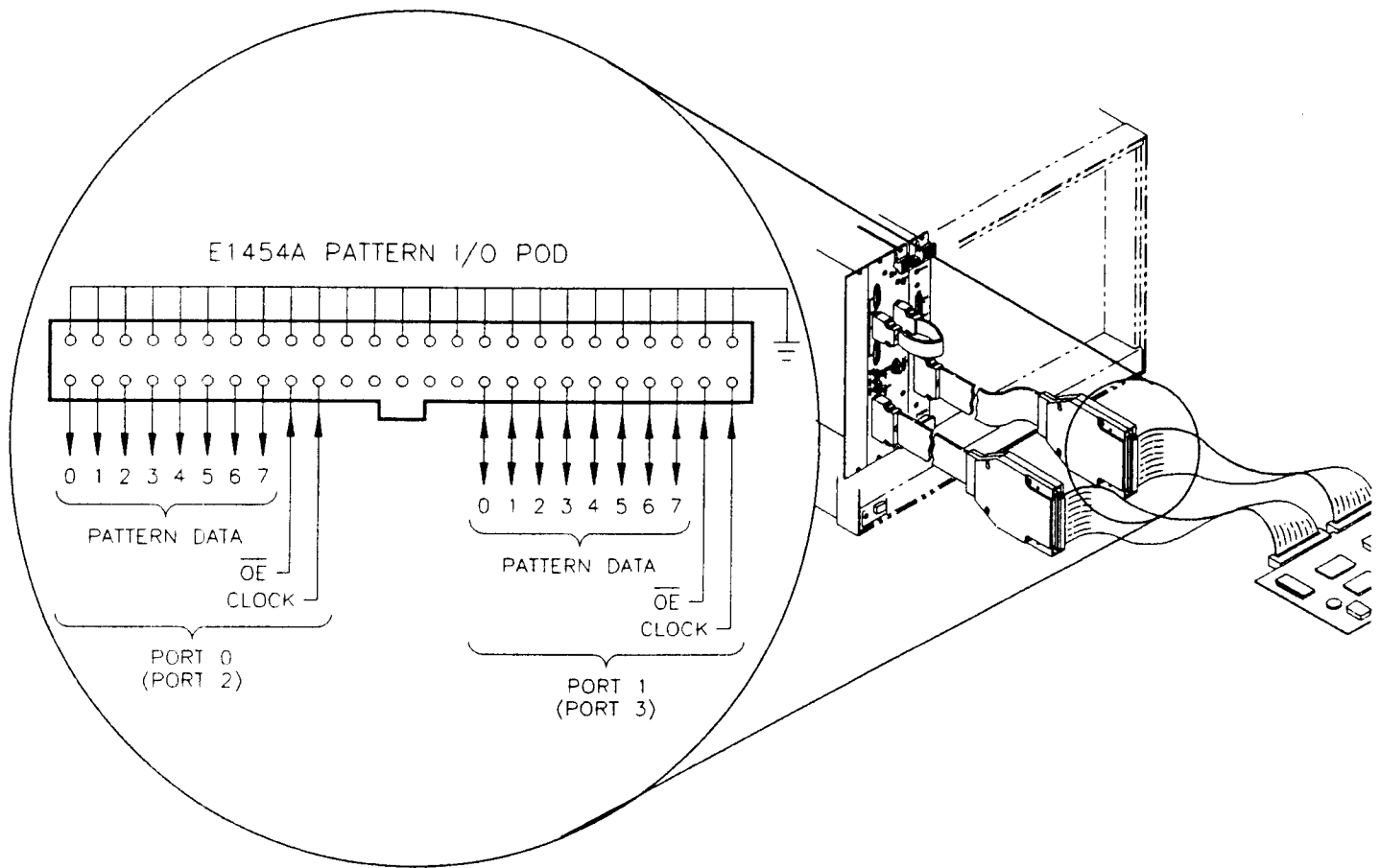
*Plug-in modules also contain Interrupt Switches. We recommend that you leave these switches set to 1 (factory setting). This causes the modules to use interrupt line 1 which is the default line for most interrupt handlers (command module, embedded controller, etc.). Refer to the "C-Size VXibus Systems Installation and Getting Started Guide" if you need more information on Interrupt Switches.*

# Wiring Information

This section shows the module's front panel connector pin-out, the optional HP E1454 Pattern I/O Pod connector pin-out (DUT side), and the optional DUT interface cable wiring.



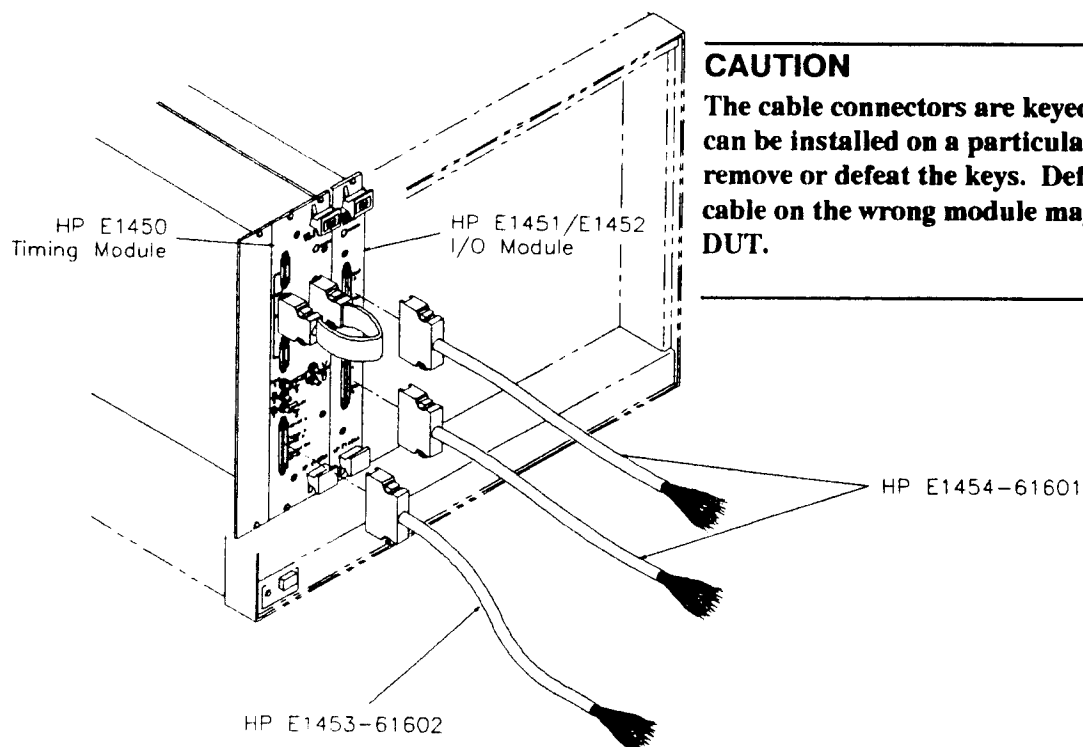
**Figure 2-3. Pattern I/O Front Panel Connectors**



**Figure 2-4. Pattern I/O Pod Connector**

### CAUTION

The pod connectors are keyed so that only the correct pod can be installed on a particular plug-in module. Do not remove or defeat the keys. Defeating a key and installing a pod on the wrong module will damage the module and the pod.



## CAUTION

The cable connectors are keyed so that only the correct cable can be installed on a particular plug-in module. Do not remove or defeat the keys. Defeating a key and installing a cable on the wrong module may damage the module and the DUT.

Figure 2-5. Module to DUT Interface Cables

Table 2-1. Pattern I/O (HP E1454-61601) Wiring

| Pin | Color         | Signal             | Pin | Color         | Signal           |
|-----|---------------|--------------------|-----|---------------|------------------|
| 1   | NC            |                    | 2   | NC            |                  |
| 3   | RED/BLUE      | D0 (Port 0 or 2)   | 4   | NC            |                  |
| 5   | WHITE/BROWN   | D1 (Port 0 or 2)   | 6   | NC            |                  |
| 7   | RED/ORANGE    | D2 (Port 0 or 2)   | 8   | VIOLET/BLUE   | GROUND           |
| 9   | WHITE/ORANGE  | D3 (Port 0 or 2)   | 10  | NC            |                  |
| 11  | RED/GREEN     | D4 (Port 0 or 2)   | 12  | NC            |                  |
| 13  | WHITE/GREEN   | D5 (Port 0 or 2)   | 14  | NC            |                  |
| 15  | WHITE/BLUE    | D6 (Port 0 or 2)   | 16  | NC            |                  |
| 17  | RED/BROWN     | D7 (Port 0 or 2)   | 18  | BLUE/VIOLET   | GROUND           |
| 19  | NC            |                    | 20  | VIOLET/ORANGE | GROUND           |
| 21  | WHITE/GRAY    | EXT CLK2[Port 0 or | 22  | YELLOW/BROWN  | OE (Port 0 or 2) |
| 23  | NC            |                    | 24  | ORANGE/VIOLET | GROUND           |
| 25  | NC            |                    | 26  | NC            |                  |
| 27  | NC            |                    | 28  | VIOLET/GREEN  | GROUND           |
| 29  | RED/GRAY      | EXT CLK3[Port 1 or | 30  | YELLOW/GRAY   | OE (Port 1 or 3) |
| 31  | NC            |                    | 32  | GREEN/VIOLET  | GROUND           |
| 33  | BLACK/ORANGE  | D0 (Port 1 or 3)   | 34  | VIOLET/BROWN  | GROUND           |
| 35  | BLACK/BROWN   | D1 (Port 1 or 3)   | 36  | NC            |                  |
| 37  | YELLOW/BLUE   | D2 (Port 1 or 3)   | 38  | NC            |                  |
| 39  | BLACK/GREEN   | D3 (Port 1 or 3)   | 40  | NC            |                  |
| 41  | BLACK/BLUE    | D4 (Port 1 or 3)   | 42  | NC            |                  |
| 43  | YELLOW/ORANGE | D5 (Port 1 or 3)   | 44  | BROWN/VIOLET  | GROUND           |
| 45  | BLACK/GRAY    | D6 (Port 1 or 3)   | 46  | NC            |                  |
| 47  | YELLOW/GREEN  | D7 (Port 1 or 3)   | 48  | NC            |                  |
| 49  | NC            |                    | 50  | NC            |                  |

Notes: NC = No Connection. Colors listed as main body color/stripe color. For example, WHITE/BROWN is a white wire with a brown stripe.

## Recommended Fixturing Techniques

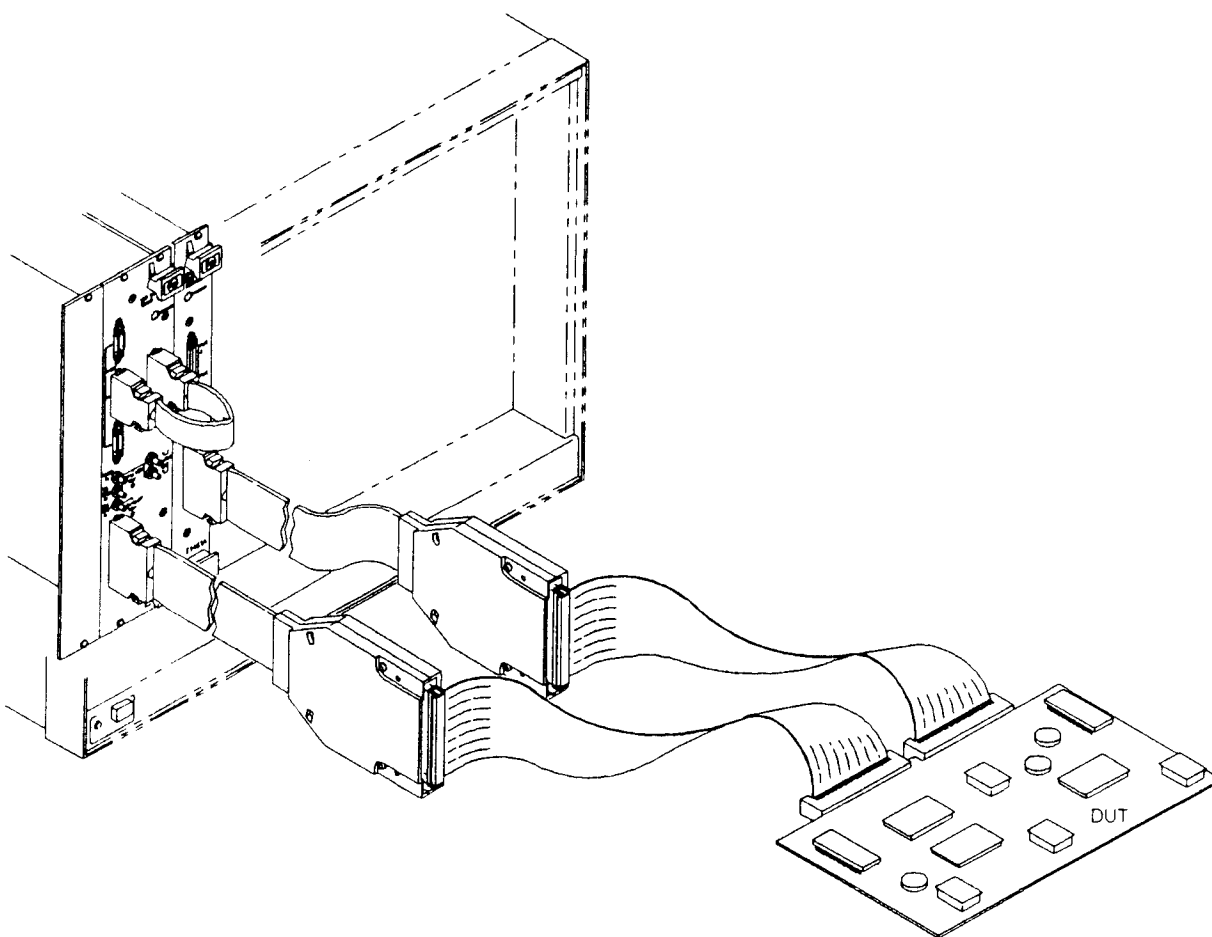
- The pod mating connector (Dut side) is a 50-pin (2 x 25) male dual in-line connector with 0.025-inch (0.64mm) round or square pins on 0.100-inch (2.54mm) centers. This connector is not supplied with the product and is available from electronic supply houses.
- Do not connect the device under test (DUT) directly to the pod connector. Whenever possible, use intermediate wiring between the pod mating connector and the test fixture connector (such as the PC Board Edge Connector shown below). This minimizes the number of insertions/removals made to the pod connector which extends its lifetime.
- Keep all wiring to the DUT as short as possible.

---

### CAUTION

Clearly label the wiring and connectors to identify timing connections and I/O connections. Equipment or DUT damage can occur if these connections are accidentally reversed.

---



E1493\_PODS\_1

**Figure 2-6. Recommended Fixturing Techniques**



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## Chapter 3

# Register Maps

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### Using This Chapter

The HP E1451/E1452 modules are a register-based devices. This chapter contains the register information for these modules.

---

#### CAUTION

The register maps in this chapter are included for reference information only. WE DO NOT RECOMMEND THAT YOU ATTEMPT TO PROGRAM THE MODEL D20 AT THE REGISTER LEVEL. Register-based programming of this product is difficult; requires in-depth knowledge of the internal workings of the product; can result in the erasure of calibration constants requiring the product to be serviced at an HP Service Center. REPAIRS MADE TO THE PRODUCT TO REPLACE CALIBRATION CONSTANTS ERASED BY REGISTER-BASED PROGRAMMING ARE NOT COVERED BY THE PRODUCT WARRANTY.

---

### Register Addresses

The following table shows the HP E1451/E1452 register offset values within the A16 address space (note that a base address must be added to the register offset value to produce the register address).

**Table 2-1. HP E1451/E1452 Registers within A16 Address Space.**

| Address (Hex) | Register Description           |
|---------------|--------------------------------|
| 3E            | Port 3 Mask/Calibration Value  |
| 3C            | Port 3 Status/Clock Source     |
| 3A            | Port 3 I/O Control             |
| 38            | Port 3 Configuration           |
| 36            | Port 3 Data Bus                |
| 34            | Port 3 Branch Destination      |
| 32            | Port 3 Sequence Memory Address |
| 30            | Port 2 Mask/Calibration Value  |
| 2E            | Port 2 Status/Clock Source     |
| 2C            | Port 2 I/O Control             |
| 2A            | Port 2 Configuration           |
| 28            | Port 2 Data Bus                |
| 26            | Port 2 Branch Destination      |
| 24            | Port 2 Sequence Memory Address |
| 22            | Port 1 Mask/Calibration Value  |
| 20            | Port 1 Status/Clock Source     |
| 1E            | Port 1 I/O Control             |
| 1C            | Port 1 Configuration           |
| 1A            | Port 1 Data Bus                |
| 18            | Port 1 Branch Destination      |
| 16            | Port 1 Sequence Memory Address |
| 14            | Port 0 Mask/Calibration Value  |
| 12            | Port 0 Status/Clock Source     |
| 10            | Port 0 I/O Control             |
| 0E            | Port 0 Configuration           |
| 0C            | Port 0 Data Bus                |
| 0A            | Port 0 Branch Destination      |
| 08            | Port 0 Sequence Memory Address |
| 06            | Calibration ROMs               |
| 04            | Status/Control                 |
| 02            | Device Type                    |
| 00            | ID                             |

## The Base Address

To access a register, you must specify the register address in either hexadecimal or decimal. The register address consists of a base address plus a register offset. The base address depends on whether the A16 address space is accessed via the Series C HP E1405 Command Module or via some other controller.

### A16 Address Space when not using the HP E1405 Command Module

When the Command Module or Mainframe is not part of your VXIbus system, the module's base address is computed by taking the controller specific offset and adding the following:

| hexadecimal             | decimal                 |
|-------------------------|-------------------------|
| $C000h + (LADDR * 64)h$ | $49,152 + (LADDR * 64)$ |

where C000h (49,152) is the starting location of the register addresses, LADDR is the module's logical address, and 64 is the number of address bytes per register-based module. For example, the module's factory set logical address is 136. If this address is not changed, the module will have a base address consisting of the controller specific offset with the following added to it:

| hexadecimal                                     | decimal                                           |
|-------------------------------------------------|---------------------------------------------------|
| $C000h + (136 * 64)h$<br>$C000h + 2200 = E200h$ | $49,152 + (136 * 64)$<br>$49,152 + 8704 = 57,856$ |

### A16 Address Space Using the Command Module

When the A16 address space is accessed via the Command Module, the module's base address is computed as:

| hexadecimal               | decimal                    |
|---------------------------|----------------------------|
| $1FC000h + (LADDR * 64)h$ | $2,080,768 + (LADDR * 64)$ |

where 1FC000h (2,080,768) is the starting location of the register addresses, LADDR is the module's logical address, and 64 is the number of address bytes per register-based module. For example, the module's factory set logical address is 136. If this address is not changed, the module will have a base address of:

| hexadecimal                                            | decimal                                                    |
|--------------------------------------------------------|------------------------------------------------------------|
| $1FC000h + (136 * 64)h$<br>$1FC000h + 2200h = 1FE200h$ | $2,080,768 + (136 * 64)$<br>$2,080,768 + 8704 = 2,089,472$ |

## Register Offset

The register offset is the register's location in the block of 64 address bytes (see Table 2-1). For example, the module's Port 1 Mask/Calibration register has an offset of 22h. When writing a value to this register, this offset is added to the base address to form the register address:

| Address Space              | Hexadecimal Register Address                                                    | Decimal Register Address                                                  |
|----------------------------|---------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| Outside the command module | $\text{OFFSET} + \text{E200h} + 22\text{h} =$<br>$\text{OFFSET} + \text{E222h}$ | $\text{OFFSET} + 57,856 + 34 =$<br>$\text{OFFSET} + 57,890 + 34 = 52,258$ |
| Inside the command module  | $1\text{FE200h} + 22\text{h} = 1\text{FE222h}$                                  | $2,089,472 + 34 = 2,089,506$                                              |

---

### Important

*These modules are D16-only devices. That is, they may only be accessed via 16-bit words on even addresses. Attempts to access these modules via 8-bit bytes (D8) or 32-bit words (D32) will result in a bus error.*

---

## Register Definitions

All addresses are given in hexadecimal. Unless otherwise noted, register contents are unaffected by hard or soft resets. "X" or "x" denote bits which are "don't-care". All registers reside at even addresses and are WORD wide.

### ID Register (Read)

Address = Base + 00H. This address returns the Hewlett-Packard VXI manufacturer ID of FFFFH

### Device Type (Read)

Address = Base + 02H. This register defines the module's device class, addressing mode and manufacturer's ID according to the VXIbus specification. A read of this address returns 0151H (337<sub>10</sub>) for an HP E1451 or a 0153H (339<sub>10</sub>) for an HP E1452 (corresponding to a register-based device using the A16 address space only and manufactured by Hewlett-Packard)..

### Status/Control Register (Read)

This register returns the I/O Module Status.

| Address: B<br>+ 04 <sub>H</sub> |     |        |      |      |        |        |     |
|---------------------------------|-----|--------|------|------|--------|--------|-----|
| Bit #                           | 15  | 14     | 13-9 | 8    | 7      | 6-4    | 3-0 |
| Value                           | A24 | MODID* | 1    | TERM | INTEN* | ILS2-0 | 1   |

#### Bit Definitions

- A24: Informs VXI controllers that the I/O module is not A24/A32 compatible. This bit is always clear.
- MODID\*: A 1 in this field indicates the device is not selected via the P2 MODID line. A 0 indicates that the device is selected by a high state on the P2 MODID line. Reset value is 1.
- INTEN\*: Interrupt Enabled. This field indicates the I/O Module may interrupt on the VXI backplane. Reset value is 0 (disabled), value of 1 enables.
- ILS2-0: The octal value read from this field indicates the interrupt level currently selected by the interrupt switch.
- TERM: Terminated. If this field is clear, the I/O module is an E1451 Unterminated Module. If set, the I/O module is an E1452 terminated module (50 ohm terminations on the local bus).

## Status/Control Register (Write)

This register sets Control Bits.

|                              |      |        |        |     |        |
|------------------------------|------|--------|--------|-----|--------|
| Address: B + 04 <sub>H</sub> |      |        |        |     |        |
| Bit #                        | 15-8 | 7      | 6-4    | 3-1 | 0      |
| Value                        | X    | INTEN* | ILS2-0 | X   | SRESET |

### Bit Definitions

- **INTEN\***: Interrupt Enabled. A write to this field enables the I/O Module to interrupt on the VXI backplane. Reset value is 1 (disabled), value of 0 enables.
- **ILS2-0**: The octal value written to this field sets the interrupt level which will be set when the I/O Module Interrupts the VXI backplane. Reset value is 0 (interrupts not enabled).
- **SRESET**: A write of 1 in this field Soft Resets the I/O Module. Bit 7 is set to 1 by Hard Reset (SYSRESET\*) but not by SRESET.

## Calibration ROM Register (Read/Write)

This address accesses the Calibration ROMs of the I/O Module.

---

### CAUTION

**DO NOT WRITE TO THIS REGISTER. DOING SO MAY ALTER THE CALIBRATION ROM'S CONTENTS, CAUSING THE MODULE TO FAIL AND REQUIRE FACTORY REPAIR.**

---

|                              |      |           |           |              |          |          |         |         |             |
|------------------------------|------|-----------|-----------|--------------|----------|----------|---------|---------|-------------|
| Address: B + 06 <sub>H</sub> |      |           |           |              |          |          |         |         |             |
| Bit #                        | 15-8 | 7         | 6         | 5            | 4        | 3        | 2       | 1       | 0           |
| Value                        | X    | POD_1_OUT | POD_0_OUT | ROM_DATA_OUT | POD1_SEL | POD0_SEL | ROM_SEL | DATA_IN | CAL_ROM_CLK |

## I/O Port Registers

The following registers are common for each of the four I/O ports of the I/O Module (Port 0 through Port 3).

## Sequence Memory (Read/Write)

This register contains the current address into sequence memory. It is used when reading or writing to that memory and it should be set to the first location of a sequence prior to starting that sequence. If bit 6 of the Configuration Register is set, the sequence memory address will increment by 1 whenever the Port Data Bus Register is accessed. Address: Port 0 = Base + 08<sub>H</sub>, Port 1 = Base + 16<sub>H</sub>, Port 2 = Base + 24<sub>H</sub>, Port 3 = Base + 32<sub>H</sub>

|              |          |
|--------------|----------|
| <b>Bit #</b> | 15-0     |
| <b>Value</b> | AC15-AC0 |

### Branch Destination (Read/Write)

Address: Port 0 = Base + 0AH, Port 1 = Base + 18H, Port 2 = Base + 26H, Port 3 = Base + 34H

This register supplies the sequence memory address to which a jump is made when the sequencer encounters a set branch bit. All 16 bits are significant, and reading this location gives the last value written.

|              |          |
|--------------|----------|
| <b>Bit #</b> | 15-0     |
| <b>Value</b> | BA15-BA0 |



## Port Data Bus (Read/Write)

Address: Port 0 = Base + 0CH, Port 1 = Base + 1AH, Port 2 = Base + 28H, Port 3 = Base + 36H

This register allows access to the internal pattern and control buses of the port.

| Bit # | 15-14 | 13   | 12   | 11  | 10  | 9-8 | 7-0   |
|-------|-------|------|------|-----|-----|-----|-------|
| Value | X     | COMP | TRIS | BRA | EOS | X   | PD7-0 |

### Bit Definitions

- Control Bus:
  - COMP: Enables (1) or disables (0) the compare test.
  - TRIS: Drives (0) or tri-states (1) the stimulus stage.
  - BRA: Branch. If set, causes jump to branch destination.
  - EOS: End of Sequence. If set, causes sequencer to stop.
- Pattern Bus PD7-0: Pattern Data.

## Configuration Register (Read/Write)

Address: Port 0 = Base + 0EH, Port 1 = Base + 1CH, Port 2 = Base + 2AH, Port 3 = Base + 38H

This register controls what happens on the port's internal control and pattern buses. It also control the operation of the sequence memory. It can be read at any time and can be written when the port is stopped or paused (not receiving clocks).

| Bit # | 15-8 | 7     | 6     | 5       | 4-2      | 1-0      |
|-------|------|-------|-------|---------|----------|----------|
| Value | X    | COMEN | ENISC | ENIIOC* | PBRAM2-0 | CBRAM1-0 |

### Bit Definitions

- COMEN Compare Enable. When set (1), Compare is Enabled. When clear (0), compare function is disabled and any compare errors generated are cleared (see Status/Clock Source Register). Be sure that errors have been serviced before disabling compare mode.
- ENISC: Enable Injected Sequencer Clock. When set, the Address Counter will be incremented after each read or write to the Port Data Bus Register. This feature is used to load or dump sequence memory. Advancing the sequencer address in this way ignores the stop and branch bits.
- ENIIOC\*: Enable Injected I/O Clock. When set (0, notice inverse logic sense), enables an I/O clock to be generated as part of a Read or Write to the Port Data Bus Register. This feature is used to directly control the input or output stages. The I/O clock will clock the input register, output register, tristate register (a group of tristate control flip flops), expected response register, compare flip flop, stop flip flop, and branch flip flop. If compare is enabled, an injected I/O clock operation could cause a compare error. If the branch or stop bits are true, an injected I/O operation could cause a stop or branch.
- PBRAM2-0: Pattern Bus/RAM. These bits control action on the pattern bus and operation of the pattern sequence memory.

---

**Note**

*In end of record mode, the ram continues to write the contents of the input register into the last ram location even after the port has stopped. It is important to take the port out of record mode before the contents of the input register or the data on the port data bus is allowed to change.*

---

| PBRAM2-0 | Function                      |
|----------|-------------------------------|
| 000      | Read (RAM drives bus)         |
| 001      | Record Mode (see note above)  |
| 010      | Safe (pattern bus tri-stated) |
| 011      | Access Input Stage            |
| 100      | unused                        |
| 101      | Load RAM from VXI             |
| 110      | Safe (pattern bus tri-stated) |
| 111      | Access Output Stage           |

**Bit Definitions (continued)**

- CBRAM2-0: Control Bus/RAM.

| CBRAM1-0 | Function                  |
|----------|---------------------------|
| 00       | Safe (Bus tri-stated)     |
| 01       | Read (RAM drives bus)     |
| 10       | Load RAM from VXI         |
| 11       | Access control flip-flops |

## I/O Control (Read/Write)

Address: Port 0 = Base + 10H, Port 1 = Base + 1EH, Port 2 = Base + 2CH, Port 3 = Base + 3AH

This register controls the external, i.e., the user accessible, buses of the port. A hard or soft reset will set bits 0 - 7 to 0. The port should be stopped or paused (not receiving clocks) before writing to the output control register.

| Bit # | 15-8 | 7        | 6-4    | 3-2      | 1-0       |
|-------|------|----------|--------|----------|-----------|
| Value | X    | LIVE_I/O | unused | PDBUS1-0 | CSTBUS1-0 |

### Bit Definitions

- **LIVE\_I/O**: When set, live I/O flip-flop will reflect live access.
- **PDBUS1-0**: Pod Bus Control. The Pod Bus connects the Module to the Pod. When the pod is not being used, this is the bus connected to the device under test. Reset causes the pod bus to go to the safe mode.

| PDBUS1-0 | Function                                                                      |
|----------|-------------------------------------------------------------------------------|
| 00       | Safe (Pod Bus is Tristate)                                                    |
| 01       | Pod Input Buffer is Driver (used for all input modes)                         |
| 10       | Module Output Register can operate (used for output modes with pod absent)    |
| 11       | Module Output Register Always Drives (used for output modes with pod present) |

The following table shows the effects on the outputs by switching from one mode to another. This table is complete and does not assume that power is cycled between cases of pod being present and cases of pod being absent.

| FROM                               | TO      | OUTPUTS   |
|------------------------------------|---------|-----------|
| reset, input, drive, operate, safe | safe    | tristate  |
| safe, drive, operate, input        | input   | tristate  |
| safe, input, operate, drive        | drive   | drive     |
| safe, input                        | operate | tristate  |
| drive                              | operate | drive     |
| operate                            | operate | unchanged |

## Bit Definitions

- **CSTBUS1-0: User Bus Control.** The user bus is what the user sees at the end of the pod. Reset causes the user bus to go to the input mode.

| CSTBUS1-0 | Function                                                                                                                              |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------|
| 00        | User drives the Bus (used for all Pod input modes)                                                                                    |
| 01        | Pod Output Register can operate (used for Pod output modes using external clock)                                                      |
| 10        | Pod Output Buffer drives the Bus (not normally used but could be used for Live Output if you want to ignore the tristate control bit) |
| 11        | Pod Output Buffer can operate (used for Pod Output modes using internal clocks)                                                       |

The following table shows the effects on the outputs by switching from one mode to another.

| FROM                                  | TO       | OUTPUTS   |
|---------------------------------------|----------|-----------|
| reset, input, drive, register, buffer | input    | tristate  |
| input, drive, register, buffer        | register | tristate  |
| input, drive, register, buffer        | drive    | drive     |
| input, register                       | buffer   | tristate  |
| drive                                 | buffer   | drive     |
| buffer                                | buffer   | unchanged |

The drive mode may never be used. The following table assumes this case. It further ignores the input case.

| FROM                    | TO       | OUTPUTS   |
|-------------------------|----------|-----------|
| input, register, buffer | register | tristate  |
| input, register         | buffer   | tristate  |
| buffer                  | buffer   | unchanged |

## Status/Clock Source Register (Write)

Address: Port 0 = Base + 12H, Port 1 = Base + 20H, Port 2 = Base + 2EH, Port 3 = Base + 3CH

This register performs two different control tasks. Bits 0-6 select the clock source for the sequencer. Bits 15, 14, and 9 control the starting and stopping of the sequencer. This is the Status/Clock Source Register for each I/O Port. If changing the internal clock source, the port should be stopped, not just paused. For other fields in the status/clock register, the port can be either stopped or paused (not receiving clocks) before writing.

| Bit # | 15  | 14    | 13-10 | 9     | 8      | 7 | 6-5      | 4      | 3-0      |
|-------|-----|-------|-------|-------|--------|---|----------|--------|----------|
| Value | RUN | CLSE* | X     | STOP* | Unused | X | EXTCS1-0 | PODECP | INTCS3-0 |

### Bit Definitions

- Bits 15, 14, and 9: These three bits are ephemeral. Their states are not latched. It is the action of writing the specified value into them that produces their effect.

**RUN:** Setting this bit (1) causes the sequencer, if currently stopped, to enter its running state. If the sequencer is already running, setting this bit has no effect. Writing "0" into this bit has no effect.

**CLSE\*:** Clear Stop Event. Setting this bit to "0" clears the event caused by a sequencer "RUN" to "STOP" transition. Setting this bit to "1" has no effect. The stop events of all four ports are OR'ed together to produce an interrupt request event for the module.

**STOP\*:** If clear, stop. No action if set. Sending a stop command (write 0 to stop bit) to a running port will stop the port and cause a stop event interrupt. Sending a stop command to a stopped port does not cause a stop event interrupt. Sending a stop command to a port that is receiving clocks will cause it to stop. However, it may stop in an uncoordinated fashion. That is, the contents of the address counter may not match the behavior of the I/O stage. This warning should apply only to external clocks, since it is assumed that clocks from the Timing Module would be turned off before a stop command would be sent to a port.

- **PODECP:** Pod external Clock Polarity. If set, the pod's external clock is inverted (high-to-low edge clocks). If clear, the pod's external clock has normal polarity, i.e., the low-to-high clocks. This bit is used only if a pod is present. Toggling the pod external clock polarity bit will inject an external clock. This can be used to prime the pipe stage (pod output register) in the pod in the case of output - pod present - external clock. It can also be used to single step the port. In both of these cases, the external clock must be static.
- **EXTCS1-0:** External Clock Select. If external clock is selected, the internal clock select should be off. Inverted external clock select is normally used only when the pod is absent. If the pod is absent, the polarity of the external clock can be toggled to inject an external clock for the purposes of single step. The external clock must be static high or low in this instance.

| EXTCS1-0 | Function                                                                                         |
|----------|--------------------------------------------------------------------------------------------------|
| 00       | External Clock Off                                                                               |
| 01       | Non-inverted External Clock (used if Pod is present or not, internal clock select should be OFF) |
| 10       | Select Inverted External Clock (used if Pod is not present, internal clock select should be OFF) |
| 11       | unused                                                                                           |

- **INTCS3-0: Internal Clock Select.** When using internal clocks, the external clock select is set OFF. Changing the clock source on a port that is running or PAUSED (not receiving clocks) may cause spurious clocks and uncoordinated operation. The port should be stopped before changing the clock source. Changing the internal clock source will require that a new calibration value be loaded into the mask/cal register.

| INTCS3-0 | Function       |
|----------|----------------|
| 0000     | Stimulus CLK 0 |
| 0001     | Stimulus CLK 1 |
| 0010     | Stimulus CLK 2 |
| 0011     | Stimulus CLK 3 |
| 0100     | Stimulus CLK 4 |
| 0101     | Stimulus CLK 5 |
| 0110     | OFF            |
| 0111     | OFF            |
| 1000     | Response CLK 0 |
| 1001     | Response CLK 1 |
| 1010     | Response CLK 2 |
| 1011     | Response CLK 3 |
| 1100     | Response CLK 4 |
| 1101     | Response CLK 5 |
| 1110     | OFF            |
| 1111     | OFF            |

## Status/Clock Source Register (Read)

Address: Port 0 = Base + 12H, Port 1 = Base + 20H, Port 2 = Base + 2EH, Port 3 = Base + 3CH

| Bit # | 15  | 14     | 13     | 12        | 11 | 10       | 9         | 8         | 7 | 6-5      | 4      | 3-0      |
|-------|-----|--------|--------|-----------|----|----------|-----------|-----------|---|----------|--------|----------|
| Value | RUN | STOPEV | CMPSEI | DA_STATUS | X  | CARD_OE* | QPIPE_OE* | QOBUF_OE* | X | EXTCS1-0 | PODECP | INTCS3-0 |

### Bit Definitions

- RUN: Run. If set, Port is presently Running, if clear the Port is presently stopped.
- STOPEV: Stop Event Interrupt. If set, the port had a RUN to STOP transition
- CMPSEI: Compare Error Interrupt. If set, a compare error occurred.
- DA\_STATUS: Can be used to indicate whether the current output is due to direct access or due to sequencer.
- CARD\_OE\*: Card Output Enable. If set,
- QPIPE\_OE\*: Pipe Register Output Enable. If set.
- QOBUF\_OE\*: Output Register Output Enable. If set.
- PODECP: Pod external Clock Polarity. Readable status of this field.
- EXTCS1-0: External Clock Select. Readable status of this field.
- INTCS1-0: Internal Clock Select. Readable status of this field.

## Mask/Calibration Value Register (Read/Write)

Address: Port 0 = Base + 14H, Port 1 = Base + 22H, Port 2 = Base + 30H, Port 3 = Base + 3EH

This is the Status/Clock Source Register for each I/O Port

| Bit # | 15-8      | 7-0        |
|-------|-----------|------------|
| Value | CMPMK15-8 | CALVAL 7-0 |

### Bit Definitions

- CMPMK15-8: Compare Mask field. If a bit is set in this field, compare in this bit position, otherwise ignore.
- CALVAL7-0: Calibration Value field. Resolution is 100ps. There are minimum and maximum legal values.

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# Appendix A

## Specifications

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### Sequencer Specifications

**Memory Depth:** 65,536 (64k) vectors. Multiple test sequences may co-reside in memory.

**Memory Functions:** Stimulus Pattern or Response Pattern (expected or recorded) as well as control of Tri-state, Compare, and End-of-Sequence functions.

### Specifications For Ports Configured As Outputs

**Clock Source :** External Clock, HP E1450 Timing Module (one of six Stimulus Pattern Clocks)

#### Output Levels:

##### HP E1451/E1452 Module Outputs

Maximum Continuous Output Current:  $\pm 24\text{mA}$  per line

High, Open-Circuit: 4.4V, min.

Low, Open-Circuit: 0.1V, max.

Output Impedance:  $50\Omega$ , typical

Capacitance (outputs disabled): 30pf, max.

Leakage Current (outputs disabled):  $120\mu\text{A}$ , max.

##### HP E1454 Pod Outputs

Maximum Continuous Output Current:  $\pm 24\text{mA}$  per line

High, Open-Circuit: 4.3V, min.

High, Sourcing 24mA: 3.7V, min.

Low, Open-Circuit: 0.1V, max.

Low, Sinking 24mA: 0.44V, max

Capacitance (outputs disabled): 30pf, max.

Leakage Current (outputs disabled):  $120\mu\text{A}$ , max.

**Tri-state:**

Outputs can be disabled on a cycle-by-cycle basis by a control bit in the Sequencer memory, or by driving the Output Enable high. All eight pins of the port are controlled simultaneously.

**Tri-State Control Input Levels and Loading (for HP E1451/E1452 and HP E1454):**

High: >2.0V at <150 $\mu$ A

Low: <0.8V (internal pull-down)

**Tri-state Control Input Delay:**

HP E1451/E1452 without pod: 9ns typical, 14ns max

HP E1454 with pod: 8ns typical, 11ns max

**Timing:**

Pattern Rate: 0 to 20MHz

**Skew:**

Between output pins in the same port: 3ns, typical

Risetime: 6.5ns typical

Falltime: 7.0ns typical

**Data Delay From External Clock:**

HP E1451/E1452 without pod: 20ns typical, 27ns max

HP E1454 with pod: 14ns typical, 20ns max

## **Specifications For Ports Configured As Inputs**

**Clock Source:** External Clock, HP E1450 Timing Module (1 of 6 Response Pattern Clocks)

**Input Levels And Loading (for HP E1451/E1452 and HP E1454):**

Low: <0.8V at <150 $\mu$ A

High: >2.0V (internal pull-up)

Capacitance: 30pf max.

**Real-time Compare:**

A programmable static mask can identify any pin of the port to be 'don't-care' for the duration of the test sequence. For those pins which are not masked, a Sequencer Control bit can enable the comparison of input patterns with expected response data on a cycle-by-cycle basis.

**Input Timing:****Setup Time to External Clock**

HP E1451/E1452 without Pod: -1.6ns

HP E1454 with Pod: 5ns

**Hold Time from External Clock**

HP E1451/E1452 without Pod: 11.5ns

HP E1454 with Pod: 14ns

## **External Clock Input Specifications (for HP E1451/E1452 And HP E1454):**

Minimum Period: 50ns

Minimum Pulse Width: 6ns

Polarity: Selectable

Input Levels (for HP E1451/E1452 or HP E1454):

Low: <0.8V at <150 $\mu$ A

High: >2.0V (internal pull-up)

Capacitance: 30pf max.

## **Miscellaneous Specifications**

### **Power Requirements:**

+5.0V (excluding load currents): 1.5A peak, 40ma dynamic

-5.2V: 2.2A peak, 200mA dynamic

-2.0V: 0.6A peak, 80mA dynamic

+12.0V: 0.1A peak, 10mA dynamic

### **Cooling Requirements:**

Average Power/slot: 22w

Ambient Temperature:

Operating: 0 to 55°C

Storage: -40 to 75°C

Humidity: 65 % relative from 0 to 40°C

Operating temp: 0 to 55°C

Storage temp: -40 to 75°C

Airflow Requirements (for 10°C rise): 2.0 liter/sec at 1.2 mm water

**Weight:** 1.1kg



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