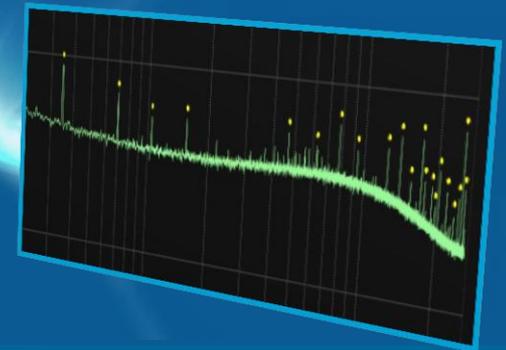


DCA Family

What's New?

Oscilloscope Products Division
Sampling Scopes Marketing
Santa Rosa, CA

Joachim Vobis, Sales Development
joachim_vobis@agilent.com



Anticipate — Accelerate — Achieve

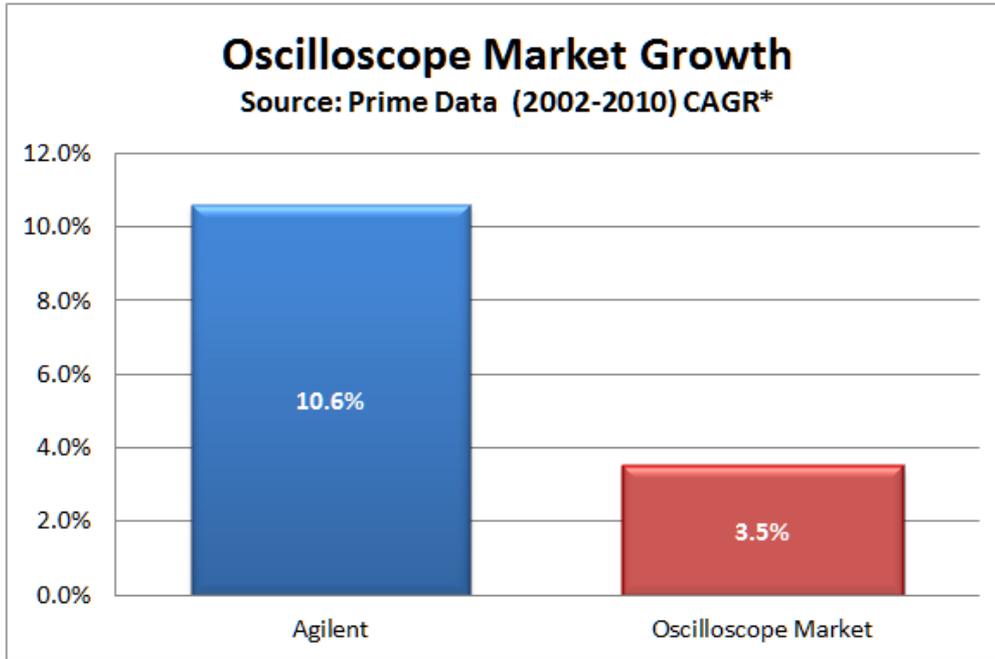


Agilent Technologies

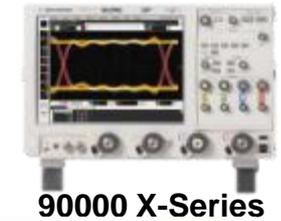


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October 14, 2013

Agilent Oscilloscopes – Portfolio Overview



* CAGR = Compound Annual Growth Rate



U1600 Series
U2700 Series



1000B Series
2000 X-Series



3000 X-Series to 1GHz



6000 Series



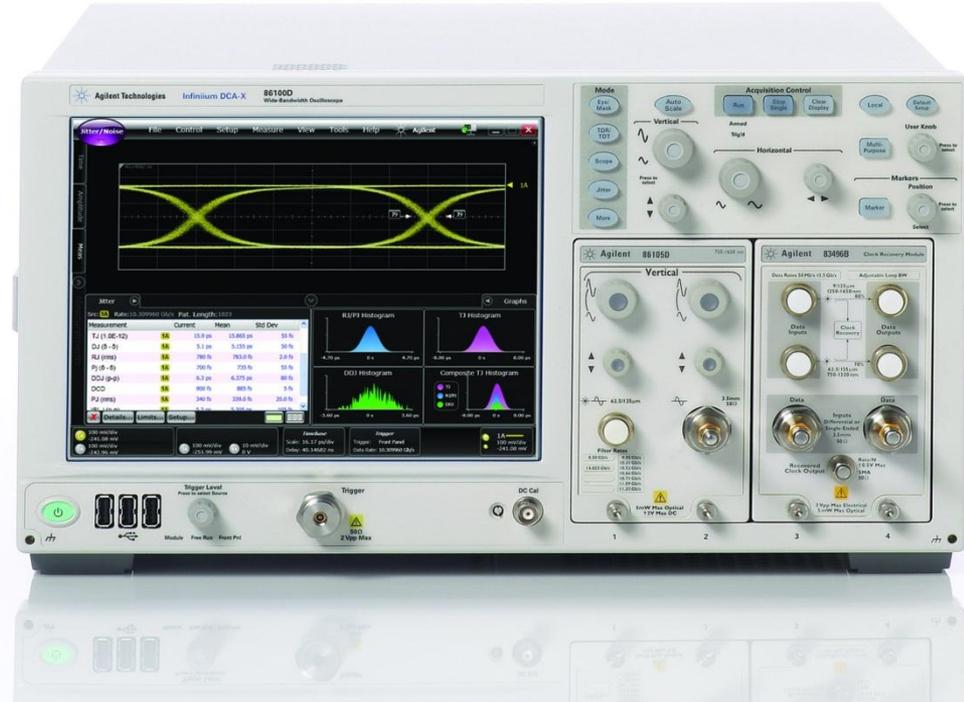
7000B Series



9000 Series

Table Of Content

- ❑ [DCA Family Overview](#)
- ❑ [FlexDCA Software \(New DCA User Interface\)](#)
- ❑ [28G 850 nm Multimode Receivers](#)
- ❑ [Electrical Mini-Modules](#)
- ❑ [Precision Waveform Analyzer](#)
- ❑ [Jitter Spectrum Analysis](#)
- ❑ [External Clock Recovery](#)
- ❑ [Standard Compliance Applications](#)
- ❑ [UDA & SCPI Tools](#)
- ❑ [Productivity Package](#)
- ❑ [System Impulse Response Correction \(SIRC\)](#)
- ❑ [Signal Processing & De-Embedding](#)



DCA Family Overview

Mainframe

- DCA-X, FlexDCA

Optical Modules

- Best Accuracy vs. highest flexibility
- Single vs. multi-channel

Electrical Modules

- 2-Channel Modules
- TDR

Specialty Modules

- Clock Recovery
- Precision Timebase

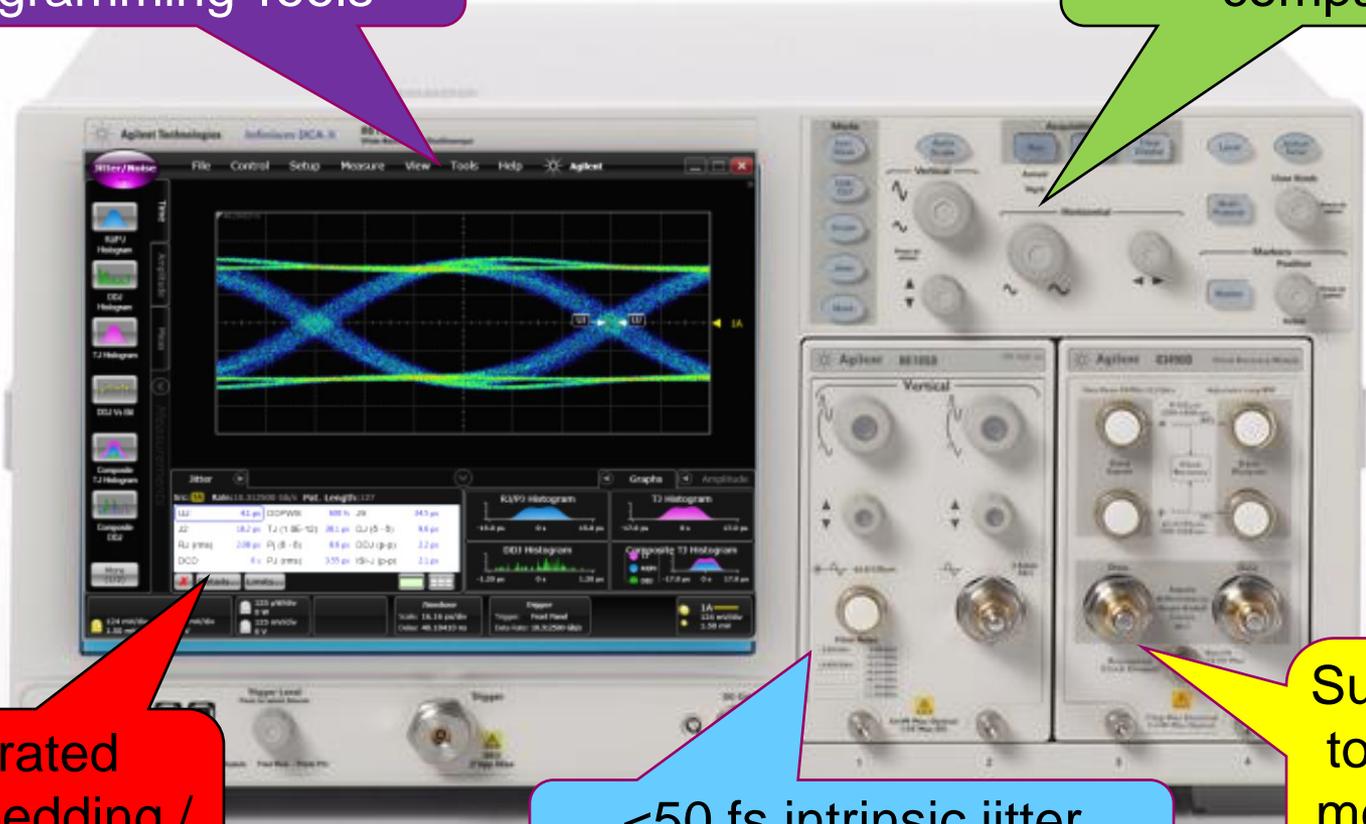


86100D DCA-X Wide-Bandwidth Oscilloscope

Engineered for unmatched measurement accuracy, insight, and ease-of-use

SCPI Recorder & Programming Tools

Fully backwards compatible

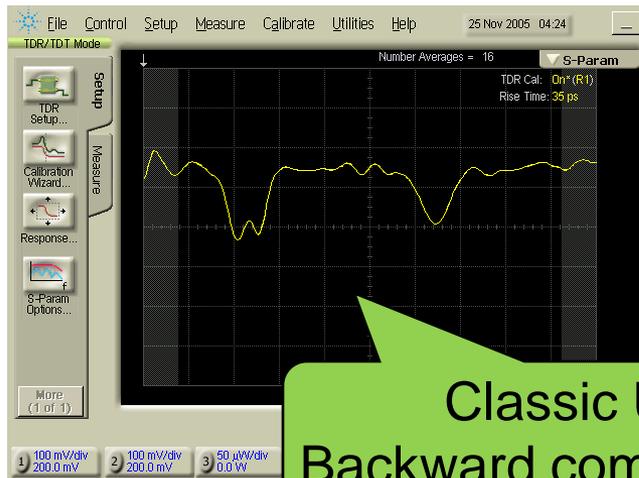
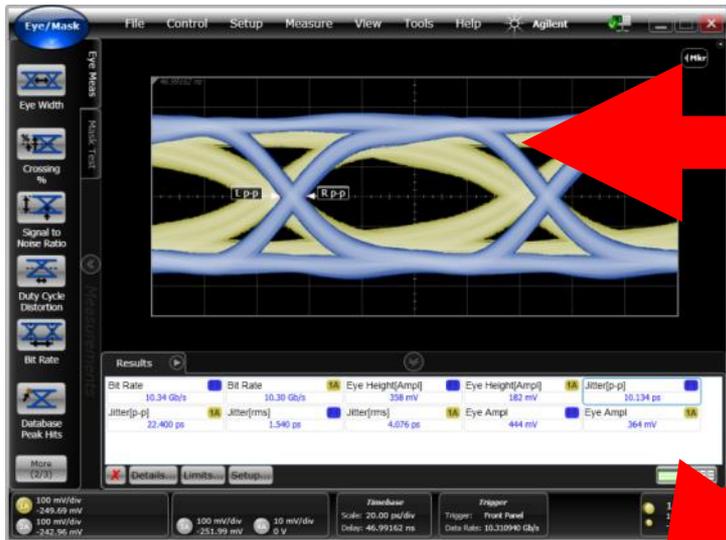


Integrated De-Embedding / Embedding

<50 fs intrinsic jitter (when using 86108B)

Support for up to 16 parallel measurement channels

Four Instruments In One



Classic UI:
Backward compatibility

FlexDCA UI:
Forward compatibility

Optical Modules

86105C Optical/Electrical Module

- 9 GHz amplified optical channel
 - 750-1600 nm
 - 9/125 to 62.5/125 um fibers
 - 155 Mbps to 11.3 Gbps options
- 20 GHz electrical channel

Optimized for greatest **flexibility**



86105D Optical/Electrical Module

- 20 GHz optical channel
 - 750-1650 nm
 - 9/125 to 62.5/125 um fibers
 - 8.5 Gbps to 14.025 Gbps
- 35 GHz electrical channel

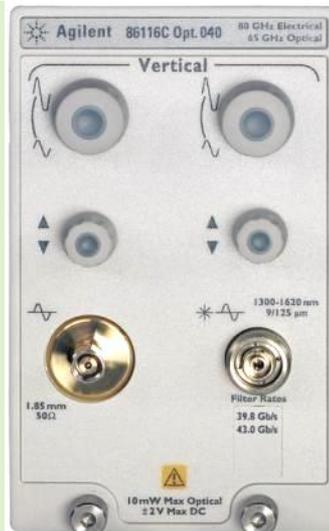
Optimized for best **accuracy**



86116C Optical/Electrical Module

- Option 25: 45 GHz (typical) optical
 - Option 40: 70 GHz (typical) optical
 - 1200-1600 nm
 - 9/125 fiber (single-mode)
- 93 GHz (typical) electrical channel

Optimized for **highest bandwidth**



86115D Dual/Quad Optical Module

- 20 GHz optical channels
 - 750-1650 nm
 - 9/125 to 62.5/125 um fibers
 - 8.5 Gbps to 14.025 Gbps

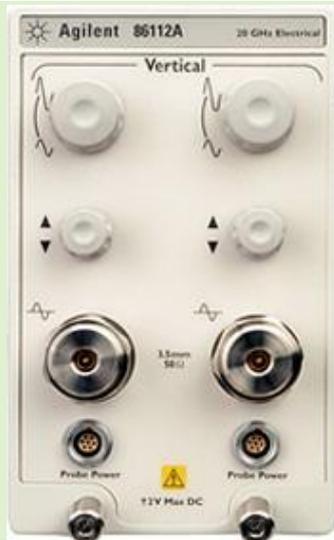
Optimized for **lowest cost of test**



Electrical Modules

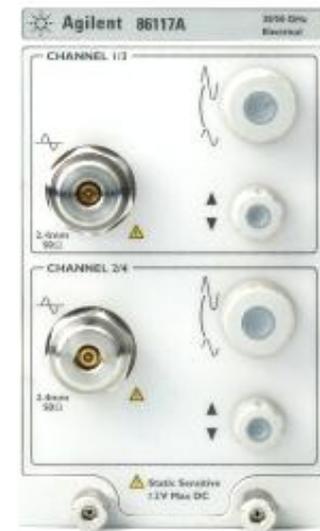
86112A Dual Electrical Module

- 20 GHz electrical channel
- Characteristic rms noise:
 - 0.25 mV (12 GHz BW)
 - 0.5 mV (20 GHz BW)



86117A Dual Electrical Module

- 50 GHz electrical channel
- Characteristic rms noise:
 - 0.4 mV (30 GHz BW)
 - 0.6 mV (50 GHz BW)



86108B Precision Waveform Analyzer

- Combines 3 modules into one (Two 50 GHz electrical channels, 32G clock recovery and precision timebase)
- <50 fs intrinsic jitter
- 50 or 35 GHz bandwidth
- 32 or 16 Gb/s CDR
- Jitter Spectrum Analysis to find root causes



86118A Dual Remote Heads

- 2 remote heads/module
- Max. 2 modules/frame
- 70 GHz channels
- Characteristic rms noise:
 - 0.4 mV (30 GHz BW)
 - 1.3 mV (70 GHz BW)



N1045A Electrical Mini-Module

- 2 or 4 remote heads/module
- Max 4 modules/frame
- 60 GHz channels
- Characteristic rms noise:
 - 0.3 mV (20 GHz BW)
 - 0.8 mV (60 GHz BW)



N4877A Clock Recovery

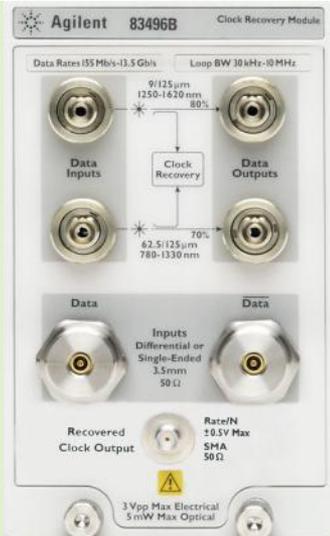
- N4877A: Electrical Only
- N1070A: Electrical with optical front end
- Continuous 0.05 to 32 Gb/s
- Adjustable loop bandwidth
- PLL and Jitter Spectrum Analysis



Specialty Modules

83496B Clock Recovery Module

- Option 100: Electrical Only
- Option 101: Optical & Electrical
- Continuous 0.05 to 14.2 Gb/s
- Adjustable loop bandwidth
- PLL and Jitter Spectrum Analysis



86107A Precision Timebase

- <100 fs jitter (86100D mainframe)



54754A Differential TDR Module

- 18 GHz electrical channel
- 35 ps step generators (*effective rise time software adjustable from 15 to 500 ps*)
- Single-ended or differential
- TDR or TDT operation
- Can be used as a 2-channel receiver module



Application Software

- 200: Jitter Analysis
- 201: Advanced Waveform Analysis
- 202: Enhanced Impedance and S-Parameters
- 300: Amplitude Analysis
- 400: PLL and Jitter Spectrum (83496B or 86108A)
- 401: Advanced Eye Analysis (supports PRBS31)
- 500: Productivity Package
- SIM: InfiniiSim-DCA Waveform Transformation
- JSA: Jitter Spectrum Analysis (86108A/B)
- N1019A: User Defined Applications framework
- N1012A: OIF-CEI:3.0 Compliance Test Application
- N1014A: SFF-8431 Compliance Test Application

The Industry's First 30 GHz Probing System InfiniiMax III probe amp/probe head architecture

Probe Amplifier



Performance verification and de-skew fixture

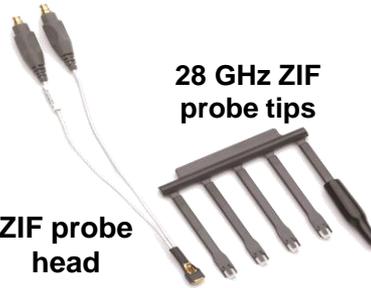


Probe Heads

30 GHz Browser with LED Headlight



ZIF probe head



28 GHz ZIF probe tips

16 GHz solder-in probe head



28 GHz 2.92mm/3.5mm/SMA probe head



Probe Adapters

Sampling scope adapter



High impedance probe adapter

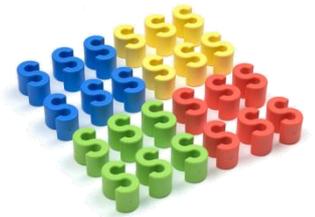


Precision BNC 50 ohm adapter



Accessories

See www.agilent.com/find/N1027A (or lit # 5991-2340EN) for full list



- Compatibility: Backwards compatible with all sampling scope modules ever sold (e.g., for 54750A, 83480A, 86100A/B/C/D mainframes)
Forward compatible with mini-modules, FlexDCA and application software
- Web Site: www.agilent.com/find/dcax (main page)
www.agilent.com/find/86100D_download (firmware upgrades)
- Video: <http://www.youtube.com/watch?v=4vnkC5DuDvk>
(search YouTube “86100D” and/or “FlexDCA” for related videos)
- Sampling Scope Theory: Dennis Derickson, Markus Müller: *Digital Communications Test and Measurement*, Chapter 7; Prentice Hall, 2008 (ISBN 0-13-220910-1)
- Pricing (US):

86100D Mainframe (hardware)	\$21K - \$29K
Licenses for advanced measurements (ea.)	\$3K-\$14K
Application Software	\$4K - \$10K
Electrical Modules (ea.)	\$15K - \$125K
Optical Modules (ea.)	\$36K - \$88K

FlexDCA Software

Applications

- Electrical, Optical, Jitter, Apps SW

Block Diagram

- Dual User Interface concept

Live demo

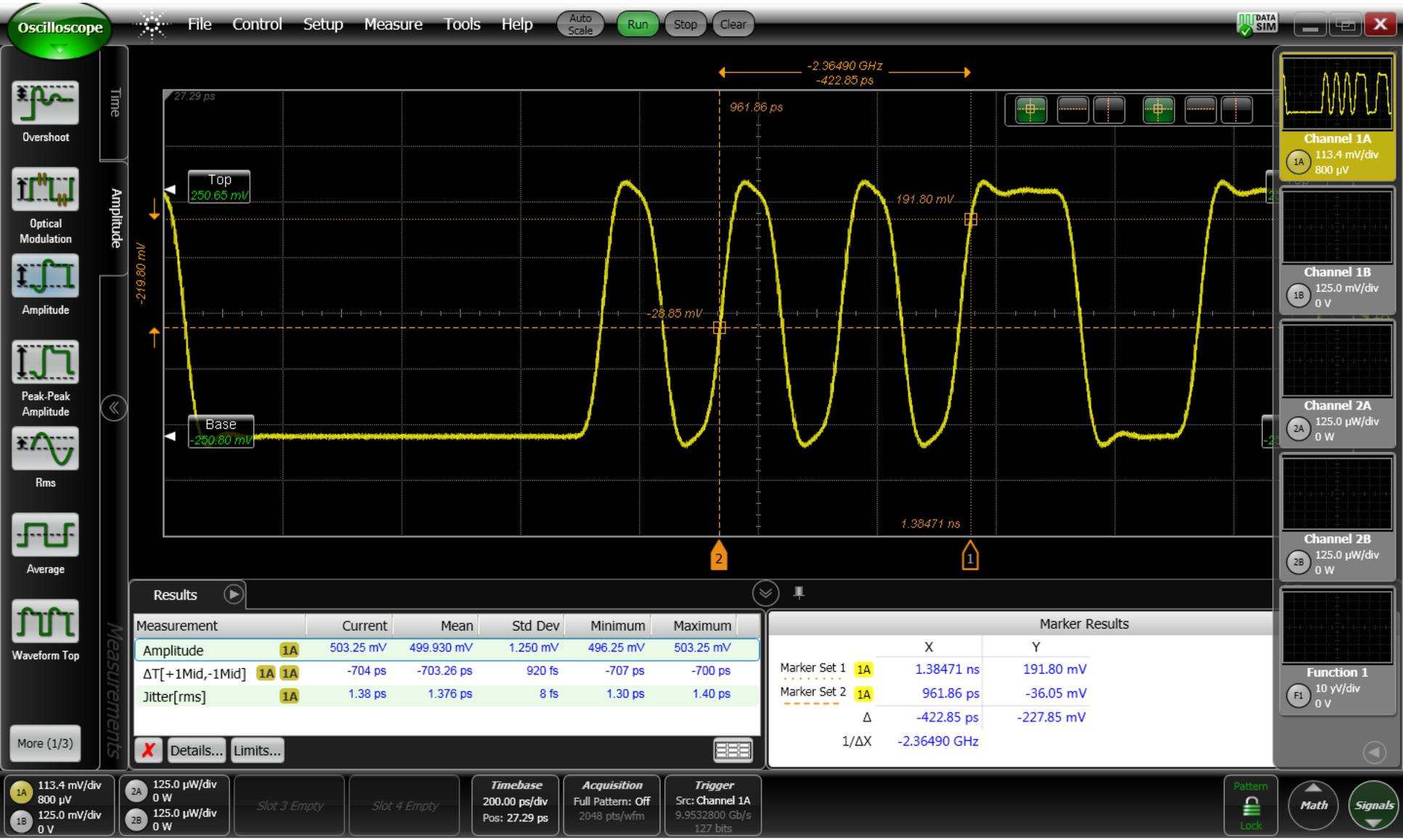
- Get FlexDCA Express fro free!

References

- Website, application notes, etc.

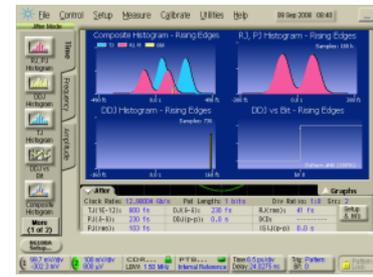
Overview

ToC



Concept Of Dual Interfaces

- Classic UI – *raster graphics*
 - Runs on 86100C and 86100D
 - 100% backward compatibility (incl. remote control)
 - **>15 year old SW architecture** (*now too many constraints/issues*)
- FlexDCA UI - *vector graphics*
 - Runs on 86100D and external PC/Laptop
 - 100% forward compatibility (*future modules may run on FlexDCA only*)
 - **Modern .NET SW architecture** (*more powerful/flexible/easier to enhance*)



Why two interfaces?

- Need new architecture for de-embedding, 16 channels, SIRC, ...
- **Future hardware requires new software technologies**
- New architecture can't be made fully backwards compatible

FlexDCA Modes

Standard Mode is new in FW Rev. A.02.xx

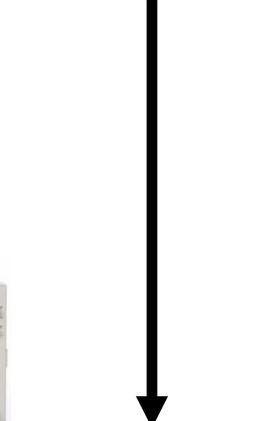
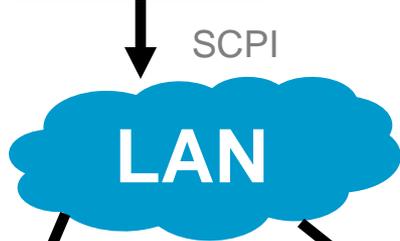
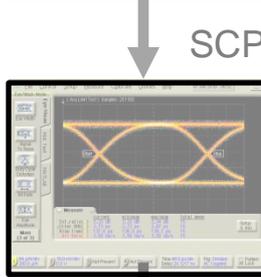
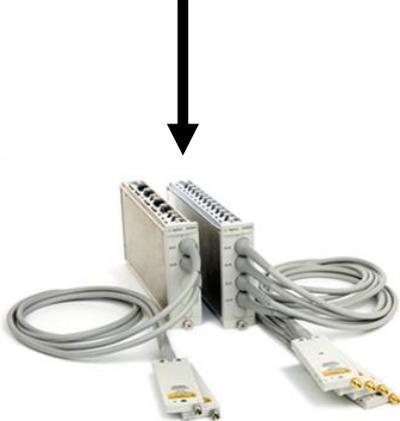
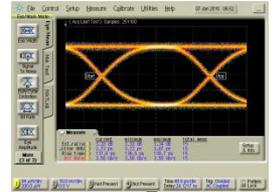
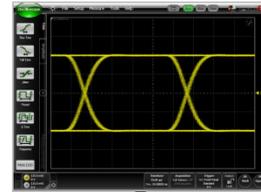
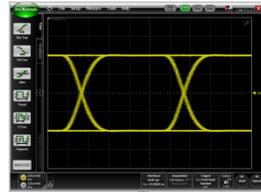
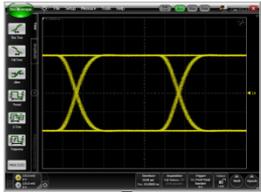
"Current" = shipping in 2012

Standard

Compatibility

Remote

Classic



DCA-J/DCA-X
(Classic UI only)

Implies all current & legacy modules

Mini-modules
All current modules

All current & legacy modules

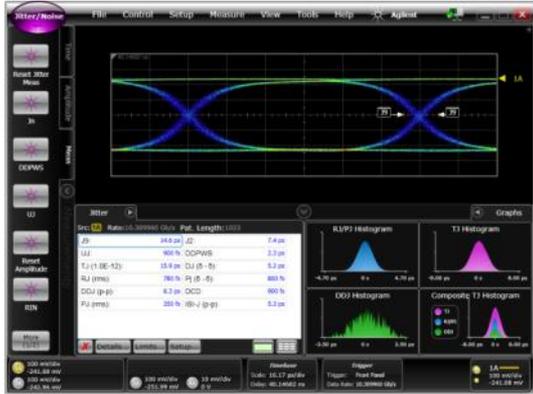
All current & legacy modules

N1010A FlexDCA Application

- DCA application providing new user interface, new capabilities
- Runs on 86100D and on external laptop/PC
- FlexDCA Pro (\$) includes I/O libraries and software licenses
- FlexDCA Express (free) includes signal generator but no advanced feature

Typical Use Cases:

- Remote measurements (“-DCA” license connects to 86100C or 86100D)
- Offline analysis and simulation
- Virtual device demonstration
- Output device for SystemVue
- Training & education



Why Switch to FlexDCA?

Feature	FlexDCA	Classic UI
Channel Count	16	4
Measurement Count	64	4
Differential Measurements	Direct support (easy to use)	Multi-step Math Function
Signal Processing	Add, Subtract, Delay, Align, Embedding, De-embedding, Filters, Transformations, LFE, CTLE, DFE	Add, Subtract, LFE
Channel Deskew	SW: any channel, any delay HW: supported modules up to +/- 65p	HW: supported modules up to +/- 65p
New Measurements / Features	DDPWS, Measurement Regions, SIRC, Mask Margin Uncertainty External HW support (e.g., CDR)	N/A
Compatibility	Classic and future modules (e.g., N10XXX mini-modules)	Classic modules only (861XXX, 834XX, 547XX)
Applications	UDA, OIF-CEI, SFF-8431	MATLAB
Usability	Higher resolution & better graphics Swap / detach / resize windows Copy results to clipboard Find bit sequence Programming Tools / SCPI Recorder Import & simulate waveforms	N/A

FlexDCA Express

- **Free download** from Agilent.com
 - Oscilloscope Mode
 - Eye/Mask Mode
 - Built-In Simulator
 - Load waveforms from file
 - Bessel/Butterworth/Sin(x)/x Filters
 - Align/Delay, Deskew
 - Fast Fourier Transformation
 - SCPI Recorder / SCPI Tools
 - Undo / Redo / History
- *Installation file < 100 Mbytes*

FlexDCA Pro (N1010A)

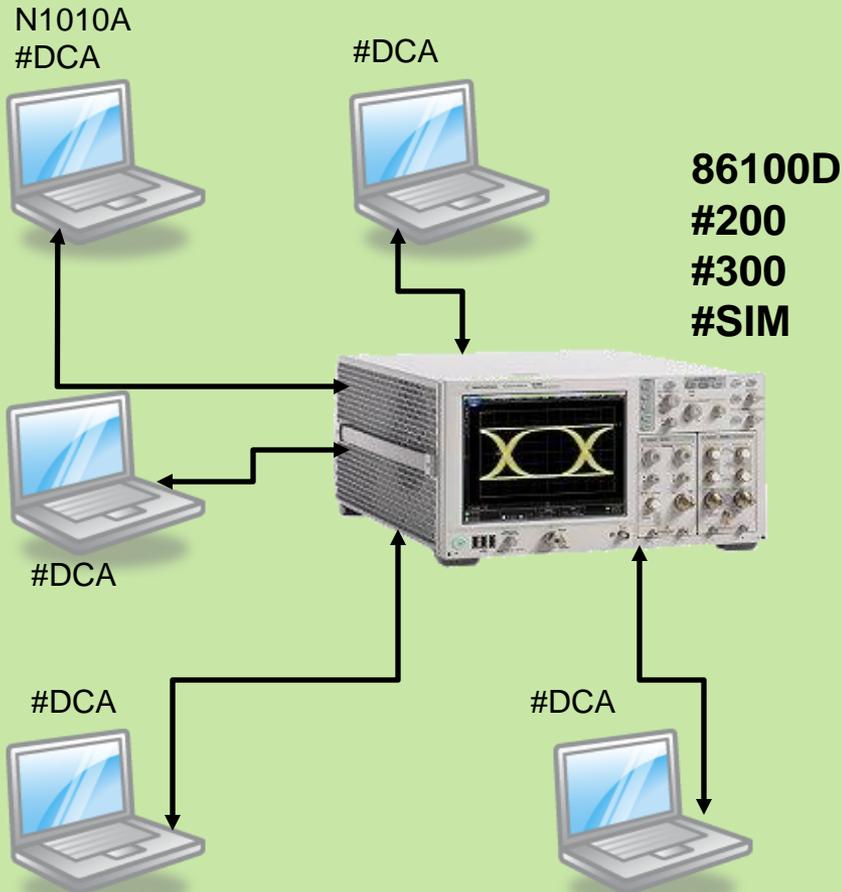
Same features as FlexDCA Express **PLUS**

- Live connectivity to 86100C or 86100D via LAN (#DCA)
 - Jitter Analysis (#200)
 - Equalization – LFE, CTLE, DFE (#201)
 - Amplitude Analysis (#300)
 - Simulation/De-embedding (#SIM)
 - Productivity package (#500)
 - Jitter Spectrum Analysis (86108xU-JSA)
- *Installation file > 900 Mbytes (I/O libraries, license manager)*

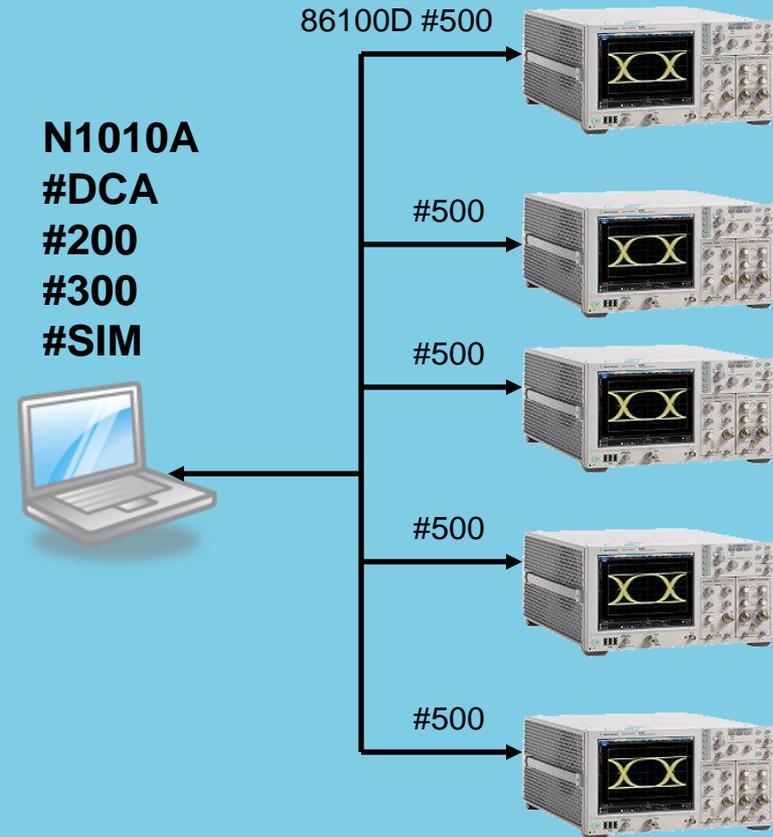
Use Cases For SW Licenses

Should licenses reside on the DCA or the PC?

Multiple people share DCA-X
(e.g., research lab)



Engineer controls multiple DCAs in
manufacturing



FlexDCA References

- Compatibility: 86100D (included)
PC/laptop running MS Windows XP, MS Windows 7 or MS Windows 10
- Web Site: www.agilent.com/find/flexdca
- Brochure: [**Infiniium DCA-X 86100D Wide-Bandwidth Oscilloscope Mainframe and Modules**](#)
(Agilent literature # 5990-5822EN)
- Videos: <http://www.youtube.com/watch?v=DI5JA4eqRuo> (virtual device demo)
<http://www.youtube.com/watch?v=Jk5JeJ7ZBNE> (installation, trial licenses)
- Pricing (US):

N1010AU	FREE
N1010AU-DCA 86100C/D Connectivity	\$0.5K
N1010AU-200/300 Jitter & Noise Analysis	\$14.0K
N1010AU-201 Advanced Waveform Analysis	\$4.7K
N1010AU-SIM Waveform Transformation SW	\$5.3

Upgrades to the latest revision are available free of charge from www.agilent.com/find/N1010A and www.agilent.com/find/86100D download

28G Multimode Receivers

Applications

- 850 nm Multimode for 100 GbE, 32G FC

Key Features

- Channels, Bandwidth, etc.

Performance

- Eye Diagrams

References

- Website, application notes, etc.

86105D-281: One optical, one electrical channel

86115D-282: Two optical channels

ToC

Key features:

- Compatible with 86100C and 86100D mainframes
- 750-1650 nm multi- and single-mode
- Filters for 25.781 and 28.05 Gb/s¹
- Unfiltered optical bandwidth: ≥ 30 GHz (spec TBD)
- Electrical bandwidth ≥ 50 GHz (86105D-281 elec. channel)
- Optional System Impulse Response Correction (SIRC)
- “Software reference receiver” for any rate from ~ 8.5 to ~ 40 Gb/s

¹ The 28.05 Gb/s filter can also be used for 27.739 Gb/s



Optical Performance

Frequency Response: see graph

Eye diagram: see screen capture

PRELIMINARY DATA – NOT SPEC’D

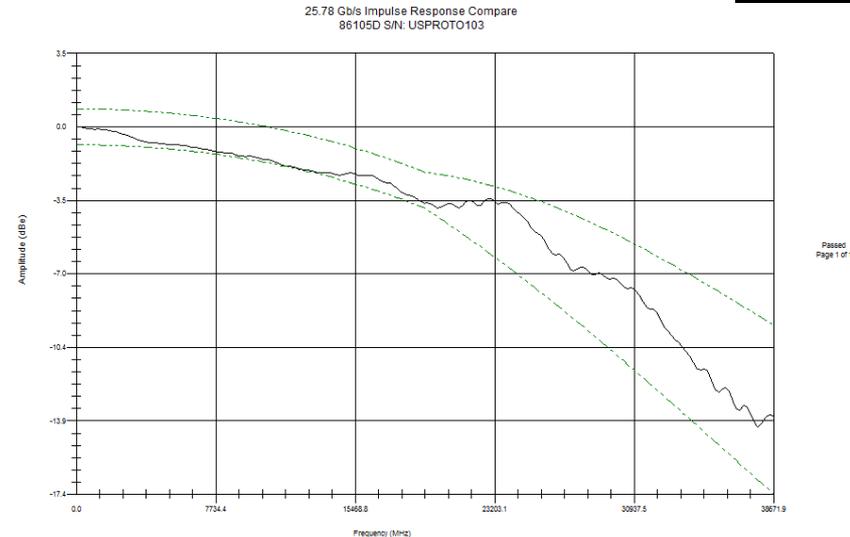
Noise (µW):

Wavelength	25 Gb/s	28 Gb/s
850 nm	15	16
1310/1550 nm	11	12

Sensitivity (dBm):

Wavelength	25.8 Gb/s	28 Gb/s
850 nm	-8	-8
1310/1550 nm	-10	-10

Sensitivity is the characteristic average optical power required for eye mask measurements on signals with ≥ 10 dB ER. Signals with less ER usually require more optical power.



86105D-281, 86115D-282 References

- Compatibility: 86100D with FlexDCA revision A.01.80 or greater (*option ETR highly recommended*)
86100C with firmware revision A.10.80 or greater (*option 001 highly recommended*)
- Web Site: www.agilent.com/find/86105D, www.agilent.com/find/86115D
- Pricing (US):

86105D	Optical/Electrical Module	\$46,749
86105D-281	Single optical channel (25G and 28G)	~\$12,400
86105D-IRC	System impulse response correction	\$ 6,132
86115D	Dual optical module	\$ 0
86115D-282	Dual optical channel (25G and 28G)	~\$84,700
86115D-IRC	System impulse response correction	\$12,448
- Trade-Ins:
 - 30% credit for an 861x5D (legacy) -> 861x5D-281/282 trade-in
 - 20% credit for any other current module -> 861x5D trade-in (any option)
 - 10% credit for any discontinued module -> 861x5D trade-in (any option)

Electrical Mini-Modules

Applications

- Multi-channel I/O semiconductors

Block Diagram

- Configuration choices

Performance

- Bandwidth, intrinsic jitter

References

- Website, application notes, etc.



Standard	Data Rates Gb/s	Link Type
IEEE 802.3ap, 10 G	10.3125	Backplane
IEEE 802.3ba, 40 G	4 x 10.3125	Chip-to-chip, backplane, copper cable
IEEE 802.3ba, 100 G	10 x 10.3125	Chip-to-module
IEEE 802.3ba, 100 G	4 x 25.78	Chip-to-chip, chip-to-module, cable
IEEE 802.3bj, 100 G	4 x 25.78	Backplane
OIF CEI 25G-LR	N x 19.6-28.05	Chip-to-module, backplane
OIF CEI 28G-SR	N x 19.6-28.05	Chip-to-chip
OIF CEI 28G-VSR	N x 19.6-28.05	Host and module PCB traces
Fibre Channel 16X 32X	14.025 28.05	Cable, host and module PCB trace
InfiniBand	10 x 10.3125 12 x 10.5 4 x 25	Cable, host PCB trace
SFF-8431	1 x 10	Host PCB trace

25/28G Standards are under development and are evolving

N1045A Performance

Bandwidth

- Specification: ≥ 60 GHz (65 GHz typical)
- User settings: 65/60/45/35/20 GHz

Remote head configurations:

- 2 or 4 heads per module¹
- 1.85 mm male or female inputs¹
- Up to 16 channels/mainframe

Data acquisition:

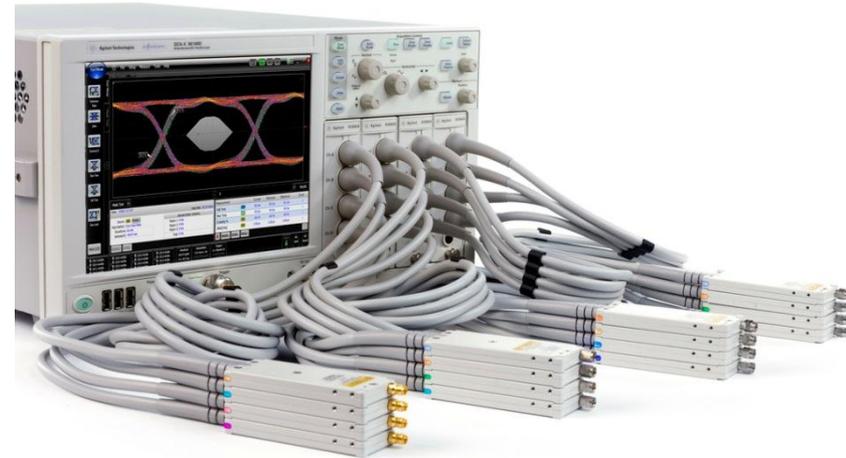
- Simultaneous data acquisition on all channels
- Independent skew control on each sampler

Usability:

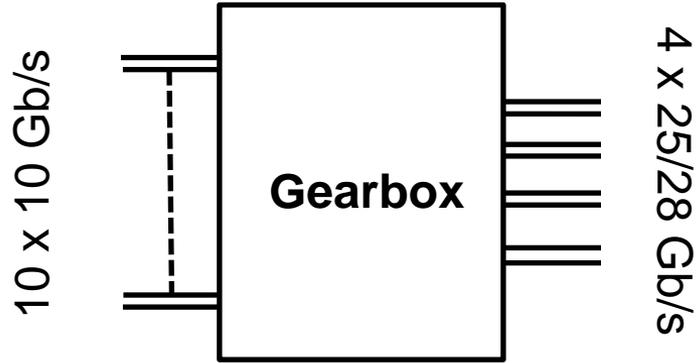
- 10 mm thickness, stackable up to 4 heads²
- Remote head mounting threads, brackets
- Color LED channel identification

¹ Must be specified at time of order

² See cooling requirements when spacing more than four heads very closely



N1045A Application Example



Configuration:

- 86100D/ETR/200/300/SIM Mainframe with jitter analysis and simulation capabilities
- N1045A/04x (quantity 2) provide four differential measurement channels
- 86107A/040 Precision Timebase (PTB) reduces intrinsic jitter to < 200 fs

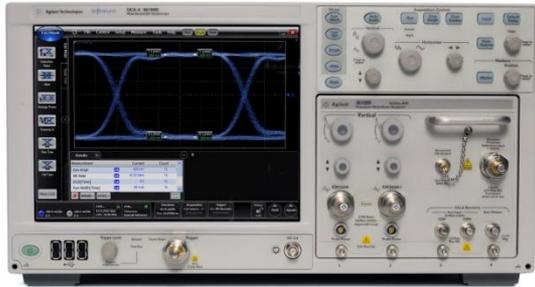
Benefits:

- Efficiently test a quad differential port device operating up to 32 Gb/s
- Saves money - only one mainframe and PTB required
- Saves time – parallel testing on all channels

N1045A or 86108B?

Trade-off intrinsic jitter, throughput and cost

Lowest jitter



86108B

- 2 channels
- 50 GHz bandwidth
- < 50 fs intrinsic jitter
- Integrated clock recovery

HW List price: \$155K
 Cost/Channel: \$77K

Best for quad I/Os



86107A + 2 * N1045A/04x

- 8 channels
- 60 GHz bandwidth
- < 200 fs intrinsic jitter

HW List price: \$238K
 Cost/Channel: \$30K

Highest channel count



4 * N1045A-04x

- 16 channels
- 60 GHz bandwidth
- < 780 fs intrinsic jitter

HW List price: \$362K
 Cost/Channel: \$23K

N1045A References

- Compatibility: 86100D with FlexDCA A.02.00 or greater
(not compatible with classic user interface or older mainframes)
- Web Site: www.agilent.com/find/N1045A
- Video: *<check later>*
- Application note: *<check later>*
- Pricing (US):

N1045A-02F	(two channels, female 1.85 mm inputs)	\$43K
N1045A-02M	(two channels, male 1.85 mm inputs)	\$43K
N1045A-04F	(four channels, female 1.85 mm inputs)	\$83K
N1045A-04M	(two channels, male 1.85 mm inputs)	\$83K
Accessories	(DC blocks, adapters, cables)	<i>ask for quote</i>
- Trade-Ins:
 - 30% credit for an 86118A -> N1045A trade-in
 - 20% credit for any other current module -> N1045A trade-in
 - 10% credit for any discontinued module -> N1045A trade-in

Precision Waveform Analyzer

Applications

- Next generation semiconductors

Block Diagram

- Three modules integrated into one

Performance

- World's most accurate scope

References

- Website, application notes, etc.

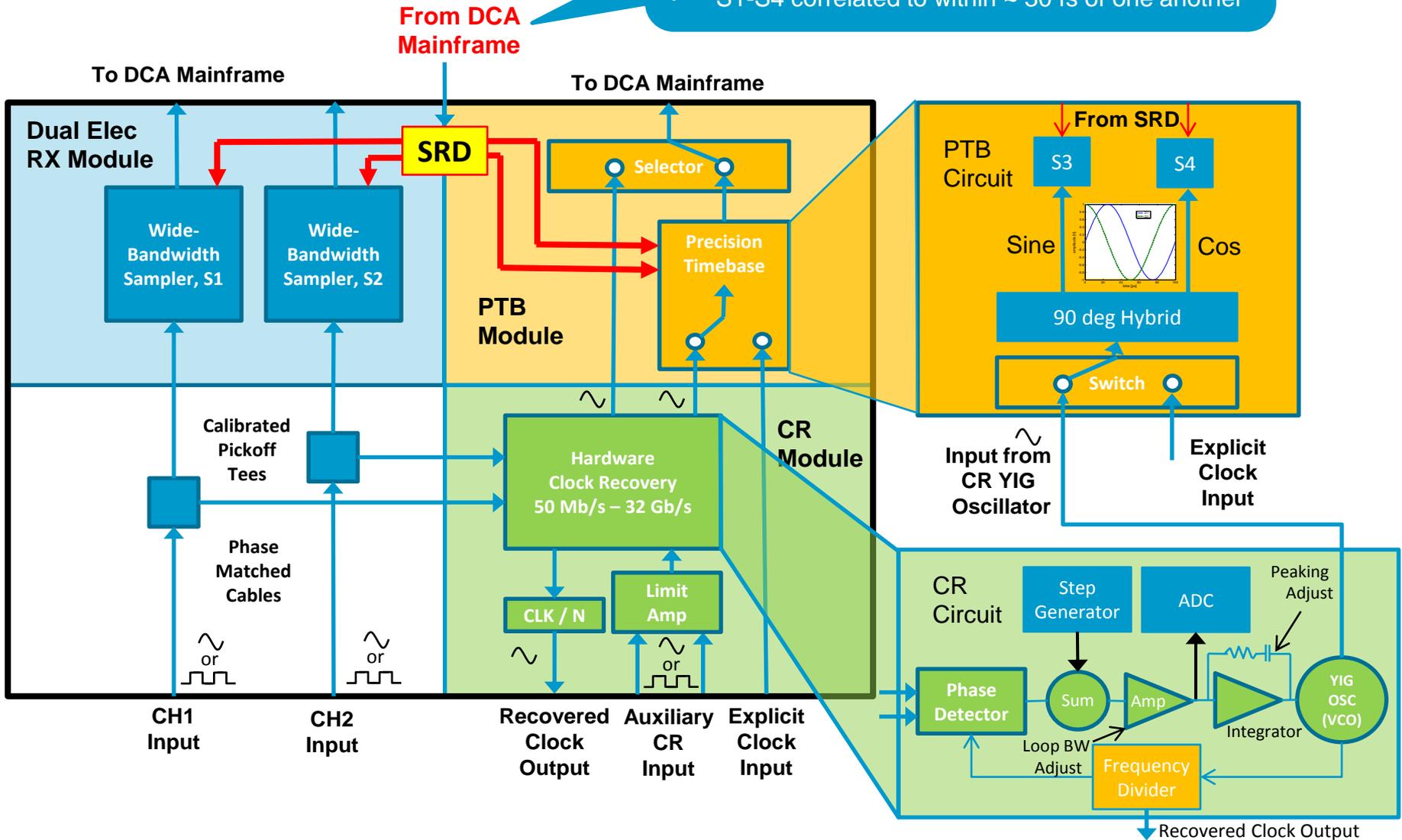
Standard	Data Rates Gb/s	Link Type
IEEE 802.3ap, 10 G	10.3125	Backplane
IEEE 802.3ba, 40 G	4 x 10.3125	Chip-to-chip, backplane, copper cable
IEEE 802.3ba, 100 G	10 x 10.3125	Chip-to-module
IEEE 802.3ba, 100 G	4 x 25.78	Chip-to-chip, chip-to-module, cable
IEEE 802.3bj, 100 G	4 x 25.78	Backplane
OIF CEI 25G-LR	N x 19.6-28.05	Chip-to-module, backplane
OIF CEI 28G-SR	N x 19.6-28.05	Chip-to-chip
OIF CEI 28G-VSR	N x 19.6-28.05	Host and module PCB traces
Fibre Channel 16X 32X	14.025 28.05	Cable, host and module PCB trace
InfiniBand	10 x 10.3125 12 x 10.5 4 x 25	Cable, host PCB trace
SFF-8431	1 x 10	Host PCB trace

25/28G Standards are under development and are evolving

86108B Block Diagram

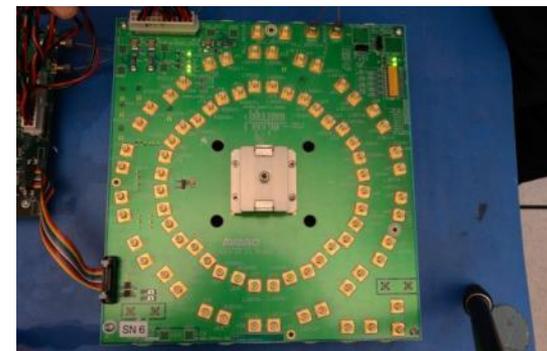
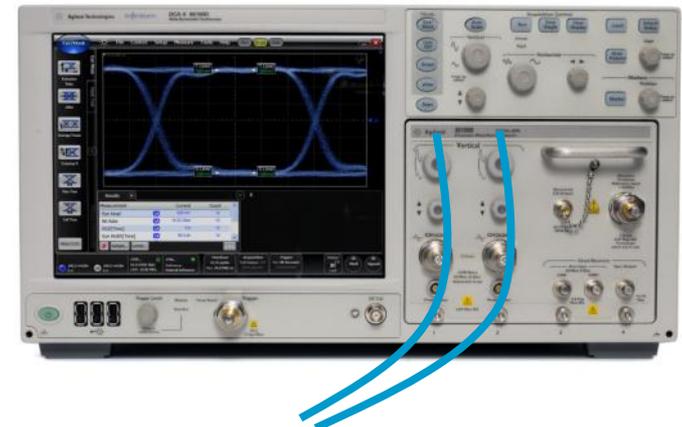
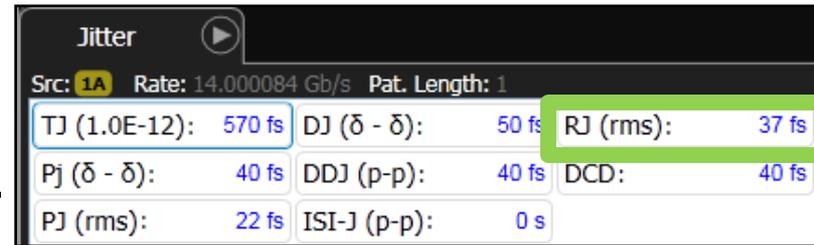
Simultaneous samples taken by S1-S4.

- S1, S2 measure input waveform amplitudes
- S3, S4 provide "timestamp" info (PTB)
- S1-S4 correlated to within ~ 30 fs of one another



86108B Performance

- WORLD'S LOWEST SCOPE JITTER!!
 - See the true performance of your device.
 - Provides more margin for your devices.
- Simple and easy setup
 - Connect only signal (no trigger required)
- Signal degradation minimized
 - Internal pickoffs
 - Phase matched cabling
 - Everything calibrated internally



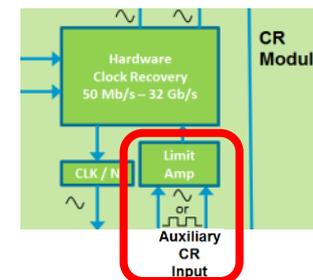
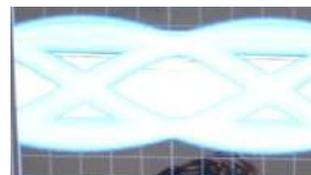
86108B-400 Auxiliary Clock Recovery Input

Auxiliary CR Input Data Range: 50 Mb/s – 5 Gb/s

Provides improved performance in the following situations:

1. Marginal Input Signals

- a. Closed eyes (large amounts of ISI)
=> No edges for CR circuit.
- a. Low amplitude data or clock signals
=> Noisy signal leading to high trigger jitter.
- a. Signals that have excessive noise on slow edges (e.g. Ref Clocks in the MHz range).
=> Minimize AM to PM conversion due to limit amp.

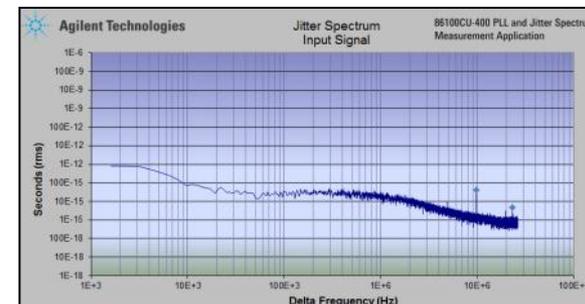


2. Improved Phase Noise Measurements

- => Bypass CH1/CH2 pickoff circuits, improve SNR into CR circuit.

3. Measurements on data rates above the 32 Gb/s Clock Recovery limit

- => e.g. 40 Gb/s data into CH1/CH2, Divide-by-4 clock into Auxiliary CR Input (ultra-low jitter, but low BW too)



86108B Key Features & Benefits

1. Highest Accuracy

1. Ultra-Low Jitter <50 fs typ (<70 fs spec)
2. Bandwidth > 50 GHz
3. Low Noise < 900 μ V
4. High Signal Integrity CR Pick-off (integrated)
5. ~ 0ns Clock-to-Data delay (best accuracy)

2. Best in world ease-of-use

1. Single Connection
2. Easy Setup
3. Integrated HW Clock Recovery and PTB

3. New Features

1. Extended Data Rates: 50 Mb/s to 32 Gb/s (continuous)
2. Higher Clock Recovery Loop BW (20MHz)
3. Higher Bandwidth (> 50 GHz, 3dB BW)
4. Max Vertical Scale: 140 mV/div
5. Aux CR Input with built-in Limit Amp (50 M- 5 Gbps), minimizes AM->PM conversion for slow edges)



- Compatibility: 86100C and 86100D with firmware revision A.10.70 or greater
(option 86100C-001 or 86100D-ETR highly recommended)
- Web Site: www.agilent.com/find/86108B
- Video: <http://www.youtube.com/watch?v=XIJgURRp-KM>
- Application note: [Tips and Techniques for Accurate Characterization of 28 Gb/s Designs](#)
(Agilent literature # 5990-9784EN)
- Pricing (US):

86108B (35 GHz BW, 16 Gb/s CDR):	\$80K
Option HBW (increases BW to 50 GHz)	add \$20K
Option 232 (increase CDR to 232 Gb/s)	add \$25K
Option JSA (Jitter Spectrum Analysis)	add \$4K
Accessories (phase trimmers, DC blocks, cables)	<i>ask for quote</i>
- Trade-Ins:

30% credit for an 86108A -> 86108B trade-in
20% credit for any other current module -> 86108B trade-in
10% credit for any discontinued module -> 86108B trade-in

Jitter Spectrum Analysis

Applications

- Find root causes of jitter

Science

- JTF versus OJTF

Performance

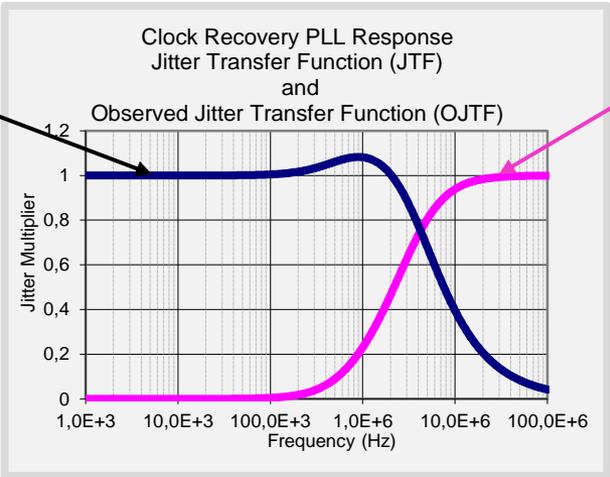
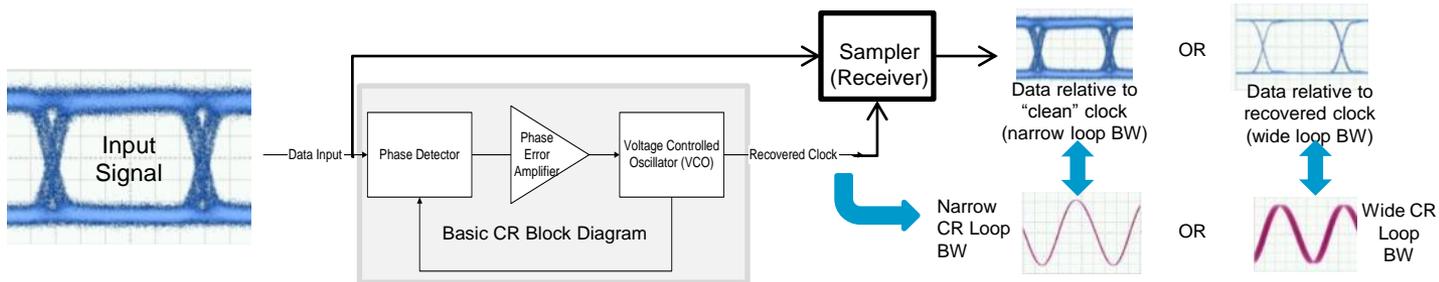
- Emulate *any* CDR

References

- Website, application notes, etc.

Clock Recovery Basics

- CR manages jitter in the system
- Standards specify CR Phase Locked Loop (PLL) **order, bandwidth, peaking**



“Observed Jitter Transfer Function” (OJTF)

- indicates the jitter that is “observed” by the receiver (scope)
- high frequency jitter on the data stream is “transferred” to the receiver (HPF)

JTF= Closed loop gain

$$= \frac{\phi_{out}}{\phi_{in}} = \frac{A(s)}{1 + A(s)} = G(s) = |G(s)|e^{j\phi(s)}$$

$$OJTF = 1 - JTF$$

$$= 1 - G(s) = 1 - |G(s)|e^{j\phi(s)}$$

BEWARE of Clock Recovery (PLL) Definitions!

- Standards (and scopes) describe PLL requirements differently.

Agilent 86100C/D Sampling Scope

- CR loop BW setting configures **JTF**
- Based on SONET/SDH (decades old)

Agilent 90K Series Real-time Scope

- CR loop BW setting configures **OJTF**
- Based on SATA definition

86108A/B

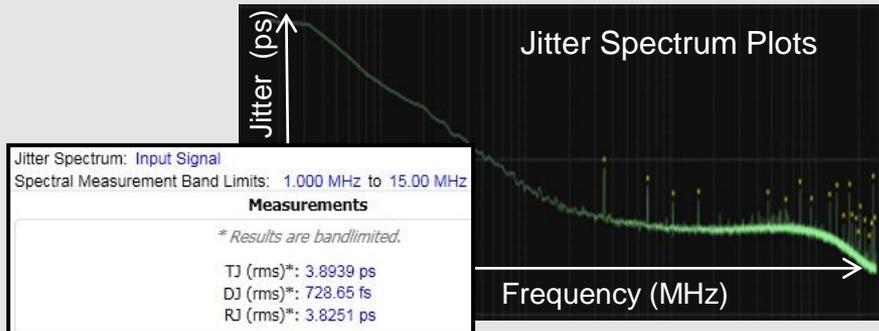


1. Improves jitter measurement accuracy

- Complements 86100C/D-200 “Jitter Mode”
- Emulates an “ideal” clock recovery (CR) response (user specified); analyze “what-if” scenarios using different CR responses
- Compensates for “non-ideal” hardware CR response that can increase random jitter

2. Improves insight into jitter

- Jitter magnitude vs frequency plots
- Helps to isolate jitter problems more quickly
- Emulate “ideal” software CR design
- Bandlimited TJ/DJ/RJ measurements

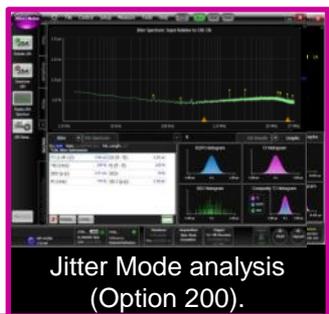
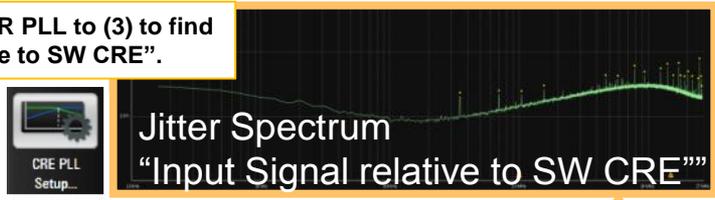


3. Simplifies clock recovery setup

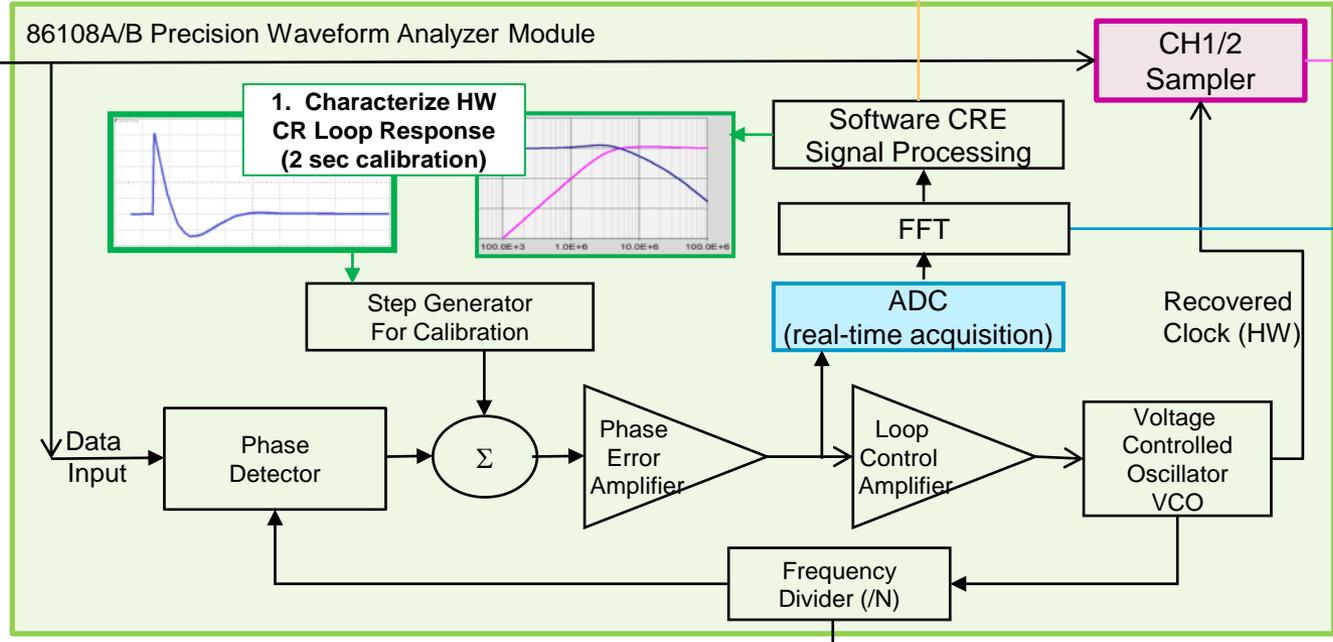
- Easy setup of loop order, bandwidth, peaking (or damping factor)
- Visual aid of Jitter Transfer Function (JTF) and Observed JTF (OJTF)
- Automatic calculation between JTF and OJTF

How is JSA done?

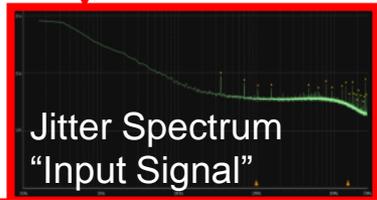
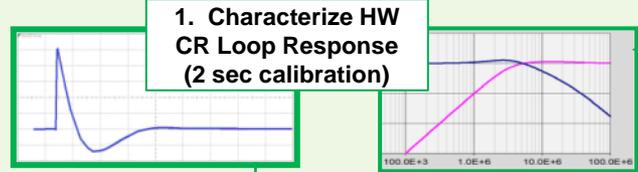
4. Embed desired SW CR PLL to (3) to find "Input signal relative to SW CRE".



2b. Simultaneous Jitter Mode measurement using high BW sampler.
5. Calculate difference in RJ between (2a) & (4); optimize Jitter Mode result (2b).

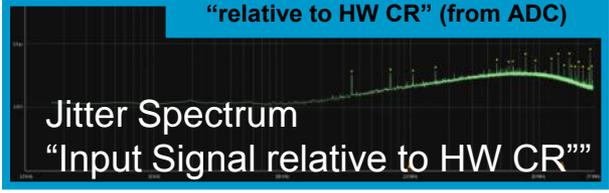


Data Input



3. De-embed loop response (1) from ADC signal (2) to determine Jitter Spectrum of "Input Signal".

2a. Measure Jitter Spectrum "relative to HW CR" (from ADC)



1. Jitter Optimization – 25 Gb/s Example

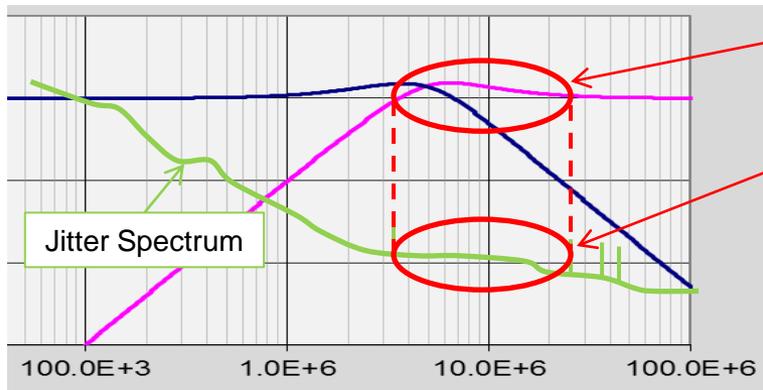
Hardware Clock Recovery (CR)

- behaves like a “real” receiver
- may have non-ideal bandwidth, peaking, roll-off

Hardware CR with Software Clock Recovery Emulation (CRE)

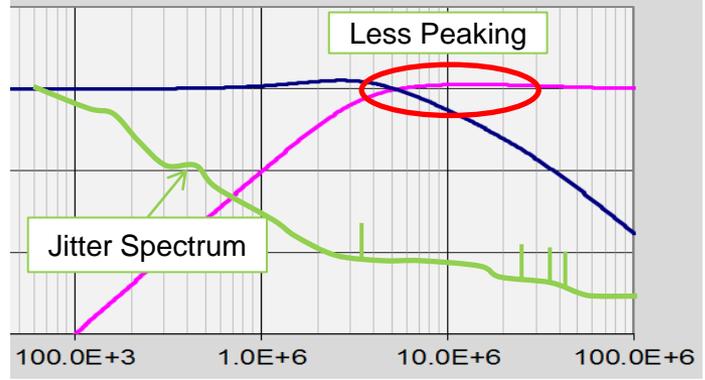
- Emulates “ideal” Software Clock Recovery
- Automatically optimize Jitter Mode (Option 200) results using an “ideal” Clock Recovery PLL

HW CR Loop Response



HW CR response may have higher peaking in OJTF than “desired”.
 This will amplify jitter in this region.
Note – significance depends on DUT jitter spectrum.

Desired SW CR Loop Response



Apply “ideal” PLL using Software Clock Recovery Emulation

Jitter			
TJ (1.0E-12):	6.40 ps	DJ ($\delta - \delta$):	2.27 ps
RJ (rms):	302 fs	Pj ($\delta - \delta$):	430 fs
DDJ (p-p):	2.52 ps	DCD:	10 fs
PJ (rms):	180 fs	ISI-J (p-p):	2.36 ps

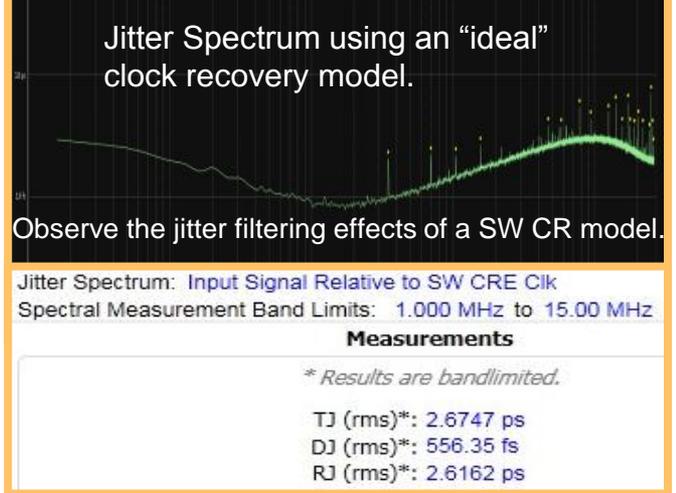
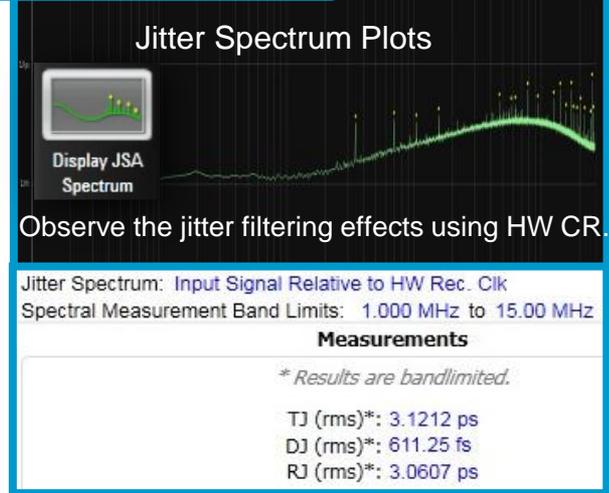
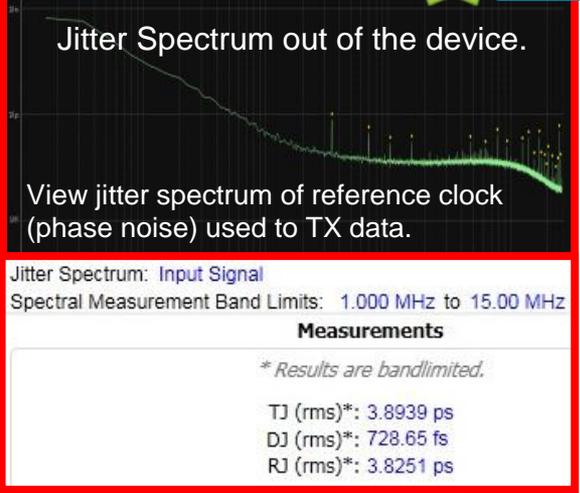
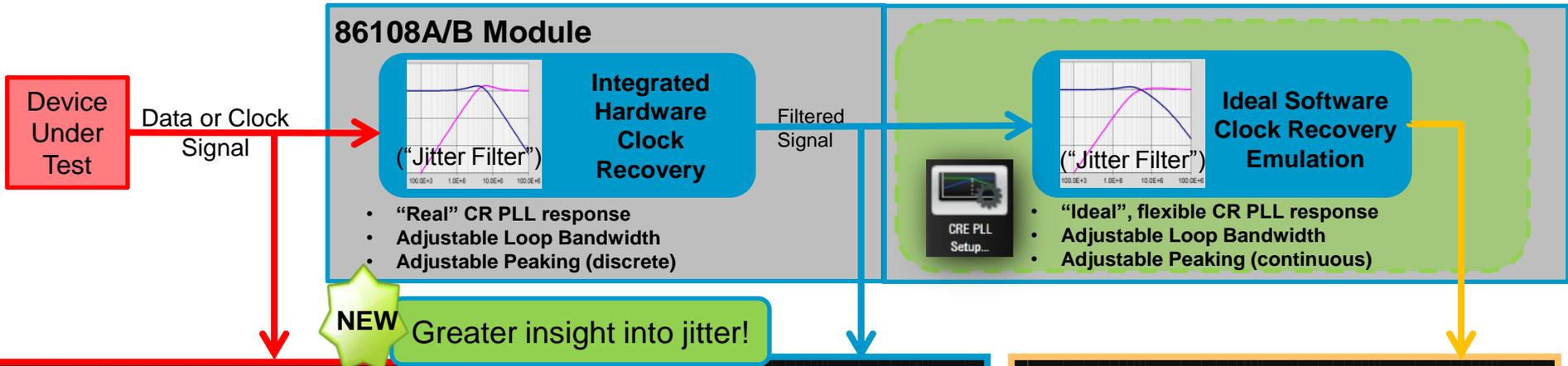
Jitter Mode with hardware clock recovery

Jitter			
*CRE Jitter Optimization			
TJ (1.0E-12):	5.66 ps	DJ ($\delta - \delta$):	2.26 ps
*RJ (rms):	249 fs	Pj ($\delta - \delta$):	360 fs
DDJ (p-p):	2.51 ps	DCD:	10 fs
PJ (rms):	178 fs	ISI-J (p-p):	2.30 ps

Higher Accuracy

Jitter Mode with SW ClkRec Emulation enabled

2. Improved Insight Into Jitter

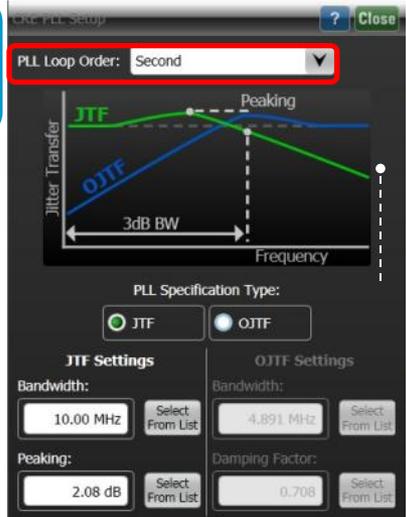


Simplified CR Setup

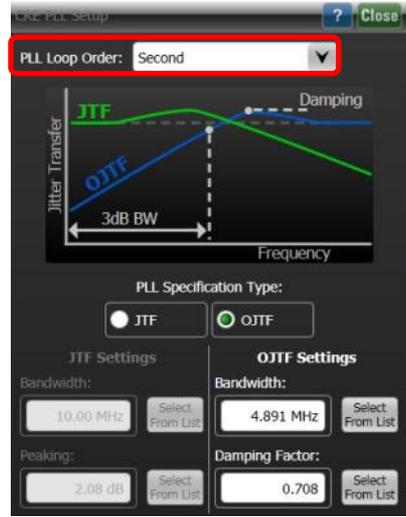
Setup Jitter Transfer Function (JTF) and/or Observed JTF (OJTF) parameters.



1st Order PLL:
JTF BW = OJTF BW
(no peaking)



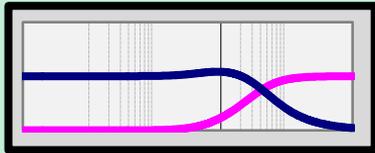
2nd Order, Type 2 PLL:
JTF BW > OJTF BW



3rd Order PLL:
JTF BW > OJTF BW

Standards usually specify Clock Recovery PLL parameters using:

- Loop Order (roll-off)
- Bandwidth (3dB)
- Peaking (or Damping Factor)



BEWARE of Clock Recovery (PLL) Definitions!
Standards describe clock recovery requirements differently!



Agilent 86100C/D DCA Sampling Scope

- CR loop BW setting configures **JTF** (LPF)
- Based on SONET/SDH (decades old)

Agilent 90K Series Real-time Scope

- CR loop BW setting configures **OJTF** (HPF)
- Based on SATA definition

- Compatibility: 86108B and 86108A with firmware revision A.10.70 or greater
(mainframe needs options 86100C-001/200 or 86100D-ETR/200)
- Web Site: www.agilent.com/find/86108B-JSA
- Video: <http://www.youtube.com/watch?v=CwmogDzPuH8>
- Application note: TBD
(Agilent literature # TBD)

- Pricing (US):

86108B-JSA (for new 86108B orders)	\$4K
86108BU-JSA (upgrading existing 86108B)	SSC + \$4K
86108AU-JSA (upgrading existing 86108A)	SSC + \$4K
SSC (<i>Service Center Charge</i>)	TBD

- Trade-Ins:

30% credit for an 86108A -> 86108B trade-in
20% credit for any other current module -> 86108B trade-in
10% credit for any discontinued module -> 86108B trade-in

Standard Compliance Apps

Application

- OIF-CEI 3.0

Application

- SFF-8431

Application

- IEEE 802.3 KR/CR

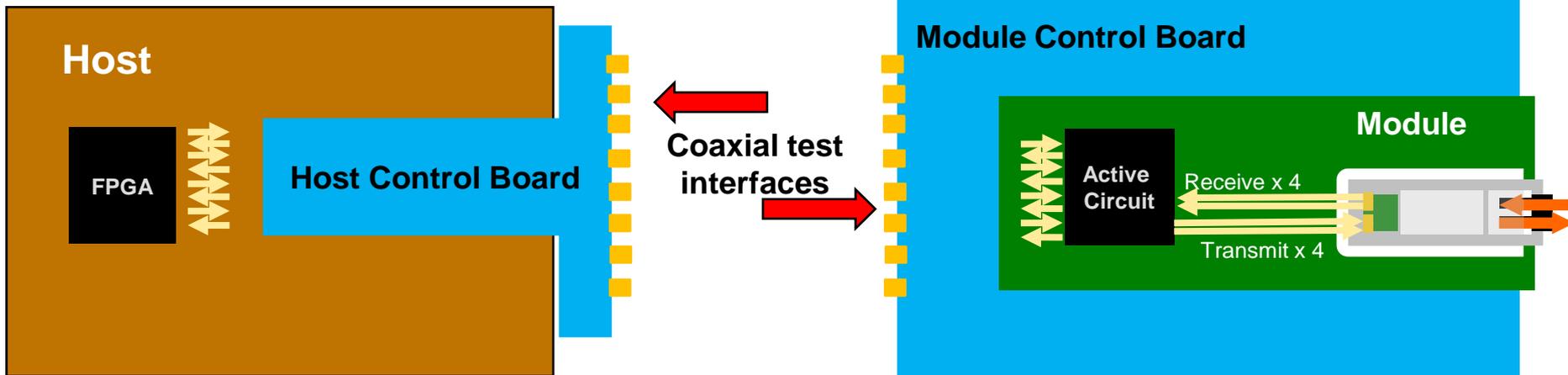
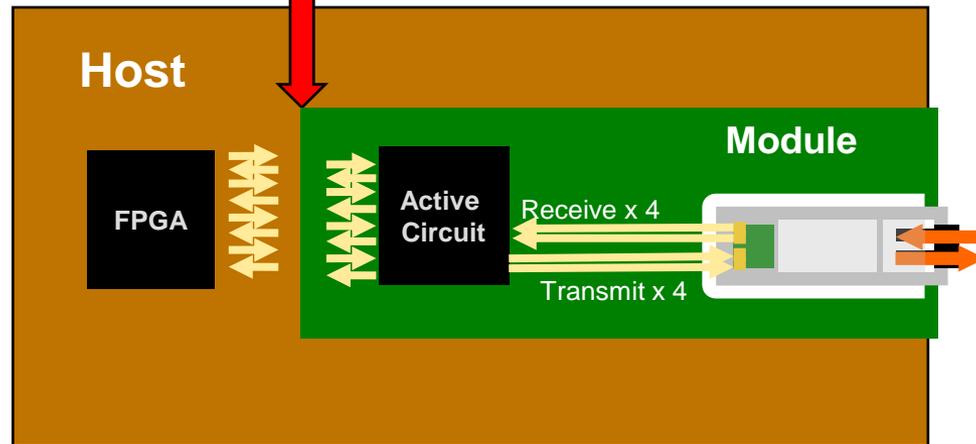
References

- Website, application notes, etc.



Typical 11G/25G/28G Blocks & Test Points

OIF CEI, SFF-8431
Interfaces



N1012A CEI 3.0 Application for 86100D

Reduce hours of testing to a few minutes

Convenient groups for CEI interfaces

Utilities for de-skew and CTLE optimization

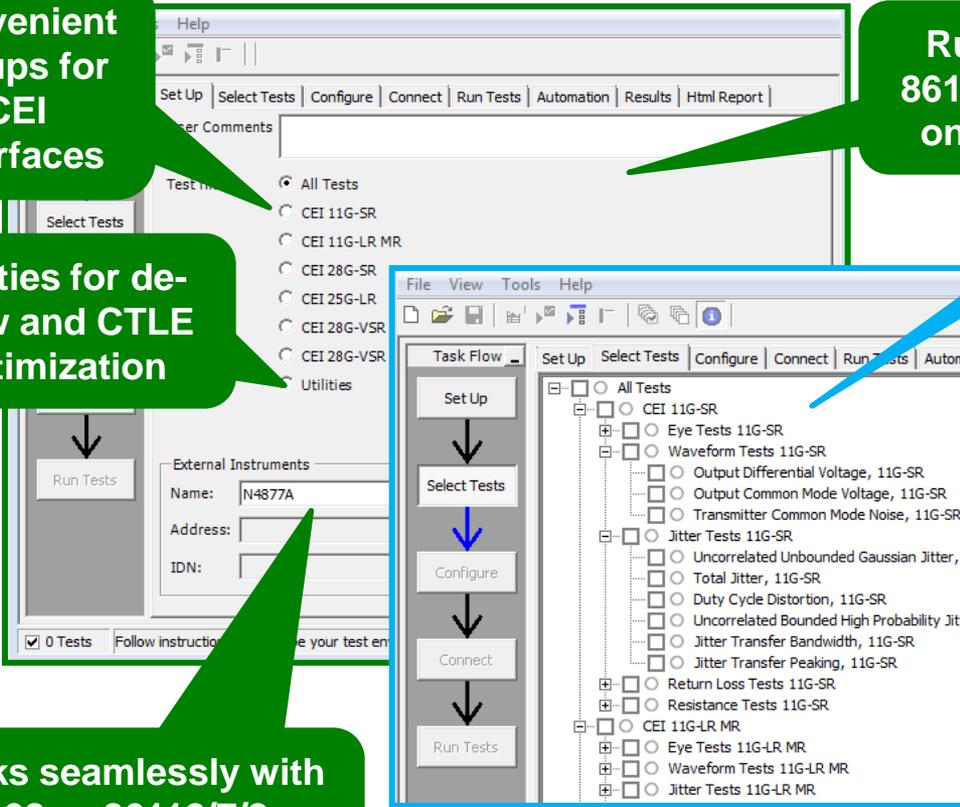
Works seamlessly with 86108 or 86112/7/8 + 86107A + N4877A

Run on 86100D or on a PC

Includes all tests for each interface

Test to compliance or custom limits

Concise compliance reports



User Defined OIF_CEI.3_0 Test Report

Overall Result: **FAIL**

Test Configuration Details	
Test Session Details	
FlexDCA SW Version	P:01.80.27
DCA Model Numbers	Frame: N1010A, Slot1: 86108A, Slot2: Not Present, Slot3: Not Present, Slot4: Not Present
DCA Serial Numbers	Frame: MY50100109, Slot1: MY50150138, Slot2: XXXXXXXXXXXX, Slot3: XXXXXXXXXXXX, Slot4: XXXXXXXXXXXX
Application SW Version	0.01.0382
Debug Mode Used	No
Compliance Limits (official)	Spec01.0m
Last Test Date	4/18/2012 9:18:21 AM

Summary of Results

Test Statistics	Failed	Passed	Total
Failed	2	10	12

Margin Thresholds

Warning	Critical
< 2 %	< 0 %

Pass #	Failed #	Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Baud Rate_11G-SR	10.001862000Ggbs	4.1 %	9.950000000Ggbs <= VALUE <= 11.200000000Ggbs
✓	0	1	Rise Time_11G-SR	41.6ps	73.3 %	VALUE > 24.0ps
✓	0	1	Fall Time_11G-SR	67.4ps	180.8 %	VALUE > 24.0ps
✓	0	1	Output Differential Voltage_11G-SR	470mV	26.8 %	360mV <= VALUE <= 770mV
✗	1	1	Output Common Mode Voltage_11G-SR	-1mV	3.6 %	50mV <= VALUE <= 3.550V

Eight CEI Interfaces

- 6G Short and Long Reach
- 11G Short, Medium and Long Reach
- 25G Long Reach and 28G Short Reach
- 28G Very Short Reach (host to module and module to host)

Nearly 120 Tests

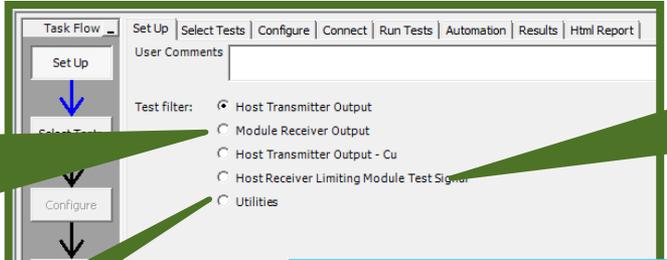
- Baud rate
- Rise and fall times
- Differential and common mode amplitudes
- Common mode noise
- Random, DCD, deterministic, and total jitters
- Eye opening
- Differential and common mode return losses
- Differential to common mode conversion losses
- Utilities for de-skew and CTLE



*Typical HW configuration:
86100D/ETR/GPI/200/201/300/SIM
86108B/232/HBW
(other configurations supported)*

N1014A SFF-8431 Application for 86100D

Reduce hours of testing to a few minutes



Convenient groups for SFF interfaces

Utilities for de-skew

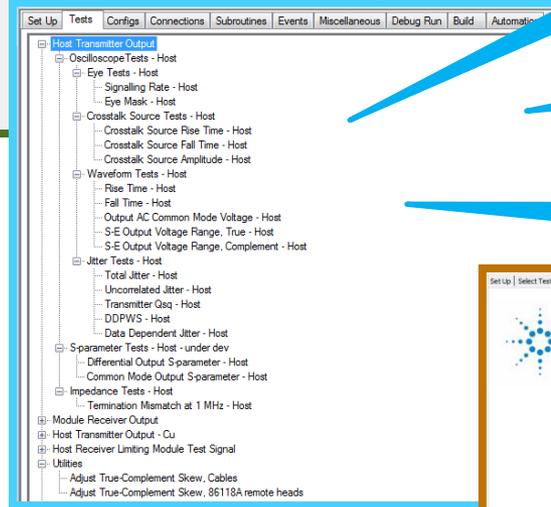
Works seamlessly with 86108 or 86112/7/8 or 54754A + 86107A + N4877A

Run on 86100D or on a PC

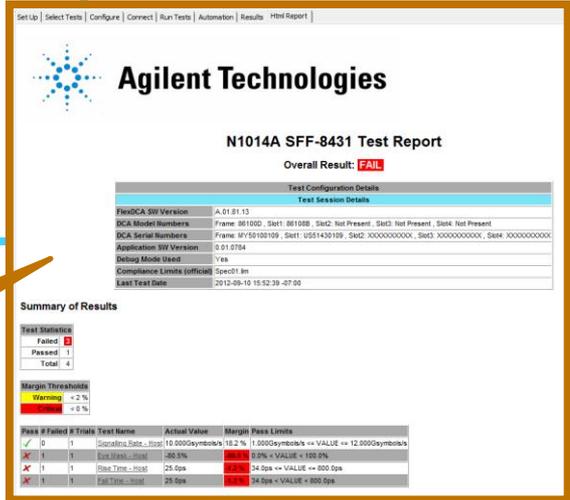
Includes all tests for each interface

Obtain S-parameters directly from ENA/ PNA

Test to compliance or custom limits



Concise compliance reports



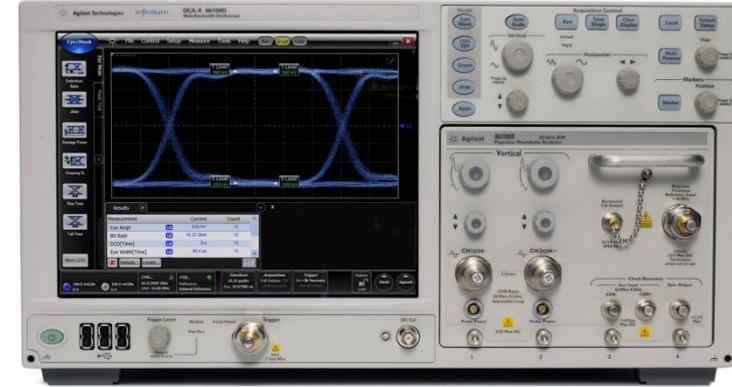
N1014A SFF-8431 Application Details

Seven SFF-8431 Interfaces:

- Host transmitter output
- Module receiver output
- Host transmitter output for Copper
- Host receiver limiting module test signal
- Host receiver linear module test signal
- Module transmit input signal
- Host receiver stress generator

About 70 Tests

- Signaling rate
- Rise and fall times for outputs and crosstalk
- Differential, single-ended, crosstalk and common mode amplitudes
- Common mode noise
- Jitter: Total, DDJ, UJ, QSQ, 99%, DDPWS
- TWDP (through user-provided script)
- Eye mask
- Differential and common mode S-parameter
- Differential to common mode conversion loss



*Recommended HW configuration:
86100D/ETR/GPI/200/201/300/SIM
86108B/216/LBW
(other configurations supported)*

N108xA IEEE 802.3 KR/CR Applications

Reduce hours of testing to a few minutes

Convenient groups for IEEE 802.3 clauses

Utilities for de-skew

Works seamlessly with 86108 or 86112/7/8 or 54754A + 86107A + N4877A

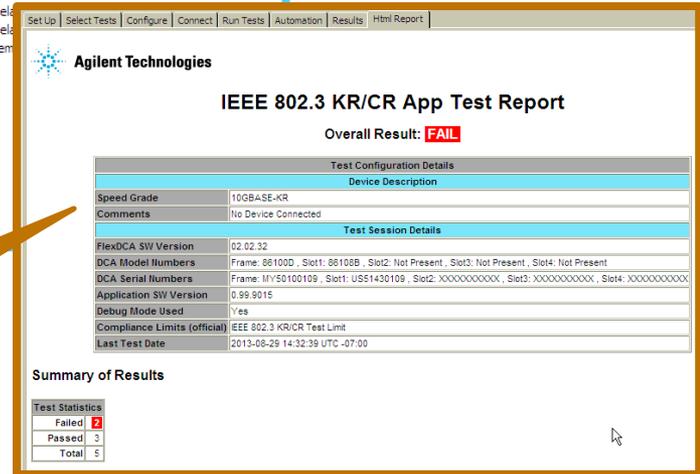
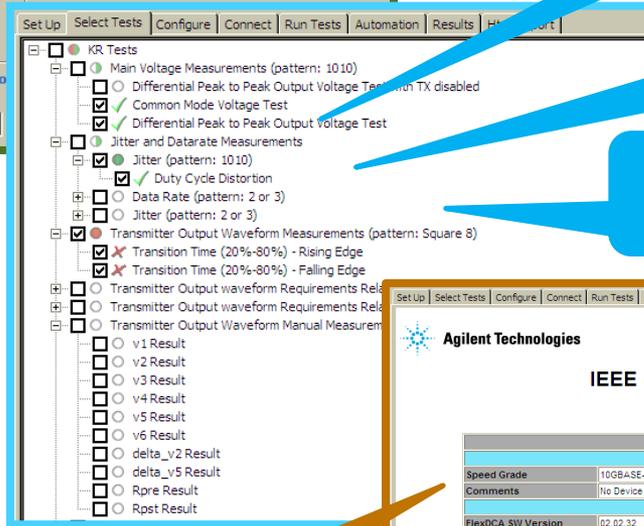
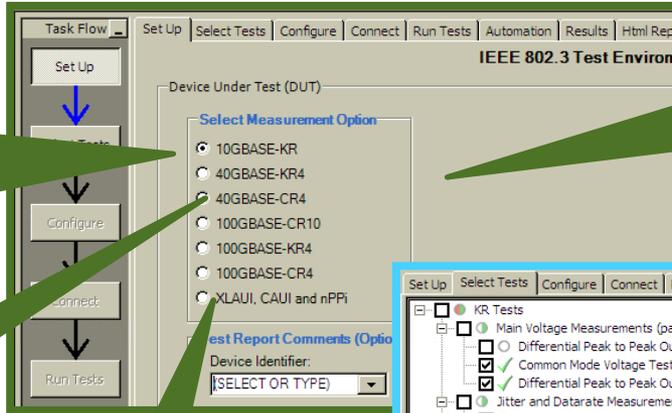
Run on 86100D or on a PC

Includes all tests for each interface

Obtain S-parameters directly from ENA/PNA

Test to compliance or custom limits

Concise compliance reports



N108xA IEEE 802.3 KR/CR Application Details

Nine IEEE 802.3 Clauses

- 10G-KR / 40G-KR4
- 40G-CR4 / 100G-CR10
- 100G-KR4 / 100G-CR4
- XLAUI / CAUI / nPPI

About 150 Tests

- Signaling rate
- Rise and fall times
- Differential & CM amplitudes
- Jitter: RJ, DJ, DCD, TJ
- Transmitter output waveform
- Differential and common mode S-parameter
- Differential to common mode conversion loss



*Recommended HW configuration:
86100D/ETR/GPI/200/201/300/SIM
86108B/232/HBW
(other configurations supported)*

DCA Application References

- Compatibility: FlexDCA Revision A.02.00 or higher running on 86100D mainframe
- Web Site: www.agilent.com/find/N1012A, www.agilent.com/find/N1014A, www.agilent.com/find/N1081A
- Datasheets:
 - [OIF CEI 3.0 Compliance Test Application for 86100D DCA-X](#)
(Agilent literature # 5991-0561EN)
 - [SFF-8431 Compliance and Debug Application for 86100D DCA-X](#)
(Agilent literature # 5991-1296EN)
 - IEEE 802.3 Compliance and Debug Application for 86100D DCA-X
(Agilent literature # 5991-2877EN)
- Pricing (US):

N1012A OIF-CEI Compliance Application	\$9.5K
N1014A-HST SFF-8431 Host Compliance Suite	\$5.5K
N1014A-MOD SFF-8431 Module Compliance Suite	\$4.0K
N108x-series IEEE 802.3 Compliance Applications	\$6 to 8K
N5452A Remote Programming Interface	\$1.2K

N1010A FlexDCA and 86100D DCA-X upgrades to the latest revision are available free of charge from www.agilent.com/find/N1010A and www.agilent.com/find/86100D

External Clock Recovery

Applications

- Next generation data links

Block Diagram

- Electrical versus optical CDR

Performance

- Data rates, loop BW, etc.

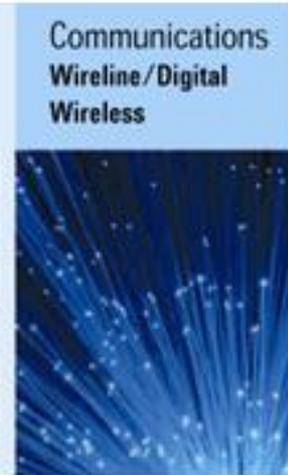
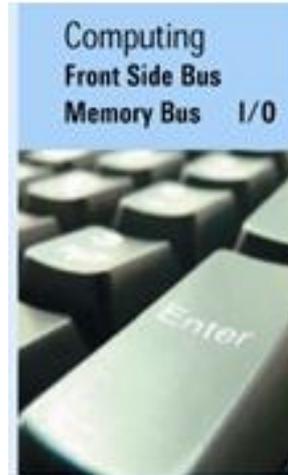
References

- Website, application notes, etc.

Applications

Physical layer characterization and validation engineers in the computer, enterprise and communications market

Primarily R&D, less manufacturing

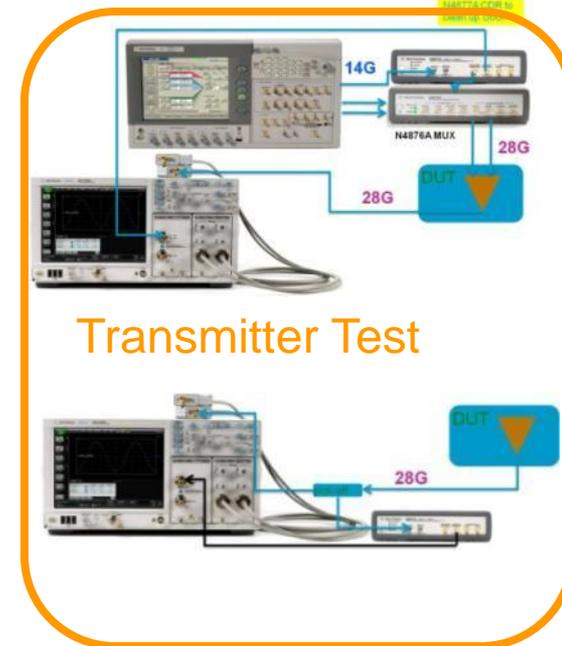
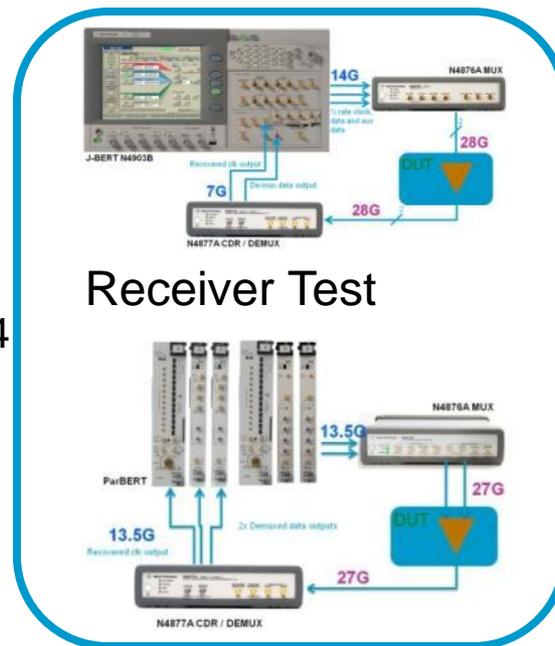


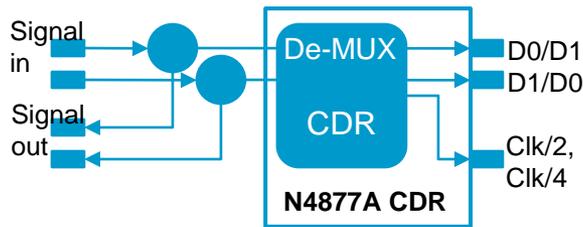
>16Gb/s

- 100GbE
- FCx32
- OIF CEI25/28
- Infiniband
- SERDES

≤16Gb/s

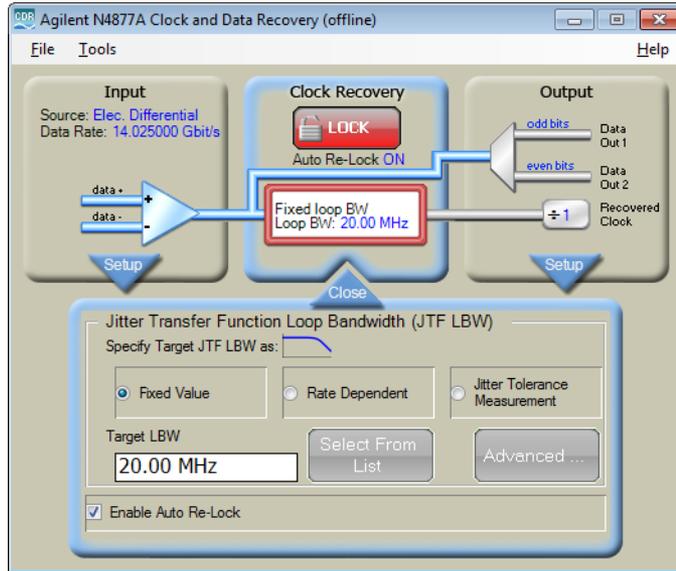
- SAS 12G
- SATA I, II, III
- PCIe gen 1,2,3, 4
- USB 3
- FCx16





Clock recovery instrument and demultiplexer

- Operates from 50Mb/s to 32Gb/s
- Lower cost 16.5Gb/s version available
- Tunable loop bandwidth and adjustable peaking
- Built-in demultiplexer generates subrate data streams
- Clock and auxiliary clock output with residual jitter as low as 100fs rms
- Sensitive data input for small signals
- Easy to use graphical user interface via USB connection to a PC

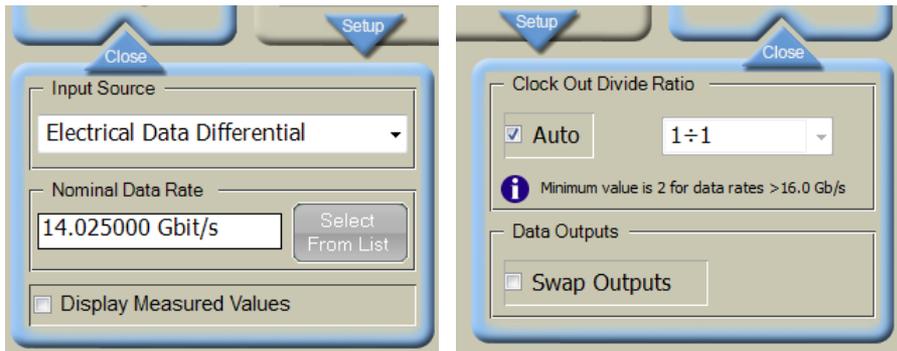


Intuitive Operation

- Adjustable loop bandwidth up to 20MHz and selectable peaking for golden transfer characteristics
- Single ended and differential data input
- User defineable clock divide stages for trigger signals

Special Receiver Test Support

- Swapable demux outputs to simplify >12.5Gb/s receiver testing with Agilent BERTs
- Jitter tolerance test mode



N1075A Optical-to-Electrical Converter

Provides an optical coupler to pick off optical energy and an O/E convertor to create an electrical signal for the N4877A CDR

- S32: Single-mode up to 32 Gbps
- M14: Multimode up to 16 Gbps



- Compatibility: Windows XP, Windows 7 or Windows 10
(user interface runs on PC/laptop, DCA-X or J-BERT)
- Web Site: www.agilent.com/find/CDR
- Brochure: [Clock Recovery Solutions to 32 Gb/s](#) (Agilent lit. #5990-9933EN)
- CR Theory: Dennis Derickson, Markus Müller: *Digital Communications Test and Measurement*, Chapter 9; Prentice Hall, 2008 (ISBN 0-13-220910-1)
- Pricing (US):

N4877A-232 Electrical CDR up to 32 Gb/s	\$52K
N4877A-216 Electrical CDR up to 16 Gb/s	\$33K
N1075A-S32 Single-mode O/E up to 32 Gb/s	\$18K
N1075A-M14 Multimode O/E up to 16 Gb/s	\$18K
N1070A Bundle Discount (N4877A + N1075A pair)	(\$5K)
N1027A-S32 or -M14 Delay matching fibers & cables	\$5K

UDA & SCPI Tools

SCPI Recorder

- Push buttons, record commands

Interactive SCPI Command Tree

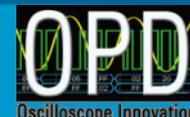
- Explore syntax, parameters

User Defined Application

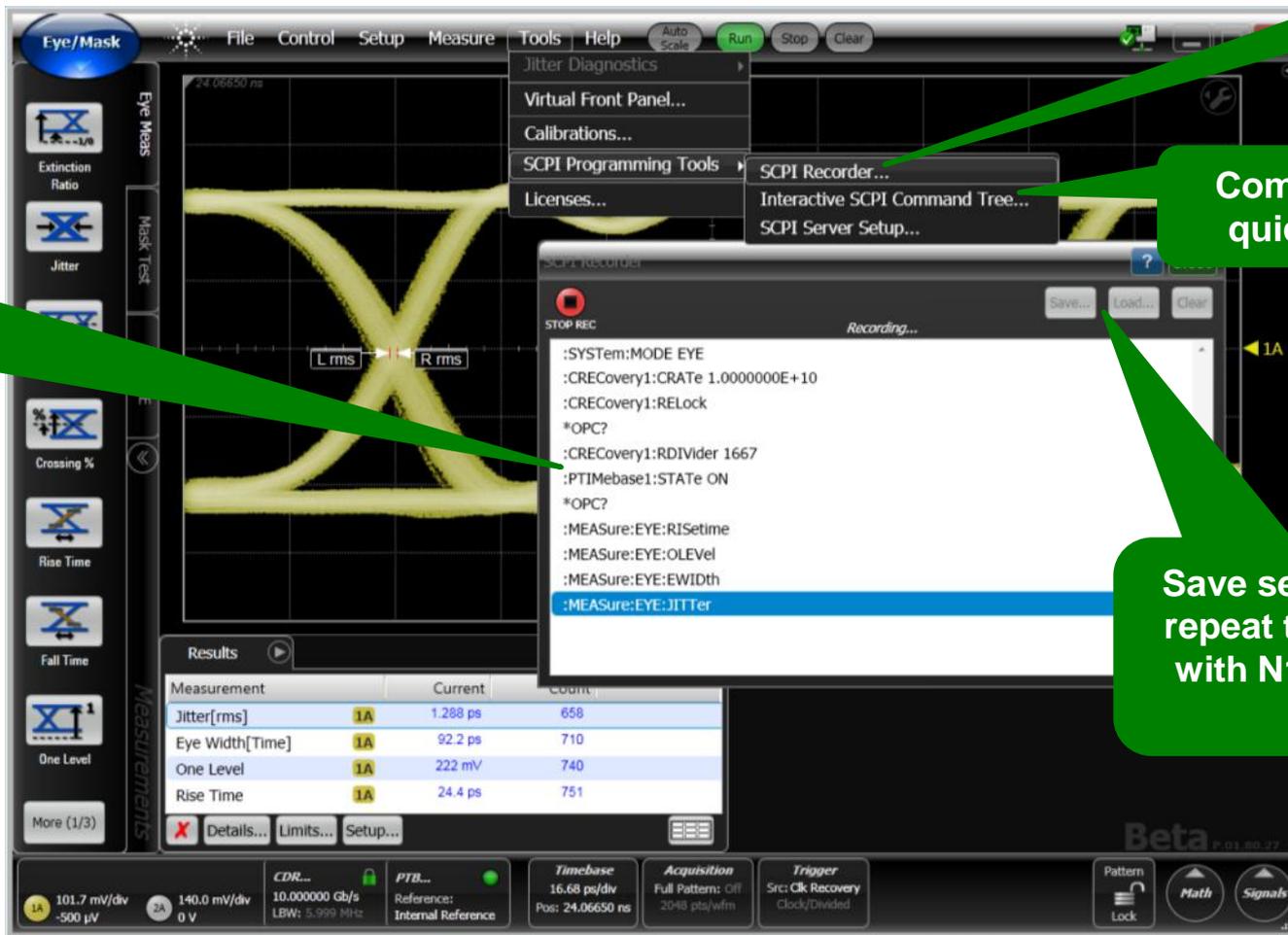
- Same UI as on RT scopes

References

- Website, application notes, etc.



Powerful tool reduces programming time



Record any button push or screen touch

Invoke from menu

Command tree is quick reference

Save sequences to repeat tests or use with N1019A UDA tool

Interactive SCPI Command Tree

Quickly find the right command/query syntax

The SCPI command tree is shown below. (2704 nodes total)
Select a command, then interact with the controls at the bottom:

Node	Full Command Path
[-] :MEASure	
[-] :AMPLitude	
[+] :BERFloor	:MEASure:AMPLitude:BERFloor
[+] :BERLimit	:MEASure:AMPLitude:BERLimit
[+] :DEFine	
[+] :DEPCie	:MEASure:AMPLitude:DEPCie
[+] :DIONes	:MEASure:AMPLitude:DIONes
[+] :DIZeros	:MEASure:AMPLitude:DIZeros
[-] :EOPening	
:LOCation	:MEASure:AMPLitude:EOPening:LOCation?
:SOURce1 SOURce	:MEASure:AMPLitude:EOPening:SOURce1
[+] :STATus	:MEASure:AMPLitude:EOPening:STATus?
[+] :HONE	:MEASure:AMPLitude:HONE
HZERo	:MEASure:AMPLitude:HZERo

Selected Command:
:MEASure:AMPLitude:EOPening:SOURce1 [dropdown]
:MEASure:AMPLitude:EOPening:SOURce1?

Run [?] Query

Run/Query Output

Complete coverage of SCPI commands

Enter numerical or other parameters

Instantly execute a command

Link to description in online help

Instantly query a result

N1019A User Defined Application for 86100D

Quickly build your own applications

Create groups of tests

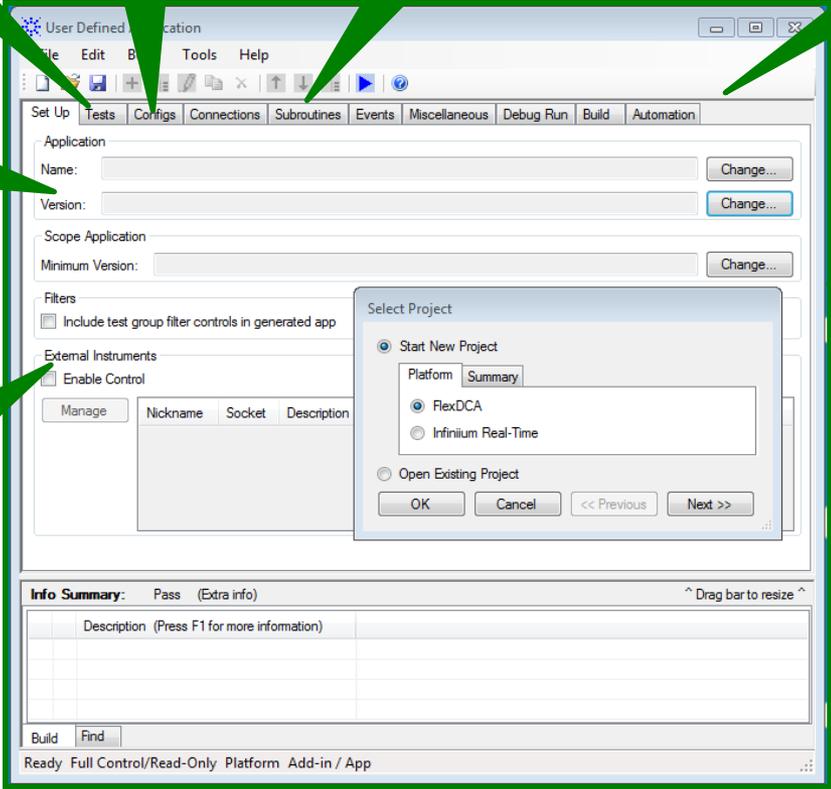
Configure test conditions

Streamline repetitive tasks

Obtain results tested to limits and reports

Quickly generate automated applications

Interface with external equipment such as SA, VNA, CDR

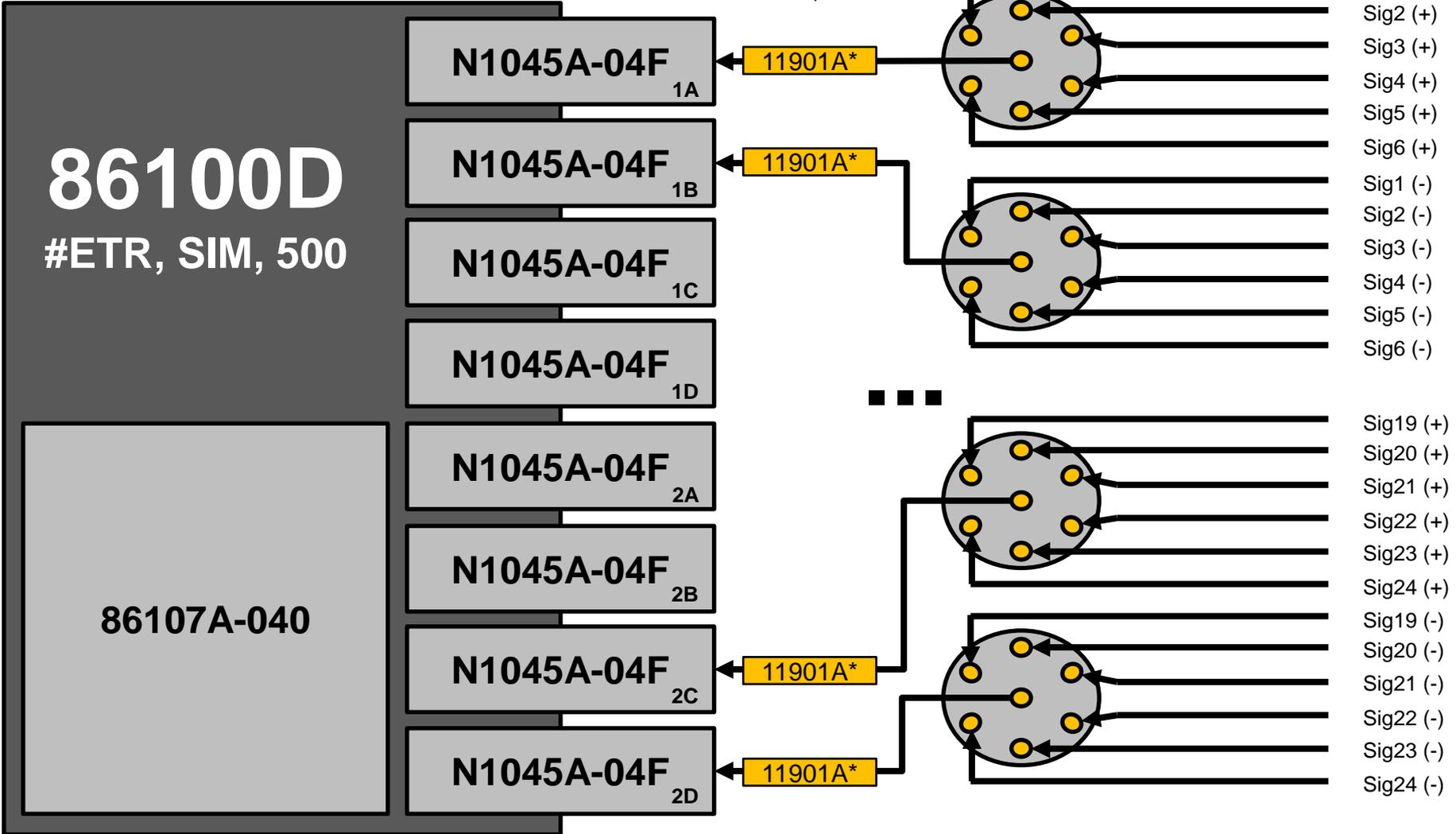


Run on 86100D or on a PC

Same functionality and appearance as N5467A for RT scopes

Test Automation – 24 Differential Channels

3.5/2.92 mm Switches: 8x 87106C (26 GHz) or 87106D (40 GHz)
 Switch Controller Unit: 1x L4491A



- Compatibility: FlexDCA Revision A.01.80 or higher
86100D mainframe
- Remote Control Documentation (FlexDCA): See “Programming“ in the Online Help of FlexDCA
*Install the **free** version of FlexDCA on your PC/laptop from www.agilent.com/find/flexdca_express :
Open FlexDCA Express in simulation mode, then click “Help, Contents”, or use the SCPI tools.*
- SCPI Tools (FlexDCA firmware upgrade – download from www.agilent.com) **FREE**
- UDA URL: www.agilent.com/find/N1019A
- UDA Data Sheet: [User Defined Application For 86100D DCA-X](#)
(Agilent literature # 5991-0572EN)
- UDA Pricing (US): N1019A (requires FlexDCA revision **A.01.80** or higher) \$3.6K
N5452A [Remote Programming Interface](#) \$1.2K

Productivity Package

Applications

- Optical transceiver manufacturing

Block Diagram

- Rapid eye: 100% sampling efficiency

Performance

- 2X to 5X more DUTs tested per hour

References

- Website, application notes, etc.

Speed

- Increase throughput by testing more efficiently

Smart

- Increase throughput by testing smarter

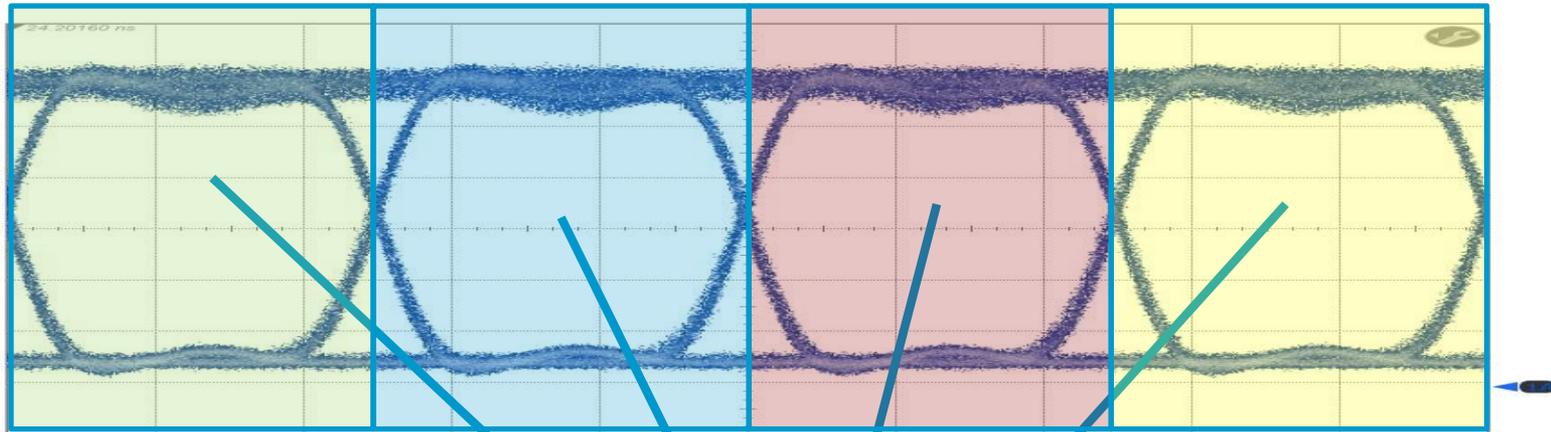
Parallel

- Test more devices with one mainframe

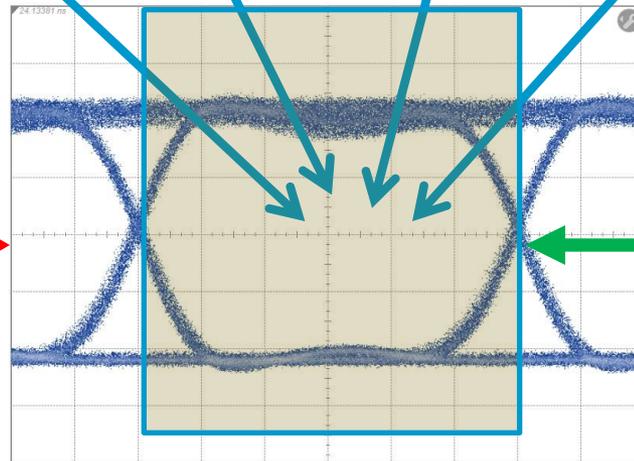


Increase Test Efficiency

HW acquires four or more UIs (important when using sub-rate triggering)



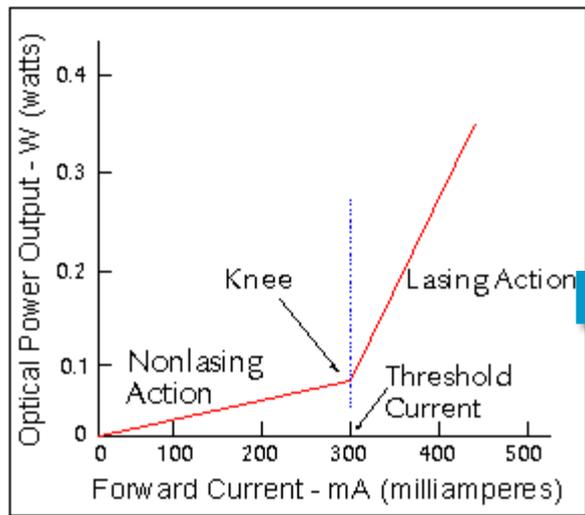
Classic method: 38% of HW samples not used, except for mask alignment



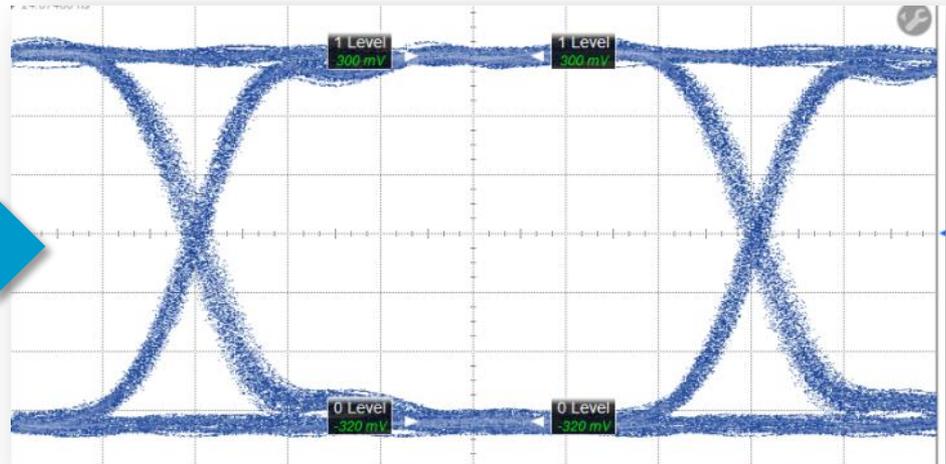
Productivity package: 100% of HW samples mapped into the eye and used for measurements

Fast Eye Tuning Mode

Quickly determine ideal bias conditions for an optimum eye



injection-laser diode: output vs. input current

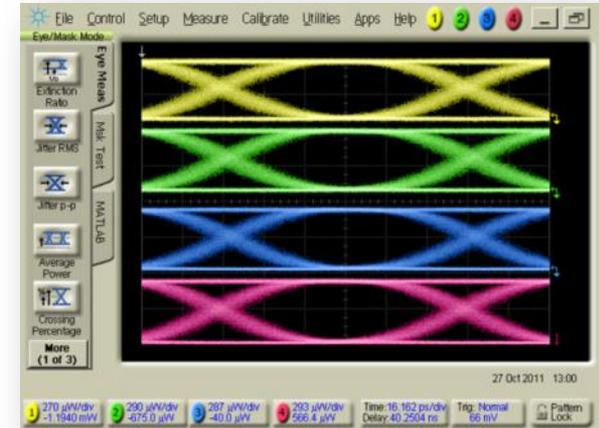
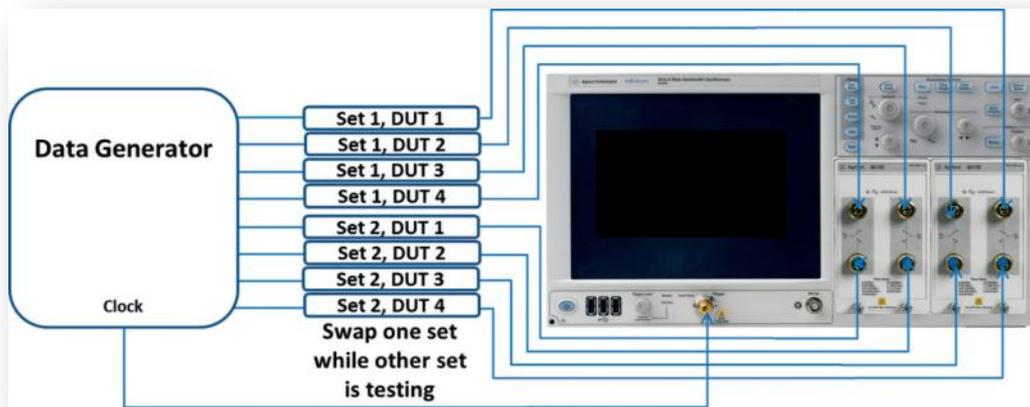


Multiple Channel Systems

86115D provides up to 8 test ports for a single mainframe

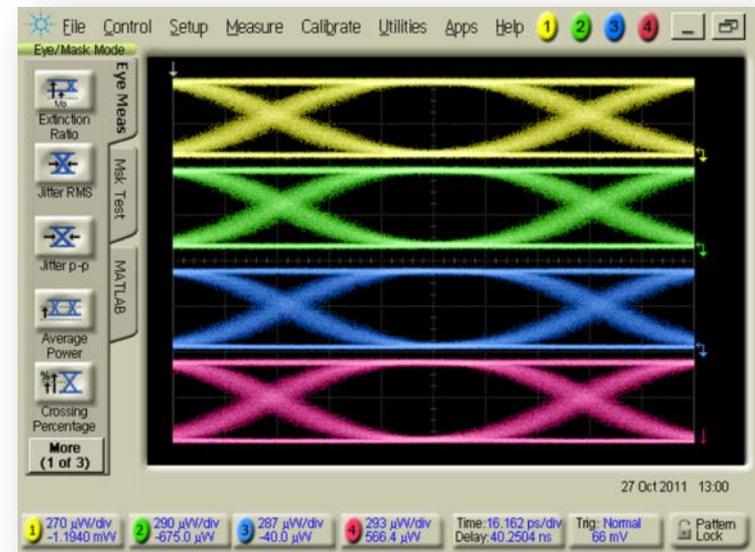
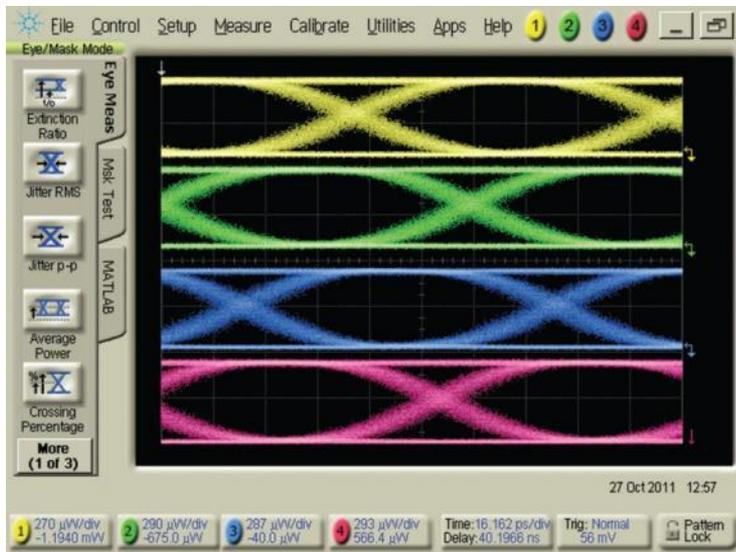
- Test many single channel DUTs
- Test DUTs with multiple outputs

NO throughput reduction when testing several channels

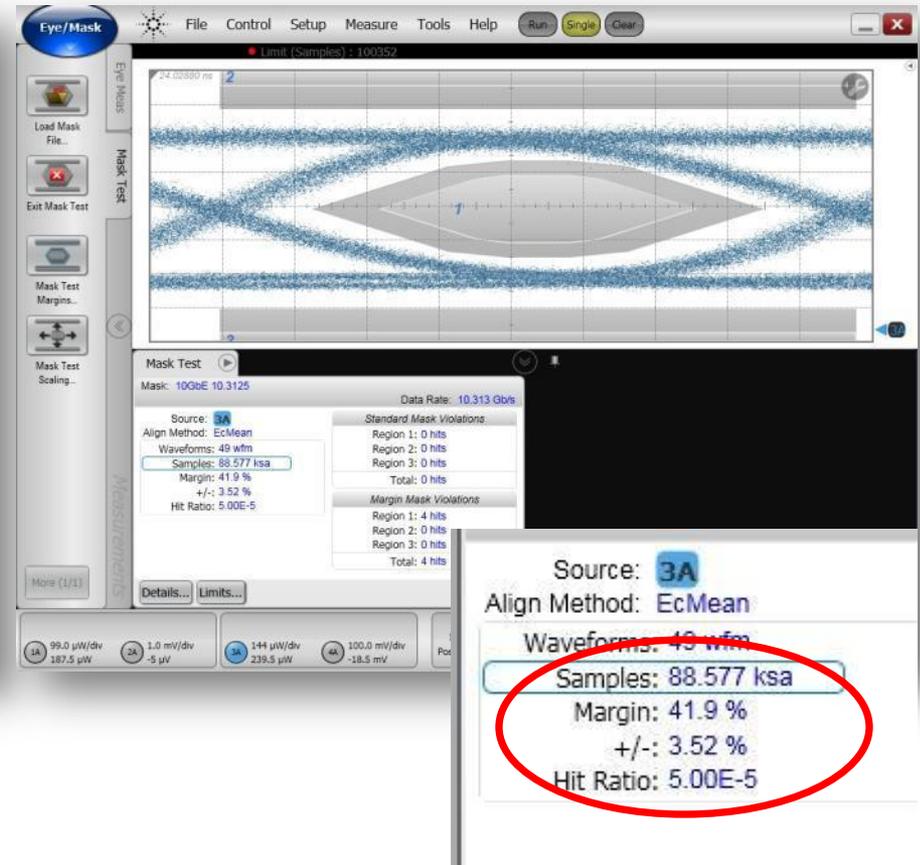
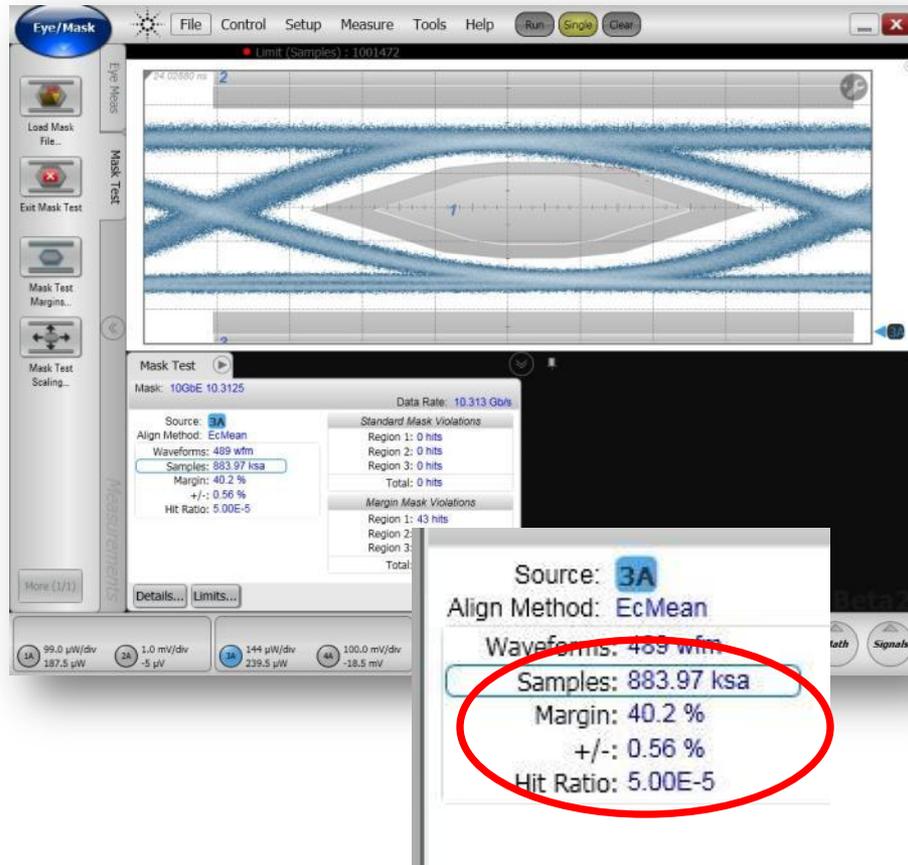


Faster Autoscale (up to 3X)

- Takes advantage of Rapid Eye and known bit rate
- Optimally aligns eye diagrams when testing multiple channels
 - No throughput reduction even when channels are skewed



Mask Margin Uncertainty Metric



- Only need to acquire enough data to meet margin accuracy limits
- Potential to reduce test times by 80%

- Compatibility: 86100D (full), 86100C (most features)
- Web Site: www.agilent.com/find/dcax
- Video: <http://www.youtube.com/watch?v=ZKQ-4tvhSv4>
- Application note: [Techniques to Reduce Manufacturing Cost-of-Test of Optical Transmitters](#) (Agilent literature # 5990-9609EN),
- Pricing (US):

Productivity Package	
86100D-500	\$664 (new)
86100DU-500	\$664 (upgrade)



The image shows the cover of an application note. At the top left is a blue starburst logo. To its right is the title 'Techniques to Reduce Manufacturing Cost-of-Test of Optical Transmitters, Flex DCA Interface' and the subtitle 'Application Note'. Below the title is a circular inset image showing an oscilloscope screen with colorful waveforms. At the bottom left is the word 'Introduction' and at the bottom right is a short paragraph of text.

Techniques to Reduce Manufacturing Cost-of-Test of Optical Transmitters, Flex DCA Interface

Application Note

Introduction

Manufacturers of optical transceivers are faced with increasing challenges to their businesses, particularly how to reduce product costs. Pressures to reduce costs as data rates rise means manufacturing engineering managers and their

System Impulse Response Correction

Applications

- New data rates not covered by HW

Freq. Response

- De-embeds its own hardware

Performance

- Eye diagrams

References

- Website, application notes, etc.

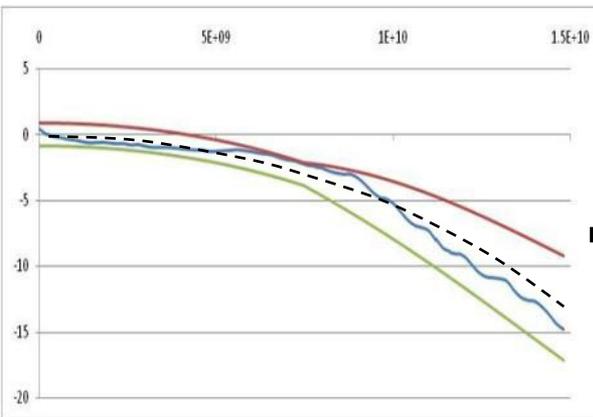
- Usually oscilloscope based to verify transmitter performance
- Primary goal: consistency of eye diagram measurements
- System frequency response defined by standards
 - Practically all use 4-th order Bessel-Thomson low-pass behavior
 - Many standards also define tolerance bands
- Typical 3-dB_{ele.} bandwidth = 0.75 * data rate
 - Too much bandwidth increases noise, captures relaxation oscillations
 - Too little bandwidth causes inter-symbol interference
- Eye diagram results are:
 - Insensitive to small variations of the *3-dB bandwidth****
 - Sensitive to small variations in the *shape* of the frequency response

*** Allows standards share a receiver:

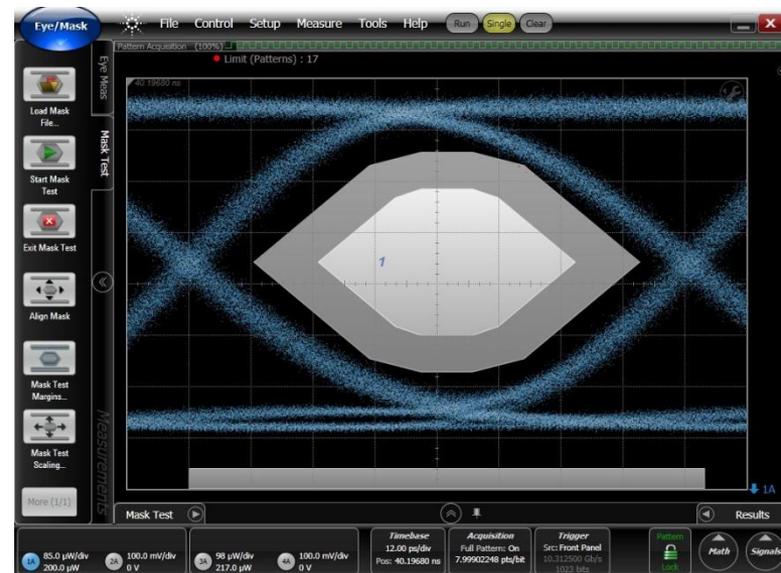
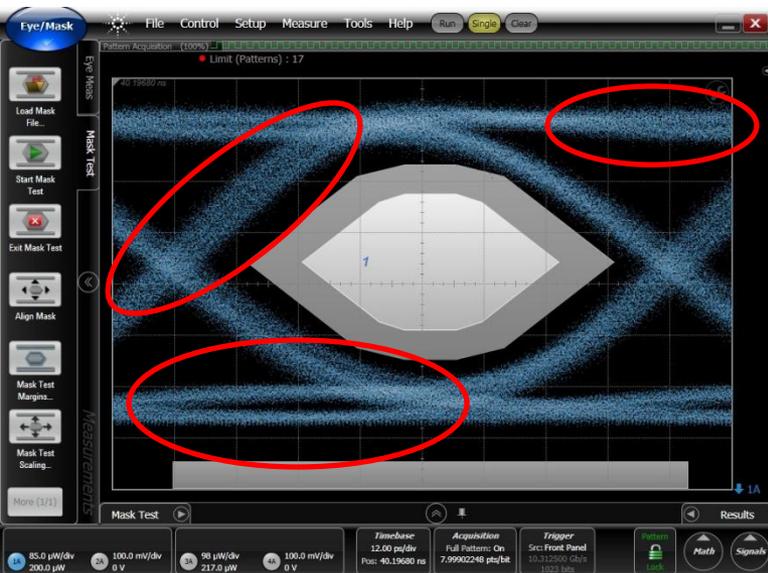
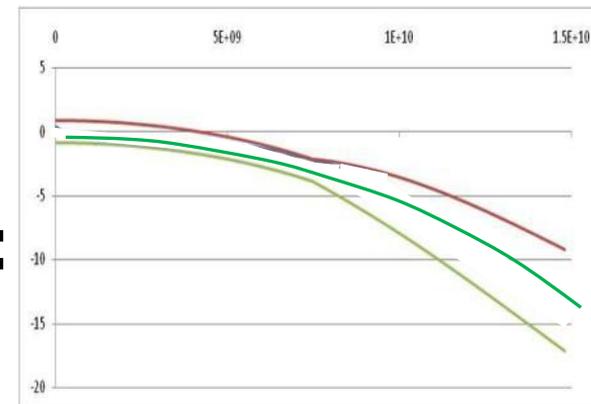
STM-64/OC-192 (9.953 GBaud), 10 GbE (10.3125 GBaud) and 8G FC (8.5 GBaud) all use 7.5 GHz bandwidth



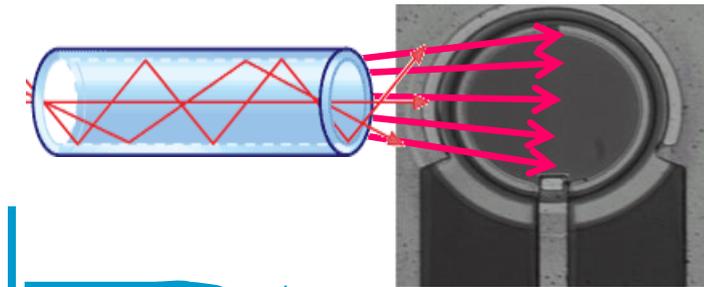
System Impulse Response Correction (SICR)



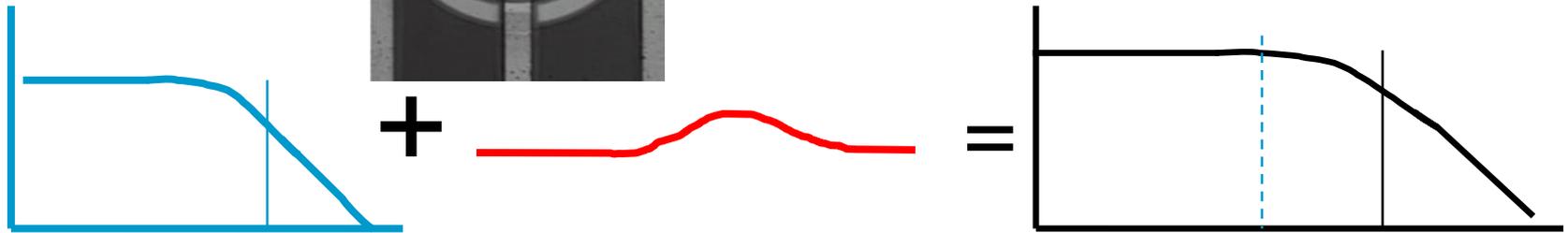
HW tolerances tightened to ideal behavior



System Impulse Response Correction (SIRC)

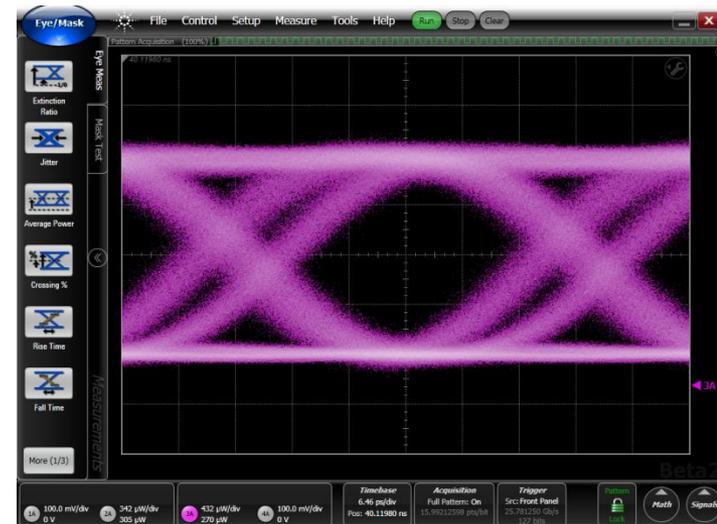
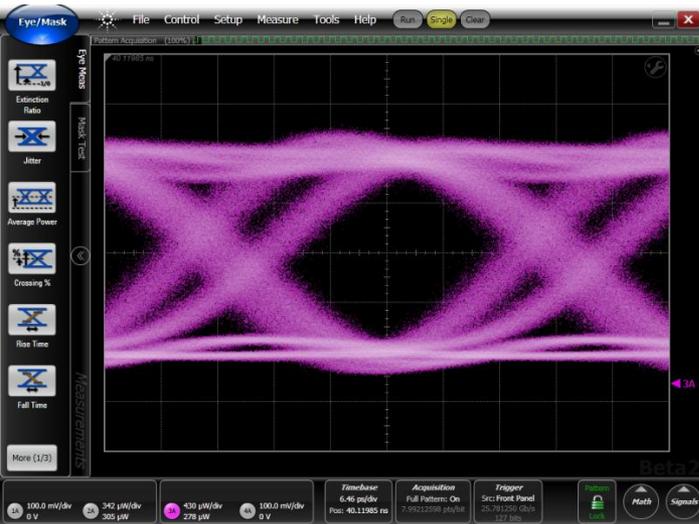


Bandwidth transformation to cover new data rates

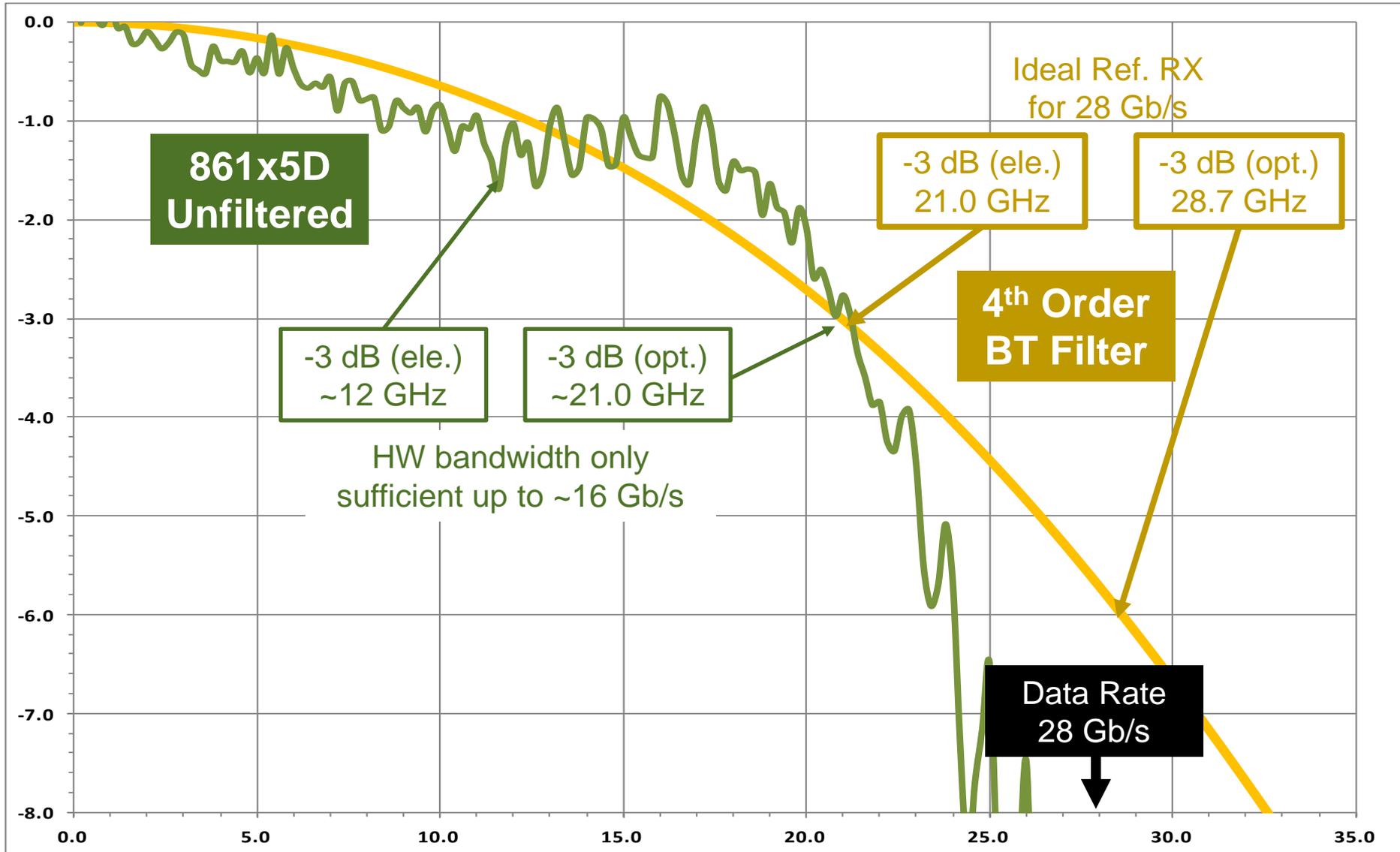


HW BW

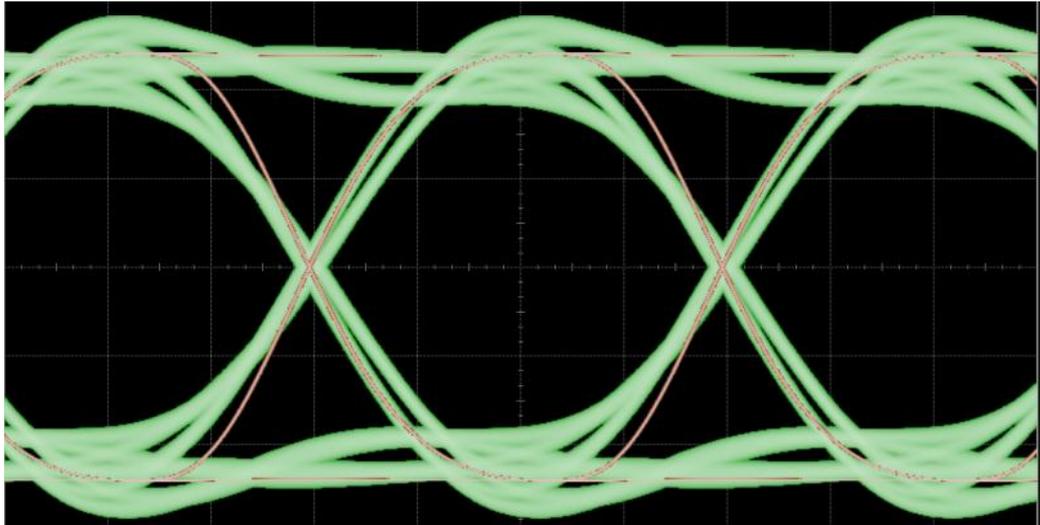
HW BW + SIRC



Optical Vs. Electrical Bandwidth

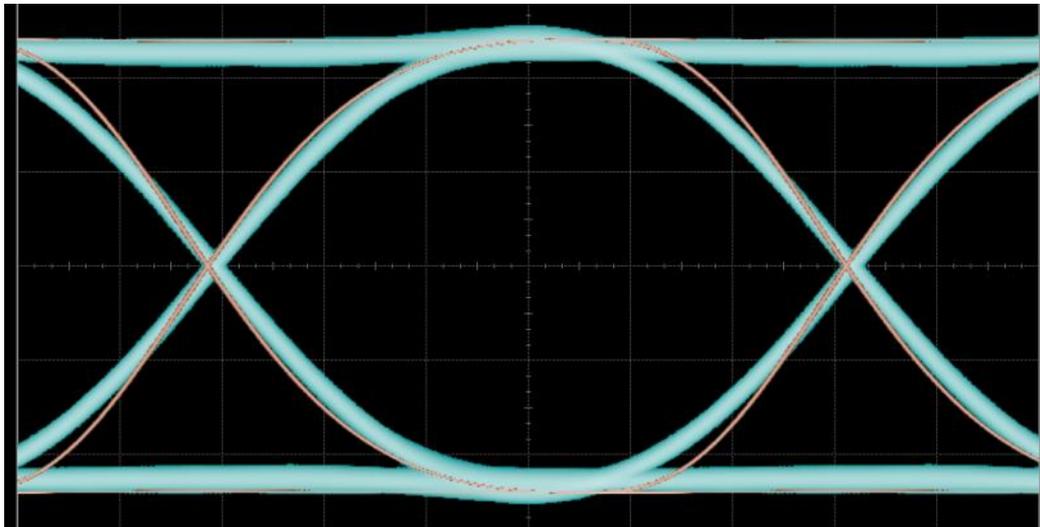


Actual Versus Theoretical Eye – 28 Gb/s



Orange: BT4
(ideal result)

Green: BW
Unfiltered 861x5D



Orange: BT4
(ideal result)

Blue: SIRC
applied to 861x5D

- Compatibility: 86105C, 86105D, 86115D, 86116C
- Web Site: <http://www.agilent.com/about/newsroom/presrel/2011/27jun-em11076.html>
- Application note: [Techniques for Higher Accuracy Optical Measurements](#)
(Agilent literature # 5990-8812EN)

- Pricing (US):

86105C-IRC	\$6K
86105D-IRC	\$6K
86115D-IRC	\$12K
86116C-IRC	\$12K

IRC upgrades have an additional service center charge (5% - 10%)

Signal Processing & De-Embedding

Applications

- Fixtures for 10 to 40 Gb/s designs

Signal Processing

- DFE, CTLE, etc.

Simulation

- Embedding, De-embedding, etc.

References

- Website, application notes, etc.

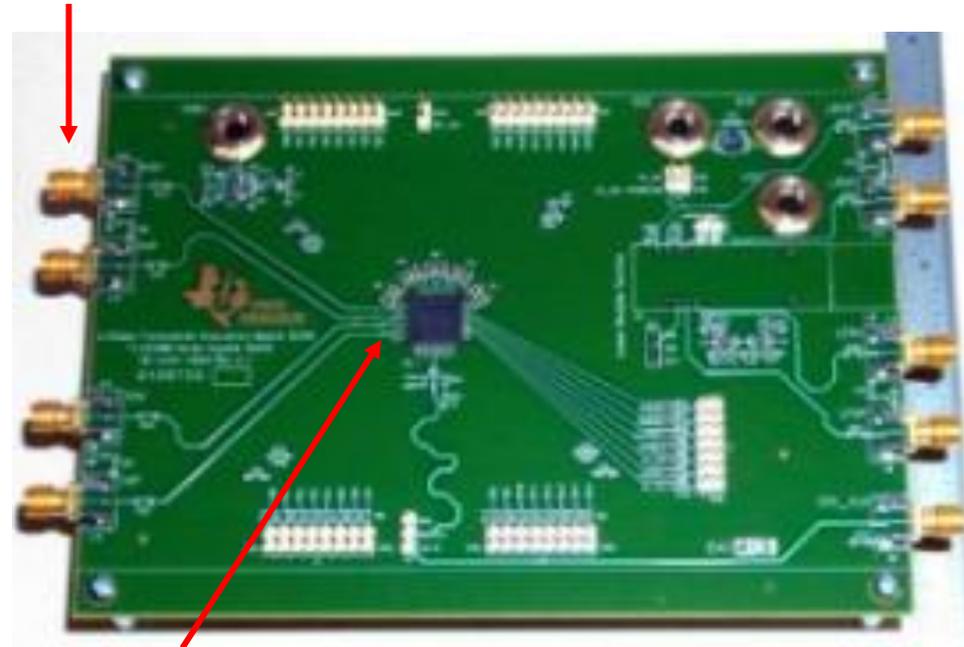
Applications

- 10/100 Gb Ethernet
- 8/16/32 G Fibre Channel
- OC-192, OC-768

- *IC Designers: see what the performance looks like inside your package, at the balls / pins of your IC*

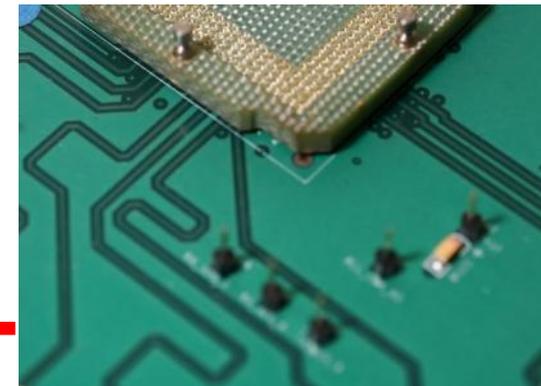
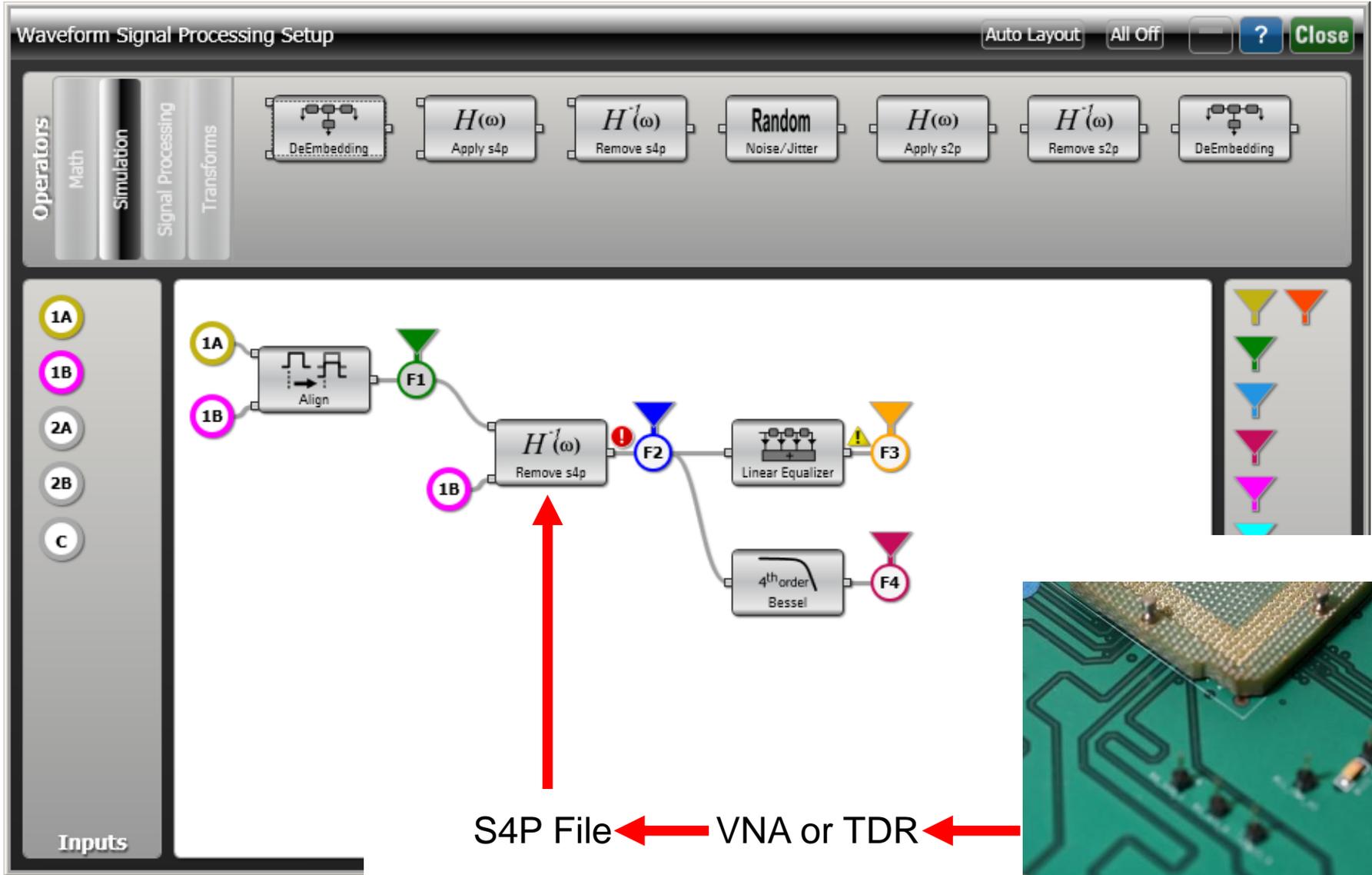
- *Serial Bus Designers: add a 'virtual' cable (e.g. SAS, SATA) or remove fixture effects*

Measure TX performance here (at the connector)



Predict performance here (pins, balls of IC)

Block Diagram



Free Versus Licensed Operators

Operators

- Math: (+) Add, (-) Subtract, (*) Multiply, X^2 Square
- Simulation: Align, Amplify
- Signal Processing: $X(t+\tau)$ Delay, \bar{X} Average, \tilde{X} Median, Max(x) Maximum, Min(x) Minimum
- Transforms: $-(X)$ Invert, $|X|$ Absolute Value

SIM

Operators

- Math: DeEmbedding
- Simulation: $H(\omega)$ Apply s4p, $H^*(\omega)$ Remove s4p, Random Noise/Jitter, $H(\omega)$ Apply s2p, $H^*(\omega)$ Remove s2p, DeEmbedding
- Signal Processing: (None)
- Transforms: (None)

201

Operators

- Math: $x(n) - x(n-1)$ Difference, CTLE
- Simulation: $\sum^n X$ Summation, Linear Equalizer, DFE
- Signal Processing: 4th order Bessel, Butterworth, Gaussian, Sin(x)/x
- Transforms: $\uparrow n$ Interpolation

Operators

- Math: VS. Versus
- Simulation: $\mathcal{F}(x)$ FFT
- Signal Processing: (None)
- Transforms: (None)

- Compatibility: 86100D Mainframe or 86100DU FlexDCA Software
DCA must have the extended trigger hardware

- Web Site: www.agilent.com/find/flexdca

- Free version: www.agilent.com/find/flexdca_express
(oscilloscope & eye mask modes, built-in simulator, waveform viewer)

- Videos: <http://www.youtube.com/watch?v=YMxIJ6ccJoo> (de-embedding)
<http://www.youtube.com/watch?v=Jk5JeJ7ZBNE> (installation, trial licenses)

- Pricing (US):

86100DU-201 Advanced Waveform Analysis	\$4.7K
86100DU-SIM Waveform Transformation SW	\$5.6K
N1010AU-201 Advanced Waveform Analysis	\$4.7K
N1010AU-SIM Waveform Transformation SW Upgrade	\$5.6K

Upgrades to the latest revision are available free of charge from
www.agilent.com/find/N1010A and www.agilent.com/find/86100D

ESD/EOS - #1 failure mechanism:

- ALWAYS apply good **ESD safety practices**
- **Turn off** all power supplies, **discharge** even small capacitors, coax cables

OVER-TORQUE - #2 failure mechanism:

- 1.85 / 2.4 mm connectors: **0.57 nm** (5 lbs-in) – use torque wrench 8710-1582
- 3.5 mm connectors: **0.9 nm** (8 lbs-in) – use torque wrench 8710-1765
- Bulkheads: **0.9 nm** (8 lbs-in) – use torque wrench 8710-1764

OPTICAL SPIKE - #3 failure mechanism:

- Optical amplifiers send out a destructive optical power spike if they are turned on improperly.
Idling EDFAs are a big pool of energy waiting for just a few photons to release it!
- Always turn on the **signal first, then the optical amplifier.**
Or use a variable optical attenuator (> 40 dB) or shutter

GENERAL:

- When finished **re-install all caps, adapters and input/connector protection.**
- Use a **front cover** during transportation
- Use N9355CK01 DC coupled **limiters** on TDR or electrical channels
- Return **mouse and keyboard!** We spend too much each year buying replacements



Qty 2 N9355CK01



N1000-40008 fits DCA-X