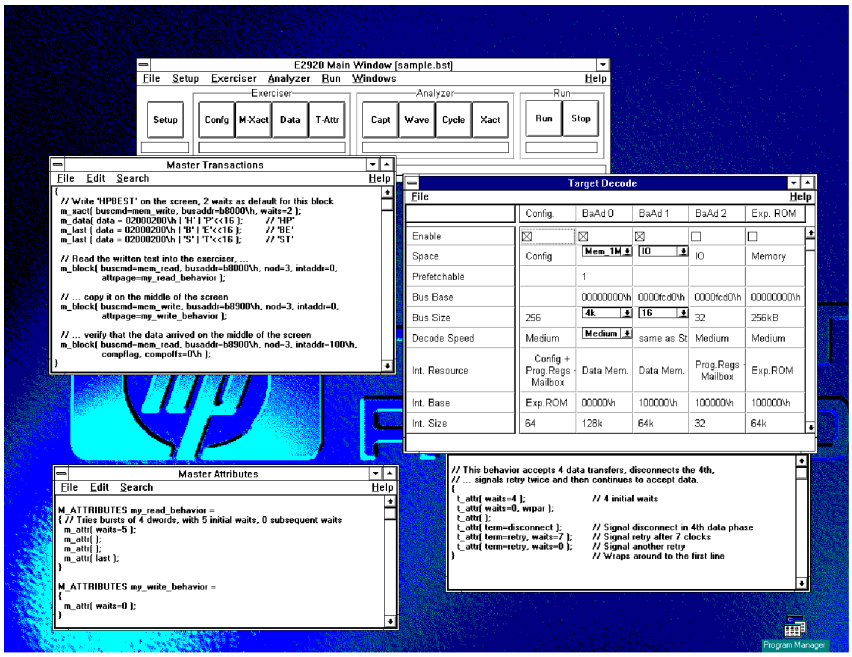
HP E2971A PCI Exerciser Graphical User Interface for Windows 95/NT

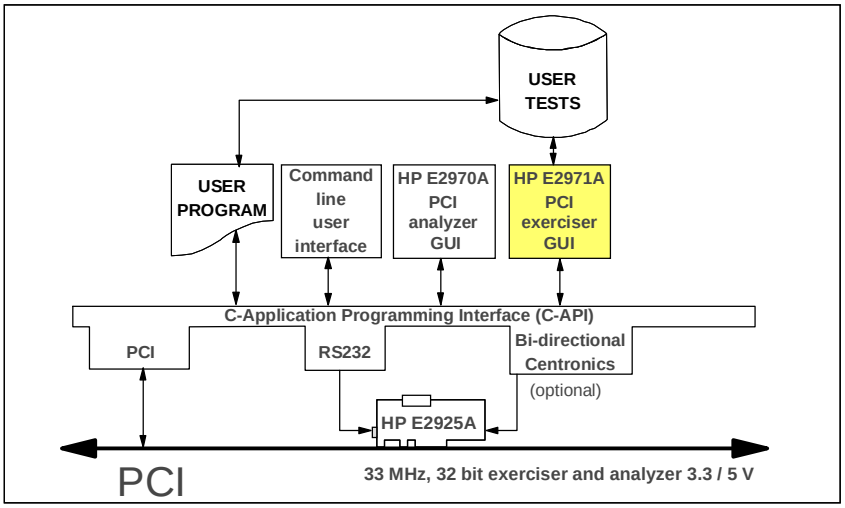
Technical Specifications

HP E2971A PCI Exerciser Graphical User Interface for HP E2925A PCI Exerciser and Analyzer Card

Key Features

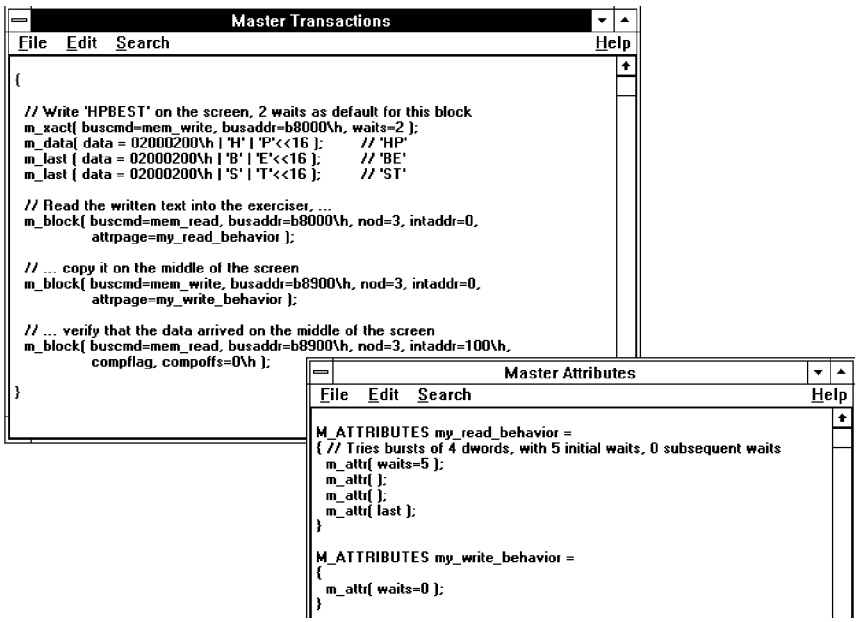
- PCI bus transaction language for defining master traffic, protocol behavior and target protocol behavior.
- Master transaction editor to set up linear sequence of master transactions. High level block transfer commands can be mixed with low level per data phase commands.
- Master attribute editor to define protocol behavior sets for block transfer commands.
- Target attribute editor to set up protocol behavior for target.
- Configuration editor to set up/ view PCI configuration space.
- Data memory editor to view/modify on-board memory content.





HP E2920 Computer verification tools, PCI series

Part of the HP E2920 Computer verification tools, PCI series, the HP E2971A PCI exerciser graphical user interface provides a comprehensive Windows 95/NT interface for the HP E2925A's PCI exerciser. Use it to set up the programmable master and target. It runs on an external PC connected via RS232 (or via bi-directional Centronics using the HP E2925A option 002), or on the system-under-test itself accessing the card via PCI.



PCI Bus Transaction Description Language (BTDL)

The BTDL gives you complete control over the traffic and protocol behavior of the exerciser. Optional parameters minimize your programming effort.

Master Transaction Editor

Use the transaction editor to set up a linear sequence of bus transactions. High level block transfer commands and low level per data phase commands can be mixed to let you choose the right level of abstraction or detail.

Block transfer command

This facilitates the movement of large blocks of data. Optionally, the underlying protocol can be specified in the master attribute editor.

Block parameter	Description
busaddr	Start address on bus
buscmd	PCI command used
byten	C/BE[] in data phases
nod	Number of transferred Dwords
intaddr	Address of internal data memory
compflag	Enables data compare
compoffs	Internal address offset of reference data for comparison
attrpage	Pointer to protocol behavior set

Data phase commands

These are optimized for clear and easy control over the protocol behavior. They let you specify protocol attributes and data values per data phase, yet defaults can be set for a whole block transfer.

Protocol attribute	Description
stepmode	Generates four address steps with toggling AD[]
awrpar	Generates wrong PAR in address phase
aperr	Asserts SERR for address phase
lock	Generates exclusive access
relreq	De-asserts REQ#
waits	Inserts 0 to 31 wait cycles
waitmode	Generates data steps with toggling data
dwrpar	Sets wrong PAR in data phase
dperr	Asserts PERR in data phase
dserr	Asserts SERR in data phase
last	Terminates a transaction

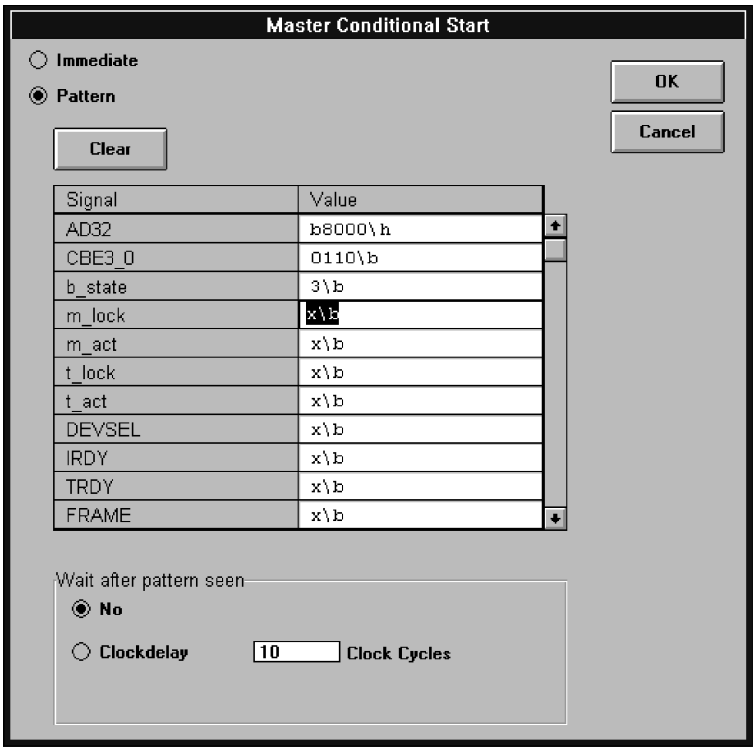
Master Attribute Editor

Use the master attribute editor to set up protocol behavior sets which are used during block transfers. Protocol attributes can be specified per data phase. When the end of a behavior set is reached, it jumps back to the start again.

Master Conditional Start

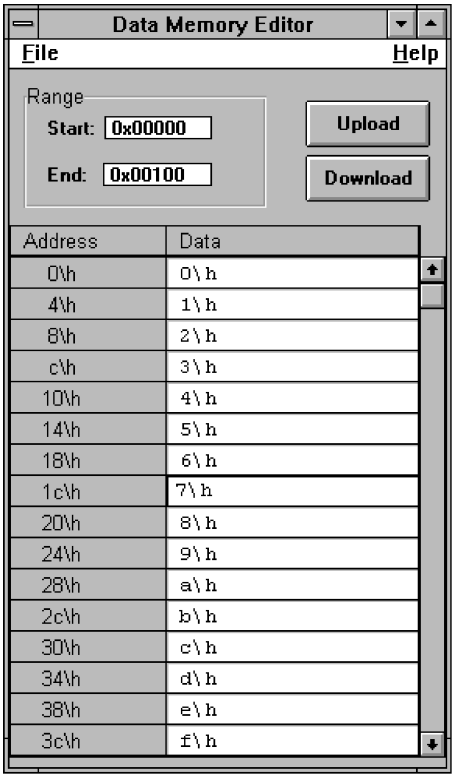
The master conditional start window lets you set up the start conditions for the master traffic. Following a run command, the master can be programmed to start:

- immediately,
- triggered by a pattern,
- delayed additionally by a number of PCI clock cycles.



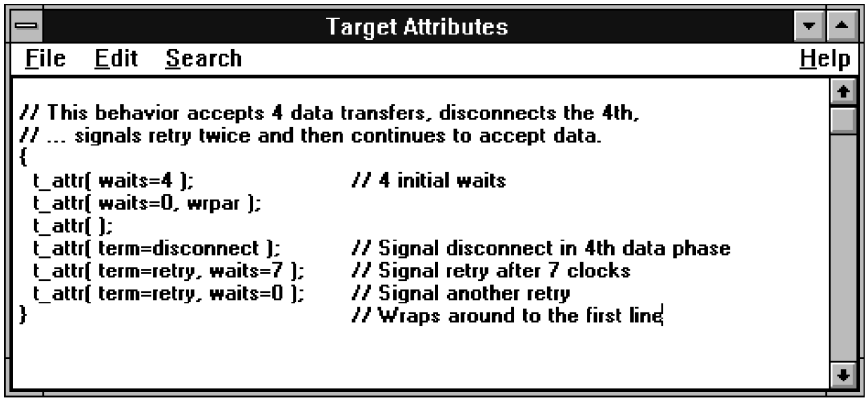
Data Memory Editor

The data memory editor lets you view and modify the contents of the PCI exerciser's on-board memory. This allows you to define the data content for master write transfers or target read accesses to the card, as well as to view the data received from master read transfers or target write accesses. The data can be viewed in hex, binary, decimal, or ASCII formats.



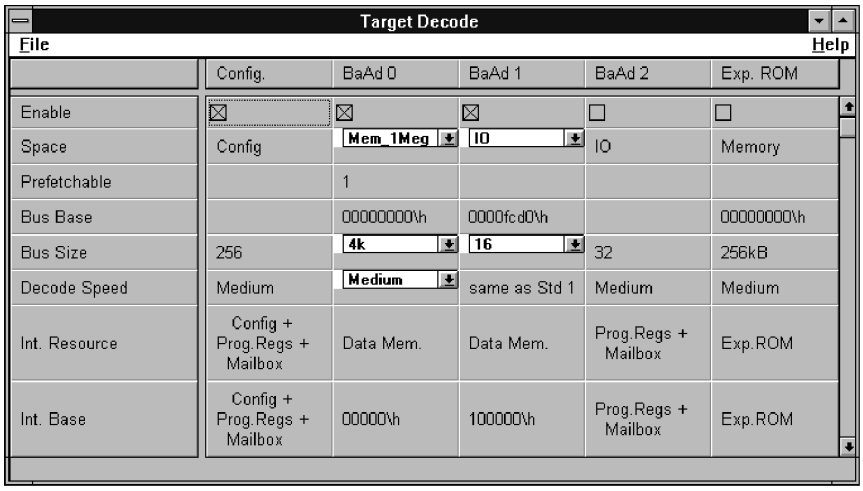
Target Attribute Editor

The target attribute editor lets you define the target's protocol behavior on a phase-by-phase basis. When the target is accessed, the attributes are used sequentially for each data phase. When the end is reached, it jumps back to the start. You can select whether the target should restart with each new transaction, or continue in the linear sequence.



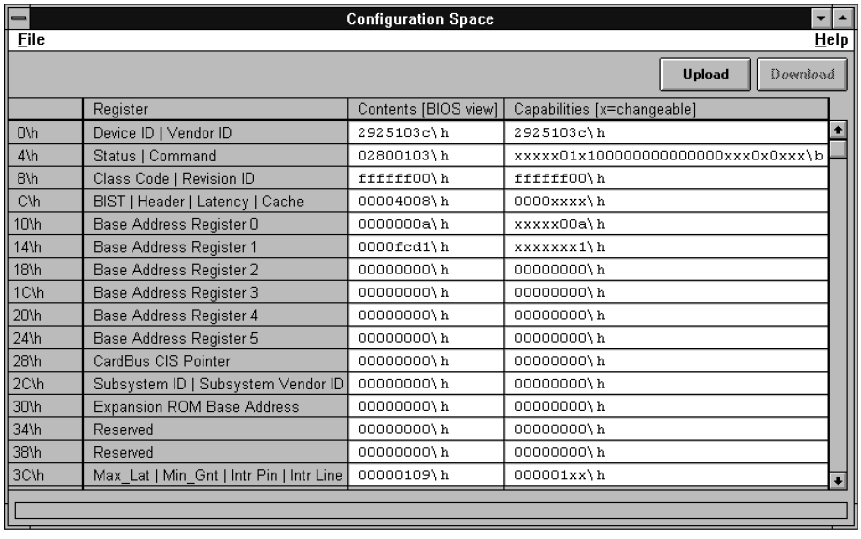
Target Decode Window

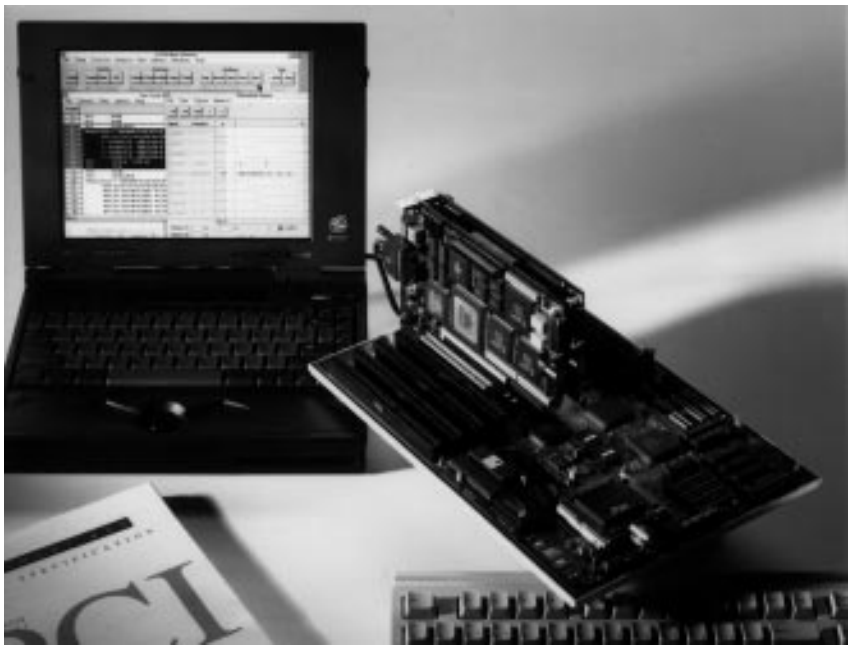
The target decode window lets you configure the target address decoders. As well as configuring the programmable decoders for the exerciser's on-board memory, you can individually enable or disable the decoders for configuration space and expansion ROM.



Configuration Window

The configuration window lets you view and modify the current configuration space settings of the PCI exerciser and analyzer card. You can also store the current settings as defaults, which will then be used following all subsequent power cycles or PCI resets.





HP E2971A PCI exerciser graphical user interface with HP E2925A 32 bit, 33 MHz PCI exerciser and analyzer card

System Requirements

To use the HP E2971A PCI exerciser graphical user interface, you require a PC with the following specifications:

PC: IBM-PC or 100% compatible with recommended minimum 90 MHz Pentium CPU and CD-ROM drive.

Graphics: 800 x 600 required, recommended 1024 x 768 SVGA.

O/S: Windows 95 or Windows NT.

Memory: 16 MB minimum, 24 MB recommended.

Hard disk: minimum 50 MB available disk space required, 100 MB recommended.

Expansion slots: if you want to use the fast host interface option 002 of the PCI exerciser and analyzer card, one ISA slot is required to host the bi-directional Centronics card.

Interfaces: an RS232 port is required, unless you are using the fast host interface option 002 of the PCI exerciser and analyzer card, or accessing the card via PCI. A parallel port is required for the software ID module, supplied with the HP E2925A, to enable the software license.

Ordering Information

The HP E2971A includes:

- License to use the PCI exerciser GUI software with a single PCI exerciser and analyzer card.
- Software media (CD-ROM).

Note that if you want to simultaneously analyze more than one HP E2925A card using a single PC, you require the appropriate number of HP E2971A GUIs running on that PC, as well as sufficient RS232 ports (or HP E2925A option 002) to connect to each card (unless you are connecting via PCI).

Related HP Literature

- HP E2925A 32 bit, 33 MHz PCI exerciser and analyzer, technical specifications, p/n 5965-4724E.
- HP E2970A PCI analyzer graphical user interface for Windows 95/NT, technical specifications, p/n 5965-4726E.

For more information:
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