HEWLETT PACKARD

HP 64700 Series Emulators for Hitachi H8/500 Family Microprocessors

Technical Data

Design, debug, and integrate real-time embedded systems

Hewlett-Packard has an array of solutions for transparent emulation and analysis for the Hitachi H8/532, H8/520, H8/534/536, and H8/510 microprocessors. The emulators run at speeds up to 10 MHz and can include up to 1 Mbyte of emulation memory.

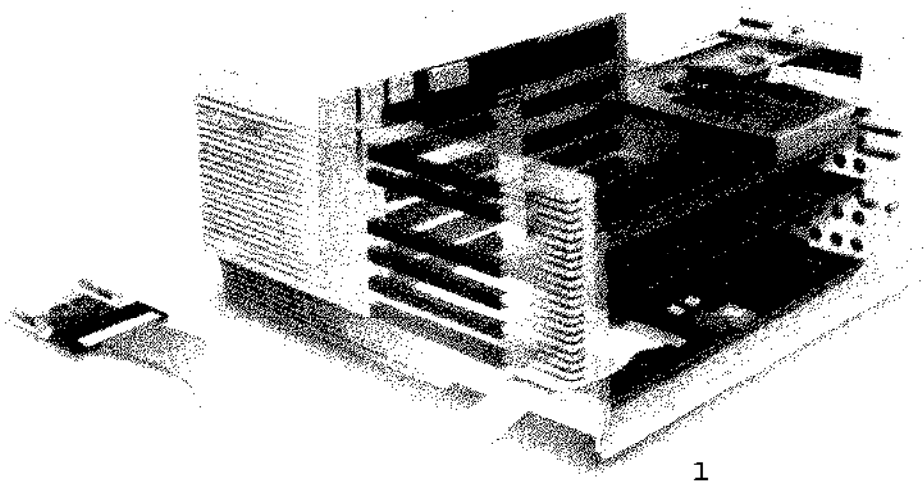
HP's host-independent emulation and analysis systems can be controlled from a simple terminal, HP 9000 workstations, and IBM PC compatibles. Access to these systems is via a selection of user interfaces, including an X-11-window-based interface for HP workstations. This allows several emulation and analysis windows to be opened for simultaneous display during a session, providing an engineer with visibility on several parameters at once.

Hitachi Microprocessor	HP Emulator	Probe	Memory (bytes)
H8/532	64737F	84-pin PLCC	8-bit; 128K
H8/520	64738F	68-pin PLCC or 64-pin SDIP	8-bit; 128K
H8/534/536	64739A	84-pin PLCC	8-bit; 128K
H8/510	64732A	112-pin QFP	16-bit; 128K, 512K, or 1M

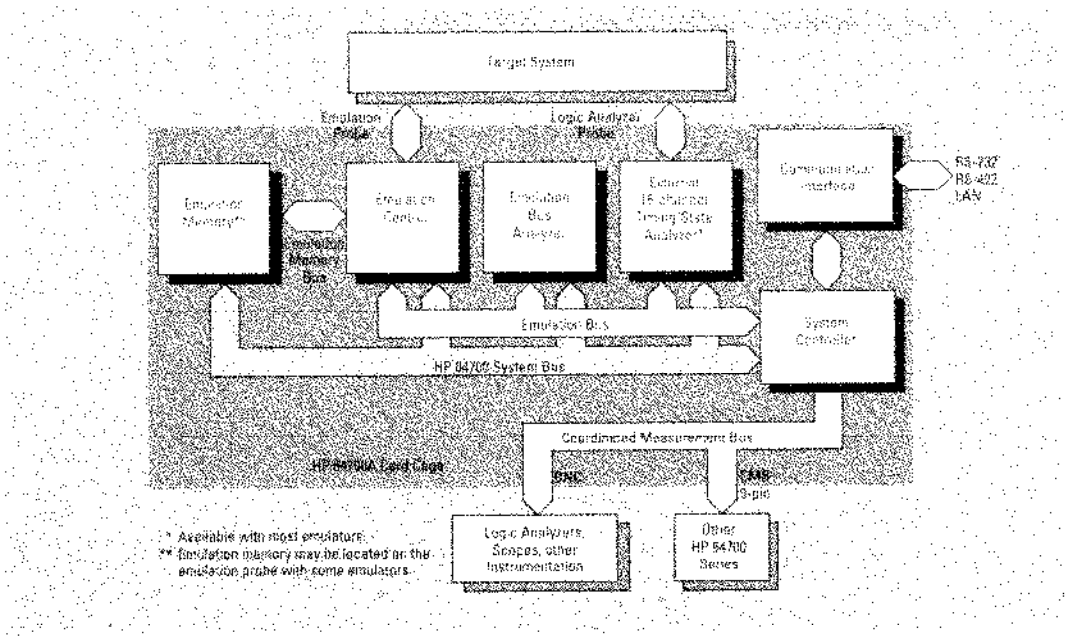
Summary of HP emulators for Hitachi H8/500 family of microprocessors.

The HP 64700A card cage is the foundation in configuring a system to meet specific needs. A host computer can communicate with the card cage via LAN, RS-232-C, or RS-422, allowing HP development tools to function in a variety of design environments. Passive emulation probes support non-intrusive, electrically transparent, easy plug-in to all Hitachi H8/500 family microprocessors.

HP emulation and analysis systems for the Hitachi H8/500 family microprocessors offer a complete feature set for emulation, emulation bus analysis, and emulation memory. These include a coordinated measurement bus (CMB) for synchronization and cross triggering up to 32 HP 64700 Series emulators. Also, powerful sequencing and windowing capability for analyzing multitasking operating systems make HP tools a thorough and viable solution for your Hitachi H8/500 development needs.



Modular HP 64700 Series systems



HP 64700 Series development tools include emulators, emulation bus analyzers, and an external 16-channel timing/state analyzer.

Emulation and analysis systems can be combined in any number of configurations to meet your design needs. Emulators for the Hitachi H8/500 family are available for use in the HP 64700A card cage.

HP 64700A card cage

The HP 64700A card cage is the basis for modular HP 64700 Series emulators and analyzers. It can be disassembled and reassembled for easy, cost-saving reconfiguration to support other 8-, 16-, or 32-bit processors.

The card cage has six and a half card slots. Two and a half slots are dedicated to a card cage host control card, an emulation bus analyzer card, and an optional LAN card. The remaining four slots are available for emulator card sets, a Flash EPROM card, and future products. The Flash EPROM card provides easy software and firmware updates.

Your host computer can communicate with the card cage via LAN, RS-232-C, or RS-422, allowing the HP development tools to operate in a wide variety of design environments. The card cage contains two independent RS-232-C serial ports, each with standard 25-pin female connectors. RS-422 capability embedded in one of the ports can be programmed to operate at rates up to 460 Kbaud and is available for the HP 9000 workstations or IBM PC compatibles. A LAN card supports connection to Ethernet networks via ThinLAN, ThickLAN, or StarLAN. TCP/IP protocols, LAN gateways, subnets, and ARPA/Berkeley standards are supported.

Real-time emulation

State-of-the-art probing technology insures nonintrusive, electrical transparency of targeted processors.

Extensive breakpoint capabilities let you define where to start and stop the execution of code. Up to 32 software breakpoints can be set up in the emulators, allowing execution to be halted at an instruction point. Eight real-time hardware breakpoints increase the flexibility and power of this feature, extending functionality to include stopping at processor address, data, and status points.

Flexible memory configuration

Emulation memory is available as substitution or replacement memory in your embedded design. Emulation memory sizes vary according to the processor selected. Basic assignable memory attributes include target or emulation, and RAM, ROM, or guarded memory. Additional memory attributes may be included, depending on the emulator you select. Dual-port emulation memory lets you display and modify emulation memory locations without interrupting target processor execution. All of these features give you considerable flexibility in a nonintrusive development environment.

Emulation bus analysis

Dual-bus architecture provides real-time, nonintrusive analysis. This allows traces to be set up and reviewed without breaking processor execution.

Tracing microprocessor code flow is a major strength of the HP 64700 Series emulators and analyzers. Up to eight hardware resources, each consisting of addresses, data, and status event comparators, can be combined in sequential trace specifications, using "find A, followed by B..." constructs up to eight levels deep. A range comparator can be applied to address or data events at any one of these levels.

Precise time-tagging of events helps you identify discrepancies in code execution times. Each event is logged into the analyzer with an execution time. Bus cycle, instruction, and module duration times can be measured with 40 ns resolution.

Prestore assists you in pinpointing possible problem areas in your code. For example, prestore determines which of several different tasks accessing a variable is responsible for corrupting it.

These comprehensive resources in the emulation bus analyzer combine to solve both simple and complex problems.

Robust symbolic support

Symbolic debugging clarifies trace list interpretation by allowing you to see program symbols in the trace list. This enables quick identification of problems involving the interaction of software and hardware. You also can use symbols in emulation commands and expressions to simplify command entries and user interaction.

Code coverage analysis

Real-time code coverage analysis by the emulator is an important feature for assessing test program coverage. The coverage analyzer records memory locations accessed by executing code. This information is displayed as a measure of what percentage of memory is being accessed. Unaccessed or accessed memory addresses can be listed to determine quickly how exhaustive a test suite has been.

External state/timing analysis

Sixteen channels of state and timing analysis are available on a 64-channel emulation bus analyzer that can be used with many emulators. The state/timing analysis provides full trigger-and-store qualification capabilities to identify complex problems. The external analyzer can serve as a stand-alone logic analyzer or can be coupled with the emulation bus analyzer for correlation of microprocessor activity with other target system activity. The two analyzers can cross trigger or arm each other on the basis of hardware or software events that one analyzer detects.

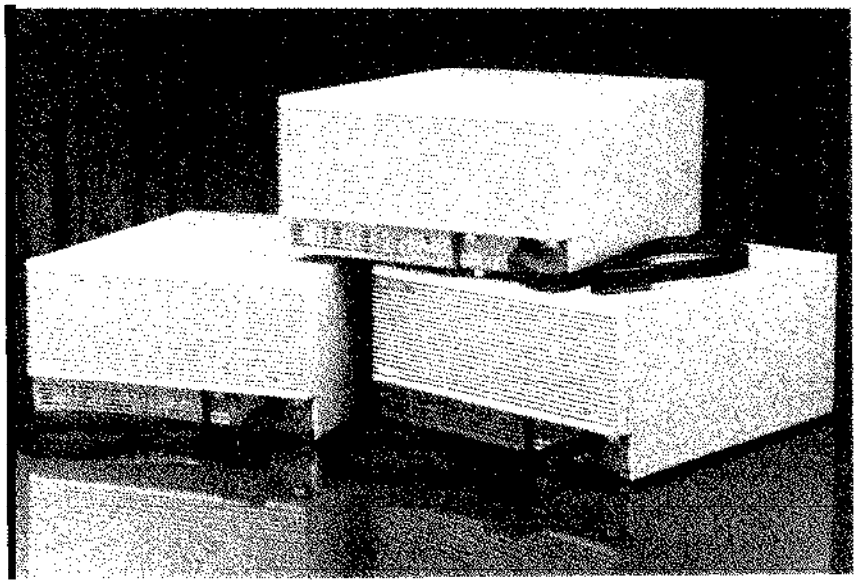
Coordinated measurement bus

Designs involving multiple microprocessors can take advantage of the coordinated measurement bus for synchronized execution (start/stop) of multiple emulators. To help understand and isolate relationships between processors, up to 32 emulators and analyzers can be set up to cross trigger one another. A BNC connector on the card cage can drive or receive a trigger signal to allow cross triggering of logic analyzers, oscilloscopes, and other instruments.

Hitachi H8/500 emulator features

Emulation

- Optional softkey interface or PC user interface for symbolic debug and a friendly, windowed user environment
- 32 software breakpoints
- Eight real-time hardware breakpoints
- Display and modify functions for all registers (including SFR), memory (virtual/actual), and I/O ports
- Coordinated measurement bus for synchronization and cross triggering with up to 32 HP 64700 Series emulators/analyzers
- Two-foot-long, flexible, slim emulation cable, terminating in an 84-pin PLCC probe for H8/532 and H8/534/536, 68-pin PLCC probe or 64-pin SDIP probe (with optional 64-pin DIP adapter) for H8/520, or 112-pin QFP probe for H8/510
- Two independent RS-232-C serial ports, one with RS-422 capability for high-speed upload and download rates
- Optional LAN interface card for use with HP 9000 workstations



Analysis

- 48-, 64-, or 80-channel emulation bus analyzer for H8/532, H8/520, H8/534/536; 64- or 80-channel emulation bus analyzer for H8/510
- 64-channel analyzer has additional 16 channels of external state/timing analysis
- Disassembly of H8/500 instruction set
- Real-time analysis of all address, data, and status lines
- Powerful sequencing and windowing capability for analysis of multitasking operating systems
- Real-time code coverage analysis

Memory

- Real-time, no-wait-state execution up to 10 MHz
- 128 Kbytes of 8-bit emulation memory, mappable in 256-byte blocks (H8/532, H8/520, H8/534/536)
- 128 Kbytes, 512 Kbytes, or 1 Mbyte of 16-bit emulation memory, mappable in 256-byte blocks (H8/510)
- Dual-port memory allows emulation displays and modifications of emulation memory without halting the processor during emulation

Specifications

Processor compatibility: Compatible with Hitachi H8 520 (HD6475208/ HD6433308), H8/532 (HD6475328), and H8/534/536 (HD6435348CP/ HD6475368CP/HD6436358CP), H8/510 (HD6415108F), and any other microprocessors that comply with the specifications of these processors.

Electrical

Maximum external clock speed: 10 MHz with no wait states required for target system or emulation memory.

Internal clock speed: 10 MHz.

Data inputs (H8/520): MD0-MD2, /NMI, 1 HCT load, 10 kohm pull-up to Vcc; /RES, 1 CMOS load plus 1 F load and microprocessor specification load, 5 kohm pull-up to Vcc; PORT2-PORT5, PORT7, P11-P17, 10 kohm pull-up to Vcc; PORT6, unbuffered to CPU; P10, 1 HCT load plus microprocessor specification load, 10 kohm pull-up to Vcc; Avcc, unbuffered to CPU. All inputs have approx 40 pF additional capacitance.

Data inputs (H8/532): MD0-MD2, /STBY, /NMI, 1 HCT load, 10 kohm pull-up to Vcc; /RES, 1 CMOS load plus 1 F load and microprocessor specification load, 5 kohm pull-up to Vcc; PORT2-PORT7, PORT9, P10, P11, P15, P16, P17, 10 kohm pull-up to Vcc, unbuffered to CPU; PORT8, unbuffered to CPU; P12, P13, P14, 1 HCT load plus microprocessor specification load, 10 kohm pull-up to Vcc; Avcc, unbuffered to CPU. All inputs have approx 40 pF additional capacitance.

Data inputs (H8/536): MD0, MD1, MD2, /STBY, /NMI, /RES, 1 HCT load, 10 kohm pull-up to Vcc; PORT1-PORT9, 10 kohm pull-up to Vcc, unbuffered to CPU. All inputs have approx 40 pF additional capacitance.

Data inputs (H8/510): MD0, MD1, MD2, /STBY, /NMI, /RES, 1 HCT load, 10 kohm pull-up to Vcc; PORT3-8, 10 kohm pull-up to Vcc, unbuffered to CPU. All inputs have approx 40 pF additional capacitance.

Data outputs: Approx 40 pF load; 51 ohm series; 10 kohm pull-up to Vcc.

Power: 60 mA at +5V drawn from target system; all other power supplied by emulator.

Regulatory compliance

(When installed in HP 64700A card cage)

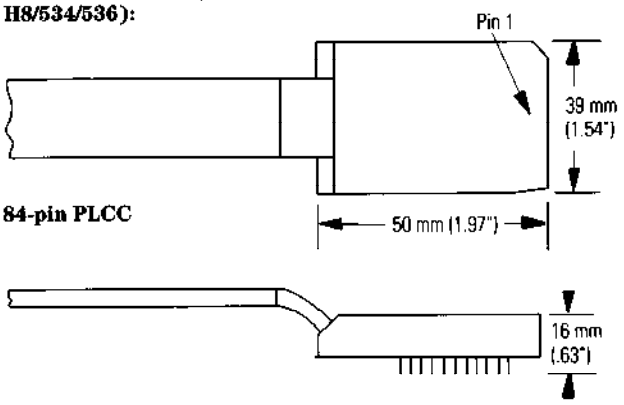
Electromagnetic interference: VDE 0871/6.78 Level A; C.I.S.P.R. 11.

Safety approvals: self-certified to UL 1244, IEC 348, CSA 22.2.

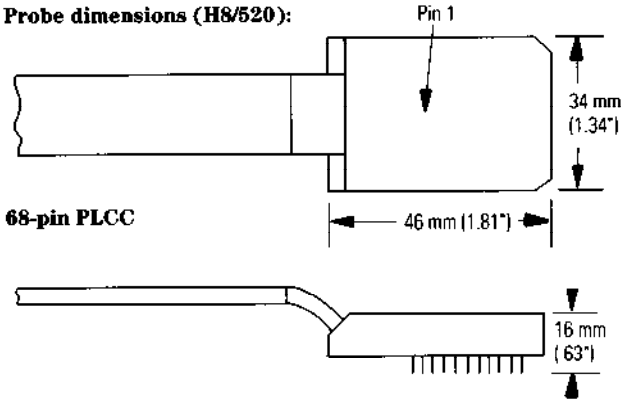
Physical

Cable length: emulator to target system, approx 600 mm (2 ft).

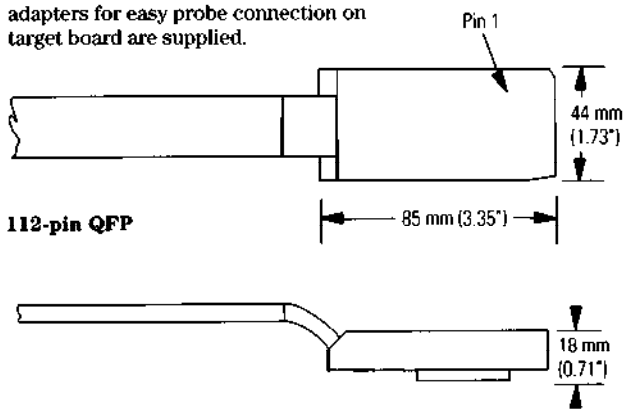
Probe dimensions (H8/532 and H8/534/536):



Probe dimensions (H8/520):



Probe dimensions (H8/510): special adapters for easy probe connection on target board are supplied.



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Ordering Information

Complete Emulation System

Model	Description
64737F	**H8/532 Emulator Card**
64738F	**H8/520 Emulator Card**
64739A	**H8/534/536 Emulator Card**
64732A	**H8/510 Emulator Card**
64725A	**8-bit, 128 Kbytes Emulation Memory** (for H8/520/532/534/536)
64727A	**16-bit, 512 Kbytes Emulation Memory** (for H8/510)
64706A	**48-channel Emulation Bus Analyzer Card** (for H8/520/532/534/536)
64704A	**80-channel Emulation Bus Analyzer Card**
64700A	**Card Cage**

Emulation System Options

64726A	**16-bit, 128 Kbytes Emulation Memory** (for H8/510)
64728A	**16-bit, 1 Mbyte Emulation Memory** (for H8/510)
64703A	**64-channel Emulation Bus Analyzer Card** with 16 channels of external state/timing
64737S	**H8/532 Host Interface Software**
Opt 004	Softkey Interface hosted on HP 9000 Series 300/400 workstations*
Opt 006	PC Interface on IBM PC/XT, PC/AT, HP Vectra PCs and compatibles
64738S	**H8/520 Host Interface Software**
Opt 004	Softkey Interface hosted on HP 9000 Series 300/400 workstations*
Opt 006	PC Interface on IBM PC/XT, PC/AT, HP Vectra PCs and compatibles
64739S	**H8/534/536 Host Interface Software**
Opt 004	Softkey Interface hosted on HP 9000 Series 300/400 workstations*
Opt 006	PC Interface on IBM PC/XT, PC/AT, HP Vectra PCs and compatibles
64732S	**H8/510 Host Interface Software**
Opt 004	Softkey Interface hosted on HP 9000 Series 300/400 workstations*
Opt 006	PC Interface on IBM PC/XT, PC/AT, HP Vectra PCs, and compatibles
64869L/M/U	**Cross Assembler/Linker for H8/500 Family**
Opt 004	For HP 9000 Series 300/400 workstations
64869L/M	**Cross Assembler/Linker for H8/500 Family**
Opt 006	For IBM PC/XT, PC/AT, HP Vectra PCs and compatibles
64701A	**LAN Card** (supported on HP 9000 workstations)
64037A	**RS-422 Interface Card for PC compatibles**
98659A	**RS-422 Interface Card for HP 9000 workstations**
64023A	**CMB Cable** (4 m long includes three 9-pin connectors)
64738-61611	**64-pin SDIP Adapter for H8/520**

Note: an RS-232-C interface is supplied with all HP 64700A card cages.

Software Support

HP provides software upgrades through the purchase of the Software Materials Subscription (SMS) service. Contact your HP sales representative for more information.

* Requires HP 64801 Operating Environment software.

HP Sales and Support Offices

United States:
Microprocessor Development Hotline
tel: (800) 447 3282
fax: (719) 590 5054

Canada:
Hewlett-Packard Ltd.
6877 Goreway Drive
Mississauga, Ontario
L4V 1M8
(416) 678 9430

Europe:
Hewlett-Packard S.A.
Marcom Operations Europe
P.O. Box 529
1180 AM Amstelveen
The Netherlands
(31) 20 547 9999

Japan:
Yokogawa-Hewlett-Packard Ltd.
15-7, Nishi Shinjuku 4 Chome
Shinjuki-ku
Tokyo 160, Japan
(03) 5371 1351

Latin America:
Latin American Region
Headquarters
Monte Pelvoux No. 111
Lomas de Chapultepec
11000 Mexico, D.F. Mexico
(525) 202 0155

Australia/New Zealand:
Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Melbourne, Australia
(03) 895 2895

Far East:
Hewlett-Packard Asia Ltd.
22/F Bond Centre, West Tower
89 Queensway, Central,
Hong Kong
8487777

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