HEWLETT PACKARD

HP 64700 Series Emulators for Motorola 68020/68EC020 and 68030/68EC030 Processors

Technical Data

Design, debug, and integrate real-time embedded systems

Description

The HP 64747B emulator supports Motorola 68030 and 68EC030 microprocessors through 40 MHz operation. The HP 64748A emulator supports Motorola 68020 and 68EC020 microprocessors through 33 MHz.

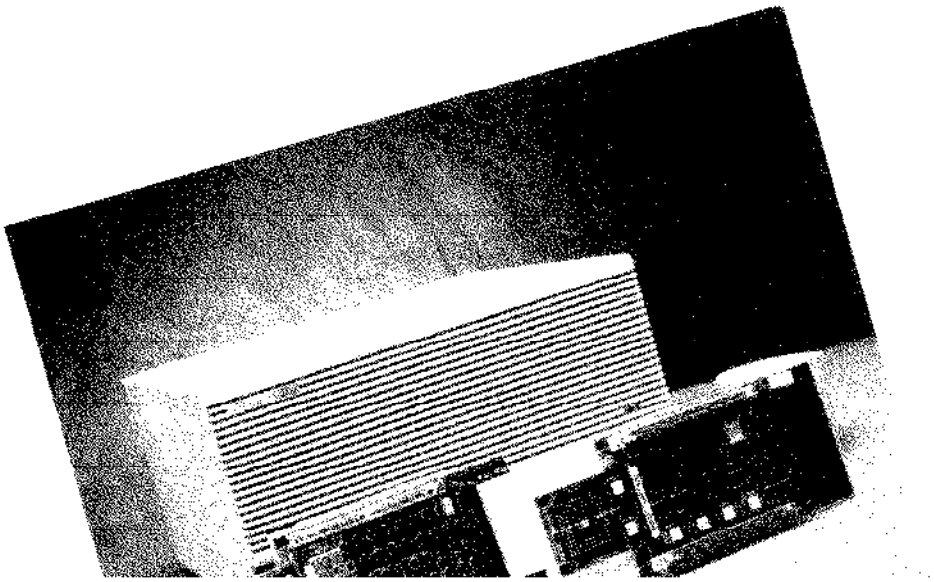
The HP 64747B active probe emulator supports 68030 target systems that use the memory management unit (MMU). The 68030 MMU registers and tables are displayed and physical addresses are translated to corresponding logical addresses to link bus and program activity (DeMMUing). MMU table information can be updated automatically from the target system by user command.

The emulators plug into the modular HP 64700A card cage, which connects to your host via RS-232, RS-422, or LAN. Easy-to-use interfaces are offered on IBM-compatible PCs, Sun SPARC-stations, and HP 9000 Series 300/400/700 workstations. Additionally, the card cage has a firmware-resident interface which can talk to any ASCII terminal.

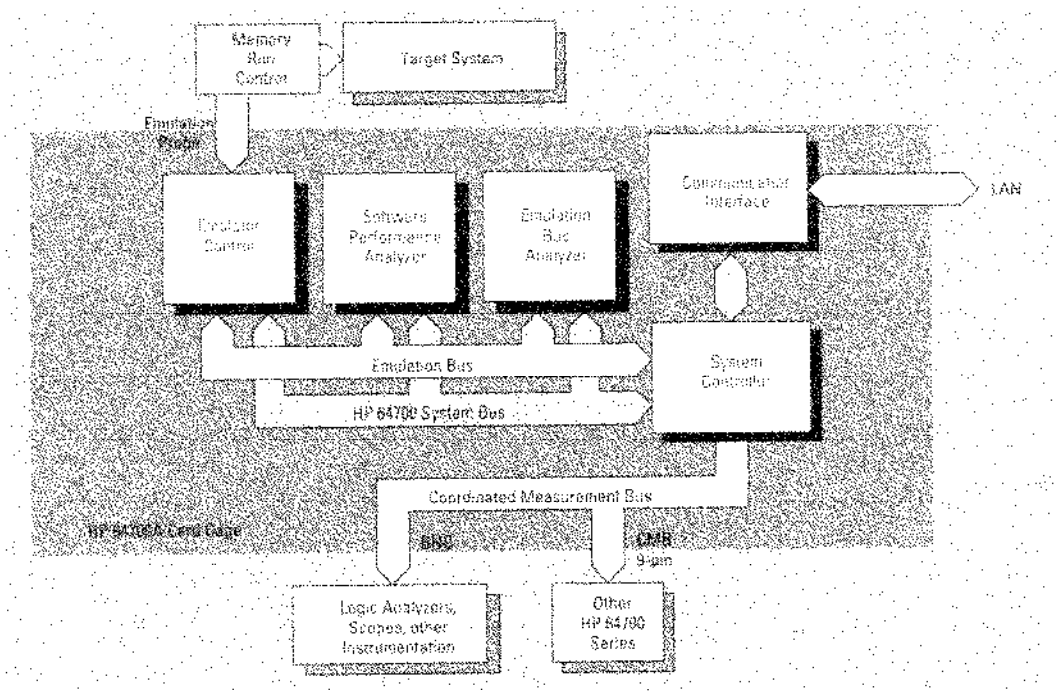
For software development, the HP AxCASE environment is available on Sun SPARCstations and HP workstations. This environment includes an ANSI standard C compiler, assembler/linker, a debugger that uses either a software simulator or the emulator for instruction execution, and the HP Branch Validator for test suite verification.

If your software development platform is a personal computer, language support is available from several software vendors. The emulators consume industry standard output file formats including IEEE-695.

Ada language support is provided on HP 9000 workstations, DEC VAX/VMS, and Sun SPARCstations by several software vendors. An Ada application developer can use the HP emulator with any compiler that generates IEEE-695.1 object format.



Modular HP 64700 Series systems



HP 64700 Series development tools include an emulator, an emulation bus analyzer, and an optional software performance analyzer (SPA).

HP 64700A card cage

The HP 64700A card cage is the basis for modular HP 64700 Series emulators and analyzers. It can be disassembled and reassembled for easy, cost-saving reconfiguration to support other 8-, 16-, or 32-bit processors.

The card cage has six and a half card slots. Two and a half slots are dedicated to a card cage host control card, an emulation bus analyzer card, and an optional LAN card. The remaining four slots are available for an emulator card set, an optional software performance analyzer card and future products.

Communication with the card cage is accomplished via LAN, RS-422 or RS-232, allowing the HP development tools to operate in a variety of environments.

Your investment in HP emulators for Motorola 68020, 68EC020, 68030, 68EC030 or 68340 processors is protected through the modular subsystems. Each of the emulators can be reconfigured by simply changing the active probe. This modular design results in cost effective support for a variety of processors.

Real-time emulation

The HP 64747B and HP 64748A are active probe emulators that contain the microprocessor, emulation monitor, and run control circuitry. Additionally, both a custom memory mapper chip and memory are located on the probe. As a result of this technology, the HP 64748A (68020/EC020) runs up to 33 MHz with zero wait-states out of target memory. HP 64747B (68030/EC030) runs with zero wait-states out of target memory through 25 MHz. Above 25 MHz three cycle asynchronous and synchronous accesses are supported. Burst mode accesses above 25 MHz support a 3-2-2-2 cycle pattern.

For run control, extensive breakpoint capabilities let you define where to start and stop the execution of code. Up to 32 software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point. Hardware breakpoints increase the flexibility and power of this feature, for stopping at processor address, data and status points.

Flexible memory configuration

Memory modules are used for emulation memory. Two slots are available on the active probe, allowing you to plug in the amount of memory you need up to two megabytes. If you initially order less than the maximum amount, you can easily expand your system by adding the appropriate module[s]. Modules for 256 Kbyte (HP 64171A) and 1 Mbyte (HP 64171B) are available and can be used in any combination with a maximum configuration of 2 Mbytes.

For the HP 64748A (68020/68EC020) there are zero wait-states out of emulation memory through 25 MHz operation. Above 25 MHz one wait-state is inserted.

Three cycle asynchronous and synchronous accesses are supported through 40 MHz operation for HP 64747B (68030/EC030). Burst mode accesses are made in a 3-2-2-2 cycle pattern.

In addition to the memory modules, four kilobytes of dual-ported emulation RAM is available when the background monitor is used. This dual-ported memory allows you to display and modify critical program variables without halting the target system.

Emulation bus analysis

Dual-bus architecture provides real-time, nonintrusive analysis. This allows traces to be set up and reviewed without breaking processor execution.

Tracing microprocessor code flow is a major strength of the HP 64700 Series emulators and analyzers. Up to eight hardware resources, each consisting of addresses, data, and status event comparators can be combined in sequential trace specifications, using "find A, followed by B..." constructs up to eight levels deep. A range comparator can be applied to address or data events at any one of these levels. The analyzer will trigger and store any subsequent execution or store only specified execution information. These comprehensive resources may be combined to solve both simple and complex problems.

Precise time tagging of events helps you identify discrepancies in code execution times. Each event is logged into the analyzer with an execution time through a 16.67 MHz bus rate. Bus cycle, instruction, and module duration times can be measured with 40 ns resolution.

Robust symbolic support

If your language system generates HP/MRI IEEE-695, or HP-OMF file formats and if you are using the PC or workstation interface, extensive symbolic information is available. Program symbols can be used in run control, trace specification, and storage qualification commands. Symbol information is displayed in trace and memory mnemonic displays and when you are single stepping.

If you are using C language on a workstation, source lines can be intermixed in the trace display for easy correlation between the analysis trace and original source. Source line numbers are displayed within the PC interface.

Software performance analysis

Optional software performance analysis enables you to tune and verify the time-critical aspects of your design. These capabilities are provided at both the C source and assembly language level. Through automated one-key set up, this system quickly identifies code bottlenecks and gathers statistics and timing information that significantly reduce time and effort in optimizing code.

Probing accessories

Probing accessories are available for the active probe PGA connectors on both emulators. There are PGA-to-PGA low-profile extension cables and ninety-degree CW and CCW rotators. For surface-mounted packages, there are PGA-to-PQFP adapters. To complete the PQFP connection, a PQFP dummy part replaces an active surface-mount processor and must be assembled on the target board during the surface mount process for the PQFP adapter to connect properly.

Coordinated measurements

Designs involving multiple microprocessors can be analyzed with the Coordinated Measurement Bus (CMB) for synchronized execution (start/stop) of multiple emulators. To help understand and isolate relationships between processors, up to 32 emulators and analyzers can be set up to cross trigger one another. A BNC connector included on the card cage can drive or receive a trigger signal to allow cross triggering of logic analyzers, oscilloscopes, and other instrumentation.

Emulation features

68020/68EC020
(Adapter required for 68EC020)

- Support for 68020 and 68EC020
- 33 MHz active probe emulator
- Zero wait-states out of target memory
- Zero wait-states out of emulation memory through 25 MHz (one wait-state above 25 MHz)

68030/68EC030

- Support for 68030 MMU and DeMMU operation
- 40 MHz active probe emulator
- Supports burst and synchronous mode in target memory and emulation memory
- Supports zero wait-states out of target memory through 25 MHz. Above 25 MHz 3 cycle accesses in async and sync modes (burst 3-2-2-2 cycles)
- Emulation memory supports 3 cycle asynchronous accesses through 40 MHz (three cycle synchronous and 3-2-2-2 burst cycle accesses through 40 MHz)
- Selective cache inhibit for block of memory (256 byte resolution)

Common features

- 36-inch probe cable terminating in active probe
- Symbolic support (with PC and workstation interface)
- 32 software breakpoints
- 8 real-time hardware breakpoints
- Background and foreground monitors (Background monitor is not available while using the 68030 MMU)
- Simulated I/O (on workstations)
- Support for IEEE-695, HP-OMF, Motorola S-Records and Extended Tek HEX file formats (symbols supported with IEEE-695 and HP-OMF)
- Multiprocessor emulation
  –synchronous start of up to 32 emulators
  –cross triggering from another emulator, logic analyzer, or oscilloscope
- Integrated C language system available
- Demo board and self test module

Emulation bus analyzer

- 80-channel emulation bus analyzer (HP 64704A)
- Postprocessed dequeued trace with symbols and source lines (the PC interface trace listing contains source line numbers)
- 8 events each consisting of address, status and data comparators
- Events may be sequenced 8 levels deep and can be used for complex trigger qualification and selective store

Emulation memory

- 256 Kbyte, 512 Kbyte, 1 Mbyte, 1.25 Mbyte, and 2 Mbyte memory configurations
- Mapping resolution of 256 bytes

Easy-to-use interfaces

Easy-to-use interfaces are available on HP 9000 workstations, Sun SPARCstations, and PCs.
The workstation interface can run in the X-Windows or Open Windows environments, allowing you to open several emulation and analysis windows during a session. For example, you can have a window open displaying global symbols and another window displaying trace results. Command selection is done with the click of a mouse button and the interface guides you through command completion.

On the PC, the emulation interface is windowed. Commands are selected by pressing the first letter of a command and you are guided through completion of the command syntax. Function keys can be defined as a macro to represent a sequence of commonly used commands. For trace specification, there is a window dedicated to defining events and another window dedicated to defining the search sequence. This logical partioning aids a user in defining complex measurements.

High-level debug

The same high level debugger interface that controls the software simulator can also be used to control the emulator on supported workstations. This allows a designer to debug code in real time while maintaining the benefits of a source level debugger.

Full source debugging is provided for the HP 64748A and 64747B emulators by the AxCASE debuggers on HP 9000 workstations and Sun SPARCstations. These debuggers support data types, stack backtrace, and stack-resident local variables. Code runs in real-time on the emulators and breakpoints are set via the debugger interface. Source debugging is also provided by various third-party software vendors.

Specifications

Processor compatibility: HP 64748A is compatible with Motorola 68020/68EC020. (HP E3400A adapter required to connect to 68EC020-based systems.) HP 64747B is compatible with Motorola 68030 and 68EC030.

Electrical

Maximum clock speed
68020/68EC020: 33 MHz with no wait-states required for target system memory.

68030/EC030: supports zero wait-states out of target memory through 25 MHz. From 25 MHz to 40 MHz, 3 cycle accesses in async and sync modes (burst 3-2-2-2 cycles).

Emulation memory speed
68020/68EC020: 25 MHz with no wait-states for emulation memory (one wait-state above 25 MHz).

68030/EC030: supports 3 cycle asynchronous accesses through 40 MHz (three cycle synchronous and 3-2-2-2 burst cycle accesses through 40 MHz).

Environmental

Temperature: operating, 0° to +40°C (+32°F to +104°F) nonoperating -40°C to +70°C (-40°F to +158°F). It is recommended that 100 LFM of airflow be provided over the 68EC030 probe for optimum performance.

Altitude: operating, 4600 m (15 000 ft); nonoperating 15 300 m (50 000 ft).

Relative humidity: 15% to 95%.

Regulatory Compliance

(When installed in HP 64700A card cage)

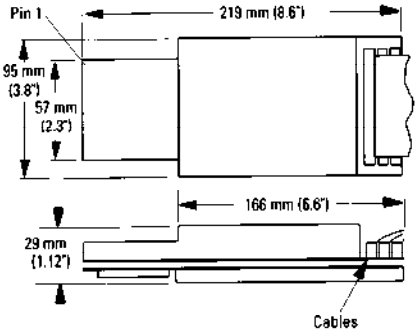
Electromagnetic interference: VDE 0871/6.78 Level A; C.I.S.P.R. 11.

Safety approvals: self-certified to UL 1244, IEC 348, CSA 22.2.

Physical

Cable length: emulator to target system, approx 914 mm (36 in.).

Probe dimensions:



Emulator AC Electrical Specifications (68020/EC020) — Read and Write Cycles

Num.	Characteristic	33 MHz Min	Max	Unit
6	Clock High to FC, Size, $\overline{RMC}$, Address Valid	0	21	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, Asserted	3	20*	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, Negated	3	20*	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to FC, Size, $\overline{RMC}$, Address Invalid	0*	-	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	0*	-	ns
23	Clock High to Data Out Valid	-	23*	ns
25	$\overline{AS}$, $\overline{DS}$ Negated to Data Out Invalid	2	-	ns
26	Data Out Valid to $\overline{DS}$ Asserted (Write)	5	-	ns
27	Data-In Valid to Clock Low (Synchronous Setup)	10*	-	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup)	10*	-	ns
31	$\overline{DSACK}$x Asserted to Data-In Valid (Asynchronous Data Setup)	-	13*	ns
31A	$\overline{DSACK}$x Asserted to $\overline{DSACK}$x Valid (Skew)	-	7	ns
47A	Asynchronous Input Setup Time ($\overline{HALT}$, $\overline{BERR}$, $\overline{DSACK}$x)	10*	-	ns
	Asynchronous Input Setup Time ($\overline{IPL}$x)	10*	-	ns

* Differs from chip specification.

Emulator DC Electrical Specifications (68020/EC020)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	–0.5	0.8	V
Input Leakage Current — $\overline{BR}$, $\overline{BGACK}$, $\overline{IPL}$x	I_{in}	–2.5	2.5	µA
GND≤Vin≤V_{CC}				
Input High Current — $\overline{BERR}$, $\overline{AVEC}$, $\overline{DSACK}$x	I_{IH}	-	25	µA
CLK, $\overline{RESET}$, $\overline{HALT}$		-	50	
Input Low Current — $\overline{RESET}$, $\overline{HALT}$	I_{IL}	-	–1.4	mA
CLK, $\overline{BERR}$, $\overline{AVEC}$, $\overline{DSACK}$x		-	–0.25	
Output High Voltage — A0-A31, $\overline{AS}$, $\overline{BG}$, D0-D31, $\overline{DBEN}$, $\overline{DS}$, $\overline{ECS}$, R/$\overline{W}$,	V_{OH}	2.4	-	V
I_{OH}=–400µA — $\overline{IPEND}$, $\overline{OCS}$, $\overline{RMC}$, SIZ0-SIZ1, FC0-FC2				
Output Low Voltage	V_{ol}			V
I_{OL}=2.5 mA — A0-A31, FC0-FC2, SIZ0-SIZ1		-	0.5	
I_{OL}=3.2 mA — $\overline{BG}$, D0-D31		-	0.5	
I_{OL}=4.5 mA — R/$\overline{W}$, $\overline{RMC}$		-	0.5	
I_{OL}=5.3 mA — $\overline{AS}$, $\overline{DS}$, $\overline{DBEN}$, $\overline{IPEND}$		-	0.5	
I_{OL}=2.0 mA — $\overline{ECS}$, $\overline{OCS}$		-	0.5	
I_{OL}=9.3 mA — $\overline{RESET}$, $\overline{HALT}$		-	0.5	
Power Dissipation — T_A=0°C	P_D	-	2.2	W
T_A=70°C		-	2.2	
Capacitance	C_{in}	-	20	pF
V_{in}=0 V, T_A=25°C, f = 1 MHz				
Load Capacitance — A0-A31, FC0-FC2, SIZ0-SIZ1, R/$\overline{W}$	C_L	-	100	pF
All Other		-	50	

Emulator AC Electrical Specifications (68030/EC030) — Read and Write Cycles

Num.	Characteristic	25 MHz Min	25 MHz Max	40 MHz Min	40 MHz Max	Unit
6	Clock High to FC, Size, $\overline{RMC}$, $\overline{CIOUT}$, Address Valid	0	20	0	14	ns
	Clock High to $\overline{IPEND}$ Valid	0	24*	0	24*	ns
6B	FC, Size, $\overline{RMC}$, $\overline{CIOUT}$, Address Valid to Negating $\overline{ECS}$	3	-	3	-	ns
	$\overline{IPEND}$ Valid to Negating $\overline{ECS}$	1*	-	–7*	-	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CBREQ}$ Asserted	3	18	2	15*	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CBREQ}$ Negated	0	18	0	15*	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to FC, Size, $\overline{RMC}$, $\overline{CIOUT}$, Address Invalid	6*	-	–2*	-	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	6*	-	–2*	-	ns
23	Clock High to Data Out Valid	-	20	-	19*	ns
24	Data Out Valid to Negating Edge of $\overline{AS}$	5	-	1*	-	ns
25	$\overline{AS}$, $\overline{DS}$ Negated to Data Out Invalid	7	-	0*	-	ns
26	Data Out Valid to $\overline{DS}$ Asserted (Write)	7	-	1*	-	ns
27	Data-In Valid to Clock Low (Synchronous Setup)	6*	-	6*	-	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup)	8*	-	8*	-	ns
31	$\overline{DSACK}$x Asserted to Data-In Valid (Asynchronous Data Setup)	-	28	-	12*	ns
31A	$\overline{DSACK}$x Asserted to $\overline{DSACK}$x Valid (Skew)	-	7	-	1*	ns
47A	Asynchronous Input Setup Time ($\overline{HALT}$, $\overline{BERR}$, $\overline{DSACK}$x)	7*	-	7*	-	ns
	Asynchronous Input Setup Time ($\overline{IPL}$x)	12*	-	12*	-	ns
60	Synchronous Input Valid to Clock High (Setup Time)	4*	-	4*	-	ns

* Differs from chip specification.

Emulator DC Electrical Specifications (68030/EC030)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	–0.5	0.8	V
Input Leakage Current — $\overline{BR}$, $\overline{BGACK}$, $\overline{IPL}$x, $\overline{CDIS}$	I_{in}	–2.5	2.5	µA
GND≤Vin≤V_{CC}				
Input High Current — $\overline{CBACK}$, $\overline{CIIN}$, $\overline{STERM}$	I_{IH}	-	0	µA
— $\overline{BERR}$, $\overline{AVEC}$, $\overline{DSACK}$x, $\overline{HALT}$, $\overline{MMUDIS}$		-	25	
— CLK, $\overline{RESET}$		-	50	
Input Low Current — $\overline{RESET}$, $\overline{CBACK}$, $\overline{CIIN}$, $\overline{STERM}$	I_{IL}	-	–1.4	mA
— CLK, $\overline{BERR}$, $\overline{AVEC}$, $\overline{DSACK}$x, $\overline{HALT}$, $\overline{MMUDIS}$		-	–0.25	
Output High Voltage — A0-A31, $\overline{AS}$, $\overline{BG}$, D0-D31, $\overline{DBEN}$, $\overline{DS}$, $\overline{ECS}$,	V_{OH}	2.4	-	V
— R/$\overline{W}$, $\overline{STATUS}$, $\overline{REFILL}$, $\overline{IPEND}$, $\overline{OCS}$, $\overline{RMC}$,		2.4	-	
I_{OH}=–400µA — SIZ0-SIZ1, FC0-FC2, $\overline{CBREQ}$, $\overline{CIOUT}$		2.4	-	
Output Low Voltage	V_{ol}			V
I_{OL}=2.5 mA — A0-A31, FC0-FC2, SIZ0-SIZ1		-	0.5	
I_{OL}=3.2 mA — $\overline{BG}$, D0-D31		-	0.5	
I_{OL}=4.5 mA — R/$\overline{W}$, $\overline{RMC}$		-	0.5	
I_{OL}=5.3 mA — $\overline{AS}$, $\overline{DS}$, $\overline{DBEN}$, $\overline{IPEND}$		-	0.5	
I_{OL}=2.0 mA — $\overline{STATUS}$, $\overline{REFILL}$, $\overline{CBREQ}$, $\overline{CIOUT}$, $\overline{ECS}$, $\overline{OCS}$		-	0.5	
I_{OL}=9.3 mA — $\overline{RESET}$		-	0.5	
Power Dissipation — T_A=0°C	P_D	-	3.4	W
Capacitance	C_{in}	-	20	pF
V_{in}=0 V, T_A=25°C, f = 1 MHz				
Load Capacitance — A0-A31, FC0-FC2, SIZ0-SIZ1, R/$\overline{W}$, $\overline{CBREQ}$, $\overline{CIOUT}$	C_L	-	100	pF
— All Other		-	50	pF

Ordering Information

Terminal Based Emulation System

Model	Description
64748A	**68020/68EC020 Active probe emulator** (HP E3400A adapter required to connect to 68EC020 PGA-based systems)
64747B	**68030/EC030 Active probe emulator**
64748C	**Emulation control card**
64700A	**Card Cage**
64704A	**80-channel Emulation Bus Analyzer card**

Emulation System Components

64171A	**256 Kbyte 35 ns SRAM Memory Module**
64171B	**1 Mbyte 35 ns SRAM Memory Module**
64701A	**LAN Card** (supported on HP 9000 Series Workstations and SunSPARCstations)
64037A	**RS-422 Interface Card for PC Compatibles** (software supplied)
64708A	**Software performance analyzer card** (B1487A software required) (supported on HP 9000 series workstations and Sun SPARCstations)
64023A	**CMB cable** (4 m long; includes three 9-pin connectors)

Software for PCs

64748S	**68020/EC020 User Interface**
Opt 006	
64747S	**68030/EC030 User Interface**
Opt 006	

Software for Workstations

Note: for each software model number ordered, purchase one media option and at least one license option for each concurrent user.

B1471B	**64000-UX Operating environment** (required for all workstation based systems)
B1487A	**Software Performance Analysis Hosted User Interface**

68020/EC020 Support

B1475B	**Graphical User Interface**
B1464A	**Cross Assembler linker**
B1461A	**Cross C Compiler**
B1466B	**Cross Debugger Simulator**
B1476B	**Cross Debugger Emulator**

68030/EC030 Support

B1479B	**Graphical User Interface**
B1465A	**Cross Assembler linker**
B1461A	**Cross C Compiler**
B1466B	**Cross Debugger Simulator**
B1476B	**Cross Debugger Emulator**

Option Numbers

Opt AAH	HP 9000 Series 300/400 manuals/media (DDS DAT tape)
Opt AAX	HP 9000 series 300/400 manuals/media (1/4 in cartridge tape)
Opt UBX	HP 9000 series 300/400 single user license
Opt AAY	HP 9000 series 700 manuals/media (DDS DAT tape)
Opt UBY	HP 9000 series 700 single user license
Opt AAV	Sun SPARCstation manuals/media (1/4 in cartridge tape)
Opt UBK	Sun SPARCstation single user license

HEWLETT PACKARD

Adapters/Extenders/Rotators

Model	Description
	Emulator to Target
E3400A	**68020 PGA to 68EC020 PGA adapter**
E3401A	**68020 PGA to 68EC020 PQFP adapter** (includes HP P/N 64748-87607 SMT adapter)
E3403A	**68020 PGA to PGA flexible cable extender**
E3404A	**68020 PGA to 68020 PQFP adapter** (includes HP P/N 64748-87608 inactive mechanical sample)
E3405A	**68030/EC030 PGA to PGA flexible cable extender**
E3406A	**68030/EC030 PGA to 68030/EC030 PQFP adapter** (includes HP P/N 64748-87608 inactive mechanical sample)

HP P/N	Description
64748-87608	**Inactive Mechanical Sample** (this is an inactive 132 pin PQFP processor package that replaces the target system processor, two per package)
64748-87607	**Additional SMT Adapter for E3401A**

Note: The inactive mechanical sample is supplied with the E3404A and E3406 PGA to PQFP adapters. The sample should be assembled on the target board during the surface mount process for the PQFP adapter to connect properly.

The following information about probe rotators is supplied courtesy of Emulation Technology, Inc.

Processor	Description	Emulation Technology P/N
68020 PGA	Rotates probe 90° CW	RA114P3CCW68020
68020 PGA	Rotates probe 90° CCW	RA114P3CW68020
68EC020 PGA	Rotates probe 90° CW	RA100P3CCWEC020
68EC020 PGA	Rotates probe 90° CCW	RA100P3CWEC020
68030 PGA	Rotates probe 90° CW	RACCW90CP368030
68030 PGA	Rotates probe 90° CCW	RAC90CP368030
68EC030 PGA	Rotates probe 90° CW	RA124P3CCWEC030
68EC030 PGA	Rotates probe 90° CCW	RA124P3CWEC030

Please order rotators from:

Emulation Technology, Inc.
2344 Walsh Ave. Bldg. F
Santa Clara, CA 95051
408-982-0660
FAX 408-982-0664

Or, refer to the Emulation Technology catalog for the nearest distributor.

Software Support

HP provides software upgrades through the purchase of the Software Materials Subscription (SMS) service. Contact your HP field engineer for more information.

Note: Contact your local HP Field Engineer for configuration information, supported processor speeds, and latest software options.

HP Sales and Support Offices

United States:
Microprocessor Development Hotline
(800) 447 3282

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Hewlett-Packard Ltd.
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