HP E2444A

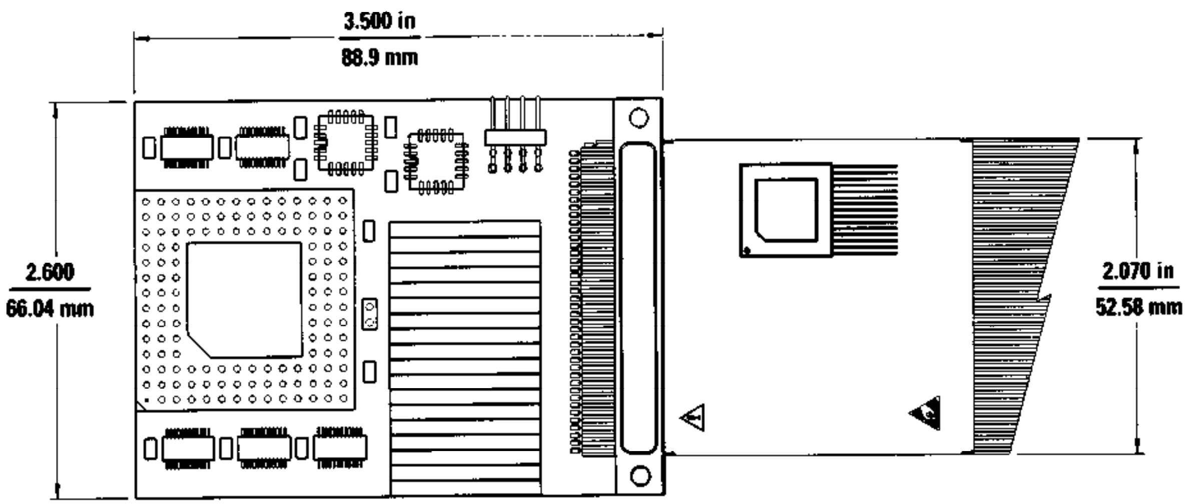
Preprocessor Interface for the Intel i386DX

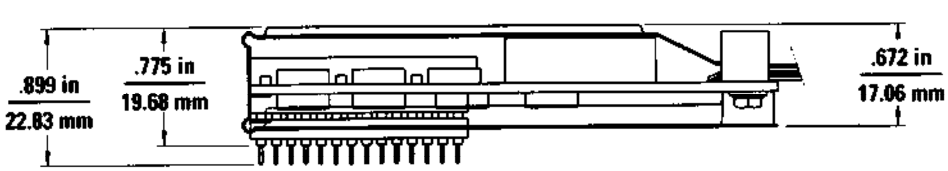
For use with HP logic analyzers

The Hewlett-Packard E2444A preprocessor supports the Intel i386DX. The preprocessor interface provides an electrical and mechanical connection between your target system and an HP logic analyzer.

Preprocessor software configures the logic analyzer labeling address, data and status lines. Additionally, when a state trace is displayed the data is disassembled and listed in Intel i386DX mnemonics.

The disassembler also decodes coprocessor cycles for target systems that use the Intel i386DX .





HEWLETT PACKARD

Key Specifications

Microprocessor Supported:
25 and 33-MHz, 132-pin PGA Intel i386DX

Capabilities:
Signal Loading: 8 pF on all channels, except 15 pF on ADS and READY.
Low profile, non-intrusive design.

Data Sampling Modes:

- **State-per-bus mode** - address and data are aligned and captured on the same state. All unnecessary wait states and idle states are filtered out. Both pipelined and non-pipelined modes are supported. Complete software inverse assembly is provided. All queue flush instructions are marked (Default mode).

- **State-per-clock mode** - address and data are captured on each CPU clock. This feature is useful in debugging system crashes.

- **Timing mode** - all active buffers are tri-stated and data is sampled every 4 ns. This feature is used when accurate timing measurements are desired.

Inverse Assembler Features:
All processor and coprocessor instructions and all bus cycles are supported.

The following CPU operations are supported: Memory Read/Write, I/O Read/Write, Opcode Fetch, Interrupt Acknowledge Type 0-255, Halt, Shutdown, 80287/80387 Coprocessor operations, and register and bus sizes 16 and 32.

Disassembly is synchronized at branch addresses.

Queue flush instructions are identified and marked for all bus sizes. Instructions which are pre-fetched but not executed, are marked in the state listing. FPU instructions are decoded in the display.

The preprocessor allows you to control the amount of information being sent to the analyzer. This improves trace readability. For example, you can configure the preprocessor to not pass cache invalidation cycles to the analyzer. For DMA transfers you can configure the preprocessor to send all DMA cycles, to send just one cycle which indicates a DMA transfer occurred, or to send no DMA cycles to the analyzer.

Logic Analyzers Supported:
HP 1650B/52B, HP 16510B, HP 16511B, HP 16540/41[A-D], HP 16550A, HP 1660 series.

Number of Probes Required:
Five, 16-channel probes are required for complete state disassembly.

Termination Adapters (TA):
No TAs are required; all terminations are mounted on the pod.

For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below:

United States:
Hewlett-Packard Company
4 Choke Cherry Road
Rockville, MD 20850
(301) 670 4300

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5201 Tollview Drive
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