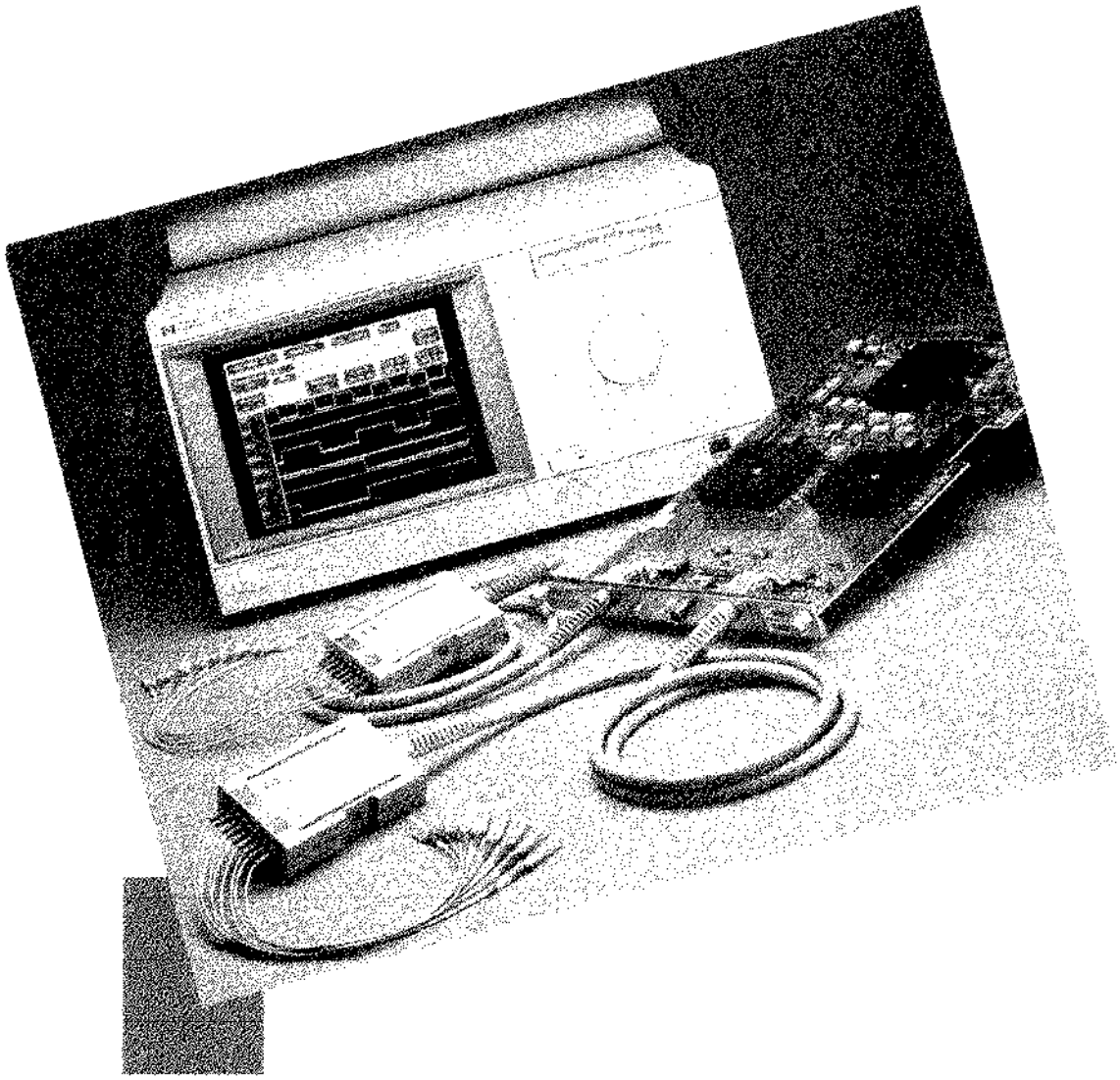
HEWLETT PACKARD

4-GSa/s Timing and 1-GSa/s Synchronous State for the HP 16500A/B Logic Analysis System



The HP 16517/18A — Ultra High Speed Timing and State Analysis at an Affordable Price

Trace more channels with higher accuracy than ever before in a logic analyzer. Solve your toughest problems with the fastest, most flexible state analysis available.

Timing Analysis

- **4-GSa/s Conventional Timing Analysis**

  Verify the timing of critical edges with 250 ps resolution, across up to 40 channels, or 500 ps resolution, across up to 80 channels.

Synchronous State Analysis

- **1-GSa/s Synchronous State Analysis**

  View high speed data streams at full speed on up to 80 channels.

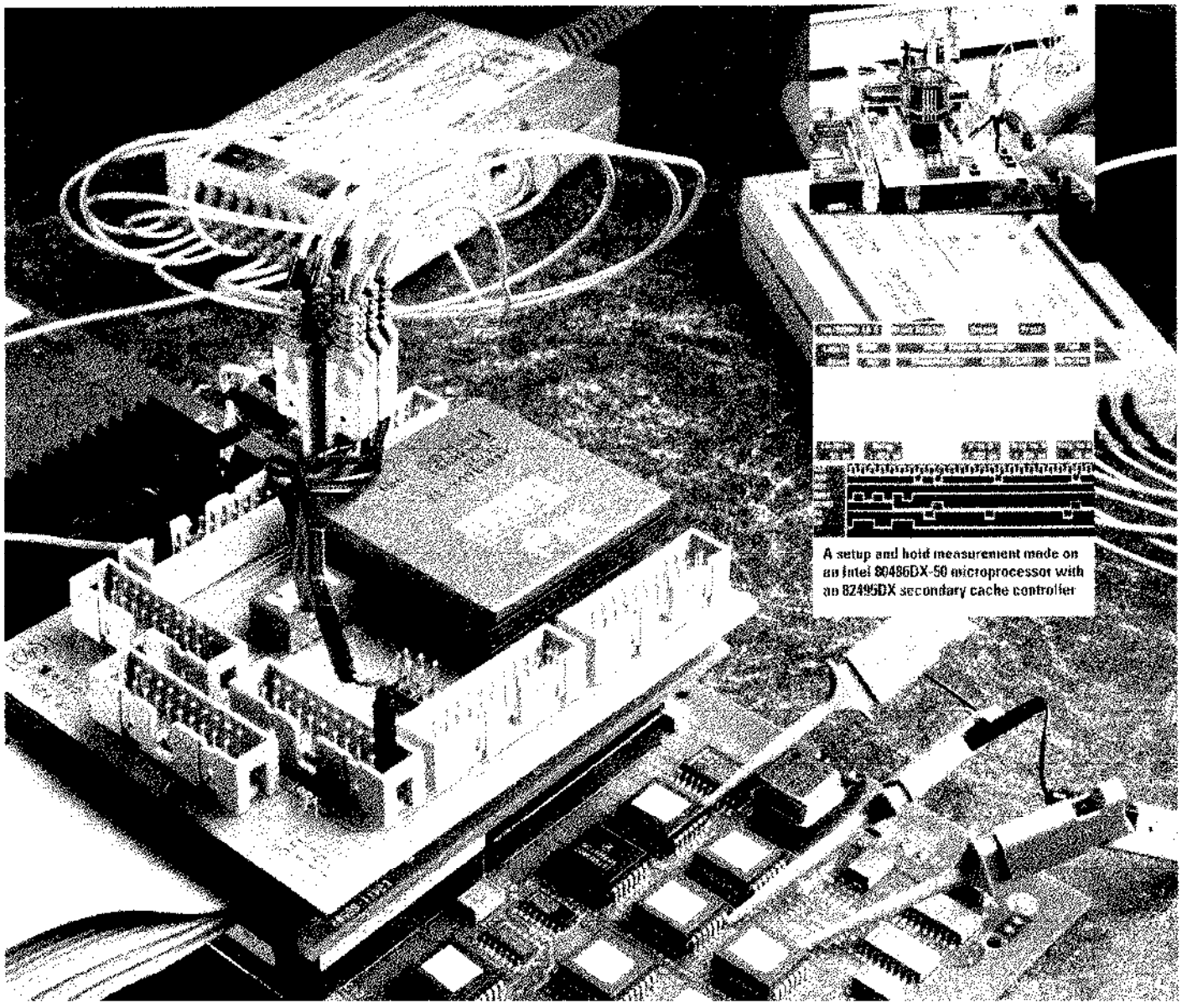
- **200-ps Variable Sample Point**

  Vary the sample point with respect to the external clock edge in 200-ps increments over a ±5 ns range. *Precisely* characterize setup or hold times, across up to 80 channels.

- **Oversampled External Clock**

  Take state traces with the resolution of a timing trace. The oversampled mode allows more than one sample per clock edge, up to a sample rate of 2 GSa/s. This mode provides the functional equivalent of Dual-Analysis-Per-Pin (DAPP).

Flexible probe options allow you to get the measurement you need.



A setup and hold measurement made on an Intel 80486DX-50 microprocessor with an 82495DX secondary cache controller

Memory Depth

- **64K Samples in Full Channel Mode**

  Full channel mode is available in timing and synchronous state mode.

- **128K Samples in Half Channel Mode**

  Half-channel mode is available in the timing mode only. With this memory depth, traces taken at 4 GSa/s are 32.8 μs long.

Advanced Triggering Features

- **Trigger Macro Library**
  Both basic and complex macros are available. Macros can be combined to create custom trigger conditions
- **Easy Trigger Setup**
  A menu with graphics of the measurement and sentence-like structure make triggering easy.
- **True, 500-MHz, 4-level Trigger Sequencer**
  Trigger on complex events with durations as short as 2 ns.
- **4 Pattern Terms**
  Trigger on events occurring across groups of channels up to the full width of the analyzer. The trigger terms and their logical combinations let you identify when to branch and when to trigger.
- **2 Edge Terms**
  In timing mode, use the edge terms to trigger on an asynchronous rising edge, falling edge, or either edge.
- **Timer/ Occurance Counter**
  For each sequence level, trigger when events occur too soon, or when a time-out occurs in a data stream.

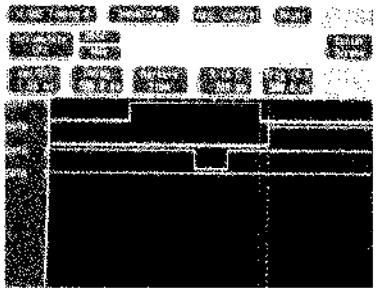
Time-Correlated Measurements Add to the Power of the HP 16517/18A

- **Creating a 160-Channel System Using the HP 16501A**
  Use the intermodule bus to combine two 80 channel HP 16517/18A systems with 2 ns accuracy. Double probe a data line to achieve greater accuracy between the two systems. Display traces from both systems on one screen
- **Establishing Context Using the HP 16550A**
  Use 102 or 204 channels at 4-ns resolution to establish the context of the measurement. Then trigger up to 40 channels at 250-ps resolution on the HP 16517/18A.

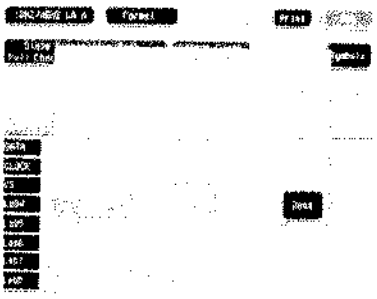
Display Options Help You Identify Interesting System Activity Quickly

In addition to the traditional state listing and timing waveform display modes, the HP 16517/18A provides the following:

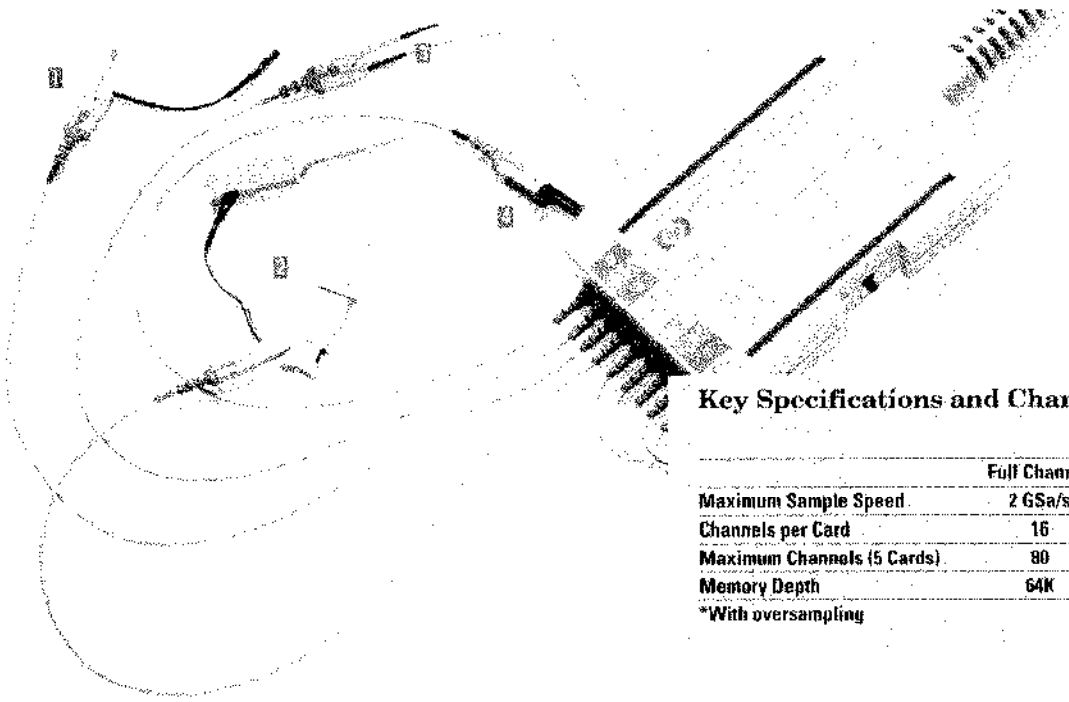
- **State Waveforms**
  View large portions of the state acquisition at a glance.
- **State Compare**
  Find differences between acquisitions automatically.
- **Timing Listing**
  Observe bus values or other timing activity in listing format with time tags.



The Ultimate in Timing Resolution and Accuracy
The 250-ps resolution of this analyzer is only part of the story. An innovative approach, using phase-locked loops, keeps the skew between channels to ±250ps. This accuracy is maintained across all pods and expansion boards, for a total of up to 80 channels.



Characterize Your High-Speed ASIC or Target System
Now, you can speed up the process of making setup and hold time measurements by taking advantage of the high channel count of a logic analyzer. This can be done in one of two ways. First, use the sample point offset of the synchronous state mode to take advantage of the precision of 50-ps increments (using the fine adjustment). Or, second, use the 250-ps resolution of the timing mode.



Key Specifications and Characteristics

	Timing Mode		State Mode
	Full Channel	Half Channel	Full Channel
Maximum Sample Speed	2 GSa/s	4 GSa/s	1 GSa/s, 2 GSa/s*
Channels per Card	16	8	16
Maximum Channels (5 Cards)	80	40	80
Memory Depth	64K	128K	64K

*With oversampling

Probe Accessories:

1. Probe pin with right angle ground
2. 0.05 pitch grabbers
3. SMT tack on signal and ground wire
4. Ground extender

Primary Specifications and Characteristics

Timing Analysis

Sample Period Accuracy	±0.005% of sample period
Channel-to-Channel Skew	250 ps, typical
Time-Interval Accuracy	±(sample period + channel-to-channel skew + 0.01% of time interval reading)

Synchronous State Analysis

Maximum External Clock Frequency	1 GHz
Setup/Hold Time (Internal)	350/350 ps (with deskew) adjustable with sample placement
Sample Placement with Respect to External Clock Edge	±5 ns in 200 ps increments (course adjustment) ±250 ps in 50 ps increments (fine adjustment)
Number of Samples per External Clock	Adjustable in increments of 1, 2, 4, 8, 16, 32
Maximum Sample Rate, with Oversampling	2 GSa/s

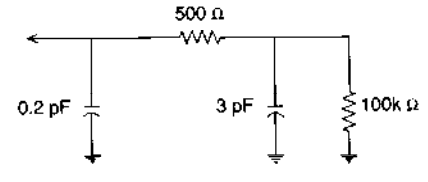
Triggering

Sequencer Speed	500 MHz, maximum
Timing/State Sequence Levels	4
Pattern Recognizers	4
Maximum Channel Width For Patterns	16 – one card 32 – two cards 48 – three cards 64 – four cards 80 – five cards
Edge Recognizers (Timing only)	2
Maximum Channel Width For Edges	16 – one card 32 – two cards 48 – three cards 64 – four cards 80 – five cards
Maximum Number of Recognizers at One Time	4
Timers / Counters	1 per sequence level

Probes

Input dc Resistance	100k Ω, ±2%
Input Impedance	500Ω typical, at 100 MHz through 1 GHz
Input Capacitance	0.2 pF and then, through 500 Ω, 3 pF (see figure 1)
Minimum Voltage Swing	500 mV peak-to-peak
Threshold Range	±5.0 V, adjustable in 10 mV increments

Figure 1



HP 16517/18A Probe load equivalent circuit

Demonstrating Commitment to Meeting Your Evolving Digital Design Needs

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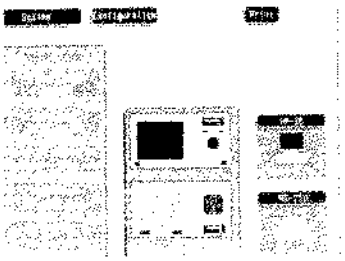
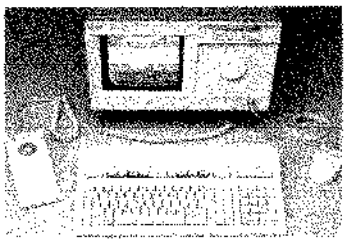
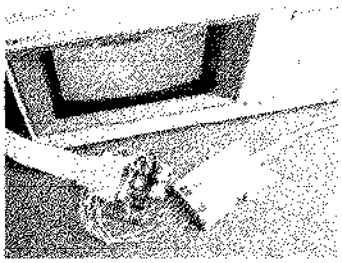


Modularity
HP's modular 16500A/B family lets you configure your mainframe with the modules you need today, while providing you the flexibility to grow with your evolving digital design needs.



Intuitive User Interface
If you are already familiar with one HP Logic analyzer interface, you'll be able to start making measurements right away. An optional keyboard, mouse, or trackball provide you with the most flexible user interface available on any logic analyzer.



Quick-Start Training Kit
Get a quick start making measurements with your logic analyzer. The Quick-Start Training Kit includes an active-circuit target system, a training guide, and software. Several easy-to-understand exercises are designed to improve the productivity of new or intermediate users.

Ordering Information

HP 16517A
4-GHz Timing / 1-GHz Synchronous State
Logic Analyzer Master Module
HP 16518A
4-GHz Timing / 1-GHz Synchronous State
Logic Analyzer Expansion Module
(Requires HP 16517A)
Option AV8
Extra operating and Programming Manuals
Option 110
1-Mbyte or 2.5-Mbyte to 4-Mbyte CPU Upgrade for the HP 16500A mainframe
(Requires 16500A frame)
HP 16500B
Logic Analysis System Mainframe
HP 16500L
Local area network card for 16500B
HP 16500U
Upgrades HP 16500A to an HP 16500B
(Requires 16500A frame)

For more information, call your local HP sales office listed in your telephone directory or an HP regional office listed below for the location of your nearest sales office.

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(301) 670-4300

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(708) 255-9800

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Fullerton, CA 92631
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