
State and Timing Analyzers for the HP 16500C Logic Analysis System

**The HP 16550 series—
depth and performance
to match the needs of the
entire digital design team**



High-performance Features Help You Solve Your Toughest Problems Today

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State Analysis

Up to 110-MHz State Analysis

View system activity at full speed with up to 110-MHz state analysis on all channels.

Full-speed Time or State Counting

Count states or time between samples with 8-ns resolution while acquiring clocked data at rates up to 110-MHz.

Timing Analysis

Up to 500-MHz Conventional Timing Analysis

Verify critical edge times with measurements requiring up to 2-ns timing resolution.

125-MHz or 250-MHz

Transitional Timing Analysis

Analyze timing events that are seconds apart while maintaining 4-ns resolution in half-channel mode, or 8-ns resolution in full-channel mode. Available with the HP 16550A only.

125-MHz Timing Analysis with Glitch Detection

Detect intermittent problems or glitches without reprobing. Capture glitches as narrow as 3.5 ns in half-channel mode. Available with the HP 16550A only.

Wide Channel Count

Up to 340

2 M-Deep Channels

Debug 64-bit microprocessor systems or ASICs, or other applications requiring large channel counts. Connect five HP 16556A or 16556D cards together for measurements requiring up to 340 deep-memory channels. Three HP 16554A, or 16555A or 16555D cards connected together provide 204-deep memory channels. The HP 16555D and HP 16556D provide 2 M of memory depth; the HP 16555A and 16556A provide 1 M memory depth per channel while the HP 16554A is 500 K deep. Trace depth for all cards doubles in half-channel timing mode.

100/500MHz LA E		Listing 1	Invasm	Cancel	Group Run
Markers Pattern	Find 0-pattern	1760	from Trigger	Specify Patterns	

Label>	ADDR	DATA 68040 Mnemonic
Base>	Hex	decimal (\$ = hex) Dequeuing
190	F2000398	MOVE.L #00002C00,(\$00000778,D2.L*8)
191	F200039C	\$00002C00 supr pgm
192	F20003A0	\$2FB00000 supr pgm
193	0000078C	\$F2011A0C supr data write
194	F20003A4	MOVE.L D2,D0
195	F20003A8	ADDQ.L #1,D2
		MOVE.L #\$F2011A12,(\$00000774,D0.L*8)
196	F20003AC	\$F2011A12 supr pgm
197	00000798	\$00002C00 supr data write
198	F20003B0	\$0FB00000 supr pgm
199	F20003B4	MOVE.L #00003000,(\$00000778,D2.L*8)
200	F20003B8	\$00003000 supr pgm
201	F20003BC	\$2FB00000 supr pgm
202	00000794	\$F2011A12 supr data write
203	F20003C0	MOVE.L D2,D0
204	F20003C4	ADDQ.L #1,D2

State Analysis

100/500MHz LA C		Waveform 1	Acq. Control	Print	Run
Accumulate Off	CYCLE	X → DATA READ	Center Screen		
	Symbol	0 → ADDRESS CYCLE			
sec/Div 10 ns	Delay -24.50 ns	Markers Time	X to 0 28.00 ns	Trig to X -19.80 ns	Trig to 0 8.20 ns

PCLK1	
ADDR a11	E00FB888 B0000000
BE a11	0000
DATA a11	E00FB000 +FF 15114444
CYCLE a11	DATA READ ADDRESS CYCLE
ADS	
BLAST a11	LAST XFER
D/C a11	DATA CODE

Timing Analysis

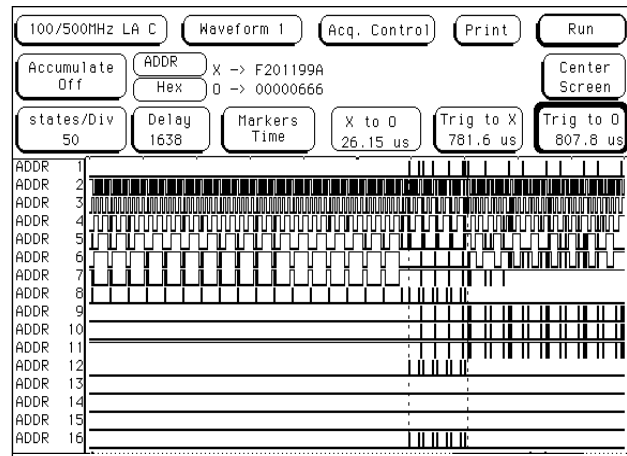
1M SAMPLE LA H		Configuration	Cancel	Run
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Analyzer 1		Analyzer 2		Pods
Name: MACHINE 1	Type: Timing	Name: MACHINE 2	Type: State	
H1: _____ J_	H3: _____ L_			Unassigned Pods
H2: _____ K_	H4: _____ M_			
J1: _____ J_	J3: _____ L_			
J2: _____ K_	J4: _____ M_			
I1: _____ J_	I3: _____ L_			
I2: _____ K_	I4: _____ M_			
G1: _____ J_	G3: _____ L_			
G2: _____ K_	G4: _____ M_			
F1: _____ J_	F3: _____ L_			
F2: _____ K_	F4: _____ M_			

Wide Channel Count

A Variety of Display Options Helps You Identify Problems Quickly

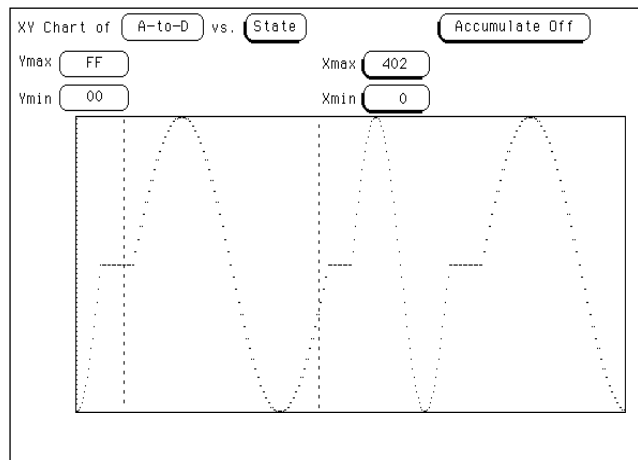
In addition to the traditional state listing and timing waveform display modes, the HP 16550-series also provides state waveforms, state chart, state compare, and timing listings.



State Waveforms:
View the entire state acquisition at a glance.

100/500MHz LA C		Compare 1		Invasm		Print		Run	
Difference listing		Find Error 0		Compare Full		Specify Stop Measurement			
Mask>		*****		*****					
Label>	Time	ADDR	DATA	DATA 66040 Mnemonic					
Base>	Relative	Hex	Hex	decimal (\$ = hex) D					
1732	496 ns	F2000894	4A3029B0	TST.B (\$F201199A,D2.					
1733	552 ns	F2000898	F201199A	\$F201199A supr pgm					
1734	504 ns	F2011990	6F6D0000	\$xx6Dxxxx supr data					
1735	496 ns	F200089C	66E623FC	BNE.B \$F2000884					
				MOVE.L #\$F2000000,\$00					
1736	96 ns	0000065F	0000006D	\$xxxxxx5D supr data					
1737	504 ns	F20008A0	F2000000	\$F2000000 supr pgm					
1738	504 ns	F201199E	6F6D0000	\$xxxx00xx supr data					
1739	496 ns	F20008A4	00000666	\$00000666 supr pgm					
1740	552 ns	F20008A8	74016026	MOVEQ #\$00000001,D2					
				BRA.B \$F20008D2					
1741	96 ns	00000666	0000F200	\$xxxxF200 supr data					
1742	504 ns	F20008AC	2002D080	nu MOVE.L D2,D0					
				nu ADD.L D0,D0					
1743	96 ns	00000668	0000F200	\$0000xxxx supr data					
1744	504 ns	F20008D0	52827014	MOVEQ #\$00000014,D0					

State Compare:
Find differences between acquisitions easily.



State X-Y Chart :
Verify A/D performance or track code flow graphically.

100/500MHz LA D		Listing 1		Cancel		Run	
Markers Time		Trig to X -20 ns		Trig to 0 8 ns		X to 0 28 ns	
Label>	ADDR	DATA	CYCLE	Time	D/C		
Base>	Hex	Hex	Symbol	Absolute	Symbol		
-11	E00F8888	15114444	DATA READ	-44 ns	DATA		
-10	E00F8888	15114444	DATA READ	-40 ns	DATA		
-9	E00F8888	15114444	DATA READ	-36 ns	DATA		
-8	E00F8888	15114444	DATA READ	-32 ns	DATA		
-7	E00F8888	15114444	DATA READ	-28 ns	DATA		
-6	E00F8888	15114444	DATA READ	-24 ns	DATA		
-5	E00F8888	15114444	DATA READ	-20 ns	DATA		
-4	F00F8888	15114444	DATA READ	-16 ns	DATA		
-3	B0000000	15114444	absolute	-12 ns	DATA		
-2	B0000000	15114444	ADDRESS CYCLE	-8 ns	CODE		
-1	B0000000	15114444	ADDRESS CYCLE	-4 ns	CODE		
0	B0000000	15114444	ADDRESS CYCLE	0 ns	CODE		
1	B0000000	15114444	ADDRESS CYCLE	4 ns	CODE		
2	B0000000	15114444	ADDRESS CYCLE	8 ns	CODE		
3	B0000000	15114444	ADDRESS CYCLE	12 ns	CODE		
4	B0000000	15114444	ADDRESS CYCLE	16 ns	CODE		

Timing Listing :
Observe bus values or other timing activities in listing format with time tags.

Advanced Trigger Macros Make It Easy to Capture Elusive Problems

• Trigger Macro Library

Both basic and complex macros are available. The state library includes 11 macros, the timing library 12 macros. You can also combine macros to create custom trigger setups.

• Easy Trigger Setup

Each macro has a graphic of the measurement and a sentence-like structure to make triggering easy. Set up your trigger in terms of the measurement you want to make, rather than the trigger functions in the logic analyzer.

A Large Variety of Trigger Resources Helps You Find Your Most Complex Problems

12-level, up to 125-MHz Trigger Sequencer

Trigger on complex events at full state speed. In timing, trigger on sequences of events as close together as 8 ns.

10 Pattern Terms

Trigger on events occurring across groups of channels up to the full width of the analyzer. Trigger terms and their logical combinations let you identify which states to store, when to branch, and when to trigger. Use extra terms to redefine the trigger conditions quickly.

Two Range Terms

Monitor program and data accesses simultaneously without capturing unneeded states.

Two Timers

Trigger on events that occur too late or too soon, or when a software time-out occurs.

Two Timing Glitch or Edge Terms

In timing, use the glitch/edge terms to trigger on an asynchronous rising edge, a falling edge, either edge, or a glitch (both edges).

Timing Trigger Macro Library		Internal Levels Used
Macro Type	Trigger Macro	
Basic Macros	1. Find any state n times	1
	2. Find pattern present/absent for > duration	1
	3. Find pattern present/absent for < duration	4-5
	4. Find edge	1
	5. Find Nth occ. of an edge	1
Patt/Edge Combos	1. Find edge within a valid pattern	2
	2. Find pattern occurring too soon after edge	3-4
	3. Find pattern occurring too late after edge	2
Time Violations	1. Find 2 edges too close together	3-4
	2. Find 2 edges too far apart	2
	3. Find width violation on a pattern/pulse	4-5

Typical Trigger Macro Library

Sequence Level 1
Find pattern occurring too soon after edge

Find pattern

occurring within after edge

Typical Trigger Macro Screen

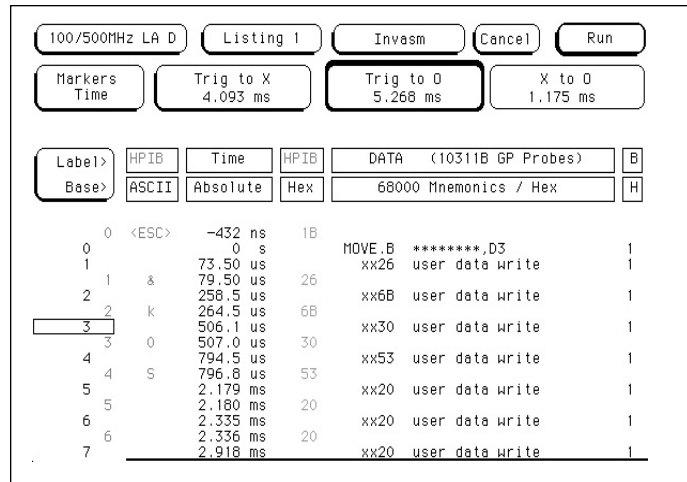
Combined Measurements Bring Together the Full Power of the HP 16500 Modules

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• State/State

Track Problems in Multiprocessor Systems or Between a Processor and Its Interface Bus.

Configure any HP 16550 series card as two independent state analyzers that sample data using separate clocks. Then, view both time-correlated state listings interleaved on the same screen.

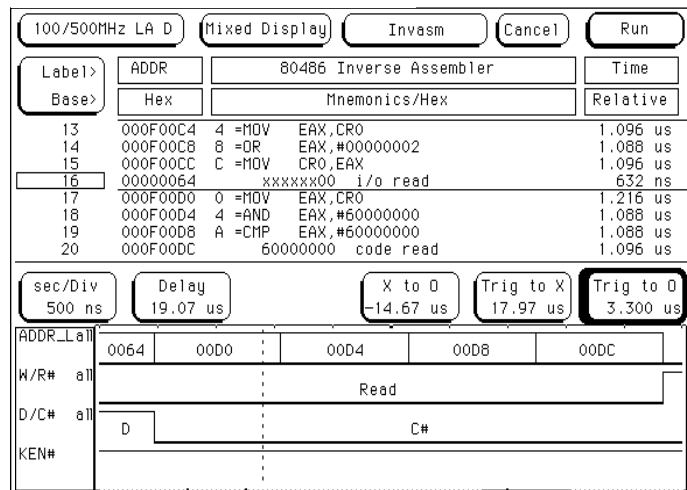


State/State

• State/Timing

Find Whether the Problem is in Software or Hardware

Arm the timing analyzer with the state analyzer to capture system behavior between states. Display both measurements on one screen, and using the time-correlated markers to identify the cause of problem states.

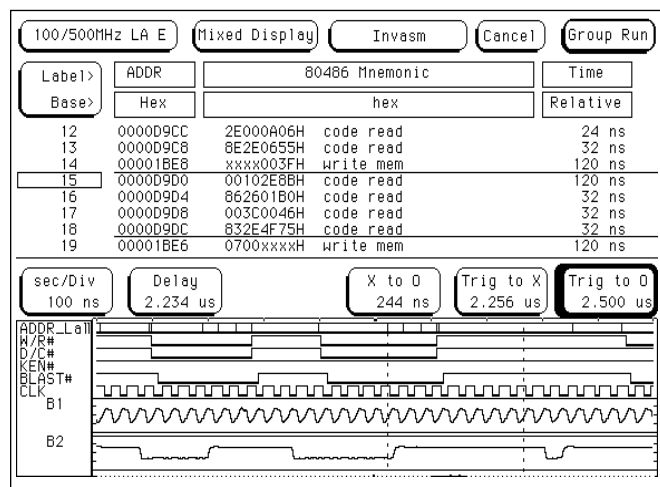


State/Timing

• State/Timing with Oscilloscope

Capture the Analog Behavior of a Signal at the Critical Time

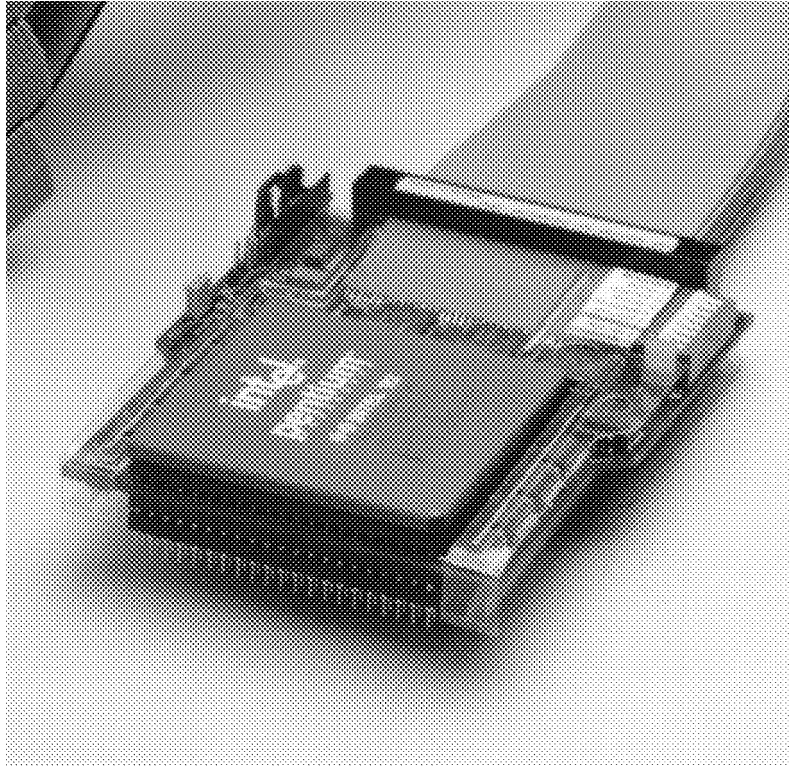
Trigger the 2-GSa/s digitizing oscilloscope from either the state or timing analyzer. Observe relationships among all three time-correlated measurements by displaying them together on the same screen. An HP 16533A or 16534A oscilloscope module is also required for this measurement.



State/Timing with Oscilloscope

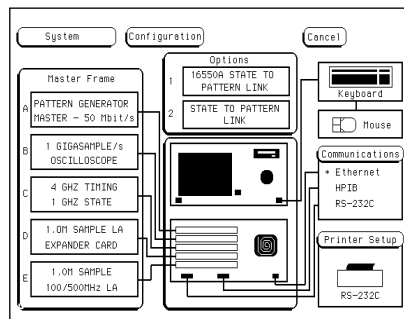
Complete Support for Your CISC or RISC Microprocessor System Analysis Needs

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HP microprocessor adapters are compact in design. This Pentium® adapter provides over 160 signal connections to the logic analyzer.

Meeting Your Evolving Digital Design Needs



Configuration

The HP's modular 16500-series modules let you configure your mainframe with the modules you need today, while providing the room to grow with your evolving digital design needs.

Intuitive User Interface

If you are already familiar with one HP logic analyzer interface, you'll be able to start making measurements right away on HP 16550 logic analyzer modules. A mouse or optional keyboard provides the most flexible user interface available on any logic analyzer.

Broadest Preprocessor Support in the Industry

HP and its Preprocessor Connection program offer the widest range of interfaces for processors and buses. HP is committed to providing support for major new processors at their introduction.

Support for Popular Industry-Standard Buses

- SCSI I, II, and III
- IEEE-448 (HP-IB)
- Universal Serial Bus
- MCA
- PCI
- ISA
- EISA
- FDDI
- RS-232
- VME, VXI
- 72-Pin-SIMM
- PCMCIA
- APIC

Support for Over 180 Processors, Including:

- Intel 80386, 80486, 80860, 80960, Pentium, Pentium Pro
- Motorola 68000, 68020, 68030, 68040, 68360, 68340, 68302, 68332, 5202/03 MCF
- MIPS R4000/4400PC
- AMD AM29000
- Power PC 601, 603, 603e, 604
- SPARC 64801
- TI TMS 320C50/51/52/53, TMS 320c 541/3/6

Start Your High-Performance Measurements Right Away

No Need to Reconfigure

The HP 16550-series automatically translates configuration files from the HP 16510A/B, 16511B, 16550A, 16540A/D, 16541A/D, 1650-series, 1660-series; and 1670-series logic analyzers.

No Need to Relearn

The HP 16550-series uses the same friendly, familiar menus and controls as current HP logic analyzers.

Consistent Probing

The HP 16550-series uses the same probes and accessories as the HP 16510A/B, 16540A/D, 16541A/D, and 16542A, 1650-series, 1660-series, and 1670-series logic analyzers.

	HP 16550A	HP 16554A	HP 16555A	HP 16556A	HP 16555D	HP 16556D
Maximum State Clock Rate	100 MHz	70 MHz	110 MHz	100 MHz	110 MHz	100MHz
Maximum Conventional Timing Rate (1/2 channel)	500 MHz	250 MHz	500 MHz	400 MHz	500 MHz	400 MHz
Maximum Conventional Timing Rate (full channel)	250 MHz	125 MHz	250 MHz	200 MHz	250 MHz	200 MHz
Maximum Transitional Timing Rate (1/2 channel)	250 MHz	N/A	N/A	N/A	N/A	N/A
Maximum Transitional Timing Rate (full channel)	125 MHz	N/A	N/A	N/A	N/A	N/A
Channel Count Per Board	102	68	68	68	68	68
Maximum Channel Count on One Time Base	204	204	204	340	204	340
Memory Depth (full channel)	4 K	500 K	1 M	1 M	2 M	2 M
Memory Depth (1/2 channel)	8 K	1 M *	2 M *	2 M*	4 M*	4 M*

* For the HP 16554A, 16555A, 16555D, 16556A, and 16556D, memory depth doubles in timing mode only.

Supplemental Characteristics

Probes		Channel-to-Channel Skew	
Input Resistance	100 k Ω $\pm$ 2%	2 ns, typical	
Input Capacitance	~8 pF	Time Interval Accuracy	
Minimum Voltage Swing	500 mV peak-to-peak	$\pm$ (sample period + channel-to-channel skew + 0.01% of time interval reading)	
Threshold Range	$\pm$ 6.0 V adjustable in 50-mV increments	Minimum Detectable Glitch	
State Analysis		Triggering	
Setup/Hold Time [1]	0/3.5 ns through 3.5/0 ns, adjustable in 500-ps increments	Sequencer Speed	
Minimum State Clock Width	3.5 ns	125 MHz, maximum (HP 16550A,16554A, 16555A, 16555D)	
State Clock/Qualifiers	6 (HP 16550A) 4 (HP 16554A, HP 16555A, HP 16555D, HP 16556A, and HP 16556D)	100 MHz, maximum (HP 16556A,16556D)	
Time Tag Resolution [2]	8 ns	State Sequence Levels	
Maximum Time Count Between States	34 seconds	12	
Maximum State Tag Count [2]	4.29×10^9 states	Timing Sequence Levels	
Timing Analysis		10	
Sample Period Accuracy	0.01% of sample period	Maximum Occurrence Counter	
		1,048,575	
		Pattern Recognizers [3]	
		10	
		Range Recognizers	
		2	
		Range Width	
		32 bits each	
		Timers	
		2	
		Timer Value Range	
		400 ns to 500 seconds	
		Glitch/Edge Recognizers	
		2 (timing only)	

[1] Minimum setup/hold time specified for single-edge, single-clock acquisition. Single-clock, multi-edge setup/hold window is 4.0 ns. Multiclock, multi-edge setup/hold window is 4.5 ns. All setup/hold windows are adjustable in 500-ps increments.

[2] Maximum state clock rate with or without time or state tags on is 100 MHz (HP 16550A, HP 16556D, and 16556A), 70 MHz (HP 16554A), and 110 MHz (HP 16555A, and 16555D). When all pods are assigned to a state or timing machine, enabling time or state tags cuts memory in half.

[3] Eight pattern recognizers are available in HP 16554A timing modes and in HP 16555A/D timing and 110-MHz state analysis modes.

Ordering Information

HP 16550A

4 K Sample, 100-MHz state/500-MHz timing logic analyzer module

HP 16554A

500 K-Sample, 70-MHz state/250-MHz timing logic analyzer module
(Requires an HP 16500B or 16500C mainframe)

HP 16555A

1 M-Sample, 110-MHz state/500-MHz timing logic analyzer module
(Requires an HP 16500B or 16500C mainframe)

HP 16555D

2 M-Sample 110-MHz state/500-MHz timing logic analyzer module (Requires an HP 16500B or HP 16500C mainframe)

HP 16556A

1 M-Sample, 100-MHz state/400-MHz timing logic analyzer module
(Requires an HP 16500B or 16500C mainframe)

HP 16556D

2 M-Sample 100-MHz state/400-MHz timing logic analyzer module (Requires an HP 16500B or HP 16500C mainframe)

HP 16500C

Logic Analyzer System mainframe

HP 16505A

Prototype Analyzer System

HP B4600A

System Performance Toolset

HP B4620

Software Analyzer Toolset

HP E2479A

Upgrades an HP 16500A or 16500B mainframe to an HP 16500C mainframe

For more information on Hewlett-Packard Test & Measurement products, applications or services please call your local Hewlett-Packard sales offices. A current listing is available via Web through Access HP at <http://www.hp.com>. If you do not have access to the internet please contact one of the HP centers listed below and they will direct you to your nearest HP representative.

United States:

Hewlett-Packard Company Test and Measurement Organization
5301 Stevens Creek Blvd.
Bldg. 51L-SC
Santa Clara, CA 95052-8059
1 800 452 4844

Canada:

Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
(905) 206 4725

Europe:

Hewlett-Packard
European Marketing Centre
P.O. Box 999
1180 AZ Amstelveen
The Netherlands

Japan:

Hewlett-Packard Japan Ltd.
Measurement Assistance Center
9-1, Takakura-Cho, Hachioji-Shi,
Tokyo 192, Japan
Tel: (81-426) 48-0722
Fax: (81-426) 48-1073

Latin America:

Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive
9th Floor
Miami, Florida 33126
U.S.A.
(305) 267 4245/4220

Australia/New Zealand:

Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
1 800 629 485

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Hewlett-Packard Asia Pacific Ltd
17-21/F Shell Tower, Times Square,
1 Matheson Street, Causeway Bay,
Hong Kong
Fax: (852) 2506 9285