HEWLETT PACKARD

# HP E1430A
# 10 MSample/sec ADC, with Filtering and Memory

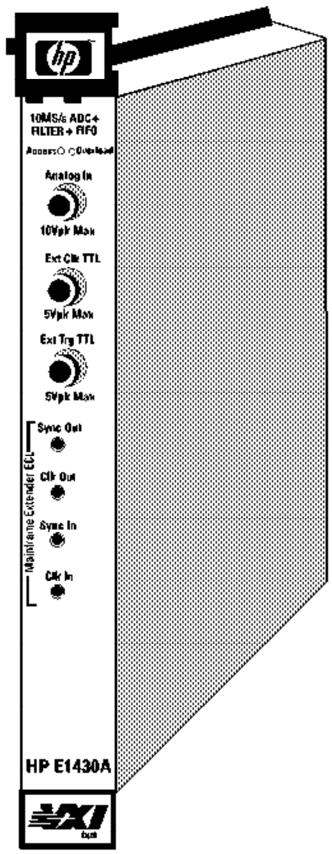
## Technical Data

The HP E1430A is more than a digitizer, it is a complete A/D module. Included with its low distortion, low noise, analog-to-digital converter is flexible input signal conditioning, alias protection, tunable digital filtering, a deep FIFO memory and a choice of high-speed interfaces.

**A remarkable A/D**

Whether you analyze spectrums or capture transients, digitize IFs or record waveforms, at audio frequencies or baseband, the quality of your measurement starts with the quality of your analog-to-digital conversion. The digitizer in the HP E1430A uses a combination of dithering and an extraordinary on-the-fly distortion correction technique to produce up to 18 bits (110 dBFS) of distortion-free, spur-free, dynamic range. Low distortion digitizing means higher quality data—data that will reveal even more about the signal when averaged, filtered, or FFT'd.

The HP E1430A also has low noise. Low noise means better resolution on single-shot events and less processing to resolve the signal on repetitive events. For the HP E1430A the noise density is as good as -136 dBFS/Hz. The sensitivity on the lowest input range is -160 dBm/Hz. The noise figure is 14 dB.




**Alias protection**

Use the HP E1430A for spectrum analysis. Its built-in 4-MHz anti-alias filter is ideal for the Nyquist (2X highest frequency of interest) sampling common to that analysis. Alias filtering also limits the noise bandwidth of the input giving lower noise time-domain data as well. And, if you need the fastest rise times possible you can switch the filter out.

- **18-bit (110 dBFS) spur-free dynamic range**
- **Alias protection**
- **Tunable digital filtering**
- **8 Mbyte FIFO memory**
- **Up to 25 MByte/sec data transfer rate**
- **Internal or external clock**

**Digital filtering**

Sometimes you must narrow in on a signal to exclude unwanted signals or noise. The HP E1430A features multiple digital filters, with decimation, and a digital LO.

Filter bandwidths range from 4 MHz to 0.24 Hz, in octave steps. After the data is filtered, it is decimated, halving the effective sample rate while maintaining alias-protected Nyquist sampling. This means you get the best of both worlds, digital filtering to exclude unwanted signals, and alias-protected Nyquist sampling, the most data-efficient form of digitizing.

Tune the digital LO to center any of the digital filters on your signal of interest to maximize rejection of unwanted signals. Tune the center frequency of the filters anywhere in the 4-MHz input range of the module with 10 µHz resolution. Both the I and Q data is output from the filters and is available for processing by the user.

**Sample rate control**
A built-in temperature compensated 10-MHz crystal oscillator provides precise sample timing. An optional 10.24-MHz clock (opt AYD) is available for applications requiring the sample rate to be an exact power of 2.

Use the digital filter/decimation capability to reduce the sample rate. This feature reduces the effective sample rate in factor-of-2 steps from 5.0 MHz to 0.47 Hz.

If finer control of the sampling rate is needed an external clock input is available to accept an external sampling clock. And, multiple HP E1430A's can be connected to sample synchronously.

**Signal conditioning for flexibility**
Signal conditioning for flexible AC/DC coupling and 11 attenuation/gain ranges protect the digitizer, letting you digitize a wide range of signal amplitudes.

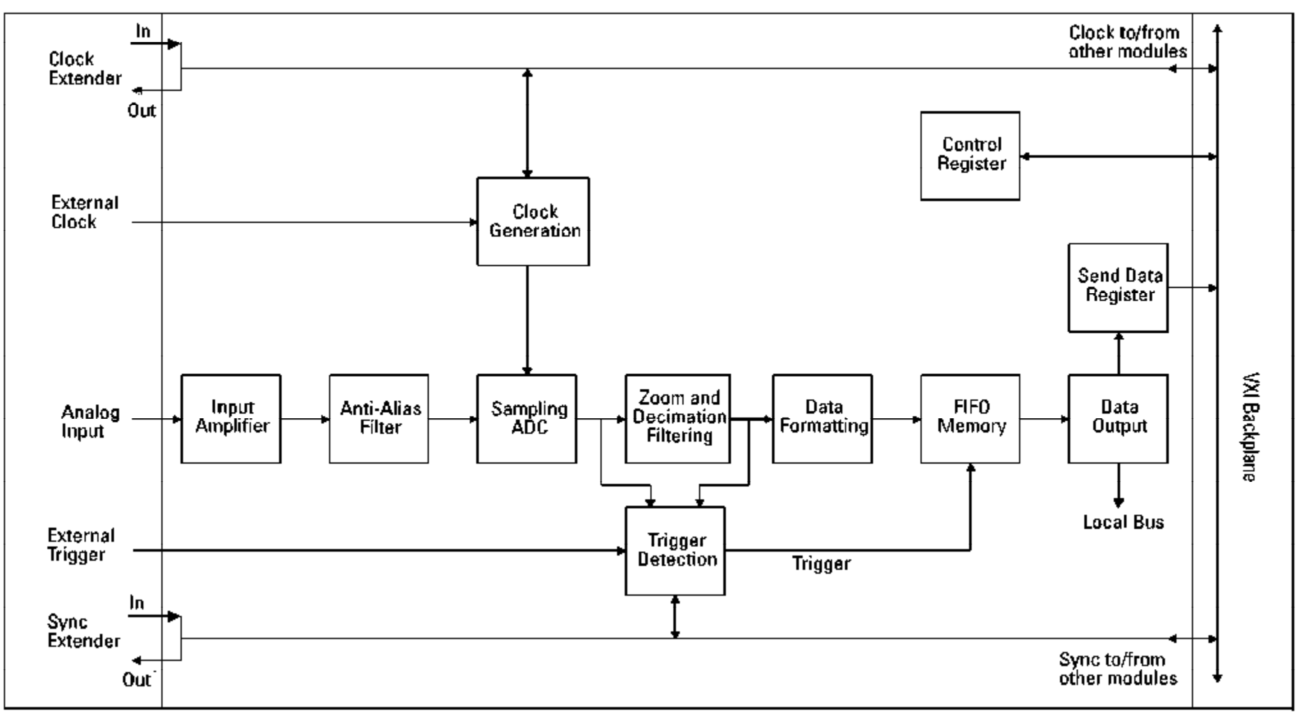
**Memory for signal capture**
A high-speed, 8-Mbyte FIFO memory can be used to capture signals. Use the FIFO feature to store new data while old data is being read out, ensuring gap free data.

**Local Bus for highest speed data transfer**
Transfer data off the module over VXI's VME bus or use the high-speed Local Bus. Over the Local Bus the HP E1430A can transfer blocks of data out at rates up to 40 MBytes/sec.

**Programming**
Program the HP E1430A from VEE and ITG using the pre-programmed drivers that come with VEE. Or, for the highest speed control and data transfers, program the HP E1430A's registers directly. A library of C functions is provided to simplify user program development. Filter correction functions are included as well. Source code is included to allow user modification, recompilation to a different target computer, and to provide examples of register programming.

**Summary**
When high-resolution, low-distortion, robust data is the key, when signal conditioning, filtering, on board memory and fast data transfers are a must, the HP E1430A is the answer to your digitizing needs.

**HP E1430A Block Diagram**



# Specifications

Specifications describe warranted performance over the temperature range of 0° to 55° C (except where noted) and include a 30-minute warm-up from ambient conditions and automatic calibrations enabled unless otherwise noted. Supplemental characteristics, identified as "typical" or "characteristic," provide useful information by giving non-warranted performance parameters. Typical performance is applicable over ±5° C from the temperature during the most recent measurement calibration and is not warranted.

## Analog Input

### Input Modes

DC coupled, AC coupled, grounded; Single-ended, differential

### Input Ranges

**Input voltage ranges** (clipping voltages):

| | |
|---|---|
| ±8 Vpk (28 dBm) | ±0.125 Vpk (-8 dBm) |
| ±4 Vpk (22 dBm) | ±62.5 mVpk (-14 dBm) |
| ±2 Vpk (16 dBm) | ±31.25 mVpk (-20 dBm) |
| ±1 Vpk (10 dBm) | ±15.625 mVpk (-26 dBm) |
| ±0.5 Vpk (4 dBm) | ±7.8125 mVpk (-32 dBm) |
| ±0.25 Vpk (-2 dBm) | |

**Maximum input voltage without damage:**
8 VRMS for any time interval > 10 ms

### Input Impedance

50 Ω ±1% DC; > 40 dB return loss to 4 MHz;
DC coupled or grounded modes only

### AC Coupling

In AC coupled mode, a 0.2 µF ±10% capacitor is placed in series with the input signal. Maximum DC voltage without damage is ±50 V when AC coupling is used.

### Common Mode Characteristics

**Impedance to chassis ground:**
47 Ω ±10% in parallel with 0.04 µF ±10%, differential input mode; < 0.1 Ω, single-ended input mode
**Maximum common mode current without damage:**
±1 Amp peak; diode clamped to < ±1 V peak
**Common mode response:**
$< (-90 + 20 \times \mathrm{LOG}(V_{com}))$ dBfs, range ≥ 125 mV
$< (-80 + 20 \times \mathrm{LOG}(V_{com}))$ dBfs, range = 62.5 mV
$< (-65 + 20 \times \mathrm{LOG}(V_{com}))$ dBfs, range ≤ 31.25 mV

**Note:** The common mode source for these characteristics is a sine wave voltage source of Vcom mV applied through a 50 Ω series resistor. The characteristics apply for source frequencies < 4 MHz.

## Accuracy

### Resolution

**Raw ADC resolution:**
23 bits, two's complement
**After digital zoom and filter operations:**
32 bits, full resolution mode;
16 bits, reduced resolution mode

### Amplitude Accuracy

**Absolute voltage measurement accuracy:**
±0.03 dB ( < 100 kHz, ±1 V input range, 25° C, analog alias filter on, digital decimation filters off, DC coupled)
**Range accuracy** (relative to ±1V range):
±0.03 dB (for all ranges), < 100 kHz
**Alias filter off mode:**
±0.02 dB relative to alias filter on mode, 12 kHz
**Temperature drift:**
< 0.001dB per ° C of deviation from 25° C

### DC Offset

**Programmable DC offset:**
Resolution: < 0.05% of input range clipping voltage
Range (minimum): ±50% of input range clipping voltage, range ≥ 62.5 mV
**Input bias current:**
< 64 µA (in parallel with 50 Ω input load)
**DC offset voltage vs temperature** (% of clipping voltage):
< ±0.01% / ° C for 62.5 mV and higher ranges;
< ±0.1% /° C for ranges < 62.5 mV

## Dynamic Range

**Note:** If you reset the HP E1430A, and your application depends on the dynamic range specifications, allow at least 20 seconds after the reset for the ADC correction to settle before beginning your measurement.

### Signal-to-Noise Ratio

The reference signal is a sine wave with peaks at the clipping voltage of the current range.

**Alias filter on:**
70 dB, range ≥ 62.5 mV; 62 dB, range ≤ 31.25 mV
**Alias filter off:**
66 dB, range ≥ 62.5 mV; 53 dB, range ≤ 31.25 mV

**Input Noise Density**
(Alias filter on, ADC sample clock ≥ 10 MHz)

**Range ≥ 62.5 mV:**
–136 dBfs/Hz, f > 100 kHz
–134 dBfs/Hz, 10 kHz ≤ f < 100 kHz
–130 dBfs/Hz, 2 kHz ≤ f < 10 kHz
(–97–10 × LOG(f)) dBfs/Hz, f < 2 kHz
**Range ≤ 31.25 mV:**
–127 dBfs/Hz, f ≥ 200 kHz
–122 dBfs/Hz, 20 kHz < f < 200 kHz
(–79–10 × LOG(f)) dBfs/Hz, f < 20 kHz

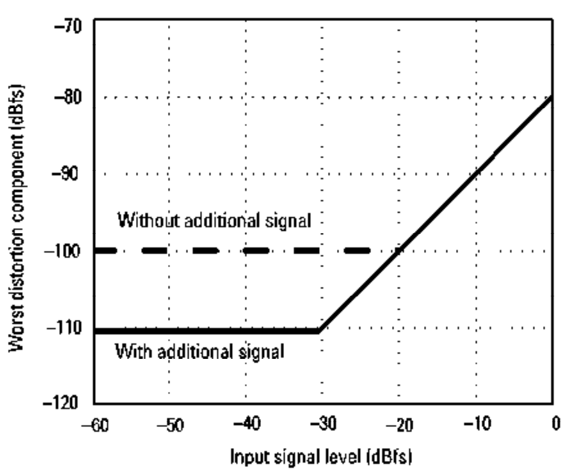
**Spurious Signals**
(Between 0 to 4 MHz;
terminated with 50 Ω at input connector)

< –110 dBfs, alias filter on, DSP clock = ADC clock
< –95 dBfs, alias filter on, DSP clock ≠ ADC clock
< –70 dBfs, alias filter off, DSP clock = ADC clock

**Distortion**
Includes aliased distortion components

**Harmonic distortion:**
< –80 dBc or < –110 dBfs,
with additional signal applied > –20 dBfs
< –80 dBc or < –100 dBfs, without other signals applied
**Intermodulation** (two tones each at –6 dBc):
< –80 dBc or < –110 dBfs,
with additional signal applied > –20 dBfs
< –80 dBc or < –100 dBfs, without other signals applied

**Distortion vs Input Signal**




**Phase Noise**
$F_{in}$ < 4 MHz, vibration < 0.01G

**Phase noise density** (single sideband power density):
< –128 dBc/Hz, Δf = 100 Hz
< –122 dBc/Hz, Δf = 50 Hz
< –92 dBc/Hz, Δf = 5 Hz
**Discrete sidebands** (5 Hz < Δf < 1 MHz):
< –110 dBc, internal clock
< –80 dBc, internal clock distributed on backplane

**Note:** The sideband specification for the backplane-distributed clock requires that all modules in the mainframe comply with the VXI 1.4 specification for ECL trigger lines; and that the 10-MHz VXI system clock be turned off. External clock input must be disconnected when not being used for ADC clock.

## Clock

**Clock I/O Connections**

**External ADC clock input: (ExtClk):**
BNC input compatible with TTL, ECL, and > – 6 dBm sine waves. AC coupled with input impedance of 1k Ω above 10 kHz. ±10 V absolute maximum input without damage
**Clock extender input:**
ECL-10K compatible, 50 Ω termination to –2V, SMB, –7 V to + 0.5 V without damage
**Clock extender output:** ECL-10K compatible, SMB
**Sync extender input:** ECL-10K compatible,SMB, –7V to +0.5 V without damage
**Sync extender output:** ECL-10K compatible, SMB

**Clock sources**

**ADC clock:**
Internal 10-MHz clock (optional 10.24 MHz)

External clock, BNC input (the external clock frequency must be > 100 kHz if the DSP clock is the ADC clock, and must be < 4.9 MHz if the DSP clock is internal)

ECL clock, SMB input

**DSP clock:**
Internal 10-MHz clock (optional 10.24 MHz)
ADC clock (ADC clock must be > 100 kHz in this mode)

**Internal Clock**

**Frequency:** 10 MHz (optional 10.24 MHz)
**Accuracy:** ±70 Hz, 0° C to 40° C
**Jitter** (typical): < 10 ps RMS, 1s interval (see phase noise specification for spectral content of jitter)

**Sampling skew (typical)**

**Within mainframe:** 5 ns
**Between mainframes:** 20 ns, clock extended via a 1-M coaxial cable

# Trigger

### Trigger Sources

External TTL
Level
LOG(Magnitude)
Software (via register write)

### Slope

Positive/negative

### Threshold

**Level Trigger:**
$V_{range} \times N/128$, $-128 \le N \le 128$; hysteresis is $V_{range}/32$
**LOG(Magnitude) Trigger:**
$V_{range}$(dBm) – $N \times 0.375$ dBm,
$0 \le N \le 255$; hysteresis is 1.5 dB

### External Trigger Input

TTL, BNC, ± 10 V absolute maximum input without damage

### Trigger Offset

**Resolution (in output sample periods):**
1 sample, 32-bit complex data
2 samples, 16-bit complex or 32-bit real data
4 samples, 16-bit real data
**Maximum pre-trigger delay:**
1,048,575 × trigger offset resolution
**Maximum post-trigger delay:**
8,388,607 × trigger offset resolution

# Programming

# Filtering

### Total Frequency Response

Total frequency response is:

$$H(f) = H_{analog}(f) \times H_{digital,N}\left(\frac{f-f_0}{f_s}\right)$$

where:
f = input signal frequency
$f_0$ = zoom center frequency (zero in baseband mode)
$f_s$ = ADC sampling frequency (10 MHz with standard internal clock)
N = digital filter bandwidth selector N = 0, 1, 2, ..., 24

### Analog Frequency Response ($H_{analog}$)

**Analog Flatness** (peak to peak):
Alias filter on:
03 dB, f ≤ 100 kHz; 0.25 dB, f ≤ 2.5 MHz; 0.8 dB, f ≤ 4 MHz
Alias filter off:
0.25 dB, f ≤ 4 MHz; 3 dB nominal, f = 20 MHz
**Stopband rejection:** 100 dB, f > 6 MHz, alias filter on

### Analog Frequency Response Function

(nominal), with alias filter off

$$H_{analog}(f) = \left. \frac{1}{(1-s/c_0)\prod_{n=1}^{2}[(1-s/c_n)(1-s/c_n^*)]} \right|_{s=j2\pi f}$$

| n | $c_n/2\pi$ |
|---|---|
| 0 | 20 MHz |
| 1 | 40 + j × 52 MHz |
| 2 | 50 + j × 120 MHz |

### Analog Frequency Response Function

(nominal), with alias filter on

$$H_{analog}(f) = \left. \frac{\prod_{n=1}^{5}[(1-s/a_n)(1-s/a_n^*)]}{(1-s/b_0)\prod_{n=1}^{5}[(1-s/b_n)(1-s/b_n^*)]} \right|_{s=j2\pi f}$$

| n | $a_n$ (Radians/sec) | $b_n$ (Radians/sec) |
|---|---|---|
| 0 | | $-8.2909964 \times 10^6$ |
| 1 | $j3.4904432 \times 10^7$ | $-7.5372809 \times 10^6 + j9.0528495 \times 10^6$ |
| 2 | $j3.7024164 \times 10^7$ | $-5.7386094 \times 10^6 + j1.6425689 \times 10^7$ |
| 3 | $j4.2617433 \times 10^7$ | $-3.7379055 \times 10^6 + j2.1470763 \times 10^7$ |
| 4 | $j5.6601087 \times 10^7$ | $-2.0233064 \times 10^6 + j2.4424917 \times 10^7$ |
| 5 | $j1.0424240 \times 10^8$ | $-6.3191539 \times 10^5 + j2.5754323 \times 10^7$ |

### Digital Filter Response ($H_{digital}$)

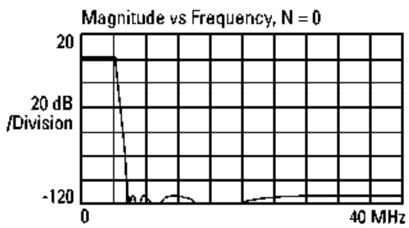
**Amplitude flatness** ($1 \le N \le 24$):
+ 0/–0.23 dB, $|f-f_0| < 0.36 \times fs/2^N$
**Stopband rejection** ($1 \le N \le 24$):
> 111 dB, $|f-f_0| < 0.64 \times fs/2^N$

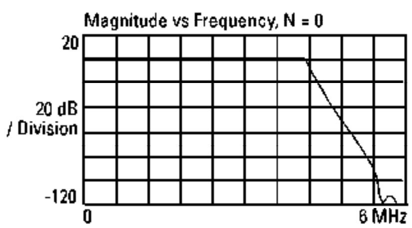
**Frequency Response Function:**

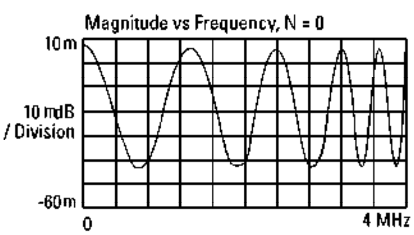
$$H_{digital,N}\left(\frac{f-f_0}{f_s}\right) = \begin{cases} 1, & N = 0 \\ \left.\prod_{n=1}^{N}\left(\frac{z^3+2z^2+2z+1}{4z^3+2z}\right)^5\right|_{z=e^{j2^n\pi(f-f_0)/f_s}}, & N > 0 \end{cases}$$

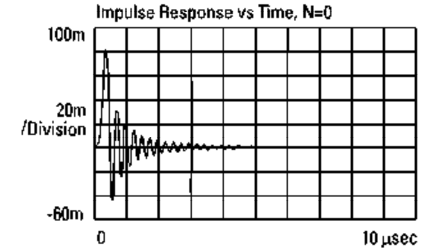
## Filter characteristics for nominal 4-MHz analog anti-alias filter

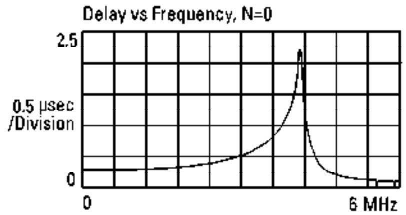
The following graphs are derived from the analog frequency response function on page 5. They describe the behavior of the 4-MHz analog anti-alias filter located between the ADC and the input connector on the E1430A. All other filters are disabled. Three frequency versus magnitude response curves are provided: Broadband (0 to 40 MHz), Medium band (0 to 6 MHz) and Narrowband (0 to 4 MHz). Graphs for phase delay, step response and impulse response are also provided. The second graph of the impulse and step responses shows the deviation of the absolute value of the response from its final value in dB. That is, the step response will settle to within 0.1% (-60db) of its final value in 6.4 µsec.

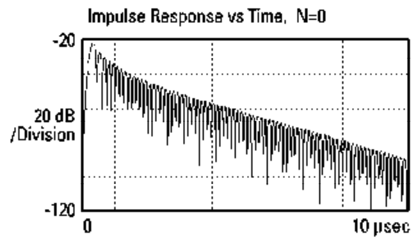


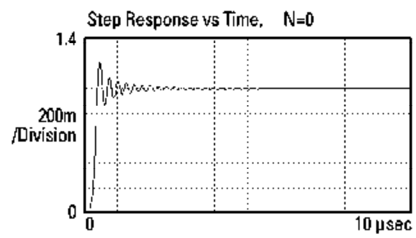



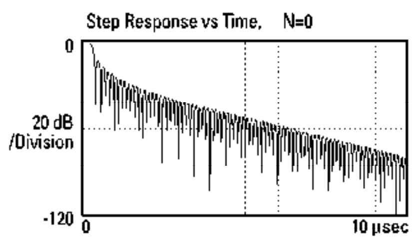



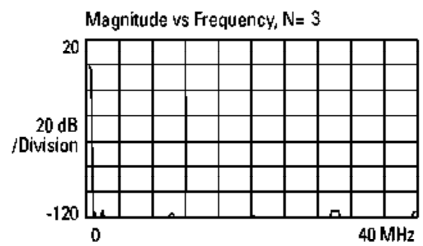



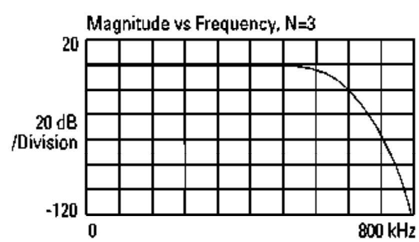



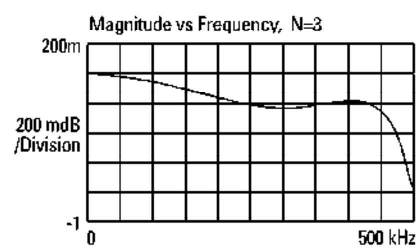




## Filter characteristics for 500-kHz digital filter and analog anti-alias filter

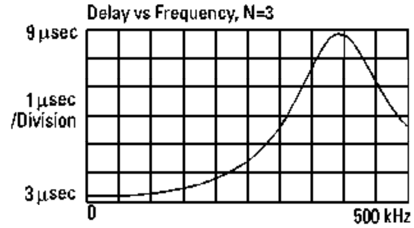
The following graphs are derived from the frequency response functions on page 5. These graphs show the combined response of the 4-MHz analog anti-alias filter that precedes the ADC and the 500-kHz digital filter that follows the ADC. The responses are dominated by the 500-kHz filter. The shape of the responses is typical of the E1430A digital filters and can be used to estimate the behavior of the < 500-kHz digital filters. Three frequency versus magnitude response curves are provided: Broadband (0 to 40 MHz), Medium band (0 to 800 kHz) and Narrowband (0 to 500 kHz). Graphs for phase delay, step response and impulse response are also provided. The second graph of the impulse and step responses shows the deviation of the absolute value of the response from its final value in dB. That is, the step response will settle within 0.1% (-60dB) of its final value in 16 µsec.



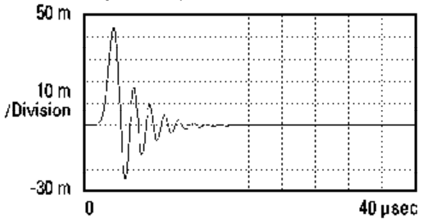



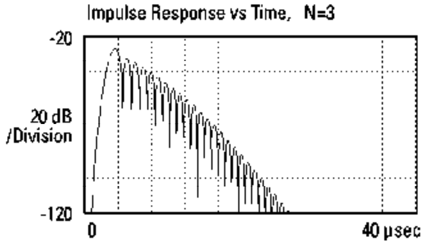
Delay vs Frequency, N=3



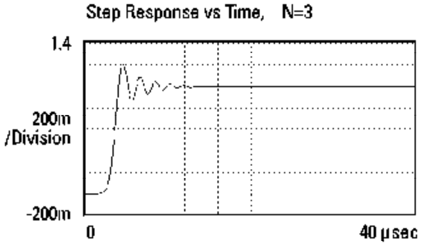

Impulse Response vs Time, N=3



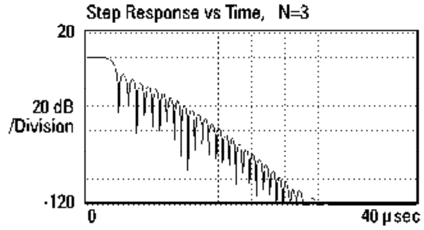

Impulse Response vs Time, N=3




Step Response vs Time, N=3



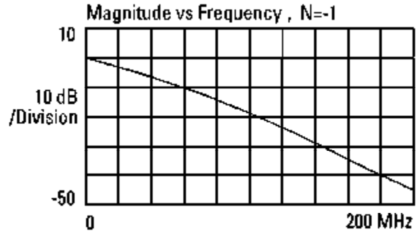

Step Response vs Time, N=3



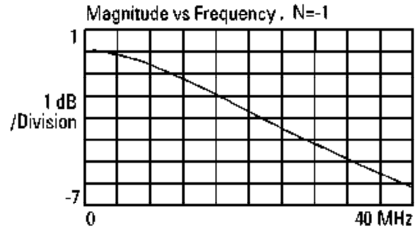

## Filter characteristics with all filtering off (based on an approximate model)

The following graphs are derived from an approximate model of the ADC frequency response when all filters, including the analog anti-alias filter, are switched off. Three frequency versus magnitude response curves are provided: Broadband (0 to 200 MHz), Medium band (0 to 40 MHz) and Narrowband (0 to 4 MHz). Graphs for phase delay, step response and impulse response are also provided. The second graph of the impulse and step responses shows the deviation of the absolute value of the response from its final value in dB. That is, the step response will settle to within 0.1% (-60dB) of its final value in 58 nsec.

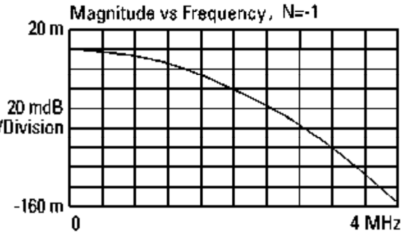
Magnitude vs Frequency , N=-1



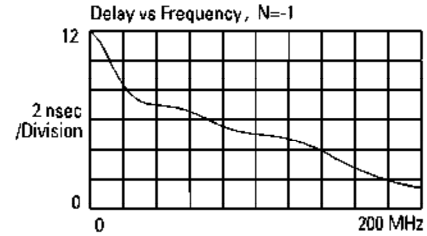

Magnitude vs Frequency , N=-1



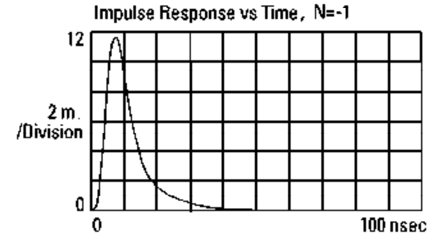

Magnitude vs Frequency , N=-1



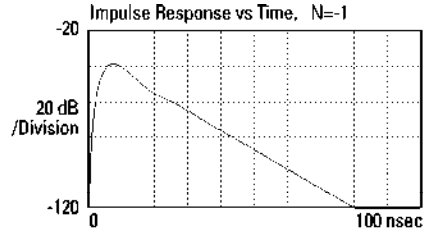

Delay vs Frequency , N=-1



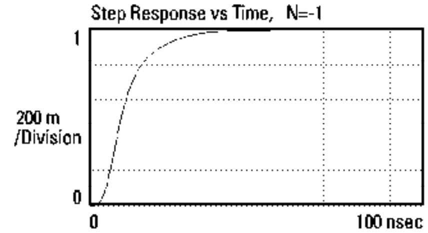

Impulse Response vs Time , N=-1



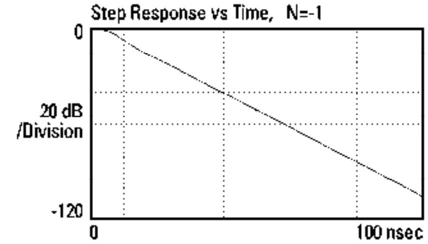

Impulse Response vs Time, N=-1




Step Response vs Time, N=-1




Step Response vs Time, N=-1



All functions are programmable via the VXI register interface.

**Center Frequency**

**Resolution:** ADC clock frequency ÷ (1024 × 109)

**Range:** ± ADC clock frequency ÷ 2

**Filtering and Decimation**

**Bandwidths** (-15 dB):

± 0.5 × $Fs/2^N$, 1 ≤ N ≤ 24 (See the frequency response section for filter characteristics)

**Output sample rate:**

$Fs/2^N$ (Nyquist sampled), 2 × $Fs/2^N$ (2X over-sampled)

**Data Output**

**Formats:** real, complex

**Resolution:** 16 bits, 32 bits

**Output Ports:**

VME data transfers; Local Bus data transfers

**Transfer rate:**

40 Mbyte/s, local bus, block mode

20 MByte/s, local bus, continuous mode

3 MByte/s, VME

**Block sizes:** 8, 16, 32, ..., 8388608 bytes

**Measurement modes**

Block mode (individually triggered blocks); continuous mode

**Information Available in Read Registers**

**Manufacturer's Code:** 4095 Decimal (Hewlett-Packard)

**Model Code:** 0454 Decimal (E1430A)

**Other:** Logical address, status, measurement loop state, data

**Status bits:** Data word ready, data block available, armed, measurement done, overload, ADC error

**Interrupts**

Two independent priority interrupts initiated by masked status bits.

**Memory**

8 Mb (4 MSamples, 16 bit), FIFO

## General

**Standards Compliance**

VXI (Rev. 1.4); Register based; A16/D16

**Power Required**

**DC voltage/current:**

+5 V / 4.2 A, –5.2 V / 4.2 A, -2V / 0.3 A, +12 V / 0.3 A, –12 V / 0.1 A

**Dynamic current:**

+5 V / 0.5 A, –5.2 V / 0.2 A, –2 V / 0.1 A, +12 V / .05 A, –12 V / .02 A

**Size**

Single slot, C-size VXI module

**Dimensions:**

14 inches deep, 9.2 inches high, 1.2 inches wide (approx. 36 cm deep, 23 cm high, 3 cm wide)

**Weight:**

3.9 pounds (approx. 1.8 kg)

**Environmental**

**Temperature**

**Operating:** 0° to 55° C

**Storage:** –20° to 65° C

**Humidity, non-condensing**

**Operating:** 10% to 90% at 40° C

**Storage:** 10% to 90% at 40° C

**Altitude**

**Operating:** 4600 m (15,000 ft)

above 2285 m (7500 ft), derate operating temperature by –3.6° C per 1000 m (–1.1° C per 1000 ft)

**Storage:** 4600 m (15,000 ft)

**Calibration interval:** 1 year

**Warm-up time:** 1 minute

**Data subject to change.**

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