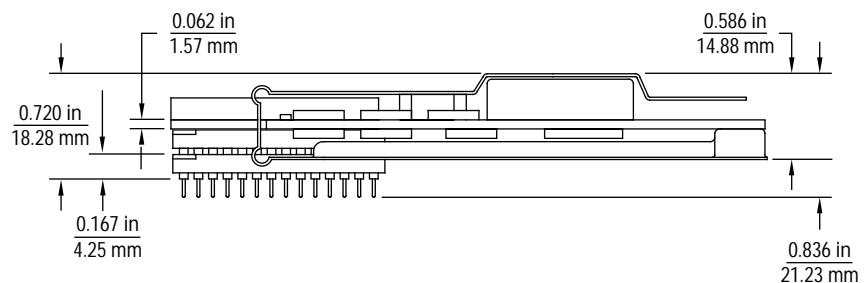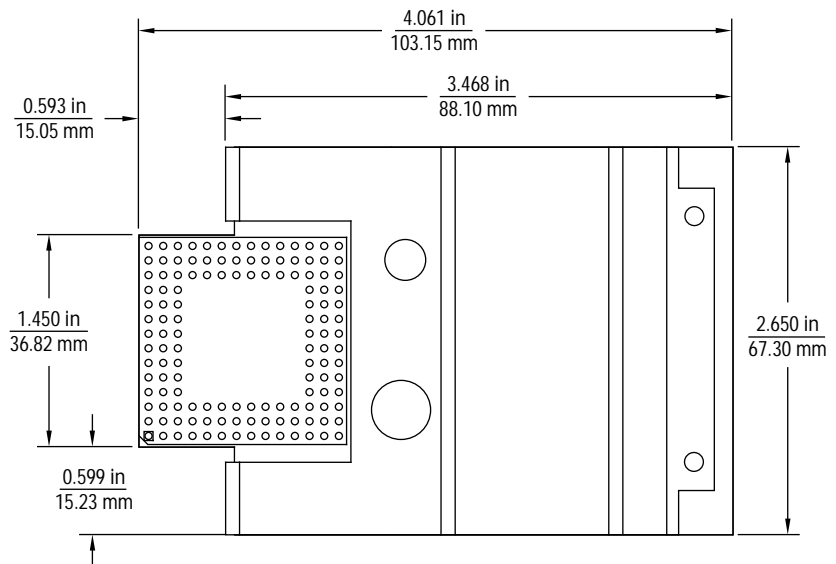# HP E2464A

Intel 80960J-Series Preprocessor Interface

**For use with
HP logic analyzers**

The Hewlett-Packard E2464A preprocessor interface provides an easy way to connect a Hewlett-Packard logic analyzer to a target system using the Intel 80960J-series microprocessors. All necessary clocks are passed through by the preprocessor to the logic analyzer, ensuring that data is captured at the correct time. Software is shipped with the product that automatically configures the logic analyzer, generating labels for address, data, and status signals. Included with the software is a disassembler which displays execution traces in 80960J-series microprocessor mnemonics. Three modes of operation are available to the user: state-per-clock, which provides a complete display of all bus activity; state-per-transfer, which filters out wait and idle states; and timing analysis up to 500 MHz. Channel to channel skew is 1 ns.

**HP E2464A Intel
80960J-series
preprocessor**

Key Specifications

Timing Analysis Support
All signals are buffered by 74FCT646ATQ gates with a 1 ns channel-to-channel skew.

Pods
The preprocessor has 6 pods available. For inverse assembly 5 logic analyzer pods must be used. Six pods would allow timing measurements of all processor signals.

Termination Adapters (TAs)
None are required as the pods are terminated on the preprocessor.

Logic Analyzers Supported
HP 1650B, 1652B, 1654B, 1660A/61A, 16510B, 16511B, 16540/41[A-D], 16542A, 16550A, 16554A, 16555A

Processors Supported

80L960JA	3.3 V, 40 MHz and 50 MHz, 132-pin PGA package
80960JD	5 V, 40 MHz and 50 MHz, 132-pin PGA package
80960JF	5 V, 40 MHz and 50 MHz, 132-pin PGA package
80L960JF	3.3 V, 40 MHz and 50 MHz, 132-pin PGA package

Optional Adapter Available
The HP E5337A adapts the HP E2464A to the 132-pin PQFP version of the chip.

Signal Line Loading
8 pF on all signals except for DEN#, RESET#, and RDYRCV# which have 16 pF.

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