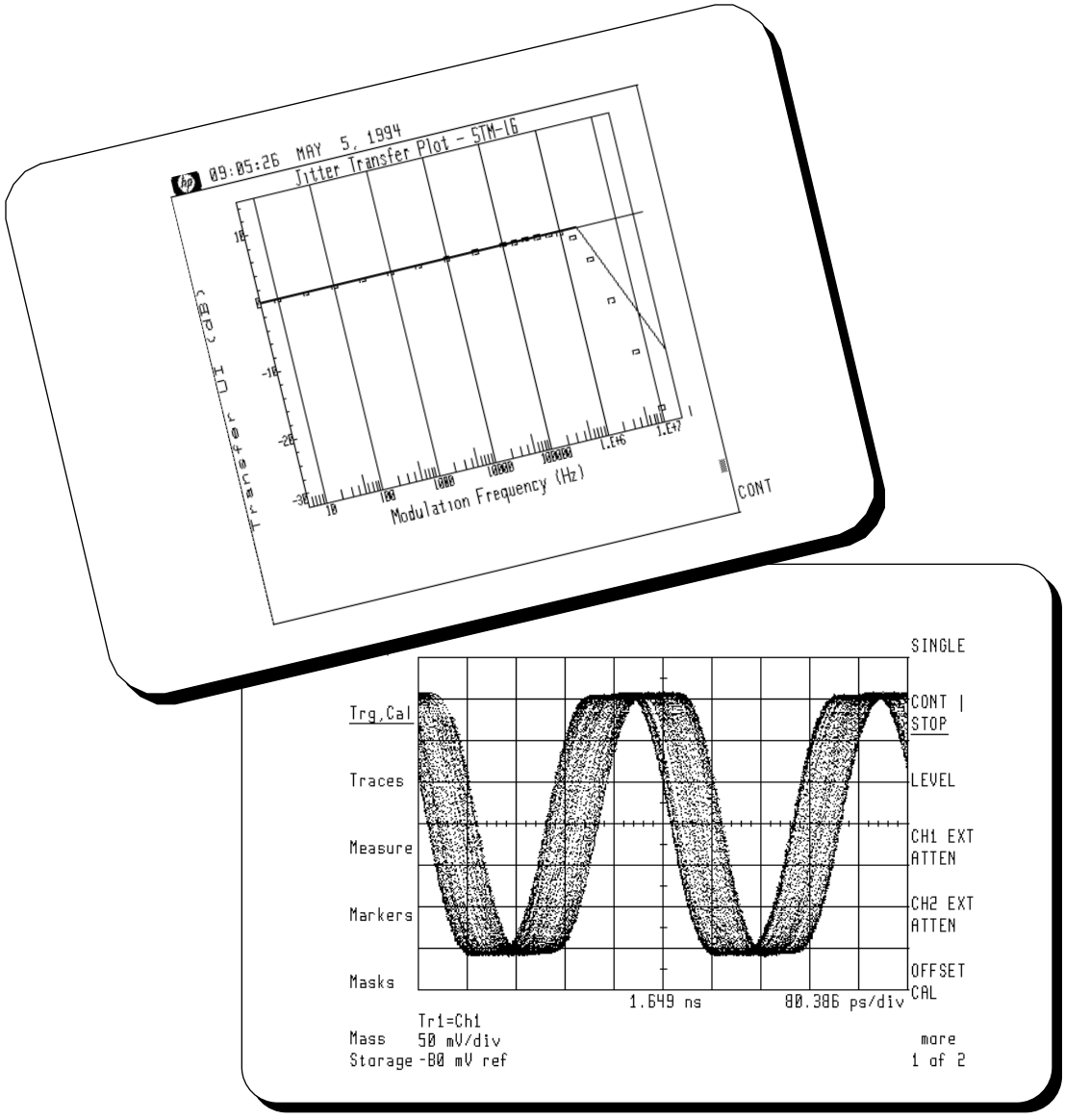
HEWLETT PACKARD

Frequency agile jitter measurement system

Application Note 1267



Contents

Introduction

This application note focuses on jitter measurements of components and equipment that make up synchronous networks such as the synchronous digital hierarchy (SDH) and the synchronous optical network (SONET). First, jitter is described, along with a discussion on why it is important. Next, jitter conformance tests are described, followed by a comparison of jitter measurement techniques. Finally, the measurement contributions of a frequency agile jitter measurement solution with diagnostic capability are presented.

What is jitter?

ITU-T G.701 defines jitter as short-term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time. The significant instant can be any convenient, easily identifiable point on the signal such as the rising or falling edge of a pulse or the sampling instant.

A second parameter closely related to jitter is wander. Wander generally refers to long-term variations in the significant instants. There is no clear definition of the boundary between jitter and wander, however phase variations below 10 Hz are normally called wander.

Deriving the jitter function

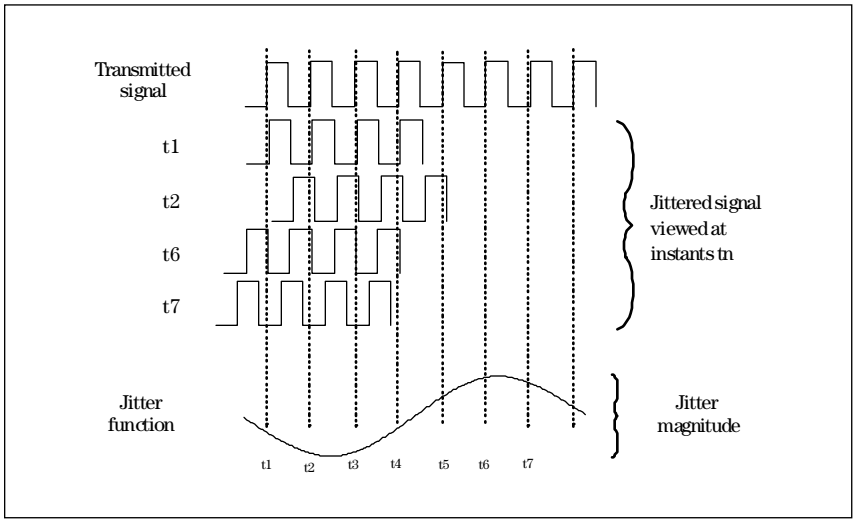


Figure 1. Jitter function

Figure 1 shows an ideal pulse train compared at successive instants t_n with a real pulse train which has some timing jitter. By plotting the relative displacement in the instants, the jitter function is obtained. Typically, the jitter function is not sinusoidal. In addition to the jitter time function, the jitter spectrum could be displayed in the frequency domain.

The unit interval (UI)

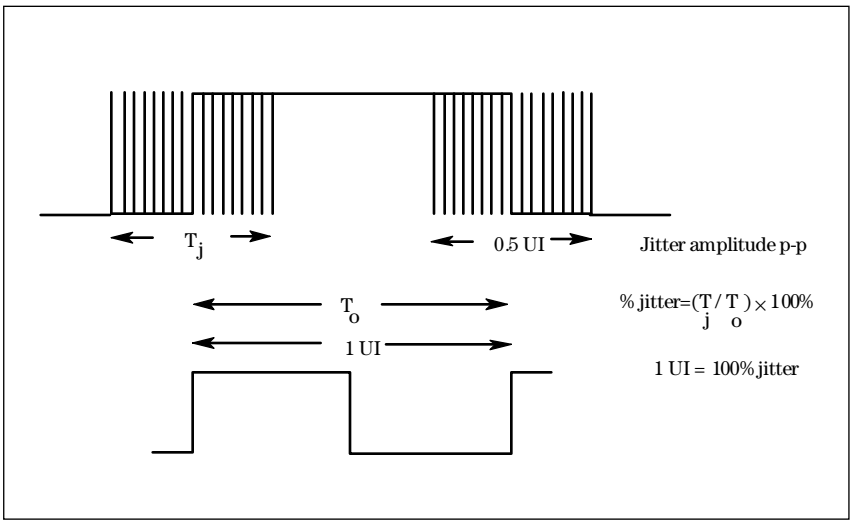


Figure 2. Definition of UI

Jitter amplitude is traditionally measured in unit intervals (UI), where 1 UI is the phase deviation of one clock period. The peak-to-peak UI deviation of the phase function with respect to time is referred to as the jitter amplitude. Since this is normalized to the clock period, it is independent of bit rate. It is therefore possible to compare jitter amplitude at different hierarchical levels in a digital transmission system.

Controlling jitter is important because jitter can degrade the performance of a transmission system introducing bit errors and uncontrolled slips in the digital signals. Jitter causes bit errors by preventing the correct sampling of the digital signal by the clock recovery circuit in a regenerator or line terminal unit. In addition, jitter can accumulate in a transmission network depending on the jitter generation and transfer characteristics of the interconnected equipment.

Categories of jitter measurement

- Jitter tolerance
- Jitter transfer
- Jitter generation

There are several categories of jitter measurement. Jitter tolerance is defined in terms of an applied sinusoidal jitter component whose amplitude, when applied to an equipment input, causes a designated degradation in error performance. Jitter transfer is the ratio of the amplitude of an equipment's output jitter relative to an applied sinusoidal jitter component. Jitter generation is a measure of the jitter at an equipment's output in the absence of an applied input jitter. A related jitter noise measurement is output jitter, which is a measure of the jitter at a network node or output port.

Jitter tolerance measurement and template

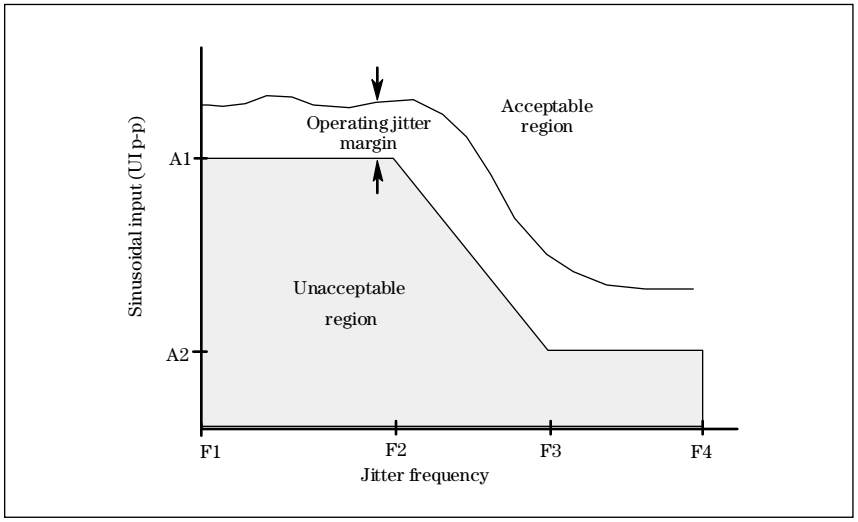
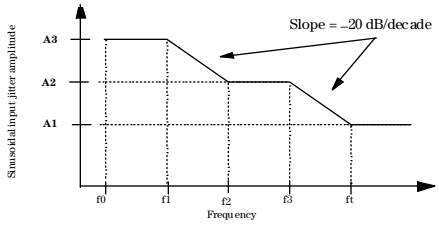


Figure 3. Jitter tolerance template

Equipment jitter tolerance performance is specified with jitter tolerance templates. Each template defines the region over which the equipment must operate without suffering the designated degradation in error performance. The difference between the template and actual equipment tolerance curve represents the operating jitter margin, and determines the pass/fail status.



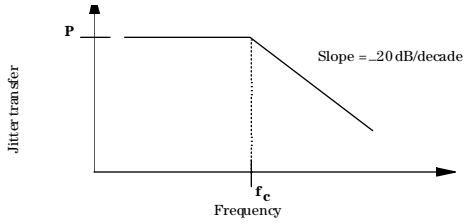
OC/STS-N [1]	STM-N [2]	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)	A1 (UI p-p)	A2 (UI p-p)	A3 (UI p-p)
1		10	30	300	2	20	0.15	1.5	15
3		10	30	300	6.5	65	0.15	1.5	15
	1(A)				6.5	65	0.15	1.5	
12		10	30	300	25	250	0.15	1.5	15
	4(A)				25	250	0.15	1.5	
24		10	200	2000	2	20	0.15	1.5	15
48		10	600	6000	100	1000	0.15	1.5	15
	16(A)				100	1000	0.15	1.5	
	16(B)				1.2	12	0.15	1.5	

1. Bellcore technical reference: TR-NWT-000253, Issue 2, December 1991
2. ITU-T G958

Figure 4. Input jitter tolerance specification

Each transmission rate typically has its own input jitter tolerance template. In some cases, there may be two templates for a given transmission rate to accommodate different regenerator types. In addition, different standards may have different templates at similar rates. Shown here are the input jitter tolerance specifications for SONET and SDH transmission systems.

Jitter transfer specification



OC/STS-N [1]	STM- [2]	f_c (kHz)	P (dB)
1		40	0.1
3	1(A)	130	0.1
12	4(A)	500	0.1
24		40	0.1
48 (A)	16(A)	2000	0.1
48 (B)	16(B)	30	0.1

1. Bellcore technical reference: TR-NWT-000253, Issue 2, December 1991
2. ITU-T G.958

Figure 5. Jitter transfer specification

The jitter transfer function is also specified for each transmission rate and regenerator type. Jitter transfer requirements on clock recovery circuits specify a minimum amount of jitter gain versus frequency up to a given cut-off frequency, beyond which the jitter must be attenuated. The jitter transfer specification is intended to prevent the buildup of jitter in a network consisting of a cascade of regenerators.

Jitter generation specification

		Output jitter limit (UI p-p)		Measurement filter bandwidth corresponds to a band pass filter having lower cut-off frequency F_1 or F_3 and minimum upper cut-off frequency F_4		
STS level	**OC level**	**Band 1 F_1 to F_4**	**Band 2 F_3 to F_4**	**F_1 (Hz)**	**F_3 (kHz)**	**F_4 (MHz)**
1	1	1.5	0.15	100	20	0.4
3	3	1.5	0.15	500	65	1.3
(N/A)	12	1.5	0.15	1000	250	5
	24	1.5	0.15	2000	20	10
	48 (with type A regenerators)	1.5	0.15	5000	1000	20
	48 (with type B regenerators)	1.5	0.15	5000	12	20

Figure 6. STS-n and OC-n output jitter specification

Jitter generation is essentially a phase noise measurement and for SONET/SDH equipment is specified not to exceed 10 mUI rms when measured using a highpass filter with a 12 kHz cut-off frequency.

Although similar to jitter generation, the output jitter of the network ports is specified somewhat differently, as shown in this table. Notice that for a given transmission rate the output jitter is specified in terms of peak-to-peak UI over two different bandwidths.

1. Oscilloscopes.
2. Phase detectors.
3. Sampling techniques with digital signal processing.
4. Dedicated SONET/SDH jitter analysis (including payload mapping and pointer adjustments).

Shown here are the most frequently encountered techniques to measure jitter. The first three techniques apply primarily to the measurement of jitter transfer and generation. Though the tests are applied to digital data, they tend to be analog in nature.

There are additional jitter measurements that deal with asynchronous data being mapped into the SONET/SDH format. Tests that examine the jitter due to payload mapping and pointer adjustments are performed by dedicated SONET/SDH testers, and are beyond the scope of this application note.

Jitter measurements using an oscilloscope

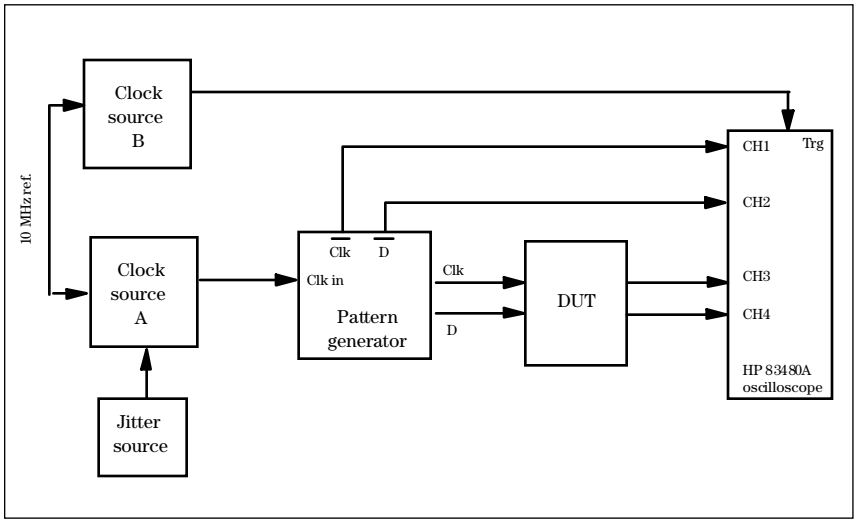


Figure 7. Configuration when using a sampling oscilloscope

Intrinsic data jitter, intrinsic clock jitter or jitter transfer can be directly measured with a high-speed digital sampling oscilloscope such as the HP 83480A oscilloscope. As shown, a jitter-free trigger signal for the oscilloscope is provided by clock source B, whose frequency reference is locked to that of clock source A. Clock source A, which is modulated by the jitter source, drives the pattern generator, which supplies jittered data for the jitter transfer measurement to the device under test (DUT). The jittered input and output waveforms can be analyzed using the built-in oscilloscope histogram functions.

The limitations of the oscilloscope measurement technique are listed here. The maximum jitter amplitude that can be measured is limited to 1 UI peak-to-peak. Above this level, the eye diagram is totally closed. This technique offers poor measurement sensitivity, because of the inherently high noise level, due to the large measurement bandwidth involved. In addition, the technique does not provide any information about the jitter spectral characteristics or time domain waveform. Finally, the technique requires an extra clock source to provide the oscilloscope trigger signal.

Jitter measurement using a phase detector

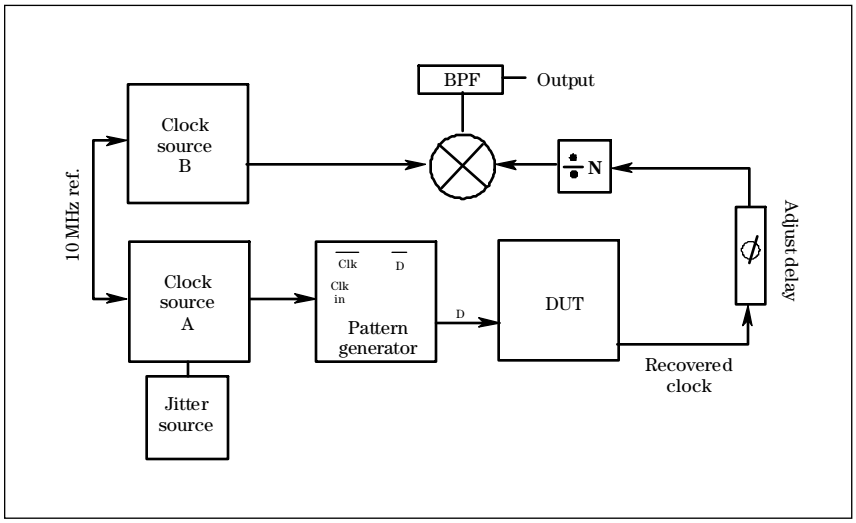


Figure 8. Configuration when using a phase detector

Many of the limitations of the sampling oscilloscope technique can be addressed using a phase detector. The phase detector compares the phase of the recovered clock from the device or equipment under test with a jitter-free clock source. The output of the phase detector is a voltage that is proportional to the jitter on the recovered clock signal. The range of the phase detector can be extended beyond 1 UI by using a frequency divider. Intrinsic jitter is measured with appropriate bandpass filters.

The phase detector method forms the basis for most dedicated jitter measurement systems. It is relatively easy to implement and provides fast intrinsic jitter measurements. Low frequency network analyzers are often employed to measure jitter transfer.

There are several limitations of the phase detector technique. This type of jitter measurement system usually consists of dedicated hardware which only functions at specific transmission rates. Furthermore, a range of bandpass filters are needed for each hierarchical level. In addition, the accuracy of the jitter transfer measurement with a network analyzer may be insufficient to guarantee the specification is being met. Finally, the technique requires an additional clock source as a reference for the phase detector.

Specific advantages of the HP 71501B analyzer's jitter measurement technique

Sampler-based instruments offer a general purpose solution. These instruments typically operate by taking time samples of the data, then analyzing it using digital signal processing techniques. One such instrument is the HP 71501B jitter and eye diagram analyzer, which offers several distinct advantages. The analyzer provides automatic SONET/SDH jitter equipment measurement capability at 2.48832 Gb/s and 622.08 Mb/s. The measurement technique employed is frequency agile, allowing the instrument to make jitter measurements from 50 Mb/s to greater than 10 Gb/s. A special version of the HP 71501B analyzer is available to perform jitter measurements for multiplexers and demultiplexers where the input rate and output rates are dissimilar. Furthermore, the HP 71501B analyzer is unique in offering diagnostic measurements of the jittered clock waveform and spectrum, as well as the demodulated jitter waveform and spectrum.

In addition, the HP 71501B analyzer can perform eye diagram and extinction ratio measurements on digital waveforms.

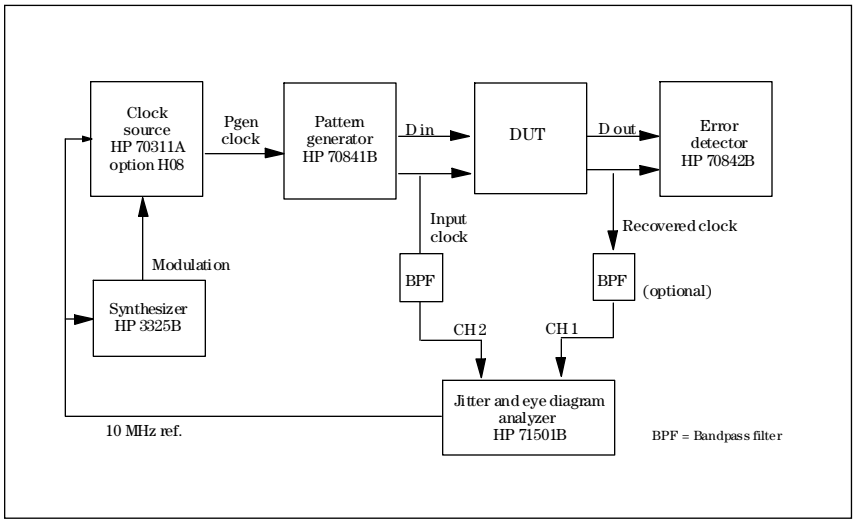


Figure 9. Configuration when using the HP 71501B analyzer

Shown here is the HP 71501B analyzer-based jitter measurement system. The system configuration includes a HP 70841B 3 Gb/s pattern generator, HP 70842B error detector, HP 70311A option H08 clock source, and HP 3325B synthesizer which serves as the jitter modulation source. A jitter application program is downloaded into the instrument basic software of the HP 71501B analyzer. The program allows the HP 71501B analyzer to take control of all the other instruments in the jitter measurement system and to coordinate the measurements.

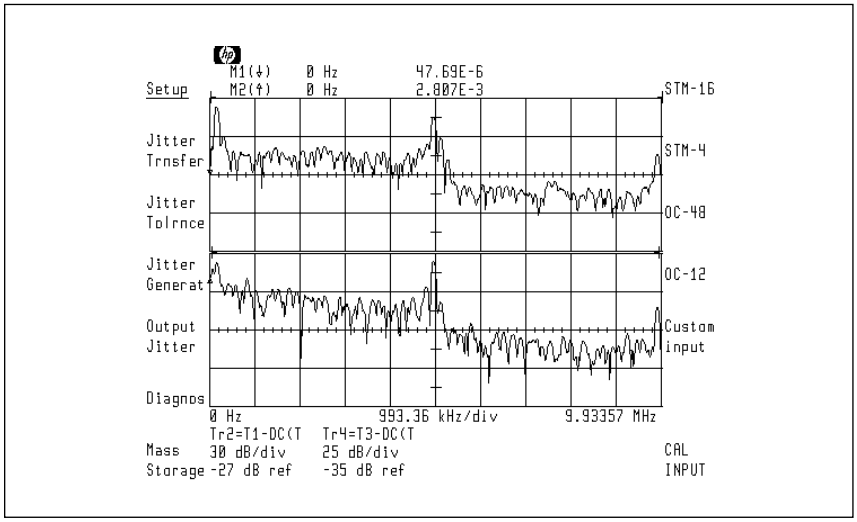


Figure 10. Jitter application menu

A jitter application specific menu is provided with softkeys to lead the user through the measurement procedure. First, the transmission rate and accompanying input jitter (tolerance) template is selected. SONET, SDH or custom templates may be selected. Custom templates can be created, edited and stored on a RAM card. A calibration routine is required to establish the recommended jitter levels that conform to the template prior to a jitter transfer or jitter tolerance measurement.

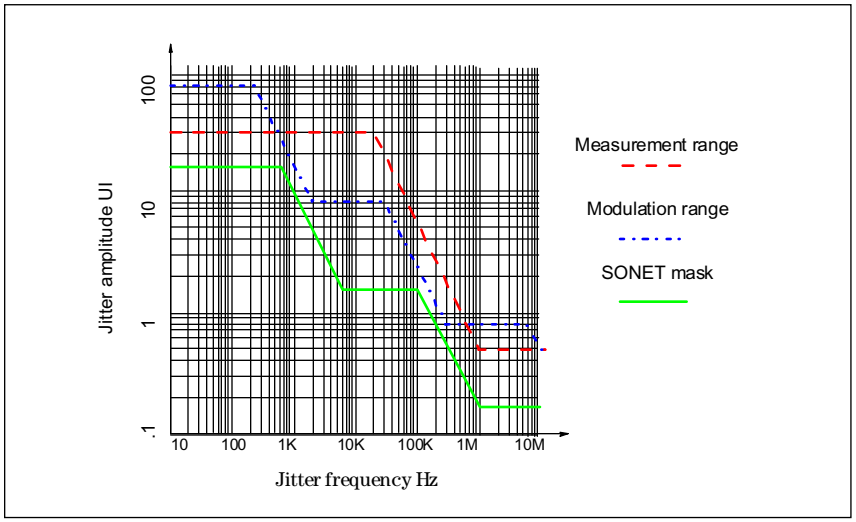


Figure 11. Jitter measurement characteristics (rate: 2.48832 Gb/s)

This figure shows the capability of the jitter measurement system at 2.48832 Gb/s compared to the jitter tolerance masks for OC-48 and STM-16. The measurement range of the HP 71501B analyzer is shown, as well as the jitter modulation capability of the HP 70311A option H08 clock source. Both the jitter modulation and measurement capability exceed that required by the standards.

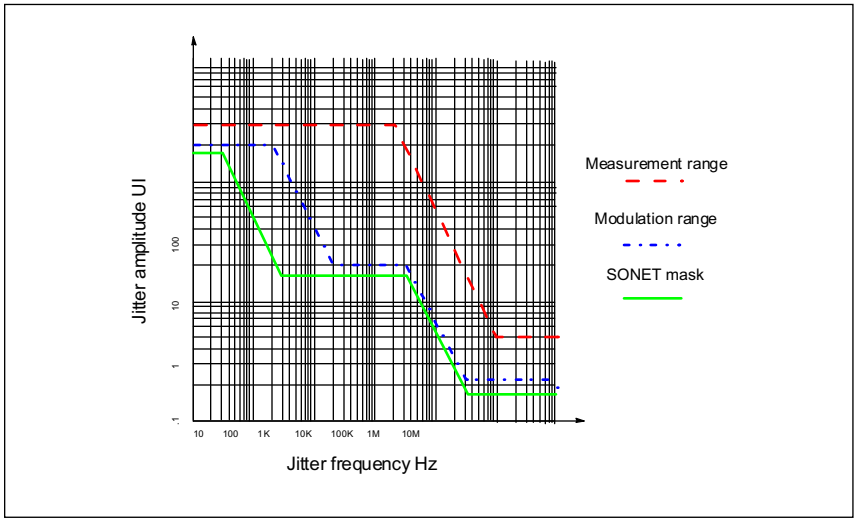


Figure 12. Jitter measurement characteristics (rate: 622.08 Mb/s)

Similarly, figure 12 shows the jitter modulation and measurement capability of the measurement system relative to the jitter tolerance templates for OC-12 and STM-4. This capability is sufficient to meet the requirements of the standard.

Jitter measurement range, in terms of the data rates, jitter rates and jitter magnitudes, is essentially dependent upon the clock source used. The standard clock source for the analyzer-based system is the HP 70311 option H08, which is typically used for 622 Mb/s and 2488 Mb/s compliance testing A special option of the HP 71501B analyzer is available to use other clock sources providing improved performance from 50 Mb/s to 12 Gb/s. Refer to HP 71501B analyzer configuration information at the end of this application note.

Jitter tolerance measurement setup

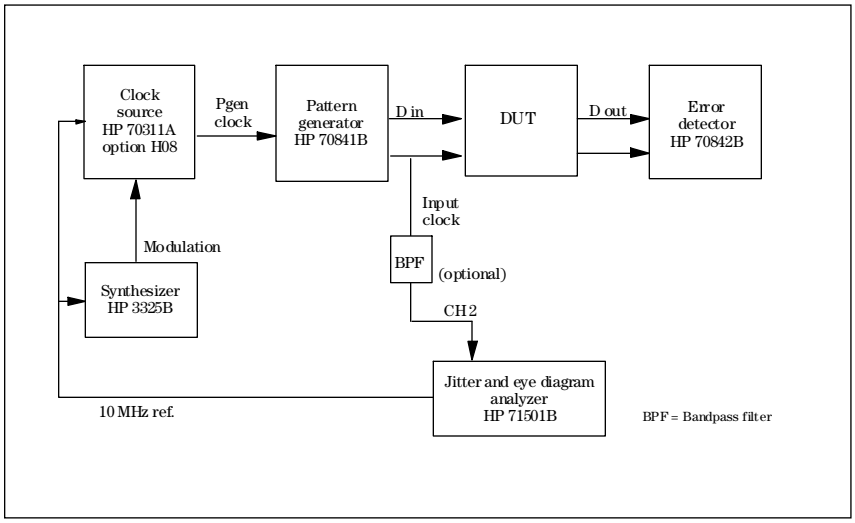


Figure 13. Setup for jitter tolerance measurement

The jitter tolerance measurement determines whether a test device or subsystem can transmit error-free data in the presence of jitter. The HP 70842B error detector monitors the recovered clock and regenerated data. Typically, an attenuator is placed in the input data path to reduce the signal power until the threshold of error generation is achieved. The attenuation is then reduced by 1 dB. Then, at a number of modulation frequencies, the amount of sinusoidal jitter corresponding to the input tolerance template is applied, while the error status is monitored.

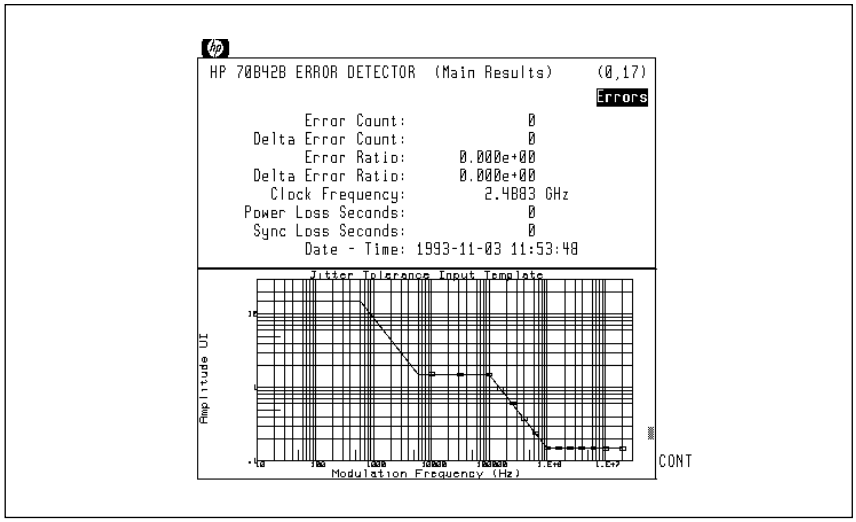


Figure 14. Results of a jitter tolerance test

This plot shows the jitter levels at each jitter measurement frequency, and whether or not errors were generated. The jitter frequencies and amplitude levels, along with pass/fail status can also be displayed in table format.

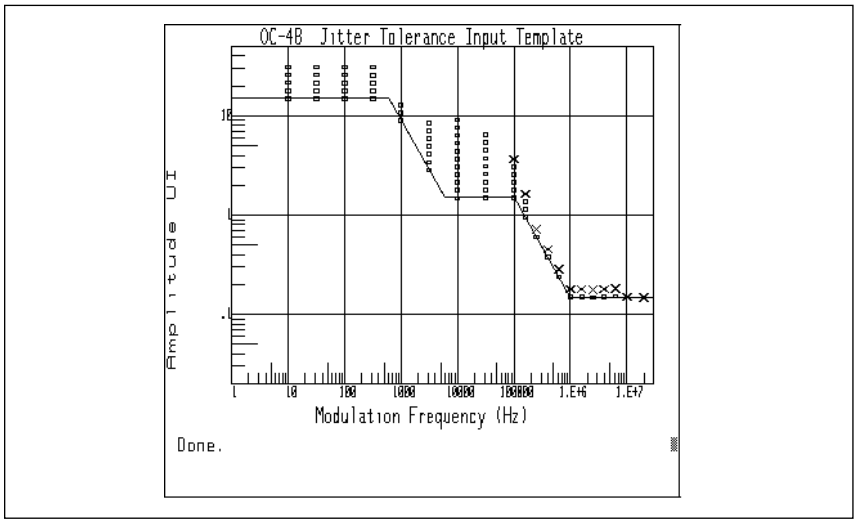


Figure 15. Results of jitter tolerance test

In addition to the jitter compliance test, it is often useful to determine by what margin a system or device exceeds the jitter tolerance template. The HP 71501B analyzer can automatically search for the jitter level at which the jitter tolerance failure threshold is reached. The search step size is user defined. The system will either increase jitter until the failure criteria is met, or until the the maximum jitter generation capability of the system is reached. Failures, and thus the jitter tolerance margin level are indicated by an 'X'.

Jitter transfer measurement setup

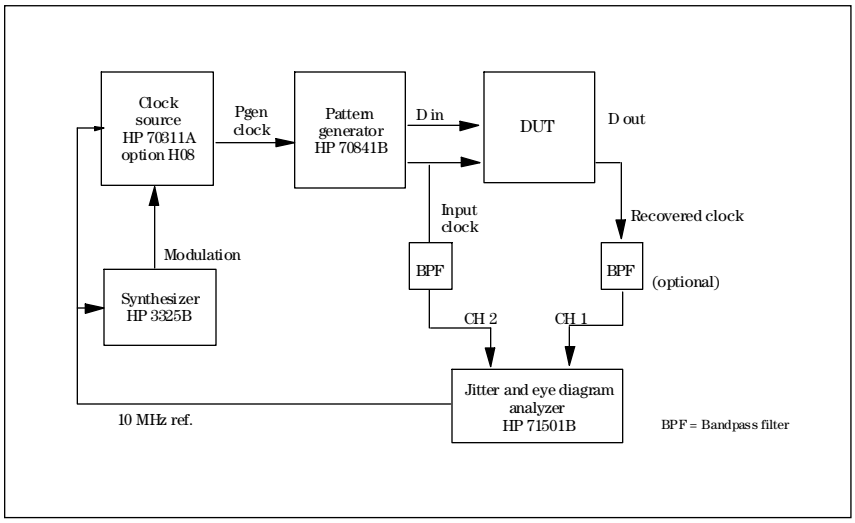


Figure 16. Setup for jitter transfer measurement

The jitter transfer measurement setup is similar to the jitter tolerance measurement setup. The main difference is that the error detector is not required as we are now measuring the ratio of applied jitter to output jitter. The recovered clock signal from the device under test is routed to channel 1 of the analyzer while the applied jitter on the input clock signal is monitored on channel 2. This measurement technique works well for several reasons. First, jitter applied to the clock input of the HP 70841B/70843A pattern generator appears equally at its data and clock outputs, therefore any data test pattern can be used. In addition, the HP 71501B analyzer's two input channels are sampled synchronously, allowing accurate phase measurements between the two channels.

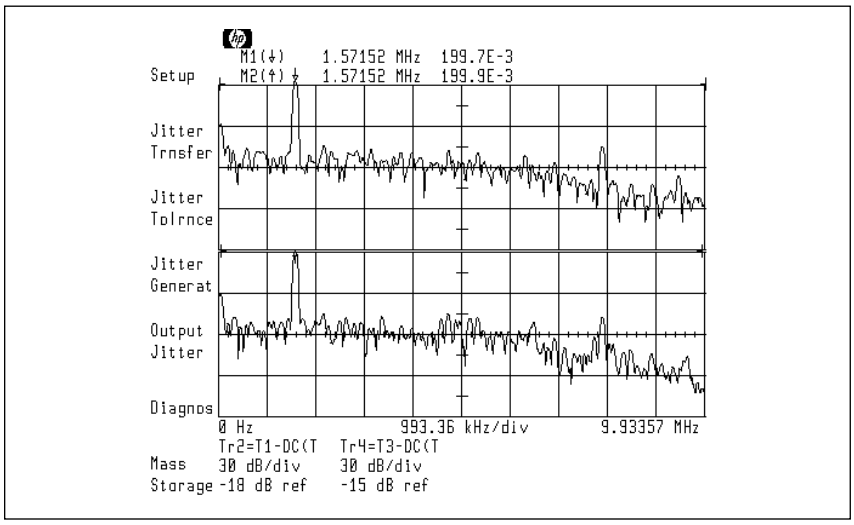


Figure 17. Example jitter transfer measurement

Figure 17 shows an example of a jitter transfer measurement at a single jitter modulation frequency, 1.57 MHz. The data rate is 2.48832 Gb/s. The upper trace is the demodulated jitter spectrum of the input clock signal on channel 2. The lower trace is the demodulated jitter spectrum of the recovered clock signal from the DUT measured at channel 1. The ratio of the signal amplitudes at the jitter modulation frequency is the jitter transfer of the DUT at that frequency. The HP 71501B analyzer can make this measurement accurately because it simultaneously measures both the input and output jitter.

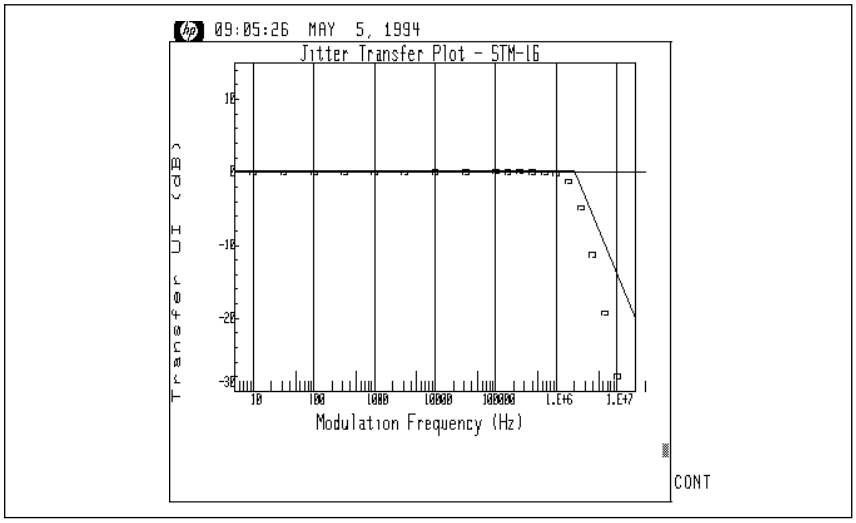


Figure 18. Plot of jitter transfer function

After the jitter transfer is plotted. The specified transfer function for the selected standard transmission rate is over-laid. Any failures are noted. Above is a plot of jitter transfer of a clock recovery circuit operating at 2.48832 Gb/s. For this device the jitter transfer is flat to a jitter modulation frequency of 2 MHz. Beyond that frequency, the output jitter level rolls off rapidly, which is the desired response. The difference between the measured jitter transfer data and the specified transfer function can also be plotted, or a table can be displayed which lists all of the data.

The jitter test template can be customized by raising or lowering the transfer function level (typically 0.1 dB). The frequency of the transfer template roll-off can also be user defined.

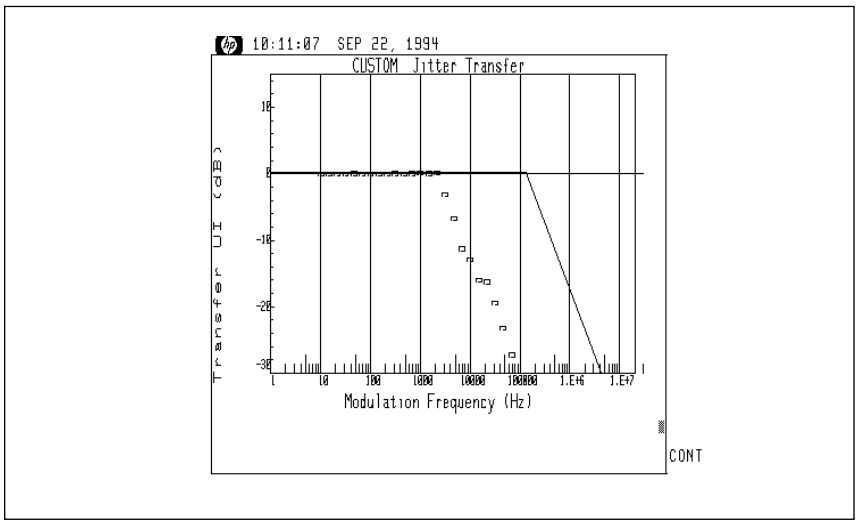


Fig 19. Results for custom jitter transfer measurement

Jitter transfer for multiplexer and demultiplexer devices is a complex measurement. The input rates and output rates are dissimilar. However, the task is easily performed with the HP 71501B analyzer-based system. In the above measurement, testing a 1:32 mux, channel 2 of the HP 71501B analyzer (the reference channel) is set to receive a 155 Mb/s clock signal; whereas channel 1 receives the 4.98 Gbit output clock. This measurement is achieved because of the frequency agility of the analyzer-based system.

Intrinsic jitter measurement

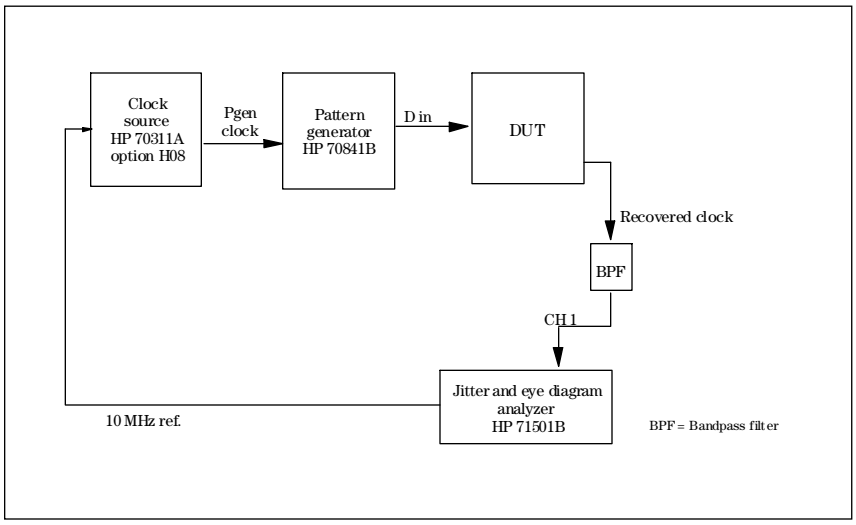


Figure 20. Setup for intrinsic jitter measurement

The intrinsic jitter measurement setup is similar to the jitter transfer setup, except there is no jittered input signal to the DUT. The intrinsic jitter on the recovered clock output of the DUT is monitored on channel 1 of the HP 71501B analyzer. Note that intrinsic jitter is essentially a noise measurement. A bandpass filter at the appropriate clock frequency is used to set the upper limit of the noise measurement bandwidth.

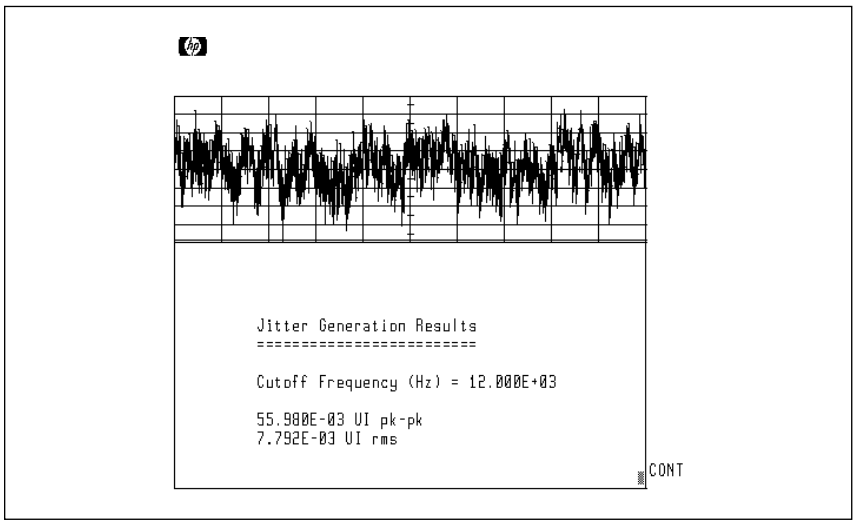


Figure 21. Example results for jitter generation measurement

As previously stated, jitter generation is an intrinsic jitter measurement on a piece of network equipment, such as a regenerator or component. The standards specify the jitter spectrum be measured with a 12 kHz highpass filter. The HP 71501B analyzer implements the 12 kHz highpass characteristic in software with the corner frequency for the filter being adjustable. The bandlimited noise spectrum is then transformed to the time domain and displayed as shown above. Transformation to the time domain makes it possible to determine the peak-to-peak as well as rms jitter values.

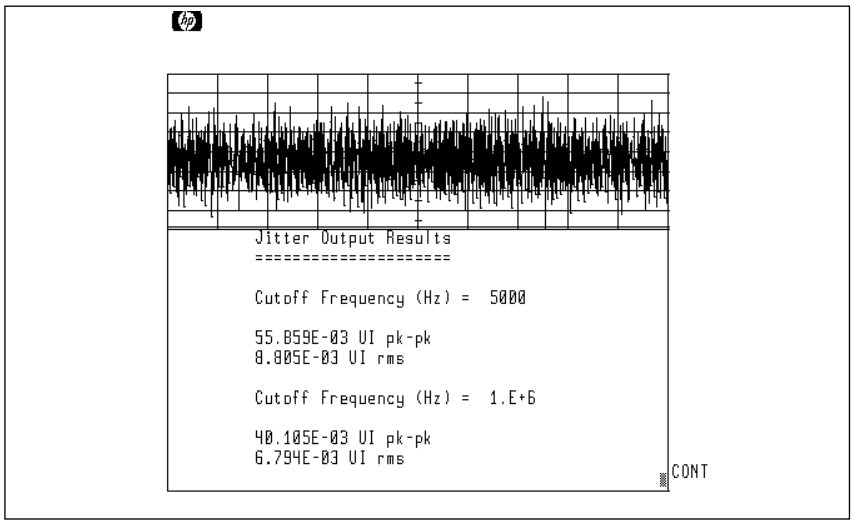


Figure 22. Example jitter output results

The output jitter measurement technique is similar to the jitter generation measurement. However, in the case of output jitter, the measurement is intended to be performed at network interfaces. The output jitter specifications apply to line systems which may contain terminals, add-drop multiplexers and regenerators. Two measurement bandwidths with different low cut-off frequencies are required by the standards. The upper measurement frequency limit is set by the hardware filter.

Shown above is the measurement performed on a clock recovery unit at 2.48832 Gb/s. Both bandwidths are measured automatically, and the results displayed in both peak-to-peak UI and rms UI. Note that to make this measurement at the interface of a line system, some form of broadband clock recovery unit is required to measure the jitter. The bandwidth of the broadband clock recovery unit should be significantly larger than the equipment in the network to allow the jitter in the network to be measured.

HP 71501B jitter and eye diagram analyzer

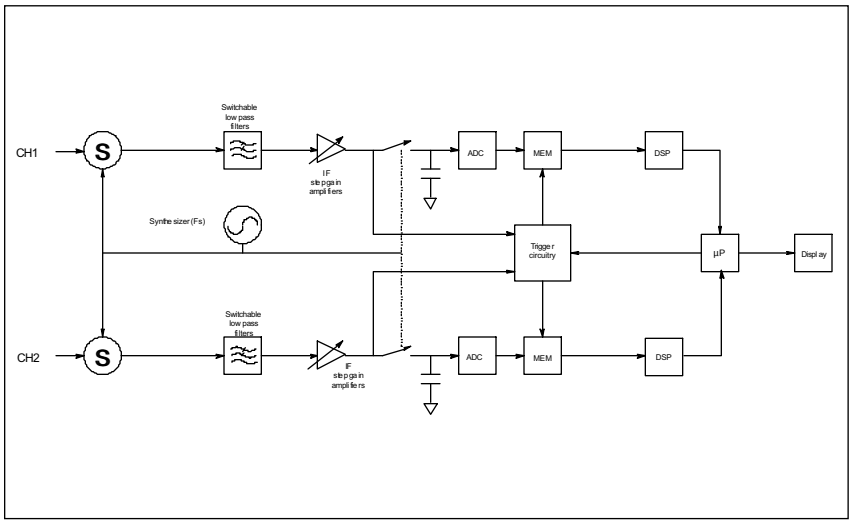


Figure 23. Block diagram of HP 71501B analyzer

The unique architecture of the HP 71501B analyzer allows it to have the attributes of a digital sampling oscilloscope, an RF spectrum analyzer and a modulation analyzer. This makes it very useful for a number of diagnostic measurements. In addition, it is a two channel instrument which is appropriate for this application. As shown in the block diagram, microwave samplers are used to down convert the input signal to a DC to 10 MHz intermediate frequency (IF), where the signal is digitized and appropriate digital signal processing (DSP) can be applied. The sample rate is nominally close to 20 MHz but adjusts itself, based on the incoming signal frequency, to optimally down convert the signal to the IF section. The internal DSP is used to perform fast fourier transforms (FFTs), inverse fast fourier transforms (IFFTs), and demodulation on the input signal.

Diagnostic capabilities of the HP 71501B jitter and eye diagram analyzer

- View demodulated jitter waveform and spectrum
- View clock waveform and spectrum
- Generate custom input tolerance templates
- Analyze intrinsic jitter with variable highpass filter

The HP 71501B analyzer may be unique in its ability to display the data, clock, and demodulated jitter waveforms and spectra. A mode is available to assist in the diagnosis of equipment failures, or with the development of new components or systems, as each jitter modulation frequency or jitter amplitude can be examined.

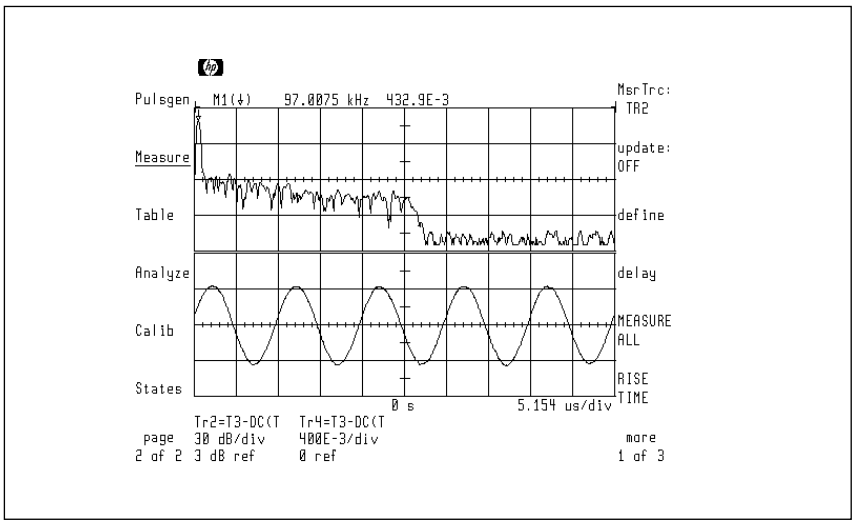


Figure 24. Display of the demodulated jitter spectrum and waveform

In the above example, the demodulated jitter spectrum and waveform of a sinusoidally modulated clock signal are displayed. The modulating frequency was approximately 97 kHz and the clock rate was 2.48832 Gb/s.

This capability may be useful in determining the relative contributions of random and systematic jitter. As was previously mentioned, custom tolerance templates can be constructed to analyze error performance. In addition, adjustable software highpass filters aid intrinsic noise analysis.

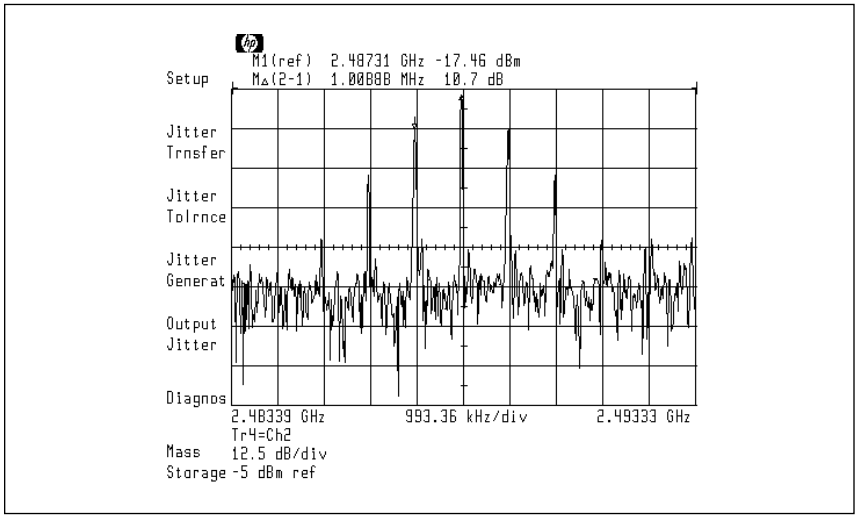


Figure 25. Display of sinusoidal jitter modulation present on the clock

The sinusoidal jitter modulation present on the clock can be displayed in the frequency domain similar to the display of an RF spectrum analyzer. The above trace shows the spectrum of the clock at 2.48832 GHz being sinusoidally modulated at a 1 MHz rate. The sidebands, as expected, have the appropriate Bessel amplitudes corresponding to FM modulation.

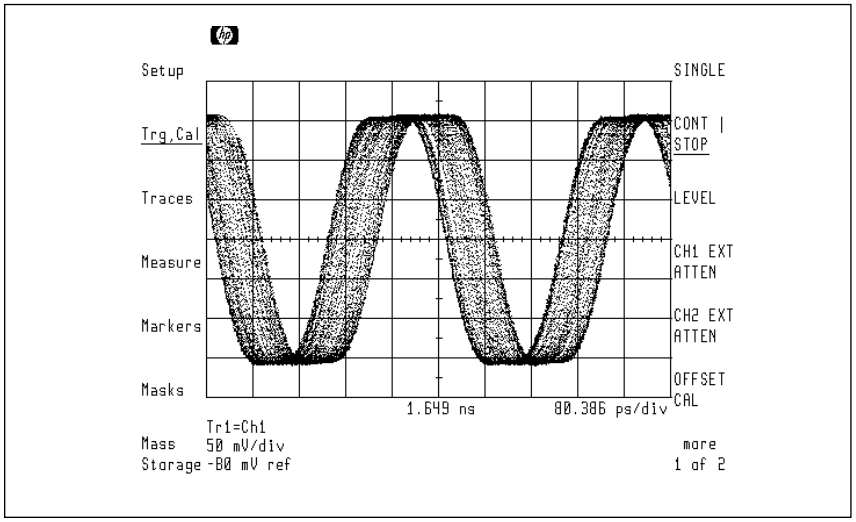


Figure 26. Display of clock waveform with jitter

The clock and data waveforms can also be displayed similar to a digital sampling oscilloscope. A full set of histogram functions are available to measure timing jitter. In addition, eye diagram mask and extinction ratio measurements can be performed. The above trace shows a display of a jittered clock waveform. The transmission rate was 2.48832 Gb/s and the jitter frequency and amplitude were 10 kHz and .2 UI respectfully.

Summary

Jitter is an important parameter that must be controlled in a transmission system to minimize bit errors. Equipment level standard specifications, such as ITU-T G.958 have been developed to insure that network equipment will operate within the appropriate jitter budget. The HP 71501B jitter and eye diagram analyzer can aid equipment manufacturers by performing industry standard jitter measurements such as jitter tolerance, jitter transfer, jitter generation, and output jitter at 622.08 Mb/s and 2.48832 Gb/s. It's measurement capability is frequency-agile from 50 Mb/s to greater than 10 Gb/s. Custom input tolerance templates can be constructed and variable bandwidth noise measurements can be performed. To aid equipment designers, the HP 71501B analyzer has significant diagnostic capability that allows the demodulated jitter spectrum and waveform to be observed. In addition, it can perform extensive eye diagram and extinction ratio measurements.

Configuration information

HP 71501B analyzer-based system configuration

The standard configuration of the HP 71501B analyzer-based jitter analysis system is capable of operating from 50 Mb/s† to 3 Gb/s. It is capable of SDH/SONET compliance measurements at 622 Mb/s and 2.488 Gb/s and must include the following equipment:

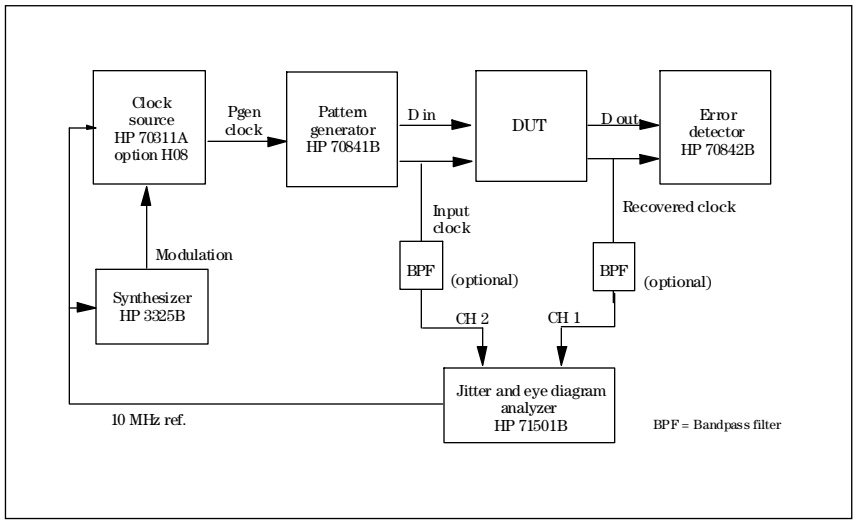


Figure 27. System configuration for 50 Mb/s to 3 Gb/s

HP 71501B jitter and eye diagram analyzer
Includes:
HP 70004A display mainframe.
HP 70820A microwave transition analyzer with expanded memory.
Standard jitter measurement software.
Bandpass filter for 622 Mb/s and 2.488 Gb/s testing.
Cables and accessories for system phase-locking.
HP 3325A/B synthesized function generator (jitter source)
HP 71603B bit error rate analyzer
Includes:
HP 70311A option H08 clock source.
HP 70841B pattern generator.
HP 70842B error detector.
HP 70001A module mainframe.
HP 70004A display mainframe (Note that the system can operate with either one or two display mainframes).

† Note: 100 Mb/s as standard, 50 Mb/s available as option.

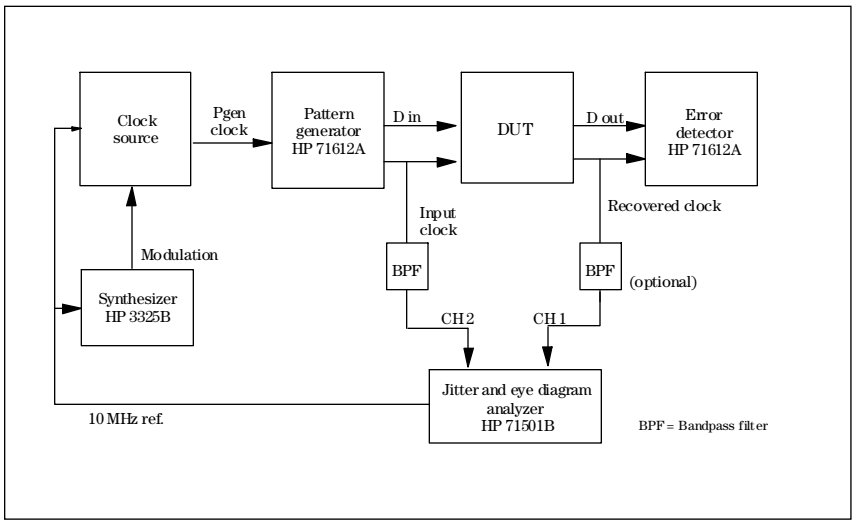


Figure 28. System configuration for 100 Mb/s to 12 Gb/s

A new version of the HP 71501B system has been developed to operate with the HP 71612A 12 Gb/s error performance analyzer for jitter analysis at data rates up to 12 Gb/s. This system is capable of jitter compliance testing at 155 Mb/s data rates when used with either the HP 71603B 3 Gb/s or HP 71612A 12 Gb/s error performance analyzers using alternative clock sources to the standard configuration. In addition to expanding the measurement range of the HP 71501B analyzer-based system, the following measurement features (not available with the standard system) are present:

- Jitter testing for mulitplexers and demultiplexers
- Automatic determination of jitter tolerance margins
- Wider selection of clock sources

When this version of the HP 71501B analyzer-based system is used, performance is dictated by the clock source used. A selection of clock sources is available as there are trade-offs of data rate, jitter magnitude and jitter bandwidth. The following shows the available compatible clock sources and their performance:

HP 70311A option H08 clock source

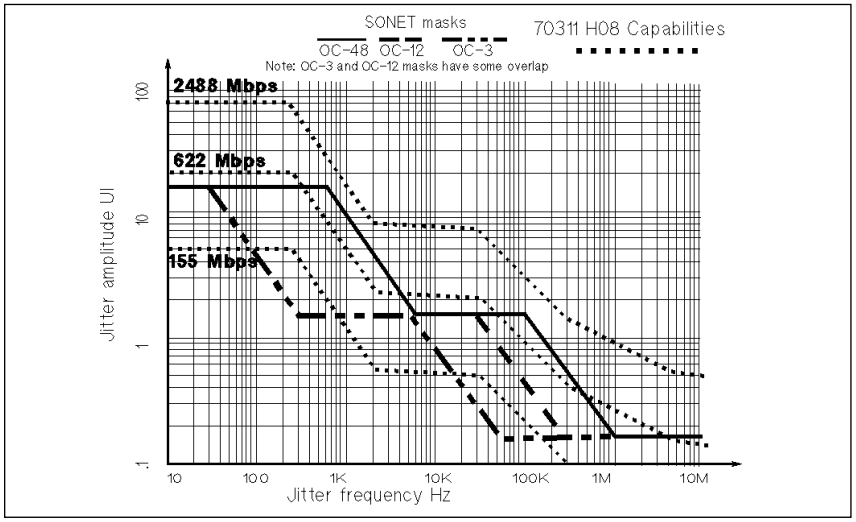


Figure 29. HP 70311A H08 clock source modulation capability

Note that the HP 70311A H08 clock source has a range of 100 Mb/s to 3 Gb/s. However, jitter modulation capability is data rate dependent. Jitter magnitude scales with data rate. Thus jitter modulation at 622 Mb/s is one-fourth the modulation level achieved at 2.488 Gb/s. Modulation capability is reduced a factor of four again when operating at 155 Mb/s. Thus compliance measurements at 155 Mb/s are not achievable using the HP 70311A H08 clock source.

HP 70340A clock source

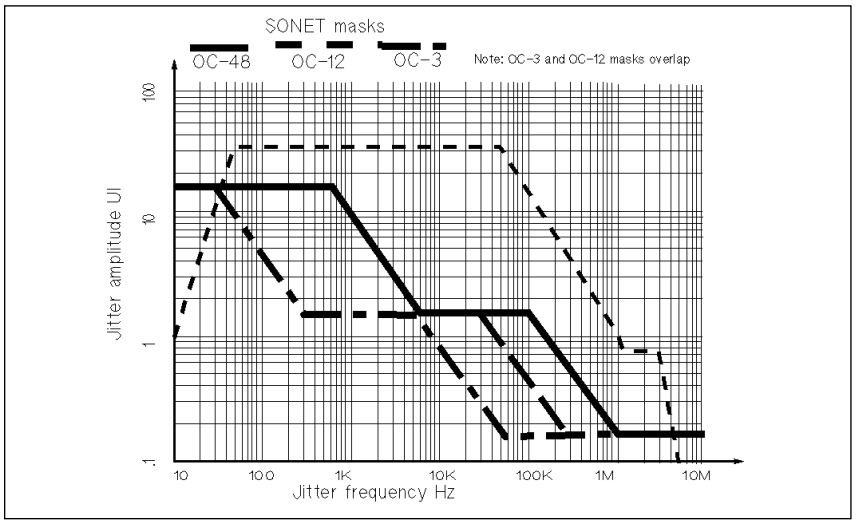


Figure 30. HP 70340A clock source modulation capability

The HP 70340A is the standard clock source used with the HP 71612A error performance analyzer. It operates from 1 to 12 Gb/s. Jitter generation capability is constant with data rate. It can achieve over 30 UI of jitter over the frequency range of 70 Hz to 60 KHz. However, the jitter modulation range is approximately 5 MHz. It is useful for general jitter measurements, but is not capable of operating to the full 20 MHz required for compliance testing at 2.488 Gb/s. As no standard has been set for 10 Gb/s compliance tests, the system can be used at this rate.

HP 83752A clock source

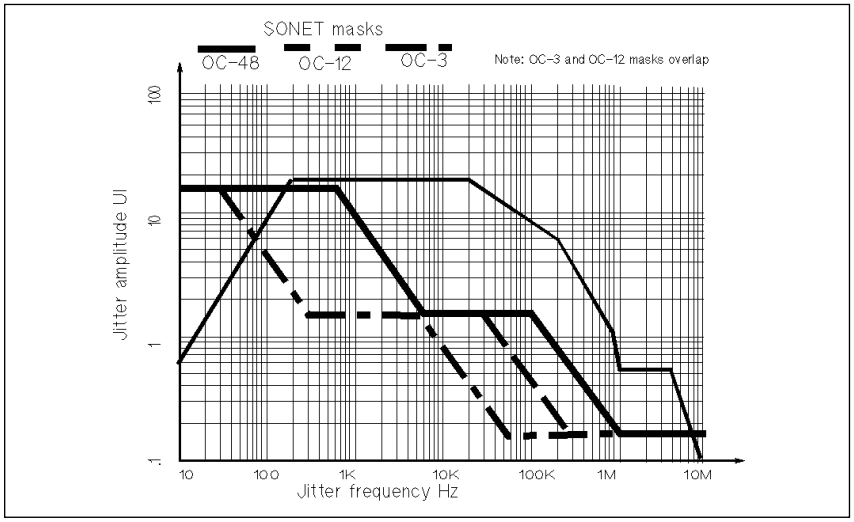


Figure 31. HP 83752A clock source modulation capability

The HP 83752A synthesized sweep generator is a general purpose signal generator that operates from 10 MHz to 20 GHz. Jitter is independent of data rate, thus this clock source can be used over the full range of the HP 71501B analyzer-based system (50 Mb/s to beyond 12 Gb/s). It also has a jitter bandwidth approaching 10 MHz, approximately double that of the HP 70340A clock source. Maximum level of jitter that can be generated with the HP 83752A generator is approximately 16 UI.

References

ITU-T recommendation G.958, “Digital line systems based on the synchronous digital hierarchy for use on optical fibre cables.”

ITU-T recommendation G.825, “The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy.”

ANSI T1X1.3/93-006R2, “Synchronous Optical Network (SONET): Jitter at network interfaces.”

Bellcore TA-NWT-00253, “Synchronous Optical Network (SONET) transport systems: Common generic criteria.”

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