HEWLETT PACKARD

HP 16522A 200 M Vector/sec Pattern Generator Module for the HP 16500B Logic Analysis System

Digital Stimulus for Prototype Turn-on and Verification

Key Characteristics

Maximum Clock	200 MHz	100 MHz	50 MHz
Number of data channels per HP 16522A module	20	40	40
Memory depth, in vectors	258,048	258,048	258,048
"IF" command	no	no	yes
Maximum Vector Width (5 module system)	100 bits	200 bits	200 bits

Functionally Test Your Designs

The HP 16522A digital pattern generator module is the perfect tool for functional testing your digital design. The pattern generator allows you to check the functional characteristics of your system. See how your system responds to specific signals or clock speeds. Correlate data captured with other HP 16500B series modules to verify correct operation. Use the HP 16522A in automated test environments to run design verification tests quickly, using only one instrument. Save time normally spent developing custom test hardware used for stimulus.

Use Parallel Development of Subsystems to Reduce Time to Market

When you have the ability to test system subcomponents, you can find problems earlier in the design process. As a result, you can cut your development time and make improvements in the finished product. Use the HP 16522A as a substitute for missing boards, integrated circuits (ICs), or buses. Instead of waiting for the missing pieces, you can continue to test and verify your design.

Software engineers can create infrequently encountered test conditions and verify that their code works — before complete hardware is available. Hardware engineers can generate the patterns necessary to put their circuit in the desired state, operate the circuit at full speed or single-step the circuit through a series of states.

Digital Stimulus and Response

Configure the HP 16500B system to provide both stimulus and response in a single instrument. For example, have the pattern generator simulate a circuit initialization sequence. The pattern generator can then signal the state or timing analyzer to begin making measurements. Use the compare mode on the state analyzer to determine if the circuit or subsystem is functioning as expected.

Use the HP 16500B's timing analyzer or oscilloscope modules to locate the source of timing problems or to troubleshoot signal problems due to noise, ringing, overshoot, crosstalk, or simultaneous switching.

Vectors Up To 200 bits Wide

Vectors are defined as a "row" of labeled data values. Each data value can be from one to 32-bits wide. Each vector is output on the rising edge of the clock. Up to five, 40-channel HP 16522A modules can be interconnected within an HP 16500B (or HP 16501A expansion frame) to support vectors of any width up to 200 bits with excellent channel-to-channel skew characteristics (see specific data pod information below). At clock speeds above 100 MHz, the pattern generator operates in "half channel" mode, resulting in 20 output channels per HP 16522A module.

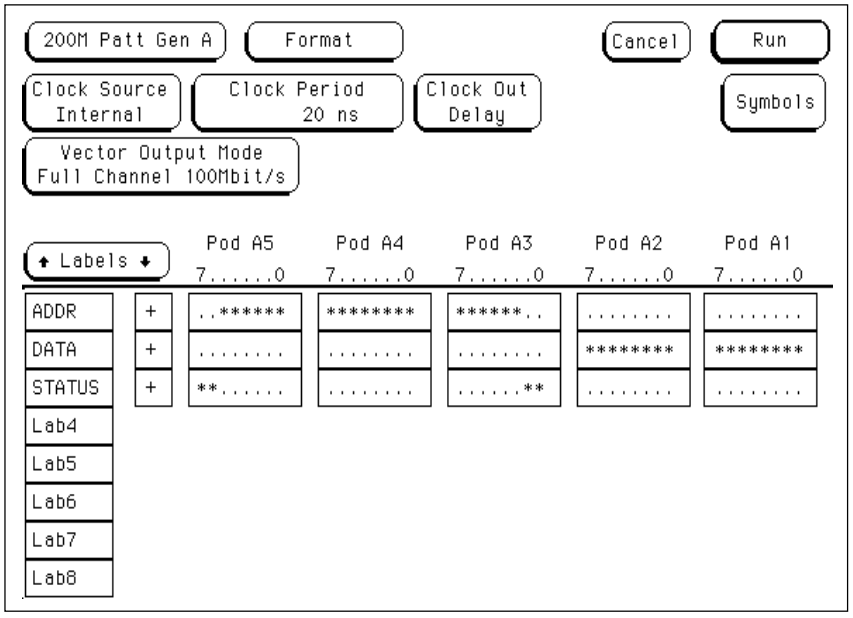


Figure 1. Use the Format menu to group output channels into logical labeled groups.

Synchronized Clock Output

You can operate with either an internal or external clock. The external clock is input via a clock pod, and has no minimum frequency or duty cycle requirements (other than a 2 ns minimum high time). The internal clock is selected as a clock period from 5 ns to 250 µs in a 1, 2, 2.5, 4, 5, 8 sequence (4 KHz to 200 MHz). A Clock Out signal is available from the pod and can be used as an edge strobe with a variable delay of up to 11 ns.

Wait for Input Pattern

The clock pod also accepts a 3-bit input pattern. These inputs are level-sensed so that any number of "Wait for Pattern" instructions can be inserted into a stimulus program. Up to four pattern conditions can be defined from the ORing of the eight possible 3-bit input patterns. A "Wait for IMB" can also be defined to wait for an intermodule measurement bus event.

Initialize Block for Repetitive Runs

When running repetitively, the vectors in the init sequence are output once, while the main sequence is output as a continually repeating sequence. This feature is very useful when the circuit or subsystem needs to be initialized. A "Signal IMB" instruction can be inserted to signal other modules to start acquisition at the time "interesting activity" is started.

Conditional Branch at 50 MHz

With clock speeds of 50 MHz or less, a single "IF block" of vectors can be defined. The "IF condition" can be either a 3-bit input pattern or an IMB (intermodule measurement bus) event. When running repetitively, use of the "IF" instruction will result in a latency time of indeterminate duration between the last and first vectors of the main sequence.

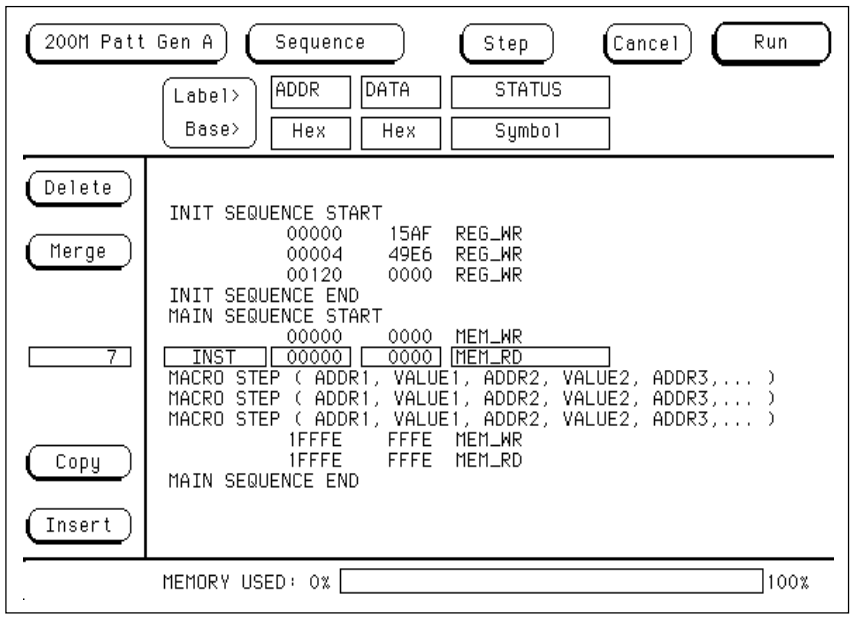


Figure 2.
Stimulus files are defined in the Sequence Menu.

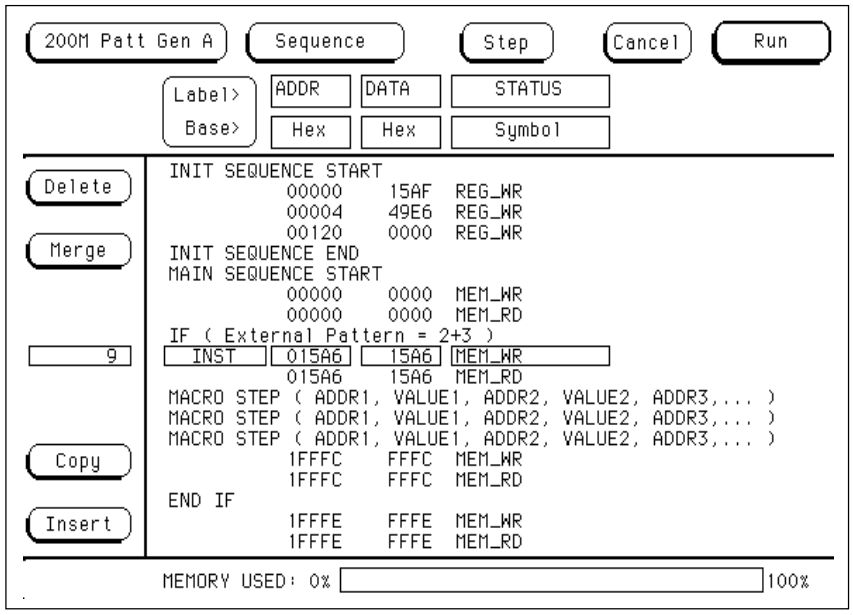


Figure 3.
If the External Pattern is true, the vectors between the IF and END IF are output, otherwise this block is skipped (clock period must be 20 ns or greater)

Macros and Repeat Loops Simplify Creation of Stimulus Programs

Parameterized macros permit you to define a pattern sequence, once, and then insert the macro by name wherever it is needed. Parameters let you create a generic macro. Then, for each instance of the macro, you specify unique values for the parameterized variable. Each macro can have up to 10 parameters. Up to 100 different macros can be defined for use in a single stimulus program.

Repeat loops enable you to repeat a defined block of vectors a specified number of times. The repeat counter can be any value from 1 to 20,000.

Repeat loops and Macros can be nested, except a macro can not be nested within another macro. When nested, each invocation of a repeat loop or a macro is counted towards the 1,000 invocation limit.

A memory utilization indicator helps you track the percent of memory used by the stimulus program.

Convenient Data Entry and Editing Features

You can conveniently enter patterns in hex, octal, binary, decimal, two's complement, or symbolic bases. The data associated with an individual label can be viewed with multiple radixes to simplify data entry.

Delete, Insert, Copy, and Merge commands are provided for easy editing.

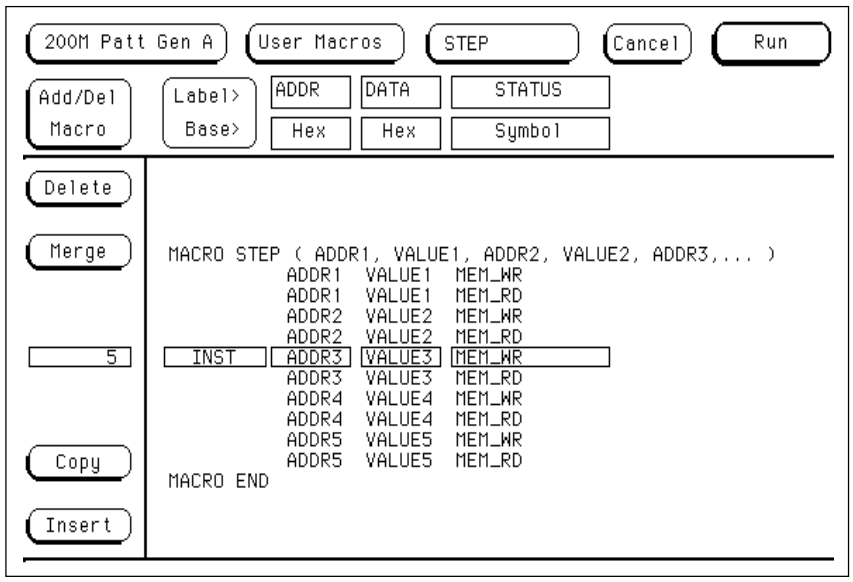


Figure 4.
A macro can be defined once and used whenever the generic pattern is required.

ASCII Input File Format

The HP 16522A supports an ASCII file format which facilitates connectivity to other tools in your design environment. By generating stimulus vectors in this file format, you can read stimulus programs into the pattern generator via the HP 16500B LAN (Local Area Network) connection, via the HP 16500B HP-IB connection, or via the HP 16500B floppy disk drive. This format has been specifically designed for fast file transfer into the HP 16522A pattern generator.

The ASCII format does not support instructions, so WAIT, IF, SIGNAL IMB, and BREAK functionality can not be used.

Macros and Repeat Loops are also not supported, so vectors need to be fully expanded in the ASCII file. This is typically not a problem for machine generated ASCII files.

Data must be in Hex format, and each label must represent a set of contiguous output channels.

Configuration

The HP 16522A requires a single slot in an HP 16500B or 16501A frame (The pattern generator is not compatible with the HP 16500A frame). The pattern generator is designed for operation with the external clock and data pods and lead sets described below. The data pods, clock pods and data cables use standard connectors.

The electrical characteristics of the data cables are also described for users with specialized applications who want to avoid the use of a data pod.

Direct Connection

The pattern generator pods can be directly connected to a standard connector on your system. Use a 3M #2520 Series, or similar connector. The HP 16522A clock or data pods will plug right in.

Short, flat cable jumpers can be used if the clearance around the connector is limited. Use a 3M #3365/20, or equivalent, ribbon cable; a 3M #4620 Series, or equivalent, connector on the HP 16522A pod end of the cable; and a 3M #3421 Series, or equivalent, connector at your target system end of the cable.

Probing Accessories

The probe tips of both the HP 10474A and HP 10347A lead sets plug directly into any 0.1 inch grid with 0.026 inch to 0.033 inch diameter round pins or 0.025 inch square pins. These probe tips work with the HP 5090-4356 surface mount grabbers and with the HP 5959-0288 through-hole grabbers. Other compatible probing accessories are listed in ordering information on page 8.

Pattern Generator Characteristics

Maximum memory depth	258,048 vectors
Number of output channels at ≤200 MHz clock	20
Number of output channels at ≤100 MHz clock	40
Maximum number of "IF Condition" blocks at ≤50 MHz clock	1
Maximum number of different macros	100
Maximum number of lines in a macro	1024
Maximum number of parameters in a macro	10
Maximum number of macro invocations	1,000
Maximum loop count in a repeat loop	20,000
Maximum number of repeat loop invocations	1,000
Maximum number of Wait event patterns	4
Number of input lines to define a pattern	3
Maximum number of HP 16522A modules in a system	5
Maximum width of a vector (in a 5 module system)	200 bits
Maximum width of a label	32 bits
Maximum number of labels	126

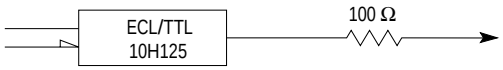
Lead Set Characteristics

HP 10474A 8-channel probe lead set	Provides most cost effective lead set for the HP 16522A clock and data pods. Grabbers are not included.
HP 10347A 8-channel probe lead set	Provides 50 Ω coaxial lead set for unterminated signals, required for HP 10465A ECL Data Pod (unterminated). Grabbers are not included.

Data Pod Characteristics

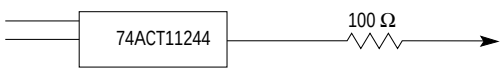
HP 10461A TTL DATA POD

Output type	10H125 with 100 Ω series
Maximum clock	200 MHz
Skew (note 1)	typical < 2 ns; worst case = 4 ns
Recommended lead set	HP 10474A



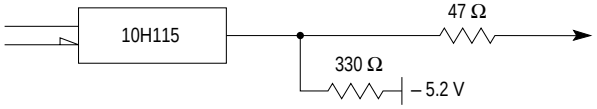
HP 10462A 3-STATE TTL/CMOS DATA POD

Output type	74ACT11244 with 100 Ω series; 10H125 on non 3-state channel 7 (note 2)
3-state enable	negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	100 MHz
Skew (note 1)	typical < 4 ns; worst case = 12 ns
Recommended lead set	HP 10474A



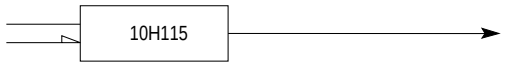
HP 10464A ECL DATA POD (TERMINATED)

Output type	10H115 with 330 Ω pulldown, 47 Ω series
Maximum clock	200 MHz
Skew (note 1)	typical < 1 ns; worst case = 2 ns
Recommended lead set	HP 10474A



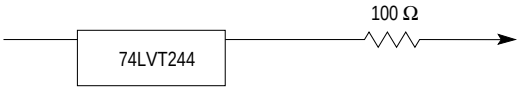
HP 10465A ECL DATA POD (UNTERMINATED)

Output type	10H115 (no termination)
Maximum clock	200 MHz
Skew (note 1)	typical < 1 ns; worst case = 2 ns
Recommended lead set	HP 10347A



HP 10466A 3-STATE TTL/3.3 VOLT DATA POD

Output type	74LVT244 with 100 Ω series; 10H125 on non 3-state channel 7 (note 2)
3-state enable	negative true, 100 KΩ to GND, enabled on no connect
Maximum clock	200 MHz
Skew (note 1)	typical < 3 ns; worst case = 7 ns
Recommended lead set	HP 10474A



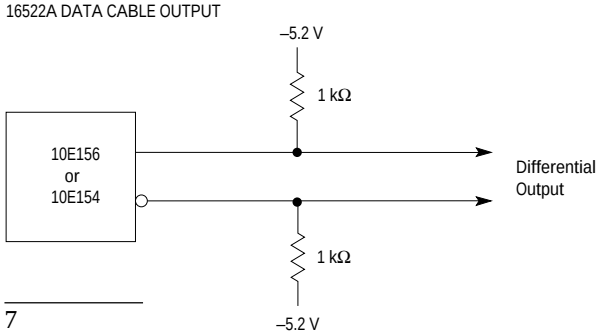
Note 1: Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.

Note 2: Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

Data Cable Characteristics Without a Data Pod

The HP 16522A data cables without a data pod provide an ECL terminated (1 KΩ to –5.2V) differential signal (from a type 10E156 or 10E154 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).

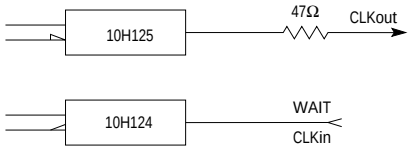
16522A DATA CABLE OUTPUT



Clock Pod Characteristics

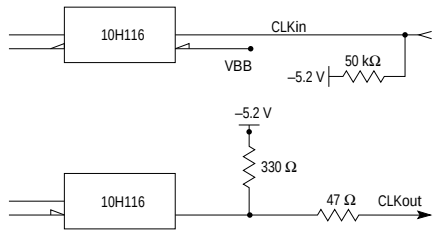
10460A TTL CLOCK POD

Clock output type	10H125 with 47 Ω series; true & inverted
Clock output rate	100 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	TTL – 10H124
Clock input rate	dc to 100 MHz
Pattern input type	TTL – 10H124 (no connect is logic 1)
Clock-in to clock-out	approximately 30 ns
Pattern-in to recognition	approx. 15 ns + 1 clk period
Recommended lead set:	HP 10474A



10463A ECL CLOCK POD

Clock output type	10H116 differential unterminated; and differential with 330 Ω to –5.2V and 47 Ω series
Clock output rate	200 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	ECL – 10H116 with 50 KΩ to –5.2v
Clock input rate	dc to 200 MHz
Pattern input type	ECL – 10H116 with 50 KΩ (no connect is logic 0)
Clock-in to clock-out	approximately 30 ns
Pattern-in to recognition	approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



Ordering Information

Note: Please order at least one clock pod for each HP 16522A used as a master, and at least one data pod for every eight (8) output channels. This typically means at least five data pods for each HP 16522A.

HP 16522A 200 M Vector/s Pattern Generator (requires an HP 16500B mainframe)
Option 0B0 - Delete Manual Set
Option 011 - TTL Clock Pod and Lead Set (1 ea 10460A + 1 ea 10474A)
Option 012 - 3-state TTL/3.3V Data Pod and Lead Set (1 ea 10466A + 1 ea 10474A)
Option 013 - 3-state TTL/CMOS Data Pod and Lead Set (1 ea 10462A + 1 ea 10474A)
Option 014 - TTL Data Pod and Lead Set (1 ea 10461A + 1 ea 10474A)
Option 021 - ECL Clock Pod and Lead Set (1 ea 10463A + 1 ea 10474A)
Option 022 - ECL (terminated) Data Pod and Lead Set (1 ea 10464A + 1 ea 10474A)
Option 023 - ECL (unterminated) Data Pod and Lead Set (1 ea 10465A + 1 ea 10347A)
HP 10460A TTL Clock Pod for 16522A
HP 10461A 8-channel TTL Data Pod for 16522A
HP 10462A 8-channel 3-state TTL/CMOS Data Pod for 16522A
HP 10463A ECL Clock Pod for 16522A
HP 10464A 8-channel ECL (terminated) Data Pod for 16522A
HP 10465A 8-channel ECL (unterminated) Data Pod for 16522A (use HP 10347A lead set)
HP 10466A 8-channel 3-state TTL/3.3V Data Pod for 16522A
HP 10474A 8-channel Probe Lead Set for 16522A
HP 10347A 8-channel (50-ohm Coaxial) Probe Lead Set
HP 5090-4356 Grabbers, surface mount (package of 20)
HP 5959-0288 Grabbers, through-hole (package of 20)
HP 10211A IC probe clip, 24-pin dual in-line package
HP 10024A IC probe clip, 16-pin dual in-line package
HP E2421A SOIC Clip Adapter test kit (Pomona 5514)
HP E2422A Quad Clip Adapter test kit (Pomona 5515)

For more information on Hewlett-Packard Test & Measurement products, applications or services please call your local Hewlett-Packard sales offices. A current listing is available via Web through Access HP at http://www.hp.com. If you do not have access to the internet, please contact one of the HP centers listed below and they will direct you to your nearest HP representative.

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