

E4219A ATM Network Impairment Emulator

The HP Broadband Series Test System Technical Specification

1. Product Description

Part of the modular HP Broadband Series Test System (BSTS), the E4219A ATM Network Impairment Emulator module provides the capability to insert cell loss, cell error, cell misinsertion, cell delay and cell delay variation impairments into an ATM cell stream at rates up to 155 Mb/s.

Ideal for network equipment manufacturers, service providers, R&D labs and CPE vendors, the ATM Network Impairment Emulator emulates real-world effects of impairments in an ATM network.

Key Features

Emulates real-world impairments

 Inserts constant cell delay, cell delay variation, cell loss, cell error and cell misinsertion into an ATM cell stream

Impairment distributions

 Several statistical distributions, including user-defined, are available for cell error, cell loss, cell delay variation and cell misinsertion

Wide delay range

- Up to 220 ms (+/-3 %) cell delay at 155 Mb/s
- ◆ Up to 2.57 ms (+/-3 %) cell delay variation at 155 Mb/s

User-program environment

 Write your own C-language user programs for automated testing

Filter on any cell header

 Select impaired cell streams by field filtering on any ATM cell header field

Works with CPP

 Works with an E4209B Cell Protocol Processor to insert additional traffic such as signalling

Cascadable

 Cascade up to four modules to increase total delay or provide impairments for additional VPI/VCIs

Full regulatory approval

Meets EMI emission standards

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1.2) Applicable Standards *Impairments*

ITU-T Recommendation I.356, B-ISDN ATM Cell Layer Cell Transfer Performance, 1993

ATM

ITU-T Recommendation I.361 B-ISDN ATM Layer Specification, 1993; ITU-T Recommendation I.150 B-ISDN ATM Functional Characteristics, 1993

1.3) Use With Other BSTS Line Interfaces, Hardware Modules & Test Software

When installed in a BSTS chassis, the E4219A ATM Network Impairment Emulator can emulate impairments with all BSTS ATM-based line interfaces at rates up to 155 Mb/s.

to 133 MD/S.		
Speed	Line Interface	
1.5 Mb/s	E1616A 1.5/45 Mb/s (T1/T3) Line Interface	
2 Mb/s	E4201A 2.048 Mb/s (E1) Line Interface	
6.3 Mb/s	E1613A 6.3 Mb/s Electrical Line Interface	
	E1614A 6.3 Mb/s Optical Line Interface	
25.6 Mb/s	E1619A 25.6 Mb/s (4B/5B) Line Interface	
34 Mb/s	E1610A 34 Mb/s (E3) Line Interface	
45 Mb/s	E1616A 1.5/45 Mb/s (T1/T3) Line Interface	
	E1695A 45 Mb/s (T3) Line Interface	
52 Mb/s	E1617A 52 Mb/s (OC-1) Line Interface	
155 Mb/s	E1612A 155 Mb/s Electrical Line Interface	
	E1697A 155 Mb/s (SONET/SDH) Optical Line Interface	
	E4203A 155 Mb/s Protocol Line Interface	
	E4205A 155 Mb/s (UTP-5) Line Interface	

Additionally, this module can be used with an optional E4209B Cell Protocol Processor and test software to provide test capabilities at the ATM, AAL and Services layers.

Several test software packages are available for traffic analysis, simulation, signalling, performance and conformance testing. See the following technical specifications for more information.

- E4209B Cell Protocol Processor Technical Specifications publication 5963-7403E
- ◆ E4211A SMDS Test Software Technical Specifications, publication 5963-7402E
- ◆ E4212A AAL Test Software Technical Specifications, publication 5963-7401E
- ◆ E4214A LAN Protocols Test Software Technical Specifications, publication 5963-7398E
- ◆ E4215A UNI Signalling Test Software Technical Specifications, publication 5963-7399E
- ◆ E4226A MPEG-2 Protocol Viewer Test Software Technical Specifications publication 5964-2107E

1.4) User Programming

You can automate testing or set up complex scenarios by executing your own programs on the BSTS's embedded UNIX® controller.

Access the E4219A ATM Network Impairment Emulator by simply linking your code with a library of test routines. A UNIX workstation environment is provided on the BSTS, including networking tools and utilities.

1.5) Documentation Included

- ◆ User's Guide
- Programmer's Guide

2. Impairment Emulation

2.1 Impairment Independent Parameters

Channel Parameters

Total bandwidth	Up to 149.76 Mb/s
Modes	UNI or NNI
Empty Cell Definition	Idle or unassigned

ATM Header Matching or Misinsertion Values

VCI	Any value 0 to 65536
VPI	Any value 0 to 255 (UNI) or 0 to 4095 (NNI)
GFC	Any value 0 to 15 (UNI)
Payload type	Any value 0 to 7
Cell loss priority	Set priority to 1 or 0
Cell type	ATM

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2.2 Variable Cell Delay

Variable cell delays are caused by congestion, cell blocking and multiplexing. Delays can be specified in milliseconds or multiples of four cells; delay scales as a function of line rate. There is an inertial delay associated with the data path of the E4219A which should be calibrated as described in the product documentation.

Distributions	Parameter/s
Binomial	User-specified mean & standard deviation
Geometric	User-specified mean
User Defined	User-specified X,Y pairs representing desired probability density function
Variable Cell De	elav Range

CDV 0 to 926 cells

To quickly estimate maximum cell delay variation in seconds, divide 392,624 bits (926 cells x 53 octets per cell x 8 bits per octet) by line rate. Note that

this calculation ignores any additional framing bits.

2.3 Constant Cell Delay

Constant cell delay results from fixed network delays, such as lengthy transmission distances and switching delays.

Constant Cell Delay Range CD 0 to 79.136 cells

To quickly estimate maximum constant cell delay in seconds, divide 33,553,664 bits (79,136 cells x 53 octets per cell x 8 bits per octet) by line rate. Note that this calculation ignores any additional framing bits.

2.4 Cell Error

Cell errors are caused by bit errors caused by line noise. Errored bytes are selected from the payload according to the specified distribution. The E4219A module can introduce up to four consecutive bit errors. The header cannot be errored. Errors can be specified in terms of cells or bytes.

Distributions	Parameter/s
Normal	User-specified mean error interval from 5 to 2E10 cells or 1000 to 1E12 bytes with user-specified standard deviation
Exponential	User-specified mean error interval from 5 to 2E10 cells or 1000 to 1E12 bytes
Deterministic	User-specified cell error rate from 5E-11 to 2E-1; byte error rate from 1E-12 to 1E-3.
Uniform	User-specified lower error interval limit of 5 cells or 1000 bytes; user-specified upper error interval limit of 2E10 cells or 1E12 bytes
User Defined	User-specified X,Y pairs representing error intervals from 5 to 2 ³² -1 cells or 1000 to 2 ³² -1 bytes with associated probability from 0.0 to 1.0

2.5 Cell Loss

Cell loss results from such network problems as buffer overflow, switch malfunction, traffic policing, and uncorrectable header errors. The E4219A module can introduce bursts of up to eight consecutive cell losses. Lost cells can be replaced either by idle cells or by cells with user defined headers.

Distributions	Parameter/s
Normal	User-specified mean error interval from 1000 to 1E12 cells with user-specified standard deviation
Exponential	User-specified mean error interval from 1000 to 1E12 cells
Deterministic	User-specified cell error rate from 1E-12 to 1E-3

Uniform	User-specified lower limit of error interval 1000 cells; user-specified upper error interval limit of 1E12 cells
User Defined	User-specified X,Y pairs representing error intervals from 1000 to 2 ³² -1 cells with associated probability from 0.0 to 1.0

2.6 Cell Misinsertion

Cell misinsertion is caused by transmission errors and situations where an undetected header error matches an existing VPI/VCI.

The header of the misinserted cell can be fully specified by the user.

The first two and last two payload octets of the misinserted cell can be independently specified.

A fill pattern for payload bytes 3-46 can also be specified.

Distributions	Parameter/s
Normal	User-specified mean error interval from 1000 to 1E12 cells with user-specified standard deviation
Exponential	User-specified mean error interval from 1000 to 1E12 cells
Deterministic	User-specified cell error rate from 1E-12 to 1E-3
Uniform	User-specified lower error interval limit of 1000 cells; user-specified upper error interval limit of 1E12 cells
User Defined	User-specified X,Y pairs representing error intervals from 1000 to 2 ³²⁻¹ cells with associated probability from 0.0 to 1.0

3. External Triggers

External TTL trigger pulses may be output through the connector on the E4219A front panel. This allows the module to work in conjunction with other hardware. Triggers can be output under the following circumstances.

Variable Cell Delay	The delay value changes
Cell Misinsertion	A cell has been misinserted by the module
Cell Error	A byte or cell has been errored by the module
Cell Loss	A cell has been lost by the module
Constant Cell Delay	A cell has been delayed by the module
Incoming	The module detects an incoming non-empty cell
Outgoing Non-Empty Cell	The module detects an outgoing non-empty cell

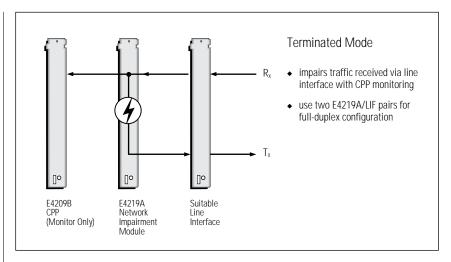
4. Configuration Modes

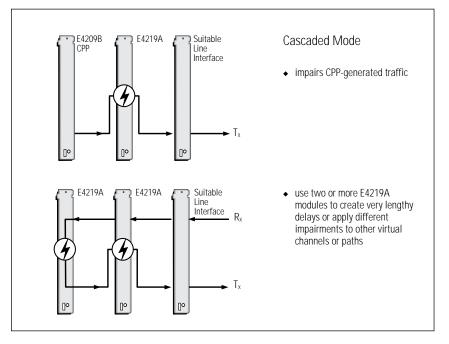
Terminated

Default interface mode; cells received through the cell bus from the module on the right are impaired by the E4219A, then looped back through the cell bus to the same module on the right.

Cascaded

Default interface mode when the test application includes another module located to the left of the E4219A (i.e. a CPP).
Cells received through the cell bus from the module on the right pass through the E4219A without sampling or modification. Cells received through the cell bus from the module on the left are impaired by the E4219A, then sent through the cell bus to the next module on the right.





Disabled

This mode is used when the E4219A is to be temporarily removed from the application without having to stop the application and start a new one. Cells received through the cell bus from modules to the right or left pass through the E4219A modification.

5. Input and Output

5.1) I/O Connectors

Trigger Out	TTL output; BNC socket
Test out	TTL output; BNC socket

5.2) LED Status Indicators

Status LED	Color	Indicator Description
Failed	Red	Lights during startup; if the module passes the self-test, the light turns off; otherwise it stays lit
Access	Green	Module is currently being accessed by the VXI control bus
CDV	Green	Variable cell delay impairments are enabled
	Red	A change in delay has been introduced by the module
Cell Error	Green	Cell error impairments are enabled
	Red	A byte or cell has been errored by the module
Cell Drop	Green	Cell loss impairments are enabled
	Red	A cell has been lost by the module
Cell Misinsert	Green	Cell misinsertion impairments are enabled
	Red	A cell has been misinserted by the module
Cell Delay	Green	Constant cell delay impairments are enabled
	Red	A cell has been delayed by the module

6. Physical Specifications

6.1) VXIbus Characteristics

Device type	Register based
Backplane connectors	P1 and P2 (as per VXIbus Specification Rev 1.3)
Local bus LBUSA	Active connection to and LBUSC
Module keying	ECL
Power dissipation	25 W max

6.2) Size and Weight

Size	1 C-sized slot
Weight	1.5 kg (2.9 lb) nominal

6.3) Operating Environment

	•	
Operating temperature		0 to 55 degrees C
Storage temperature		-40 to 75 degrees C
Humidity		5% RH over O degrees C
Safety	61010:1	ns with EN 1993 / IEC 1990 + A1
EMC	55011:1 (Group EN 500 (IEC 801	ns with EN 1991/CISPR 11:1990 1, Class A), 82-1:1992 1-2:1991; -3:1984; -4:1988)

7. Ordering Information

Part number	Description
E4219A	ATM Network Impairment Emulator; includes module and documentation
E4219A-002	Additional User's Guide
E4219A-003	Additional Programmer's Guide



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8. For More Information

For an introduction to the modular Broadband Series Test System, please see brochure 5962-9751E. An ordering guide, publication 5964-0393E, helps you determine the appropriate system configuration for your testing needs. Technical specifications detailing other hardware modules and test software packages for the BSTS are also available. To find the location of your local HP sales office, please contact the nearest regional sales headquarters listed to the right.

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