HP 64784A and 64797A Emulators for Hitachi H8/300H Series Microprocessors

Product Overview

Design, debug, and integrate real-time embedded systems

The HP 64784A emulator supports Hitachi H8/3001/02/03/04/05, 3030/31/32, and 3040/41/42 microprocessors of H8/300H Series up to 16 MHz.* The HP 64797A emulator supports Hitachi H8/3044/47/48/48F microprocessors up to 18 MHz. Both emulators support emulation in both 3 V and 5 V versions. They offer the real-time measurement capabilities needed to develop H8/300H Series embedded systems, including interpreted displays of on-chip registers, emulation memory, a deep-trace analyzer, and hardware break events.

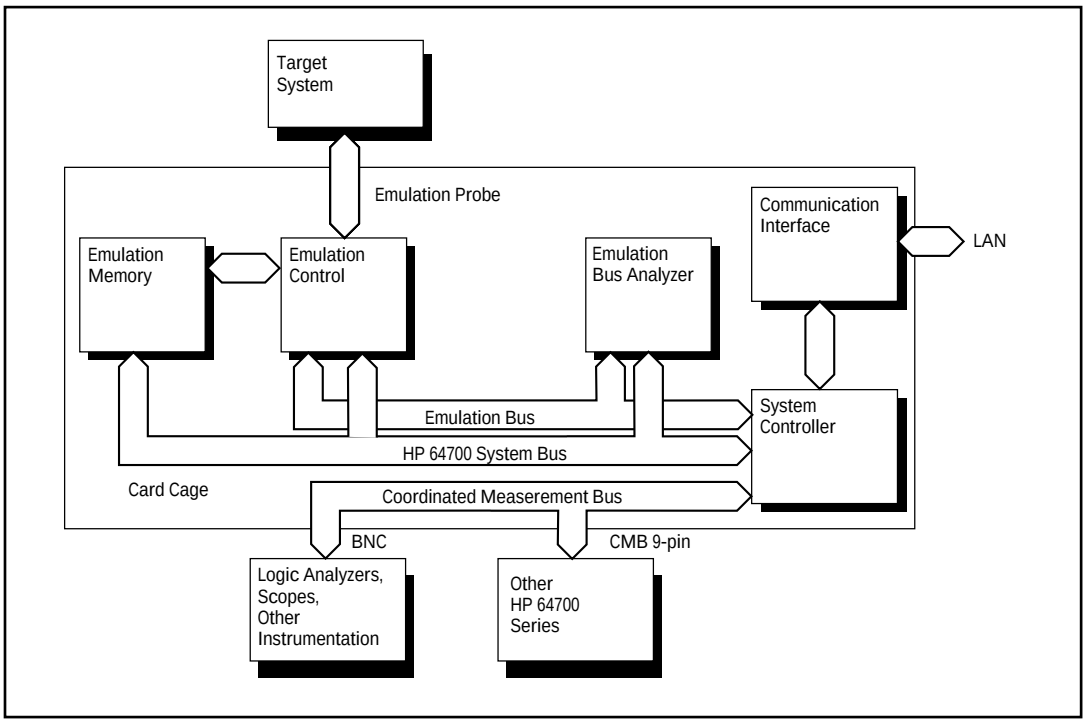
HP's host-independent emulation and analysis systems can be controlled from a simple terminal, HP 9000 workstations, or Sun SPARCstations. Access to these systems is through a selection of user interfaces, including an X/Motif based embedded debug environment for HP workstations and Sun SPARCstations. This allows you to open several emulation and analysis windows for simultaneous display during a session, providing visibility on several parameters at once.

HP 64784A Features

- Support for 5-V and 3-V processor versions by the HP 64797B low-voltage adapter
- No- wait state execution up to 16 MHz* at 5 V, and 10 MHz* at 3 V, using with HP 64797B low-voltage adapter
- Support for H8/3001/02/03/04/05, 3030/31/32, and 3040/41/42 processors
- Configuration menu for easy emulator setup
- Display and modify functions for internal I/O registers
- Background monitor
- Eight real-time hardware break events
- Unlimited software execution breakpoints
- Termination to 112-pin QFP, 100-pin QFP, or 80-pin QFP packages by exchanging a flexible probe cable
- Flexible probing to target system by 9-inch flexible probe cable
- Two-foot probe cable to the adapter
- QFP socket adapter, soldered on target system, for both the emulator probe and a QFP real chip
- Simulated I/O (on workstation)
- Cross-triggering from another emulator, logic analyzer, or oscilloscope
- Support for Hitachi assembler and compiler on HP 9000 Series 300/400/700 and Sun SPARCstations
- Support for IAR SYSTEMS AB assembler and compiler on HP 9000 Series 700 and Sun SPARCstations.

*Contact your HP 64000 field engineer for the latest configuration information and supported processor speeds.

Modular HP 64700 Series system



HP 64700 Series development tools include emulators and emulation bus analyzers.

HP 64797A Features
- Support for 5-V and 3-V processor versions by the HP 64797B low-voltage adapter
- No-wait state execution up to 18 MHz* used with HP 64729A 2 MB emulation memory and 16 MHz* used with HP 64727A 512 KB emulation memory
- No-wait state execution up to 13 MHz* at 3 V used with HP 64797B low-voltage adapter
- Support for H8/3044/47/48/48F processors
- Support for on-board programming of internal flash memory by substituting emulation memory
- Configuration menu for easy emulator setup
- Display and modify functions for internal I/O registers
- Background monitor
- Eight real-time hardware break events
- Unlimited software execution breakpoints
- Termination a 100-pin QFP package
- Flexible probing to target system by 9-inch flexible probe cable
- Two-foot probe cable to the adapter
- QFP socket adapter, soldered on target system, for both the emulator probe and a QFP real chip
- Simulated I/O (on workstation)
- Cross-triggering from another emulator, logic analyzer or oscilloscope
- Support for Hitachi assembler and compiler on HP 9000 Series 300/400/700 and Sun SPARCstations
- Support for IAR SYSTEMS assembler and compiler on HP 9000 Series 700 and Sun SPARCstations

Emulation Bus Analyzer
- 80 channels available with trace buffer depths of 1 K, 8 K, 64 K, or 256 K
- 64 channels available with 16 external channels and trace bugger depth of 1 K
- Postprocessed software-based dequeued trace with symbols and source lines
- Eight events, each consisting of address, status, and data comparators
- Events that can be sequenced up to 8 levels deep
- Time tag with 20-ns resolution (64794x) and state counts
- Prestore capability

Emulation Memory
- Dual-ported emulation memory to allow modification and display without processor interruption
- 512-KB and 2-MB memory configurations
- Mapping in 512-byte block

Software Support
- Real-time operating system measurement tools

* Contact your HP 64000 field engineer for the latest configuration information and supported processor speeds

Card Cage
The card cage is the basis for modular emulators and analyzers. It can be disassembled easily for cost-saving reconfiguration to support 8-, 16-, and 32-bit processors.

The card cage host control card contains LAN capability, along with RS-232-C/RS-422 serial port and system configuration firmware. System, emulation, and analysis firmware are always resident and may be updated.

Networking
In many embedded design environments, it is not possible for each member of a design team to have a target system and an emulator, which makes remote access from a networked host essential. The HP 64700 Series emulators offer a LAN connection so that you can share a central emulator and target from either a PC or a workstation. In addition, the rapid file transfers—rates of up to 6 MB per minute—can increase your productivity. The card cage connects to all popular Ethernet/803.2 networks through a 10Base2 ThinLAN BNC connector or a 15-pin AUI (attachment unit interface). The system supports TCP/IP protocols, LAN gateways and ARPA/Berkeley standards.

Emulation Bus Analysis
Emulation bus analysis provides real-time, nonintrusive operation along with extensive triggering, tracing, and qualification features. Analysis features include selective tracing, time-tagging, prestore and a selection of 1-K, 8-K, 64-K, or 256-K trace depths. These comprehensive resources combine to help you solve both simple and complex problems.

The dual-bus architecture results in real-time, nonintrusive analysis. You can set up and review traces without breaking processor execution. Selective tracing of microprocessor code flow without breaking execution is a major strength of the HP 64700 Series emulators and analyzers.

You can combine up to eight hardware breakpoint resources, each consisting of address, data, and status event comparators, in sequential trace specifications using “find A, followed by B...” constructs up to eight levels deep. Apply a range comparator to address or data events at any one of these levels. The analyzer will trigger on and store all subsequent executions or store only specified execution information.

Precise time-tagging of events helps you identify discrepancies in code execution. The analyzer logs each event with its execution time. Bus cycle, instruction, and module duration can be measured at full processor speeds.

Prestore helps assists you pinpoint possible problem areas in your coding by determining which of several different functions is accessing a variable and is responsible for corrupting it.

Real-Time Emulation
The HP 64784A and 64797A contains the microprocessor, emulation monitor, run-control circuits, and up to 2 MB of dual-port emulation memory. The included background monitor uses no target address space.

HP high-speed emulation memory provides you with no-wait state real- time execution; dual ports let you display and modify emulation memory locations without interrupting target processor execution. All of these features give you considerable flexibility in a nonintrusive development environment.

Extensive breakpoint capabilities are included, allowing you to define where to stop code execution. Software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point.

Real-time hardware break events increase the flexibility and power of this feature, extending functionality to include stopping at processor address, data, status points, or a combination of all three.

Flexible Memory Configuration
Emulation memory is available as replacement memory in your embedded design in 512-KB or 2-MB sizes mappable in 512-byte blocks.

Symbolic Support
Symbolic debugging clarifies trace -list interpretation by allowing you to see program symbols in the trace list. This feature facilitates quick identification of problems involving the interaction of software and hardware. You can also use symbols in emulation commands and expressions to simplify command entries and user interaction.

Workstation-Hosted Environment
The HP embedded debug environment is an emulator/analyzer user interface for software development.

The emulator/analyzer tool gives you the ability to perform trace analysis, set breakpoints, and establish emulator configuration parameters. In addition, the graphical interface tool is integrated with the embedded debug environment, which coordinates high-level microprocessor run control.

The HP debug environment supports language tools from Hitachi and IAR SYSTEMS, which provide software tools compatible with the HP 64784A and HP 64797A emulators. The Hitachi toolset includes a C cross-compiler and assembler hosted on HP 9000 Series 300/400/700 and Sun SPARCstations. The IAR SYSTEMS toolset includes a C cross-compiler and assembler hosted on HP 9000 Series 700 and Sun SPARCstations.

Terminal Mode Operation
A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; the system accepts file transfers using industry-standard formats. Because a terminal can access these commands, host independence is realized.

HP 64784A, 64797A, and 64797B Specifications

Processor Compatibility

Model 64784A:
Hitachi H8/3001/02/03/04/05, 3030/31/32, and 3040/41/42
Model 64797A:
Hitachi H8/3044/47/48/48F

Electrical	
Maximum Clock Speed:	64784A (5 V) : 16 MHz 64784A (3 V) : 10 MHz 64797A (5 V) : 18 MHz * 16 MHz * 64797A (3 V) : 13 MHz with no-wait states required for emulation or target system memory.

* 18 MHz used with HP 64729A 2-MB emulation memory and 16 MHz used with HP 64727A 512-KB emulation memory

Minimum Clock Speed:	64784A : 0.5 MHz 64797A : 1 MHz
Power:	Primary power supplied by card cage
Environmental	
Temperature:	Operating, 0 to +40 °C (+32 to +104 F); Non-operating, –40 to +60 °C (–40 to 140 F)
Altitude:	Operating, 4600 m (15,000 ft); Non-operating, 15300 m (50,000 ft)

Regulatory Compliance
when installed in HP 64700 card cage

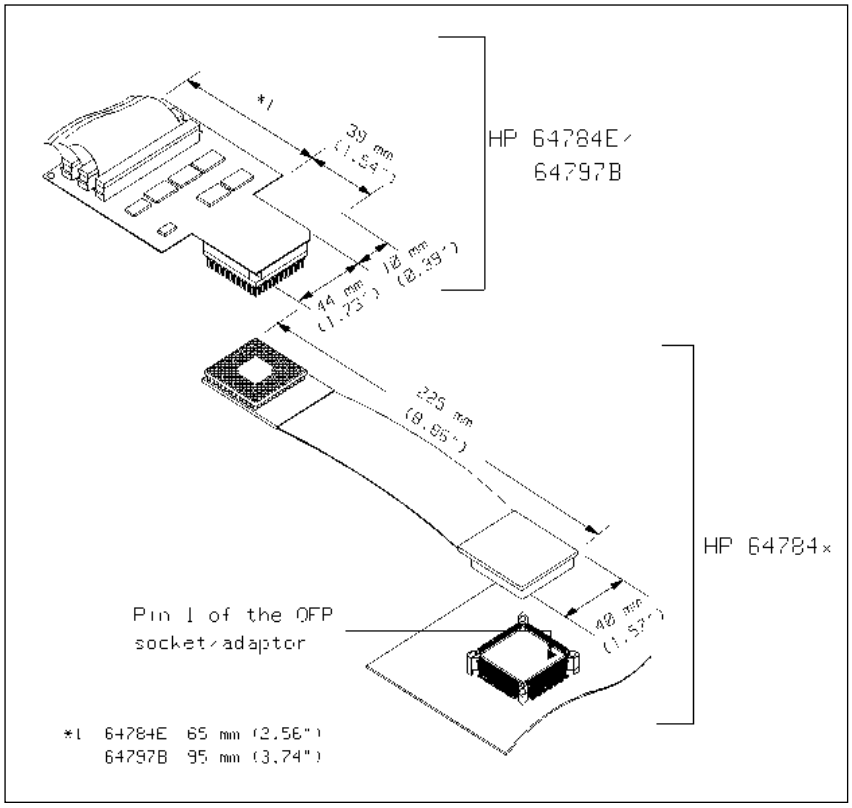
Electromagnetic Interference:	EN55011 Group1 Class A
Safety:	64784A is self-certified to UL 1244, IEC 348, and CSA-556B 64797A is self-certified to UL 1244, IEC 1010, and CSA-1010

Physical

Cable length:	Probe to card cage approximately 1 m (40")
Dimensions: see drawings at right	

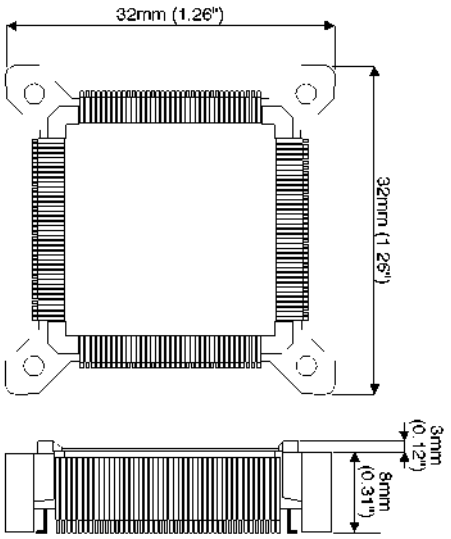
HP 64797B Low-Voltage Adapter Electrical Specification

Operation Voltage:	2.7 – 5.25 V
Input high voltage (Vih):	
Item	Minimum (V)
/RES, /STBY, NMI, MD0, MD1, MD2	Vcc x 0.9 V
P1 – P5, D0 – D15	Higher of (Vcc x 0.7) and 2.4 V
Others	Higher of (Vcc x 0.7) and 2.0 V

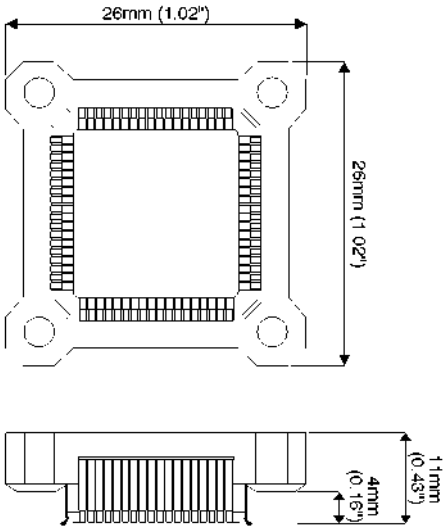


Adapters and Cable Dimensions

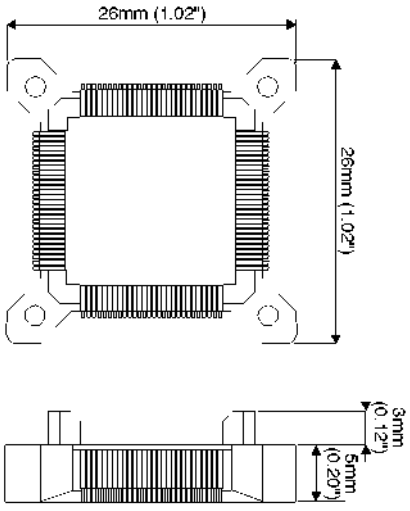
HP 64784A, 64797A, and 64797B Specifications (continued)



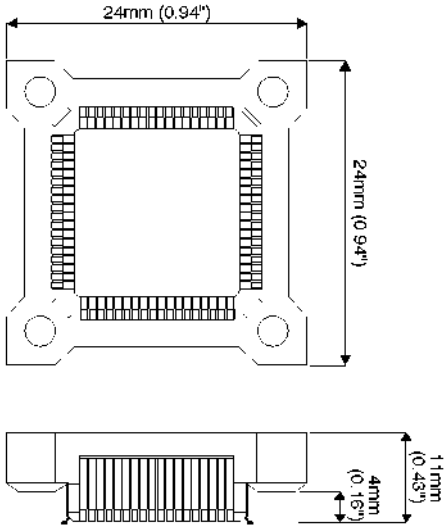
QFP Socket Adapter Dimensions for
HP 64784C and F (HP P/N 64784-61611)



QFP Socket Adapter Dimensions for
HP 64784D and G (HP P/N 64784-61612)



QFP Socket Adapter Dimensions for
HP 64784H and K (HP P/N 64784-61613)



QFP Socket Adapter Dimensions for
HP 64784J (HP P/N 64784-61614)

Notice for the QFP Socket Adapter
The QFP socket adapter is an expendable supply because the electrical contacts degrade gradually as the flexible probe cables attached and detached. One QFP socket adapter is supplied with each of HP 64784C, D, F, G, H, J, and K. Please prepare some spares of the QFP socket adapter in advance.

HP 64784A AC Timing Specifications
Vcc = 5 V, f = 16 MHz

Characteristics	Symbol	H8/3003		Probe Type				Unit
		Vcc = 5 V, f = 16 MHz		64784E and 64784x		64784C/D		
		min.	max.	Typical*	Worst	Typical*	Worst	
Clock cycle time	tCYC	62.5	500	–	–	–	–	ns
Clock low pulse width	tCL	20	–	23.2	12.9	23.8	13.3	ns
Clock high pulse width	tCH	20	–	28.3	12.9	28.3	13.3	ns
Clock rise time	tCR	–	10	5.6	17.1	5.0	16.7	ns
Clock fall time	tCF	–	10	5.4	17.1	5.4	16.7	ns
Address delay time	tAD	–	30	24.0	33.5	23.6	32.0	ns
Address hold time	tAH	10	–	41.0	–4.8	41.2	–5.2	ns
Address strobe delay time	tASD	–	30	7.4	35.8	6.6	34.7	ns
Write strobe delay time	tWSD	–	30	10.0	35.8	9.6	34.7	ns
Strobe delay time	tSD	–	30	2.8	35.8	3.0	34.7	ns
Write data strobe pulse width 1	tWSW1	35	–	53.0	28.6	53.8	29.1	ns
Write data strobe pulse width 2	tWSW2	65	–	83.0	58.6	83.8	59.1	ns
Address setup time 1	tAS1	10	–	9.8	–24.1	10.6	–23.2	ns
Address setup time 2	tAS2	40	–	41.4	5.9	42.2	6.8	ns
Read data setup time	tRDS	20	–	30.4	49.7	24.0	47.3	ns
Read data hold time	tRDH	0	–	–27.0	29.7	–20.6	33.3	ns
Write data delay time	tWDD	–	60	29.0	68.7	29.8	69.9	ns
Write data setup time 1	tWDS1	35	–	31.0	–4.8	30.0	–6.6	ns
Write data setup time 2	tWDS2	5	–	3.2	–36.0	2.4	–37.8	ns
Write data hold time	tWDH	20	–	47.2	4.4	47.6	5.8	ns
Read data access time 1	tACC1	–	55	42.4	21.3	51.2	24.8	ns
Read data access time 2	tACC2	–	115	104.0	83.8	112.8	87.2	ns
Read data access time 3	tACC3	–	25	25.8	–12.3	33.4	–9.2	ns
Read data access time 4	tACC4	–	85	87.2	50.2	94.8	53.3	ns
Pre-charge time	tPCH	35	–	62.8	28.6	62.8	29.1	ns
WAIT setup time	tWTS	25	–	26.2	60.9	22.6	54.7	ns
WAIT set hold time	tWTH	5	–	–23.6	–11.0	–20.0	–6.1	ns
BREQ setup time	tBRQS	40	–	–	75.9	–	69.7	ns
BACK delay time 1	tBACD1	–	30	10.4	35.8	10.0	34.7	ns
BACK delay time 2	tBACD2	–	30	–4.2	35.8	–4.0	34.7	ns
Bus floating time	tBZD	–	40	19.0	46.2	20.4	44.7	ns
/RAS delay time 1	tRAD1	–	30	23.6	41.6	17.8	39.0	ns
/RAS delay time 2	tRAD2	–	30	22.2	41.6	16.2	39.0	ns
/RAS delay time 3	tRAD3	–	30	8.0	41.6	6.6	39.0	ns
Row address hold time	tRAH	15	–	22.0	–10.5	27.0	–9.5	ns
/RAS pre-charge time	tRP	35	–	60.8	25.8	61.4	26.7	ns
/CAS to /RAS pre-charge time	tCRP	35	–	61.4	28.6	60.2	29.1	ns
/CAS pulse width	tCAS	40	–	52.8	33.6	53.2	34.1	ns
/RAS access time	tRAC	–	85	74.4	44.4	82.8	49.0	ns
Address access time	tAA	–	55	42.4	21.3	51.2	24.8	ns
/CAS access time	tCAC	–	25	23.0	–12.3	30.6	–9.2	ns
Write data setup time 3	tWDS3	40	–	33.8	–4.8	33.4	–6.6	ns
/CAS setup time	tCSR	15	–	24.2	11.6	24.2	11.0	ns
Read strobe delay time	tRSD	–	30	9.0	35.8	9.6	34.7	ns
/RES setup time	tRESS	200	–	–	281.9	–	275.7	ns
/RES pulse width	tRESW	10	–	–	–	–	–	tcyc
/RESO output delay time	tRESD	–	100	–	109.6	–	108.4	ns
/RESO output pulse width	tRESOW	132	–	–	–	–	–	tcyc
NMI setup time	tNMIS	150	–	–	231.9	–	225.7	ns
NMI hold time	tNMIH	10	–	–	–9.0	–	–4.1	ns
Interrupt pulse width	tNMIW	200	–	–	209.2	–	208.3	ns
Crystal oscillator setting time (reset)	tOSC1	20	–	–	–	–	–	ms
Crystal oscillator setting time (software standby)	tOSC2	8	–	–	–	–	–	ms

*Typical outputs measured with 50 pF Load

HP 64784A AC Timing Specifications
Vcc = 3 V, f = 10 MHz

Characteristics	Symbol	H8/3003 Vcc=3V, f=10MHz		Probe Type 64797B and 64784x		Unit
		min.	max.	Typical*	Worst	
Clock cycle time	tCYC	100	500	–	–	ns
Clock low pulse width	tCL	30	–	42.8	31.5	ns
Clock high pulse width	tCH	30	–	46.0	31.5	ns
Clock rise time	tCR	–	15	4.8	17.3	ns
Clock fall time	tCF	–	15	6.4	17.3	ns
Address delay time	tAD	–	50	23.0	33.9	ns
Address hold time	tAH	20	–	42.2	12.6	ns
Address strobe delay time	tASD	–	40	7.8	36.6	ns
Write strobe delay time	tWSD	–	50	10.4	36.6	ns
Strobe delay time	tSD	–	50	3.4	36.6	ns
Write data strobe pulse width 1	tWSW1	60	–	88.7	64.7	ns
Write data strobe pulse width 2	tWSW2	110	–	137.5	113.4	ns
Address setup time 1	tAS1	15	–	29.4	–6.3	ns
Address setup time 2	tAS2	65	–	79.7	42.4	ns
Read data setup time	tRDS	35	–	38.4	52.6	ns
Read data hold time	tRDH	0	–	–35.0	28.7	ns
Write data delay time	tWDD	–	75	27.8	69.4	ns
Write data setup time 1	tWDS1	65	–	68.1	31.4	ns
Write data setup time 2	tWDS2	10	–	23.1	–18.6	ns
Write data hold time	tWDH	20	–	66.3	22.0	ns
Read data access time 1	tACC1	–	100	107.8	74.4	ns
Read data access time 2	tACC2	–	200	206.9	174.4	ns
Read data access time 3	tACC3	–	50	72.2	21.7	ns
Read data access time 4	tACC4	–	150	171.1	121.7	ns
Pre-charge time	tPCH	60	–	100.3	64.7	ns
WAIT setup time	tWTS	40	–	30.2	63.1	ns
WAIT set hold time	tWTH	10	–	–27.6	–13.0	ns
BREQ setup time	tBRQS	40	–	–	78.1	ns
BACK delay time 1	tBACD1	–	50	10.8	36.6	ns
BACK delay time 2	tBACD2	–	50	–4.0	36.6	ns
Bus floating time	tBZD	–	70	17.8	46.6	ns
/RES setup time	tRESS	200	–	–	284.1	ns
/RES pulse width	tRESW	10	–	–	–	tcyc
/RESO output delay time	tRESD	–	100	–	110.3	ns
/RESO output pulse width	tRESOW	132	–	–	–	tcyc
NMI setup time	tNMIS	150	–	–	234.1	ns
NMI hold time	tNMIH	10	–	–	–11.0	ns
Interrupt pulse width	tNMIW	200	–	–	209.2	ns
Crystal oscillator setting time (reset)	tOSC1	20	–	–	–	ns
Crystal oscillator setting time (software standby)	tOSC2	8	–	–	–	ns

*Typical outputs measured with 50 pF load

HP 64797A AC Timing Specifications
Vcc = 5 V, f = 18 MHz

Characteristics	Symbol	H8/3048 Vcc = 5 V, f = 18 MHz		Probe Type 64784E and 64784G		64784C/D		Unit
		min.	max.	Typical*	Worst	Typical*	Worst	
Clock cycle time	tCYC	55.5	1000	–	–	–	–	ns
Clock low pulse width	tCL	17	–	19.4	9.9	20.0	10.3	ns
Clock high pulse width	tCH	17	–	26.8	9.9	26.8	10.3	ns
Clock rise time	tCR	–	10	7.6	17.1	7.0	16.7	ns
Clock fall time	tCF	–	10	7.6	17.1	7.6	16.7	ns
Address delay time	tAD	–	25	19.6	53.2	19.2	51.7	ns
Address hold time	tAH	10	–	36.0	–17.3	36.2	–17.8	ns
Address strobe delay time	tASD	–	25	6.4	30.8	5.6	29.7	ns
Write strobe delay time	tWSD	–	25	10.0	30.8	9.6	29.7	ns
Strobe delay time	tSD	–	25	4.6	30.8	4.8	29.7	ns
Write data strobe pulse width 1	tWSW1	32	–	47.2	25.6	48.0	26.1	ns
Write data strobe pulse width 2	tWSW2	62	–	75.2	55.6	76.0	56.1	ns
Address setup time 1	tAS1	10	–	14.0	–18.8	14.8	–17.9	ns
Address setup time 2	tAS2	38	–	42.8	9.2	43.6	10.1	ns
Read data setup time	tRDS	15	–	23.2	50.7	17.4	48.3	ns
Read data hold time	tRDH	0	–	–22.0	14.2	–16.2	17.8	ns
Write data delay time	tWDD	–	55	39.6	58.7	40.4	59.9	ns
Write data setup time 1	tWDS1	10	–	14.6	–1.8	13.6	–3.6	ns
Write data setup time 2	tWDS2	–10	–	1.2	–29.5	0.4	–31.3	ns
Write data hold time	tWDH	20	–	20.0	5.9	20.4	7.3	ns
Read data access time 1	tACC1	–	50	45.0	–9.9	53.2	–6.4	ns
Read data access time 2	tACC2	–	105	100.5	45.6	108.7	49.1	ns
Read data access time 3	tACC3	–	20	27.2	–15.3	34.2	–12.2	ns
Read data access time 4	tACC4	–	80	82.7	40.2	89.7	43.3	ns
Pre-charge time	tPCH	40	–	56.0	33.6	56.0	34.1	ns
WAIT setup time	tWTS	25	–	25.6	60.9	22.8	54.7	ns
WAIT set hold time	tWTH	5	–	–24.8	–11.0	–22.0	–6.1	ns
BREQ setup time	tBRQS	40	–	–	75.9	–	69.7	ns
BACK delay time 1	tBACD1	–	30	8.8	35.8	8.4	34.7	ns
BACK delay time 2	tBACD2	–	30	–1.2	35.8	–1.0	34.7	ns
Bus floating time	tBZD	–	40	18.4	46.2	19.8	44.7	ns
/RAS delay time 1	tRAD1	–	30	10.8	41.6	5.0	39.0	ns
/RAS delay time 2	tRAD2	–	30	15.6	41.6	9.6	39.0	ns
/RAS delay time 3	tRAD3	–	30	6.0	41.6	4.6	39.0	ns
Row address hold time	tRAH	15	–	26.0	–10.4	31.0	–9.4	ns
/RAS pre-charge time	tRP	40	–	56.0	30.8	56.6	31.7	ns
/CAS to /RAS pre-charge time	tCRP	40	–	54.4	33.6	53.2	34.1	ns
/CAS pulse width	tCAS	35	–	46.8	28.6	47.2	29.1	ns
/RAS access time	tRAC	–	70	62.0	29.4	69.8	34.0	ns
Address access time	tAA	–	45	34.0	–9.9	42.2	–6.4	ns
/CAS access time	tCAC	–	25	12.4	–15.3	19.4	–12.2	ns
Write data setup time 3	tWDS3	10	–	16.4	–1.8	16.0	–3.6	ns
/CAS setup time	tCSR	10	–	23.2	6.6	23.2	6.0	ns
Read strobe delay time	tRSD	–	30	10.0	35.8	10.6	34.7	ns
/RES setup time	tRESS	200	–	–	281.9	–	275.7	ns
/RES pulse width	tRESW	10	–	–	–	–	–	tcyc
/RESO output delay time	tRESD	–	100	–	109.6	–	108.4	ns
/RESO output pulse width	tRESOW	132	–	–	–	–	–	tcyc
NMI setup time	tNMIS	150	–	–	231.9	–	225.7	ns
NMI hold time	tNMIH	10	–	–	–9.0	–	–4.1	ns
Interrupt pulse width	tNMIW	200	–	–	209.2	–	208.3	ns
Crystal oscillator setting time (reset)	tOSC1	20	–	–	–	–	–	ms
Crystal oscillator setting time (software standby)	tOSC2	7	–	–	–	–	–	ms

*Typical outputs measured with 50 pF load

HP 64797A AC Timing Specifications
Vcc = 3 V, f = 13 MHz

Characteristics	Symbol	H8/3048 Vcc = 3 V, f = 13 MHz		Probe Type 64797B and 64784G		Unit
		min.	max.	Typical*	Worst	
Clock cycle time	tCYC	76.9	1000	—	—	ns
Clock low pulse width	tCL	20	—	30.9	20.4	ns
Clock high pulse width	tCH	20	—	36.5	20.4	ns
Clock rise time	tCR	—	15	6.8	17.3	ns
Clock fall time	tCF	—	15	8.6	17.3	ns
Address delay time	tAD	—	50	18.6	53.6	ns
Address hold time	tAH	20	—	37.2	–18.7	ns
Address strobe delay time	tASD	—	50	6.8	31.6	ns
Write strobe delay time	tWSD	—	50	10.4	31.6	ns
Strobe delay time	tSD	—	50	5.2	31.6	ns
Write data strobe pulse width 1	tWSW1	40	—	66.8	45.6	ns
Write data strobe pulse width 2	tWSW2	90	—	105.5	86.3	ns
Address setup time 1	tAS1	15	—	25.5	–9.1	ns
Address setup time 2	tAS2	45	—	65.0	29.6	ns
Read data setup time	tRDS	30	—	34.0	44.8	ns
Read data hold time	tRDH	0	—	–32.8	23.9	ns
Write data delay time	tWDD	—	75	38.4	59.4	ns
Write data setup time 1	tWDS1	20	—	35.6	18.3	ns
Write data setup time 2	tWDS2	–10	—	13.1	–20.1	ns
Write data hold time	tWDH	15	—	30.9	15.5	ns
Read data access time 1	tACC1	—	60	75.4	27.9	ns
Read data access time 2	tACC2	—	140	152.3	104.8	ns
Read data access time 3	tACC3	—	30	46.7	11.4	ns
Read data access time 4	tACC4	—	100	123.6	88.3	ns
Pre-charge time	tPCH	55	—	77.4	53.6	ns
WAIT setup time	tWTS	40	—	31.2	63.1	ns
WAIT set hold time	tWTH	10	—	–30.4	–13.0	ns
BREQ setup time	tBRQS	40	—	—	78.1	ns
BACK delay time 1	tBACD1	—	50	9.2	36.6	ns
BACK delay time 2	tBACD2	—	50	–1.0	36.6	ns
Bus floating time	tBZD	—	70	17.2	46.6	ns
/RAS delay time 1	tRAD1	—	50	8.8	41.6	ns
/RAS delay time 2	tRAD2	—	50	13.2	41.6	ns
/RAS delay time 3	tRAD3	—	50	7.0	41.6	ns
Row address hold time	tRAH	20	—	38.9	–0.3	ns
/RAS pre-charge time	tRP	55	—	75.2	52.2	ns
/CAS to /RAS pre-charge time	tCRP	55	—	73.8	53.6	ns
/CAS pulse width	tCAS	55	—	67.8	48.6	ns
/RAS access time	tRAC	—	80	103.5	78.3	ns
Address access time	tAA	—	45	64.4	27.9	ns
/CAS access time	tCAC	—	30	31.9	11.4	ns
Write data setup time 3	tWDS3	20	—	39.8	18.3	ns
/CAS setup time	tCSR	10	—	43.6	16.5	ns
Read strobe delay time	tRSD	—	50	10.2	36.6	ns
/RES setup time	tRESS	200	—	—	284.1	ns
/RES pulse width	tRESW	10	—	—	—	tcyc
/RESO output delay time	tRESD	—	100	—	110.3	ns
/RESO output pulse width	tRESOW	132	—	—	—	tcyc
NMI setup time	tNMIS	200	—	—	234.1	ns
NMI hold time	tNMIH	10	—	—	–11.0	ns
Interrupt pulse width	tNMIW	200	—	—	209.2	ns
Crystal oscillator setting time(reset)	tOSC1	20	—	—	—	ms
Crystal oscillator setting time (software standby)	tOXC2	7	—	—	—	ms

*Typical outputs measured with 50 pF load

Adapter and Cable Configuration

5-V Operation

Processor	Pin Count	Package Type QFP	TQFP	Configuration of Emul.bd., Adapter & Cable
H8/3001	80	No (.65)	Yes (.5)	64784A + 64784E + 64784J
H8/3002	100	Yes (.5)	Yes (.5)	64784A + 64784D *
H8/3002	100	Yes (.5)	Yes (.5)	64784A + 64784E + 64784G
H8/3003	112	Yes (.65)	none	64784A + 64784C *
H8/3003	112	Yes (.65)	none	64784A + 64784E + 64784F
H8/3004/05	80	Yes (.65)	No (.5)	64784A + 64784E + 64784K
H8/3030/31/32	80	Yes (.65)	No (.5)	64784A + 64784E + 64784H
H8/3040/41/42	100	Yes (.5)	Yes (.5)	64784A + 64784D *
H8/3040/41/42	100	Yes (.5)	Yes (.5)	64784A + 64784E + 64784G
H8/3044/47/48/48F	100	Yes (.5)	Yes (.5)	64797A + 64784D *
H8/3044/47/48/48F	100	Yes (.5)	Yes (.5)	64797A + 64784E + 64784G

Low-Voltage Operation

Processor	Pin Count	Package Type QFP	TQFP	Configuration of Emul.bd., Adapter & Cable
H8/3001	80	No (.65)	Yes (.5)	64784A + 64797B + 64784J
H8/3002	100	Yes (.5)	Yes (.5)	64784A + 64797B + 64784G
H8/3003	112	Yes (.65)	none	64784A + 64797B + 64784F
H8/3004/05	80	Yes (.65)	No (.5)	64784A + 64797B + 64784K
H8/3030/31/32	80	Yes (.65)	No (.5)	64784A + 64797B + 64784H
H8/3040/41/42	100	Yes (.5)	Yes (.5)	64784A + 64797B + 64784G
H8/3044/47/48/48F	100	Yes (.5)	Yes (.5)	64797A + 64797B + 64784G

* : Not a configuration with a flexible probe cable
Yes : Package is supported
No : Package is not supported
( ) : Pin pitch (mm)

HP 64784A Ordering Information

HP 64784A for H8/300x, 303x and 3040/41/42 Processors

Terminal-Based Emulation System

Model	Description
64784A	16-MHz emulator card for H8/3001/02/03/04/05, 3030/31/32, and 3040/41/42 processors
64784x*	Adapters and flexible probe cables
64794A	8 K-deep emulation bus analyzer card, 80 channels
64727A	512 KB emulation memory card
64700B	Card cage

* See Adapter and Cable Configuration

Emulation System Options

Model	Description
64784C	H8/3003 QFP adapter
64784D	H8/3002 and 3040/41/42/44/47/48/48F QFP adapter
64784E	H8/300H Series PGA adapter
64784F	H8/3003 flexible probe cable
64784G	H8/3002 and 3040/41/42/44/47/48/48F flexible probe cable
64784H	H8/3030/31/32 flexible probe cable
64784J	H8/3001 flexible probe cable
64784K	H8/3004/05 flexible probe cable
64797B	Low-voltage adapter
64729A	2 MB emulation memory card
64704A	1 K-deep 80-channel emulation bus analyzer card
64703A	1 K-deep 64-channel emulation bus analyzer card with 16 channels of external state/timing
64794C	64 K-deep emulation bus analyzer card, 80 channels
64794D	256 K-deep emulation bus analyzer card, 80 channels
64023A	CMB cable (4 m; includes three 9-pin connectors)

Software Options

For each software model number ordered, purchase one media option and at least one license option for each concurrent user:

Model	Description
B3074B	Graphical user interface

Media/License Options

opt AAH	HP9000 Series 300/400 manuals/media (DDS DAT tape)
opt UBX	HP9000 Series 300/400 single-user license
opt AAY	HP9000 Series 700 manuals/media (DDS DAT tape)
opt UBY	HP9000 Series 700 single-user license
opt AAV	Sun SPARCstations manuals/media (1/4-inch cartridge tape)
opt UBV	Sun SPARCstations single-user license

Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

HP 64797A Ordering Information

HP 64797A for H8/3044, 3047, 3048 and 3048F Processors

Terminal-Based Emulation System

Model	Description
64797A	18-MHz emulator card for H8/3044, 3047, 3048, and 3048F processors
64784x*	Adapters and flexible probe cables
64794A	8 K-deep emulation bus analyzer card, 80 channels
64727A	512-KB emulation memory card
64700B	Card cage

* See Adapter and Cable Configuration

Emulation System Options

Model	Description
64784D	H8/3002 and 3040/41/42/44/47/48/48F QFP adapter
64784E	H8/300H Series PGA adapter
64784G	H8/3002 and 3040/41/42/44/47/48/48F flexible probe cable
64797B	Low-voltage adapter
64729A	2 MB emulation memory card
64704A	1 K-deep 80-channel emulation bus analyzer card
64703A	1 K-deep 64-channel emulation bus analyzer card with 16 channels of external state/timing
64794C	64 K-deep emulation bus analyzer card, 80 channels
64794D	256 K-deep emulation bus analyzer card, 80 channels
64023A	CMB cable (4 m; includes three 9-pin connectors)

Software Options

For each software model number ordered, purchase one media option and at least one license option for each concurrent user:

Model	Description
B3077B	Graphical user interface

Media/License Options

opt AAH	HP9000 Series 300/400 manuals/media (DDS DAT tape)
opt UBX	HP9000 Series 300/400 single-user license
opt AAY	HP9000 Series 700 manuals/media (DDS DAT tape)
opt UBY	HP9000 Series 700 single-user license
opt AAV	Sun SPARCstations manuals/media (1/4-inch cartridge tape)
opt UBV	Sun SPARCstations single-user license

Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

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