HEWLETT® PACKARD

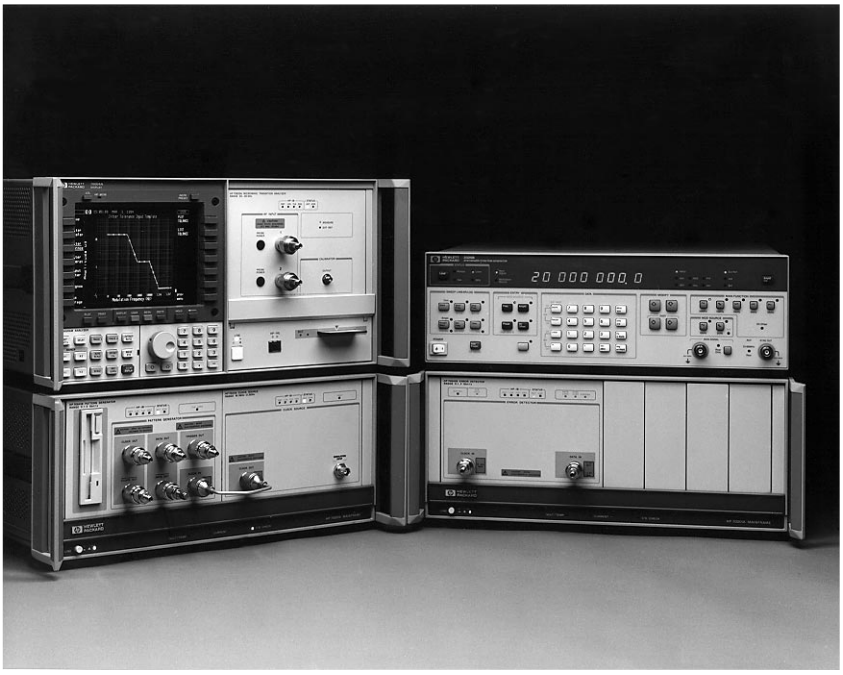
HP 71501C
Jitter Analysis System

Product Overview

A flexible, wide bandwidth jitter analysis system

- Jitter characterization at any rate from below 50 Mb/s through 12 Gb/s
- Measure jitter transfer, jitter tolerance, and jitter generation/output
- Built-in standard test templates for SDH/SONET compliance test, or customize your own test templates
- Diagnostic testing to view demodulated jitter spectrum and waveform or clock spectrum and waveform

High-speed digital transmission systems are often required to receive or regenerate data using a clock signal that is recovered or extracted from the data waveform. Variation in the data rate, commonly known as jitter can complicate the clock recovery and data regeneration process. To guarantee a high level of performance in the presence of jitter, components and systems are typically required to adhere to a rigorous set of jitter performance standards.



The HP 71501C Jitter Analysis System is designed to help you do a thorough jitter characterization of your devices from the chip/component level through complete transmission systems. Coupled with either an HP 71603B or HP 71612A Error Performance Analyzer[1], SDH/SONET standard tests for jitter transfer, jitter tolerance, and jitter generation/output can be performed at STM-1/OC-3 (155 Mb/s), STM-4/OC-12 (622 Mb/s), STM-16/OC-48 (2488 Mb/s), and STM-64/OC-192 (9953 Mb/s) rates. Because the system is completely frequency agile, these tests can also be performed at *any* rate from below 50 Mb/s to above 12 Gb/s such as the Fibre Channel 1063 Mb/s rate.

The HP 71501C Jitter Analysis System is designed to give basic parametric information without requiring functional performance such as data headers, framing, or alarms. This makes it an attractive solution for semiconductor/component manufacturers as well as more complex modules and systems.

[1] The HP 71501C Jitter Analysis System must communicate directly to the error performance analyzer over the HP Modular Measurement System "MMS" interface. Thus only the HP 71603B and HP 71612A Error Performance Analyzers can be used in the system.

Jitter transfer

Jitter transfer is typically used to describe how a clock recovery module or repeater locks and tracks data as the data has jitter placed upon it. In simple terms, it is the ratio of the jitter on the output of the device or system compared to the jitter on the data going into the device. Jitter transfer is typically measured as a function of jitter frequency.

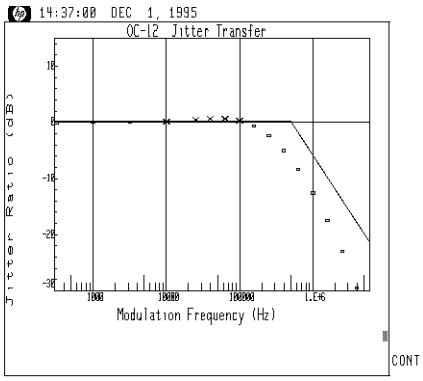


Figure 1. Jitter transfer measurement of a device operating at 622 Mb/s

Figure 1 shows a jitter transfer measurement of a device operating at 622 Mb/s (STM-4/OC-12). Because the measurement is a ratio, the results are unitless, and expressed in decibels. In this measurement, the jitter modulation, at a specific modulation rate or frequency, is impressed upon the data. (The magnitude of the jitter is typically set at levels specified for a jitter tolerance test, discussed later). The jitter at the input to the device-under-test (DUT), as well as the jitter at the output of the DUT are measured simultaneously. The jitter transfer at this jitter rate is then computed. The jitter frequency is incremented and the measurement repeated. This process continues until the device has been characterized over the full bandwidth of interest.

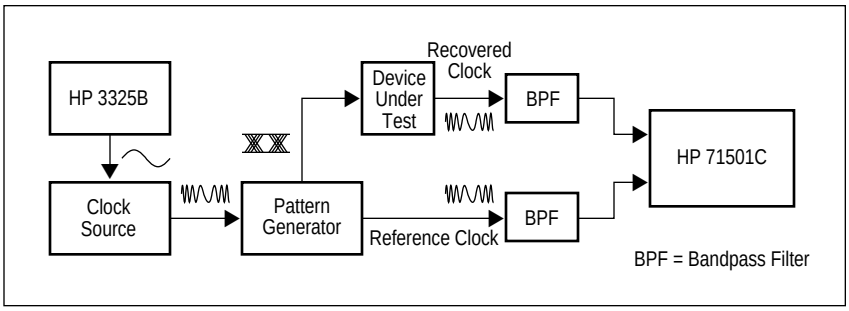


Figure 2. Block diagram for jitter transfer measurements

The test system block diagram for a jitter transfer measurement is shown in Figure 2. The HP 3325B is used as a source of jitter modulation from as low as 10 Hz to as high as 20 MHz. The HP 3325B signal is routed to the phase/frequency modulation input of the system clock source. The HP 3325B output is automatically set to generate the desired jitter level and frequency. The clock source is routed to the HP 71603B or 71612A pattern generator, thus producing data with the desired jitter. This data signal is then fed to the DUT. The recovered clock signal is routed to Channel 1 of the HP 71501C. The clock signal from the pattern generator is used as a reference signal and is routed to Channel 2 of the HP 71501C. Jitter transfer measurement accuracy is enhanced if signal harmonic content is suppressed. Thus low pass or bandpass filters are typically used in the measurement paths.

The results of the jitter transfer measurement can be displayed in one of three ways. Figure 1 shows the jitter transfer function in the "transfer plot" mode. In this mode, the jitter transfer function is displayed on a 10 dB/division scale, usually against the SDH/SONET specification line.

A second method for displaying the jitter transfer performance is with the "delta plot". In this mode the results are displayed as the difference between actual performance and specified performance. For example, if the maximum allowable value of the jitter transfer is 0.1 dB, and the actual performance is 0 dB, the delta plot will show this as being a value of –0.1 dB, as it is 0.1 dB below or within specification. A delta plot is shown in Figure 3.

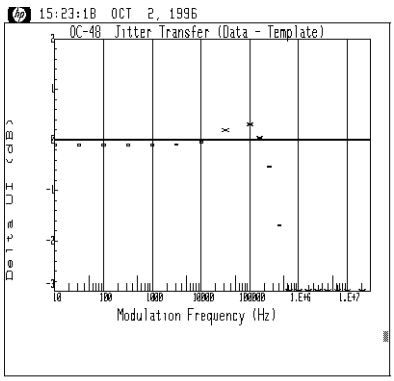


Figure 3. Delta plot jitter transfer test results

Note also that in the delta plot, the vertical scale is 2 dB/division, presenting a much higher resolution display than the transfer plot.

A third technique for displaying the jitter transfer function is a numerical listing. Figure 4 shows a listing of the jitter transfer measurement results. The measured response, the maximum allowed response, the difference between actual and specified performance, and a pass/fail status are all listed.

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JITTER TRANSFER RESULTS

Pt#	Freq	Meas(dB)	Max(dB)	Delta(dB)	Status
1.	10.00 Hz	.006	.100	-.094	PASS
2.	31.60 Hz	-.001	.100	-.101	PASS
3.	100.00 Hz	.003	.100	-.097	PASS
4.	316.00 Hz	.004	.100	-.096	PASS
5.	1.00 kHz	.002	.100	-.098	PASS
6.	3.16 kHz	.010	.100	-.090	PASS
7.	10.00 kHz	.060	.100	-.040	PASS
8.	31.60 kHz	.290	.100	.190	FAIL
9.	100.00 kHz	.410	.100	.310	FAIL
10.	158.00 kHz	.140	.100	.040	FAIL
11.	251.00 kHz	-.429	.100	-.529	PASS
12.	398.00 kHz	-1.590	.100	-1.690	PASS
13.	631.00 kHz	-5.375	.100	-5.475	PASS
14.	1.00 MHz	-14.178	.100	-14.278	PASS

Figure 4. Jitter transfer tabular test results

For margin testing, or to create a custom specification, the magnitude and the location of the corner frequency of the specification limit can be set by the user.

To accurately characterize the jitter transfer function, it may be necessary to perform an analysis over a frequency range that is narrower than that provided by the default test setup. This is achieved by generating a custom template to define the test over the region of interest. For example, if the jitter transfer function exhibits some peaking, the test can easily be altered to zoom in on the region of peaking, as is shown in Figure 5.

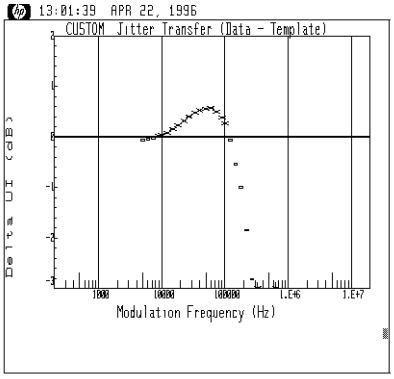


Figure 5. "Zoomed in" transfer results

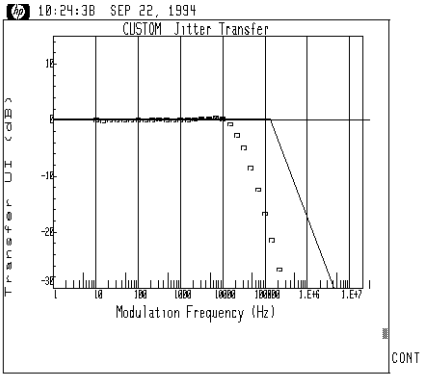


Figure 6. Jitter transfer measurement of a multiplexer

Multiplexers and demultiplexers: Jitter analysis for devices where the output rate is different than the input rate

A unique feature of the HP 71501C jitter analysis system is the ability to measure jitter transfer through a device where the input and output rates are not the same. Typical examples include devices where several data channels are multiplexed together. A higher rate clock signal may be derived from the lower data rate input. Or, characterization of jitter transfer from a low frequency reference clock (such as 19.44 MHz) to a standard rate output (such as 622.08 Mb/s) may be required[2]. The input and output rates do not need to be harmonically related because of the frequency agility of the HP 71501C jitter analysis system.

Figure 6 shows a jitter transfer measurement of a 155.52 Mb/s to 4.977 Gb/s multiplexer. Note that the measurement is automatically scaled such that 0 dB represents no jitter "gain" or "loss" through the multiplexing process.

The architecture of the HP 71501C jitter analysis system is sampler based, which is the key to a frequency agile system. The tradeoff is that the jitter transfer measurements are performed by analyzing the recovered clock signal, as the test system is not capable of measuring jitter on a true data signal. There are devices where clock recovery and data regeneration take place, yet no external clock signal is produced. Unfortunately, the HP 71501C jitter analysis system requires a clock signal from the DUT for jitter transfer measurements. In these cases, the pattern from the HP 71603B or 71612A is set to produce data with a high clock content, such as a 10101010 pattern. This will provide a valid jitter transfer measurement when the transfer response of the DUT is dominated by the loop bandwidth of the phase-locked loop in the clock recovery system and PLL bandwidth is not dependent upon data patterns. Also, because the apparent clock rate from a 10101010 pattern is one-half of a true clock signal, the measurement is made in the multiplex mode.

[2] When using signals below 100 MHz, the quality of the clock outputs of the pattern generator may be degraded. The signal from the clock source may need to be used as the reference as opposed to the clock output of the pattern generator.

Note that the intent of the jitter transfer measurement is not to see how much jitter a component or device adds to a data signal. This is better measured using the jitter generation/output measurement which is discussed later. Instead, jitter transfer is intended to show the performance of clock recovery as a function of jitter frequency.

Jitter transfer measurement uncertainties

An important feature of the HP 71501C jitter analysis system measurement technique is that it is a two channel "simultaneous" measurement technique. Thus system drift is common to both channels and is not a significant factor in the measurement. Jitter transfer measurement uncertainty is then a function of the inherent ability of the HP 71501C jitter analysis system to measure jitter. The uncertainty of a jitter transfer measurement is ±0.05 dB. This assumes that both measurement channels are filtered to reject harmonic signal content[3].

Jitter tolerance

Jitter tolerance is used to describe the ability of a device or system to maintain communication quality in the presence of jitter. The test can be viewed in two ways. A standards based compliance test would require the equipment to maintain a specific bit-error-ratio (BER) level at predefined jitter levels and jitter frequencies. Another form of testing would determine the actual jitter levels where the DUT can no longer maintain a desired BER. Both test methods are available with the HP 71501C jitter analysis system.

Similar to a jitter transfer test, a jitter tolerance test is performed at several jitter frequencies. The jitter magnitudes are normally defined by the standard against which the test is being performed. For SONET-based tests, the jitter magnitude is 15 unit intervals (UI, one bit period of jitter) for low jitter rates, 1.5 UI for medium jitter rates, and 0.15 UI for high jitter rates. For SDH-based tests, the jitter level is 1.5 UI at low and mid jitter rates, and 0.15 UI at high jitter rates. Both SDH and SONET test templates are built into the system. If jitter levels and frequencies other than those defined by the standard based tests are desired, a straightforward procedure is available to develop custom templates. For example, proposed jitter tolerance tests for Fibre Channel 1062.5 Mb/s systems can be performed using the HP 71501C.

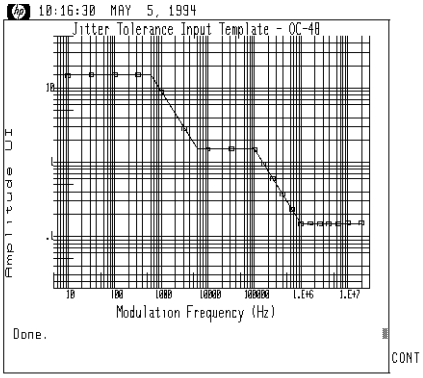


Figure 7. Jitter tolerance compliance test

Figure 7 shows the results of a SONET OC-48 jitter tolerance test displaying the test points with their associated jitter magnitudes and frequencies in a graphical display (A tabular display is also available). (Jitter transfer tests are also performed with these jitter levels and frequencies applied to the data). The measurement process is as follows: A BER measurement of the DUT is performed with jitter-free data. The signal power is attenuated until the onset of errors or a specific BER is achieved. The attenuation is then reduced 1 dB. The jitter modulation source, the HP 3325B, is routed to the FM port of the clock source. The HP 3325B is also controlled by the HP 71501C to yield the required jitter frequency and magnitude on the clock signal, which in turn will translate this jitter to the pattern generator data output. This data is then sent to the DUT. The recovered clock and data from the DUT is then routed to the HP 71603B or 71612A error detector where a BER measurement is performed. (Pattern lengths, data levels, gating times and so forth are set by the HP 71603B or 71612A).

[3] Typically, filtering is achieved using the bandpass filters supplied as part of the system for jitter generation measurements.

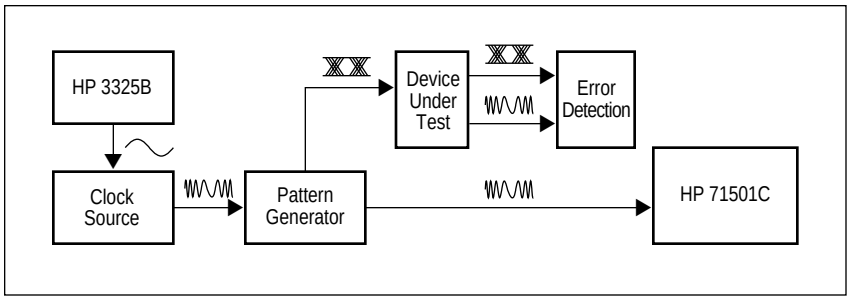


Figure 8. System block diagram for jitter tolerance measurements

The results of the BER test are monitored by the HP 71501C. The HP 71501C compares the actual BER performance to the desired level (defined by the user) to determine the pass or fail status. If the desired BER limit is maintained, a green box ☐ is placed at that test point on the results plot. If the BER limit is exceeded, a red X is placed on the results plot. This process is repeated for each test point as defined by the test template.

The above method is used to verify compliance to a given test standard. If the DUT passes the test, it is still unknown just what level of tolerance is achievable. A simple margin test can be performed by selecting a percentage margin by which to increase the jitter magnitude at each test point. Figure 9 shows a test performed at 50% above the compliance level.

Another available technique is to perform a tolerance search. In this mode the HP 71501C will initially perform the BER test with the jitter level set to that of the template. The jitter will then be systematically increased by a user-defined factor and a BER test performed until the desired BER limit is exceeded, or the test system generation capability is exceeded. If the DUT is not capable of achieving basic compliance levels, the search factor can be set to a negative level. In this mode, the jitter level will be decreased until a level is reached where the DUT can maintain the desired BER. Figure 10 shows the results of a tolerance search test.

For single point testing, the jitter frequency and magnitude can be arbitrarily selected and a BER test performed.

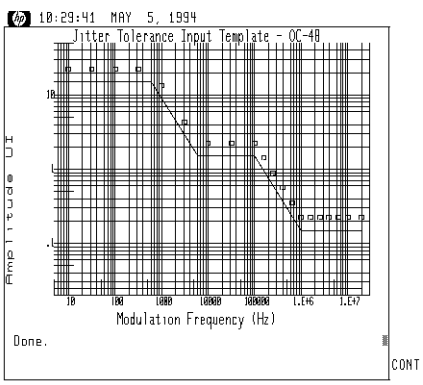


Figure 9. Jitter tolerance test with a 50% margin

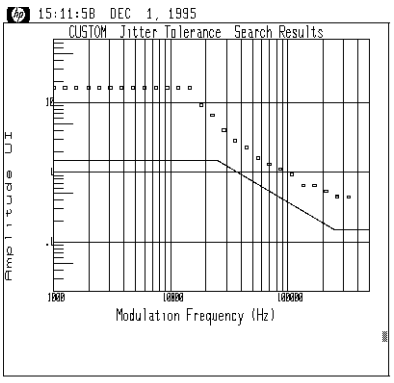


Figure 10. Jitter tolerance search results

All of the above jitter tolerance tests may also be performed on multiplexing and de-multiplexing devices. The HP 71501C jitter analysis system simply sets the desired jitter levels at the input side of the DUT, and the appropriate BER test is performed at the output rate by the HP 71603B or 71612A.

Jitter tolerance measurements on devices with no clock output signal

If the DUT has no recovered clock output, the source of the clock signal for the HP 71603B or 71612A BERT would be the same as what would be used for a conventional BER test (as if no jitter were applied to the data). For example, the clock output of the pattern generator might be used as an input to the error detector.

Jitter tolerance measurement uncertainties and accuracies

The key measurement in a jitter tolerance test is BER. The uncertainty of a BER measurement is dictated by the HP 71603B or 71612A and how they are configured. Accuracy of the HP 71501C jitter analysis system involves precision in setting a specific jitter level. The HP 71501C will typically set jitter to within ±2% of the desired level.

Jitter generation and output jitter

Jitter generation and output jitter are measurements which determine the amount of jitter a component or system adds to an input data signal. In this measurement the HP 3325B jitter modulation source is disabled, thus no jitter modulation is applied to the data. The jitter-free data from the HP 71603B or 71612A is routed to the DUT, and the DUT output clock signal is received and measured by the HP 71501C.

Because this is essentially a noise measurement, it is defined over a specific bandwidth. For example, a jitter generation measurement at the STM-4/OC-12 rate of 622 Mb/s examines only the demodulated jitter spectrum from 12 KHz to 5 MHz. The band limiting process is achieved in two stages. First, the signal is sent through a hardware bandpass filter centered at the data rate frequency. The bandwidth of the filter is dependent upon the data rate and in the 622 Mb/s case is ±5 MHz centered at 622.08 MHz. Filter bandwidth and center frequency are unique to each data rate. By passing the signal through the hardware filter, the high end of the jitter spectrum is determined. The signal is then demodulated to extract the jitter modulation. The baseband jitter is passed through a software filter to reject the low frequency spectrum. In the case of the 622.08 Mb/s jitter generation measurement the filter cutoff is 12 kHz. Several "traces" of the intrinsic jitter are recorded. The peak-to-peak extremes of the signal are monitored to yield the required measurement of peak-to-peak jitter. The RMS jitter is also determined. Figure 11 and 12 show the measurement configuration and a measurement of jitter generation on a 622 Mb/s regenerator.

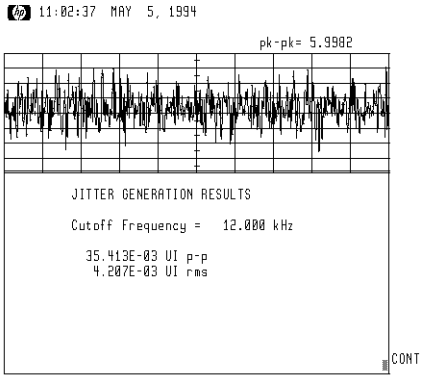


Figure 12. Jitter generation measurement of a 622 Mb/s regenerator

These measurements can only be made on clock signals and not on data signals. If only a data signal is available from the DUT, it would first need to pass through a clock recovery scheme which would not add a significant amount of jitter while extracting a clock signal. This clock recovery scheme would also need to have a jitter transfer function that was flat over the spectrum of interest so as not to degrade the measurement results.

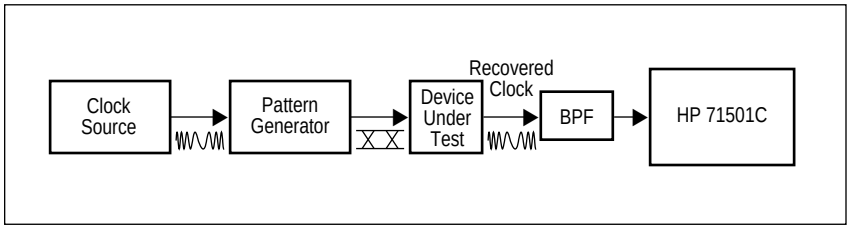


Figure 11. Measurement configuration for jitter generation

Output jitter

Output jitter measurements are almost identical to jitter generation measurements. The only difference from a measurement perspective is that the frequency position of the software highpass filter is set for two values. In the case of the 622 Mb/s signal, instead of a 12 kHz cutoff, measurements are made with both a 1 kHz and a 250 kHz cutoff. The hardware filter is identical to that used in the jitter generation measurement, yielding an approximate 5 MHz jitter spectrum. Figure 13 shows an output jitter measurement made at a 9953 Mb/s (STM-64/OC-192) rate.[4]

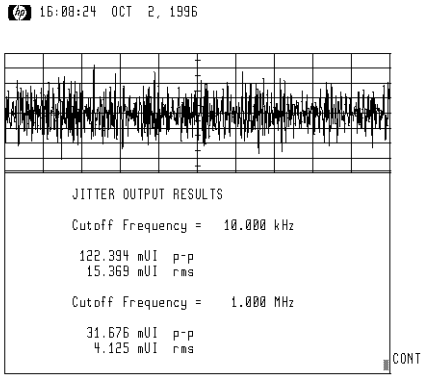


Figure 13. 9953 Mb/s output jitter measurement

Hardware filters for 155, 622, 2488, and 9953 Mb/s are supplied as standard equipment with the HP 71501C system. If measurements are to be made at other rates, a filter design template is included in the system documentation to facilitate custom rate filter designs.

[4] Specifications for 9953 Mb/s rates are subject to revision by the SONET/SDH standards committees.

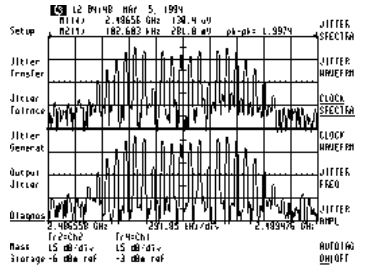
Jitter generation and output jitter measurement accuracy

The factors which dominate intrinsic jitter measurement accuracy are the jitter of the test system itself and its ability to accurately characterize jitter "noise" signals. Test system jitter is dictated to a large extent by the clock source used to time the pattern generator. This then sets a minimum or baseline level of jitter that can be measured. The uncertainty in making intrinsic jitter measurements, not accounting for the baseline jitter is ±10% of the measured value. Thus measurement uncertainty is ±10% + baseline. Table 1 (page 9) shows the baseline limitations for various system configurations.

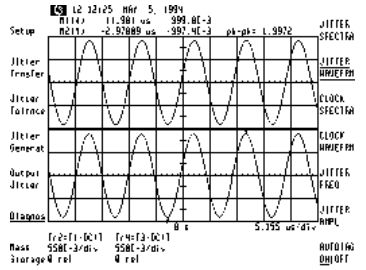
Diagnostic capabilities of HP 71501C system

For diagnostic purposes, the HP 71501C has the ability to display the demodulated or "baseband" jitter spectrum and waveform of a phase modulated clock signal. Also, similar to using a high-frequency spectrum analyzer and high-speed oscilloscope, the clock spectrum and waveform can be displayed. Examples are shown in Figure 14.

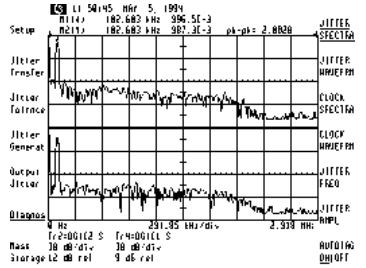
For troubleshooting purposes, the system can provide data signals with arbitrary jitter magnitudes and frequencies. For example, if a data stream with 2 UI of jitter at 15 KHz is desired, simply enter in these values and the system will automatically produce the desired signal.



Clock spectrum



Demodulated jitter waveforms



Demodulated jitter spectrum

Figure 14. Diagnostic measurement capabilities

Configuring a system

There are a variety of configurations allowable with the HP 71501C Jitter Analysis System. Selection of the correct configuration is dependent upon the range of data rates over which testing is to occur. The fundamental components of a complete system include:

1. **HP 71501C jitter receiver/ system controller.** This is made up of the HP 70004A[5] Display Mainframe and the HP 70820A Microwave Transition Analyzer.
2. **HP 3325A/B synthesizer/ function generator** which acts as the jitter modulation source[6].
3. **Frequency/phase modulatable clock source:** HP 83752A, HP 70311A option H08, HP 70340A, or HP 83732A/B
4. **Data pattern generator:** HP 71603B error performance analyzer (specific component of this modular system is the HP 70841B pattern generator) or the HP 71612A error performance analyzer (specific component is the HP 70843A pattern generator)
5. **Error detector** (for jitter tolerance test): HP 71603B error performance analyzer (specific component of this modular system is the HP 70842B error detector) or the HP 71612A error performance analyzer (specific component is the HP 70843 error detector)

The HP 71501C and 3325A/B must be included in the system. Choosing a pattern generator and error detector is dictated by the highest data rate at which testing is to occur. The HP 71603B system normally operates from 100 Mb/s to either 1500 Mb/s or 3000 Mb/s (special options exist to allow operation down to 50 Mb/s). The HP 71612A system operates from 100 Mb/s to 12000 Mb/s. Choosing a clock source is based on the following criteria:

1. Range of data rates to be tested
2. Jitter modulation bandwidth requirements
3. Jitter magnitude requirements

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[5] The HP 71501C/71603B or HP 71501C/71612A system can operate with one or two HP 70004A display mainframes.

[6] The system is not compatible with HP 3325B option 002 High Voltage Output.

HP 83752A clock source

(included as a standard part of the HP 71501C jitter analysis system, a delete option is available)

This clock source can operate from 10 Mb/s to 20 Gb/s. It is a general-purpose signal generator with frequency/phase modulation characteristics that are essentially independent of the selected clock frequency. That is, the modulation capabilities at 155 Mb/s are similar to the capabilities at 10 Gb/s. The jitter magnitude versus jitter frequency response is shown in Figure 15. Modulation range is about 250 Hz to 9 MHz. SDH/SONET jitter transfer measurements require operation beyond 2 MHz at 2488 Mb/s and beyond 1 MHz for jitter tolerance. Standards are still being defined for 9953 Mb/s rates, but jitter tolerance is likely to require testing to 4 MHz. Lower data rates require proportionally lower jitter modulation bandwidths. Thus the HP 83752 provides very good jitter capabilities over a broad range of data rates[7].

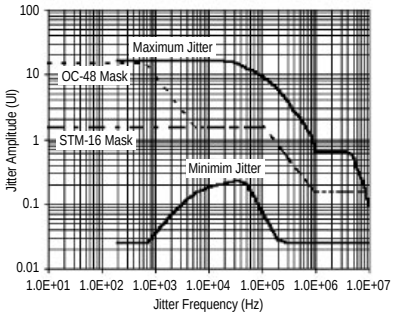
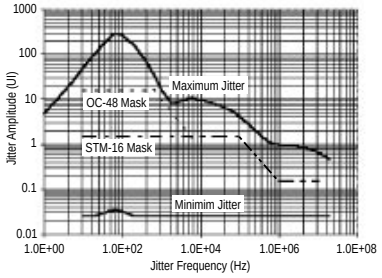


Figure 15. Modulation capabilities of the HP 83752A clock source

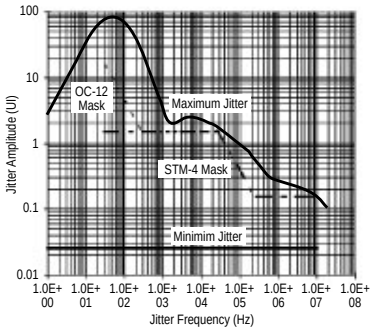
The HP 83752A clock source does not operate as part of the Hewlett-Packard Modular Measurement System. When operating either the HP 71603B or 71612A as a standalone BERT independent of the HP 71501C jitter analysis system, setting the clock frequency for the pattern generator is achieved directly at the 83752A either manually or over HP-IB. (The HP 83752A is controlled automatically by the 71501C when performing jitter analysis). Minimum jitter refers to the smallest jitter level that can be precisely set by the system.

HP 70311 option H08 clock source

The standard clock source for the HP 71603B error performance analyzer is the HP 70311A. Option H08 gives this source phase modulation capability. The HP 70311A H08 will operate at rates from 16 MHz to 3.1 GHz. The phase/frequency modulation range is from 10 Hz to 20 MHz. Different than the HP 83752A, the HP 70311A H08 modulation sensitivity decreases proportionally as data rate decreases. That is, the maximum jitter level achievable at 622 Mb/s is one-fourth the level achievable at 2488 Mb/s. Because of its 20 MHz modulation range, the HP 70311 H08 is the optimum source for STM-16/OC-48 jitter test. Even though the modulation capability is reduced at 622 Mb/s, the system will still be able to do a full jitter compliance test. However, jitter levels at 155 Mb/s are inadequate for jitter tolerance testing. Jitter generation/output capabilities are discussed in Table 1 page 9.



2488 Mb/s



622 Mb/s

Figure 16. HP 70311A H08 modulation capabilities

[7] The 83752A is not capable of producing 15 UI of jitter over the 10 to 30 Hz range as required by the SONET jitter tolerance test for the OC-3 and 12 rates. However, most devices easily tolerate this jitter level at rates into the kHz range and beyond. For these data rates, when the HP 83752A clock source is used, it is recommended that the test template be adjusted to produce 15 UI at jitter rates beyond 250 Hz. This will confirm SONET jitter tolerance at low jitter rates. Jitter generation/output capabilities are discussed in Table 1 page 9.

HP 70340A clock source

The HP 70340A is the standard clock source used with the HP 71612A error performance analyzer. It will operate at data rates from 1 Gb/s to 20 Gb/s. Its jitter modulation range is from 60 Hz to 5 MHz. Because it does not operate below 1 Gb/s, it cannot be used for 155 and 622 Mb/s testing. However, modulation performance exceeds 2488 Mb/s templates and marginally exceeds tentative templates for 9953 Mb/s tolerance testing. Similar to the HP 83752A, modulation performance is independent of data rate. Performance is shown in Figure 17. Jitter generation/output capabilities are discussed in Table 1.

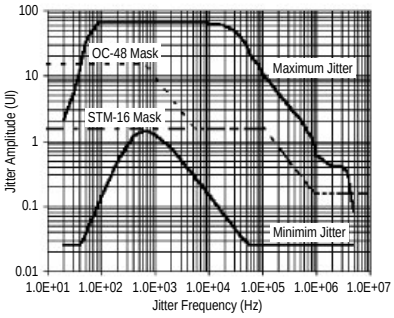


Figure 17. Jitter performance of the HP 70340A

HP 83732B clock source

The HP 83732B clock source will operate from 10 Mb/s to 20 Gb/s. Its jitter modulation range is from 20 Hz to 5 MHz. However, it can produce larger jitter levels at low frequencies in comparison to the HP 83752A.

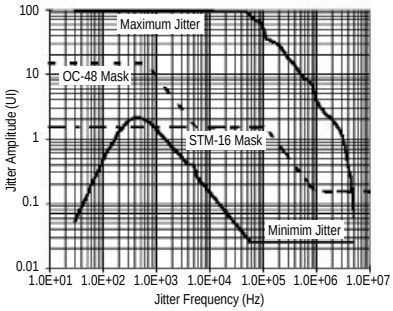


Figure 18. Jitter performance of the HP 83732B

A summary of the various clock sources is found in Table 1 listing performance in terms of standard data rates.

Jitter measurement range of the HP 71501C

Figure 19 shows the ability of the HP 71501C to measure jitter as a function of jitter frequency. This combined with the jitter modulation characteristics of the clock source define the system measurement range.

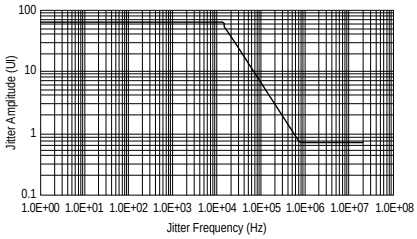


Figure 19. Measurement range of the HP 71501C

Jitter testing at Fibre Channel and other non-SDH/SONET rates

Because the HP 71501C is frequency agile, jitter transfer, tolerance and generation/output testing at Fibre Channel or other rates is performed in the same fashion as SDH/SONET tests. At the time of this writing, Fibre Channel jitter tests are still being defined. Thus some user definition is required for testing. For example, if testing at Fibre Channel 1063 Mb/s, the user would simply set this as the HP 71501C data rate. The jitter levels for transfer and tolerance test could be default values used in a SONET or SDH test, or could be user defined. Once a test template has been defined, it can be easily saved and recalled for any subsequent testing.

Table 1. Clock source characteristics

	Data Rate Range	Modulation Range	Jitter Generation (noise) UI (RMS/pp)			
			OC-3/STM-1 (12 kHz–1.3 MHz)	OC-12/STM-4 (12 kHz–5 MHz)	OC-48/STM-16 (12 kHz–20 MHz)	OC-192/STM-64 (50 kHz–80 MHz)
83752A	10 Mb/s–>12 Gb/s	300 Hz–9 MHz	0.0015/0.012	0.0025/0.022	0.0027/0.02	0.007/0.052
70311A H08	622 Mb/s[8]–3 Gb/s	10 Hz–20 MHz	0.0007/0.006	0.0008/0.007	0.0014/0.009	———
70340A	1000 Mb/s–>12 Gb/s	50 Hz–5 MHz	———	———	0.0013/0.011	0.004/0.04
83732A/B	10 Mb/s–>12 Gb/s	50 Hz–5 MHz	0.0009/0.005	0.0008/0.004	0.0015/0.012	0.0063/0.065

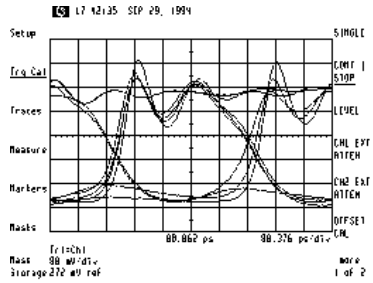
8 Clock rate can be as low as 16 MHz, but jitter modulation capabilities are severely reduced for rates below 622 Mb/s.

Eye-diagram analysis

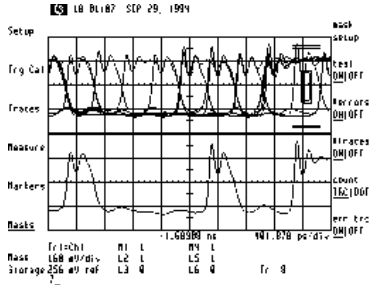
The HP 71501C jitter analysis system can also be configured as a high-speed eye-diagram analyzer using Option 005 eye-diagram analysis software. The HP 71501C eye-diagram analysis software allows the system to operate similar to a high-speed sampling oscilloscope such as the HP 83480A digital communications analyzer[9].

The HP 71501C can perform eye-diagram analysis such as extinction-ratio testing and mask testing. In addition, the software allows the system to operate in HP Eyeline mode. In eyeline mode the eye-diagram display shows continuous traces instead of synchronous dots. This allows pattern dependent effects to be investigated. For example, the trace leading to a mask violation can be captured and displayed. The eyeline eye diagram can take advantage of trace averaging. Thus very small energy signals can be extracted from broadband noise. Finally, eye diagrams can be analyzed using software filters. Fourth-order Bessel-Thomson filters can be easily designed for virtually any data rate allowing analysis without having to actually construct a hardware filter.

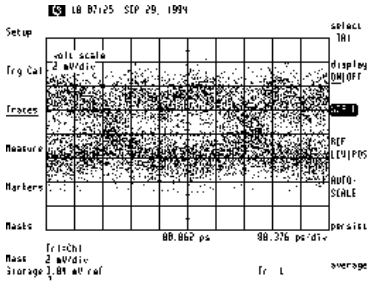
The eye-diagram analysis software is a separate application from the jitter analysis software. The applications cannot be run simultaneously. Switching from eye-diagram analysis to jitter analysis requires reloading of the jitter application program (or vice-versa).



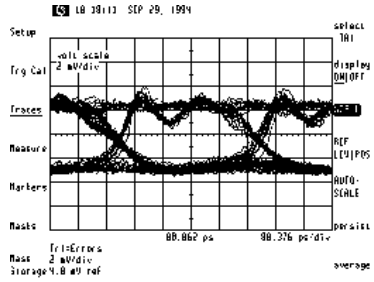
Eye-diagram using eyeline mode



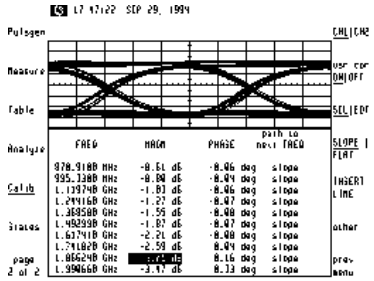
Capturing the trace causing a mask violation



Small power eye-diagram without using eyeline



Small power eye-diagram using eyeline mode



Creating a custom software eye filter

Figure 20. HP Eyeline mode examples

[9] In terms of ease-of-use, measurement speed, accuracy, and configuration flexibility, the HP 83480A digital communications analyzer is a superior measurement tool for eye-diagram analysis in comparison to any other instrument, including the HP 71501C. A general recommendation is that the HP 71501C should not be selected for eye-diagram analysis alone, but as a jitter analysis system with incremental eye-diagram analysis capabilities.

Ordering information

The HP 71501C comes standard with the following equipment to have a complete jitter analysis system when configured with either the HP 71603B or 71612A error performance analyzers:

HP 71501C:

HP 70820A microwave transition analyzer (jitter receiver/system controller)[10]

HP 70004A display mainframe

HP 83752A synthesized signal generator (10 MHz to 20 GHz clock source)

HP 3325B synthesizer/function generator (10 Hz to 20 MHz jitter modulation source). The HP 71501C system is not compatible with option 002 high voltage output.

Cables and adapters
(3 one meter high-frequency cables, 1 MS-IB interface cable, 2 HP-IB cables, cables for 10 MHz reference connections, cable for jitter modulation connections)

Four pairs of hardware bandpass filters
(155.52 MHz, 622.08 MHz, 2488.32 MHz, and 9953.28 MHz)

Jitter analysis system software

[10] The HP 71501C system uses a special version of the 70820A microwave transition analyzer that has expanded memory capacity compared to a standard 70820A module.

For modifications of the standard system, the following options are available:

Option 001: Delete HP 83752A clock source

Option 003: Delete HP 3325B synthesizer/function generator

Option 004: Delete hardware bandpass filters

Option 005: Add eye-diagram analysis software

Option 200: Delete HP 70004A display mainframe (This assumes that the HP 70004A from the HP 71603B or 71612A is used as the system display. System can be used with either one or two display mainframes. The HP 70820A must reside in either a 70004A or 70001A mainframe)

Option 201: Substitute HP 70001A module mainframe for the 70004A display mainframe

The following options are also available:

Option 0B1: Add manual set

Option 0BW: Assembly level service documentation

Option 810: Rackmount slide kit for HP 70004A

Option 908: Rackmount flange kit for HP 70004A

Option 913: Rackmount flange kit for HP 70004A that has handles

Note: The HP 71603B or 71612A error performance analyzers are ordered separately from the 71501C.

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