Agilent Technologies
Innovating the HP Way

TACHYON*
Fibre Channel
Interface Controller

Product Overview

HPFC-5000

Description

TACHYON is a fundamental building block compatible with Agilent Technologies' Fibre Channel solution which includes interface controllers, physical link modules, adapters, switches and disk drives.

The TACHYON architecture supports both networking and mass storage connections to provide a low cost, high performance solution with low host overhead.

Features

- Single chip Fibre Channel interface (no I/O processor required)
- Supports 1062.5, 531, and 266 MBaud links
- Supports 3 topologies; direct connect, fabric, and Fibre Channel Arbitrated Loop (FC-AL)
- Supports Fibre Channel Class 1, 2, and 3 Services
- Supports up to 2-Kbyte frame payload for all classes of service
- Sequence segmentation/ reassembly in hardware

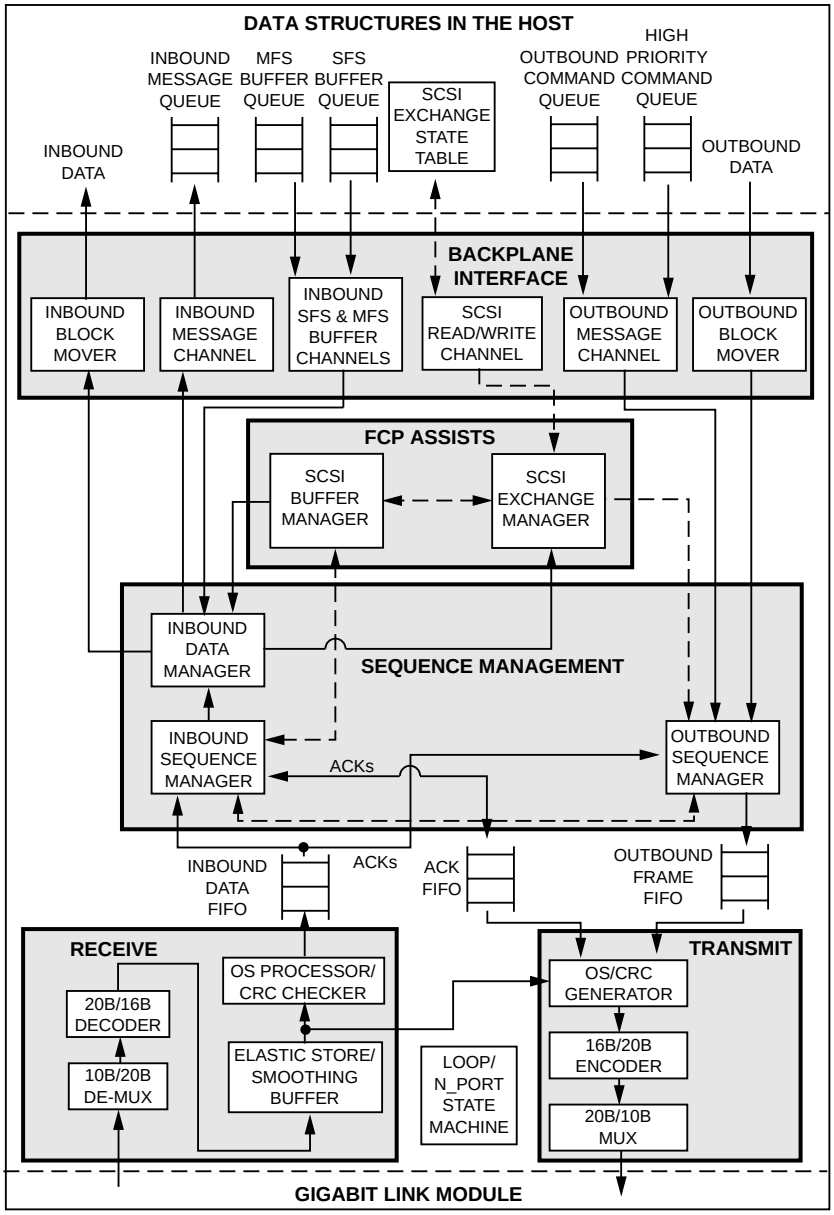

Figure 1. TACHYON Internal Block Diagram

* TACHYON (tak' - ē - än)

1. a subatomic particle that only exists at speeds faster than the speed of light.
2. Agilent's Fibre Channel Interface chip.

Features (continued)

- Automatic ACK frame generation and processing
- On-chip support of FCP for SCSI Initiators and Targets
- Supports up to 16,384 concurrent SCSI I/O transactions
- Compliant with Internet MIB-II network management
- Direct interface to industry standard 10 and 20-bit Gigabit Link Modules (GLM)
- Hardware assists for TCP/UDP/IP networking
- Parity protection on internal data path
- Eight internal DMA channels
- Full duplex internal architecture that allows TACHYON to process inbound and outbound data simultaneously

Specifications

System Clock Frequency:
24-40 MHz backplane operation

Operating Temperature:
0-50°C @ 0 m/s airflow,
0-70°C @ 1.5 m/s airflow

Testability:
Full internal scan path. IEEE Standard 1149.1 Boundary Scan

Packaging:
208-pin metal quad flat pack

Standards:
Intended to be compliant with ANSI standards and FCSI/FCA profile definitions

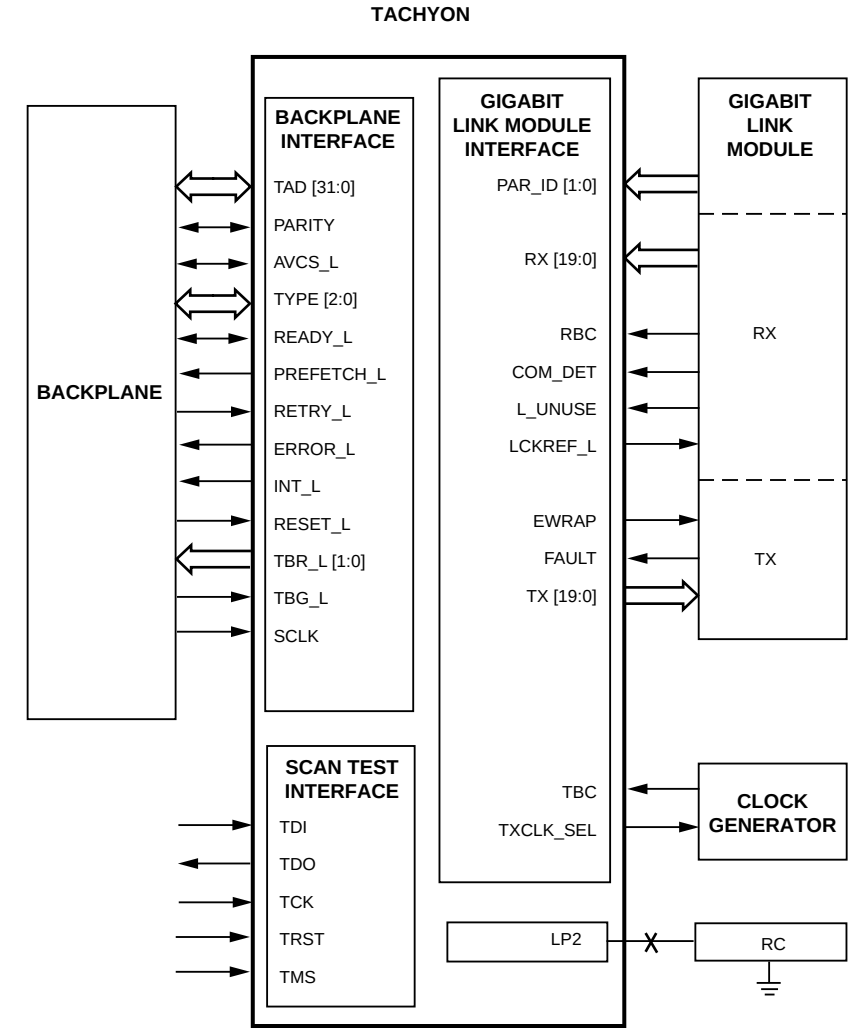

Figure 3. TACHYON Pin-out Block Diagram

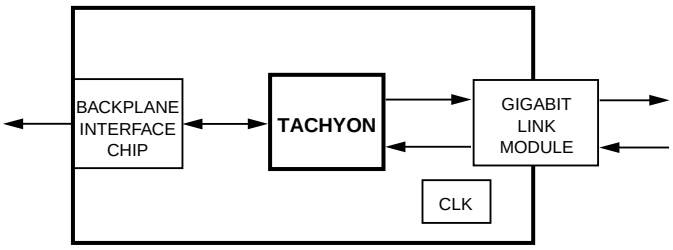

Figure 2. System Adapter Card Block Diagram

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