HP E2484A

Intel i960RP Preprocessor Interface

For use with HP logic analyzers

The HP E2484A preprocessor for the Intel i960RP is a mechanical and electrical interface between the Intel i960RP and various HP logic analyzers for real-time timing and state analysis. The preprocessor routes signals; aligns address, data and status signals; and allows filtering of non-data transfers such as idle and wait states.

Preprocessor software configures the logic analyzer labeling address, data lines and status lines. Additionally, when a state trace is displayed, i960RP mnemonics are listed providing data captured and the controlling program.

Package Supported

352 pin BGA (refer to *Intel i960RP Connector Specification for Using In-Circuit Emulators and Logic Analyzers with the i960RP Processor,* Rev 2.0, for board layout information.)

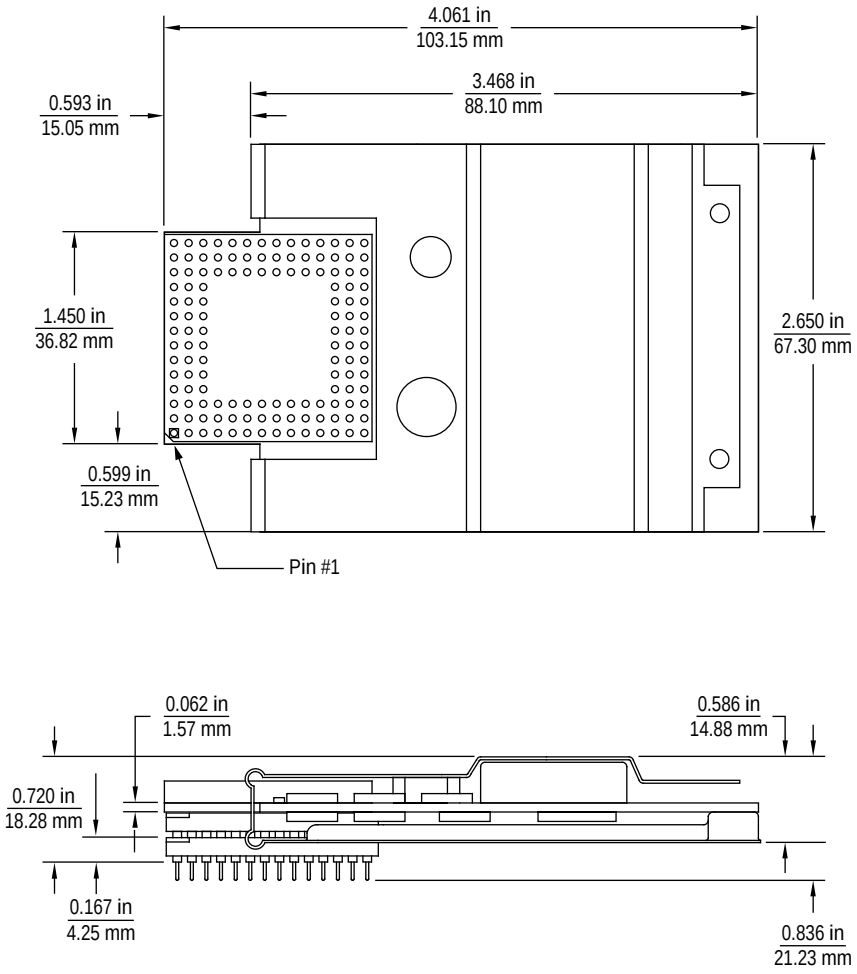

Figure 1. The HP E2484A preprocessor interface dimensions

Capabilities

The HP E2484A preprocessor supports timing, state-per-clock, and state-per-transfer operating modes.

- Timing mode, the HP E2484A buffers i960RP signals and passes them to the logic analyzer.
- State-per-clock mode all valid data transfers on the i960RP bus clock data into the logic analyzer.
- State-per-transfer mode aligns address, status, and data, before clocking the logic analyzer, deskewing the pipelined bus of the i960RP processor.

The HP E2484A filters states so that only valid data transfers (instruction fetches/caches fills, data reads and writes) get clocked into the analyzer in state-per-transfer mode. Wait states, idle states (that is, states when there is no valid data on the bus) do not get passed to the analyzer. This ensures optimal use of the analyzer's acquisition memory. Logic analyzer time tags can be used to measure the duration of the transactions from state to state.

- Address bits A0 and A1 are reconstructed by the HP E2484A hardware improving state analysis triggering and disassembly readability.
- The following i960RP instructions can be selected to be displayed or suppressed:

  - unexecuted prefetches
  - jumps
  - calls/returns, and other instructions.
  - memory read/write cycles.

- Monitors all i960RP processor core signals (excluding PCI buses) of interest including the on-chip interrupt and DMA controllers.

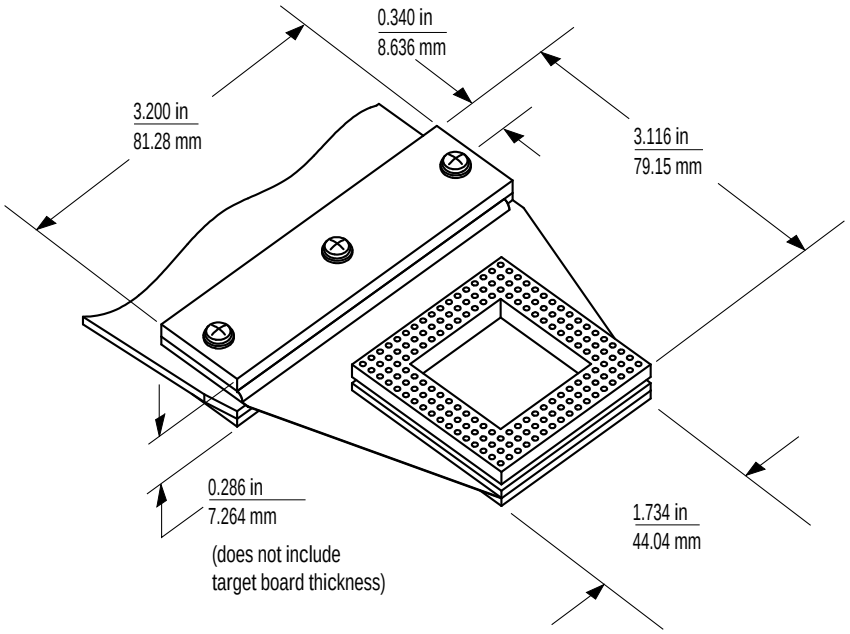

Figure 2. flexible adaptor: conforms to Intel i969RP connector specification for using in-circuit emulators and logic analyzers with the i960RP processor

Logic Analyzers Supported
HP 1660A/AS, C/CS
HP 1661A/AS, C/CS
HP 1670A
HP 1671A
HP 16550A (one or two cards)
HP 16554A/55A/56A (two cards)

Probes Required
- Five 17-channel pods are required for instruction inverse assembly
- Six 17-channel pods are required to monitor all i960RP core signals. Monitoring activity on the i960RP PCI buses requires the use of a separate PCI bus preprocessor(s).

Power and Pod Termination Requirements
All power is supplied by the logic analyzer. Probe/pod termination networks are built in to the preprocessor.

Microprocessor Bus Clock Speed
33 MHz

Timing Analysis Support
1 ns typical channel-to-channel timing skew.

Signal Line Loading
- Approximately 24 pF DEN#, RESET#, and RDYRCV#
- Approximately 16 pF all other signals

Adapter
The HP E2484A preprocessor includes an adapter that is fully compatible with the Intel i960RP *Connector Specification for Using In-Circuit Emulators and Logic Analyzers with the i960RP Processor*, specification Rev 2.0.

Environmental Characteristics

Temperature

Operation	0 to 50 °C +32 to 131 °F	
Altitude	4600m	50,000 feet
Humidity	Up to 75% noncondensing. Avoid sudden, extreme temperature changes that could cause condensation on circuit board.	

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