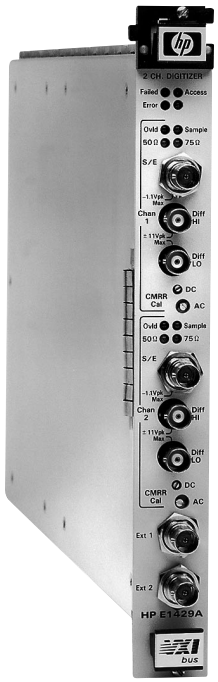
20 MSa/s Digitizer
HP E1429A

Technical Specifications

- **0.05 Sa/s to 20 MSa/s sample rate, 12-bit resolution**
- **2 channels of 512 kSa/channel, segmentable memory**
- **Analysis capability with the HP E1485A DSP**
- **Built-in test**
- **Message-/register-based programming supported**



Description

The HP E1429A digitizer is a **C-size, 1-slot, message-based VXI module.** It makes 12-bit, 20 MSa/s measurements, and contains two analog channels, memory, timebase, and data paths. The HP E1429A is functionally identical to the HP E1429B, except the E1429A does not support local bus.

Ideally suited for transient signals, the HP E1429A's arm/trigger circuits can be programmed to wait for the transient to occur. Up to 128 pre- and post-arm data sets can be stored in its segmentable memory. If power is lost, the HP E1429A keeps the data intact in its non-volatile memory. Both message- and some register-based programming is supported by the HP E1429A.

SCPI commands are used to program at a high level. Register-based reads and writes are supported for high-speed data-only access. An on-board voltage reference is used to verify that the HP E1429A is operational. Attenuators, amplifiers, A/Ds, memory, timebase, and digital circuits are tested upon power-up and upon receipt of the *TST command. The normal path for retreiving data is the VXI data transfer bus.

Refer to the HP Website directory of addresses (URLs) for instrument driver availability and downloading instructions.

Analog

Each channel has its own analog electronics, including signal conditioning and A/D converters. By providing separate paths, the input gains and impedances can be matched to the incoming signals.

A differential and a single-ended input on each channel allow a mix of signal types to be connected. The differential inputs offer a high impedance to minimize circuit loading, while the single-ended inputs can be programmed for 50 or 75 Ω to match source impedances.

Memory

A segmentable, battery-backed memory is dedicated to each channel. Up to 128 segments can be defined to allow multiple pre- and post-arm events to be captured. When using the pre- and post-arm mode, the HP E1429A loops within a segment until it records the programmed number of post-arm readings. The HP E1429A will then move to the next segment and wait for the next arm. The single ported memory (not FIFO) can be read after the measurements have taken place.

A replaceable battery preserves readings in memory when power is lost. The data will still be intact even when the HP E1429A is removed from the mainframe.

Time Base and Triggering

Both channels sample at the same time. The sample rate can be driven by internal or external timebase references. These references can be divided to provide variable sample rates up to 20 MSa/s in 1-2-5 steps. Dual sample rates can be used in the pre- and post-arm mode, wherein the sample rate changes upon receipt of an arm event.

Arm and trigger signals can be generated internally or received from a variety of sources on the VXI backplane and the faceplate BNCs. In addition, the arm and trigger signals can be sourced by the HP E1429A to synchronize multiple instruments.

Data Paths

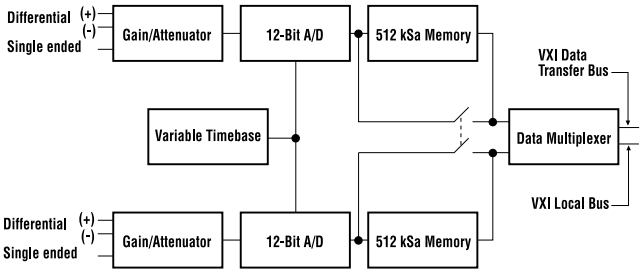
The normal path for retrieving data is the VXI data transfer bus.

Programming

Both message- and some register-based programming is supported by the HP E1429A. SCPI commands are used to program at a high level. Register-based reads and writes are supported for high-speed data-only access.

Built-in Self-Test

An extensive self-test uses an on-board voltage reference to verify that the HP E1429A is operational. Attenuators, amplifiers, A/Ds, memory, time-base, and digital circuits are tested upon power-up and upon receipt of the *TST command. By running the self-test, you gain a high degree of confidence that the HP E1429A is operational.



HP E1429A Block Diagram

Specifications

In accordance with IEEE Std 1057 Trial-Use Standard for Digitizing Waveform Recorders. This document available from IEEE.

General

Number of channels:	2
Built-in DSP:	No
Alias protection:	Oversample
Basic accuracy:	0.5%
Low-Frequency CMRR:	68 dB
Variable bandwidth:	External Filters
2 dB Input range headroom:	No
Dual-Ported memory:	No
Dual-Rate sampling:	Yes

Sampling

Resolution:	12 bits including sign
Effective bits:	10 bits at 100 kHz; 9.5 bits at 10 MHz *(typical on 1 V range, 50 Ω input, full scale input)*
Sample rates:	0.05 to 20 MSa/s
Sample sequence:	1-2-5
Dual sample rate:	switches between programmed rates upon receipt of arm

Memory

Memory:	512 kSa/s channel, battery-backed
Segmented memory:	yes

Input

Input impedance:	50 or 75Ω single-ended and 1 MΩ||20 pF differential *(both inputs on each channel, DC coupled, nominal)*
Signal ranges:	50/75 Ω: 0.1 V to 1 V; 1 MΩ: 0.1 V to 100 V in 1-2-5 steps
Bandwidth:	50 MHz @ 1 V single-ended, 5 MHz @ 10 V differential, typical
Filtering:	10 MHz nominal, 2-pole Bessel, switchable
Signal to noise ratio:	−62 dB typical

Timebase

Internal reference:	20 MHz, ±50 ppm, <25 ps rms jitter typical
Reference sources:	internal crystal, faceplate BNC, CLK 10, and ECLTRG
Timebase resolution:	50 ns

Arm and Trigger

Each trigger event causes one A/D conversion in both channels; each Arm event allows acquisition of a burst of one or more dual-channel A/D conversions.

Programmable arm delay:	50 ns to 32 ms using internal 20MHz reference *(derived from reference)*
Pre-arm capture:	yes
Readings per arm:	1, 7 to 16,777,215, or continuous post-arm; 0 or 3 to 65,535 pre-arm
Re-arm rate:	up to 2 MHz *(non-segmented memory)*
Arm sources:	internal, faceplate BNC, input voltage level, TTLTRG, ECLTRG, and logical OR of any two signals
Trigger:	on event
Trigger (sample clock) sources:	internal, VME read, faceplate BNC, TTLTRG, and ECLTRG
ECLTRG functions:	arm, trigger, and reference *(input and output)*
TTLTRG functions:	trigger and arm *(input)*arm and ready for trigger *(output)*

Connectors

EXT1 faceplate BNC:	arm and trigger (input) arm, trigger and reference (output)
EXT2 faceplate BNC:	trigger and reference *(input)*

Backplane Connector Shielding

To ensure compliance with RFI levels specified in standards EN55001 and CISPR11, this product requires the Backplane Connector Shields installed in an HP VXI C-size mainframe; accessories, HP P/Ns E1400-80920 and E1421-80920, are available for retrofitting existing HP mainframes HP E1401A/B and HP E1421B, respectively (one accessory per mainframe required).

VXI Characteristics

VXI device type:	Message-based
Data transfer bus:	A24 slave;A16/A24, D8/D16, D32 data read only
Size:	C
Slots:	1
Connectors:	P1/2
Shared memory:	n/a
VXI busses:	Local Bus A-row (left), Local Bus C-row (right), TTL Trigger Bus, ECL Trigger Bus
C-size compatibility:	Yes

Instrument Drivers

See the HP Website (http://www.hp.com/go/inst__drivers) for driver availability and downloading.

Command module firmware:	n/a
Command module firmware rev:	n/a
I-SCPI Win 3.1:	n/a
I-SCPI Series 700:	n/a
C-SCPI LynxOS:	n/a
C-SCPI Series 700:	n/a
HP VEE Drivers:	Yes
VXI*plug&play* Win Framework:	Yes
VXI*plug&play* Win95/NT Framework:	Yes
VXI*plug&play* HP-UX Framework:	No (not available at time of publication)

Module Current

	I_{PM}	I_{DM}
+5 V:	2.9	0.5
+12 V:	0.2	0.04
−12 V:	0.2	0.04
+24 V:	0.1	0.05
−24 V:	0.1	0.05
−5.2 V:	3.6	0.05
−2 V:	1.2	0.12

Cooling/Slot

Watts/slot:	41.50
ΔP mm H_2O:	0.80
Air Flow liter/s:	3.80

Ordering Information

Description	Product No.
Two channel, 20 MSa/s, 12-bit digitizer	HP E1429A
Service manual	HP E1429A 0B3
3 yr. retn. to HP to 1 yr. OnSite warr.	HP E1429A W01
SHIELD, BACKPLANE CONN	HP E1400-80920
VXI BACKPLANE CONN SHLD KT	HP E1421-80920

HP Publication No.: 5965-5565E