Course Number E3795C or Y Scheduled, Dedicated

Agilent 3070 Family Boundary-Scan Concepts & Applications

Overview

Develop an understanding of a powerful technology that provides an alternative solution for the development of complex device test routines, and a methodology to deal with limited access test challenges

Course Overview

Learn concepts of Boundary-Scan technology (IEEE STD 1149.1). The architecture of the TAP (Test Access Port), the functionality of the various registers (BYPASS, boundary, IDCODE), and the structure of the "boundary-cell" in its various forms are described. Operation of Boundary-Scan instructions (EXTEST, BYPASS, Sample/Preload) is addressed. Attain a working knowledge of the industry standard Boundary-Scan Description Language (BSDL). The "state diagram" is used as a tool to understand how the device performs its operations. In-circuit tests are developed and a suite of "interconnect tests" are generated to support efficient limited access testing through the "scan chain." A technique is implemented to test conventional logic via the scan chain (Silicon Nails). Advanced testing concepts such as RUNBIST and INTEST are discussed. Concepts are reinforced with labs where debug techniques are explored.

What You Will Learn

- Over fifteen hands-on labs provide practical experience reinforcing Boundary-Scan concepts. Debug techniques are practiced and diagnostics enhancements are implemented on the 3070.
- The course stays current discussing enhancements to the IEEE 1149.1 standard.
- Important considerations of Design-for-Testability using Boundary-Scan technology are included

Specifications

Course Type
User/Application Training

Audience
3070 programmers who need to understand and implement Boundary-Scan technology and testing techniques

Prerequisites
E1031A and a minimum four months experience using the 3070

Course Length
4½ days

Course Format
Instruction consists of a combination of audio-visual, lectures, and lab exercises.

Delivery Method
Scheduled (at Agilent training location) or *Dedicated* (at customer site)
To save you time and travel, many Agilent courses can be delivered at your site. Agilent can provide required equipment, or save money by furnishing your own.

Detailed Course Agenda

Boundary-Scan Overview
- Boundary-Scan history and evolution
- Concept, purpose (manufacturing faults, test generation time reduction, better diagnostics)
- Test applications: in-circuit and interconnect

Boundary-Scan Fundamentals
- Introduction to BSDL
- TAP (registers: instruction, bypass, boundary, ID), (control signals: tck, tms, tdi, tdo)
- Introduction to the state diagram
- Introduction to the boundary-cell
- Extest, sample/preload, bypass
- Test Macros (e.g. parallel toggle, running toggle, verify bsdl)

Improving Diagnostics
- Conventional ICT: faults on inputs, outputs indicated
- Boundary-Scan diagnostics: ICT diagnostics and improvements

Reducing System Channel Count Requirements
- Fitting large devices on a limited resource system

The State Diagram
- 16 States of the TAP
- Capture-IR (inherent diagnostics), clocking
- Normal (sample, bypass) and test mode (extest)

Scan Chain Testing
- Integrity, powered-shorts, interconnect, connect, bus-wire
- Counting algorithm
- Aliasing
- Adaptive (vs. deterministic)
- Safety issues: limited access, shorts
- Quality issues (non-digital coverage)
- Probe access reduction
- Diagnostics
- Overview of test structure (e.g. interconnect VCL)
- Miscellaneous issues (multiple chains, safe bits, observability, and controlability)
- System chain evaluation and chain override

Scan-Test of Conventional Logic
- Silicon nails
- Issues: timing/speed/vector length, fault masking
- Library vector extraction tools and serializer

Application Specific Issues
- RUNBIST
- INTEST

Improving In-circuit Diagnostics
- Use of connect test for ICT
- Minimal vector set
- Automatic, multiple faults

BSDL
- Automatic program generation
- Vendor supplied
- Synthesis (port and pin mapping, instruction opcodes, cell description)
- Additional BSDL constructs (Hi-Z, clamp, component comformance, group port)

Boundary-Scan Cell Variations
- Cell types including: f10-12, f10-11, f10-17, self-monitoring, f10-22 (reversible) [BC_1, BC_4, BC_2, new_cell, BC_6 resp.]
- Cell definitions
- Defining new cell types

Current and Future Directions
- 1149.1a, 1149.1b, 1149.2, 1149.3, 1149.4, 1149.5

Design-For-Testability
- Boundary-Scan (a design-for-testability tool imposes its own testability constraints)
- Access analysis
- Scan-Path linkers (optional)

Recovering From BSDL Errors
- What NOT to do and what to do if you did!

Disabling Considerations (B Revision Software)
- Disabling Boundary-Scan devices through the scan chain

Debug Techniques

- Converting Scan Chain test to traditional VCL
- Editing the ITL (Interconnect Test Language description)
- Verifying IR and DR (cell) length

Custom Test Development

- Logic Cell Arrays (LCAs)
- Using the SPD.LOG feature (scan port driver log file)

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