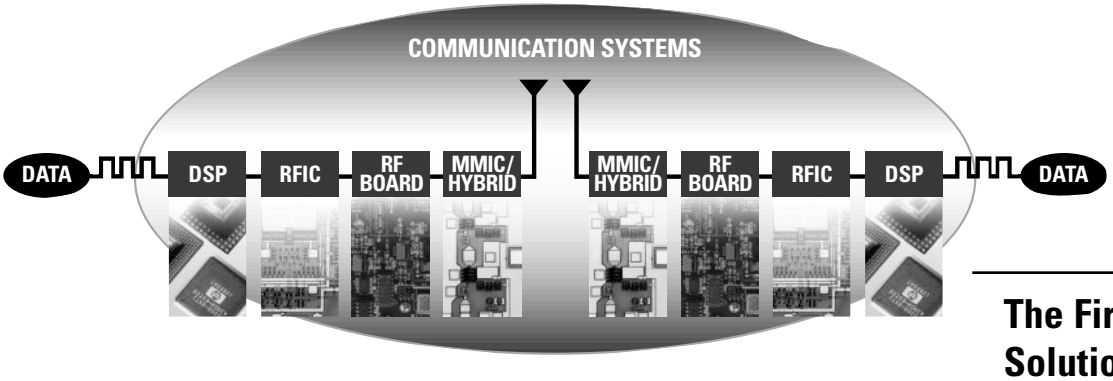
HP Advanced Design System
Release 1.0



The First Integrated Solution for Communication Signal Path Design

Features & Benefits

- Allows simulation and verification of DSP, RFIC, RF board, microwave, and electromagnetic designs prior to costly prototyping.
- Permits co-simulation of RF and DSP solutions to improve design performance and speed product development time.
- Eases creation of optimal RTL for any DSP flow diagram.
- Provides faster new harmonic balance, with reduced memory needs.
- Offers expanded links to HP measurement instrumentation.
- Includes libraries of over 90,000 parts and links to third-party software.

What is HP Advanced Design System?

HP Advanced Design System is a new electronic-design-automation (EDA) software system that helps speed communications products to market. It provides the industry's first integrated, end-to-end signal path design solution to developers of products such as cellular and portable phones, pagers, wireless networks, and radar and satellite communications systems. With this system, HP now provides a full range of communication system design capabilities — from circuit and electromagnetic simulation to digital signal processing (DSP) synthesis and physical design — seamlessly integrated in a single environment.

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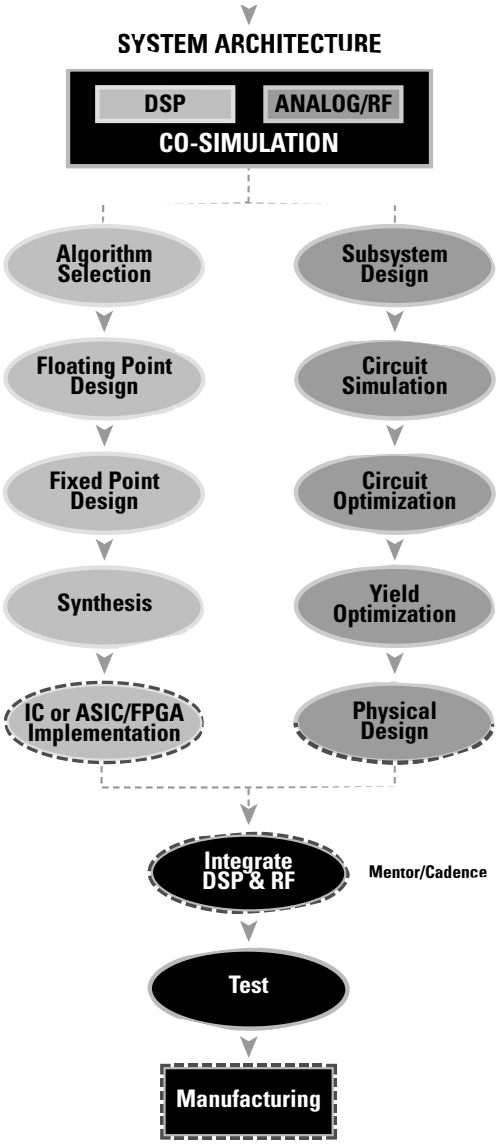
HP Advanced Design System



The Time-to-Market Challenge

The primary challenge facing today's communication product designers is how to reduce the time it takes to get new products into the hands of consumers. Competition is intense. A few months' delay in bringing a new product to market can result in failure of the product offering.

HP Advanced Design System was developed to help bring your communication designs to market in the most expedient and cost-effective manner possible. This new system is the culmination of HP EEsof's years of expertise in developing RF, microwave, and system design automation solutions.

Complete, Integrated Solutions for End-to-End Communication Signal Path Design

HP Advanced Design System is a family of EDA modules that offers designers of communications products a complete signal path solution.

The family is composed of EDA modules including circuit and system simulators, translators, layout solutions, models, libraries, etc. The modules have been selectively bundled into design suites that provide solutions to specific problems.

HP Advanced Design System Suites

HP offers a variety of suites, bundled to provide solutions to communications system, DSP, RFIC, microwave, RF board, layout, and related design problems. The following suites are explained in this document:

- HP Communication Systems Designer
- HP DSP Designer
- HP DSP Synthesis
- HP RFIC Designer
- HP Microwave Circuit Designer
- HP RF Board Designer

This document defines the design suites, their components, their features and benefits, and their applications. The individual modules that comprise the suites are also described.

HP also offers specialized solutions for high-frequency structure simulation and statistical modeling of ICs and nonlinear devices (see page 46).

HP Communication Systems Designer

Features and Benefits

- Provides accurate RF system models for faster development of system specifications.
- Contains bi-directional instrumentation links that provide a better way to control the integration of hardware.
- Offers propagation and matrix models that allow modeling of complete wireless systems.
- Contains hundreds of DSP and analog models for development of algorithms to combat analog effects.
- Co-simulates with MATLAB to leverage your intellectual property models.

Overview
Developed for communication system architects and subsystem designers, this suite lets you model, compare, and trade off architectures, standards, system partitions, specifications, and other factors that affect a system's performance. The suite simplifies the generation of system-level and subsystem-level specifications that are not over- or under-specified. This can translate into significant savings of component development time. A typical radio link, for example, has at least an encoder, decoder, modulator, demodulator, upconverter, downconverter, power amplifier, low-noise amplifier, and IF section. The minimal benefit from not over-specifying these components could exceed one engineering month. Further, the statistical package (included in Premier) offers guidance on how to maximize manufacturing yield and minimize cost. Finally, the ability to download or upload analog and digital signals to instrumentation leads to better analysis and understanding of the hardware during the critical integration phase.

Suite Capabilities
There are three versions of this suite:

- **HP Communication Systems Designer** is tailored for RF system engineers. It contains an RF simulator that accurately predicts performance of complete RF systems. It also includes a set of block-level RF models for linear and non-linear parts. Some functionality is restricted with this version of the suite.
- **HP Communication Systems Designer Pro** offers RF system modeling and general signal processing, including DSP. In addition, it allows co-simulation between RF system models and DSP simulations. For example, this package allows you to implement floating-point DSP algorithms and, in the same simulation, predict system performance measures like BER.
- **HP Communication Systems Designer Premier** extends the suite's simulation capability to include radio propagation models for GSM, IS-95 CDMA, and IS-54 TDMA. And, with the addition of the Matrix model set, you can create block processing models for data compression methods such as JPEG and MPEG. The matrix models also allow you to do bi-directional co-simulation with MATLAB.

Suite Configurations

HP Communication Systems Designer	**E8850A***
Design Environment	
Data Display	
RF System Simulator	
RF System Models	
HP Communication Systems Designer Pro	**E8851A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
RF System Simulator	E8853A/AN
RF System Models	E8854A/AN
HP Ptolemy Simulator	E8823A/AN
Statistical Design	E8824A/AN
HP Communication Systems Designer Premier	**E8852A/AN**
Contains all of HP Communication Systems Designer Pro plus:	
HP Ptolemy Matrix Models	E8826A/AN
Antenna and Propagation Models	E8856A/AN

* Some functionality is restricted:
- File I/O only; instrument I/O not included
- Available node-locked for PC platforms only
- Not expandable with other modules, except with the purchase of E88581A Communication Systems Designer to Unbundled

Note: Throughout this datasheet, all modules have a product number with a suffix. Modules with an 'A' suffix are available node-locked only. Modules with an 'A/AN' suffix are available either node-locked or network licensed.

HP DSP Designer

Features and Benefits

- Provides HP Ptolemy hybrid dataflow and time-domain design and simulation capability for mixed DSP, analog and RF systems.
- Offers ability to co-simulate with analog (High-Frequency SPICE) and RF (Circuit Envelope) simulators to speed the design process.
- Has easy-to-use data export and import capability to measurement instrumentation.
- Works with DSP Synthesis to provide a path from the DSP algorithm to implementation in silicon.
- Comes with MATLAB co-simulation ability for model reuse.

Overview
Designers need DSP design solutions that speed a complete DSP design process and provide the ability to model analog distortions. The physical layer modeling capability of the DSP Designer family enhances your ability to perform these tasks.

The design process starts with the construction of a block diagram that describes the DSP algorithm. This diagram is assembled and wired together in a Windows®-like environment. Each block in the design can be selected from the system's extensive model library or you can create custom models. The suite also includes a Digital Filter module (E8825A/AN) to input filter specifications and generate a schematic design. The HP Ptolemy engine supports mixing of numeric signal processing with analog/RF blocks.

The suite's simulation solutions can then be used to refine and optimize a design. Visual results such as eye diagrams and constellations are available. The suite also includes data display and data processing capabilities to create custom measurements.

Suite Capabilities
HP DSP Designer suite is available in two versions:

- **HP DSP Designer** provides floating-point DSP system design and simulation for the PC only. Designs can include a mix of DSP and analog behavioral models. You can design baseband processors, mixed-signal carrier recovery loops, AGC control loops, modulators, and other building blocks. The suite includes hundreds of DSP behavioral and analog/RF behavioral models and a model development kit. Some functionality is restricted with this suite.
- **HP DSP Designer Pro** is available for the PC and Unix platforms. Combining DSP Synthesis with DSP Designer Pro provides a complete flow from DSP system-level design through RTL output for implementation in silicon. The Pro suite includes fixed-point analysis and matrix models (including bi-directional co-simulation with MATLAB). You can also add options to facilitate modeling of channel propagation characteristics of wireless systems. Finally, this suite can be combined with analog and RF design solutions for mixed-signal design and simulation.

Suite Configurations

HP DSP Designer	**E8820A***
Design Environment	
Data Display	
HP Ptolemy Simulator	
HP DSP Designer Pro	**E8821A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
HP Ptolemy Simulator	E8823A/AN
HP Ptolemy Fixed Point Analysis	E8822A/AN
HP Ptolemy Matrix Models	E8826A/AN
Digital Filter	E8825A/AN

*Some functionality is restricted:
- File I/O only; instrument I/O not included
- Available node-locked for PC platforms only
- Not expandable with other modules, except with the purchase of E8837A DSP Designer to Unbundled

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HP DSP Synthesis

Features and Benefits

- Integrates with DSP Designer, which eliminates need to hand-code HDL.
- Provides estimation capability to preview possible design choices.
- Optimizes according to user-specified constraints to minimize area or maximize performance.
- Uses Adaptive Waveform Comparator to compare test vectors generated from high-level schematic simulation and RTL HDL simulation.
- Incorporates HDL simulator for verification of HDL code.
- Provides schematic generation capability for design optimization.

Overview
The HP DSP Synthesis suite allows you to implement high-level DSP designs into ASICs and FPGAs. With this suite you can optimize designs for the silicon chips of your choice (ASIC or FPGA) and then generate Verilog or VHDL code that can be synthesized at the Register Transfer Level.

DSP Synthesis is integrated with DSP Designer, which eliminates hand coding. This behavioral synthesis capability, combined with DSP Designer's simulation capabilities, permits you to reduce design iterations and to implement design concepts onto silicon in an efficient and accurate manner.

DSP Synthesis takes a schematic design from DSP Designer and optimizes the design for a particular chip, according to your specifications. During the optimization stage, area and performance are considered as variables. A new schematic can be generated for the optimized design and brought back to DSP Designer for simulation and further refinement, or an HDL file can be created and submitted to a logic synthesis solution. The suite also includes an HDL simulator for verification of the resulting HDL code.

Suite Capabilities
This suite is available for the combinations of platforms and HDL languages described under Suite Configurations (at right).

Suite Configurations

DSP Synthesis PC VHDL	**E8838A/AN**
Synthesis Engine	E8836A/AN
Adaptive Waveform Comparator	E8833A/AN
VHDL Models & Code Generation	E8834A/AN
VHDL Simulator*	
DSP Synthesis PC Verilog	**E8830A/AN**
Synthesis Engine	E8836A/AN
Adaptive Waveform Comparator	E8833A/AN
Verilog Models & Code Generation	E8835A/AN
Verilog Simulator*	
DSP Synthesis PC Verilog & VHDL	**E8839A/AN**
Synthesis Engine	E8836A/AN
Adaptive Waveform Comparator	E8833A/AN
VHDL Models & Code Generation	E8834A/AN
Verilog Models & Code Generation	E8835A/AN
VHDL Simulator*	
Verilog Simulator*	
DSP Synthesis UNIX VHDL	**E8831A/AN**
Synthesis Engine	E8836A/AN
Adaptive Waveform Comparator	E8833A/AN
VHDL Models & Code Generation	E8834A/AN
VHDL Simulator*	
DSP Synthesis UNIX Verilog	**E8832A/AN**
Synthesis Engine	E8836A/AN
Adaptive Waveform Comparator	E8833A/AN
Verilog Models & Code Generation	E8835A/AN
Verilog Simulator*	
VHDL Simulator*	
DSP Synthesis UNIX Verilog & VHDL	**E8840A/AN**
Synthesis Engine	E8836A/AN
Adaptive Waveform Comparator	E8833A/AN
VHDL Models & Code Generation	E8834A/AN
Verilog Models & Code Generation	E8835A/AN
VHDL Simulator*	
Verilog Simulator*	

*No part number (not sold separately)

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HP RFIC Designer

Features and Benefits

- Permits co-simulation of RF and DSP designs, and of combined system-level behavioral blocks and circuit-level components, to validate overall signal-path design.
- Provides multiple simulation capability, from one schematic, in frequency, time, and modulation (Circuit Envelope) domains to validate overall design against diverse digital wireless standards.
- Contains optimization technologies and statistical design techniques to maximize design performance and improve yield.
- Provides links to third-party EDA solutions and libraries to ensure efficient design flows.

Overview
Typical RFICs are composed of diverse building blocks such as low-noise amplifiers, mixers, oscillators, phase-locked loops, power amps, and automatic level-control loops. These components require different simulation technologies to obtain desired design accuracies within realistic simulation times. HP RFIC Designer suites combine high-frequency simulation and optimization technologies with accurate models, tailored for RFIC designers. The suites combine five different simulation technologies operating in the time, frequency, and hybrid "frequency-time" domains. The ability to simulate and analyze an overall system of RF and DSP circuits in both the frequency and time domains, from one schematic, makes these suites invaluable design solutions. Solutions link to third-party EDA solutions and libraries.

Suite Capabilities
HP RFIC Designer is available in two versions:

- **HP RFIC Designer Pro** brings together the most often-used RFIC circuit simulation technologies. With Circuit Envelope, Harmonic Balance, Linear, and the new HP EEsof High-Frequency SPICE simulators available from a single schematic, you can simulate and optimize the performance specifications of RFIC chip sets. In addition, existing designs in netlists from Berkeley SPICE, PSpice, and HSPICE can be brought into this suite for simulation.
- **HP RFIC Designer Premier** adds user-defined modeling, statistical design, RF system models and convolution simulation to the RFIC Designer Pro. An Analog Model Development Kit (E8890A/AN) allows proprietary foundry models to be compiled and used. Measured RFIC package parasitics can be converted to equivalent low-pass networks using the SPICE model generator. The Statistical Design module (E8824A/AN) accounts for process variations and optimizes for yield. The RF System Models (E8854A/AN) facilitate accurate design partitioning and RF subsystem design. The Convolution Simulator (E8885A/AN) extends high-frequency simulation to include arbitrary frequency-domain data such as S-parameters and arbitrary transfer functions.

Suite Configurations

HP RFIC Designer Pro	**E8888A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
Linear Simulator	E8881A/AN
Harmonic Balance Simulator	E8882A/AN
Circuit Envelope Simulator	E8883A/AN
High-Frequency SPICE	E8884A/AN
SPICE Netlist Translator	E8880A/AN
HP RFIC Designer Premier	**E8889A/AN**
Contains all of HP RFIC Designer Pro plus:	
Convolution Simulator	E8885A/AN
Statistical Design	E8824A/AN
RF System Models	E8854A/AN
Analog Model Development Kit	E8890A/AN
SPICE Model Generator	E8891A/AN

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HP Microwave Circuit Designer

Features and Benefits

- Provides accurate simulation and analysis of distributed elements and discontinuities to analyze the effects of a circuit's physical design.
- Allows large circuits to be simulated faster, using less memory.
- Includes a statistics capability to check manufacturability and anticipated yield of designs.
- Processes time-varying effects to allow signals to be traced to point of degradation.
- Provides physical layout capabilities and optional translators via the Layout module.

Overview
HP developed this group of solutions for the accurate simulation and analysis of distributed elements and discontinuities typically found in MIC and MMIC designs. It helps designers account for the affects of physical design on their circuits' performance.

Library models for high-frequency transistors and diodes are included (E8952A/AN and E8954A/AN), to define the circuit down to the component level. Detailed circuit-level descriptions can be built using accurate microstrip, stripline, suspended stripline, and coplanar waveguide models. And a statistics capability (E8824A/AN) allows you to check the manufacturability and anticipated yield of your design.

Suite Capabilities
HP Microwave Circuit Designer suite is available in two versions:

- **HP Microwave Circuit Designer Pro** suite focuses on frequency-domain analysis for linear and non-linear circuits by using HP's new Harmonic Balance Simulator (E8882A/AN). This simulator gives steady state results represented as a complex frequency spectrum. Improvements in this simulator allow much larger circuits to be simulated, faster, using less memory than in previous versions of harmonic balance.
- **HP Microwave Circuit Designer Premier** suite adds analysis capability to the Pro suite. The addition of the Circuit Envelope Simulator (E8883A/AN) to the suite enables you to extend harmonic balance to include time-varying effects. This allows for the efficient analysis of analog and digital modulation of a carrier signal, certain phase-locked loops (PLL), automatic gain control (AGC), video switching, and other time-varying events. You can trace a complex signal through a circuit and examine it at every point to find out where, and to what extent, the signal degrades. RF System Models (E8854A/AN) add behavioral modeling capability to the circuit-level modeling provided. If a model is not provided, the Analog Model Development Kit (E8890A/AN) gives you a convenient way to add custom models.

Suite Configurations

Microwave Circuit Designer Pro	**E8911A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
Linear Simulator	E8881A/AN
Harmonic Balance Simulator	E8882A/AN
Statistical Design	E8824A/AN
Microwave Transistor Library	E8952A/AN
High-Frequency Diode Library	E8954A/AN
Microwave Circuit Designer Premier	**E8912A/AN**
Contains all of Microwave Circuit Designer Pro plus:	
Circuit Envelope Simulator	E8883A/AN
RF System Models	E8854A/AN
Analog Model Development Kit	E8890A/AN
Layout	E8902A/AN

Note: Throughout this datasheet, all modules have a product number with a suffix. Modules with an 'A' suffix are available node-locked only. Modules with an 'A/AN' suffix are available either node-locked or network licensed.

The Premier suite also adds Layout (E8902A/AN), so that hybrid-circuits or MMIC designers can do physical design. You can choose to build your circuits in either the schematic window or the layout window. To manufacture the circuit or send it to the mechanical designer, Layout's optional translators help with that part of the job. Layout also serves as the entry point for our optional electromagnetic simulator HP Momentum (E8921A/AN).

HP RF Board Designer

Features and Benefits

- Allows circuit- and system-level models in a single schematic.
- Permits frequency, time, and mixed time/frequency simulations.
- Provides multiple optimization techniques, over 90,000 vendor parts, and the ability to acquire measured data from instrumentation.
- Incorporates a high-frequency layout solution with vendor part footprints, EM simulation, DRC, and artwork generation in several output formats.
- Offers links to third-party EDA solutions and libraries to ensure efficient design flows.

Overview

The RF Board Designer suites address the challenges of board-level RF design. The suites range in capabilities, from basic linear analysis with RF Designer to complex modulation analysis and physical design with RF Board Designer Premier.

Overall, RF Board Designer suites allow you to create your board from concept to manufacturing. System simulation allows analyzing RF system block diagrams for performance tradeoffs. Test your design with the multiple circuit simulators (Linear, Harmonic Balance, Circuit Envelope), then compare the results with measured data. Optimize for best performance using Discrete Value Optimization and vendor SMT parts. Create the physical design including SMT part footprints, then generate the artwork and bills-of-material to manufacture the board. If the RF design must be combined with analog/digital circuitry, links to third party EDA solutions like Mentor Graphics* can be used.

Suite Capabilities

HP RF Board Designer is available in three versions:

- **HP RF Designer** is a low-cost suite that provides linear circuit simulation on the PC. You can analyze S-, Z-, Y-, and H-parameters, noise figure, group delay, and more, plus optimize performance. Some functionality is restricted compared to the base modules, and expansion is limited to the Layout Basic module only. Designs created are compatible with RF Board Designer Pro/Premier.
- **HP RF Board Designer Pro** improves on the RF Designer capabilities. It is fully expandable and has no functionality restrictions in linear simulation. You can analyze nonlinear effects with Harmonic Balance such as mixer noise figure and large-signal S-parameters. By including common RF part models and vendor SMT parts, manufacturing yield analysis and optimization can be performed.
- **HP RF Board Designer Premier** adds capabilities to the Pro suite. It provides the capability to analyze how your circuit handles complex modulation schemes via eye diagrams and adjacent channel power ration, and the ability to create and simulate the multilayer board layout.

Suite Configurations

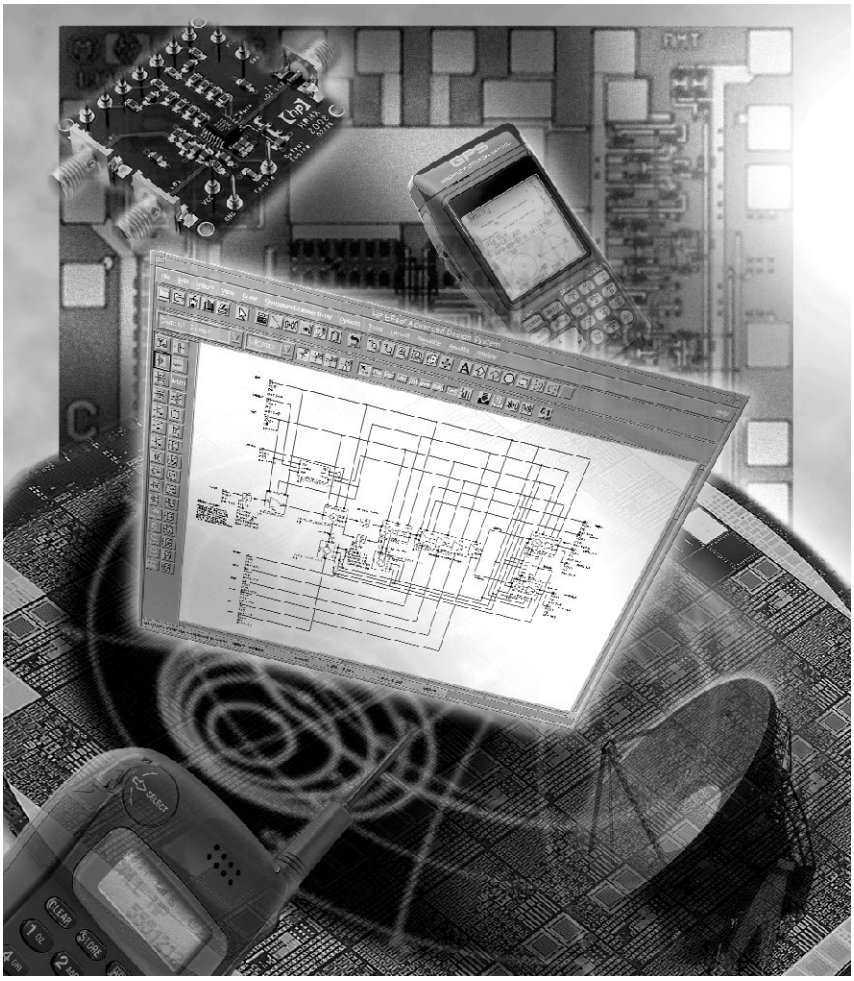
HP RF Designer	**E8940A***
Design Environment	
Data Display	
Linear Simulator	
Optional:	
Layout Basic	**E8944A****
Layout	
Gerber Translator	
HP RF Board Designer Pro	**E8942A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
Linear Simulator	E8881A/AN
Harmonic Balance Simulator	E8882A/AN
Statistical Design	E8824A/AN
RF Passive Circuit Models	E8950A/AN
RF Transistor Library	E8953A/AN
RF Passive SMT Library	E8956A/AN
HP RF Board Designer Premier	**E8943A/AN**
Contains all of RF Board Designer Pro plus:	
Circuit Envelope Simulator	E8883A/AN
Layout	E8902A/AN
Multilayer Interconnect Models	E8951A/AN
RF System Models	E8854A/AN

* Some functionality is restricted:
- 9-port limitation on linear simulation
- Two types of optimization (random, gradient) supported
- File I/O only; instrument I/O not included
- Available node-locked for PC platforms only
- Not expandable with other modules, except with the purchase of E8941A RF Designer to Unbundled.

** Some functionality is restricted:
- Gerber Translator only (DXF not included)
- One-way schematic to layout design synchronization only
- Does not support layout simulation
- Available node-locked for PC platforms only
- Not expandable with other modules, except with the purchase of E8945A Layout Basic to Unbundled

Note: Throughout this datasheet, all modules have a product number with a suffix. Modules with an 'A' suffix are available node-locked only. Modules with an 'A/AN' suffix are available either node-locked or network licensed.

Design Environment



The HP Advanced Design System is composed of approximately 50 EDA modules that include design capture and layout solutions, simulators, model sets, libraries, and translators.

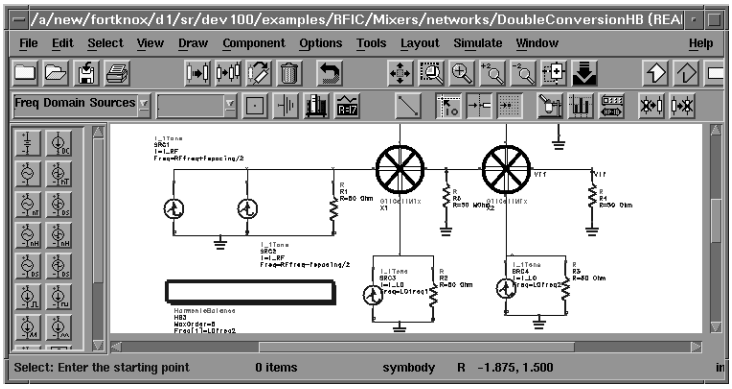
Included in this section are descriptions of the Design Environment and Data Display modules, as well as the Design Environment's instrument server capabilities. These modules form the basic platform and provide the user interface for almost all other HP Advanced Design System modules and design suites.

Design Environment

(E8900A/AN)

Features and Benefits

- Includes schematic editor for graphic manipulation and entry of RF and DSP designs.
- Allows designs and data files to be structured in your preferred hierarchy.
- Comes with easy-to-learn, flexible user interface.
- Integrates RF/DSP/EM design technologies into one user interface, eliminating need for separate tools and file transfers.
- Offers extensive ability to customize the environment for ease of use.



Overview
The Design Environment is a graphical environment for the creation, simulation, and documentation of RF and DSP designs. It provides the integration and design capture framework for plugging in our other modules, including simulators, layout, and libraries.

Design entry of RF and DSP designs is provided through a schematic page that offers both pull-down menus and a command toolbar, either of which may be customized. Components can be accessed through logically-organized palettes, as well as textual library lists or a library browser dialog. From the schematic, one or more simulations may be specified, controlled, and launched. Designs may be used as subnetworks to other designs through the schematic page; parameters can be passed to such subcircuits, which then serve as custom models.

Project organization for all files associated with a design, including data files, subnetworks, custom artwork, and user settings, is automatically provided by the Design Environment. All of these files are ASCII text files available in system default or user-specified directories. Projects can provide current revisions of a design, as well as older iterations and alternate design approaches. Because all networks of a project are maintained together, designs or portions of designs may be re-used without the need to copy them first.

The user interface was designed to have the look and feel of popular PC office tools. Toolbars, component palettes, icons, and keyboard shortcuts all provide easy access to frequently used features. System and circuit elements can be selected from palettes and placed with the mouse; they are inserted along with their parameters onto the page, ready for connection by wiring or transmission line. Component parameters can be edited on-screen, as can component types (for example, a resistor can be changed to a capacitor simply by typing in the new name, eliminating the need for deletion and rewiring). A full on-line help facility that includes both context-sensitive command help and on-line documentation is provided.

The Design Environment provides the integration of all the HP Advanced Design System design technologies in one user interface. Circuit simulations of various components may be embedded into system simulations; planar electromagnetic analysis may also be performed on part or all of a circuit, and the data fed into further circuit simulations. (EM simulation may be performed without need of a file translation or explicit meshing). Designs may be created and edited from both the schematic and the layout, allowing you to work in either the electrical or physical representation, whichever better suits a given design.

Ability to customize the environment is provided through the Application Extension Language (AEL), a C-like language that can be used for a wide variety of tasks. Because Advanced Design System's application interface is written with AEL, your own customizations can interact extensively with the system. AEL can be used for such things as generating custom libraries and layout routines, querying the database for design information, setting system preferences and options, and overriding higher-level default configurations with those for a specific project or user.

Instrument Server
The instrument server capability is built into the Design Environment, and provides a control facility for bi-directional data exchange with all instruments supported by the HP Advanced Design System. You can acquire data from network analyzers, spectrum analyzers, and oscilloscopes. Such data can be used to represent individual components, instead of datasheet or equation data; it can also be used as a real-world simulation source.

The instrument server requires either an HP-IB card or a National Instruments GP-IB card to be present in the computer communicating with the instrument.

For network analyzers, rectangular S-parameters are captured and stored.

Supported Network Analyzers:

HP 8510B,C	HP 8702
HP 8703	HP 8719
HP 8720	HP 8722
HP 8752	HP 8753
Wiltron 360	

For spectrum analyzers, amplitude vs. frequency data is captured.

Supported Spectrum Analyzers:

HP 71100A	HP 71200A
HP 71201	HP 71210A
HP 8560	HP 8561
HP 8562	HP 8563
HP 8566A,B	HP 8567A
HP 8568A,B	

For oscilloscopes, voltage vs. time data is captured.

Supported Oscilloscopes:

HP 54100A,D	HP 54110D
HP 54111D	HP 54120
HP 54121	HP 54122
HP 54123	HP 54710
HP 54720	HP 54750

Other Supported Instruments
HP 70820A Microwave Transition Analyzer — for this instrument, a range of data acquisition is possible, including complex amplitude vs. frequency; complex amplitude vs. time; and table frequencies.

Additional Models
The HP Ptolemy module also includes models that allow designers to download simulation data to various instruments.
Please see page 21.

File I/O
The Design Environment supports the import and export of Series IV mask (.msk) files as well as the import of HPGL/2 files.

HP Advanced Design System supports the following file formats for reading files into and writing files out of the dataset:

- Touchstone
- A number of formats of MDIF: MODEL_MDIF, P2D, S2D, IMT, SPW, TIM, T2D, SDF*, GEN_MDIF
- Citifile (for file read only)
- Rawfile

* Supports HP 89441 Vector Signal Analyzer

Data Display (E8901A/AN)

Features and Benefits

- Allows graphical display of simulation results, with a full set of plot types, trace types, and annotation of plots and traces, to better understand design performance.
- Permits storage and retrieval of previous simulation results for viewing and comparison to ongoing design simulations.
- Provides ability to view and manipulate data in custom equations and expressions.
- Autoscaling for data fit and markers allows users to isolate and review data points quickly.

Overview
The Data Display module allows simulation results to be viewed graphically, much as they appear on analyzers and other instruments. Graphs can be customized with a choice of markers, colors, line styles, and captions. Portions of plots can be instantly enlarged, and multiple data display windows can view the same data file, giving you the ability to look at your data in several ways simultaneously. Plot types include rectangular, polar, Smith (including impedance, admittance, and impedance plus admittance), stacked rectangular (multiple y-axes overlaid onto one x-axis), and listing columns. Trace types include line, scatter, histogram, digital, spectral, and "bus trace" (display of binary data for a whole bus, up to 128 bits width).

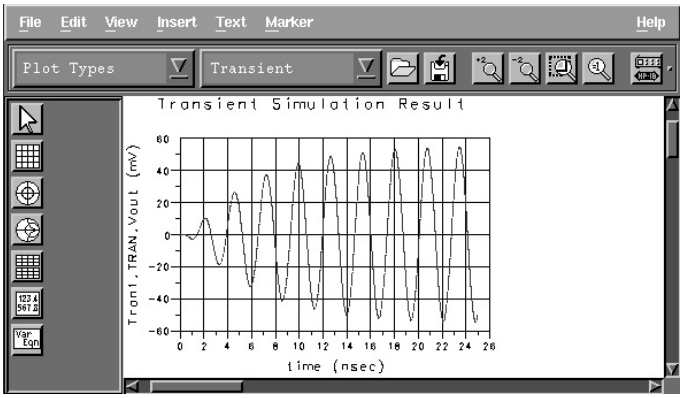
Both plots and traces allow choice of line thickness, color, and line style. Plots can be annotated with a full range of drawing elements, including lines, rectangles, circles, text, polygons, and polylines.

Through its uses of a concept called "datasets", the Data Display module allows you to slice your data for viewing and graphical analysis in any manner. Datasets maintain persistent storage of simulation results so that you can pull out all the data related to any single parameter or simulation control factor — you don't have to resimulate to create a different view of your data. The results of different simulations in different datasets can be plotted to the same Data Display window, allowing you to make comparisons.

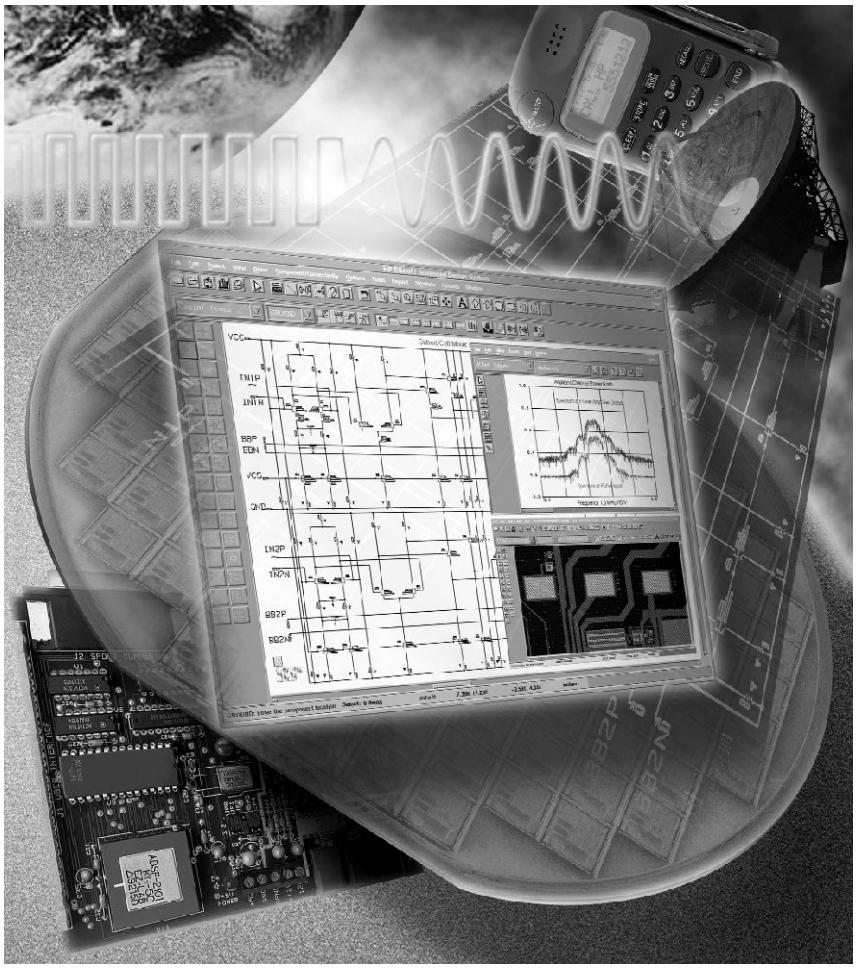
The ability to manipulate data in datasets with your own equations means that you can study the simulation results with flexibility. Dialog boxes show you all the data available to help you build your equations. Many useful expressions, such as eye diagrams, histograms, adjacent-channel power ratio, fast Fourier transforms, and VSWR are built in.

Autoscaling of axes on plots is provided to enable best fit of data and regular tick mark spacings. Manual scaling is allowed as well. Markers are also available, allowing you to obtain a read-out of specific data values at any given point. Delta markers enable you to look at incremental trace values with respect to a reference point on that trace.

Configuration Detail
Requires the Design Environment module (E8900A/AN).



Simulators



Circuit Simulation Modules

HP Advanced Design System groups its circuit analysis capability by simulator type. If you have multiple simulators available, the appropriate simulator engine is selected automatically based on the type of analysis you want to perform.

The following circuit simulators are available:

- Linear Simulator for linear and small signal S-parameter analyses
- Harmonic Balance Simulator for steady-state response from mixers, oscillators, and power amplifiers
- Circuit Envelope Simulator for analyzing complex modulation
- High Frequency SPICE to analyze transient and/or start-up effects
- Convolution Simulator to account for dispersion and skin effects in High-Frequency SPICE

Linear Simulator (E8881A/AN)

Features & Benefits

- Offers parametric subnetworking for design customization and convenience.
- Permits variables, equations and functions specific to each subnetwork.
- Permits generalized noise analysis with temperature.
- Offers circuit optimization for maximizing performance.
- Contains microstrip, stripline, Finline, and Coplanar waveguide models.
- Allows creation of user-defined linear models and output equations for design flexibility.
- Capable of back-annotating the DC solution at all nodes directly onto the schematic, without having to resimulate.
- Includes Monte Carlo analysis to predict manufacturing yield prior to production.
- Provides Symbolically-Defined Device (SDD) and Frequency-Defined Device (FDD) to allow simulating large- and small-signal behavior of a nonlinear device without having to write C code.
- Offers SDD ability to model high-level circuit blocks such as mixers or amplifiers resulting in faster simulation runs.

Overview
Linear frequency-domain circuit simulation is used to analyze and optimize RF and microwave circuits (e.g., amplifiers, oscillators, couplers, filters, matching networks) that operate under linear conditions. The technology can be applied to the design of passive and small-signal active circuits used in wireless, RF, microwave, surveillance, radar, and other communication applications.

Once the circuit is drawn, this simulator allows you to check the topology automatically for unconnected pins and wires. The simulator then performs all necessary linear measurements such as S-, Z-, Y-, and H-parameters, circuit impedance and admittance, reflection coefficients and VSWR, gain, loss, noise, unilateral gain, noise figure, input/output noise temperature, group delay, stability factor, stability measure, and noise-gain-stability circles. In addition, the simulator can perform Swept Parameter Analysis, such as noise figure versus a change in a component value.

The simulator's extensive passive and small-signal active device-model libraries include many of the parts needed for the high-frequency designs, including improved multilayer coupled-line element models. The simulator also can perform linear analysis with nonlinear models at user-defined DC bias. And it offers a parametric subnetworking feature that allows customizing and the use of any existing subnetwork from another design.

A Statistical Design package uses the Monte Carlo method to predict yield by simulating a product's manufacturing process where the units produced have randomly-varying component values (e.g., amplifiers, mixers). This helps to identify which components in your design require tighter control than others. A component's pass/fail status is determined by comparing your design's simulated performance to your design's actual requirement. Yield is then defined as the percentage of units passed.

A Symbolically-Defined Device (SDD) and a Frequency-Defined Device (FDD) allow you to create a user-defined model by specifying, on the circuit schematic, algebraic relationships for the port variables without having to write source code.

Configuration Detail
Requires the Design Environment module (E8900A/AN). The simulator includes the Circuit Models listed on page 18.

Harmonic Balance Simulator (E8882A/AN)

Features & Benefits

- New technology provides significant improvements in memory usage and simulation times.
- Simulates and optimizes nonlinear steady-state response of circuits.
- Offers swept variable analysis, parametric subnetworks, and large signal S-parameters.
- Capable of performing and displaying complex user-defined post-processing functions.
- Frequency-Defined Device (FDD) is a powerful model used for nonlinear, behavioral modeling in both frequency and time domains without having to write C code.

Overview
This fast Harmonic Balance simulator is especially useful for the design of nonlinear circuits used in wireless RF and microwave communication systems. The simulator is based on a new Krylov-subspace iterative solver algorithm that offers significant improvements in speed and memory usage over previous versions of this simulator. It simulates and optimizes the nonlinear steady-state response of amplifiers, multipliers, mixers, oscillators RF system models, etc. It provides performance measures such as DC bias, mixer-noise figure, oscillation frequency and phase noise, large-signal S-parameters, and power-added efficiency. And it offers swept variable (e.g., power, frequency or circuit parameter) analysis, parametric subnetworks, and large-signal S-parameters.

Post-Processing Measurements
In all analyses, node voltages and branch currents are computed and stored for display without resimulation. Complex user-defined post-processing functions, such as integration of a spectrum, conversion of simulation data to match formats of published wireless standards, vector and matrix operations, can also be accomplished within the post processing data display environment. Popular SPICE-type sorted listing of circuit noise contributors is now available for linear and nonlinear noise analyses.

Performance Optimization
All circuit and system simulators can work in conjunction with ten different optimizers, ensuring that you obtain the best performance possible from your designs. Please see page 24 for details.

Frequency-Defined Device
The FDD Model enables nonlinear devices, such as phase and frequency detectors, VCOs, modulators, and frequency multipliers, to be more naturally described in the frequency domain, rather than in the time domain.

Another class of the FDDs can be used in both frequency and time domain. An example is a clock or carrier-recovery circuit whose output frequency is based on the input zero-crossing trigger-time interval.

Configuration Detail
Requires the Linear Simulator (E8881A/AN) and the Design Environment (E8900A/AN).

Circuit Envelope Simulator (E8883A/AN)

Features and Benefits

- Simulates sophisticated modulated signals in high-frequency circuits whose characterization was previously impractical or impossible with SPICE or Harmonic Balance.
- Speeds the design of modern communication circuits based on CDMA or TDMA technologies.
- Optimizes circuits in the time domain for best modulation characteristics, such as VCO frequency settling time.
- Characterizes RF feedback loops to aid in the design of phase-locked loops and Automatic Gain Control circuits.
- Efficiently analyzes higher-order (3rd, 5th, 7th) mixer intermodulation products and predicts spectral regrowth of amplifiers and mixers.

Overview
The HP Circuit Envelope Simulator allows the sophisticated, modulated signals found in today's communication circuits and subsystems to be efficiently and accurately analyzed. The simulator analyzes amplifiers, mixers, oscillators, and feedback loops in the presence of modulated or transient high-frequency signals.

Circuit Envelope's technology lets you analyze modulated and transient RF signals by employing a hybrid time- and frequency-domain approach. It samples the complex modulation envelope (amplitude and phase, or I and Q) of the carrier in the time domain and then calculates the discrete spectrum of the carrier and its harmonics for each envelope time sample. Thus, the output from the simulator is a time-varying spectrum from which useful information, such as PLL frequency-vs-time transients, ACPR (adjacent channel power ratio), EVM (error vector magnitude) and NPR (noise power ratio) can be derived.

In Comparison to SPICE
Because Circuit Envelope simulation samples the modulation envelope instead of the carrier, it has an inherent speed efficiency over SPICE. Unlike SPICE, the modulation amplitude and phase of any carrier harmonic is directly accessible for display or time-domain optimization without the need for intermediate post-processing. Where SPICE has to rely on lumped-element approximations, Circuit Envelope simulation can include accurate frequency-domain models, such as S-parameter data or microstrip discontinuities.

In Comparison to Harmonic Balance
Instead of representing the modulated signals as the sum of Fourier harmonics, as in the Harmonic Balance simulator, Circuit Envelope technology computes the modulation information in the time-domain, leaving only the RF carrier and the LO for fast, accurate simulation in the frequency domain. Circuit Envelope technology is therefore faster than a regular harmonic balance simulation and also consumes less computer memory. In addition to its efficiency, Circuit Envelope can analyze RF transient response such as PLL lock times, which Harmonic Balance cannot.

Time-Domain Optimization
In addition to simulating the instantaneous amplitude, phase and frequency of any signal harmonic, you can also optimize circuit-transient performance using the new time-domain optimization capabilities in HP Advanced Design System. For example, you can optimize for the transient response of AGCs and for the locking time of phase-lock loops.

Configuration Detail
Requires the Harmonic Balance Simulator (E8882A/AN), the Linear Simulator (E8881A/AN), and the Design Environment (E8900A/AN).

High-Frequency SPICE Simulator (E8884A/AN)

Features & Benefits

- Analyzes low- and high-frequency, linear and non-linear large circuits in the time-domain.
- Directly uses high-frequency models such as microstrip and stripline transmission lines, bends, and gaps.
- Annotates on the schematic the complete solution at time=0.
- Provides time-domain optimization, overload-alert warning, swept-variable analysis, user-defined measurements and voltage, and current probes at any labeled node in the design.
- Time- to frequency-domain transform allows RF designers to view results in the frequency-domain.

Overview
High-Frequency SPICE is particularly suited to time-domain analysis of large high-frequency RFICs that have thousands of transistors. It is used to analyze the steady-state response of mixers, oscillators, amplifiers, and other circuits. It is also used to verify transient behavior, such as start-up times in oscillators, filter step-function responses, pulsed RF network responses, high-speed digital and switching circuits, and more.

This simulator has been completely re-designed. It now offers all the regular features of SPICE transient analysis plus improved convergence for large circuits and such additional features as DC back-annotation to the schematic. In addition, the simulator is able to use many high-frequency models, such as microstrip transmission lines, bends and gaps, without requiring the user to transform the

models into RLC equivalent circuits or revert to convolution. This is made possible by representing these frequency-domain analytic models in terms of their Laplace transforms. In High-Frequency SPICE, the frequency dependent elements are modeled with an approximation that neglects some of the frequency dependent effects, such as dispersion and high-frequency loss, resulting in faster simulations. For more accurate frequency models with dispersion effects and high-frequency loss, the Convolution Simulator should be used in conjunction with the High-Frequency SPICE simulator, at the expense of longer simulation times.

High-Frequency SPICE supports extensive non-linear models such as MOSFETs, MESFETs, and BJTs, and lumped and distributed models such as capacitors, inductors, resistors, and single and coupled transmission lines. It can perform nonlinear transient analyses with respect to optional swept variables. For example, you can plot the transient response of an amplifier with respect to another changing variable such as power or component value. When your design is analyzed, circuit branch currents and node voltages are calculated at each time step and can be saved for measurement or subsequent probing. The complete DC solution at t=0s can be back annotated to the schematic for viewing.

Additional capabilities of this simulator are time-domain optimization, overload alert (for checking breakdown voltage, excessive currents and power dissipation), and user-defined measurements. User-defined measurements can be manipulated mathematically using the built-in post-processing capability. The time-domain to frequency-domain transform feature allows RF designers to view the output results in the frequency domain.

Configuration Detail:
High-Frequency SPICE requires the Linear Simulator (E8881A/AN).

Convolution Simulator (E8885A/AN)

Features and Benefits

- Accurately analyzes effects of discontinuities, dispersion, skin effects, and losses in transmission lines, all of which are important at high frequencies.
- Extends the capability of the High-Frequency SPICE Simulator (E8884A/AN) by including arbitrary frequency-domain data files such as S-parameters.
- Allows swept-variable analysis for reaching optimum solutions.
- Time- to frequency-domain transform allows RF designers to view results in the frequency-domain.

Overview
The Convolution Simulator is an advanced time-domain simulator for high-frequency circuits. This simulator requires a High-Frequency SPICE license to run. It extends the capability of the High-Frequency SPICE Simulator (E8884A/AN) and can handle circuits that contain distributed elements and S-parameter data used for components. It can analyze circuit start-up conditions and transients and can accurately analyze the effects of discontinuities, dispersion, skin effects, and losses in transmission lines. The simulator can also produce transient nonlinear analyses with respect to optional swept variables.

It can accurately simulate the frequency-dependent behavior of distributed elements, such as microstrip and stripline, which cannot be analyzed properly by SPICE-type tools. The results are more accurate, at the expense of longer simulation time. Unlike High-Frequency SPICE, the Convolution Simulator can also simulate circuits that contain components characterized with measured S-parameter data, and it is particularly suitable for analyzing transient conditions where the effects of dispersion and discontinuities are significant.

It allows user-defined measurements, and voltage and current probes of designs. User-defined measurements can be manipulated mathematically using the simulator's built-in post-processing capability. The time to frequency-domain transform feature allows RF designers to view the output results in the frequency domain.

Configuration Detail
Requires the High-Frequency SPICE Simulator (E8884A/AN).

Circuit Models

An extensive set of passive and active linear and nonlinear models works with each of the circuit simulators.

HP EEsof Semiconductor Device Models

The following bias-dependent models function both as nonlinear and linear models over the entire operating bias range of the device. HP EEsof's libraries of commercial devices are designed to work with these models.

- The EEFET3 is a scaleable, bias dependent, empirical MESFET model. It accurately models both DC and RF characteristics on a wide class of devices
- The EEHEMT1 model is a scaleable, bias dependent, empirical HEMT model
- The EEMOS1 is a bias-dependent power MOSFET model
- The EEBJT2 model is a semi-physical, quasi-static, analytical BJT model. It was designed to accurately model the behavior of NPN and PNP transistors in all regions of bias and in all device configurations
- The HP Diode Model is HP EEsof's diode model

Public Domain Semiconductor Device Models

Linear Models

- Hybrid Pi and T-equivalent bipolar transistor
- Bipolar transistor models with alpha and beta current gains
- FET models with and without source resistance
- FET noise models
- Dual-gate FET
- PIN diodes

Nonlinear Models

- **MESFET/HEMT Models**
  - Curtice quadratic
  - Curtice cubic
  - Advanced Curtice
  - Statz, et. al. (Raytheon)
  - TOM scaleable
  - HP Root MESFET/HEMT
  - EEFET3 and EEHEMT1
  - EETOM1
  - Materka and Modified Materka
  - Tajima
- **BJT Models**
  - Gummel-Poon, NPN, and PNP; with and without substrate terminals
  - EEBJT2
  - VBIC
  - Philips MEXTRAM
- **MOSFET/JFET Models**
  - N and P MOSFET
  - HP Root MOSFET
  - EEMOS1
  - BSIM1,2,3 MOS
  - MOS level 1,2,3
  - Philips MOS Model 9
  - Advanced Curtice JFET
- **Diode Models**
  - HP Root
  - PN diodes

Passive Element Models

- Transmission Line Components
- Microstrip elements
  - Junction and discontinuity models
  - Single and multiple coupled lines with skin-effect loss and frequency dispersion
  - Coupled line filter section
  - Sidewall and cover effects
  - Thin-film capacitors and resistors
  - One-, two-, and four-port interdigital capacitors
  - Four-, six-, and eight-finger Lange Couplers
  - Tapered via hole, bond-wire, and ribbon
  - Spiral and rectangular inductors and interdigital capacitor
- Stripline elements
  - Single and coupled transmission lines with skin-effect loss
  - Offset Stripline
  - Junction and discontinuity models
    - Tees
    - Cross
- Suspended substrate elements
  - Single and coupled transmission lines with skin-effect loss
  - Multilayer printed circuit board coupled lines (up to 10 lines and 7 di-electric layers)
- Coplanar waveguide
  - Single and coupled lines
  - Junctions and discontinuities
- Distributed elements, including ideal, physical, and coaxial transmission line with coupling
- Rectangular waveguide
- Finline models
- General lumped element models, including resistors, capacitors, inductors, coupled coils, transformers, and gain, phase shift, and time delay elements
- Antenna impedance elements

SPICE Netlist Translator (E8880A/AN)

Features and Benefits

- Provides access to SPICE netlists in the schematic.
- Imports SPICE netlists from: Berkeley SPICE 2G6, 3C, 3E; PSpice; HSPICE; HP SPICE.
- Allows existing SPICE netlists to be analyzed and optimized with a full range of high-frequency circuit simulators.

Overview
The SPICE Netlist translator allows your existing designs in PSpice, HSPICE, and Berkeley SPICE to be translated into an HP Advanced Design System subnetwork for analysis. Once in the system, the designs can be analyzed with our full range of high-frequency circuit simulators (e.g., Convolution, S-parameter, Harmonic Balance, and Circuit Envelope). This technology provides more analyses and answers to your existing design problems than available from SPICE alone. This translator allows you to analyze such problems as ACPR, mixer-noise figure and phase-locked loop transients.

Configuration Detail
Requires the Design Environment module (E8900A/AN).

System Simulation Modules

The following system simulation modules are available in HP Advanced Design System:

- HP Ptolemy
- RF System

HP Ptolemy Simulator (E8823A/AN)

Features and Benefits

- Provides hybrid dataflow and time-domain design and simulation capability for mixed DSP, analog and RF systems.
- Comes with extensive DSP, communications, analog and RF model libraries to assemble reference systems quickly.
- Incorporates a user-defined C or C++ model builder that provides a "plug and play" approach to adding models to HP Ptolemy.
- Provides ability to co-simulate with analog (High-Frequency SPICE) and RF (Circuit Envelope) simulators.
- Comes with over 20 different optimization algorithms for fine-tuning system designs based on user-specified design goals.

Overview
The HP Ptolemy Simulator is a system-level simulation and design solution based on a hybrid of dataflow and timed-synchronous dataflow technologies. It allows you to design and simulate DSP, RF and analog designs such as RF and DSP receivers and transmitters, modems, cellular phones, radar, etc.

HP Ptolemy uses innovative simulation technologies to enable design and simulation of purely DSP-based circuits such as FIR ilters or digital Costas loops. In the same environment, it also provides the capability to analyze RF circuitry chains such as amplifiers, mixers, and filters. The digital portion of the module helps you construct sophisticated algorithms and simulate and observe performance via bit error rate, eye diagrams, constellation diagrams and other measurements. The simulator's RF modeling capability includes the ability to add effects such as third order intercept, phase noise, frequency dependent VSWR effects and noise figures. HP Ptolemy also helps you model real-world effects in mixed analog, RF, and DSP systems, while accurately predicting performance.

Models
HP Ptolemy includes an extensive set of models for designing DSP algorithms and for behaviorally modeling the analog and RF distortions that occur to signals in real-world analog or RF signal paths. The model library includes over 500 models divided into three broad groups: DSP models, communications, and analog / RF models (see HP Ptolemy Models, page 20).

1. DSP model library includes floating-point building blocks that range from simple multipliers and adders to complex equalizers and FIR filters. You can combine these blocks quickly to explore and optimize DSP algorithms without having to write code. Add the HP Ptolemy Fixed-Point Analysis (E8822A/AN) module to extend these models to include fixed-point behavioral modeling.

2. Communications library includes a large number of blocks that make it easy to assemble a communications system and to stay focused on the section of the design you wish to investigate. The library includes items such as QAM modulators, demodulators, raised cosine filters, and a variety of other standard communications blocks.

3. Analog and RF models includes sophisticated modeling algorithms developed from HP's years of experience with analog and RF solutions. The library includes mixer models, RF amplifier models, and oscillator models. These models allow you to add a variety of real-world distortions to communications signals such as phase noise from oscillators, third-order intercepts, and nonlinear phase from IF filters.

With these sets, you can accurately model everything in the communications signal path whether the part is analog, RF or DSP based.

User-Defined Model Builder
HP Ptolemy provides an easy-to-use approach to adding custom models using C or C++. You add models by specifying the number of inputs, outputs, and parameters. The solution then builds the template that handles the details of interfacing automatically. You simply add your engineering C code in the template, hit a button to compile, and you're ready to use the model in the design.

After you have assembled a DSP design in block-diagram format, you can simulate and optimize the design using measures-of-performance such as bit error rate (BER), or by looking at eye diagrams or constellations.

Co-Simulation Between DSP, Analog and RF
By itself HP Ptolemy can simulate the DSP, analog, and RF at the behavioral level. However, you may want to move from a purely top-level behavioral simulation to a simulation with more realism.

With HP Ptolemy you can include a representation of a component, such as an amplifier, that has the actual transistors, capacitors, and other circuit-level parts, co-existing with all of the behavioral models. This co-simulation between HP Ptolemy and analog circuitry is possible through co-simulation architecture that is part of the HP Advanced Design System. On one schematic, in one user interface, you can build and co-simulate a system that includes a mix of digital and analog circuitry represented at both behavioral and circuit level. HP Ptolemy can co-simulate with RF System Simulator (E8853A/AN), Circuit Envelope (E8883A/AN) or High Frequency SPICE (E8884A/AN) for DSP system, analog circuit, and RF circuit capability.

Optimization
The HP Ptolemy module also includes an optimizer package with different algorithms for fine tuning system design parameters. The optimizer includes innovative genetic optimization techniques that can be applied to problems previously considered unsolvable by traditional optimization algorithms. The optimizer solution can also be used for things such as optimizing gains, coefficient values, or filter bandwidths to meet your set design goals such as BER (bit error rate) or adjacent channel power.

HP Ptolemy Models
HP Ptolemy has extensive models for developing DSP and communications system designs. There are three groups of models: numeric, timed, and synthesizable. The numeric models simulate DSP and digital algorithms and models useful for baseband designs. The timed models are behavioral analog and RF models incorporating accurate RF effects. These models are simulated with the HP Ptolemy simulator.

Numeric Models
The numeric models in the following libraries provide models to build DSP and digital designs at the base end.

- Numeric Communications: modems, convolutional coder, Viterbi decoder, phase shift, noise channel, raised cosine filter
- Numeric Control: bus merge, bus split, commutator, distributor, upsample, downsample fork
- Numeric Conversion: signal converters between different data types (float, integer, fixed, complex, timed)
- Numeric Logic: logic gates (AND, NAND, OR, XOR), registers, counters, latches
- Numeric Math: arithmetic functions, trigonometric functions, add, multiply, max, average, integrate, log, modulo
- Numeric Signal Processing: FIR, IIR filters, equalizer, FFT
- Numeric Sources: constant, ramp, Gaussian, uniform, waveform, rectangle
- Numeric Special Functions: quantizer, limiter, Schmitt trigger, table

Timed Models
The models in the following Timed libraries are for simulating analog and RF devices. They incorporate many RF phenomena, such as gain compression, S-parameters, noise figure, and intermodulation distortion, that are very important in communications.

- Timed Data Processing: binary coder, π/4 DQPSK decoder, IQ coder, QPSK decoder, symbol converter, symbol splitters
- Timed Filters: Bessel, Butterworth, Chebyshev, Elliptic, Gaussian, Raised Cosine
- Timed Linear: RF delay, phase shifter, splitter, integrate and dump
- Timed Modem: AM, DQPSK, FM, FMSK, MSK, PM, QAM, QPSK
- Timed Nonlinear: RF gain, mixer, RF multiplier, phase comparator
- Timed Source: impulse, N_tones, pulse, QAM, ramp, sinusoid

Additional Models
HP Ptolemy includes two additional models that allow designers to download simulation data to an arbitrary waveform generator, vector signal analyzer and logic analyzer. The link to the HP arbitrary waveform generator enables you to create, in DSP Designer, complex modulated signals that can be downloaded and recreated in analog form for use in actual hardware testing. A similar setup is available so that digital test vectors created in a simulation can be easily downloaded to a logic analyzer and used as a test source for DSP hardware. Finally, a link to the HP vector signal analyzer allows you to bring real-world samples of complex modulated digital signals back into DSP Designer for use as data sources in simulation. All of these measurement instrumentation links make it easier to translate from design to hardware implementation and test.

Standard HP Ptolemy RF Behavioral Modeling
HP Ptolemy includes RF models of mixers, amplifiers, noisy oscillators, etc. to model phase noise, third-order intercept, and frequency-dependent effects (S21 only).

Optional Modules for RF Modeling & Simulation
Many optional modules can be added to HP Ptolemy to supplement its analog/RF modeling and simulation capability at levels of abstraction from system level to circuit level. Optional modules include RF System Simulator* (E8853A/AN) and RF System Models (E8854A/AN), High-Frequency SPICE (E8884A/AN) and Circuit Envelope (E8883A/AN).

Optional RF Circuit Behavioral Modeling
Add the RF System Simulator and system models to model such detailed effects as intermodulation, noise figure, frequency-dependent effects (all S-parameters), harmonics, mixer spurious, and PLL transients.

Optional RF Device-Level Modeling
Add Circuit Envelope and High-Frequency SPICE modules to HP Ptolemy to enable detailed circuit-level modeling of RF and transient effects.

Circuit Envelope provides detailed analog/RF (baseband or modulated) analysis and simulation at the device level or with RF System Models.

High-Frequency SPICE provides detailed analog/RF device-level analysis and simulation for modeling secondary and subtle transient effects.

Configuration Detail
The HP Ptolemy Simulator requires the Design Environment (E8900A/AN).

*RF System Simulator analyzes RF system models and passive components. You must add a circuit simulator (e.g., Circuit Envelope or High-Frequency SPICE) to run simulations with semiconductor models. RF System Models (E8854A/AN) can also be used with Circuit Envelope, negating the need for RF System Simulator.

HP Ptolemy Fixed-Point Analysis (E8822A/AN)

HP Ptolemy includes a wide variety of DSP and communications models that provide powerful algorithm and modeling capability using floating-point math. However, many DSP designs are implemented using fixed-point math. This module adds fixed-point analysis and modeling capability to the HP Ptolemy models. With this module designers can model fixed-point math effects (up to 256 bits using twos complement or signed magnitude), bit-width effects (user-specifiable format), and quantization effects (rounding or truncations).

Configuration Detail
Requires HP Ptolemy Simulator (E8823A/AN) and the Design Environment (E8900A/AN).

RF System Simulator (E8853A/AN)

Features and Benefits

- Allows high-accuracy linear and nonlinear simulations of complete RF systems at the top level.
- Permits simulation of behavioral models and device-level models for improved system verification.
- Has built-in measurements for forward- and reverse-power gain, intercept point, noise, dynamic range, etc. to accommodate a wide range of design requirements.
- Has extensive model set of amplifiers, mixers, modulators, demodulators, phase-lock-loop components and switches, for design flexibility.
- Contains a unique RF system budget analysis that allows users to examine dozens of system measurements (TOI, 1dBc, power, gain, noise figure, etc.) at the system- or device-level for each component in the system regardless of circuit topology.
- Computes complete spectra including harmonics and intermodulation and mixer-spurious and noise for highest accuracy.

Overview
Engineers who develop complete systems of high-frequency components will find this simulator valuable. High-frequency circuitry poses a design challenge due to the wave nature of the signal. Interactions between the various parts of the system make it difficult to achieve desired cost and performance objectives. The technology built into this simulator helps to solve these problems.

The RF System Simulator provides the ability to model an RF system with accurate block-level models that can be replaced later with device-level models for further verification.

RF System Simulator is comprised of four simulation technologies: linear, Harmonic-Balance, Circuit Envelope, and RF system performance measurements. The linear simulator is identical to the E8881A/AN Linear Simulator but restricted to passive components and/or linearized system models of amplifiers and mixers. The nonlinear simulator adds the ability to analyze nonlinear system models as well as passive circuitry. This capability is identical to the E8882A/AN Harmonic Balance Simulator except semiconductor models cannot be used unless Harmonic Balance is also available. When digitally modulated spectra are needed, the Circuit Envelope simulator can be used.

(Please note that the RF System Simulator will not analyze simulations containing semiconductor models unless a license for the semiconductor models, as well as the appropriate circuit simulator license, are available).

A set of measurements tailored for RF system designers is also provided. These include:

- Forward and reverse gain
- Forward power and reflected power
- Intercept point and intermodulation levels, and gain compression
- Noise power, noise figure, and noise-equivalent bandwidth
- Power spectrum I & Q envelopes (if Circuit Envelope is included)
- Mixer spurious
  Spurious-free dynamic range, SNR, SINAD, and others
- S-parameter

A majority of these measurements can be applied to each node in the system as part of the budget simulation.

Because full bi-directional nonlinear simulations using general topology are performed, the highest possible accuracy can be achieved, including higher-order harmonics and intermodulation distortions. In addition, HP's Harmonic Balance and Circuit Envelope technologies reduce simulation time and memory usage to allow a large number of tones in system simulation.

Models
See RF System Model set (E8854A/AN) on page 33.

Configuration Detail
Requires the Design Environment module (E8900A/AN) and Data Display (E8901A/AN).

Other Simulation Solutions

HP Advanced Design System's circuit and system simulators are augmented by the electromagnetic simulation capabilities of:

- HP Momentum
- Standalone Momentum

These solutions are also augmented by the yield optimization capabilities of:

- Statistical Design

Momentum/Planar EM Simulator (E8921A/AN)

Features and Benefits

- Offers "edge mesh" for better characterizing the current-crowding behavior of high frequency signals.
- Uses adaptive frequency sampling (AFS) to give the highest frequency sweep resolution for a minimal number of actual solved frequencies.
- Has sidewalls (waveguide mode) to simulate the effects of placing a circuit near a package sidewall.
- Incorporates box resonance mode to model package effects and to find if box resonances occur in the frequency range of interest.
- DC operating point included with S-parameters for circuit simulation that needs bias flowing to an active device through the S-parameters from HP Momentum.
- Simulates smaller circuits, with close interactions, up to 4 times faster.

Overview
HP Momentum helps take the uncertainty out of physical design by performing accurate electromagnetic analysis directly from the layout of HP Advanced Design System. It is designed to analyze multilayer planar geometries and provide results in the form of S-parameters. You can then use these results directly in HP's circuit simulators including Harmonic Balance, Convolution, and Circuit Envelope. With the use of the optional SPICE Model Generator (E8891A), S-parameters can be used to produce a SPICE-equivalent circuit in formats that are compatible with several industry versions of SPICE.

The HP Momentum simulator is based on the method-of-moments technology that is particularly efficient at analyzing planar conductor and resistor geometries. Planar structures on different dielectric layers can be connected together with vias. Slots can be drawn on ground planes and their interactions efficiently solved, because only the slots are meshed, not the ground plane.

Since HP Momentum is part of HP Advanced Design System, it is now available on the PC under Windows NT and Windows 95.

Configuration Detail
Requires the Design Environment (E8900A/AN), Data Display (E8901A/AN), and Layout (E8902A/AN).

Standalone Momentum (E8920A)

Features and Benefits

- Provides capabilities of Momentum for designers who do not need other HP Advanced Design System solutions.

Overview
If you are looking for the capabilities of Momentum (E8921A) but do not need to integrate with other HP Advanced Design System solutions, then Standalone Momentum is the simulator you should use. Standalone Momentum gives the same electromagnetic simulation capabilities as the integrated version, but provides layout and a non-expandable version of Project Design Environment and Data Display. Non-expandable means that the circuit simulators and other design solutions of HP Advanced Design System are not available for this product. This dedicated solution will provide S-parameters in either the Touchstone file format or the HP CITIfile format, for use with other simulators.

Statistical Design (E8824A/AN)

Features & Benefits

- Analyzes and optimizes manufacturing yield prior to production.
- Determines Red-X components that need to be controlled for higher production yield.
- Enables designers to compensate for unavoidable component variations.
- Provides the capability and accuracy of traditional Monte Carlo analysis in a fraction of the time normally required.
- Allows post-production tuning to analyze and predict production yields for designs that employ tunable elements.
- Offers a data display feature that allows yield and sensitivity determination at a glance.

Overview
The Statistical Design Package provides a solution for designers faced with the need to design products for high-volume production. For low-volume production, this product ensures product reliability. The solutions in this package include Yield Analysis, Yield Optimization, Design Centering, and many others that allow you to go beyond standard yield analysis.

The Statistical Design Package uses the Monte Carlo method to predict yield by simulating a product's manufacturing process where the units produced have randomly-varying component values (e.g., amplifiers, mixers). This helps you understand which components in your design require tighter control than others. A component's pass/fail status is determined by comparing your design's simulated performance to your design's actual requirement. The yield is then defined as the percentage of units passed.

A yield optimization feature automatically adjusts nominal component values to increase predicted manufacturing yield. This feature can be applied to both linear and nonlinear circuits and systems. It employs a technique called design centering, where the end result is a design that is able to tolerate unavoidable component variations due to manufacturing, environmental, and modeling errors.

Compact statistical sensitivity data is displayed on histograms to help you determine the Red-X components. Sensitivity displays also allow component tolerance assignment and nominal component value adjustment for increased yield.

Tolerance assignments and distribution are available to the component parameters through device library information or in the form of normal (Gaussian), uniform, or arbitrary user-defined distribution (e.g., a bimodal distribution).

Configuration Detail
Requires the Design Environment (E8900A/AN) and any simulator.

Performance Optimization

Performance optimization lets you specify a range of device or component values and then automatically compute the nominal values that best meet your performance specifications. All HP Advanced Design System simulators come with a family of performance optimizers that can be applied to different problems. The optimizers are grouped into three distinct categories: continuous-value, continuous- and/or discrete- value, and discrete-value.

Continuous-value optimizers

- Gradient
- Gradient Min/Max
- Quasi-Newton
- Least P
- Min/Max

Continuous- and/or discrete-value optimizers

- Random
- Random Min/Max
- Random Max
- Genetic

Discrete-value optimizer

- Discrete Value

DSP Synthesis Products

HP DSP Synthesis

HP DSP Synthesis technology includes models, code generators, simulators, and a comparator — driven by a powerful synthesis engine. Modules within this family include:

- Synthesis Engine
- VHDL Models & Code Generation
- Verilog Models and Code Generation
- Adaptive Waveform Comparator
- PC VHDL Simulator
- PC Verilog Simulator
- PC Verilog &VHDL Simulators
- UNIX VHDL Simulator
- UNIX Verilog Simulator
- UNIX Verilog & VHDL Simulators

Synthesis Engine (E8836A/AN)

Features and Benefits

- Provides estimation, scheduling, binding, and RTL schematic generation to optimize high-level designs.
- Provides a summary of non-inferior design space from which you can select resource and performance combinations.
- Identifies components most frequently used and their limitations for bottleneck analysis.
- Automatically schedules the order of operations in the design to minimize execution time.

Overview
The synthesis engine of DSP Synthesis performs several major tasks in the transition from system-level block diagram to Register Transfer Level (RTL) hardware description language. These tasks include estimation, scheduling, binding, and RTL schematic generation. The objective for the Synthesis Engine is to optimize the high-level design (using resource sharing, pipelining and other techniques) developed in DSP Designer according to your constraints. The output is an RTL description of the design in Verilog or VHDL. The scheduling and binding algorithms are simple to use and require minimal user interaction, unless you wish to specify a partial design as a starting point.

Estimation Capability
Estimation is used prior to synthesis and helps eliminate inferior design choices while reducing design times. The estimation engine provides you with a first-cut look at the chip area and performance.

The estimation capability enables you to make an informed decision on the expected area-performance metrics of the final design without going through the exhaustive and computationally expensive process of generating the actual designs. Estimation solutions provide answers to the following two fundamental questions:

- If I use this many components in the design, what will the performance be?
- If I want the design to achieve this much performance, what is the minimum number of components required?

The estimation engine uses the behavioral specification, clock cycle, and component delays to estimate a design space containing non-inferior designs that span a large spectrum of choices, from slow and inexpensive designs to fast and expensive designs. Using the design space as a guide, you can select those designs of interest and send them through the full synthesis process.

Design Constraints and Specification Entry
In order to provide more guidance in the setting of design constraints, DSP Synthesis provides a series of tabbed dialogs that you step through to specify various design constraints. These tabbed dialogs include a spreadsheet specification entry dialog for tabular data, a dialog for library selection, and a dialog for design style selection. Moreover, DSP Synthesis integrates the design constraint entry with the estimation solution, further assisting you in determining the design constraints.

Unlike other tools, DSP Synthesis enables designers to easily keep track of which constraints produce which designs. This helps in the refinement of hardware designs.

Area Estimation
The area estimator considers the impact of components, registers, multiplexers, wiring, memory, I/O pads and unused components. Because register and multiplexer areas are not known to vary significantly with design, their impact on performance is not significant. Thus, one pass through the complete design phase can provide the register and multiplexer estimates. Memory area may be estimated, assuming arrays in the specification are stored in memory. The number of I/O pads are estimated by the performance required, and then rounded-up to the best packaging available.

Performance Estimation
There are two main performance metrics used in design synthesis: latency and throughput. Latency is the total time taken to execute the algorithm on one set of input data. Throughput is the number of solutions produced by the algorithm every unit time. (This is identical to saying that throughput is the number of input data sets consumed per unit time.)

Latency is the premier metric used in non-pipelined design, which is preferred when the input data does not arrive very fast or arrives at irregular intervals. On the other hand, if the input data arrives rapidly and at regular intervals, as in most DSP designs, pipelined design style is preferred and the performance is then judged by the throughput of the design.

Pipelined vs. Non-pipelined
The Synthesis Engine treats pipelined and non-pipelined designs separately. The non-pipelined design space consists of average execution time and number of major resources, while the pipelined design space consists of expected throughput and number of major resources. The quantity of major components and their impact on throughput (in the case of pipelined design) and average execution times (for non-pipelined design) will be estimated.

Design Space Exploration
After estimation is run, the Synthesis Engine provides a spreadsheet/tabular summary of the superior design space. This table displays the estimated number of resources (both overall total and number of each resource type) and estimated performance (throughput for pipelined and latency for non-pipelined) for various design implementations. From this table, you select which resource and performance combination(s) the Synthesis Engine should pursue.

Instead of requiring you to select a single candidate resource/performance combination, perform the synthesis process, and then select another candidate resource/performance combination and re-start the synthesis process, DSP Synthesis provides you with the ability to select more than one combination, queue the various design constraints, and automatically direct the synthesis engine through each design constraint combination.

Additionally, DSP Synthesis will, through a tabular summary, indicate the estimated resource-usage profile to help identify resource bottlenecks (high-utilization vs. low-utilization) and make appropriate implementation decisions.

Bottleneck Analysis
Through a bottleneck analysis, you can gain important insight into a design. For example, you can identify which components are used most and determine the heavily-utilized components limiting the performance. You can also determine the under-utilized components in a design. If cost is an important factor, some of these under-utilized elements can be shared to reclaim area. Through this unique capability, the final design can be refined beyond the standard synthesis capabilities.

Scheduling Capability
Once the estimation is run and the results are presented, you can choose one of the designs to synthesize. The Synthesis Engine then performs scheduling on the selected design. The purpose of scheduling is to order the operations in the design to minimize the execution time of the entire design. The following features can be performed with the scheduling capability of DSP Synthesis:

- Schedule basic blocks: schedules sequence of instructions
- Pipeline loops
- Schedule non-pipelined blocks
- Schedule pipelined specifications and loops

Binding Capability
After the schedule is determined for a design, hardware resources are assigned to handle the operations in the design. This binding process offers you the following features:

- Allows complex sharing of components
- Generates steering logic automatically
- Handles partial designs to allow flexibility in synthesis
- Permits trade-offs between components and interconnect areas
- Minimizes area
- Generates data path and control path

The binding task is identical for both pipelined and non-pipelined designs. In addition to binding resources, the Synthesis Engine also produces the control signals. The algorithm is very flexible in that several different objectives can be used, such as minimizing interconnect area, maximizing testability of the design, and minimizing the area subject to meeting clock-cycle requirements.

You can also specify a fixed number of registers, in which case this number overrides minimizing the register count. You may wish to specify a partial design as the input, thus imparting your experience to the design process. Multifunction components can also be handled properly. For example, an 8-bit additional instruction can be executed on a 12-bit or an 8-bit adder and the binding algorithm determines the better choice. In addition, when you specify extra resources, such as registers, the Synthesis Engine considers the tradeoff between these extra resources and the wiring and steering logic area.

Schematic Generation
The Synthesis Engine generates schematic representations of the structural implementation designs. These schematics show you the optimized result of the scheduling and binding.

User Interface
Because DSP Synthesis is integrated with the rest of the HP Advanced Design System solutions, the same graphical user interface guides you through the entire synthesis process. This includes navigating the following design steps:

- Selection of the behavioral schematic parts to be synthesized
- Designation of design constraints/specifications
- Choice of vendor libraries
- Usage of estimation techniques for reducing the design space
- Scheduling and binding
- Viewing of synthesized results
- Management of the numerous synthesized implementations
- Generation of HDLs (Verilog and VHDL)
- HDL simulation interface
- Verification using HDL
- Comparison of adaptive waveform

Configuration Details
Requires VHDL Models and Code Generation (E8834A/AN) or Verilog models and Code Generation (E8835A/AN), HP Ptolemy Fixed-Point Analysis (E8822A/AN), HP Ptolemy Simulator (E8823A/AN), and the Design Environment (E8900A/AN).

VHDL Models and Code Generation (E8834A/AN)

Features and Benefits

- Provides models for use with Synthesis Engine and HP Ptolemy.
- Generates VHDL code.

Overview
The VHDL models are included in the Synthesizable DSP library. Each of the models in this library comes with a VHDL description. These models can be used to develop a design that can be used with the Synthesis Engine and code generation. These models can also be simulated with HP Ptolemy. The models include barrel shifters, adders, multipliers, counters, logic gates, and registers.

Generation of an RTL design description is the vehicle by which designs are exported to ASIC vendors or to FPGA solutions for implementation. The design starts at a high level of abstraction (behavioral level) and transformations proceed until the design is instantiated in terms of parameterized modules or architecture-specific primitives or macros. At this level, the design is expressed as an RTL description and it is suitable for logic synthesis or for place and route. RTL code generator is part of the HDL code generator, which performs the following operations:

- Construct a correct and simulatable VHDL description
- Generate the VHDL test vectors for HDL simulation. This also includes collecting output test vectors for waveform comparison

Configuration Detail
Requires HP Ptolemy Fixed-Point Analysis (E8822A/AN), HP Ptolemy Simulator (E8823A/AN), and the Design Environment (E8900A/AN).

Verilog Models and Code Generation (E8835A/AN)

Features and Benefits

- Provides models for use with Synthesis Engine and HP Ptolemy.
- Generates Verilog code.

Overview
The Verilog models are included in the Synthesizable DSP library. Each of the models in this library comes with a Verilog description. These models can be used to develop a design that can be used with the Synthe-sis Engine and code generation. These models can also be simulated with HP Ptolemy. The models include barrel shifters, adders, multipliers, counters, logic gates, and registers.

Generation of an RTL design description is the vehicle by which synthesized designs are exported to ASIC vendors or FPGA solutions for implementation. The design will start at a high level of abstraction (behavioral level) and transformations will proceed until the design is instantiated in terms of parameterized modules or architecture-specific primitives or macros. At this level, the design is expressed as an RTL description and it is suitable for logic synthesis or for place and route. RTL code generation is part of the HDL code generator which also performs the following operations:

- Construct a correct and simulatable Verilog description
- Generate Verilog test vectors for HDL simulation. This also includes collecting output test vectors for waveform comparison

Configuration Detail
Requires HP Ptolemy Fixed-Point Analysis (E8822A/AN), HP Ptolemy Simulator (E8823A/AN), and the Design Environment (E8900A/AN).

Adaptive Waveform Comparator (E8833A/AN)

Features and Benefits

- Accepts input from DSP Designer and HDL simulations for comparison.
- Processes two waveforms to determine closeness of fit in the area of interest (user-defined time range or time delta from a trigger point).
- Generates a status report indicating the mismatch points and the overall degree of fit between the waveforms.
- Displays a graphical comparison between two waveforms.

Overview
The Adaptive Waveform Comparator provides a design verification step for the transition between a system-level design and RTL Hardware Description Language implementation.

Design verification is the process of comparing the results of DSP Designer with the results produced by third-party HDL simulators on the generated HDL code. In the HDL code generation phase, the test bench from the user interface is automatically translated to an equivalent HDL counterpart so a comparable set of test vectors is used.

Adaptive Waveform Comparator Engine
Due to variations in set-up time, different simulators may produce waveforms that are not exact replicas of each other. These waveforms are nevertheless functionally equivalent at the points of interest. Since the waveforms are not exact duplicates of each other, a simple text-based diff provides little help with performance verification. The Adaptive Waveform Comparator enables you to compare the functional equivalence of these two waveforms.

The Adaptive Waveform Comparator compares two waveforms at the points of interest, by aligning the two waveforms so their variations due to latency, component delays, and other factors can be handled automatically. The Adaptive Waveform Comparator can also be used in this way to compare the simulation results from DSP Designer and VHDL or Verilog simulations.

Display the Comparison Result
The Adaptive Waveform Comparator sends the comparison result to the Design Environment and displays the results in two digital waveforms, stacked one on top of the other. The resulting waveforms are generated and aligned.

Configuration Detail
Requires Data Display (E8901A/AN).

HDL Simulator*

The DSP Synthesis suite includes a HDL simulator for either Verilog or VHDL. This simulator can be invoked from within the Design Environment. The RTL HDL file generated from the Synthesis Engine can be verified through HDL simulation against the original behavioral simulation.

The VHDL simulator uses the VHDL description and test benches created during VHDL generation. Invocation, compilation, and simulation is automatically accomplished and the VHDL output vectors are collected for display or use with the adaptive waveform comparison.

*No part number (not sold separately).

Digital Filter (E8825A/AN)

Features and Benefits

- Creates filter coefficients for IIR and FIR in either fixed-point or floating-point formats.
- Enables design of Low-Pass, High-Pass, Bandpass, Bandstop, Multipass, Multistop, Differentiator, Hilbert transformer, Raised Cosine, Raised-Root Cosine Filters.
- Automatically builds fixed- or floating-point versions of the designed filter in the schematic, for easy use in system simulations and silicon implementation.
- FIR filter-coefficient design methods include Equiripple, Least Squares, and windowing.
- IIR filter-coefficient design methods include Chebychev I, Chebychev II, Eliptic, Butterworth, and auto select.
- Filter order can be user-specified or automatically calculator-based on filter specifications.
- Includes optimizer-weighting function to control filter design goals

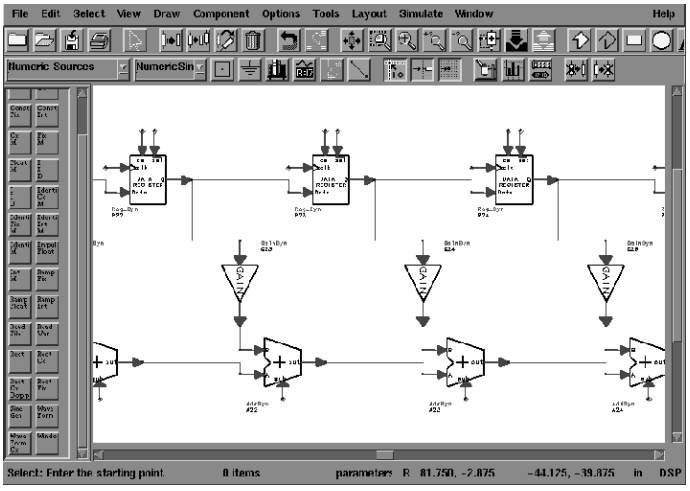
Overview
Because digital filters are one of the most common DSP circuits used, you need an efficient way to design, analyze and create schematics for them. HP's Digital Filter module works tightly with HP Ptolemy (E8823A/AN) to allow you to go easily from filter specification to synthesizable schematic implementation.

Digital Filter allows you to create FIR and IIR filters by simply entering frequency and amplitude specifications. Digital Filter then designs the coefficients and allows you to analyze the filter in terms of frequency response, phase response, and impulse response. Digital Filter also allows you to compare floating-point and fixed-point filter performance for a specified bit width.

Schematic Generation
After the filter coefficients have been designed and refined, you can automatically create schematic implementations of the filter in HP Ptolemy. Simply select what form of the filter you wish to implement (cascaded second order, Direct form II, etc.) and Digital Filter builds up the schematic representation with fixed- or floating-point models and loads in the proper coefficient values. This can be helpful with time-consuming problems such as a 128 tap FIR filter.

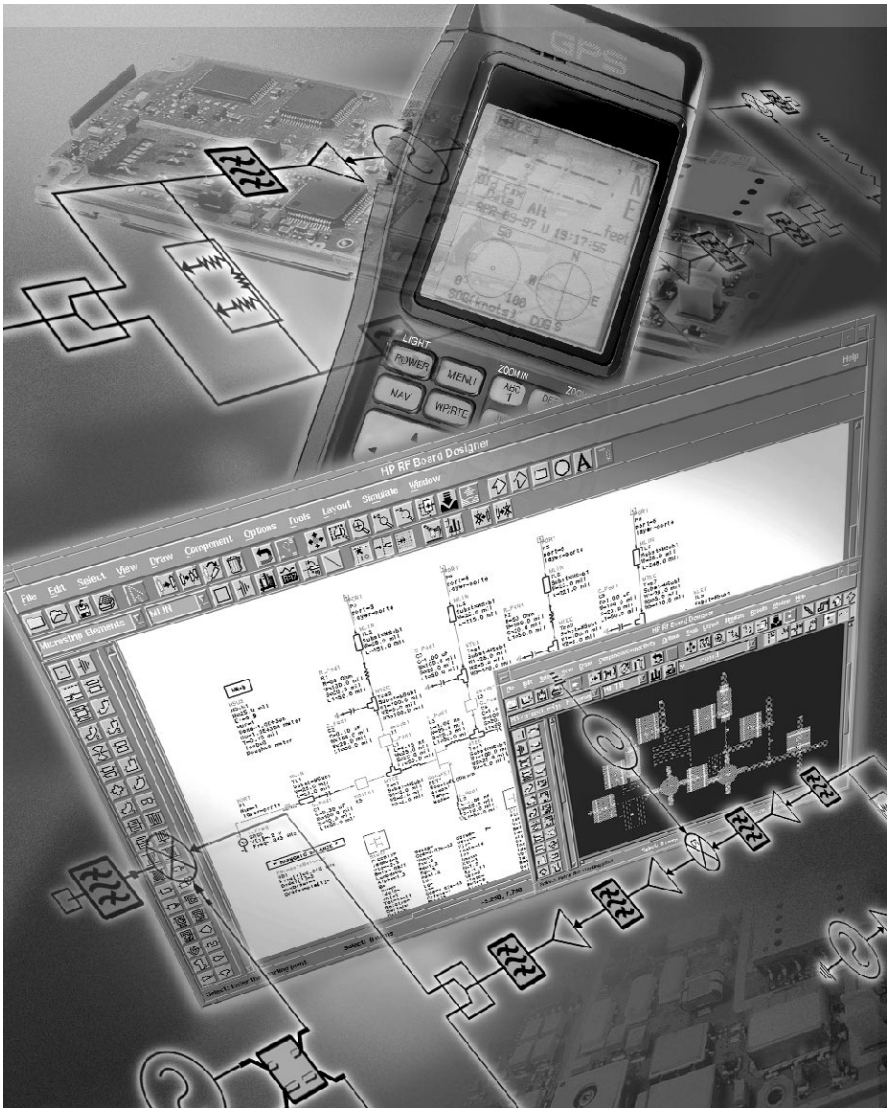
In summary, HP's Digital Filter module works with HP Ptolemy to provide a quick and easy flow from filter specification to schematic design implementation and/or to silicon implementation (with DSP Synthesis).

Configuration Detail
Requires Design Environment (E8900A/AN).



Digital Filter builds this schematic for you automatically.

Model Sets and Vendor Component Libraries



Model Sets

HP Advanced Design System incorporates models that permit you to simulate a wide variety of both DSP and analog circuitry. The model sets offered are:

- RF Passive Circuit Models
- Multilayer Interconnect Models
- HP Ptolemy Matrix Models
- RF System Models
- Antenna and Propagation Models
- Analog Model Development Kit
- SPICE Model Generator

RF Passive Circuit Models (E8950A/AN)

Features and Benefits

- Provides a wide assortment of common RF part models for board-level design.

Overview
This module provides models for many common RF parts. When combined with other circuit models, users are able to better analyze a board-level design. The models provided are:

- Air-core inductors
- Tapped air-core inductors
- Balun transformers
- Toroidal ferrite-core inductors
- Broadband n2:1 Guanella transformers with ferrite
- Ruthroff 4:1 ferrite/transmission line transformer
- Ferrite 0 degree and 180 degree ferrite hybrid combiner
- Wireline and Wirepac 90 degree reentrant couplers
- Ideal 90 degree and 180 degree hybrid couplers
- Chip capacitors
- Piezoelectric crystals with holder
- Transmission line transformers
- Multiple coupled resistive coils
- Resistive pads

Configuration Detail
Requires the Linear Simulator module (E8881A/AN) and the Design Environment (E8900A/AN).

Multilayer Interconnect Models (E8951A/AN)

Features and Benefits

- Allows definition of multilayer structures for PCB, MCM, or IC package analysis.
- Allows simulations from schematics as opposed to EM analysis of layouts.
- Allows definition of complex structures beyond microstrip or stripline configuration.

Overview
This module provides models for multiple coupled lines used in multilayer structures such as printed circuit boards, multichip devices, and IC packages. These models allow for better analysis of anticipated layout effects, without requiring the HP Momentum Planar EM simulator. There is a resultant trade-off in simulation speed vs. accuracy. The effects of impedance, loss, crosstalk, and delay are modeled with the underlying 2-D electromagnetic field solver used by these models. The advantages of the Multilayer Interconnect Models over microstrip and stripline models are that a greater number of coupled line models are available, models can be placed on any specific layer, and you do not need to specify microstrip or stripline operation because it is computed automatically.

These models are also a superset of the printed circuit board models included in the Linear Simulator module. Key advantages over these models are easier parameter entry, more available model configurations, and the ability to have models on multiple layers. With the flexible multilayer substrate definition, you choose how many layers the substrate will have and the parameters that describe a vertical cross-section of the multilayer structure.

The models available in the Multilayer Interconnect Models include:

- Multiple coupled lines (1 to 10) with variable widths and spacing
- Multiple coupled lines (1 to 16) with constant width, spacing, and layer
- Multiple coupled corners of arbitrary angle (1 to 16) with constant width and spacing
- Multiple coupled corners (1 to 16) with variable pitch, constant width and spacing
- Multiple coupled slanted lines (1 to 16)
- Multiple coupled crossovers (1 to 8)
- Multiple coupled radial lines (1 to 5)
- Discontinuities such as gap, open stub, cross, tee, and vias
- Multiple layer (2 to 16) substrate definition (metal and dielectric properties)

Configuration Detail
Requires the Linear Simulator module (E8881A/AN) and the Design Environment (E8900A/AN).

HP Ptolemy Matrix Models (E8826A/AN)

Features and Benefits

- Provides over 50 matrix math functions for both fixed- and floating-point numeric data.
- Provides co-simulation link to MATLAB.

Overview
This module adds matrix processing capability to the HP Ptolemy Simulator. The Matrix Model library includes everything from simple matrix math routines, such as matrix adders and multipliers, to more complex routines, such as matrix inversions and matrix singular-value decomposition. With this module, system-level designs can pass and manipulate matrix data in the same manner that scalar values can be manipulated in HP Ptolemy. The model set also enables use of MATLAB scripts in the HP Ptolemy environment (co-simulation). Matrix math capability makes construction of sophisticated DSP algorithms very efficient and simple.

Configuration Detail
Requires the HP Ptolemy Simulator (E8823A/AN) and the Design Environment (E8900A/AN).

RF System Models (E8854A/AN)

Features and Benefits

- Contains complete set of block-level RF models and measurements, which allow fast, accurate modeling of RF Systems.
- Offers compatibility with RF System Simulator and other simulators.

Overview
This module provides RF system models that allow system-level analysis. Circuit- and system-level models can be combined for analysis. The following models are provided:

- Gain blocks (nonlinear, bi-directional, seven different nonlinearity specifications)
- Mixer (intermodulation table, seven different nonlinearities, LO and RF feedthrough, noise)
- Filter library (Butterworth, Chebyshev, Elliptic, Bessel, Gaussian, Nyquist, Low-Pass Filter, Band-Pass Filter, Band-Stop Filter, High-Pass Filter)
- Modulators & Demodulators (AM, FM, PM, QPSK, π/4 DQPSK, IQ and arbitrary N-state modulators)
- Phase-lock loop components (VCO with phase noise, divide by N, frequency phase detector)
- Switch and algorithmic components (SPDT, DPDT, integrator, differentiator, sample and hold, sample quantizer, serial-parallel converters, etc.)
- Linear and nonlinear data file models (.S2P, .S2D, .P2D)
- Passive elements (isolator, phase shifter, couplers, radio-link models, splitters, and attenuators)

Configuration Detail
Requires the Linear Simulator (E8881A/AN) or the RF System Simulator (E8853A/AN), and the Design Environment (E8900A/AN).

Antenna and Propagation Models (E8856A/AN)

Features and Benefits

- Provides models of signal propagation effects for system-level analysis of mobile communication products.
- Offers verification environment that is in compliance with major cellular standards.
- Permits modeling of loss, complex multipath, and fading effects for design flexibility.

Overview
This module helps designers of mobile communication products examine how the dynamic radio-signal propagation channel affects the performance of the system. The models provided are compliant with the following cellular industry standards: GSM (all scenarios), IS-97 CDMA, and IS-54 TDMA.

Each model has an option for urban, suburban, and rural path-loss prediction. The models are based on a statistical treatment of electromagnetic equations governing radio wave propagation. The models give you the capability to evaluate the entire link (transmitter/channel/receiver) of many wireless systems. Also included are base-station and mobile-station antenna models. These antenna models accept information on location, elevation, vehicle speed, and direction.

When used in a simulation, the radio propagation between two or more antennas is modeled in a statistical manner to produce multipath effects with Rayleigh and Rician probability distributions. Simulations involving multiple propagation channels, such as adjacent channel interference tests or diversity systems, can also be effectively modeled.

Configuration Detail
Requires the HP Ptolemy Simulator (E8823A/AN) and the Design Environment (E8900A/AN).

Analog Model Development Kit (E8890A/AN)

Features and Benefits

- Improved and user-friendly ANSI-C allows creation and compiling of custom C-code circuit models, resulting in faster simulation time.

Overview
This kit allows you to create your own circuit and system element models, compile them, and link them into HP Advanced Design System. Written in ANSI-C code, these elements can be used in linear, nonlinear, circuit envelope, transient, and convolution circuit simulations. Models can now be created by simply specifying the symbol (which defines the number of ports) and parameters. The interface then automatically builds the C and schematic interface code (AEL) necessary to incorporate your model into the Design Environ-ment. You simply add your engineering C code in the template, hit a button to compile, and you're ready to use the model
in your design. The interface also supports Series IV Senior nonlinear models with little or no modification.

Configuration Detail
Requires the Linear Simulator (E8881A/AN) or the RF System Simulator (E8853A/AN), and the Design Environment (E8900A/AN).

SPICE Model Generator (E8891A/AN)

Features and Benefits

- Enables the generation of SPICE models from S-parameter data to speed work flow.
- Develops models from four different topologies for design flexibility.
- Allows full chip verification on SPICE after having performed the RF design.

Overview
The SPICE Model Generator lets you convert a frequency-domain S-parameter characterization into a model that SPICE can use. The S-parameters can come from the HP Advanced Design System frequency-domain simulator, High-Frequency Structure Simulator, Momentum, or network-analyzer measurement. This model generator develops a netlist containing a subnetwork representing the modeled structure.

The SPICE Model Generator develops models using four different topologies:

- Ideal transmission line topology
- N-section ladder network
- Lumped Pi topology
- Rational polynomial representation (HSpice or ApSim Spice formats)

The first three models are low-frequency extraction from S-parameter data. The fourth model uses curve fitting to frequency data. The first three models are applied when the frequency data points in the S-parameter data file are free of noise. If the S-parameter data is taken from a network analyzer, noise may be present in the low frequencies and the rational polynomial representation should be applied.

The SPICE model generator also allows for full-chip verification in the SPICE simulator after you've done the RF design in HP Advanced Design System.

Configuration Detail
Requires the Design Environment (E8900A/AN).

Vendor Libraries

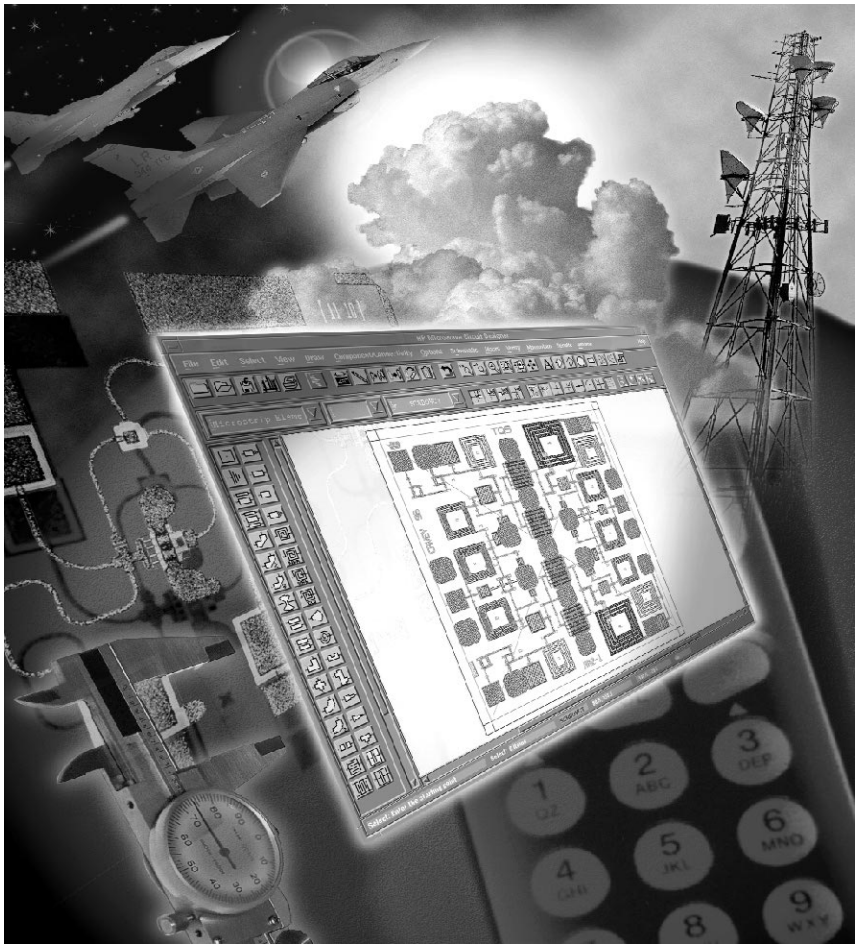
Part of the power of HP Advanced Design System lies in its extensive active- and passive-device model libraries. Palettes of model data for over 90,000 popular devices from numerous vendors are available to place in your design. A wide range of SMT capacitors, inductors, and resistors are available. The system's active device libraries contain measurement-based, bias-dependent transistor models that are backed by years of verification and experience. The SMTs contain physical layout information as well as electrical data.

The following part/vendor part libraries are available in the HP Advanced Design System:

- E8952A Microwave Transistor Library (chip FETs and BJTs, and HEMTs)
- E8953A RF Transistor Library (packaged BJTs and FETs, and MOSFETs)
- E8954A High-Frequency Diode Library (PN and Schottky)
- E8955A Analog Parts Library (diodes, N and P channel JFETs, MOSFETs, and BJTs)
- E8956A RF Passive SMT Library (resistors, inductors, capacitors)
- E8957A Murata SMT Capacitor and Inductor Library (measurement-based GRH & GRM series)

Our extensive BJT, FET, and MOSFET device libraries come complete with package layout information for each device so there is no need to create the layouts manually. Also, surface mount technology (SMT) libraries of resistors, inductors, and capacitors have both electrical and layout information.

Physical Design Products



HP Advanced Design System provides a variety of solutions to help you produce and test a physical layout of your designs. These solutions include a graphical editor, a design rule checker, translators, and a graphical cell compiler.

Layout (E8902A/AN)

Features and Benefits

- Provides ability to build and simulate circuits directly in the layout.
- Has wide range of output formats for layouts and schematics.
- Integrates with mask-making equipment.
- Provides extensive editing features for design flexibility.

Overview

The Layout module is a powerful graphical editor that allows interactive physical design and simulation of PCB, RFIC, MIC or MMIC layouts. Layout can be used with optional solutions that specifically address the problems of high-frequency designs, help reduce errors, and finish designs faster.

Optional modules that can be added to Layout include:

- Momentum Planar Electromagnetic Simulator for performance verification
- Design Rule Checker used in testing for layout errors
- Translators such as DXF, IGES, GDSII and Gerber
- Graphical Cell Compiler for adding custom parameterized layout AEL macros

Like the schematic editor, the Layout editor lets you select components for placement from a graphical palette of simulation models. You select a true-to-scale "ghosted" image of the component, select the proper orientation, and place it in your design.

When you are ready to update the schematic, you can do so interactively or automatically. In the interactive mode, you pick a component in the layout and drag its symbol into position in the schematic. This gives you precise control over the schematic. Changes made in either representation are tracked by the Design Synchronization Engine (DSE), which is at the heart of the system. This insures that your simulations represent your latest changes, and thus increase accuracy. The DSE gives you the flexibility to choose how layout components are depicted in the schematic. For instance, you can simulate a meandering trace as an ideal electrical connection if it is part of your bias network, or simulate every discontinuity along the trace for greater accuracy at higher frequencies.

An important feature of the Layout editor is simulation of Layout, which gives you the ability to build and simulate the circuit directly in the layout. You can intermix circuits that are represented in either schematic or layout; for instance, a complicated meander line may be easier to draw in the layout than in the schematic. You have the flexibility to design in whichever representation is necessary or more intuitive.

Layout Editor Features

- Work where it's most natural: generate layouts from schematics or schematics from layouts
- Cross-probe your circuit to check the schematic-layout match
- Simulate layouts directly
- Freeze item positions in schematic or layout
- Place or delete items in your schematic and layout simultaneously
- Check nodal mismatches between schematic and layout
- Reference designators (e.g., R1, TL2) automatically generated on silk-screen layers
- Check for wires or unconnected pins in layout
- Create or flatten hierarchy with one command
- Break traces or add tees to traces in one step
- Traces can be converted to equivalent circuits, shorts, or transmission lines
- Trace corners can be rounded, chamfered, or square
- Step and repeat; rotate, scale, and mirror
- Insert, move, copy, stretch, delete, unlimited undo
- Process offsets correct for under- or over-etching
- Attach or edit properties of objects
- Snap to pins, grid, or vertices plus new snapping modes: edge, circle center, intersection, and line center
- Unlimited number of layers; dozens of colors and fill patterns
- All-angles or orthogonal entry
- Simulation expressions can be utilized in layout
- Logical equivalent pins
- Correct interlayer connections are enforced
- Improved user interface
- Enhanced logical operators: merge, subtract, or, xor
- Ground-plane management

Layout Basic (E8944A/AN)

Please see page 8 for a description of this reduced-capability module.

Layout Basic is a non-expandable version of layout. It can be added to HP RF Designer (E8940A).

Artwork Translators
Many output formats are available from Layout that link to other design solutions.

Integration with mask-making equipment is made possible with the GDSII Stream File interface. Integration with mechanical CAD systems is made possible with the IGES interface, or the popular DXF translator for AutoCad(TM). The Gerber translator is widely used in the production of PC boards. Thus, your designs can be connected to almost any other popular CAD system on the market.

The following translators are available:

Bi-directional translators:

- GDSII Translator (E8904A/AN)
- IGES Translator (E8903A/AN)
- EGS Generate/Archive (built in, no purchase necessary)

Output-only translators:

- DXF and Gerber Translator (E8906A/AN)

New Gerber Features
The Gerber Translator has been updated to be compliant with the extended Gerber RS274X standard. This new standard format includes:

- Embedded format, unit and data information
- Embedded apertures
- Custom aperture definitions
- Film control statements
- Multiple layers embedded in a single file
- Special polygon definitions

Additionally, the Gerber translator has been enhanced with the following features:

- More layer control — select layers to translate without modifying the mask resource file
- A layer dialog box has been added where layers can be turned on/off
- Better Gerber file naming — mask layer name (and optionally mask layer numbers) are used to identify layers
- Gerber file merging — a film merge menu enables the user to create a new Gerber file which is a combination of mask layers
- Automatic Hole/Empty support and embedded aperture table using Gerber Standard RS 274X

Configuration Detail
Layout requires the Design Environment module (E8900A/AN). All Artwork Translators (GDSII, IGES, DXF & Gerber) require the Layout module (E8902A/AN).

Design Rule Checker (E8907A/AN)

Features and Benefits

- Verifies PC board, hybrid, RFIC or MMIC layouts.
- Checks against user provided rules.
- Identifies the error type, magnifies that portion of the layout, and highlights the specific segments that break the design rule.

Overview
HP Design Rule Checker is integrated in HP Advanced Design System. It is used to verify PC board, hybrid, RFIC or MMIC layouts generated by the system's layout so you can catch critical drawing or design errors before your circuit board or mask is fabricated. For example, if two traces are placed too closely together on a mask, or if a trace width falls below a specified tolerance, HP Design Rule Checker will identify and highlight the error.

Flexible Rule Writing
Designs are checked against a set of rules provided by the user. All design verification rules files are written in the system's database language of AEL. You can easily write rules for checking polygon spacings, widths, and grid alignment. You can write more complicated rules to check FET gate orientation, air bridge post separations, etc. Once created, rules files can be saved and reused for other designs.

Fast and Easy Operation
In addition to the ability to write customized rules, HP Design Rule Checker has a fast, automated mode that prompts for simple spacing and width rules without requiring you to write AEL code. For more complicated rules, the User Interface focuses on ease of use, with the design rules entered in an easy-to-understand process flow.

Since both HP Design Rule Checker and Layout operate within the same environment, designs can be drawn, checked, and edited all with the same software.

When errors are encountered, HP Design Rule Checker automatically identifies the error type, magnifies that portion of the layout, and highlights the specific polygon segments that break the design rule. Users can easily sequence through errors with the mouse, either editing or ignoring reported errors. Error files can also be saved and restored.

Configuration Detail
Requires the Design Environment module (E8900A/AN) and the Layout module (E8902A/AN).

Graphical Cell Compiler (E8908A/AN)

Features and Benefits

- Simplifies adding parameterized artwork to schematics.
- Provides rich set of controls for artwork manipulation.

Overview
In the past, whenever layout artwork had to be added to a schematic, it was done as either a fixed footprint instance or as an artwork macro written in the database language of AEL. Use of AEL is more flexible because artwork macros can be parameterized, but it is a manual process and requires familiarity with the AEL language. The Graphical Cell Compiler in HP Advanced Design System makes the job of adding parameterized artwork an easy process.

In general, controls are attached to layout primitives to stretch, repeat or move them. Controls can be fixed values or parameterized and tied together with equations. You determine the logical sequence for applying controls to produce the final artwork, after which the Graphical Cell Compiler will produce a compiled AEL macro. The compiled AEL macro can then be assigned to any schematic primitive or subcircuit.

Construction lines are used as control references and can be placed at any angle relative to the object. Operations such as stretching, moving or repeating are done relative to the control reference. The Controller Viewer gives you an easy way to see and modify which controls are defined and in what order they will execute.

Configuration Detail
Requires the Design Environment module (E8900A/AN) and the Layout module (E8902A/AN).

Framework Links

Framework Links (sometimes called integration modules) allow you to integrate your HP designs with third-party vendors (e.g., Mentor Graphics and Cadence Design Systems*) to provide a fully integrated process that maintains the integrity of your high-frequency designs. Separate integration modules are available for schematic and layout transfer, each utilizing the HP Intermediate File Format (IFF) as the exchange mechanism. The HP IFF is an ASCII intermediate file for both the schematic and layout transfers, allowing the HP Advanced Design System and EDA vendor solutions to be installed on different machines, platforms or sites.

*Cadence is a trademark of Cadence Design Systems, Inc.

Mentor IFF Schematic Translator (E8965A/AN)

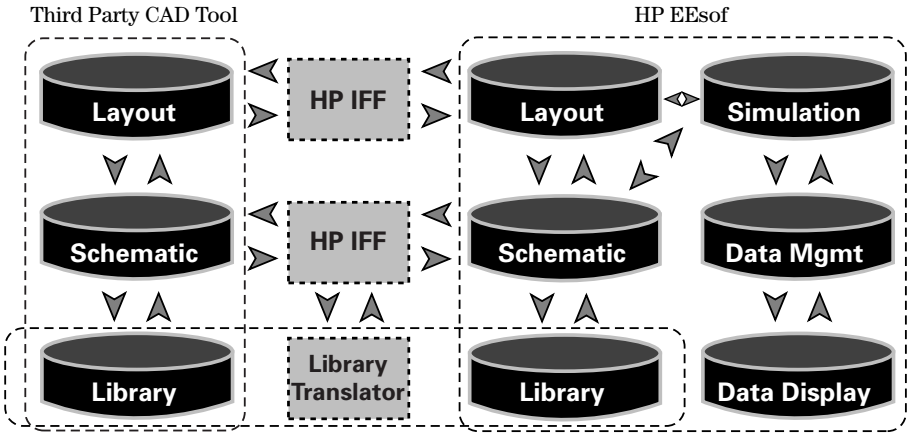
Features and Benefits

- Allows bi-directional schematic transfers to speed and simplify design processes.
- Permits RF board and IC design schematics to be shared between HP Advanced Design System and Mentor Graphics Design Architect.

Overview
High-frequency circuits can be entered and edited on the schematic in either the Mentor Design Architect or the HP environment. All edited material can be transferred to either environment. All properties and design hierarchy are preserved through the translation. Simulation and high-frequency physical design must occur in HP Advanced Design System. This preserves the high-frequency design features such as specialized plots, test equipment I/O, optimization and tuning, data presentation types, and special analysis types. Mentor component libraries can be used for simulation in HP Advanced Design System, but HP simulator properties must be attached and pin/property attributes modified on any component for the simulator to recognize the part. The HP Library Translator (E8969A/AN) is recommended to facilitate this.

Configuration Detail
Requires the Design Environment module (E8900A/AN).

Compatibility
This module is used in conjunction with the Mentor RF Gateway product (sold by Mentor Graphics) to provide the complementary IFF schematic transfer. The Mentor Falcon Framework Version B.2 and higher are supported.



Mentor IFF Layout Translator (E8966A/AN)

Features and Benefits

- Allows bi-directional layout transfers from HP Advanced Design System to Mentor Graphics Board Station, to speed and simplify design processes.
- Permits physical designs to be shared between HP Advanced Design System and Mentor Graphics Board/MCM/Hybrid Station.
- Transfers part footprints into HP Advanced Design System for library creation.
- Offers single-button transfer of HP schematic and layout to Mentor Board Station for ease of use.

Overview
This integration module provides unidirectional layout transfer between the HP Advanced Design System and Mentor's Board/MCM/ Hybrid Station. It does not support direct transfer of physical designs from the HP Advanced Design System to Mentor's IC Station (GDSII file format must be used).

With the Mentor IFF Layout Translator you can create and refine the high-frequency physical design in the HP Advanced Design System, then transfer it to Mentor Board Station. Once in Board Station, the high-frequency design is treated as a fixed high-frequency region. This region is used as a single logical part with ports on the region boundary. It can be moved and rotated like any other Board Station geometry, and any board can have a large number of high-frequency regions. You control which parts in the high-frequency region are included in the bill of materials (BOM) used in Board Station. This allows packaged components to be included in the BOM, while excluding variable components (like transmission line elements).

The Mentor IFF Layout Translator also allows Mentor Board Station component geometry ("footprint") to be transferred to the HP Advanced Design System's layout. When these component geometries are used in the HP Advanced Design System, and the design is transferred back to Board Station, the original geometry is used instead of being transferred again, reducing transfer time. A component geometry that has been transferred must be merged with an appropriate model and its high-frequency simulator properties, in order to simulate it in HP Advanced Design System. The HP Library Translator (E8969A/AN) is recommended to facilitate this.

Configuration Detail
Requires the Design Environment (E8900A/AN), Layout (E8902A/AN), and Mentor IFF Schematic Translator (E8965A/AN) modules (required for layout transfer to preserve the Mentor schematic-to-layout connectivity).

Compatibility
This module is used in conjunction with the Mentor RF Gateway product (sold by Mentor Graphics) to provide the complementary IFF schematic transfer.
The Mentor Falcon Framework Version B.2 and higher are supported for uni-directional layout transfer (HP to Mentor).

IFF Schematic Translator (E8967A/AN)

Features and Benefits

- Allows bi-directional schematic transfers to speed and simplify design processes.
- Allows schematics to be shared between HP Advanced Design System and third-party EDA vendors such as Cadence.

Overview
This integration module provides bi-directional schematic transfer between HP Advanced Design System and all EDA vendors (other than Mentor Graphics) that support IFF schematic translation. The module requires the IFF Schematic Translator from the vendor to complete the IFF translation. The schematic transfer functionality will be determined by the EDA vendor's product; its operation may be similar to the Mentor IFF Schematic Translator but cannot be guaranteed by HP.

Configuration Detail
Requires the Design Environment module (E8900A/AN).

Compatibility
A Cadence Composer IFF schematic translation module is included with this module. It supports the Cadence Design Framework II version 9502 or higher. Solutions are available for Cadence Concept and Viewlogic PowerView from these vendors, not from HP EEsof. Please contact these vendors for information.

IFF Layout Translator (E8968A/AN)

Features and Benefits

- Allows bi-directional layout transfers from HP Advanced Design System to third-party EDA tools, to speed and simplify design processes.
- Allows physical designs to be shared between HP Advanced Design System and third-party EDA vendors such as Cadence.
- Transfers part footprints into HP Advanced Design System for library creation.

Overview
The IFF Layout Translator provides unidirectional layout transfer between HP Advanced Design System and all EDA vendors (other than Mentor Graphics) that support IFF schematic translation. The module requires the IFF Layout Translator from the vendor to complete the IFF translation. The layout transfer functionality will be determined by the EDA vendor's product; its operation may be similar to the Mentor IFF Layout Translator but cannot be guaranteed by HP.

Configuration Detail
Requires the Design Environment module (E8900A/AN).

Compatibility
Solutions are available for Cadence Allegro and Intercept Technologies Pantheon from these vendors, not from HP EEsof. Please contact these vendors for information.

Library Translator (E8969A/AN)

Features and Benefits

- Creates an HP-equivalent library of third-party EDA vendor libraries for design flexibility.
- Allows mapping of pin and property attributes.
- Permits the addition of HP simulation model parameters.
- Comes with a Component Translation Table that allows incremental library updates.

Overview
The Library Translator allows access to parts that exist in either your electronic corporate data base or your digital/analog EDA vendor-system data base. The module helps translate these parts libraries into an HP equivalent-parts library including simulation information. This facilitates design transfer between HP and analog design solutions by providing common parts in both systems. The Library Translator operates independently of the HP Advanced Design System and requires that the EDA vendor solution be able to export/import an IFF schematic file.

In the HP Advanced Design System a library part is composed of a schematic symbol, a physical footprint, and an electrical simulation model. In other EDA vendor solutions, a part may be just the symbol and physical footprint. Part information may also include the part number, statistical information, thermal information, cost, reliability, tolerance, etc. It is possible that some part attributes may not be interpreted in the same fashion between HP and other EDA vendors. For example, a transistor may use a pin numbering scheme that conflicts with the HP simulation model; or the pin names for a capacitor may be different (POS vs. PLUS). For proper simulation within the HP Advanced Design System, pin and property mapping is required.

The Library Translator is a semi-automatic solution that is able to read an IFF file containing the EDA vendor parts. This allows you to view the existing part properties, select what HP simulation model the part should be mapped to, edit the simulation model values, and potentially attach a footprint geometry. You can then export the enhanced part definition to an IFF file. Part attributes/properties will be automatically converted by the HP IFF Schematic Translator. An HP library is then created by reading the IFF file of new parts and saving this information into a user library. After a library is created, all future imports/exports use the conversion information to convert designs being read in the HP Advanced Design System or exported by it. The component translation information can be saved to a file to facilitate incremental library updates in the future. With a component mapping file, parts that are the same are automatically translated and only the new or changed parts need to be re-mapped.

Configuration Detail
No licenses required.

Compatibility
Supports HP Advanced Design System simulation models only.

Ordering Structure

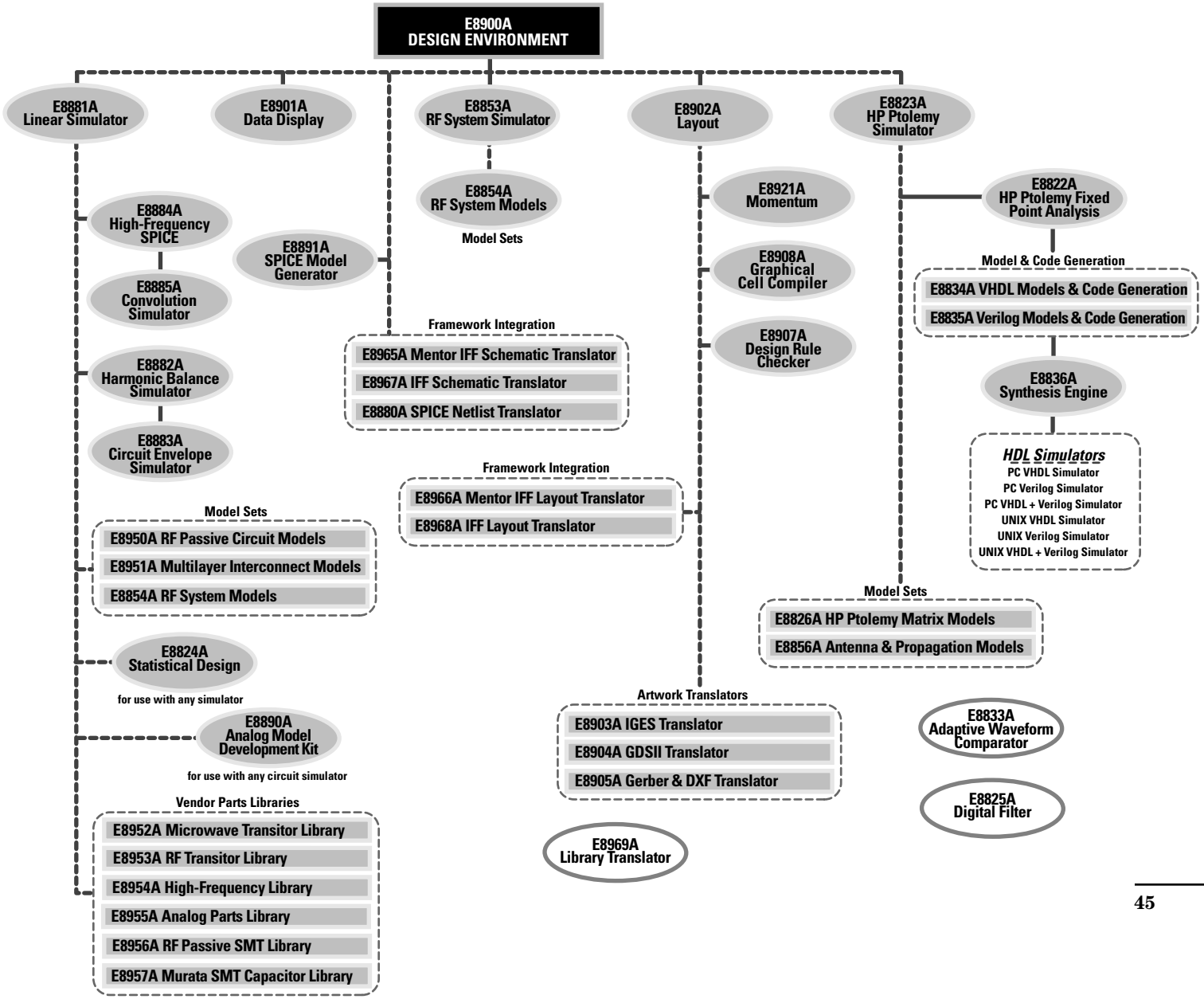
Each of the modules in the diagram below can be ordered separately or is included in bundled suites. However, with the exception of the Library Translator, Digital Filter and Adaptive Waveform Comparator, each module requires the module connected above it.

For example:

The Convolution Simulator requires High-Frequency SPICE, Linear Simulator and Design Environment .

The PC VHDL Simulator requires the Synthesis Engine, either the VHDL Models & Code Generator or the Verilog Models & Code Generator, HP Ptolemy Fixed-Point Analysis, the HP Ptolemy Simulator, and the Design Environment.

The Library Translator, Digital Filter and Adaptive Waveform Comparator can be ordered independent of any other module.



Additional Solutions

Additional solutions, which are not integrated into HP Advanced Design System, are available from HP EEsof to help you with related aspects of design. These include:

HP High-Frequency Structure Simulator 5.0
For electromagnetic modeling of arbitrarily-shaped, passive 3D structures.

In HFSS you'll find such features as:

- Finite-element simulation and mesh engines that are faster than previous releases and reduce memory requirements
- A drawing package that provides broad compatibility with other 3D drawing solutions
- A solid-model parts library that permits complex shapes and structures to be entered
- Unlimited "undo" and 3D pan and zoom flexibility, to save you time and reduce errors in the design entry process

HP IC-CAP 5.0
A versatile device-modeling program in which we've incorporated:

- A user-friendly Windows-style graphical interface that makes you more productive
- A flexible data manager that allows you to utilize data from external measurement databases and physical device simulation solutions
- A real-time graphical tuner that shows you how each parameter is related to simulated device performance
- Enhanced versions of BSIM3v3.1 model, the Philips MOS Model 9, and the HP Root FET model to improve accuracy and ease-of-use
- Support for the HP E2050A LAN/HP-IB Gateway, which allows remote control of test instrumentation via the LAN, and the HP 8720D family of network analyzers for high-frequency device characterization

Support & Training

Customer Education

HP EEsof has dedicated significant resources to its on-going customer education program. Courses have been developed to enable you to become productive as quickly as possible. Constructed to closely approximate the design process, students learn to use the software through solving an engineering design problem. For example, our course titled "Using HP Advanced Design System for RF and Microwave Circuit Designers" takes a standard block diagram and works through the design and simulation of each major component. HP EEsof courses explain all major features of the software and provide application-oriented examples of real-life solutions. Additionally, students typically spend over half their class time working on real-world lab exercises, ensuring a high degree of confidence when they return to their workplaces.

HP Advanced Design System courses are configured to meet the needs of distinct areas of communications signal path design, including RFIC, RF Board, Microwave Circuit, Communications System, and DSP. Students learn about topics that directly relate to their field of interest. Available courses include:

- HP Advanced Design System Essentials
- Using HP Advanced Design System for RF and Microwave Circuit Design
- Using HP Communication Systems Designer
- Using HP DSP Designer
- Using HP DSP Synthesis and HDL for DSP Hardware Design
- HP Momentum for HP Advanced Design System Users
- AEL Programming for HP Advanced Design System Users
- Physical Design and Customization for HP Advanced Design System Users

Designers can attend classes at specially-equipped training centers around the world or arrange for on-site instruction at their companies. Our training program gives designers the right start using HP EEsof's powerful design software.

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Documentation

HP Advanced Design System comes with complete on line documentation, as well as a hardcopy "Getting Started" manual tailored to your design process. These materials include engineering examples to get you up and running quickly. In addition to on-line documentation, you can order a set of hardcopy manuals: HP 8900AD (for the complete set of HP Advanced Design System manuals) or HP 8820AD (for the DSP Designer manuals).

System Requirements

These are the system requirements for the use of HP Advanced Design System on workstations (WS) and PCs.

Displays: High-resolution color (Super VGA, 1024/768, 15-inch min.)

RAM: 64 MB min for WS; 64 MB min for PCs

Swap Space: 200 MB recommended for WS and PCs

Hard Disk: 500 MB recommended for WS and PCs, plus swap space

Security: In WS, a codeword is locked to an individual computer ID; in PCs the codeword is locked to an external device attached to the parallel port

For additional information on this subject, please contact your HP representative.

Platform Compatibility

HP Advanced Design System products are supported on popular workstations and PC platforms including:

- HP workstations running 9.x, 10.2
- Sun workstations running Solaris 1.x to 2.x
- Intel/Pentium 90 MHz CPU or higher running Windows 95 or Windows NT 4.0

Product Information

This data sheet describes HP Advanced Design System Version 1.0

For additional information on related HP EEsof products please see:

Brochures:	**Literature#**
HP Advanced Design System	5966-2870E
HP DSP Designer	5966-2869E
HP RFIC Designer	5966-2071E
HP RF Board Designer	5966-2872E
Data Sheets	
IC-CAP 5.0 Modeling Suite	5965-7742E
HP Momentum	5963-7129E
HP/Mentor Graphics Integration	5963-6630E
HP High-Frequency Structure Simulator 5.0	5963-9794E
Transitioning to HP Advanced Design System	5966-4029E

Web Support

Bookmark www.hp.com/go/hpeesof. It is the URL of the HP EEsof web site. The site contains detailed descriptions of our products, services, documentation, support organizations, libraries, and more.

For more information, contact your local HP Sales office or the nearest listing in your telephone directory.

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