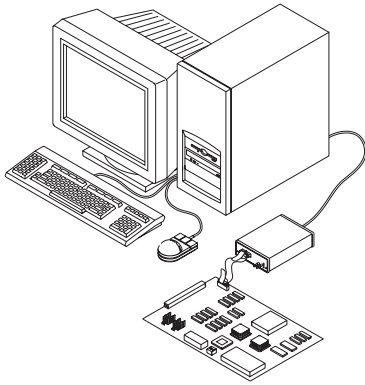


Emulation and Analysis Solutions for Motorola/IBM PowerPC 740/750 Microprocessors

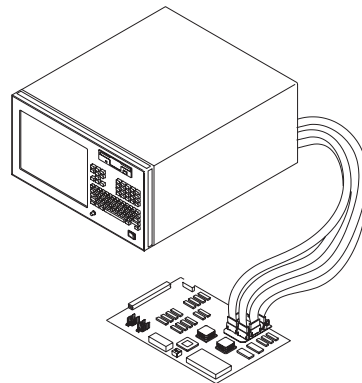
Product Overview

Debug and Integrate Real-Time Embedded Systems



JTAG Emulation

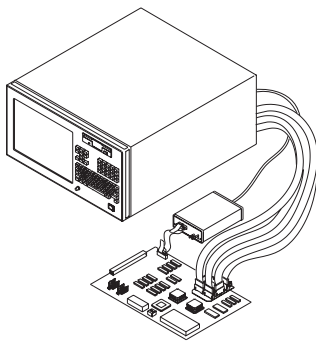
- Verify Interrupt Routines
- Debug Assembly Code
- Optimize Code



Logic Analysis Solution

- Perform Basic Signal Measurements
- Profile Hardware Operation
- Verify Signal Integrity
- Verify Conformance to Specifications
- Exercise Microprocessor and Other Hardware
- Debug Boot Code

Emulation and Analysis Solutions for the Design Team



Emulation Solution with Real-Time Trace

- Debug Hardware/Software Interaction
- Profile Hardware/Software Interaction
- Optimize System Performance
- Perform System Test

Quickly and accurately determine the root cause of your team's most difficult hardware, software, and system integration problems with Agilent Technologies' powerful emulation and logic analysis solutions.

Agilent's emulation and analysis solutions for the Motorola/IBM PowerPC 740/750 combine the powerful tools of run control,

code download, debugger connections, and logic analysis for a complete, scalable system debug environment.

With a scalable solution from Agilent Technologies, design team members can customize product offerings to meet their unique requirements. Solutions range from emulation probes combined

with the industry's leading debuggers to emulation with real-time trace to solve today's most complex Motorola/IBM PowerPC 740/750 design problems. Agilent's solutions are designed to meet your needs today and protect your investment as your needs change in the future.

With logic analysis providing timing and state analysis, you can monitor microprocessor activity in relation to other important system signals such as a PCI bus, other microprocessors, or I/O devices. Traditional emulation systems don't allow you to time-correlate events across your entire system using timing, analog, and state analysis for your most difficult integration problems.

The logic analyzer is nonintrusive, allowing you to run your target system at full speed. A system trace, up to 4 M deep, can be combined with complex triggering to find the toughest problems. The microprocessor instruction set execution can be correlated to high-level source code with the Agilent source correlation tool set.



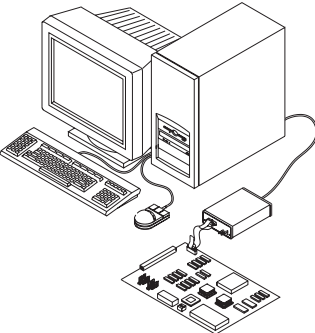
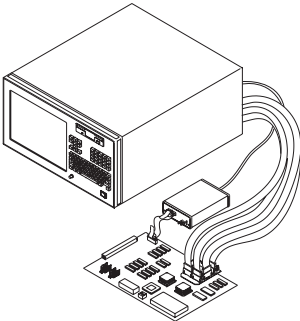
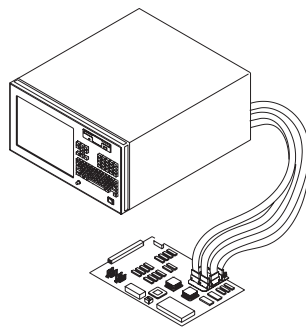
Agilent Technologies
Innovating the HP Way

Agilent Technologies' Scalable Solutions

Agilent's emulation and logic analysis solutions are scalable for each member of the digital design team. The following are three typical configurations for firmware/software debug, hardware debug, and system integration.

Components of these solutions include a logic analyzer, emulation probe/module, analysis probe, inverse assembler, source correlation tool set, and system performance analysis tool set.

Information on each of these components is included in this document.

| | System Features | System Components and Functionality | |
|---|--|---|---|
|  | JTAG Emulation <ul style="list-style-type: none">• Microprocessor run control on your target system• Debugger connection | <ul style="list-style-type: none">• Emulation Probe: (see p. 3)<ul style="list-style-type: none">- Exceptional download speed and single stepping- View and modify memory, view and modify registers on your target system or evaluation board from the debugger interface• Connection to industry-leading debuggers from Green Hills, Microtec, SDS, and WindRiver | |
| |  | Emulation Solution with Real-Time Trace <ul style="list-style-type: none">• Microprocessor run control on your target system• Debugger connection• Real-time logic analysis trace solution:<ul style="list-style-type: none">- Assembly level trace- Source code trace• BGA probing solution | <ul style="list-style-type: none">• Agilent 16700A Series Logic Analysis System:<ul style="list-style-type: none">- Capture and analyze code flow and data flow without halting the target system- Time-correlate analog, timing, and state events across your entire system- Monitor microprocessor activity in relation to system buses, other microprocessors, or I/O devices• Inverse Assembler: (see p. 8)<ul style="list-style-type: none">- Connect to target using BGA probing solution with AMP Mictor connectors- Disassemble trace listing into PPC 740/750 mnemonics• Integrated Emulation Module: (see p. 3)<ul style="list-style-type: none">- Exceptional download speed and single-stepping- View and modify memory, view and modify registers on your target system or evaluation board from the debugger interface- Connect to industry-leading debuggers from Green Hills, Microtec, SDS, and WindRiver• Agilent Source Correlation Tool Set: (see p. 9)<ul style="list-style-type: none">- Time-correlate acquired logic analysis trace to high-level source code- Step through in assembly or high-level code |
| |  | Logic Analysis Solution <ul style="list-style-type: none">• Real-time logic analysis trace solution:<ul style="list-style-type: none">- Assembly level trace• BGA probing solution | <ul style="list-style-type: none">• Agilent 16700A Series Logic Analysis System:<ul style="list-style-type: none">- Capture and analyze code flow and data flow without halting the target system- Time-correlate analog, timing, and state events across your entire system- Monitor microprocessor activity in relation to system buses, other microprocessors, or I/O devices• Inverse Assembler: (see p. 8)<ul style="list-style-type: none">- Connect to target using BGA probing solution with AMP Mictor connectors- Disassemble trace listing into PPC 740/750 mnemonics |

| Microprocessor | Package Type | Microprocessor Clock Speed | JTAG Emulation | Emulation Solution with Real-Time Trace | Logic Analysis Solution |
|----------------|--------------|----------------------------|----------------|---|-------------------------|
| PPC 740 | BGA | Up to 300 MHz | X | X | X |
| PPC 750 | BGA | Up to 300 MHz | X | X | X |

Table 1: Emulation and Analysis Solutions for Motorola/IBM 740/750 Microprocessors

Emulation Probe and Module

The emulation probe and module provide the same functionality. The emulation probe is a standalone product, as shown in figure 1. The emulation module is an integrated plug-in for the Agilent 16700A Series logic analysis systems.

The emulation probe and module have been improved to provide the exceptional download speed and single stepping. These improvements include:

- 32 bit microprocessor
- 100 Base TX LAN
- New scan-chain controller

Both the probe and module help you debug your code by providing run control, code download, and memory/register display and modification. You can control program execution through single stepping, run/break, and set/modify break-points. You can also run code at full speed in the target. Agilent's new emulation probes and modules allow you to complete these tasks more quickly so you can bring your products to market sooner.

An industry leading debugger can be used to control both the emulation probe and module. Alternatively, they can be controlled by the emulation control interface provided with the logic analyzer. These interfaces are described on page 4.

The emulation probe and module can be controlled over your local area network (LAN) by the debugger and connect to your target through a 16-pin Berg style connector, as shown in figure 4.

Unlike traditional emulators, the emulation probes and modules provide more stable operation by accessing only the debug pins of the microprocessor. You don't

need a serial port on your target system to download code. Unlike ROM monitors, they don't require user memory.

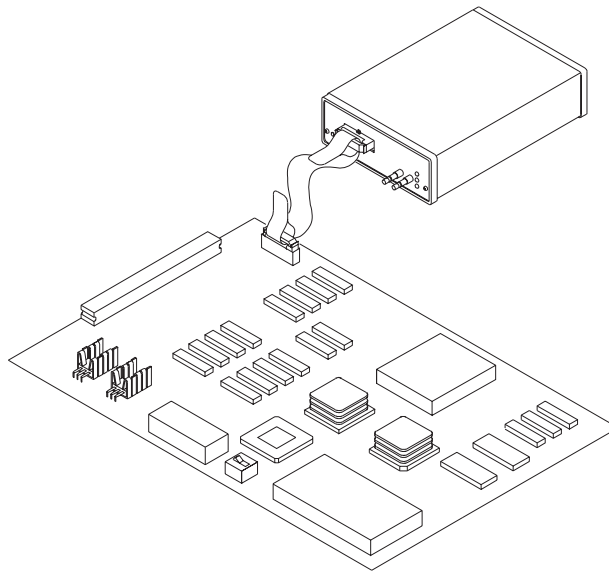


Figure 1: Standalone Emulation Probe

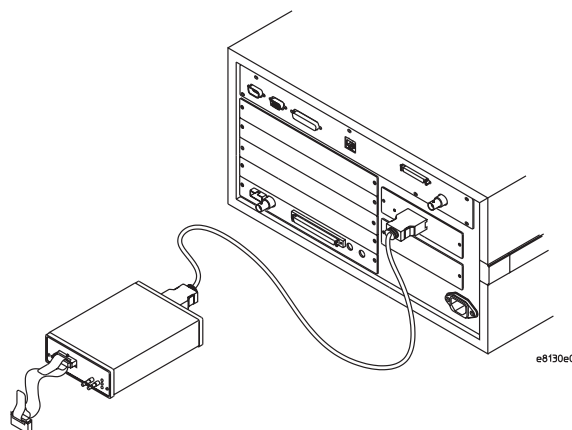


Figure 2: Agilent 16702A Logic Analysis System with Integrated Emulation Module

Debugger Interface

Industry-leading debuggers can control the emulation probe and module. You can set breakpoints, single-step through code, examine variables, and modify source code variables from the high-level source code debugger interface.

Debugger interfaces must be ordered directly from the debugger vendor.

Debugger Connections

Green Hills Software, Inc.
30 West Sola Street
Santa Barbara, CA 93101 USA
Phone: (805) 965-6044
<http://www.ghs.com>

Microtec, A Mentor Graphics Company
880 Ridder Park Drive
San Jose, CA 95131 USA
Phone: (800) 950-5554
Phone: (408) 487-7000
<http://www.mentor.com/microtec>

Diab-SDS
323 Vintage Park Drive
Foster City, CA 94404 USA
Phone: 630-724-2520
<http://www.diabsds.com>

WindRiver Systems
500 Wind River Way
Alameda, CA 94501 USA
Phone: 1-800-545-WIND
<http://www.wrs.com>

Please check with your local Agilent Test and Measurement sales office or visit our web site at <http://www.agilent.com/find/las-data> for the current list of debugger connections.

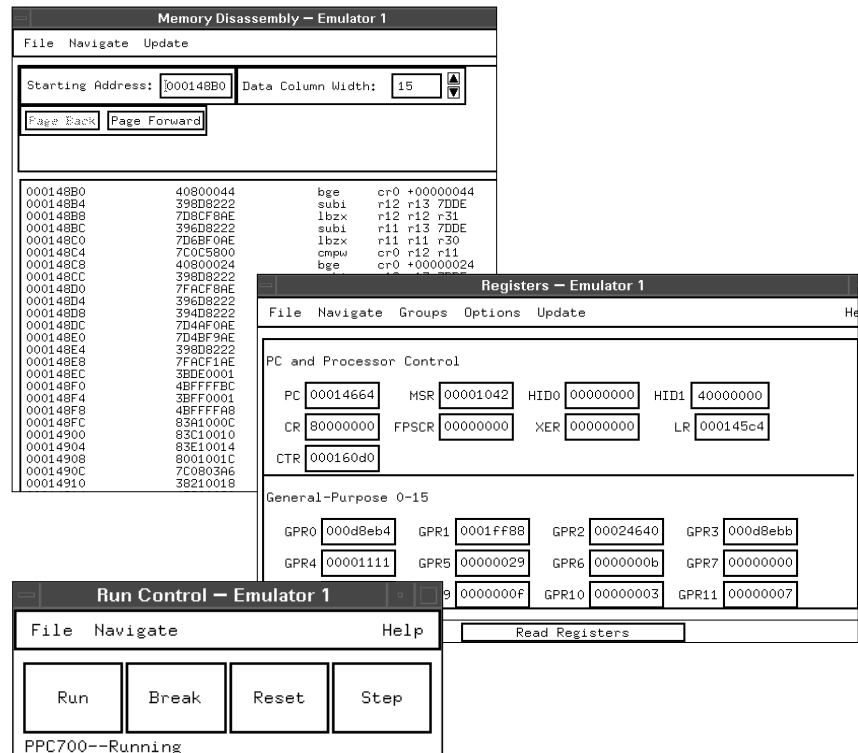


Figure 3: Emulation Control Interface

Emulation Control Interface

The emulation module integrated into the logic analysis system can be controlled directly by the emulation control interface. You can easily display and modify contents of microprocessor registers, system memory, and I/O. You can also view memory code segments disassembled into familiar Motorola/IBM PowerPC 740/750 assembly instructions.

From the run control window you can instruct the microprocessor to run, break, reset, or single-step. You also can choose whether the memory, I/O, and register displays are updated for breaks and single steps.

Writing command files that set up registers, memory, and I/O in your system is easy with the command language. Once the command file is written, save it on the logic analyzer hard disk. When you want to initialize your hardware system to a particular state, simply recall and execute the command file. Unlike a debugger interface, the emulation control interface does not reference back to the high-level source code.

Emulation Module and Probe Migration

Agilent Technologies protects your current investment by providing a migration path for the emulation modules and probes as your needs change. To move from one processor family to another, simply order a migration kit for the emulation module or probe, which will provide all the necessary hardware, firmware, and cables to support your new processor family at a fraction of the cost of a new system.

This same migration path works for the emulation probes or emulation modules. Migration is available for those processors in the E5900B Series.

Emulation Module Triggering Integration with Logic Analyzer

With the emulation module, use the powerful triggering of the 16700A Series logic analysis systems to halt on events such as microprocessor activity, system buses, or other external events. The emulation module also can trigger the logic analyzer when a breakpoint is hit. This provides powerful event correlation between the debugger interface environment and the logic analyzer.

| Specification | Description |
|----------------------------------|--|
| Microprocessors Supported | Motorola/IBM PowerPC 740/750 |
| Physical Connections | Ethernet Autosensing 10/100 Ethernet RS-232-C 9600 Kbaud rate |
| Number of Breakpoints | Virtually unlimited software breakpoints or one hardware breakpoint |
| Physical Size | 105 mm width x 151 mm depth x 40 mm height |
| Environmental | |
| Temperature | Operating: 5 °C to +40 °C (+41 °F to +104 °F) Nonoperating: -40 °C to +70 °C (-40 °F to +158 °F) |
| Altitude | Operating: 4,600 m (15,000 ft) Nonoperating: 4,600 m (15,000 ft) |
| Humidity | 15% to 80% @ 40 °C for 24 hours |
| Regulatory Compliance | EMC CISPR 11:1990/EN 55011:1991 Group 1, Class A IEC 801-2:1991/EN 50082-1:1992 4 kV CD, 8 kV AD IEC 801-3:1984/EN 50082-1:1992 3 V/m, (1 kHz 80% AM, 27-1 kHz) IEC 801-4: 1988 / EN 50082-1:1992 0.8kV Sig lines, 1 kV Power lines |
| Safety Approvals | IEC 1010-1:1990 AMD 1:1992 UL 1244 CSA-C22.2 No. 231 (Series M-89) |

Table 2: Emulation Probe and Module Specifications

Emulation Probe and Module Target Connection Information

A 16-pin male 2X8 header Berg style connector is needed on the target development board to connect the PowerPC 740/750 microprocessor interface assembly to the JTAG debug port of the microprocessor.

The header should be placed as close as possible to the processor to ensure signal integrity. TD0, TD1, TCK, TMS, and /TRST signal traces between the JTAG connector and the PowerPC 740/750 must be less than three inches. If these signals are connected to other nodes, you must connect in a daisy chain between the JTAG debug connector and the PowerPC 740/750. These signals are sensitive to crosstalk and cannot be routed next to active signals, such as clock lines on the target board.

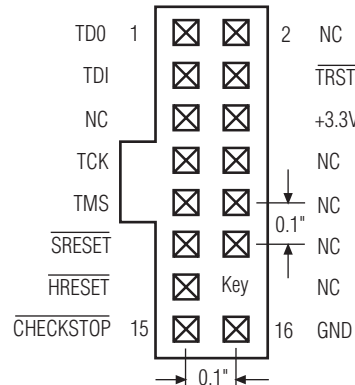


Figure 4: Target Development Board Header Connector (Top View)

| Header Pin No. | PPC 740/750 I/O | Signal Name | Resistor |
|----------------|-----------------|-------------|----------------------|
| 1 | Out | TD0 | |
| 2 | | NC | |
| 3 | In | TDI | 1K Ω pulldown |
| 4 | In | TRST | 10K Ω pullup |
| 5 | | NC | |
| 6 | | Power* | 1K Ω series |
| 7 | In | TCK | 10K Ω pullup |
| 8 | | NC | |
| 9 | In | TMS | 10K Ω pullup |
| 10 | | NC | |
| 11 | In | SRESET | 10K Ω pullup |
| 12 | | NC | |
| 13 | In | HRESET | 10K Ω pullup |
| 14 | | KEY | |
| 15 | Out | CHECKSTOP | 1K Ω pullup |
| 16 | | GND | |

Table 3. JTAG Interface Connections

* The +POWER signal is sourced from the development board and is used as a reference signal. It should be the power signal supplied to the processor (either +3.3V or +5V). It does not supply power to the emulation probe.

Note: NC Refers to No Connect

Notes and Information:

1. HRESET, SRESET, and TRST from the JTAG connector must be logically ORed with the HRESET, SRESET, and TRST signals that connect to the processor on the target system. They cannot be “dotted” or “wire-ORed” on the board.
2. If the target board does not use the QACK signal, the board must have a pull-down resistor to pull this signal low. This allows the PowerPC to enter the state required for reading and writing processor scan string data.

Real-Time Trace Analysis

Real-time trace analysis consists of a physical connection to signals on the Motorola/IBM PPC 740/750 microprocessors, acquisition of relevant data, and analysis of the real-time captured bus information.

Physical connection to the microprocessor is provided by an AMP Mictor probing solution.

The real-time trace analysis solutions for the Motorola/IBM PPC 740/750 include inverse assembly, source correlation, and system performance analysis.

For information on the data acquisition modules for the 16700A Series logic analysis systems, please refer to related literature on page 19.

| MPC 7XX Microprocessor | Supported Speed | Probing Solutions | Real-Time Trace Solutions |
|---------------------------|--------------------|--|---|
| PPC 740 | Up to 300 MHz | Mictor Connector Probing Solution: <ul style="list-style-type: none">Mictor connectors designed in target for access to critical signals for logic analysis | Inverse Assembly: <ul style="list-style-type: none">Disassembly of bus information into PPC 740/750 microprocessor mnemonicsPPC 740/750 configuration files for logic analyzer |
| PPC 750 | Up to 300 MHz | | Source Correlation: <ul style="list-style-type: none">Time-correlation of acquired trace to high-level source codeTrigger and search through trace in high-level source code |
| | | | System Performance Analysis: <ul style="list-style-type: none">Statistical performance measurements on trace dataState overview, state interval, time interval, and time overview measurements |

Table 4: Real-Time Trace and Probing Alternatives

Inverse Assembler

The inverse assembler quickly configures the logic analyzer by labeling address, data, and status signals for the PPC 740/750 microprocessors. It also provides PPC 740/750 mnemonics in the trace listing for easy correlation between captured data and target code. The inverse assembler works with the Agilent B4620B source correlation tool set to provide time correlation between the assembly-level trace and the high-level source code.

The inverse assembler provides filters and color coding to show and/or suppress different instructions such as data reads, data writes, unexecuted prefetches, and memory map regions.

The inverse assembler has several modes of operation, depending on your microprocessor configuration. The inverse assembler provides PPC 740/750 mnemonics, but the cache must be off to see all cycles on the microprocessor.

Cache-On Trace

Agilent's newest inverse assemblers provide the ability to trace while the microprocessor cache is enabled. The logic analyzer samples branch messages and reconstructs the program flow. This is the only solution that guarantees uninterrupted program execution and never disables the cache.

The cache-on trace feature is available in version 1.42 or greater of the logic analyzer system software.

| Bank Number | Base Address | End Address | Memory Width |
|-------------|--------------|-------------|--------------|
| Bank 0 | 00000000 | FFFFFFF | 64 bits |
| Bank 1 | 00000000 | 00000000 | 64 bits |
| Bank 2 | 00000000 | 00000000 | 64 bits |
| Bank 3 | 00000000 | 00000000 | 64 bits |
| Bank 4 | 00000000 | 00000000 | 64 bits |
| Bank 5 | 00000000 | 00000000 | 64 bits |
| Bank 6 | 00000000 | 00000000 | 64 bits |
| Bank 7 | 00000000 | 00000000 | 64 bits |

Figure 5: Inverse Assembler Filter Options

Modes of Operation

State Modes

In state-per-address or data-cycle modes, the logic analyzer only records those states in which one or more of the strobes AACK, ARTRY, TA, DRTRY, or TEA are asserted. This mode filters wait states and exposes the PowerPC 740/750 microprocessor's decoupled address and data buses.

In state-per-clock mode, address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and analysis during system crashes.

Timing Mode

Timing analysis is supported. All processor signals are connected directly to the logic analyzer pods.

Logic Analyzers Supported

- Contact your Agilent field engineer for the latest logic analyzer information.

Low-Cost Option for Tracing Code-Flow Only

Agilent offers a low-cost solution that provides much of the functionality of an emulation solution with real-time trace, but at a reduced cost. By connecting the logic analyzer to only the address and status bus, up to 68 channels of logic analysis can be captured. The real-time trace will still show opcode disassembly because the inverse assembler will read your S-Record file instead of the data bus. The tradeoff is that data reads and writes will be displayed with no value. Simply swap in another logic analyzer card and connect to the data bus if this functionality is required.

Source Correlation Tool Set

The inverse assembler can be used with the Agilent B4620B source correlation tool set for the 16700A Series logic analysis systems. This allows time correlation of an acquired trace to source code. The source correlation tool set uses the symbolic information provided in your object file to build a database of source files, line numbers and symbol information.

Once the logic analyzer acquires the real-time trace, you can step through the trace at assembly-code level or source-code level. You can also easily locate the cause of a problem by stepping backward to the root cause. With time-correlated analysis in both the digital and analog domains, Agilent provides powerful solutions for your most difficult hardware/software integration problems.

IEEE 695, Elf/Dwarf, Elf/Stabs and ASCII symbol files are supported.

System Correlation

With the logic analysis systems, you can time-correlate bus information from other microprocessors or bus interfaces in your target system, such as a PCI bus, with the PPC 740/750. Analysis probes are available for additional microprocessors. (Contact your local Test and Measurement sales office or visit our web site at <http://www.agilent.com/find/las-data> for more information).

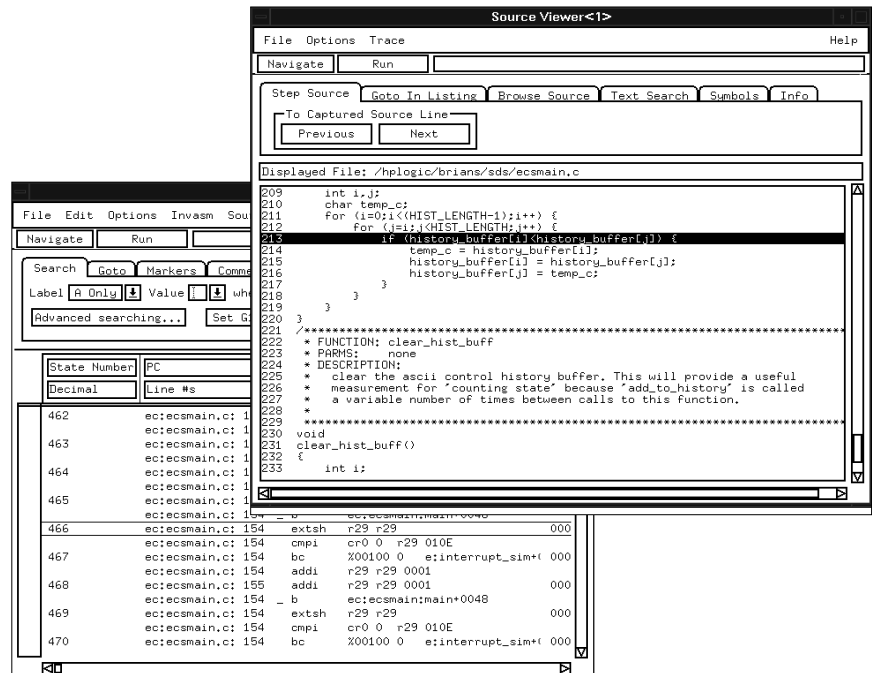


Figure 6: Inverse Assembled Trace Time-Correlated to Source Code Using the Source Correlation Tool Set

System Performance Analysis Tool Set

The Agilent system performance analysis (SPA) tool set is an optional software package for the 16700A Series logic analysis systems. The SPA tool set provides such statistical performance

measurements as state overview, state interval, time interval, and time overview. The same symbol file used with the source correlation tool set provides symbolic support for the system performance analyzer, as shown in figure 7.

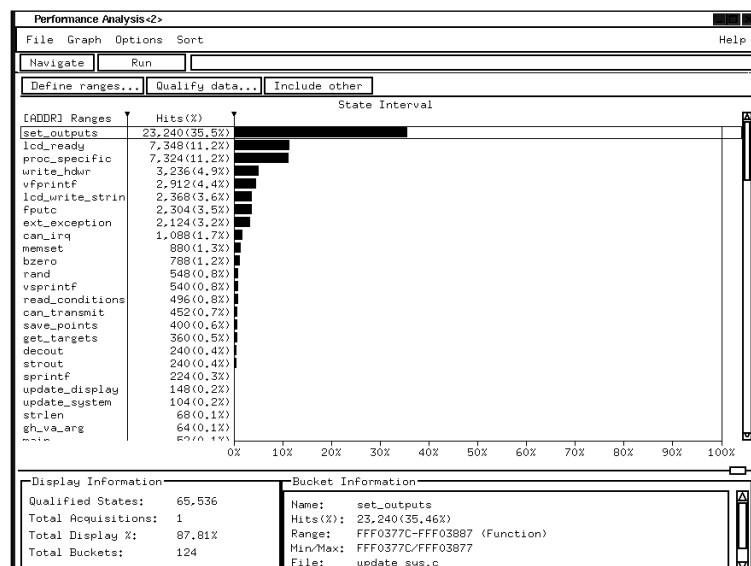


Figure 7: Statistical Performance Information from the System Performance Analysis Tool Set

Passively Probing the Target System with Agilent Logic Analyzers

Signals required for inverse assembly are shown in the pinout information table beginning on page 15 and must be routed to AMP Mictor 38 connectors for the logic analyzer.

Eight, 16-channel logic analyzer pods are required for inverse assembly. These eight pods are connected via the Mictor connectors to four high-density termination adapters. The adapters are not included with the inverse assembler and must be ordered separately.

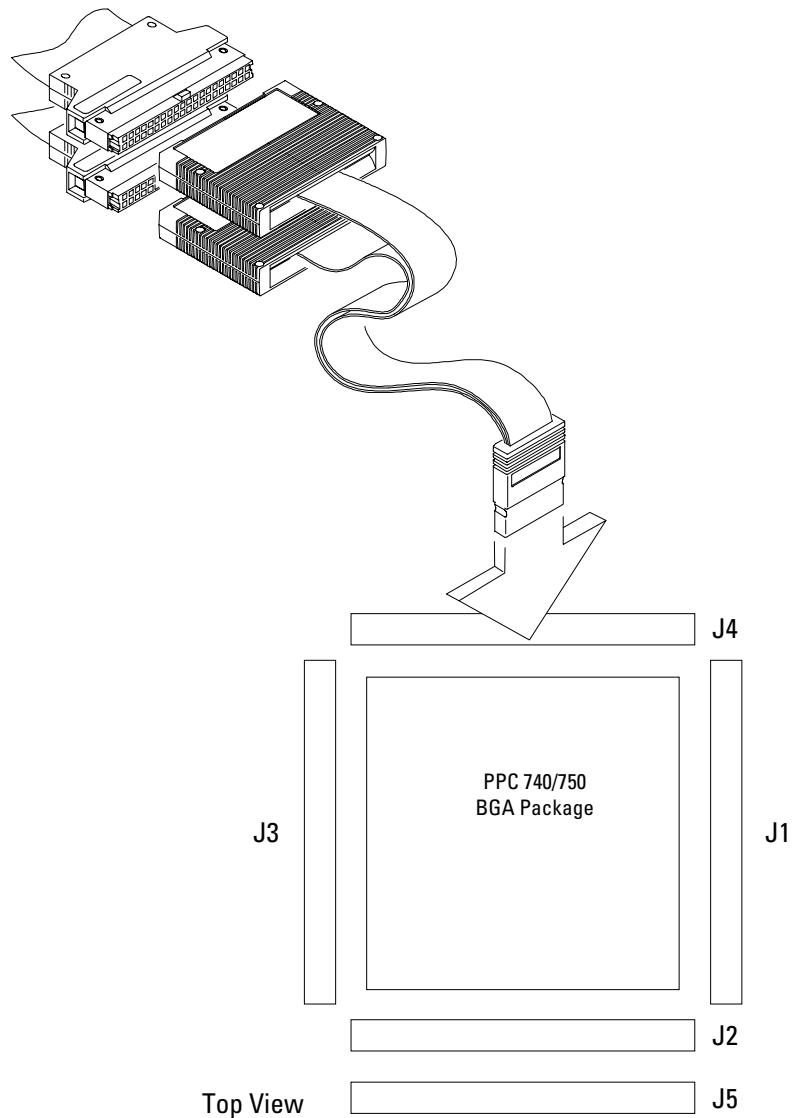


Figure 8. Connector Layout for a Motorola PowerPC 740/750 BGA Target

Direct Connection through High-Density Adapter Cables

The Agilent E5346A high-density adapters use a minimal amount of board space. Each high-density adapter connects two logic analyzer pods, providing 32 channels of logic analysis per connector and access to two clock pins, as shown in figure 9.

Grounds need to be connected to pin 3 of the AMP Mictor connector. SCL, +5VDC and SDA are not to be connected to the target system (pins 1, 2, and 4 on the Mictor connector).

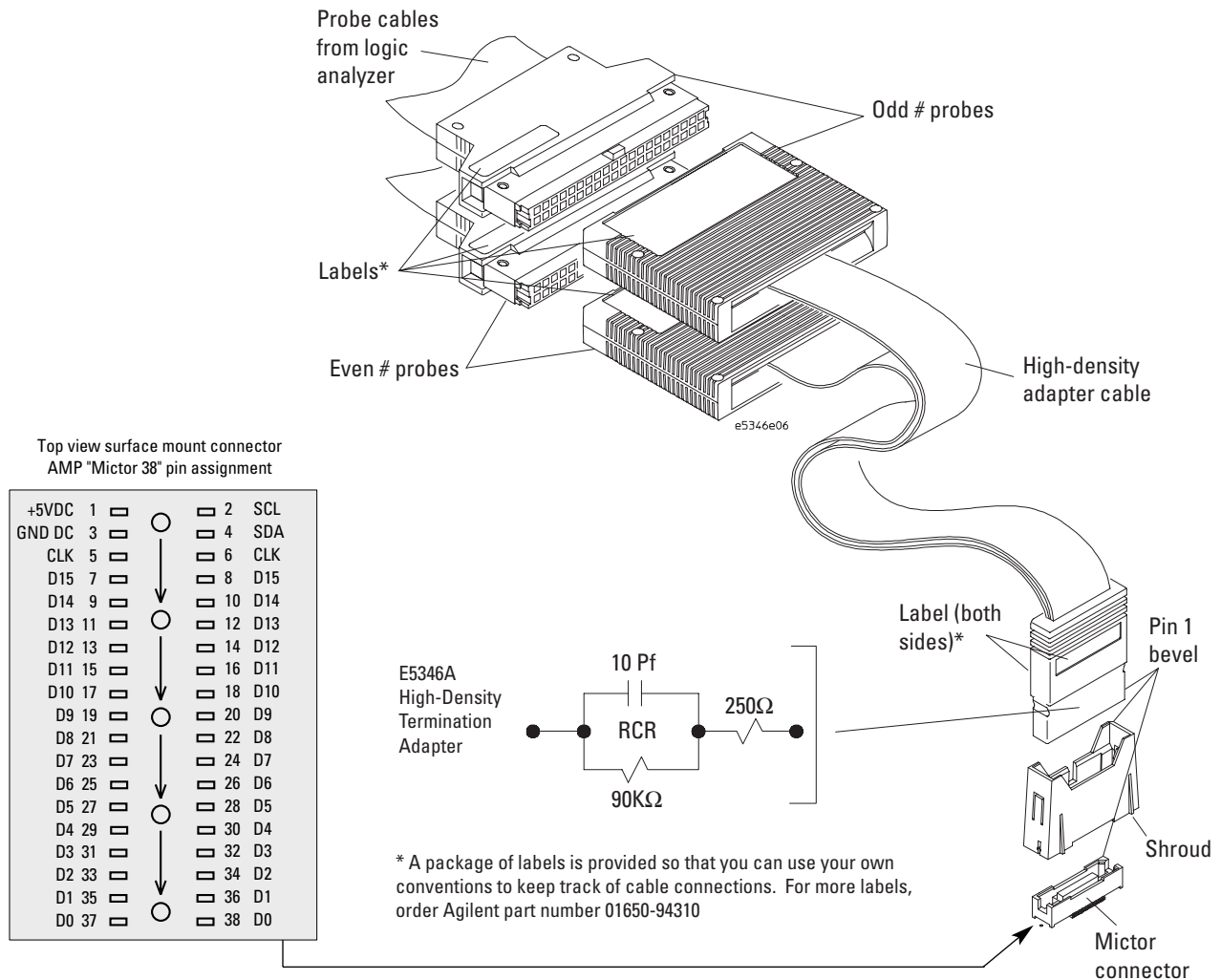


Figure 9. E5346A High-Density Termination Adapter

Termination for logic analysis is included at the probe tip of the E5346A high-density termination adapter for easy application and use. A schematic of this termination is shown in figure 10.

The AMP Mictor connector must be placed close enough to the target system so that the stub length created is less than $1/5$ the T_r (bus rise-time). For PC board material ($\epsilon_r=4.9$) and Z_0 in the range of $50\text{-}80\Omega$, use a propagation delay of 160 ps/inch of stub.

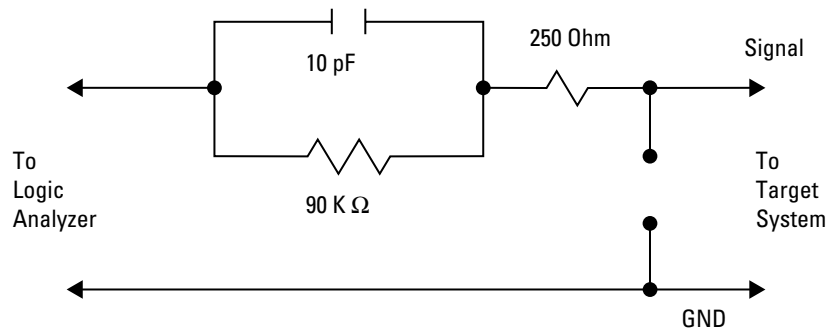


Figure 10. RC Network for Signal Termination

Four E5346A adapters and Mictor connectors are needed to probe all the required signals for inverse assembly.

Mictor Connector Placement

Placing the AMP Mictor connectors as close as possible to the signal source will minimize stub length and ensure a reliable measurement. Figure 11 shows the connector layout of J1-J5. J1-J4 are required for inverse assembly. J5 is optional for timing or state analysis of I/O ports.

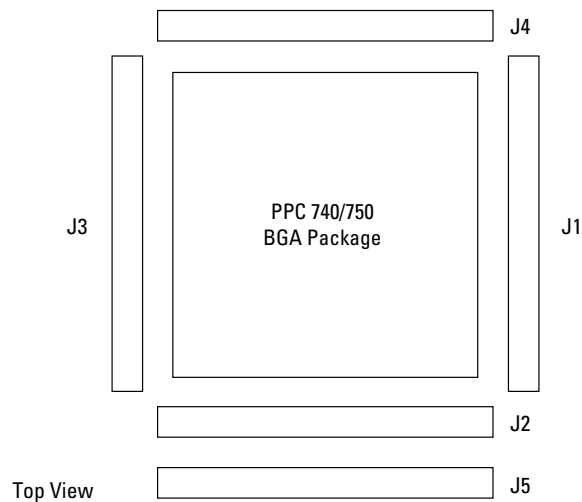


Figure 11. Mictor Connector Placement

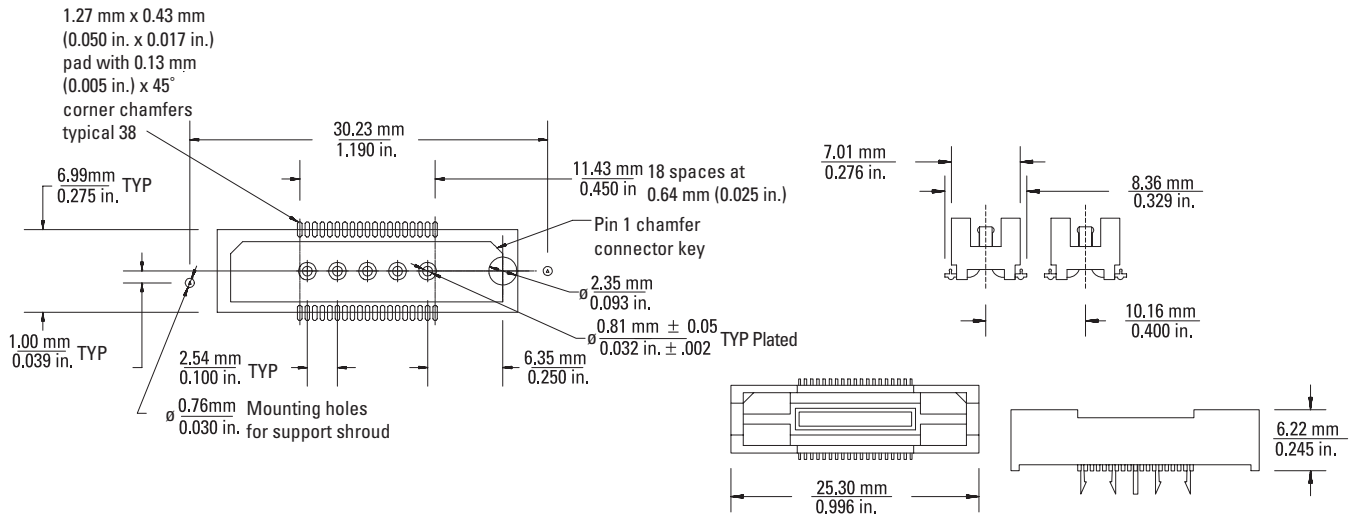


Figure 12. AMP Mictor Connector Dimensions

Mictor Connector

The AMP Mictor connectors are available from AMP (PN 2-767004-2) or from Agilent Technologies (PN E5346-68701). The Agilent Mictor kit contains five AMP Mictor connectors and five support shrouds. The signals +5 VDC, SCL, and SDA are not used for probing and should not be electrically connected to the target system. See figure 9.

Support Shroud

A support shroud (Agilent E5346-44701) is recommended to provide additional strain relief between the E5346A adapter and the AMP Mictor connector, as shown in figure 13. The shroud fits around the AMP Mictor connector and requires two through-hole connections to the target board. Five shrouds are included with five AMP Mictor connectors in the E5346-68701 kit.

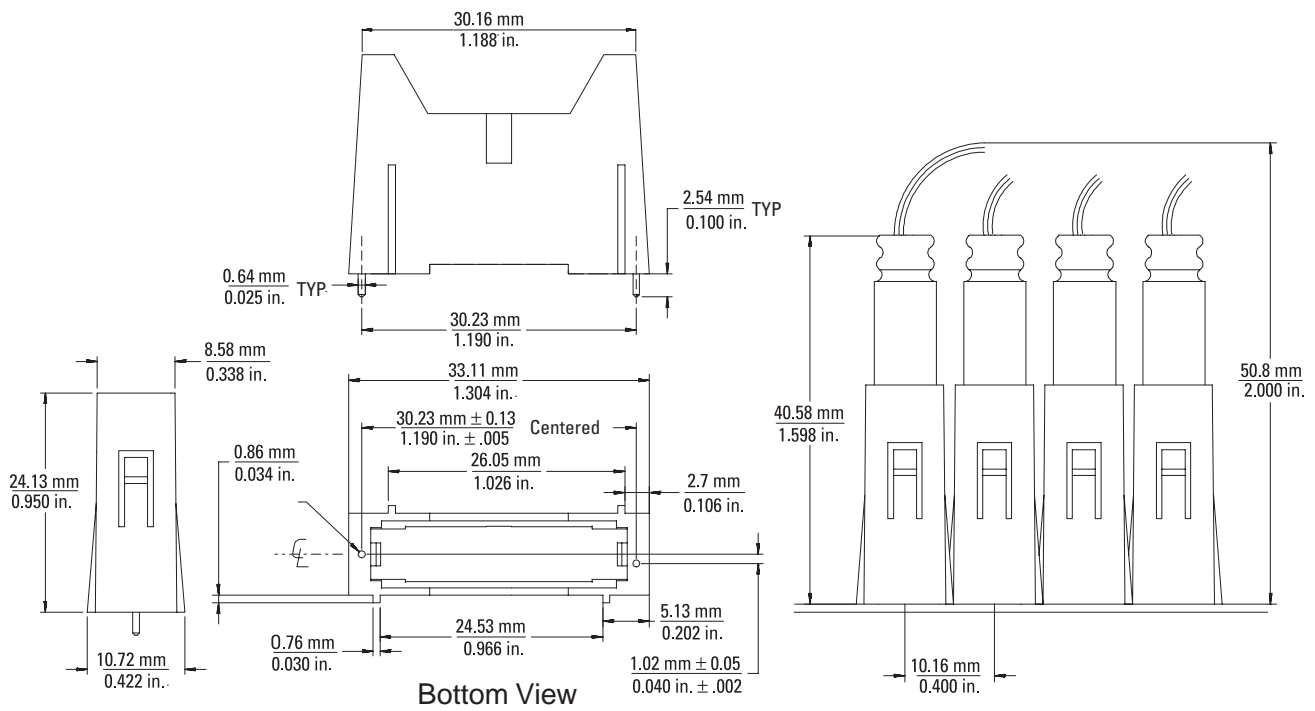


Figure 13. Support Shroud Dimensions

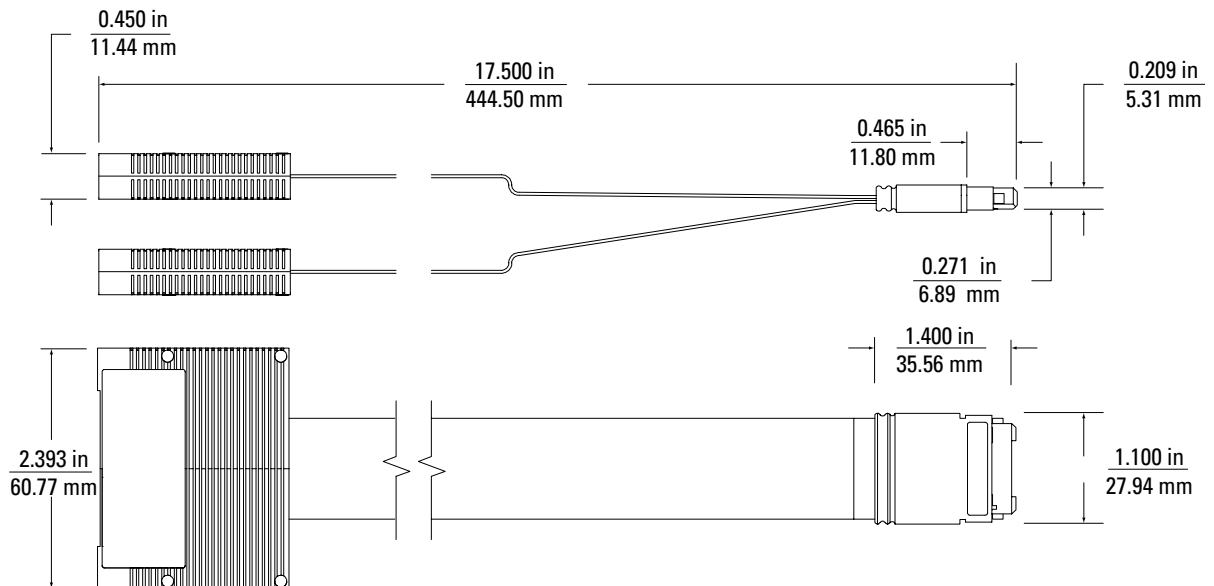


Figure 14. High-Density Termination Adapter Cable Dimensions

Pinout Information on Required Signals for Inverse Assembly

This table describes the connections for the four Mictor 38 connectors necessary for compatibility with the inverse assembler and the E5346A high-density termination adapter cables. This is intended to be a guide for placing probing connectors on a target system.

For inverse assembly, the J1, J2, J3, and J4 connectors listed below must be connected through the four high-density adapter cables. For simultaneous state and timing analysis for all signals, additional connectors must be used.

| Mictor Conn. # | AMP Mictor Pin# | Signal Name | Mictor Conn. # | AMP Mictor Pin # | Signal Name |
|----------------|-----------------|-------------|----------------|------------------|-------------|
| J1 (odd) | 38 | A31(LSB) | J1 (even) | 37 | A15 |
| | 36 | A30 | | 35 | A14 |
| | 34 | A29 | | 33 | A13 |
| | 32 | A28 | | 31 | A12 |
| | 30 | A27 | | 29 | A11 |
| | 28 | A26 | | 27 | A10 |
| | 26 | A25 | | 25 | A9 |
| | 24 | A24 | | 23 | A8 |
| | 22 | A23 | | 21 | A7 |
| | 20 | A22 | | 19 | A6 |
| | 18 | A21 | | 17 | A5 |
| | 16 | A20 | | 15 | A4 |
| | 14 | A19 | | 13 | A3 |
| | 12 | A18 | | 11 | A2 |
| | 10 | A17 | | 9 | A1 |
| | 8 | A16 | | 7 | A0 |
| | 6 | SYSCLK | | 5 | |
| J2 (odd) | 38 | ABB | J2 (even) | 37 | DBB |
| | 36 | ARTRY | | 35 | TS |
| | 34 | QREQ | | 33 | SRESET |
| | 32 | AACK | | 31 | TEA |
| | 30 | BG | | 29 | TA |
| | 28 | DBG | | 27 | DRTRY |
| | 26 | DBWO | | 25 | INT |
| | 24 | GBL | | 23 | TT4 |
| | 22 | CI | | 21 | TT3 |
| | 20 | WT | | 19 | TT2 |
| | 18 | | | 17 | TT1 |
| | 16 | | | 15 | TT0 |
| | 14 | BR | | 13 | TBST |
| | 12 | CKSTP_OUT | | 11 | TSIZ2 |
| | 10 | CKSTP_IN | | 9 | TSIZ1 |
| | 8 | HRESET | | 7 | TSIZ0 |
| | 6 | QACK | | 5 | |

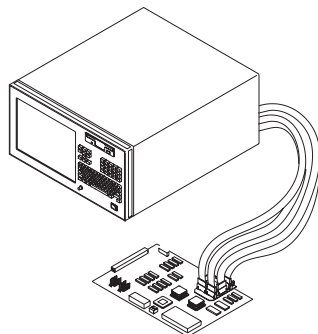
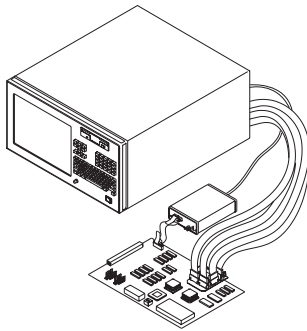
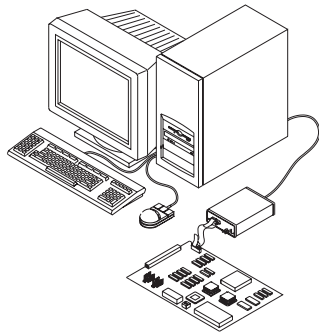
| Mictor Conn. # | AMP Mictor Pin# | Signal Name | Mictor Conn. # | AMP Mictor Pin # | Signal Name |
|-------------------|--------------------|-------------|-------------------|---------------------|-------------|
| J3 (odd) | 38 | DL31(LSB) | J3 (even) | 37 | DL15 |
| | 36 | DL30 | | 35 | DL14 |
| | 34 | DL29 | | 33 | DL13 |
| | 32 | DL28 | | 31 | DL12 |
| | 30 | DL27 | | 29 | DL11 |
| | 28 | DL26 | | 27 | DL10 |
| | 26 | DL25 | | 25 | DL9 |
| | 24 | DL24 | | 23 | DL8 |
| | 22 | DL23 | | 21 | DL7 |
| | 20 | DL22 | | 19 | DL6 |
| | 18 | DL21 | | 17 | DL5 |
| | 16 | DL20 | | 15 | DL4 |
| | 14 | DL19 | | 13 | DL3 |
| | 12 | DL18 | | 11 | DL2 |
| | 10 | DL17 | | 9 | DL1 |
| | 8 | DL16 | | 7 | DL0(MSB) |
| | 6 | | | 5 | DBDIS |
| J4 (odd) | 38 | DH31(LSB) | J4 (even) | 37 | DH15 |
| | 36 | DH30 | | 35 | DH14 |
| | 34 | DH29 | | 33 | DH13 |
| | 32 | DH28 | | 31 | DH12 |
| | 30 | DH27 | | 29 | DH11 |
| | 28 | DH26 | | 27 | DH10 |
| | 26 | DH25 | | 25 | DH9 |
| | 24 | DH24 | | 23 | DH8 |
| | 22 | DH23 | | 21 | DH7 |
| | 20 | DH22 | | 19 | DH6 |
| | 18 | DH21 | | 17 | DH5 |
| | 16 | DH20 | | 15 | DH4 |
| | 14 | DH19 | | 13 | DH3 |
| | 12 | DH18 | | 11 | DH2 |
| | 10 | DH17 | | 9 | DH1 |
| | 8 | DH16 | | 7 | DH0(MSB) |
| | 6 | | | 5 | |
| J5 (odd) | 38 | PLL_CFG3 | J5 (even) | 37 | DP7 |
| | 36 | PLL_CFG2 | | 35 | DP6 |
| | 34 | PLL_CFG1 | | 33 | DP5 |
| | 32 | PLL_CFG0 | | 31 | DP4 |
| | 30 | LSSDMODE | | 29 | DP3 |
| | 28 | | | 27 | DP2 |
| | 26 | | | 25 | DP1 |
| | 24 | | | 23 | DP0 |
| | 22 | | | 21 | TLBISYNC |
| | 20 | | | 19 | TBEN |
| | 18 | SMI | | 17 | RSRV |
| | 16 | MCP | | 15 | |
| | 14 | AP3 | | 13 | |
| | 12 | AP2 | | 11 | |
| | 10 | AP1 | | 9 | L2_TSTCLK |
| | 8 | AP0 | | 7 | L1_TSTCLK |
| | 6 | | | 5 | |

System Configuration and Ordering Information

The table below shows the system components you need to order and what is included in each. The solution product numbers do not

include logic analysis. The 16700A Series logic analysis systems must be ordered separately. If you want to configure or

upgrade your system with individual products, see page 18 for individual product number information.



| Solution | Products to Order | Included Components |
|---|--|--|
| JTAG Emulation | | |
| • PPC 7XX Emulation Probe | • E5901B #070 | |
| • Debugger Connection | • Order directly from Green Hills, Microtec, SDS, or WindRiver | |
| Emulation Solution with Real-Time Trace | | |
| • 16700A Series Logic Analysis System | • Refer to publication number 5966-3148E for logic analyzer configuration • Contact your Agilent field engineer for latest logic analyzer information | |
| • Emulation Using Mictor Probing | • E9486B #001 | • Inverse Assembler • Source Correlation Tool Set • Emulation Module |
| | • Four E5346B High-Density Termination Adapters • E5346-68701 Mictor Connector Kit | |
| • Debugger Connection | • Order directly from Green Hills, Microtec, SDS, or WindRiver | |
| • Optional System Performance Analysis Tool Set | • B4600B | |
| Logic Analysis Solution | | |
| • 16700A Series Logic Analysis System | • Refer to publication number 5966-3148E for logic analyzer configuration • Contact your Agilent field engineer for latest logic analyzer information | |
| • Logic Analysis Solution Using Mictor Probing | • E9586A #001 • Four E5346A High-Density Termination Adapters • E5346-68701 Mictor Connector Kit | • Inverse Assembler |
| • Optional Source Correlation Tool Set | • B4620B | |
| • Optional System Performance Analysis Tool Set | • B4600B | |
| • Optional Emulation Module | • E5901B #070 | |

Individual Components Ordering Information

| Description | Agilent Product |
|---|-------------------|
| Emulation Probe | E5900B #070 |
| Emulation Module | E5901B #070 |
| Inverse Assembler | E9586A #001 |
| Emulation Module and Emulation Probe Migration | E5902B #070 |
| Source Correlation Tool Set | B4620B |
| System Performance Analysis Tool Set | B4600B |
| High-Density Termination Adapter | E5346A |
| Mictor Connector Kit | E5346-68701 |
| High-Density Right Angle Adapter | E5346-63201 |
| High-Density Termination Adapter Support Shroud | E5346-44701 |
| AMP Mictor Connector (order from AMP) | AMP PN 2-767004-2 |

Training and Consulting

Agilent Technologies has experienced Digital Systems Consultants who can help you maximize the use of your emulation and analysis system through training and consulting. Digital Systems Consultants are experienced in debugging complex digital hardware/software problems and hardware/software integration.

Training can be delivered through scheduled courses, on-site classes, or one-on-one consulting. Agilent Technologies has courses for the beginner as well as advanced users migrating from the Agilent 16500 Series systems. Call 1-800-593-6632 in the U.S. for information about training schedules and location or to register. For training offered in other countries and languages, consult the Test and Measurement education web site: <http://www.hp.com/go/tmeducation>

For consulting services, contact your local Test and Measurement sales office. A digital systems consultant can help you solve tough digital debug problems by showing you how to apply Agilent Technologies tools and debug best practices. Topics covered can include:

- System Installation
- Complex Triggering
- Multiple Bus Analysis
- Source-Line Referencing
- System Performance Analysis
- Instrumenting Code to Solve Specific Issues
- Bus Signal Timing Analysis
- Signal Integrity Analysis
- 16700A/1660XA Networking

Topics related to the debug of PowerPC 740/750 microprocessor-based targets can include:

- Instruction/Data Cache Issues
- Checkstop Analysis
- Single and Multiple Beat Bus Cycles
- Pipelining and Bursts

Ordering Information

www.agilent.com

Related Literature

Pub. Number

*HP 16600A and 16700A Series Logic Analysis
System Mainframes, Product Overview*

5966-3107E

*Processor and Bus Support for Agilent Technologies
Logic Analyzers, Configuration Guide*

5966-4365E

Probing Solutions for HP Logic Analysis Systems

5968-4632E

Product Warranty

Agilent Technologies hardware products are warranted against defects in materials and workmanship for a period of one year from date of shipment. Some newly manufactured Agilent Technologies products may contain remanufactured parts, which are equivalent to new in performance. If you send notice of defects during the warranty period, Agilent Technologies will either repair or replace hardware products that prove defective.

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(tel) 1 800 452 4844

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L4W 5G1
(tel) 1 877 894 4414

Europe:

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Test & Measurement
European Marketing Organisation
P.O. Box 999
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Japan:

Agilent Technologies Japan Ltd.
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(fax) (81) 426 56 7840

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