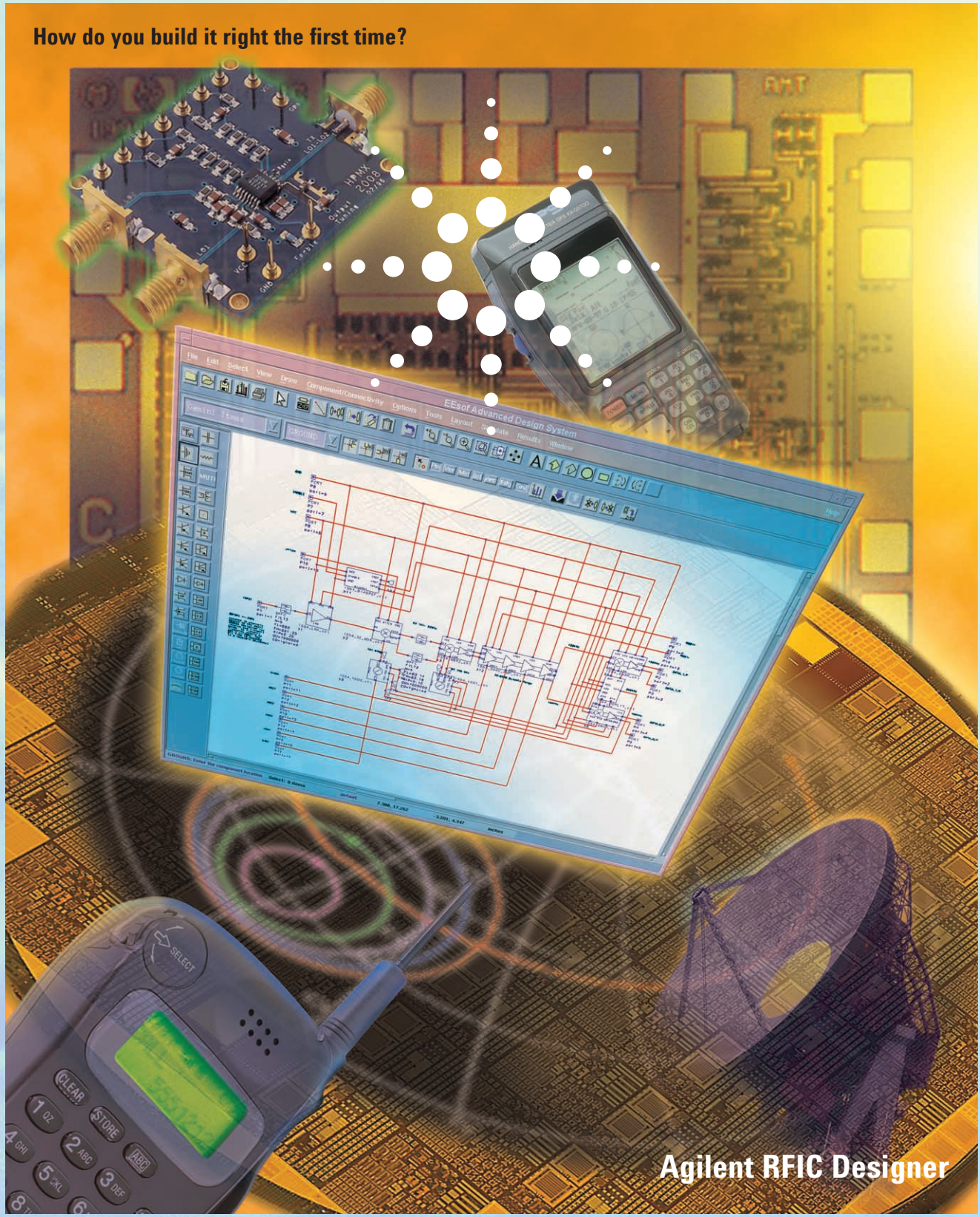
Agilent EEsof EDA Design Technology

How do you build it right the first time?



Agilent RFIC Designer

Agilent Technologies

The Genesis of RFICs

Consumer and commercial demands for wireless communications continue to grow at an amazing rate—not only in product quantity, but in product quality: powerful features, wider range, smaller size, lighter weight, longer battery life, and lower cost. Furthermore, the need for mobile connectivity for portable communications has led to spectrum congestion and has driven wireless communications to higher frequencies.

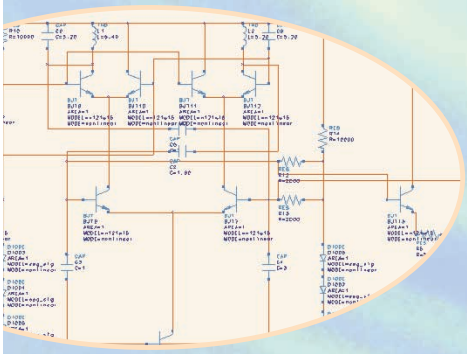
Designing in the Competitive Marketplace

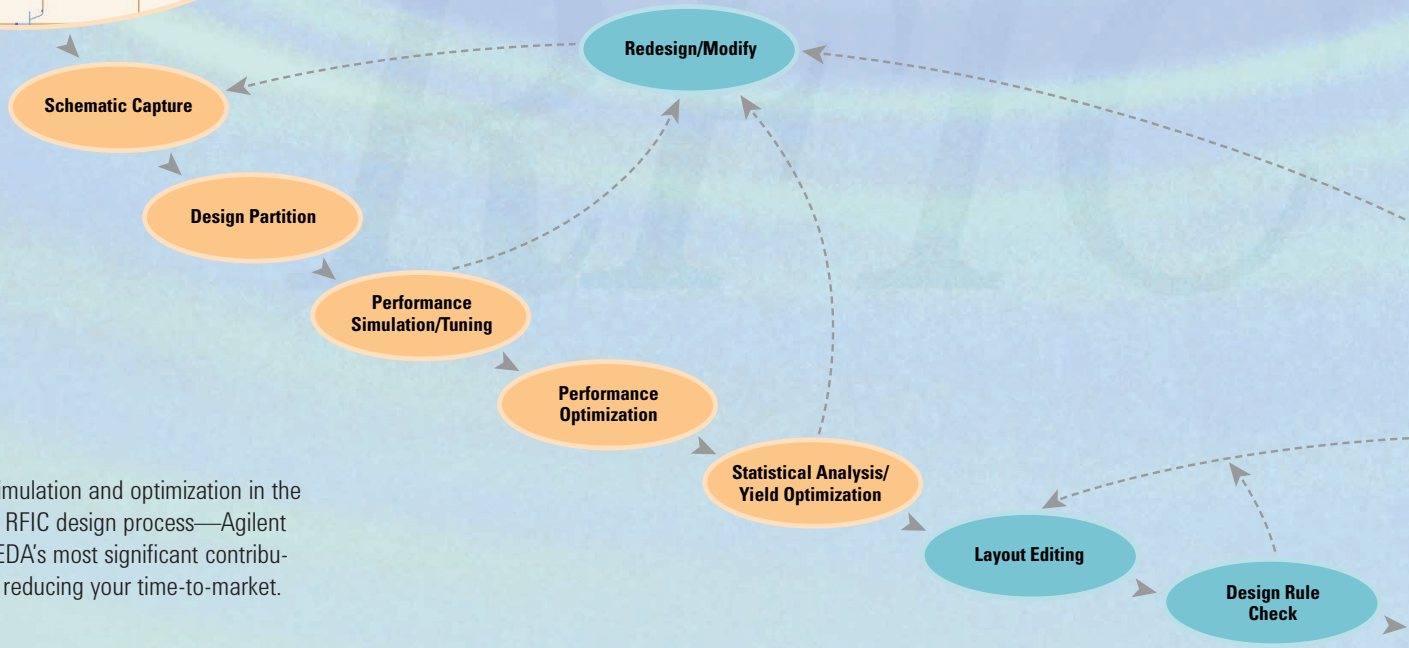
To meet increasing technical challenges, manufacturers have turned to digital communications and radio frequency integrated circuit (RFIC) technology.

Higher carrier frequencies, coupled with complex digital RF modulation schemes, have spawned a new generation of integrated chips for building advanced wireless communications products. RFICs are used in everything from pagers and cellular phones to wireless LANs and global positioning systems.

Maximum Performance and High Yield

The boom in wireless communications has created a critical demand for RFICs. However, most design tools are overwhelmed by new circuit design complexity and time-to-market requirements. To be cost- and time-efficient, design engineers must accurately simulate the performance of RFIC circuits before committing them to prototyping or production. With superior RFIC simulation capabilities, designers can create circuits with optimal performance and yield.





RFIC simulation and optimization in the overall RFIC design process—Agilent EEsof EDA's most significant contribution to reducing your time-to-market.

Solutions Developed from Experience

Hewlett-Packard pioneered high-frequency simulation in the 1960s and Agilent Technologies continues to design, fabricate, and test RFICs at our in-house silicon and GaAs (gallium arsenide) foundries. As the leading developer of RF simulation technologies, Agilent EEsof EDA is uniquely positioned to provide the most advanced RFIC design solutions. Backed by extensive in-house RFIC design experience, Agilent understands why it's important to build it right the first time.

RFIC Designer offers the most comprehensive set of simulation tools and models for accurately verifying performance and yield of the RFIC design before initiating costly prototype wafer fabrication runs.

Increasing Accuracy and Reducing Design Time

By eliminating just one RFIC prototype cycle, time-to-market can be shortened by two to three months. However, designing successful RFICs requires much more than just fast design turnaround. Obtaining simulation results early in the design process is critical to success. Building customer evaluation boards to demonstrate a finished RFIC chip can offer a competitive advantage; however, this task must be factored into the design time projection.

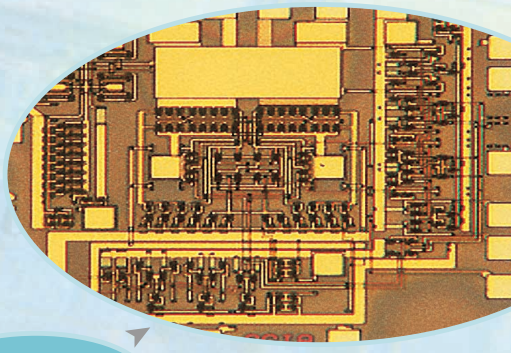
Further adding to the rigors of RFIC design, many products must also perform under different international wireless standards, such as those for digital or analog cellular phones and wireless LANs. And spectrum congestion continues to force RFIC applications to ever higher frequencies, taxing existing design tools and skills.

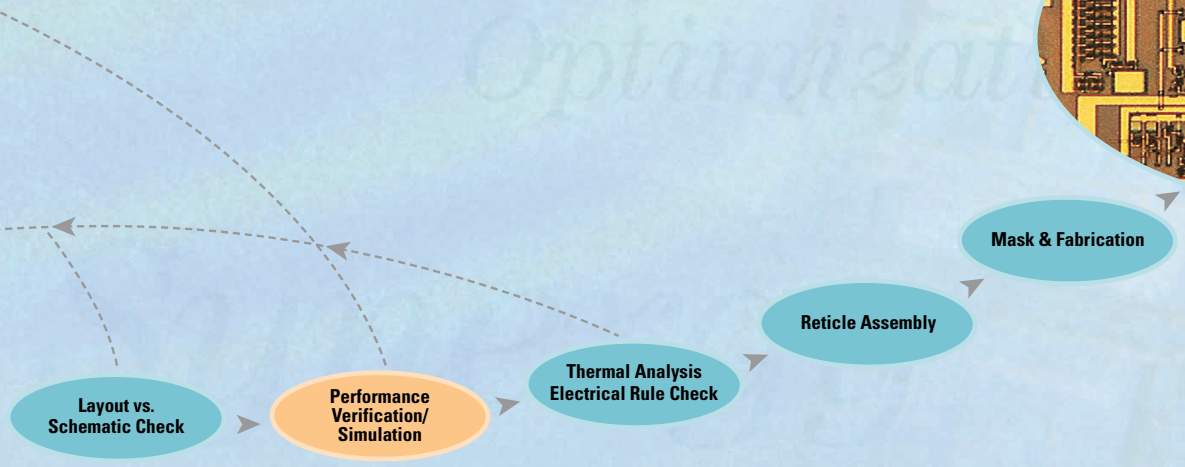
In today's market, designers can't afford the time or expense of even one failed prototype run. RFIC Designer enables engineers to efficiently design RFICs with high performance and yield for capitalizing on market opportunities.

The RFIC Design Process

The RFIC design process can be broadly divided into two primary areas: schematic capture, design simulation and optimization; and layout, verification, and mask making.

RFIC design solutions from Agilent EEsof EDA focus on the early stages of the design simulation and optimization. By obtaining the most accurate RFIC simulations early in the design process, your design can quickly meet both performance and yield requirements.





Simulation Technologies Working in Synergy

Typical RFICs are composed of diverse building blocks, such as low-noise amplifiers (LNAs), mixers, oscillators, phase-locked loops (PLLs), power amplifiers, and automatic level control (ALC) loops. Designing circuits for the different functional blocks requires different simulation technologies to obtain the necessary accuracy within realistic simulation times.

A successful RFIC design solution depends on the synergistic combination of five different simulation technologies operating in the time, frequency, and hybrid frequency-time domains.

Time-Domain Simulation

Transient (SPICE)

Transient simulation is useful for analyzing low-frequency or digital circuits without frequency translation, such as up- or down-conversion. It is effective for verifying the operation of large circuits with thousands of devices. However, when dealing with digitally modulated RF signals found in today's RFIC applications, its simulations may be slow, making it a less suitable design tool.

Convolution

Extending transient simulation, convolution technology uses accurate frequency-domain models or measured S-parameter data instead of lumped components to account for dispersion and skin effects. These effects become significant as spectrum congestion forces RFIC applications to ever-higher frequencies.

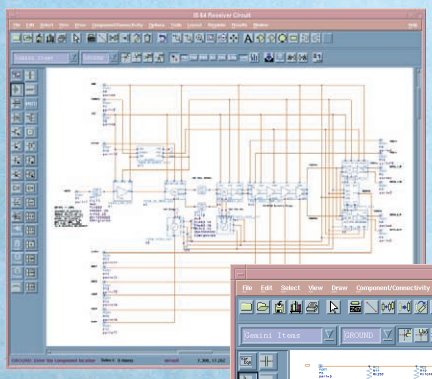
Frequency-Domain Simulation

S-Parameter Simulation

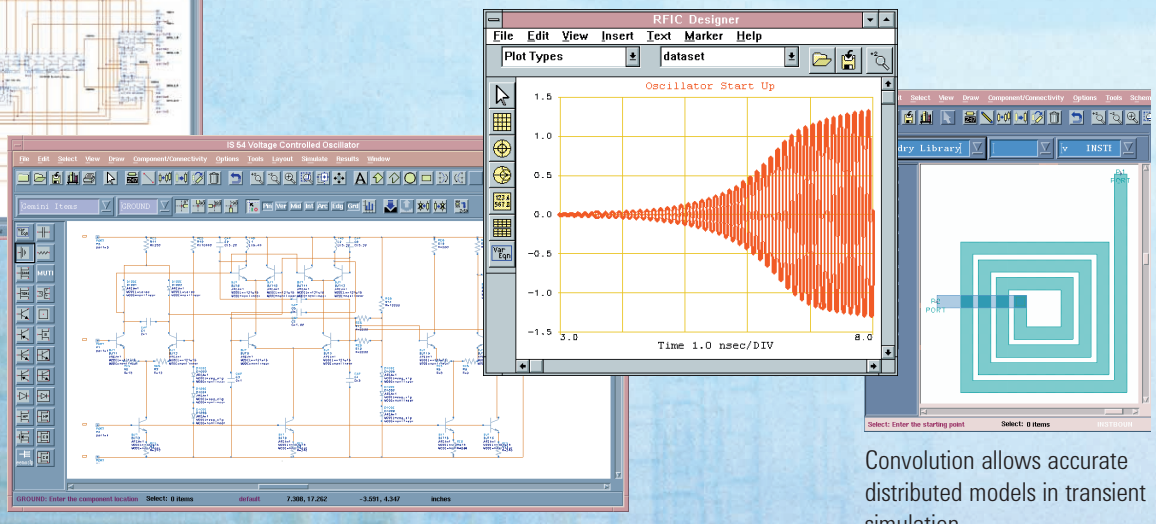
S-parameter simulation provides unmatched design insights when analyzing and optimizing RF low-noise amplifiers, matching networks, and small-signal oscillators.

Harmonic Balance

Harmonic balance simulates the steady-state response of nonlinear circuits, which is useful for mixers, oscillators, and power amplifiers. It analyzes and effectively optimizes mixer 3rd-order intermods, conversion noise figures, oscillator phase noise, amplifier compression, and power-added efficiency.



Transient simulation verifies large circuit operation.

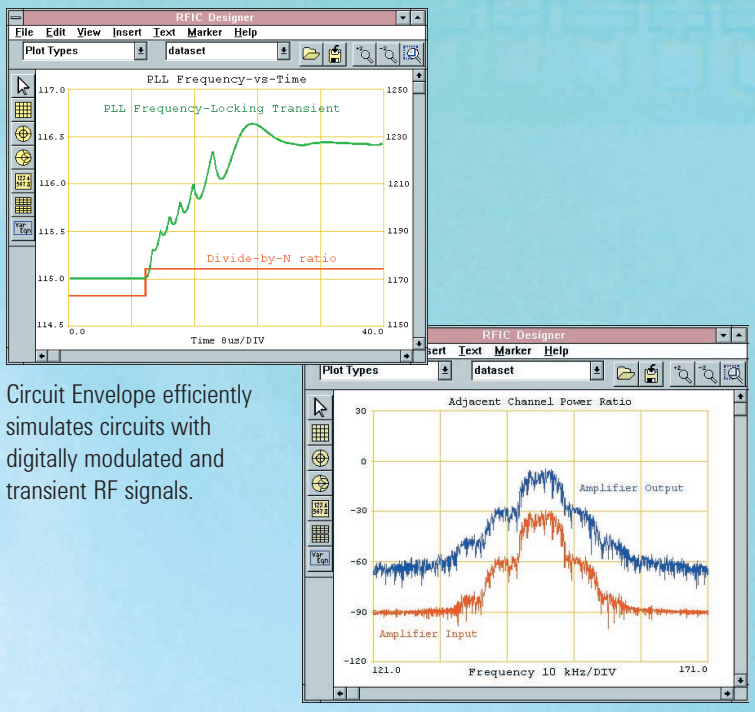


Convolution allows accurate distributed models in transient simulation.

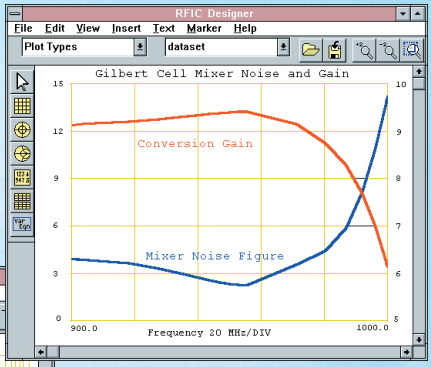
Hybrid Frequency-Time-Domain Simulation

Circuit Envelope

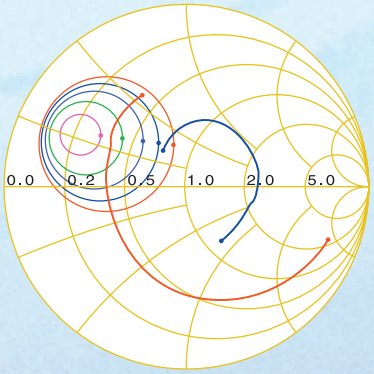
Agilent EEsof EDA developed Circuit Envelope technology to efficiently simulate today's digitally modulated RF wireless signals. It predicts digital wireless specifications, such as transmitter amplifier adjacent channel power, error-vector-magnitude, mixer 3rd-, 5th-, and 7th-order intermods, and PLL frequency lock times. These performance measures can be directly verified against international wireless cellular standards, such as NADC, GSM, and PDC. Such simulations would have been extremely difficult or impossible with any other technology.



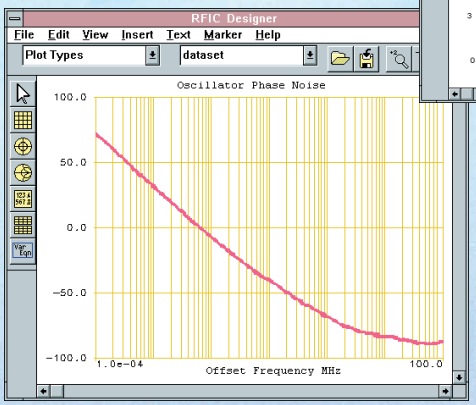
Circuit Envelope efficiently simulates circuits with digitally modulated and transient RF signals.



Harmonic balance accurately analyzes power amplifiers, mixers, and oscillator phase noise.



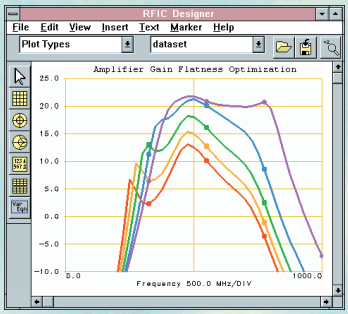
S-parameter analysis speeds low-noise amplifier and matching network designs.



Advanced Design Analysis for Maximizing Product Performance

Performance Optimization

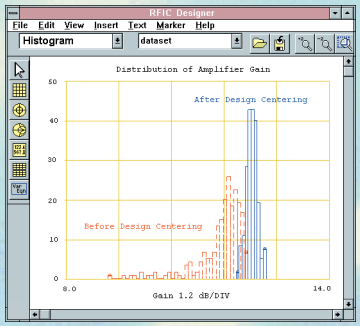
Using proven circuit optimization algorithms, designers can extract the maximum performance from an RFIC design. Frequency-domain simulators optimize more efficiently because they simulate the circuit at critical, specified frequencies only. By contrast, time-domain simulators must analyze multiple time-points to derive the same performance goals.



Optimization technologies extract the maximum performance from your RFIC designs.

Statistical Analysis and Yield Improvement

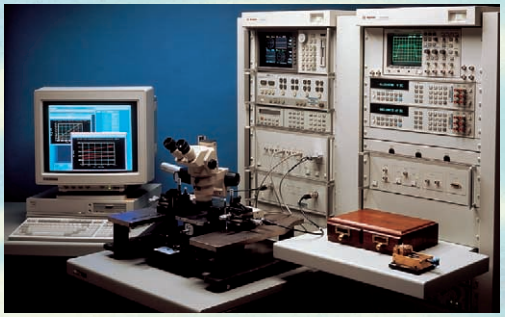
Predicting the effects of production tolerances on RFIC yield during the design stage helps to eliminate costly delays to fix production yield deficiencies. Agilent EEsof EDA pioneered statistical analysis and yield optimization in EDA tools to allow designers to locate potential yield problems and to reduce the impact of yield-sensitive parameters by changing tolerances, nominal values, or circuit topology.



Statistical design techniques ensure RFICs with better yield.

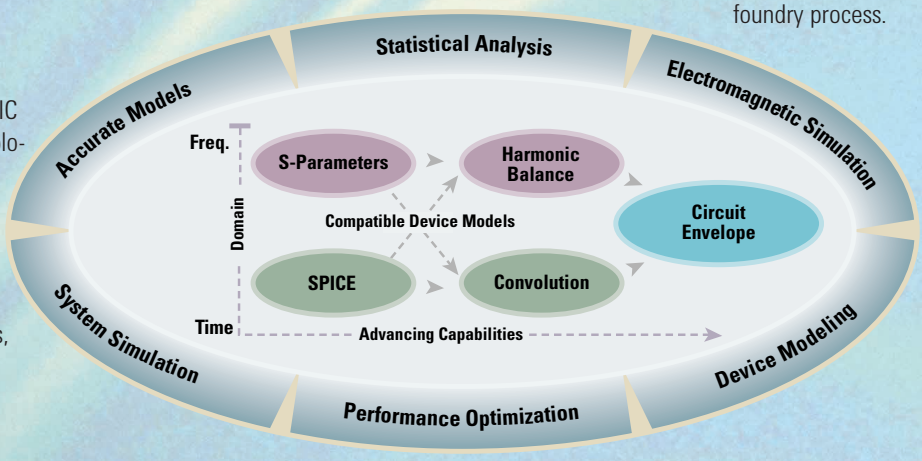
Accurate Models and Device Modeling

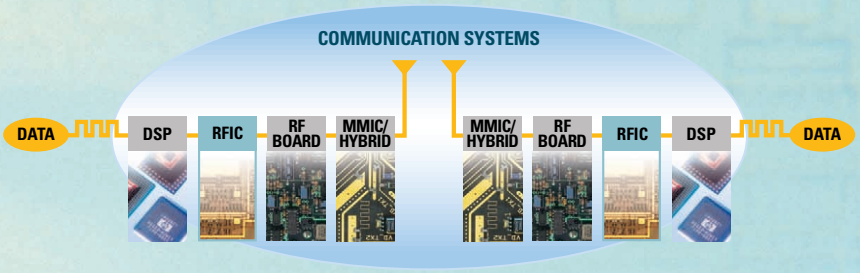
Simulators are only as accurate as the models they use. Agilent EEsof EDA has developed the largest library of accurate frequency-domain distributed models. They account for dispersion and skin effects at higher RF frequencies, which are ignored by lumped models used in typical SPICE simulators. User-defined behavioral models for custom foundry processes can also be created and accurately fitted to measured data with a parameter extraction system.



Our device modeling system employs industry-proven RF extraction methodologies to obtain the most accurate active device models for your foundry process.

Powerful core RFIC simulation technologies are further strengthened by complementary capabilities in optimization, statistical analysis, and modeling.

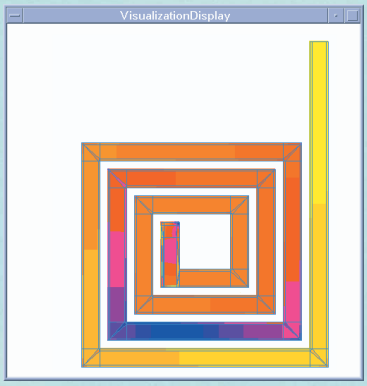




RFIC Designer is part of the Agilent Advanced Design System, which lets you simulate the entire communications signal path from input bits to output bits—with powerful tools for RFIC, DSP, RF board, MMIC/hybrid, communications systems, and planar EM—all in a single design environment.

Electromagnetic Simulation

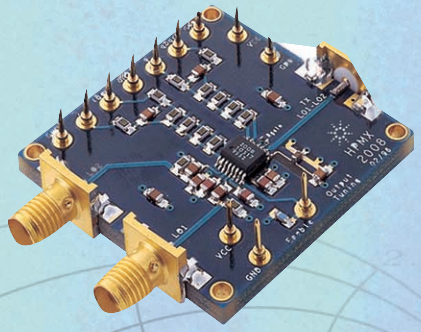
Electromagnetic simulation maintains simulation accuracy when analytical models are unavailable or used beyond their range of validity. Applications include: modeling spiral inductors on silicon, RFIC package parasitics, and interconnects on RF multi-chip modules.



Electromagnetic simulation accurately models RF spiral inductors on silicon substrates.

System Simulation and DSP

Through system simulation, system architects can properly partition the design before assigning detailed RFIC design tasks to individual engineers. Designers can analyze complete systems including circuit-level and system behavioral blocks representing RF, DSP (digital signal processing), baseband digital, and analog sections. Applications include: analyzing RF and DSP interactions within RFIC chipsets, and how RFIC chipsets work with off-chip components in an evaluation board or multi-chip module (MCM). By examining design trade-offs among the RFIC and DSP building blocks, costly over-designs can be avoided.



Support and Solution Services

Getting the Most from Your Design Software

Agilent EEsof EDA is committed to ensuring an optimum return on your investment in EDA tools with timely training and support for new and expert users worldwide. Our dedicated consulting services provide custom solutions to integrate our state-of-the-art design technologies into your current design process.

In addition, we'll help you set up the most effective design environment for your needs, including links to leading EDA frameworks such as those from Mentor Graphics and Cadence; customization of model libraries and user interfaces; and re-use of existing designs through SPICE netlist translations.

Agilent EEsof EDA's commitment to intensive research and development helps protect your long-term investment. Building upon your current design tools, we deliver timely upgrades and new product offerings as we make ongoing technology advancements that are in sync with the needs of the RFIC industry.

Product Design Suites

RFIC Designer combines leading edge high-frequency simulation and optimization technologies with accurate models in dedicated design packages tailored for RFIC designers. These cost-effective solutions are available in both node-locked and network-licensed configurations on PC and UNIX systems.

	Model Numbers
RFIC Designer Pro	**E8888A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
SPICE Netlist Translator	E8880A/AN
Linear Simulator	E8881A/AN
Harmonic Balance Simulator	E8882A/AN
Circuit Envelope Simulator	E8883A/AN
High-Frequency SPICE	E8884A/AN
RFIC Designer Premier	**E8889A/AN**
Design Environment	E8900A/AN
Data Display	E8901A/AN
SPICE Netlist Translator	E8880A/AN
Linear Simulator	E8881A/AN
Harmonic Balance Simulator	E8882A/AN
Circuit Envelope Simulator	E8883A/AN
High-Frequency SPICE	E8884A/AN
Convolution Simulator	E8885A/AN
RF System Models	E8854A/AN
Analog Model Development Kit	E8890A/AN
SPICE Model Generator	E8891A/AN
Statistical Design	E8824A/AN

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Phone or Fax
United States:
(tel) 1 800 452 4844

Canada:
(tel) 1 877 894 4414
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(fax) (31 20) 547 2390

Japan:
(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Korea:
(tel) (82 2) 2004 5004
(fax) (82 2) 2004 5115

Latin America:
(tel) (305) 269 7500
(fax) (305) 269 7599

Taiwan:
(tel) 080 004 7866
(fax) (886 2) 2545 6723

Other Asia Pacific Countries:
(tel) (65) 375 8100
(fax) (65) 836 0252
Email: tm_asia@agilent.com

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Agilent Technologies