Agilent 81250

Flat Panel Display Link Test

Product Note

The Device

With every technology cycle, the data rate between graphics controller and LCD driver increases, to accommodate the increasing number of pixels (VGA->XGA->SVGA). This implementation of TX and RX chip-set has to handle a data transmission of 1.8 Gbps.

EMI, layout, and power problems caused by a fast parallel architecture, have been overcome by faster serial interconnection between TX and RX chip.

Four serial links, working at 450 MBit, transfer color and luminescence information between Host Graphics Controller and LCD Panel Driver.

TX and RX chip functionality is mainly to multiplex /de-multiplex parallel to serial and vice versa. A specialty of this device type is:

- the 1 to 7 parallel to serial relation,
- the serial interface uses LVDS technology, (LVDS =low voltage differential signal), typ 250mV amplitude.

The Test

Verify the Bit Error Rate (BER) of 1-serial to 7-parallel Rx chip. In order to make the Bit Error Rate measurement on the RX chip, the device needs to be stimulated with PRBS (Pseudo Random Binary Sequence) at 450 MHz. The PRBS meets standards set by the IEEE and ITU. PRWS (Pseudo Random Word Sequence) has to be used on the analyzer side. This is a demultiplexed PRBS into 7 channels. The PRBS bits are assigned bit by bit (1 to 7) to the parallel lines, while bit 1, 8, 15, ... go to channel 1 and so on. The compare on the analyzer runs 7 times slower on the parallel lines.

The device needs a 65 MHz clock, which represents the device frequency on the parallel side. As the stimulus signals run at 450 MHz, this clock is generated from NRZ data.

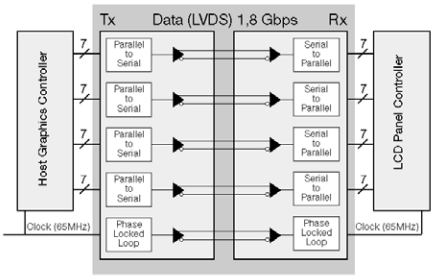

Figure 1: LCD Display Driver (LVDS) Chip Set

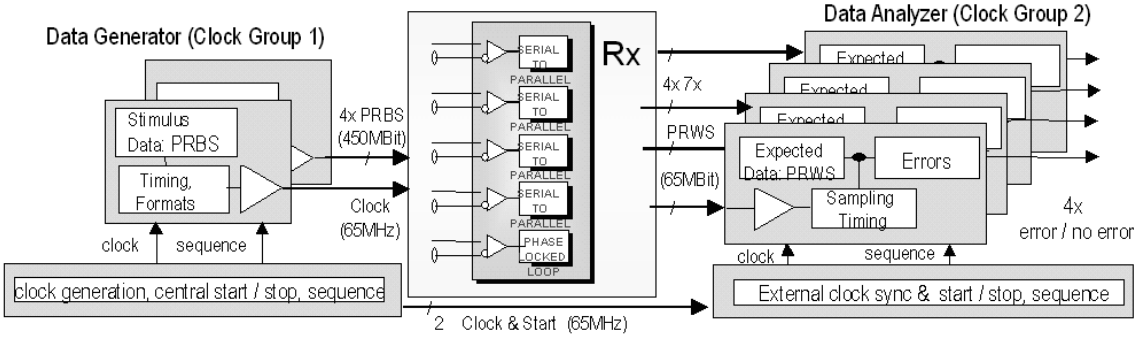

Figure 2: Data Generator and Analyzer Setup

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There are two ways to do that:

- constant average ac level: 4x ‘1’ and 3x ‘0’ is followed by 3x ‘1’ and 4x ‘0’ (-> better for ac coupled input)
- constant duty cycle: repetition of either 1110000 or 1111000 (-> better for a dc coupled input).

Data Generator & Analyzer Setup, according to Figure 2:

- Vector data: generator uses PRBS, analyzer uses PRWS
- Timing and level: LVDS, which requires quite small amplitudes on the generator channels as well as high sensitivity for the small signals applied to the test system receivers
- Sequencing: PRBS and PRWS will run infinitely or at least for quite a while to ensure that sufficient bits have been transferred for verification of a BER to be less than 10^-10 or better

The different frequencies used for stimulation and analysis need two clock groups on the test system: the generator will run at 450 MBit, while the analyzer compares at 65 MBit.

For synchronization of the analyzer, the generator feeds two signals to the analyzer part: Clock and Start. These are in addition to the stimulus signals running to the DUT.

To obtain synchronous data analysis, the generator sequencing must provide a test start according to the ‘TEST Flow’ diagram, shown in Figure 3. Once the clocks start, the device’s PLL and the analyzer clock group begin to work. When they are settled, the ‘Start’ signal initializes the generation of expected data. This has to be done in advance of stimulus data to compensate analyzer latency. When that's completed, the stimulus PRBS data is applied and the compare against PRWS in the analyzer can take place. The latency through the DUT is compensated by programming the sampling point delay.

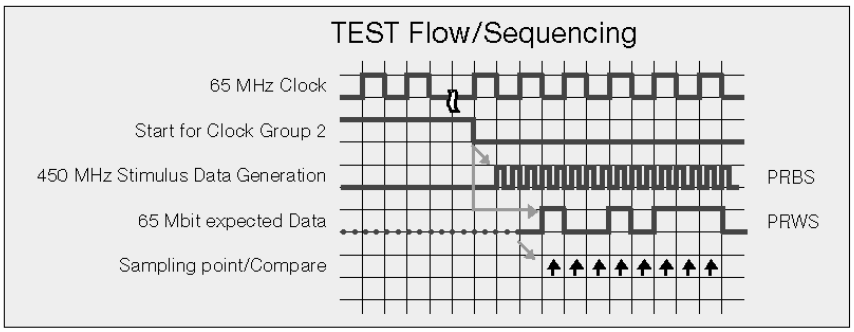

Figure 3: Data Sequencing

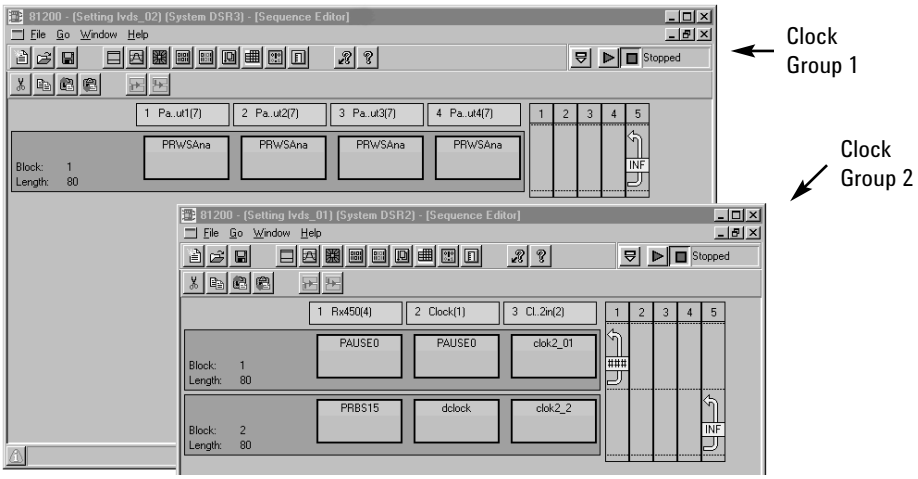

Figure 4: Sequencing Program for Clock Group 1 & 2

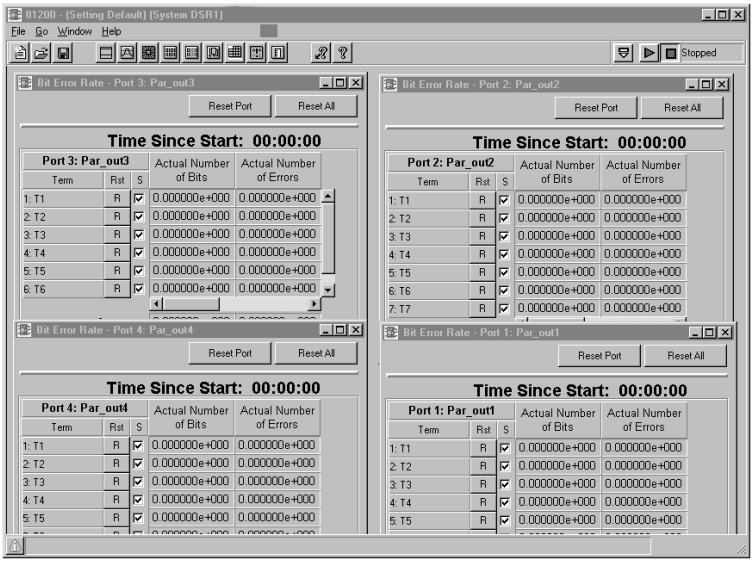

Figure 5: Error Rate Display

Tester Setup Overview

Clock Group 1 provides 7 stimulus channels, 5 for driving the DUT and 2 for synchronization of the analyzer.

Clock Group 2 provides 28 analyzer channels for the 4 times 7 parallel lines.

Figure 4 shows the sequencer programming for the two clock groups. System 2: waits for start signal from system 1.

Analyzers are set to do BER in PRWS mode for the 4 parallel ports.

System 1: Block 1 generates clocks to get the DUT & System 2 working. The 2nd block sends the “Start” signal block sends the “Start” signal to system 2 and generates the PRBS data stream.

Block Length: this specifies the number of bits processed. On system 1 the block length has to be 7 times larger as on system 2 as it works 7 times faster.

The result is given as Bit Error Rate (BER) display, which is measured and displayed per port. Each port is represented in a separate window.

All 4 ports are shown above, in Figure 5.

Summary

The description focuses on a solution using 2 clock groups, which makes efficient use of the PRWS feature on the parallel side of the DUT. It should be added, that a test is possible also just with one clock group. In this case the DUT outputs will be sampled 7 times faster as they change the data. Expected data cannot be obtained from the built in PRWS feature. But with help of acquisition from a golden device or by use of ‘BestLink 81200’ the expected data may be obtained from simulation. This product note focuses on LVDS devices with LVDS inputs and outputs down to amplitudes of 250mV. Should smaller amplitudes be required, consult your local sales representative.

Related Literature	Pub. Number
Need to Test BER?, Brochure	5968-9250E
Agilent ParBERT 81250, Mux/Demux Application, Application Note	5968-9695E
Agilent ParBERT 81250, Parallel Bit-Error-Rate Tester, Product Overview	5968-9188E
Agilent ParBERT 81250, Parallel Bit-Error-Rate Tester, Configuration Guide	5968-9189E

For more information, please visit us at: www.agilent.com/find/parbert

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