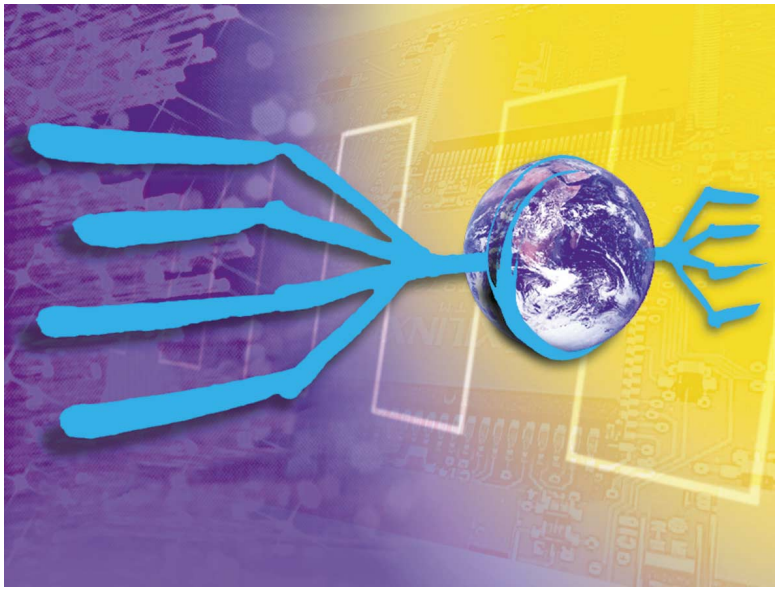
Agilent 81250

The ParBERT 81250
Parallel Bit Error Ratio Tester

Product Overview
Version 2.0

The Only Parallel Bit Error Ratio Solution up to 2.67 Gbit / s



Agilent Technologies

Agilent ParBERT 81250

Agilent ParBERT 81250 is a modular parallel bit-error-ratio test solution which works up to 2.67 Gbit/s. The system generates pseudo random word sequences (PRWS), standard pseudo random binary sequences (PRBS) and user-defined patterns on parallel lines. You can analyze bit error ratios with user-defined patterns, PRBS/PRWS or mixed data (a combination of user-defined patterns and PRBS).

ParBERT 81250 is especially suitable for multiplexer and demultiplexer (mux/demux) - or SERDES (serializer/deseralizer) - testing used in telecom and system area network (SAN) ICs, multiple transmitter and receiver testing in manufacturing and forward error correction (FEC) device testing. ParBERT 81250 also provides data and control signals for the DUT if required.

The ParBERT Measurement Software is a ready-to-use package which, offers three different levels of measurement analysis:
1. Fast pass/fail measurements ideal for production

2. Fast setup, hold time and eye opening specification results - no need to calculate values

3. Graphical results for detailed root cause analysis - see trends clearly and fast, e.g. pseudo color and contour plots

Agilent ParBERT 81250 is particularly suitable for the following applications:

Telecom Multiplexer and Demultiplexer Test

OC-768 device testing: You can test 40-gigabit devices back-to-back in parallel using the 81250 ParBERT and a golden device.

OC-48 device testing: You can test up to OC-48 without a golden device using the ParBERT 81250.

To test OC-192 devices without a golden device, the ParBERT can be combined with the 71612B, 12-gigabit-per-second error performance analyzer. The ParBERT 81250 provides thorough testing of devices including taking measurements such as setup and hold times, propagation delay or BER versus temperature.

Characterization of SAN ICs

With ParBERT 81250 you can test SAN-related multiplexers or demultiplexers, including gigabit Ethernet, flat panel display links, Fiberchannel and Infiniband. The ParBERT provides chip control signals, divided or multiple clock signals, 1Mb/s to 2.67Gbit/s operation with proprietary formats as well as LVDS load generation or analysis.

Manufacturing Test of Multiple Transmitters and Receivers

The ParBERT 81250 offers you a scaleable VXI platform ideal for the manufacturing environment. ParBERT is a cost-effective test solution which allows parallel electrical stimulus and/or error detection to increase the throughput in your manufacturing environment.

FEC Device Test

ParBERT 81250 is also an ideal solution for forward error correction (FEC) device test. Verification of FEC devices and circuits is critical in submarine and terrestrial networks. ParBERT allows you to test parallel-to-parallel with memory-based data up to 8 Mbit.

For more information on these applications, please see brochure p/n 5968-9250E.

Key Features Overview

Features	Benefits
NEW: Three different levels of measurement analysis: • Fast pass/fail measurements • Fast clock out to data out (setup and hold times), skew and eye opening specification results • Graphical results for detailed root cause analysis	• Ideal for production departments. Test times now up to 10 times faster Test 2 channels at 2.67Gb/s in under one second. • View the specifications you need e.g. clock out to data out (setup and hold times) – no need to calculate values • See trends clearly and faster, e.g. pseudo color and contour plot
NEW: • Ready-to-use measurements	• Save time when setting up tests with these complete building blocks – no need to program the measurements
NEW: Three different measurements: • Fast eye mask measurement • DUT output timing measurement (includes skew, setup and hold time) • Eye opening	• Gain more insight into your DUTs behavior with these extended measurement functions
• Program remotely via Agilent Vee, National Instruments' LabVIEW®, Excel, Agilent TestExec, C/C++ and Microsoft® VisualBasic.	• Build measurements into your test executive easily
• Generate pseudo random word sequences (PRWS) and standard PRBS up to 2^{31}-1 • Analyze bit error ratios with user-defined data, PRBS or mixed data from parallel ports	• Perform parallel BER measurements - ideal for mux/demux (serializer/deserializer) circuits
• Up to 64 channels	• Configure one system to fit your application needs
• Up to 2.67 Gbit/s	• Address high bandwidth technology • Use a channel to provide/receive control signals to/from your DUT
• Mix of channels (generator/analyzer) and speed classes • Modular and expandable architecture	• Test complex devices with many channels and many frequencies, e.g. mux/demux (SERDES), FEC circuits
• Generate and analyze single-ended, low voltage and differential signals – including true differential	• Test logic technologies e.g. LVDS, ECL, PECL • Generate the necessary signals to do margin tests, emulate frequency and level changes and stress your device as far as possible
• Data generation and analysis with sequencing and looping	• Generate complex sequences that contain memory based (up to 8Mbit) and/or PRBS/PRWS data • Generate data packets with header and payload • React on control signals from the DUT
• Auto phase & auto delay alignment	• Auto alignment of expected data with outcoming data • Save time as you do not need to find the correct sample point manually typically this takes just 100ms, so ideal for manufacturing
• Intuitive Windows-NT® based user software	• "Standard" and "detail" views show you only the parameters you want to see to perform the measurement
• System synchronizes with an external clock of a different speed than internal generator and analyzer	• Test devices with multiple frequencies, e.g. mux/demux (SERDES), FEC circuits
• Each generator or analyzer channel has independent programmable control of voltage levels and timing delay	• Allows thorough device characterization of a wide range of technologies
• Plug and play drivers	• Simplifies measurement setup
• Interrupt-free change of analyzer delay	• Continuous running signals for measurements where changing analyzer delay is needed, e.g. for shmoo plot - no need to resync

Key Features (continued)

Perform Parallel BER measurements up to 2.67 Gbit/s

ParBERT 81250 makes testing of mux/demux (serializer/deserializer) devices easier. Only ParBERT 81250 is able to generate pseudo-random-word sequences (PRWS) on the parallel side and analyze bit-error-ratios with user-defined patterns, PRBS up to 2^{31}-1 or both combined.

The polynomial 2^n-1, the PRBS algorithm and the parallel bus width define PRWS. The bits of the PRWS are assigned to parallel lines and are then multiplexed to form a PRBS (see figure 1).

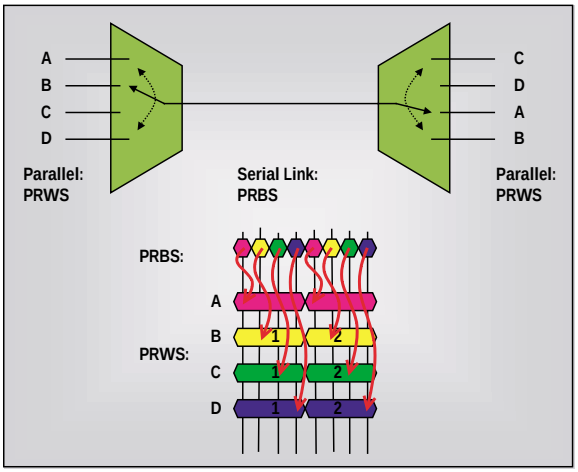


Figure 1: MUX/DEMUX Application: Relationship between PRBS and PRWS

Auto phase and auto delay alignment

As the latency from the input to the output is often not exactly known or it is not deterministic, synchronization between incoming data and outcoming data has to be carried out. ParBERT 81250 has three capabilities to synchronize/align the incoming data automatically (see figure 3):

1) Data shift bit-by-bit if PRBS is used
2) Detect Word if user-defined patterns are used
3) Moving of the sampling point delay of the analyzer up to 10ns without stopping the instrument. Moving of the sampling point delay can be also used in addition to the alignment of data patterns (1 and 2) to refine the synchronization.

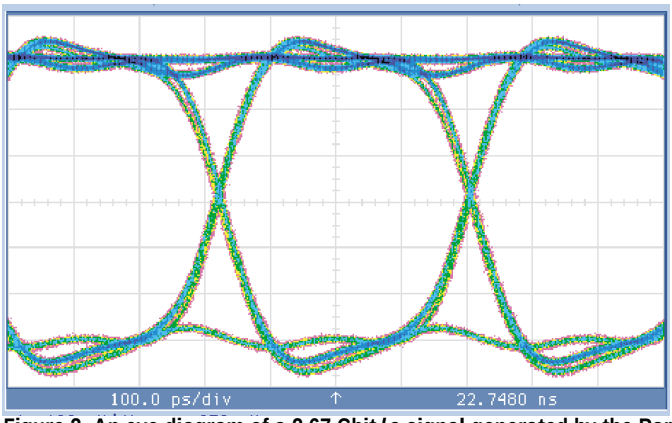


Figure 2: An eye diagram of a 2.67 Gbit/s signal generated by the ParBERT 81250

Interrupt-free change of analyzer delay

The analyzer delay can be changed +/- 1 period whilst the instrument is running without causing it to stop.

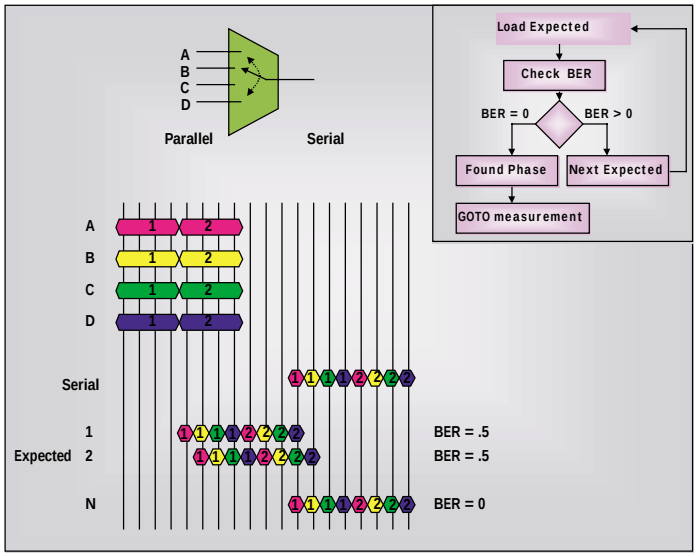


Figure 3: Mechanism of auto-phase and auto-delay assignment

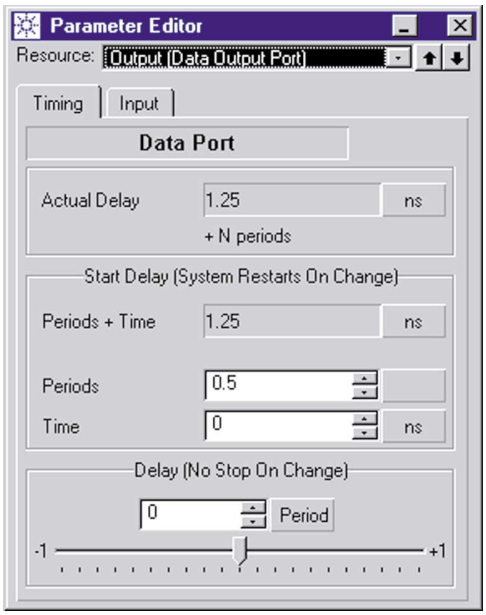


Figure 4: Parameter Editor for analyzer timing

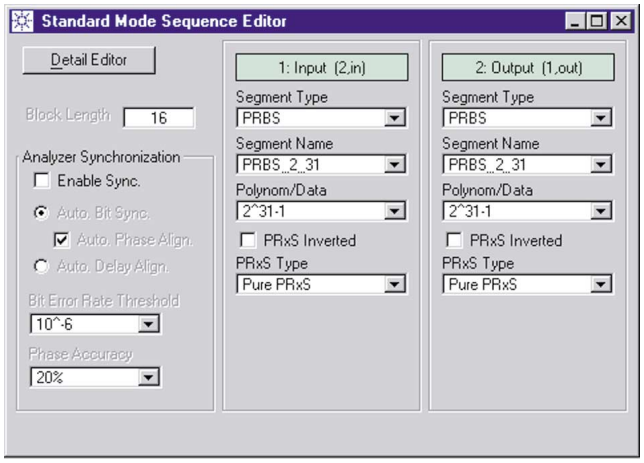


Figure 5: Standard view when choosing PRBS / PRWS patterns and data synchronization mode

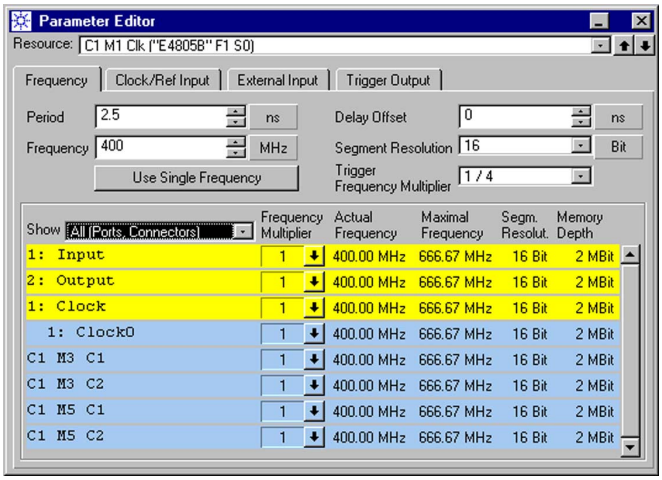


Figure 6: Parameter Editor for setting multiple frequencies

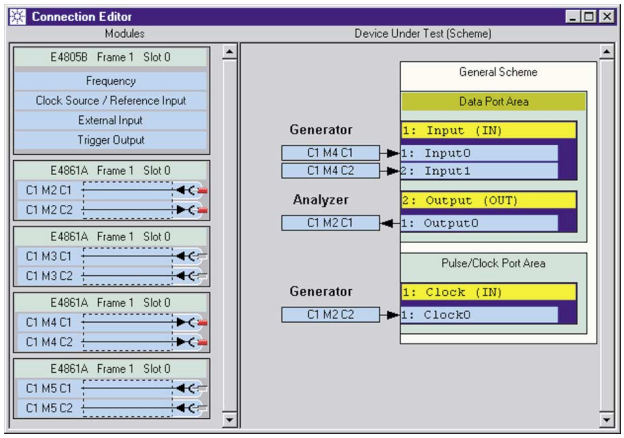


Figure 7: The connection window for setting up measurements

Measurement Software

The ParBERT 81250 measurement software is a ready-to-use measurement user interface, which aids you with the verification and characterization of high-speed digital components and modules.

The measurement software offers three different levels of measurement analysis:
1. Fast pass/fail measurements ideal for production

If you work in production you can test against limits, for example the BER is set at a given threshold. The fast pass/fail measurements allow you to test devices at up to 10 times faster than with previous test methods - it typically takes under one second!

2. Fast clock out to data out (setup and hold times), skew and eye opening specification results - no need to calculate values
3. Graphical results for detailed root cause analysis - see trends clearly and fast, e.g. pseudo color plot and contour plots

If you are in R&D you can characterize your device under test (DUT) (find the limits and specifications) of the DUT and results can be viewed graphically.

With its easy-to-use Windows® NT 4.0 based GUI and graphical results, it simplifies test development and allows easy test execution. Data can be exported and the graphical and numerical results printed.

You can create test executive round the measurement software using Agilent Vee, National Instruments' LabVIEW®, Excel, Agilent TestExec, C/C++ and Microsoft® VisualBasic.
The ParBERT measurement software includes the following measurements:
1. Fast Eye Mask Measurement
2. DUT Output Timing Measurement
3. Eye opening

The Measurement Software is included in the standard software package which comes with each ParBERT 81250 system.

Table 1

Requirements
MUI requires E4832A, E4861A modules for all used analyzer ports / terminals E4832A, E4841A, E4861A can be used for data generation.

General	
Store / recall	Workspace Single Measurements
Copy / paste	Measurement data to compare between measurements
Print	
Export of	Measurement data (Excel, Mathlab, databases)
On line help	
Remote interface	P&P Driver, Ready to use active X components to integrate complete measurements easily in VEE, Visual C++, VB, Labview, Mathlab and Excel

Fast Eye Mask

The fast eye mask measurement is ideal for use in manufacturing as typically it takes just one second (including synchronization). This measurement measures the BER of a pre-defined number of points (1 to 32) - not the whole eye - defined by a threshold and timing value relative to the starting point of the measurement. You enter the pass/fail criteria of the measurement and the BER threshold, find the middle point of the eye with the sequence and then run the BER. This measurement runs via remote programming.

Measurement results provided:
- BER at pre-defined sample points
- Pass/fail results

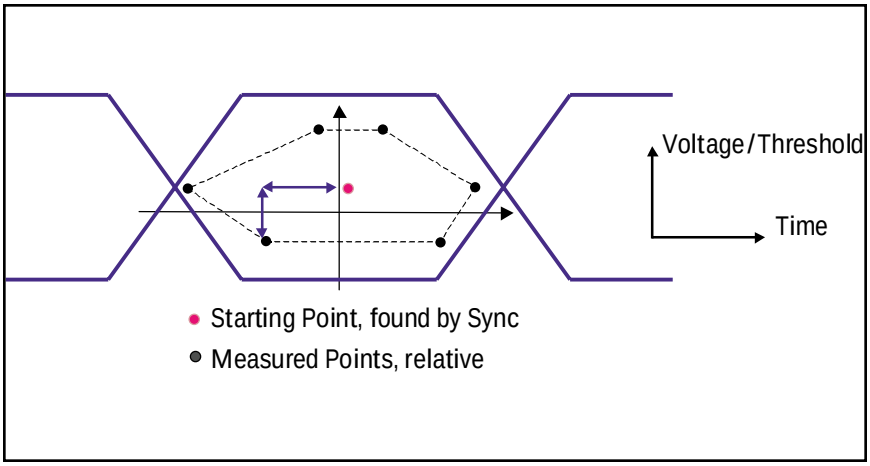


Figure 8: How the fast eye mask measurement works

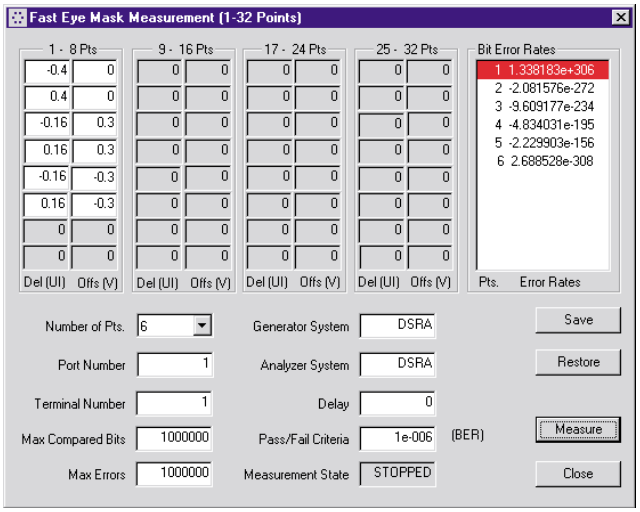


Figure 9: The fast eye mask set-up and results window

Frequency	# channels	# points measured	Compared Bits	Time Taken
2.67Gb/s	2	6	10^6	< 1 sec
2.67Gb/s	2	32	10^6	~ 1 sec
667 MHz	16	6	10^6	~ 6 sec
667 MHz	16	32	10^6	~ 6 sec

Table 2: Fast Eye Mask measurement time examples (run on a system via IEEE 1394 PC link)

DUT Output Timing Measurement

This measurement measures the BER of a DUTs output versus sample point delay, which is shown graphically as a bath tub curve. The delay is always centered to the optimum sampling delay point of the port (terminals). If a clock is defined the clock to data alignment is measured. If the absolute delay can be measured it will also be displayed. Relative timing, where edges are compared, is also possible.

Measurement results provided:
- Clock out to data out timing relations (setup/hold time)
- Skew between outputs
- Delay at optimum sample point
- Phase margin
- Pass/fail results

Also numerical view that show the "numerical return values" for the selected BER threshold only.

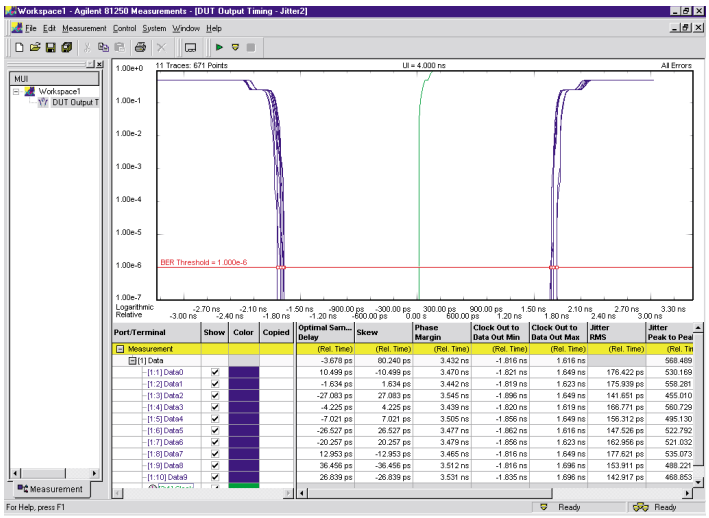


Figure 10: View the DUT output measurement results as a bathtub curve

Table 3

DUT Output Timing Measurement	
Timing Parameters	Optimum sample point delay Phase margin Clock to data out min Clock to data out max Skew between channels
Jitter Parameters	RMS Jitter Mean Value Peak Peak Jitter for specific BER
Pass /fail	For all timing and jitter parameters Each parameter can be individually enabled
Graph	View of BER versus sample delay 2 Markers: delay, BER

Eye Opening

To measure the eye opening the sampling delay and the threshold of the receiving channels are swept.

Measurement results provided:
· Eye opening (voltage and timing)
· Optimum sample point

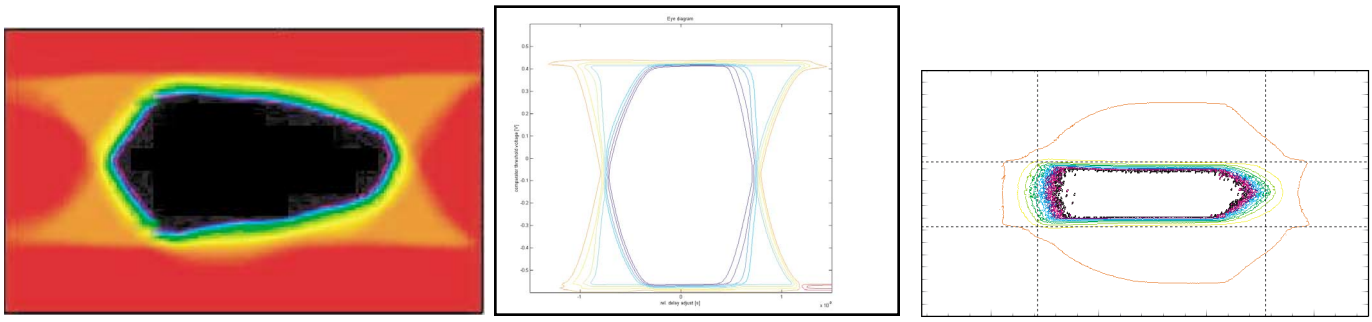


Figure 11: View the BER for one termial as a pseudo color plot or contour plot or equal BER at BER Threshold

Table 4

Eye opening	
Meas. Parameters	Optimum sample point delay Optimum threshold Eye opening (volt) Phase margin
Pass /fail	For all parameters Each parameter can be individually enabled
Graph	Two Markers: Volt, delay, BER

Fundamental Platform Description

The ParBERT 81250 is a modular instrument, which can be tailored to your specific needs. The idea of the ParBERT 81250 product structure is that you get the instrument, which matches your measurement task perfectly.

The **front-ends** determine which kind of output or input connectors your specific instrument has. This means front-ends determine the speed and input/output capabilities of your instrument.

After you have chosen the front-ends, they are placed in **data modules**, which are responsible for sequencing, generation and analysis of data patterns including PRBS/PRWS. These modules plus at least one clock module, which generates the common system frequency of the instrument, are installed in the mainframe. The mainframe can hold up to 20 channels at the data ratio of 2.67 Gbit/s or 40 channels at 667 MHz.

If more channels are needed there is the possibility of adding up to two expander frames to this, to reach the maximum number of channels (64 channels of 2.67 Gbit/s or 128 channels of 667 MHz).

Additional clock modules are needed to set up systems which work with different clock speeds which are not divisible or multipliable by the factors 2,4,8,16 (if E4832A is used) and 2 and 4 (if E4861A is used). For example, for testing 1:7 or 1:10 Mux/Demux devices two clock modules are required.

The ParBERT 81250 user software runs on a 2-slot-embedded-VXI PC or on an external PC which is connected to the system via an IEEE 1394 PC link to VXI. Both controller options can be ordered with ParBERT 81250. The operating system is MS Windows NT 4.0.

The ParBERT 81250 modules can also be combined with other standard VXI modules to build up a standard VXI test system. Plug & Play drivers are supplied.

Ready-to-go application bundles

There are ready-to-go bundles available for key ParBERT 81250 applications. These can be easily configured and are more economical than buying each part separately (see page 19 for more details).

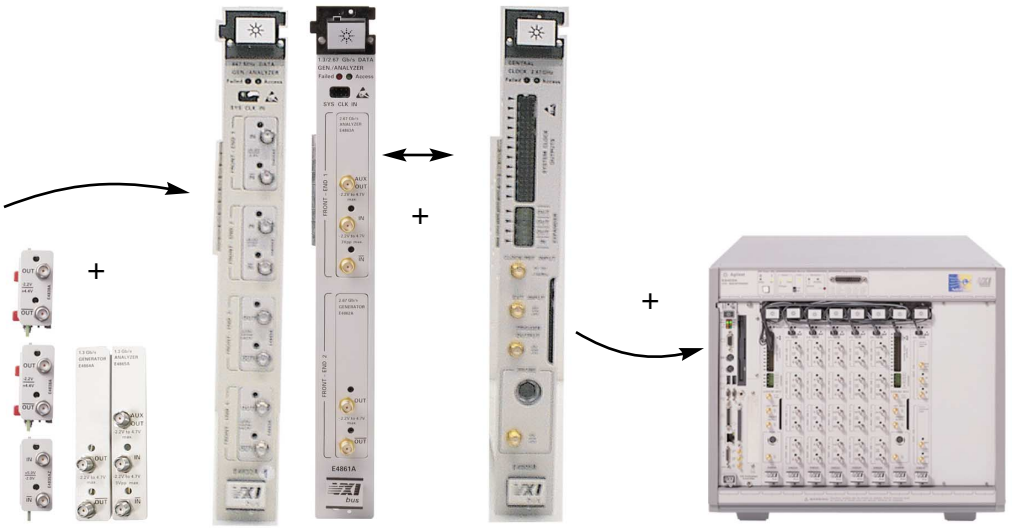
- E4891A High speed bundle with 2 generators and 2 analyzers at 1.33 Gb/s
- E4892A super high speed bundle with 2 generators and 2 analyzers at 2.67 Gb/s
- E4893A 667 MHz generator bundle (8 outputs)

Front-Ends
determine
-type (generator/ analyzer)
-speed of channels

Data Modules
determine
-signal generation/analysis capabilities
-speed of channels

Clock Module **generates the system clock and distributes the clock to Data Modules**

Mainframe **with different controller options + up to 2 additional expander frames if needed**



Technical Specifications

These specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10°C to 40°C ambient temperature after a 30 minute warm-up phase, width outputs and inputs terminate with 50 Ω to ground at EEC levels if not otherwise noticed.

Input / output Specifications

Front-ends: You can choose between four generator front-ends (outputs) and three analyzer front-ends (inputs) of the speed classes 667 MHz, 1.33 GHz and 2.67 GHz. For individual specifications see tables 1 - 5.

Auxiliary Output: At the analyzer front-ends E4863/5A, the signal from the device-under-test can be fed through the analyzer for further usage, e.g. as an input to a jitter analyzer or an oscilloscope. Auxiliary output works in differential and single-ended mode.

Total Jitter (peak-to-peak) is specified as a function of (Deterministic jitter +2×(n(BER) x random jitter σ), for further details please refer to the figure on page 9.

Connectors: SMA (f) 3.5 mm.

Enable / connect: Each output/input can be switched on and off individually, and the connect/ disconnect function allows you to disable/enable respectively, all outputs and inputs at one time.

Table 5: Parameters for Analyzer Front-Ends E4863A 2.67 GSa/s (E4865A 1.33 GSa/s)	
Number of channels	1 , differential or single ended
Typical impedance	50 Ω (100 W differential if termination voltage is switched off)
Internal termination voltage (can be switched of)	-2.0 to +3.0 V
Threshold voltage range	-2.0 to + 3.0 V
Threshold resolution	2 mV
Threshold accuracy	±20 mV ± 1%
Input sensitivity (single-ended and differential)	50mV typ
Minimum detectable pulse width	180 ps typ. at ECL levels
Maximum input voltage range	Three ranges selectable: -2V to + 1V -1V to +2V 0V to 3V
Maximum differential voltage	1.8V operating max. 3V
Random jitter	5ps RMS (3ps RMS typ.)
Deterministic jitter	25ps peak-to-peak
DCD	5ps typ.
Auxiliary out	Vout: 400 mV pp typ., AC coupled

Table 6: Parameters for Generator Front-ends E4862A 2.67Gbit/s (E4864A 1.33 GHZ)	
Outputs	1, differential
Typ. Impedance	50 Ω
Data formats	Clock: Duty cycle 50%±10% typ. Data: NRZ, DNRZ
Output voltage window	-2.00 to + 3.00 V 3.00 V to 4.5(terminated to +3V only)
Maximum external voltage	- 2.2 to +4.7 V
External termination voltage	-2V to +3V
Addressable technologies	LVDS, ECL (terminated with 50 to 0 V/-2 V), PECL,(terminated to 3 V) low voltage CMOS
Amplitude / Resolution	0.05 to 1.8 Vpp* / 10 mV
Accuracy HiLevel/Amplitude	±2%±10 mV
Short circuit current	72 mA max
Transition times (20%-80%)	90ps typ@ ECL,LVDS 110ps typ @ Vpp max
Overshooting/ringing	10% + 20mV typ
Random jitter	5ps RMS (3ps RMS typ.)
Deterministic jitter	25ps peak-to-peak
DCD	5ps typ

*does double into open, but outputs may switch off.

Table 7: Level Parameters for Differential Generator Front-end E4843A 667 MHz	
Number of channels	1, differential
Typical Impedance	50 Ω
Data formats	RZ, R1, NRZ, DNRZ
Output voltage window	-2.00 to +3.00 V (doubles into open)
Maximum external voltage	-2.5 to +4.2 V
External termination voltage	-2.5 to+4.2 V
Addressable technologies	TTL, ECL (terminated with 50 Ω to 0 V/-2 V), PECL (terminated to +3 V)
Amplitude / Resolution	0.30 to 2.50 Vpp / 10 mV (doubles into open)
Accuracy	Levels: ±5%±100 mV
Short circuit current	120 mA max
Transition times:	Fixed
20-80% at ECL levels:	< 350 ps, 200 ps typ.
10-90% at 2.5Vpp ampl:	500 ps typ.
Overshoot/ringing	< 5% typ.
Droop	2.5 Vpp < 20%, ECL < 10%
Minimum pulse width	ECL: 600 ps typ. 2.5 Vpp: 700 ps typ
Random jitter	8ps RMS typ.
Deterministic jitter	40ps peak to peak
Duty cycle distortion	< 40 ps typ.
Channel addition	XOR
Max memory with E4832A	2 Mbit

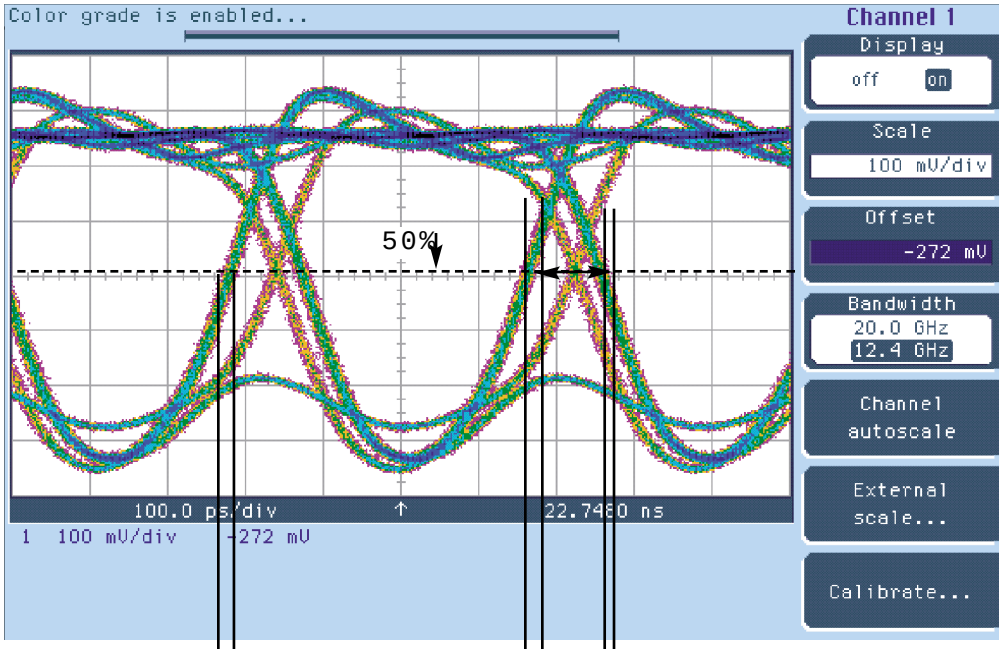
Table 8: Level Parameters for Differential Generator Front-end E4838A 667 MHz	
Number of channels	1, differential
Typical Impedance	50 Ω
Data formats	RZ, R1, NRZ, DNRZ
Output voltage window	-2.2 to +4.4 V (doubles into open up to max. 5 Vpp)
Addressable technologies	LVDS, (P)ECL, TTL, 3.3 V CMOS
Amplitude / Resolution	< 0.1 to 3.50 Vpp / 10 mV
Level accuracy	±3 %± 25 mV typ. after 5 ns settling time
@LVDS/(P)ECL	±1 %±25 mV typ. after 5 ns settling time
Variable transition time range	
(10-90% of amplitude)	0.5 to 4.5 ns
Accuracy	±5%±100 ps
@LVDS/(P)ECL (20-80% of amplitude)	0.35 ns typ
Overshoot/ringing	< 7% / < 5% typ.
Random jitter	8ps RMS typ.
Deterministic jitter	40ps peak to peak
Duty cycle distortion	< 40 ps typ.
Channel addition	XOR and analog
Max memory with E4832A	2 Mbit

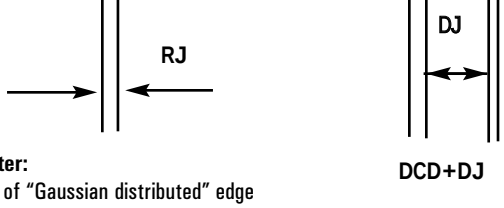
Table 9: Two Differential Analyzer Front-Ends E4835A[1], 667 MSa/s	
Number of channels	2 , differential or single ended (switchable)
Typical impedance	50 Ω (100Ω differential if termination voltage is switched off)
Termination voltage (can be switched off)	-2.0 to + 3.0 V
Threshold voltage range / Threshold accuracy	-2.00 to +4.50 V / ±1%±20mV
Threshold resolution	2 mV
Input sensitivity	Differential 50 mV typ Single-ended 100 mV typ
Minimum detectable pulsewidth	400 ps typ. at ECL levels
Input voltage range	Two ranges selectable: 0 to +5 V and –2 to +3 V

[1]occupy two front-end slots of the E4832A. The E4835A contains two front-ends (E4835AZ) and option #001 (back end). In this document we refer to one front-end as E4835A.

Jitter Definition

Total Jitter (peak-to-peak):=Deterministic jitter + 2×(n(BER) × σ)





Random Jitter:
RMS value s of "Gaussian distributed" edge (measured with pure clock signal)

Determimistic Jitter:
larger value of spacing between the two leading or trailing edges respectively (measured with 1000000101111110 pattern (and complement))

Dependancy n(BER):	
BER	n
10^{-6}	4.9
10^{-9}	6.12
10^{-10}	6.48
10^{-12}	7.12

Remark: The performance of this waveform doesn't correspond to the waveform performance of the ParBERT 81250. This waveform has been chosen only to explain the jitter specification. The waveform performance of ParBERT 81250 is shown in figure 2, page 4.

Module Descriptions

Each system consists of at least one clock module E4805B, which generates the system clock and at least one 667 MHz generator/ analyzer module E4832A or one 2.67 GHz generator/analyzer module E4861A which houses the front-ends.

E4805B Central Clock Module

The central clock module includes a PLL (Phase-Locked Loop) frequency generator to provide a system clock. Depending on the frequency chosen the data module E4832A can be clocked at a ratio of 1,2,4,8 or 16 times higher or lower than the system clock.

External start / stop: The E4805B can be started, stopped or gated on the selected active input level (also see table 7).

Ext. Clock / Ext. Reference: This input runs ParBERT 81250 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. Usage of a continuous clock is necessary. Burst clock cannot be used as an external clock. Maximum external clock is 2.67 GHz. (Note: no improvement of jitter specifications will be achieved).

Guided deskew: Individual semi-automatic deskew per channel. The deskew probe E4805B #003 allows deskew on the DUT's (Device Under Test) pins with the DUT connected. Deskew range is 20 ns.

Table 10: E4805B Central Clock Specifications	
Frequency range* **(can be entered as period or frequency)**	1 kHz to 666.66700 MHz. E4861A will run with Clock module in range of 333 MHz to 2.67GHz, E4832A in range of 333 kHz to 667 MHz.
Resolution	1 Hz
Accuracy	±50 ppm with internal PLL reference

* May be limited by modules or front-ends

Table 11: External input and ext. clock/ext. ref. input of E4805B		
Zin/Termination voltage	50 Ω /-2.10 V to 3.30 V	
Sensitivity/max levels	400 mVpp /-3 V to + 6 V	
Coupling		
Ext. Input:	dc, Threshold Range: -1.40 V to +3.70 V	
Ext. Clock/Ext. Ref:	ac	
Input transitions/slope	< 20 ns. Ext. input active edge is selectable	
Input frequency/period:		
Ext. Clock	170 kHz – 2.67 GHz	
Ext. Ref	1*, 2*, 5, or 10 MHz	
Required duty cycle	50 ±10 %	
Latency (typical):	to trigger Output	to channel output
Ext. input	16ns ±1 clock	46ns ±1 clock
Ext. clock	15ns	45ns
	Add 3 ns if an expander frame is used	

* Jitter performance may be degraded

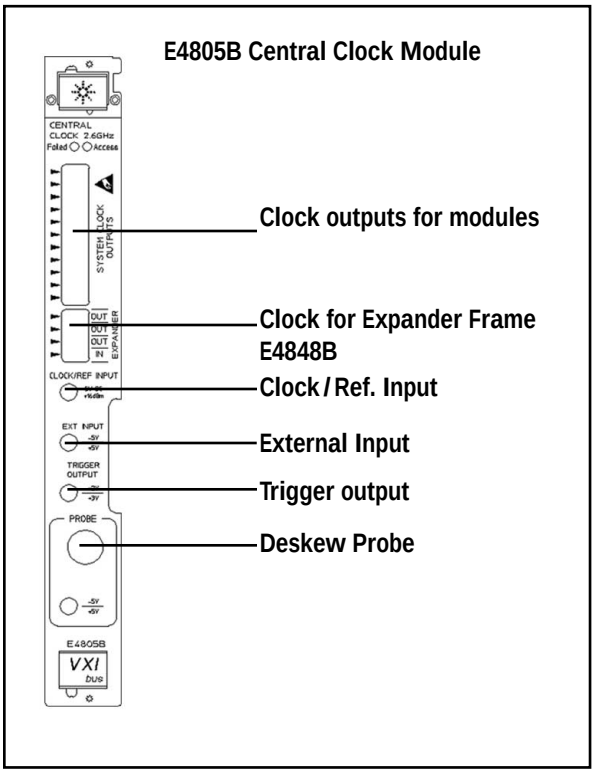


Table 12: Trigger output characteristics E4805B	
Trigger output signals	Clock mode or sequence mode (up to 667 MHz). In sequence mode the pulse can be set to mark the start of any segment.
Output impedance	50 Ω
Output level	TTL (frequency < 180 MHz), 50Ù to GND ECL 50 Ω to GND/-2 V, PECL 50 Ω to +3V
Trigger advance	30 ns typ. between trigger output and data output/ sampling point (delay set to zero in both cases)
Maximum ext voltage	-2 V to +3.3 V
Jitter (int. reference/int. clock, measured at TRIGGER OUTPUT)	< 10 ps rms (typ. 5ps)

Table13: E4805B Sequencing Features	
Number of Segments	1 to 30 (every segment looped once) 1 to 60 (no segment looped)
Looping levels	Up to 4 nested loops plus one optional infinite loop Loops can be set independently from 1 to 2^{20} repetitions
Start/stop	External input, manual, programmed
Event handling	React on internal and external events. Details see table 9a

Table 14: Event handling	
Usage on events	**Description**
Stop & Go of data sequences:	Very useful for production tests during interaction with other test equipment
Data segment switching:	Based on the events. Certain portions of the overall sequence can be executed.
Trigger external devices:	External instruments like an oscilloscope can be triggered, e.g. to sample a waveform or an error location.
ATE integration:	The ParBERT 81250 is started from an ATE platform like an IC test system for complementing missing tester functionalities. The result: pass/fail information is returned back to the ATE platform.
Match loop:	Repetition of a data segment as long as a defined event occurs. Useful for device synchronization, e.g. PLL-based device.
Event trigger sources Events can be defined as any combination of the following sources. A maximum of 10 events can be defined.	
• E4805B option 002 8-line trigger input pod for TTL signals	
• VXI trigger lines T0 and T1	
• Any capture error/or no error detected by one of the analyzer channels	
• Software command control: an event trigger command issued locally or remotely	
Reactions to an event can be set per data segment immediately or deferred and can be any combination of:	
• Data segment jump	
• Launch trigger pulse to the trigger output of the E4805B Central Clock Module	
• VXI trigger lines T0 and T1 can be set to 01, 10 or 11	

E4832A 667 MHz Generator / Analyzer Module

This module holds any combination of up to two analyzer front-ends (E4835A) and generator front-ends (E4838A, E4843A).

Segment length resolution:
This is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4832A can be set in steps of 16 bits up to a length of 2048 Kbit. If the 16-bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 13.

Sub-frequencies:
For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2,4,8, or 16. This influences the dependency between segment length resolution and maximum memory depth (see table 13).

Table 15: E4832A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND and fastest transition times)

Frequency range		333.334 kHz to 666.66700 MHz
Delay range		0 to 3.0 µs (not limited by period)
	Resolution	2 ps
	Accuracy	±50 ps ± 50 ppm relative to the zero-delay Placement *.
	Skew	50 ps typ. after deskewing at customer leves
Pulse width		Can be specified as width or % of duty cycle
	Range	750ps to [Period-750ps]
	Resolution	2 ps
	Accuracy	± 200 ps ± 0.1 %.
Duty Cycle		1 % to 99 %, subject to width limits

*Valid at 15...35ºC room temperature.

Table 16: E4832A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50Ω to GND

Sample delay:= start delay + fine delay, Fine delay can be changed without stopping**	
Sampling rate*	Same as generator
Fine delay range	± 1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

*See tables for frontend deratings

**Conditions: frequency > 20.8 MHz and by using the finest segment length resolution.

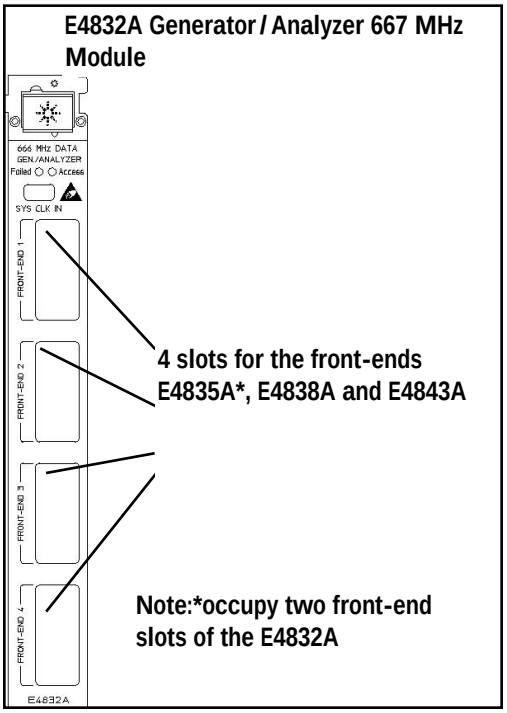


Table 17: Pattern and Sequencing features of E4832A

Patterns:	
Memory based	up to 2Mbit see table 13
PRBS/PRWS	2^n-1, n=7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS 2^n-1, n=7, 9, 10, 11,15
Errored	2^n-1, n=7, 9, 10, 11, 15
Extended ones or 0	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, 16
User	Data editor, file import
Analyzer Auto-Synchronization:**	On PRBS or memory based data manual or automatic by: Bit synchronization* with or without automatic phase alignment Automatic delay alignment around start sample delay (Range: +/-50ns) BER Threshold: 10^4 to 10^9

*Bit synchronization on data is achieved by detecting a 48Bit unique word at the beginning of the segment. Don't cares within the detect word are possible. In this mode no memory based data can be sent within the same system. If several inputs synchronize the delay difference between the terminals, it must be smaller +/-5 segment length resolution.
**Condition:frequency > 20.8 MHz and by using the finest segment length resolution.

Table 18: Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mbit/s	Segment length resolution	Maximum memory depth, bits
20.834...41.666	1 bits	131,008
41.667...83.333	2 bits	262,016
83.334...166.666	4 bits	524,032
166.667...333.333	8 bits	1,048,064
333.334...666.667	16 bits	2,097,152

In general it is possible to set higher values for the segment length resolution and also at lower frequencies than is indicated in the table. In this case the fine delay function and the auto- synchronisation function are unavailable.

Table 19: Depending between the capability of generating PRWS and port width. Almost all the combinations are possible except the following

PRWS	Port Width
2^7-1	No restriction
2^9-1	7
2^{10}-1	3, 11, 31, 33
2^{11}-1	23
2^{15}-1	7, 31
2^{23}-1	47
2^{31}-1	No restriction

E4861A Generator / Analyzer Module

This module holds any combination of up to two analyzer front-ends (E4863A, E4865A) and generator front-ends (E4862A, E4864A).

Segment length resolution:
This is the resolution to which the length of a pattern segment or mask can be set. The maximum memory per channel of the E4861A can be set in steps of 64 bits up to a length of 8192 kbits. If the 64 bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 18.

Sub-frequencies:
For applications requiring different frequencies at a fraction of the system clock, the rate can be divided or multiplied by 1, 2 or 4. This influences the dependency between segment length resolution and maximum memory depth (see table 18).

Table 20: E4861A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND

Frequency range*	333.334 MHz to 2.666667 GHz
Delay (between channels)	Can be specified as leading edge delay in fraction of bits in each channel
Range	0 to 300 ns (not limited by period)
Resolution	1 ps
Accuracy	± 50 ps ± 50 ppm relative to the zero-delay placement. (From 20°C to 35 °C without autocal) ±30 ps ± 50 ppm typ. relative to the zero-delay placement and temperature change within ± 5 °C after autocalibration
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency .
Pulse width	50% of period typ. in clock mode

* See tables for front-end deratings

Table 21: E4861A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50Ω to GND

Sample delay:= start delay + fine delay, fine delay can be change without stopping	
Sampling rate*	Same as generator
Fine delay range	± 1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

*See tables for frontend deratings

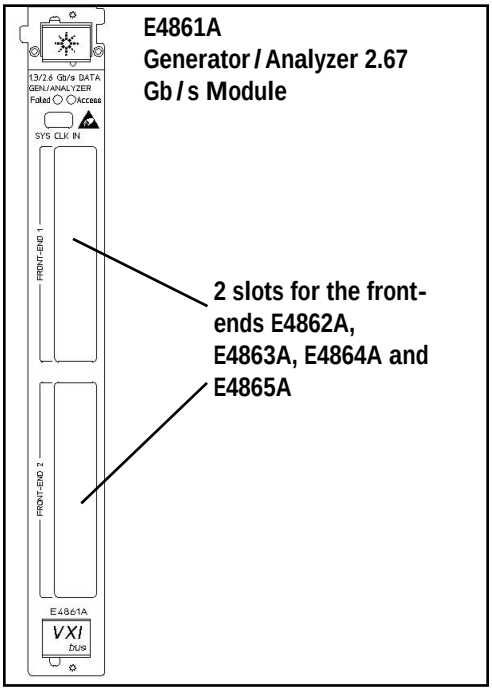


Table 22: E4861A Pattern and Sequencing	
Patterns:	
Memory based	up to 2Mbit see table 18
PRBS/PRWS	2^n-1, n=7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS 2^n-1, n=7, 9, 10, 11,15
Errored	2^n-1, n=7, 9, 10, 11, 15
Extended ones or 0	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, 16
User	Data editor, file import
Analyzer Auto-	On PRBS or memory based data
Synchronization:	manual or automatic by: Bit synchronization* with or without automatic phase alignment Automatic delay alignment around start sample delay (Range: +/-50ns) BER Threshold: 10^4 to 10^9

*Bit synchronization on data is achieved by detecting a 48Bit unique word at the beginning of the segment. Don't cares within the detect word are possible. In this mode no memory based data can be sent within the same system. If several inputs synchronize the delay difference between the terminals, it must be smaller +/-5 segment length resolution.

Table 23: E4861A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50Ω to GND	
Sample delay:= start delay + fine delay, fine delay can be change without stopping	
Sampling rate*	Same as generator
Fine delay range	± 1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

Table 24: Depending between the capability of generating PRWS and port width. Almost all the combinations are possible except the following

PRWS	Port Width
2^7-1	No restriction
2^9-1	7
2^{10}-1	3, 11, 31, 33
2^{11}-1	23
2^{15}-1	7, 31
2^{23}-1	47
2^{31}-1	No restriction

General Characteristics

Mainframes: See table 21.

Save / recall: Pattern segments, settings and complete settings plus segments can be saved and recalled. The number of settings that can be stored is limited only by internal disk space.

Vector import / export: Pattern files can be imported/exported via a 3.5 inch floppy disk, LAN or GP-IB (IEEE 488.2). File format is ASCII using a STIL subset.

Programming interface: GP-IB (IEEE 488.2) and LAN. The interface to applications such as C, Visual Basic, or VEE must be installed. Agilent 81200 Plug & Play drivers for easy programming are available.

Programming language: SCPI 1992.0

Programming times: Vector transfer from memory to hardware depends on the amount of data. Also see table 20.

On-line help: Context-sensitive.

Print-on-demand: Getting started and programming guides can be printed from .pdf files included in the ParBERT 81250 software.

Self-test: Module and system self-tests can be initiated.

Modules

Module size: VXI C-size, 1 slot.

Module type: Register-based; requires ParBERT 81250 user software E4875A supplied with the mainframes.

Weight: (including front-ends) Net: 2kg.

Shipping: 2.5 kg.

Warranty: 3 years return for repair service.

Re-calibration period: 3 years recommended.

Agilent Technologies Quality Standards
The ParBERT 81250 is produced to the ISO 9001 international quality system standard as part of Agilent Technologies commitment to continually increase customer satisfaction through improved quality control.

Table 25: Programming Times of ParBERT 81250

	Programming time
Change of levels	6 ms typ.
Change of delay	16 ms. typ. Not applicable in run mode.
Change of period	60 ms typ. For one E4805B with one E4832A. Not applicable in run mode. Increases with the number of modules but less than proportional.
Stop + start	32 ms typ.
Synchronization*	50ms typ. (without phase alignment) 110ms typ. with 20% phase accuracy @ 660MHz 650ms typ. with 1% phase accuracy @ 660MHz
Download values:	
System with 4 channels, 100,000 bit each	< 1.5 s typ.
System with 120 channels, 1 Mbit each	< 30 s typ.
System with 40 channels, 1 Mbit each	< 10 s typ.

*Add numbers for each synchronizing analyzer within one module

Table 26: General Mainframe Characteristics		
	E4860/91/92/93A mainframe	**E4848B expander frame**
Factory-installed items	E8403A 13-slot VXI C-size frame, E4805B Central Clock Module One of the Controller options: • #012 VXI 2-slot-PC E9850A with additional 64 MB memory (total 128 MB) with Windows NT 4.0, E4875A ParBERT 81250 User Software installed • #013 IEEE 1394 PC link to VXI (E8491B) with installation CD-ROM of E4875A	E8403A 13-slot VXI C-size frame, E1482B VXI bus extender module, 1 meter MXI and INTX cable
Number of slots for ParBERT 81250 modules	11 (for controller option 012) 12 (for controller option 013) (subtract 1 if expander frame is connected)	12
Operating temperature	10 °C to 40 °C	
Storage temperature	-20°C to +60°C	
Humidity	80% rel. humidity at 40 °C	
Power requirements	90-264 Vac, ±10%, 47-66 Hz , 90-264 Vac, ±10%, 300-440 Hz (not recommended, leakage current may exceed safety limits @ > 132 Vac)	
Power available for modules	950 W for 90-110 Vac supplies 1000 W for 110-264 Vac supplies	
Electromagnetic compatibility	EN 55011/CISPR 11 group 1, class A + 21 dB	
Acoustic noise	48 (56) dBA sound pressure at low (high) fan speed	
Safety	IEC 348, UL1244, CSA 22.2 #231, CE-mark	
Physical dimensions	W: 424.5 mm H: 352 mm D: 631 mm	
Weight (Net)	26.8 kg	25.3 kg
Weight (shipping)(max.)	72 kg	67 kg

Table 27: Power Requirements of Modules and Front-Ends

	DC Volts	+24V	+12V	+5V	-2V	-5.2V	-12V
Modules (These specifications are valid for the module with the front-ends installed)							
E4805B Central Clock Module	DC Current	0.15A	0.2A	1.8A	1.4A	3.8A	0.2A
	Dynamic Current	0.015A	0.02A	0.18A	0.14A	0.38A	0.02A
E4861A 2.67 Gb/s Gen./An. Module	DC Current	0.10A	0.50A	5.20A	1.80A	4.00A	0.90A
	Dynamic Current	0.01A	0.05A	0.52A	0.18A	0.40A	0.09A
Remark: For the module E4832A, the power specifications of the chosen front-ends (E4835A, E4838A or E4843A) have to be added to the power specifications of the E4832A module to get the overall value of the power specifications.							
E4832A 667 MHz Gen./An. Module	DC Current	0.10A	0.10A	2.60A	0.60A	3.60A	0.10A
	Dynamic Current	0.01A	0.01A	0.26A	0.06A	0.36A	0.01A
Front-Ends							
E4835A Two Differential Analyzer 667 Msa/s (E4835AZ)	DC Current		0.2	1.2	0.2	0.3	0.3
	Dynamic Current		0.02	0.12	0.02	0.03	0.03
E4838A Differential Generator 667 MHz, var. Slopes	DC Current		0.45	0.18	0.07	0.38	0.41
	Dynamic Current		0.045	0.006A	0.007A	0.038A	0.041
E4843A 667 MHz Generator	DC Current		0.14A	0.06A	0.06A	0.03A	0.16A
	Dynamic Current		0.014A	0.006A	0.006A	0.003A	0.016A

Table 28a: Cooling requirements for the modules E4805B and E4861A with the front-ends installed

Modules	ΔP mm H_2O for 10°C rise	Air Flow Liter/s
E4805B	0.25	3.6
E4861A	0.4	5.2

Table 28b: Cooling requirements for the module E4832A with the front-ends installed

Module	ΔP mm H_2O for 15°C rise	Air Flow Liter/s
E4832A	0.3	4.7

Short Ordering Guide - Select a system that is right for you

Ready-to-go applications bundles

The following pages describe the ready-to-go application bundles, which meet most of the ParBERT 81250 applications. The following bundles are available:

- **E4891A High Speed Bundle 1.33 Gbit/s.**
- **E4892A High Speed Bundle 2.67 Gbit/s.**
- **E4893A 667 MHz Data Generator Bundle**

The **advantage** of ordering one of these bundles instead of ordering all parts separately is:

- Easy to order: You only have to choose a controller option (#012 or #013) and you get your ParBERT 81250 pre-installed.
- If more channels are required, you only have to add optional modules to the system.
- Save money: Ordering one of these bundles is cheaper than ordering all parts separately.

Each bundle includes a mainframe with ParBERT E4875A user software, and one E4805B central clock module.

If none of the bundles meet your application needs it is possible to order parts separately. Please consult your local sales engineer.

IMPORTANT NOTE:

If your application consists of a

- **Mux/Demux application which is not 2n (1:2, 1:4, 1:8, 1:16, ...)**

or

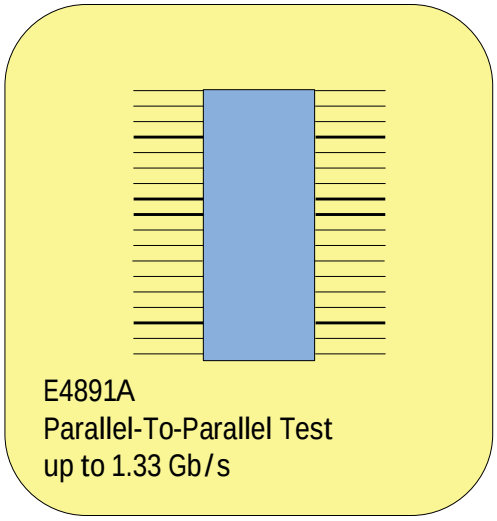
- **the auto-bit synchronization feature for memory based data for your application is required, please order an additional E4805B clock module as two are required (one E4805B is already included in all bundles).**
- **If you require the auto-bit synchronization feature for memory based data for your application and the generator and analyzer modules are in different frames, please order a trigger pod E4805B #002**

Parallel-to-Parallel test with the 1.33 Gbit/s High Speed Bundle

The E4891A bundle is ideal for parallel-to-parallel tests up to a speed of 1.33 Gbit/s. It is easily expandable for more channels by simply adding the required optional modules.

The E4891A consists of:

- 2 generator channels of 1.33 Gbit/s to stimulate (for specifications see generator front-end E4864A and module E4861A).
- 2 analyzer channels of 1.33 Gbit/s to analyze (for specifications see analyzer front-end E4865A and module E4861A).
- Mainframe Bundle consisting of a 13-slot VXI Mainframe E4803A, Central Clock Module E4805B to generate the system clock and ParBERT User Software E4875A.



In addition you have to choose controller option 012 or 013.

- The controller option 012 2-slot-PC consists of the E9850A VXI controller with Windows NT 4.0 installed.
- The controller option 013 IEEE 1394 PC link to VXI is intended to control ParBERT 81250 from an external PC. The option consists of a VXI Card and a PC plug-in card. Installation of Windows NT 4.0 (Service Pack 3 or higher) on the external PC is required to run the user software E4875A.

IMPORTANT NOTES:

- **If an additional Central Clock Module is required, please order E4805B (one E4805B is already included in bundle).**
- **If more than 8 modules (if option 013 is chosen) or 7 modules (if option 012 is chosen) are additionally required (there are already 2 data modules and 1 clock module in the bundle), please order option 150 "1st expander frame".**
- **If more than 19 modules (if option 013 is chosen) or 18 modules (if option 012 is chosen) are additionally required (there are already 2 data modules and 1 clock module in the bundle), please order option 151 "2nd expander frame" in addition to option 150.**

Table 29

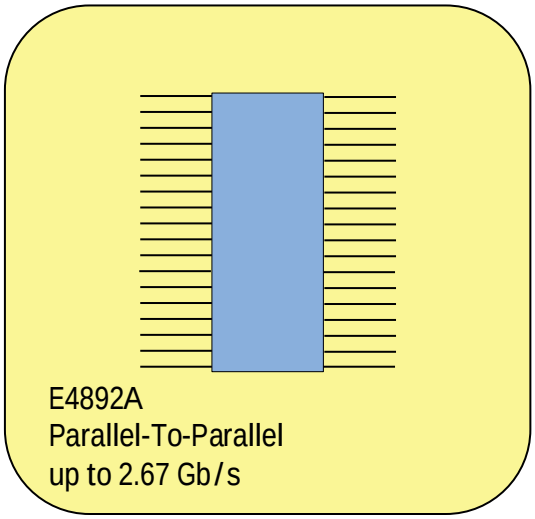
Model Number	Option	Description
E4891A		High Speed Bundle Two Pair 1.33 Gbit/s
	#010	Computer Accessories (Monitor, Keyboard, Mouse)
	#012	Controller option: 2-slot-PC
	#013	Controller option: IEEE 1394 PC link to VXI (includes PCI GPIB interface)
	#100	Add Module with 1 Generator / 1Analyzer 1.33 Gbit/s
	#101	Add Module with 2 Generators 1.33 Gbit/s
	#102	Add Module with 2 Analyzers 1.33 Gbit/s
	#150	1st Expander Frame for ParBERT 81250
	#151	2nd Expander Frame for ParBERT 81250

Parallel-to-Parallel test with the 2.67 Gbit/s Super High Speed Bundle

The E4892A is ideal for parallel-to parallel tests up to a speed of 2.67 Gbit/s. It is easily expandable to more channels by simply adding the required optional modules.

The E4892A consists of:

- 2 generator channels of 2.67 Gbit/s to stimulate (specifications see generator front-end E4862A and module E4861A).
- 2 analyzer channels of 2.67 GSa/s to analyze (specifications see analyzer front-end E4863A and module E4861A).
- Mainframe Bundle consisting of an 13-slot VXI Mainframe E4803A, Central Clock Module E4805B to generate the system clock,and ParBERT User Software E4875A.



In addition you have to choose controller option O12 or 013.

- The controller option 012 2-slot-PC consists of the VXI E9850A controller with windows NT 4.0 installed.
- The controller option 013 IEEE 1394 PC link to VXI is intended to control ParBERT 81250 from an external PC. The option consists of a VXI Card and a PC plug-in card. Installation of Windows NT 4.0 (Service Pack 3 or higher) on the external PC is required to run the E4875A user software.

IMPORTANT NOTE:

- **If an additional central clock module is required, please order E4805B (are E4805B is already included in the bundle)**
- **If more than 8 modules (if option 013 is chosen) or 7 modules (if option 012 is chosen) are additionally required (there are already 2 data modules and one clock module in the bundle), please order option 150 "1st expander frame".**
- **If more than 19 modules (if option 013 is chosen) or 18 modules (if option 012 is chosen) are additionally required (there are already 2 data modules and 1 clock module in the bundle), please order option 151 "2nd expander frame" in addition to option 150.**

Table 30

Model Number	Option	Description
E4892A		High Speed Bundle Two Pair 2.67 Gbit/s
	#010	Computer Accessories (Monitor, Keyboard, Mouse)
	#012	Controller option: 2-slot-PC
	#013	Controller option: IEEE 1394 PC link to VXI (includes PCI GPIB interface)
	#100	Add Module with 1 Generator / 1Analyzer 2.67 Gbit/s
	#101	Add Module with 2 Generators 2.67 Gbit/s
	#102	Add Module with 2 Analyzers 2.67 Gbit/s
	#150	1st Expander Frame for ParBERT 81250
	#151	2nd Expander Frame for ParBERT 81250

667 MHz Data Generator Bundle

The E4893A consists of:

- 8 channels of 667 MHz to stimulate (for specifications see generator front-end E4838A and module E4832A).
- Mainframe bundle consisting of E4803A, a 13-slot VXI mainframe, central clock module E4805B to generate the system clock and E4875A ParBERT user software .

In addition you have to choose controller option 012 or 013.

- The controller option 012 2-slot-PC consists of the E9850A VXI Controller with Windows NT 4.0 installed.

- The controller option 013 IEEE 1394 PC link to VXI is intended to control ParBERT 81250 from an external PC. The option consists of an VXI Card and a PC plug-in card. Installation of Windows NT 4.0 (Service Pack 3 or higher) on the external PC is required to run the E4875A ParBERT user software .

IMPORTANT NOTE:

- **If an additional Central Clock Module is require, please order #120.**

- **If more than 8 modules (if option 013 is chosen) or 7 modules (if option 012 is chosen) are additionally required (there are already 2 data modules and one clock module in the bundle), please order option 150 "1st expander frame".**

- **If more than 19 modules (if option 013 is chosen) or 18 modules (if option 012 is chosen) are additionally required (there are already 2 data modules and one clock module in the bundle), please order option 151 "2nd expander frame" in addition to option 150.**

Table 31

Model Number	Option	Description
E4893A		667 MHz Generators Bundle includes a ready-to-go-system with 8 outputs, E4838A
	#010	Computer Accessories (Monitor, Keyboard, Mouse)
	#012	Controller option: 2-slot-PC
	#013	Controller option: IEEE 1394 PC link to VXI (includes PCI GPIB interface)
	#100	Add Module with 1 Generator / 1 Analyzer 2.67 Gbit/s
	#101	Add Module with 2 Generators 2.67 Gbit/s
	#102	Add Module with 2 Analyzers 2.67 Gbit/s
	#110	Add Module with 4 Generators 667 MHz, E4838A
	#111	Add Module with 4 Analyzers 667 MHz, E4835A
	#112	Add Module with 2 Generators / 2 Analyzers 667 MHz
	#120	Add central clock module
	#150	1st Expander Frame for ParBERT 81250
	#151	2nd Expander Frame for ParBERT 81250

Test accessories, commercial calibration and support options

For ParBERT 81250 different test accessories, commercial calibration and support options are available. Please have a look at tables 32-35.

Table 32: ParBERT 81250 Dedicated Accessories

Model Number	Option	Description
15442A		Cable Kit: 4* SMA(m) to SMA (m)
15443A		Matched Cable Pair. Consists ot two cables SMA (m) to SMA (m) which are matched in propagation delay within 25 ps
E4805B	#002	8-line trigger input for TTL signals. When branching on external events (hardware signals) other than VXI-ECL trigger lines or compare errors is required.
	#003	Deskew probe, includes 1144A 880 MHz active probe and a BNC (f) to SMA (m) adapter

Table 33: Commercial Calibration with test report for the bundles E4890A/E4891A/E4892A

Model Number	Option	Description
E4891A		
	#U00	Commercial Calibration Option 100
	#U01	Commercial Calibration Option 101
	#U02	Commercial Calibration Option 102
	#U50	Commercial Calibration Option 150
	#U51	Commercial Calibration Option 151
	#UK6	Commercial Calibration E4891A
E4892A		
	#U00	Commercial Calibration Option 100
	#U01	Commercial Calibration Option 101
	#U02	Commercial Calibration Option 150
	#U50	Commercial Calibration Option 151
	#U51	Commercial Calibration Option 102
	#UK6	Commercial Calibration E4892A
E4893A		
	#U00	Commercial Calibration Option 100
	#U01	Commercial Calibration Option 101
	#U02	Commercial Calibration Option 102
	#U10	Commercial Calibration Option 110
	#U11	Commercial Calibration Option 111
	#U12	Commercial Calibration Option 112
	#U50	Commercial Calibration Option 150
	#U51	Commercial Calibration Option 151
	#UK6	Commercial Calibration E4890A

Table 34: General Accessories	
Model Number	**Description**
15441A	Cable Kit: 10*SMA(m) to SCI Connector
8120-4948	SMA coax. cable, 1 m.
8710-1582	Torque wrench, SMA.
15440A	Adapter Kit: 4* SMA(m) I/O Adapter
1250-1200	Adapter SMA (m)/BNC (f).
1250-1249	Adapter right-angle SMA (m-f).
1250-1397	Adapter right-angle SMA (m-m).
1250-1698	Adapter tee SMA.
11667B	Pulse adder/splitter, SMA.
15433B	500 ps transition converter.
15434B	1 ns transition converter.
15438B	2 ns transition converter.
10833B	Cable, GP-IB.
E2120F	Agilent VEE 5.0 on CD-ROM.
E4839A	Agilent 81200 Test Fixture up to 667 MHz
E4839A #001	Pogo cable kit: 4*SMA(m) & 2 Pogo adapter for the E4839A
E4839A #002	Universal DUT Test Board
E2060B	HTBasic on 3.5" disks.

Table 35: Support Options	
Option	**Description**
#W01	Convert standard warranty to 1 year on-site warranty
#W31	3 year on-site repair service
#W50	5 year return for repair service
#W51	5 year on-site repair service
#W52	5 year return for calibration service
#W54	5 year return for quality calibration service
#W32	3 year return for calibration service
#W34	3 year return for quality calibration serivce

Related Literature	Pub. Number
Need to Test BER?, Brochure	5968-9250E
Agilent ParBERT 81250, Mux/Demux Application, Application Note	5968-9695E
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Photo Card	5980-0830E
Agilent Start up Assistance	5980-2160E

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