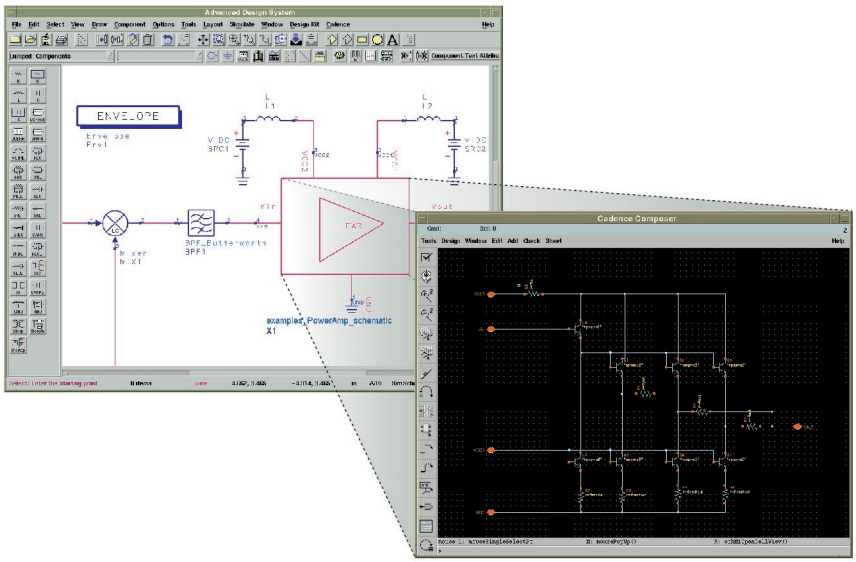
Advanced Design System

RFIC Dynamic Link for Cadence

Product Overview

Product Number E8970A/AN



Features at a Glance

Allows you to perform simulations and analyses of Cadence schematics in Advanced Design System (ADS).

- Gives full access to all simulators: Harmonic Balance, Transient, Convolution, Circuit Envelope, and Ptolemy
- Allows combination of Cadence cells with components from ADS libraries: microstrip, striplines, SMT components, and RF system models
- Provides access to ADS extensive statistical analysis and performance optimization tools
- Allows DC voltage back annotation on Cadence schematic (top-level only)
- Provides access to ADS Data Display for data post-processing and visualization
- Supports ADS release 1.3 and Cadence release 4.4.2
- Available on HP, SUN, and IBM UNIX platforms

What is the RFIC Dynamic Link for Cadence?

RFIC Dynamic Link for Cadence provides an integration interface between Advanced Design System (ADS) and Cadence Analog Artist (Cadence) design environments. The integration is based on Inter Process Communication, providing you with easy access to the powerful RF simulation and analysis capabilities of ADS while maintaining the transistor-level design information in the Cadence database.

The RFIC Dynamic Link automatically generates an ADS symbol for your Cadence schematic. You can then place this symbol on an ADS schematic and simulate it. ADS optimization and statistical analysis tools help maximize circuit performance and manufacturability.

You can process and display simulation results using the unique RF signal analysis capabilities of the ADS Data Display Environment.

RFIC Dynamic Link Architecture

RFIC Dynamic Link consists of two main parts: an ADS netlister for Analog Artist and the IDF message processor.

When you start a simulation an ADS netlist is automatically generated for every Cadence cell instantiated in ADS. These netlists are integrated in the top-level ADS netlist with the components directly placed on the ADS schematic: RF, analog, DSP behavioral components, transmission lines, sources, and simulation control blocks. The ADS simulator then processes the complete netlist.

The IDF message processor manages communication between the Cadence and ADS environments, including begin/finish sessions, simulation control, design variable passing, and DC back annotation.

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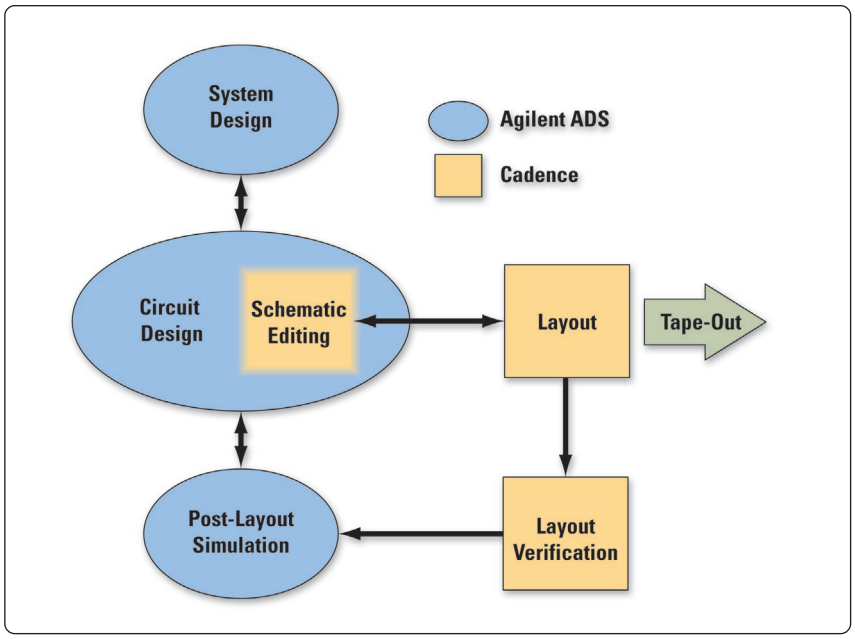


Integrated RFIC Design Flow

With the RFIC Dynamic Link you can realize a tightly integrated design flow for developing Wireless ICs, beginning with defining the top-level chip or chipset architecture all the way to completion of layout verification and tape-out.

System-Level Design

You can define the top-level chipset architecture using the unique ADS system-level analysis capabilities:

- co-simulation of the RF, analog, and DSP portions of the system
- access to several predefined system-level libraries for popular wireless communication standards such as: GSM, CDMA, and WCDMA.

Circuit Design

After you have defined the system-level specifications, you can enter the transistor-level circuit into the Cadence schematic editor.

Next, the circuit is analyzed in ADS using its DC, time domain, frequency domain, and modulation domain simulators. The transistor-level circuit can be co-simulated with the rest of the system, including other Cadence cells and components from the RF, analog, and DSP libraries available in ADS. Performance optimization and statistical analysis also takes place in the ADS environment.

Layout Editing and Verification

In the Cadence environment you can perform layout editing and verification of the circuit blocks including Layout verses Schematic check, Design Rule Check, and Parasitic Extraction.

Post Layout Simulation

The Parasitic Extractor generates a netlist that you can import into ADS via netlist translation. You can then verify final performance in ADS before tape-out.

Use Model

The following example shows a simple design created, simulated, and optimized using ADS and Cadence integrated via the RFIC Dynamic Link. This example uses a single instance of a Cadence cell containing a limited number of components. The same use model applies when dealing with multiple instances containing large numbers of components.

Step 1
Entering Circuit Schematic

After the system has been defined at the behavioral level, the circuit is entered at the transistor level in Cadence Composer. When the circuit is ready for simulation, ADS is started from the Tools menu in the Composer environment.

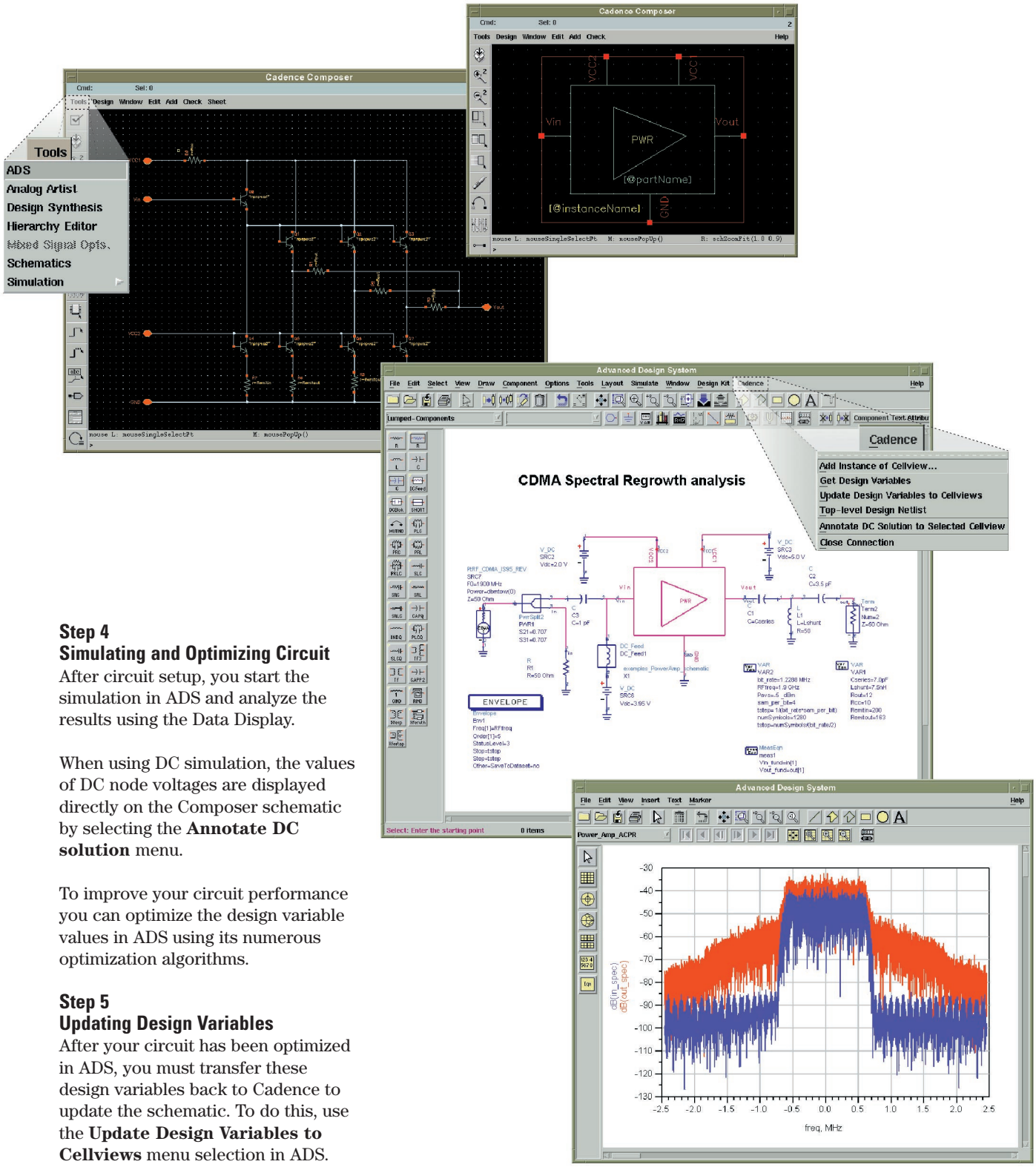
Step 2
Creating Top-Level ADS Schematic

Using the **Add Instance of Cellview** menu, the circuit entered into Composer is instantiated on the ADS schematic. The symbol view of the instantiated Cadence cell is transferred to an ADS symbol. The underlying circuit for this symbol resides only in the Cadence database.

You can then add signal sources, external bias circuitry, and simulation controls to the ADS schematic. System-level components such as amplifiers, mixers, filters, and DSP library elements must be included in the same schematic to simulate larger portions of the communication system.

Step 3
Translating Design Variables

Design variables defined for the Composer cell must be converted to ADS variables using the **Update Design Variables to Cellviews** menu. A **VAR** component is generated automatically on the ADS schematic. Variables are set to the values defined on the Cadence cell in use.



Step 4
Simulating and Optimizing Circuit

After circuit setup, you start the simulation in ADS and analyze the results using the Data Display.

When using DC simulation, the values of DC node voltages are displayed directly on the Composer schematic by selecting the **Annotate DC solution** menu.

To improve your circuit performance you can optimize the design variable values in ADS using its numerous optimization algorithms.

Step 5
Updating Design Variables

After your circuit has been optimized in ADS, you must transfer these design variables back to Cadence to update the schematic. To do this, use the **Update Design Variables to Cellviews** menu selection in ADS.

Library Requirements

The RFIC Dynamic Link requires that you use a process library containing specific ADS netlisting and model information.

Foundry Process Design Kits contain the primitives used to design the ICs. Each kit typically includes:

- schematic information (symbols)
- netlisting information (Component Description Format)
- device models for each supported analog simulator
- physical information (footprints or P-Cells) for layout

A design flow based on the RFIC Dynamic Link requires the following modifications to the process library:

- adding an ADS view to each component in the library and defining the corresponding CDF Simulation Information section
- adding device model information in the ADS format

The documentation provided with the RFIC Dynamic Link details how to perform these tasks. We highly recommend that personnel maintaining the process libraries attend training on Library Development for the RFIC Dynamic Link. For more information contact your local Agilent EEsof EDA field sales representative.

Product Availability

The RFIC Dynamic Link is a companion product to ADS release 1.3 and requires a separate codeword.

Platform Compatibility

RFIC Dynamic Link is available in nodelocked and network-licensed configurations on the following UNIX platforms:

- HP (HP-UX 10.2)
- SUN (SunOS 5.5 and 5.6)
- IBM (AIX 4.2)

System Requirements

To effectively run the RFIC Dynamic Link your system should meet these specifications and license requirements:

- 256MB RAM and 4GB disk space
- Advanced Design System:
  - E8900A/AN Project Design Environment
  - E8901A/AN Data Display
  - E8881A/AN Linear Simulator
  - E8882A/AN Nonlinear Simulator and E8883A/AN Circuit Envelope Simulator are recommended
- Cadence:
  - 34500 Composer
  - 34510 Analog Artist
  - OASIS Simulator Interface

Revision support

RFIC Dynamic Link supports ADS release 1.3 and Cadence release 4.4.2.

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