

The Digital TV (DTV) Transmission Design Library from Agilent EEsof EDA helps you successfully develop digital television transmitters or receivers based on the physical layer specifications in the ISDB-T (Japan) or DVB-T (Europe) standards. This library allows you to develop and refine specification-compliant algorithmic designs at the system level where design choices have the greatest impact. Seamless links to Advanced Design System (ADS) options, signal processing algorithms based on the ISDB-T/DVB-T, and analog and RF circuits help you move quickly to design implementation.

In addition to a complete set of behavioral models conforming to specifications, this library contains pre-built simulation systems and application examples. They allow you to explore the DTV transmitter or receiver designs to achieve higher performance and superior hardware implementation efficiency.

A Comprehensive DTV TX/RX Solution from RF/Analog to Baseband/Digital

The Digital TV Transmission Design Library is a companion product to ADS, a versatile design tool from Agilent EEsof EDA that gives you access to a wide array of analog, digital signal processing (DSP), and RF behavioral models in a user-friendly and highly integrated design environment.



Agilent Technologies

Innovating the HP Way

ADS helps you make quick and accurate modifications to the DTV transmission system implementations and develops DTV transmission chipsets, whether your goal is baseband/RF processing or mixed-signal system-onchip (SoC). The ADS development environment provides you with a variety of design and simulation tools, such as Agilent Ptolemy, Circuit Envelope, and SPICE.

In addition, ADS links your test and measurement equipment, such as ESG-D RF digital signal generator or vector signal analyzer, to your design. This link enables you to refine your designs comprehensively at the system level and replace behavioral models with actual circuit designs or measured data. When your system is partitioned into analog, digital, and highfrequency RF, you can design the baseband portion with synthesizable models and generate the registertransfer level HDL netlists for subsequent logic synthesis and implementation into silicon.

Pre-Built Test Benches and Application Examples

- OFDM 64-QAM modulation and demodulation in ISDB-T
- OFDM 64-QAM ISDB-T system without channel coding BER
- OFDM DQPSK modulation and demodulation in ISDB-T
- OFDM DQPSK ISDB-T system without channel coding BER
- OFDM equalizer in ISDB-T
- OFDM modulation and demodulation in ISDB-T (2-layer and 3-layer)
- 1-layer 64-QAM mapping ISDB-T system design
- 1-layer DQPSK mapping ISDB-T system design
- 2-layer and 3-layer ISDB-T system designs
- Complete RF transmitter and receiver design capability including nonlinear components, phase noise, and intermodulation distortion

DTV Transmission Design Library Features

- Fully compliant with the ISDB-T and DVB-T standard specifications
- Complete system structure on the physical layer
- Advanced simulation structure to support mixed-signal DTV designs
- Easy-to-use, hierarchical, and realizable models and sub-networks



DTV System-Level Design

To reduce your costs and time to market, the DTV transmission design library provides the system-level environment needed to complete highlevel designs and partitioning. The library models the complete system structure on the physical layer compliant with the ISDB-T and DVB-T specifications. It also includes advanced features, such as channel coding including convolutional codes, BCH codes and Reed-Solomon codes, DQPSK, OFDM, 16 and 64 QAM modulation and demodulation.

With the DTV transmission design library models and other models available within the Communication System Designer or DSP Designer, you can model a complete digital TV transmission system, either receiver or transmitter, including baseband digital signal processors and analog/ RF circuits.

Hardware Implementation

Once your partitioned system-level design meets performance requirements, you can move the partitioned design to implementation. Agilent ADS includes a full range of technologies to help you design the analog, RF, and digital/baseband circuits.

DSP algorithms are prepared for implementation using HDL code generation models, HDL simulation, and DSP behavioral synthesis. The system's HDL generator outputs RTL HDL code in both VHDL or Verilog format and their test environments. This reduces the need for hand coding and for translating test vectors.

You can download coded signals for hardware testing using a built-in link to the Agilent ESG-D RF digital signal generator. This powerful feature helps to reduce mistakes commonly found during the prototyping and the test phase of the design cycle. If you need assistance with your customized signal generation setup, an Agilent EEsof EDA consultant can help you.

The Agilent RFIC Designer and the RF Board Designer modules provide the necessary technology for implementing analog and RF circuit designs. The modules' simulation technologies include high-frequency SPICE, Harmonic Balance, and Circuit Envelope, to allow the widest range of design capabilities. They also include physical design capabilities and links to back-end tools to move your RFIC or board designs into your company-wide design framework. Designs with synthesizable models are verified before code generation. Synthesizable models allow you to generate HDL codes and help reduce time-consuming hand coding.



An integrated design flow with ADS and the DTV Transmission Design Library increases engineering efficiency and accelerates time to market for a DTV chipset or set-top box.

Comprehensive Components and Test Benches

Channel Coding

BCH Encoder/Decoder Convolutional Encoder/Decoder Puncture/De-Puncture Reed-Solomon Encoder/Decoder Floating-Point Interleaver Integer Interleaver PN Code Source Puncture Coder/Decoder DQPSK Coder/Decoder 160AM Coder/Decoder 640AM Coder/Decoder

DVB-T Components

Bit Interleaver DVB Propagation Channel Channel Estimator OFDM Symbol Multiplexer/Demultiplexer Data Stream Loader Symbol De-Interleavers (2-, 4-, and 6branches) Symbol Interleavers (2-, 4-, and 6branches) TPS Information Bits TPS Modulator/Demodulator

ISDB-T Components

CDSC Decoder Carrier Rotator Carrier Scrambler Channel Estimator Coherent Modulation Multiplexer/Demultiplexer Differential Modulation Multiplexer/Demultiplexer Inter-Segment Interleaver LFSR Cyclic Coder Complete TMCC Bits TMCC Bit Decomposer TMCC Differential Modulator/Demodulator TMCC Information Time Interleaver

Multiplex Components

2-Input/3-Input Commutators 2-Input/3-Input Distributors Data Stream Splitters (2-Layer/3-Layer) TSP Stream Splitters (2-Layer/3-Layer) TMCC Synthesizers (1-Layer/2-Layer, 3-Layer) Data Synthesizer (2-Layer/3-Layer) TSP Synthesizer (2-Layer/3-Layer)

OFDM Components

Fixed-Phase Addition Guard Interval Inserter FFT/IFFT Buffer Loader ML Estimator OFDM Equalizer Phase Offset Remover

Test Components

Bit Error Rate Measurement Average Power Measurement

Product Configuration

The DTV Transmission Design Library (E8868A/AN) requires the Design Environment (E8900A/AN), Data Display (E8901A/AN), and Agilent Ptolemy (E8823A/AN) in the Advanced Design System family of Agilent EEsof EDA products.

For other possible product configurations, please contact your local Agilent EEsof EDA field sales representative. For more information about Agilent EEsof EDA visit: www.agilent.com/eesof-eda

For more assistance with your test & measurement needs visit: www.agilent.com/find/assist

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