Capture By A Phase-locked Loop

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Purpose:

As we have studied in lecture, a phase-locked loop has three blocks within: a voltage-controlled oscillator (VCO), a phase detector with two inputs, and a low-pass filter/ amplifier. A good example of a PLL is the horizontal oscillator of a television receiver, which "paints" a screen of white on the picture tube by sweeping a beam of electrons back and forth horizontally. In the absence of an external signal (TV is tuned to unused channel), the horizontal oscillator is free-running and rather unstable, running *somewhere near* 15.7 KHz. When an external signal is received, the synchronization pulses in that signal are sent to the reference signal input of the PLL of the TV's horizontal oscillator. Within several cycles of the oscillator, the horizontal oscillator (a VCO) will be driven by a control voltage produced within the PLL, to make its frequency of the sync pulses on the incoming signal. Only in this way will the picture displayed by the TV be "locked" to the picture in the TV studio. This frequency in the USA is precisely 15,734.26 Hz.

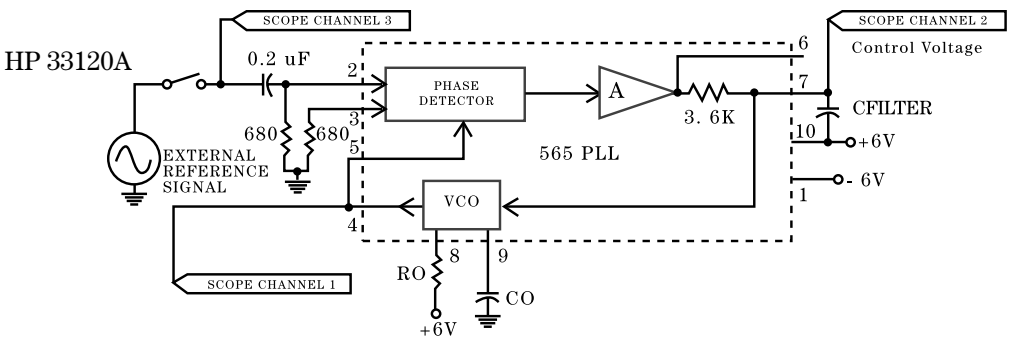
Equipment Required:

- HP 54601B - Oscilloscope
- HP 33120A - Function/Arb Generator

Observation Of Capture By A Pll:

The circuit below, a 565 PLL IC circuit which free-runs at 446 Hz, was constructed in the laboratory. In order to see the dynamics of capture occurring, a Hewlett-Packard digitizing oscilloscope was used to monitor three points in the PLL circuit, and to "freeze" them during the very short time interval (called the acquisition time) starting before the external signal is applied, and ending with in VCO of the PLL being locked to the external reference signal.

Ro = 10KΩ, Co = 68 nF, C Filter = 0.12µF



The PLL is free-running until the SPST switch is closed. The PLL then goes from its free-running condition to its locked condition in a process known as **acquisition**.

Explanation:

From top to bottom, the traces in the oscilloscope display (on the next page) are:
· the external reference input frequency (channel 3),
· the output of the VCO in the PLL (channel 1), and
· the control voltage which drives the VCO (channel 2).

Starting at the left edge of the screen, the reference signal has not yet been applied and the VCO is free-running at 439 Hz (period A is 2.28 ms; +.28ms = 439 Hz). The control voltage is a constant 3.866 VDC. At time B, a switch is closed and the 676 HZ (period E is 1.480 ms; 1/ 1.480ms = 676 Hz) reference signal is connected to the PLL's external input. Immediately a change can be seen in the control voltage, which in addition to the DC level now contains a time-varying component (the beat note equal to the difference between the reference signal and the VCO frequencies).

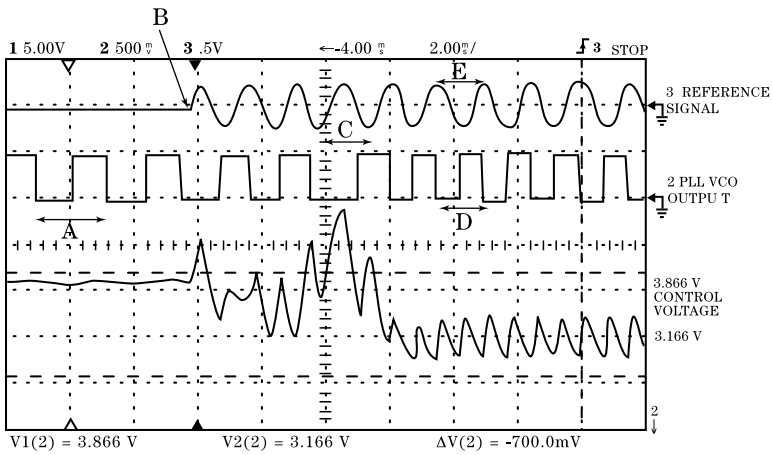
Period C is 2.44 ms, equivalent to 410 Hz, showing that the PLL's VCO is changing frequency (at first, in the wrong direction!) as the time-varying component drives it up and down from where it started (439 Hz). Within a few millisecond (each horizontal division is 2ms), the VCO frequency has risen to 676 Hz (period D is 1.480 ms; 1/1.480ms = 676 Hz) and stays constant at 676 Hz.

It is important to see that now the PLL's VCO frequency equals the reference signal frequency and **lock** has been achieved, but there is a difference in the phase of the two signals. This phase difference is what creates the control voltage (the DC level at the input of the VCO) of 3.166 V. So, a PLL **locks to an external reference**, using phase difference between the external reference and the VCO frequency.

In order to raise the VCO frequency by 237 Hz (from 439 Hz when free running to 676 Hz when locked to the external reference), the control voltage had to drop by 700 mV (from 3.866 V to 3.166 V). Clearly this VCO has a "gain" of 237 Hz/(-.7V) = -399 Hz/V.

Also of note is the "ripple" on the control voltage once lock has occurred; this is due to the "sum" frequency, produced by the phase detector, not being filtered out completely by the PLL's low-pass filter. The ripple frequency is exactly twice the VCO frequency, and the "difference" frequency is 0 Hz, since $f_{vco} = f_{ref}$.

Each time this test is done, the resulting oscilloscope display will be different, due to the VCO oscillator phase being different at the instant the switch connecting the reference signal is closed.



	State	Volts/Div	Position	Couplg	BW Lim	Invert	Probe
Chan 1	On	5.000 V	5.312 V	DC	Off	Off	10:1
Chan 2	On	500.0mV	-4.187 V	DC	Off	Off	10:1
Chan 3	On	500.0mV	1.437 V	DC	---	---	1:1
Chan 4	Off	100.0mV	0.000 V	DC	---	---	1:1

	Mode	Main Time/Div	Main Delay	Time Ref	Delayed Time/Div	Delayed Delay
Horizontal	Normal	2.000ms/	-4.000ms	Left	----------	----------

	Mode	Source	Level	Holdoff	Slope	Couplg	Reject	NoiseRej
Trigger	Single	Ch 3	125.0mV	200.0ns	Pos	DC	HF	Off

Display Mode: Normal

Cursors: t1=6.160ms t2=7.640ms V1(2)=3.866 V V2(2)=3.166 V