M8190A Arbitrary Waveform Generator

Accelerated insight into your design with Signal Scenario Generator delivering High Resolution and Wide Bandwidth









Anticipate ____Accelerate ____Achieve



Drivers for Target Markets

Realistic testing, today and tommorrow

Radar Highly realistic signal scenarios

- Simulate with the most realistic signal to avoid expensive life tests
- Need for low phase noise to detect slower moving targets

Transmitter signal, f₀ Clutter Phase noise Reflectio n from target Communication More data, faster

- Cram more information into existing bandwidth
- New standards require 100 times wider modulation bw than existing standards

R&D and Research Simulate real-world imperfections

- Ensure flexible adoption to new distortion requirements
- Mimic the analog real world imperfections

General Purpose Head-room for the future

- Keep programs on spec, on budget and on time
- Never-ending changing environment calls for new innovation





Differences M8190A Rev 1 and Rev 2

There's obviously a difference



	Revision 2 offering
Revision 1 configuration: B02	 Advanced Sequencer DC and AC Amplifier Fast switching (export control for 12GSa/s) Calibration ISO 17025 or Z54
 2 channel version 14 bit 2 GSa memory 	 1 channel or 2 channel 14 bit / 8 GSa/s or 12 bit / 12 Gsa/s 128 Msa or 2 GSa memory per channel



M8190A Arbitrary Waveform Generator

Accelerated insight into your design with Signal Scenario Generator





M8190A AWG - Reliable, repeatable measurements from precise signal simulation



 Image: Spectra service
 I



Excellent SFDR ensures that tones stand out from distortion even with hundreds of tones

- 88 dBc, 555 MHz,12 GSa/s DAC

Anticipate <u>Accelerate</u> Achieve



Optimize the Output to match your application

Three Selectable Amplifiers!



More details



M8190A AWG

Create complex signal scenarios – efficiently



Long playtime and long signal scenarios for highly realistic testing

More Details





M8190A AWG

Flexibility to stress your device to its limits

- Ensure flexible adoptions to new distortion requirements by just adopting the waveform itself
- Mimic the analog imperfections that occur in real-world environments by a
 mathematical descitions in tools like Matlab
- Reudce tests costs through realistic signal similations that minimize the need for additional hardware like power combiners



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Synchronization of more than 2 channels

- 1. Set up an external trigger generator to generate a one-shot pulse synchronous with its clock input
- Observe the skew between the marker outputs on the scope on recurring runs; make sure it is always the same skew. If not, see next slide
- 3. Adjust the waveforms and output delays to compensate the skew







Agilent Technologies More details

Flexible signal generation that enables testing of FHSS devices

Carrier frequency is rapidly changed across a wide range of frequency channels. A special receiver knew the frequency-hopping pattern.

- Interfernce, noise:
 - Spread-spectrum signals are highly resistant
 - Only a small piece of data is effected by interference because the frequency changes all the time, so error correction is much more successful.
- Secure transmission:
 - The next carrier frequency is not known, so nobody can listen in
- Effiecient use of bandwidth
- Transmission occurs only on a small portion of this bandwidth at any given time
- Spread-spectrum signals add minimal noise ot the communication,

Frequency switching characteristics

Effective output frequency ¹	
Option: -14B	$f_{max} = 3.2 \text{ GHz}$
Option: -12G	$f_{max} = 4.8 \text{ GHz}$
Effective frequency switching time ²	
Option: -14B ³	313 ps (= 1/ f _{max})
Option: -12G	No option: –FSW 210 µs
Option: -12G	Option: $-FSW 208 \text{ ps} (= 1/f_{max})$

1 Effective output frequency f_{max} is determined as $f_{Sa,max}/2.5$

2 Determines the minimum time to switch between selected segments in sequence mode

3 Option FSW does not affect switching time in 14 bit mode (Option 14B)

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With near-zero settling time, the COTS system enhances the testing of FHSS devices



Key characteristics of a Radar Pulse

- Get up to 14 bits resolution and more than 5 GHz analog bandwidth per channel simultaneously
- Build long, realistic scenarios with 2 GSa memory per channel and a sophisticated sequencer
- Push radar designs farther with highly realistic signal scenarios
- Identify deviation from the desired waveform to avoid degradation of radar performance



Radar LFM chirp – spanning 2 GHz, (Fs = 7.2 GHz, sin(x)/x compensated)

Typical Test Setup



Anticipate <u>Accelerate</u> Achieve



New features in Rev. 2 available with SW 2.1

•Output Formats (NRZ, DNRZ, RZ, Doublet)

- For RF applications, select mode based on desired frequency response
- For time-domain applications, NRZ provides better pulse performance
- For frequency-domain apps, DNRZ provides better SFDR





M8190A Programming Structure

SystemVue Wideband Wavefor





M8190A Operation with all leading software platforms





Agilent Benchlink Waveform Builder Pro

Waveform libraries provide quick and easy access to both common (sine, square, triangle, ramp, pulse, exponential) and complex signals

Free-hand, point, and line-draw modes to create custom shapes

Equation editor allows you create waveforms with exact polynomials

Advanced math functions provide additional flexibility for more complex signals

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Waveform Edit View Communications		🥝 _ 🗗 🗙
Impose April Triangle April Pulse April	E Image: Constraint of the second s	
360 m Volts 320 m 280 m	Advanced Segments Veveform Type : MultiTone	
240 m 200 m	Parameters Center Frequency 658.00000 (c) MHz Total Time 1055 (c) ns Center Frequency 658.00000 (c) MHz Total Samples 1.008 (c) kSa Number of Tones 3 (c)	
160 m 120 m 80 m	High / Low Voltage Level Tone Spacing €5000000 ⊕ MHz Amplitude 700 ♥ mVpp Phase € Fixed: 0.00 Offset 0.000 ♥ V Cycles 1.00 € Minipage 1.00	()
40 m 0 -40 m Time 0 s 246.154 u 432.308 u	Phase 0.00 c degrees table 0.4gust monolula i ores	
Samples I 1,5 M 3,2 M Time 0 s X = 5,316899 MSa,818 Sampling Rate 6,5 GSa/s Select Mode	UBSC/m 0 -115.666 m -30.333 m -30.00 p = 155007/n = 31.0154 n = 45.523 n = 52.0308 n = 77.585 n = 30.0422 n = 108.554 n = 124.052 n = 11 5amples 1 = 101.8 = 202.6 = 303.4 = 404.2 = 505 = 505.8 = 706.6 = 807.4 = 508.2 = 108.554 n = 124.052 n = 110.054 n = 100.054 n	16 M 1008 k
	Sampling Rate : 6.5 GSa/s QK Default Gar	icel

Feature	Basic	Pro
Basic Waveform Library	Yes	Yes
Cut, copy, past with Excle	Yes	Yes
Waveform math	Yes	Yes
Free hand	Yes	Yes
Line draw	Yes	Yes
Advance waveform library	No	Yes
Equatation editor	No	Yes
Point draw	No	Yes
FFT, CCDF, and contstallation diagrom	No	Yes
Filters	No	Yes
Windowing functions	No	Yes
Dual-channel operation	No	Yes

Basic version is part of M8190A shipments



Matlab

MATLAB software for the M8190A available directly from Agilent

for making your own arbitrary waveforms (multi-tone signals, pulsed radar signals, and multi-carrier modulated waveforms), measurement and analysis routines, and instrument applications.

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Function Genera	VISA Address TCPIP0: 192.168.0.111 :INSTR		- Edit Predistortion		humber of Sumbole (oll)	20		-20			
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Load data from	Skew (Ch1 vs Ch2)	- ID A			Create Random Data 🛛	2					
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	Ok Note: Parameter changes will be sent to	hardware on	next waveform download	Exa	mples can	be modified and are	downle	oadabl	e from	i the w	/eb

www.agilent.com/find/81180 examples:



Accelerate "Design to Test" for Complex Waveforms SystemVue + Agilent's M8190A





Introducing New 802.11ad Signal Creation and Signal Analysis Software or WWC





Agilent 60 GHz PHY Test Solution



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More details

The new AWG picture

Do you care about waveform resolution?



Arricist DR⁴ across Nyquitst range with f_{out} = 150 MHz
 Bandwidth of a single channel AWG output



Arbitrary Waveform Generator Ongoing Innovation



• Push Radar design farther with highly realistic signal scenarios with 2 GSa memory per channel

Agilent Labs & high speed digital R&D designed a disruptive technology through BiCMOS silicon geranium process takes us years ahead



Ordering Instruction

M8190A	Option	Rev 1 shipment	Rev 2 shipment	Comment
1 channel	001		Х	MUST order either 001 or 002
2 channel	002	Х	Х	WOST order either out of 002
14 bit/8 GSa/s	14B	Х	Х	MUST order either 14B or 12G or both
12 GSa/s/12 bit	12G		Х	options
Additional DC and AC amplifier	AMP		Х	
Upgrade to 2 GSa memory per channel	02G	Х	Х	Optional options
Sequencer	SEQ		Х	
Fast switching	FSW		Х	Fast switching for 12 GSa/s requires export control license
ISO 17025	1A7		Х	Colibration options
Z540	Z54		Х	

Rev 1 configuration requires the Options 002, 14B, 02G. These options are bundled into Option B02. Ordering of additional options based on B02 configuration requires a hardware upgrade. Additional options of revision 2 are software upgradable.

AXle infrastructure

- M9502A: Two-slot AXIe chassis with ESM
- M9505A: Five-slot AXIe chassis with ESM
- M9045A and M9045B: PCIe laptop card adapter Gen 1 x4
- M9047A: PCIe desktop card adapter Gen 2 x8
- Y1200A: x4 x8 PCIe cable
- Y1202A: x8 x8 PCIe cable
- M9536A: Embedded AXIe controller

Accelerate ____Achieve

Accessories

M8190A-801	Microwave phase matched balun, 6.5 GHz, max SMA jack
M8190A-805	Low pass filter, 2800 MHz, max SMA, VLF 2850+
M8190A-806	Low pass filter, 3900 MHZ max SMA, VLF 3800+
M8190A-810	Cable assembly coaxial–50 $\Omega,$ SMA to SMA, 457 mm length
M8190A-811	Cable assembly coaxial–50 $\Omega,$ SMA to SMA, 1220 mm length
M8190A-815	Dynamic control input cable
M8190A-820	Connector-RF, SMA termination, plug straight, 50 $\Omega,$ 12.4 GHz, 0.5 W



Auticipate _

Configurations

5-slot AXIe chassis

- fits up to 2 M8190As + system controller + ESM module
- Only a monitor is needed to form a complete instrument



2-slot AXIe chassis

- Fits one M8190A + ESM module
- **Requires PC or Laptop** with PCI-Express interface card to control it





Backup



Typical Setup





Signal Generation Setups







Agilent Arbitrary Waveform Generator Portfolio Expansion





Enhance your Reality with a Source of Greater Fidelity



5 GHz analog bandwidth

Operation with all leading software platforms





Analog vs. Digital Up-Conversion

Analog I and Q signals are generated using an AWG. An (analog) I/Q modulator generates the IF or RF signal





In digital I/Q modulation, the multiplication with a carrier signal is performed digitally – either in real-time or in software









Delivering High Resolution and Wide Bandwidth simultaneously



Back



Expansion into Signal Scenario Generators





M8190A Software Structure





M8190A AWG - Reliable, repeatable measurements from precise signal simulation





- 63 dBc, 2 GHz, 100 tones, 12 Gsa/s, DAC

- 45 dBc, 3 GHz 1000 tones, 8 Gsa/s, DAC

Excellent SFDR ensures that tones stand out from distortion even with hundreds of tones



Anticipate _____Accelerate _____Achieve



M8190A Block Diagram





Agilent Amplifier Concept



Agilent Amplifier

M8190A without sequencing

- Only a single waveform segment is available
- Waveform segment can be up to 2 GSamples long

Infinite loop

Sequence

- A sequence consists of a list of waveform segments
- Total size of waveform segments can be up to 2 GSamples
- Each segment can be looped up to 2³² times
- A sequence can contain up to 512K steps

Infinite loop

Scenario

• A scenario consists of a list of sequences

Loop 5 times

Advancement modes

Advancing from one segment/sequence to the next can be...

Automatic

Loop N times, then go to next segment/sequence (un-conditional)

Conditional

Loop until an event occurs, then go to next segment/sequence

Repeat

- Loop N times, then wait until an event occurs before going to the next segment/sequence
- Stepped
 - Same as "Repeat", but wait for an event on every loop

All transitions are "seamless". Event can be an external signal or a software command

Selection of segment/sequence to be generated

Selection of segment/sequence can be determined by...

- Pre-defined sequence
 - If the order of waveform segments is known ahead of time, it can be set up as a "sequence"
- Dynamic Control Port
 - The dynamic control port on the front panel allows you to select one of 2¹³ (2¹⁹) segments/sequences
 dynamically at runtime by applying a digital pattern to the dynamic control port connector
- Software
 - Instead of applying a digital pattern to the dynamic control port, you can also select a segment/sequence using software by sending a command to the firmware

In all cases, transitions are "seamless" – without any gaps

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Trigger modes

All of the previously mentioned cases can be combined with the following trigger modes. This applies to **segments** or **sequences**.

...and how does it work internally?

81199A Wideband Waveform Creator (GUI)

81199A WiGig / 802.11ad Modulation Analyzer

Multiple dockable windows, each independently configurable to display any mix of...

81199A Wideband Waveform Center

- Spectrum
- Main Time
- Error Summarv
- Decoded Payload Data
- LDPC Codeword Display
- Correlator Output
- Channel Estimation
- IQ Data
- Error Vector Spectrum
- Error Vector Time
- OFDM EVM vs symbol
- OFDM EVM vs subcarrier
- Carrier Tracking
- Phase Error
- Power .vs. Time

- @ X

Demod On

If true, the demod will run on the

Errors and Warnings

802.11ad Technology

Bandwidth1.76 GHz1.825 GHzModulationp/2-BPSK, p/2-QPSK,16-QAMSQPSK, QPSK,16-QAM, 64-QAM

Why New Test Tools for for 60 GHz Wireless

mm Technology

- Performance taken for granted at lower frequencies not so easy to acheive
- Mismatch, skew, cable lengths matter

Baseband Modulation & Demodulation

- 2 GHz Modulation BW
 - Data rates up to 7 Gbps
 - 100 times wider modulation bandwidth than 802.11n.
 - 1.5 times wider than 802.11ac
- Traditional sources and analyzers lack BW
- Complex frequency response (flatness) difficult

No connectors at 60 GHz

- Built-in multi-element anntenas lack test connection
- No place to insert 1.85mm connectors
- · Over-the-air (OTA) testing required
- Multi-path intrinsic in performance and in measurement environment

Agilent Participation in the WiGig Alliance

In the Alliance and Participation in the PlugFest

- Agilent representatives have chaired the WGA Interoperability Working Group (IWG) for the last two years.
- Agilent exclusively provided the test equipment for the PlugFest

From WiGig Alliance Press Release

"Key test instrumentation for the PlugFest is being provided by Agilent Technologies, the leader in test and measurement and the only commercial provider of signal creation and modulation analysis SW and HW solutions for the WiGig Standard."

Triggering of M8190A modules

Trigger latency is the amount of time it takes from the (active) edge of the trigger input to the start of the output signal

- The trigger latency can typically be broken down into
 - a fixed amount (due to the delay in cables & asynchronous circuits)

 a certain number of clock cycles (due to internal flip-flop stages)
 a.g. 2.6 ns + 7680 clk.cycles +/- 24 clk.cycles – and an amount of uncertainty (see next slide) fixed number of clocks uncertainty

Definition: Trigger uncertainty

Trigger **uncertainty** is the worst case variation of trigger latency that can be observed on recurring trigger events

- Without any precautions (= asynchronous trigger input), the trigger uncertainty in the M8190A is +/- 3 ns @ 8GHz sample rate. At slower sample rates proportionally more!!
- While the fixed and clock-dependent amounts of trigger latency can easily be compensated by the system setup, a large trigger uncertainty might be not acceptable for many applications

Why does the M8190A have a large trigger uncertainty? (when using asynchronous triggering)

- Inside the M8190A, the trigger input is sampled with the SYNC clock.
 [SYNC clock = Sample clock divided by 48 (64) in 14-bit (12-bit) mode]
- Now consider two different scenarios of when a trigger input can occur relative to SYNC Clock

\rightarrow Different Trigger latencies are observed by the user

How can the trigger uncertainty be avoided?

Make sure the **trigger input** is **synchronized** with the **SYNC Clock** Output of the M8190A. This reduces the trigger uncertainty to an excellent **+/- 5 ps** (typ.) !!

...of course this only works if the DUT can operate at the SYNC clock frequency (= M8190A sample rate divided by 48 or $64^{(*)}$)

(*) SYNC clock = Sample clock divided by 48 in 14-bit mode, divided by 64 in 12-bit mode

How to use synchronous triggering at other frequencies?

Use the device's clock output to drive the Ref.Clk Input of the M8190A. This works under the following conditions:

- M8190A sample clock is set to the Ref.Clk Input frequency times 48 or 64^(*) divided by an integer ≥ 1. (Example: Ref.Clk = 100 MHz, Sample Clk = 4.8 / 2.4 / 1.6 / 1.2 GHz, etc. in 14-bit mode)
- The other device generates its output synchronous to its Clock Output
- The Clock Output frequency is a multiple of 1 MHz in the range 1...200 MHz

(*) SYNC clock = Sample clock divided by 48 in 14-bit mode, divided by 64 in 12-bit mode

... or use an external Reference Clock

Use an external Ref.Clk to drive both the device's clock input and the Ref.Clk Input of the M8190A

- M8190A sample clock must be set to the Ref.Clk Input frequency times 48 or 64^(*) divided by an integer ≥ 1
- The other device generates its output synchronous to its Clock Input
- The Ref.Clk. frequency is a multiple of 1 MHz in the range 1...200 MHz

(*) SYNC clock = Sample clock divided by 48 in 14-bit mode, divided by 64 in 12-bit mode

Synchronization of two or more M8190A modules

Synchronization of two or more M8190A modules - Timeline

- Synchronization between two M8190A modules (up to 4 channels) will be officially supported in fall 2012
 - The current plan is to support the synchronization without any hardware changes just an FPGA / Firmware update and a sync cable
- Synchronization between more than two M8190A modules (more than 4 channels) is on the roadmap to be supported at a later date
 - This will require an extra "clock distribution" module. Other than that, the plan is to work without any hardware changes to the modules
- In the meantime, the approach that is described on the following slides can be used as a <u>work-around</u> to synchronize two or more modules

What does it exactly mean to "synchronize" two or more M8190A modules? (1)

Synchronization requires two things:

- 1. Frequency Synchronization
 - This is to make sure that the modules run at the same sample rate which must be derived from the same master oscillator for all modules
 - This can easily be achieved in one of two ways:
 - Feed all modules with a common reference clock. In case of two modules in the same AXI chassis, this is the default
 - Feed all modules with a common sample clock. The common sample clock can either come from an external generator or one module acts as a master and the clock is daisy chained to the other ones
- 2. (see next slide)

What does it exactly mean to "synchronize" two or more M8190A modules? (2)

- 2. All modules must be started at the same time and run with a repeatable skew
 - Starting the modules at the **exact same time** is practically impossible without the means that will be implemented inside the modules later
 - Starting the modules with a repeatable skew is possible.
 - Repeatable skew means it stays the same across multiple "runs" and waveform downloads - as long as the sample rate and other operation modes are unchanged
 - The procedure is to download "test waveforms" that are used to measure the skew between the outputs of multiple modules during a "test run".
 - Once the skew values are known, the waveforms and delays can be adjusted to compensate for the measured skew
 - Finally, the adjusted waveforms can be downloaded and the modules started again – this time with zero skew between the outputs

Why is it so difficult to start multiple modules at the exact same time?

- Consider the Sync Clock timing of two or more modules. Even though they are both derived from the same sample clock, they can have 1 of 48 (or 64) different phase relationships to each other
- An asynchronous start signal might be sampled by the different modules in different order every time → no repeatable skew → useless
- A start signal that is synchronous to the first module's SYNC Clock is better but might violate setup/hold times of other modules – depending on their phase alignment

Synchronization setup

(shown for two M8190A, but can be extended to more)

- 1. Set up the M8190A in "armed" mode; load waveforms to all module that contain a marker at the start of the waveform; start all modules
- 2. Set up an external trigger generator to generate a one-shot pulse synchronous with its clock input
- 3. Observe the skew between the marker outputs on the scope on recurring runs; make sure it is always the same skew. If not, see next slide
- 4. Adjust the waveforms and output delays to compensate the skew

What if the skew is not repeatable?

- ...then you have a setup or hold-time violation on one of the modules
- identify which module does not generate a repeatable timing (expect the skew to "jump" by SYNC clk period)
- Change the sample rate of the module to a different sample rate and change it back to the original sample rate. This will cause the sync clock divider to find a new (random) phase. Go back to the previous step
- With a little programming effort it should be possible to automate this procedure
- Note: After every power cycle / change of sample rate / change of 12-/14bit mode, synchronization is LOST

Example

Four M8190A channels in sync

Waveforms consist of a pulse (to show perfect alignment) -

followed by a sinewave (to show that channels are independent)

In a real application, the waveform can of course be completely arbitrary

Example

Other considerations for multi-module operation

- **Two** M8190A modules can be plugged into a 5-slot AXI frame (plus an optional embedded controller). That's the simplest configuration, since the sample clock can easily be shared between the modules
- **Three** or **four** M8190A modules will have to be split up into two AXI 5-slot chassis. In order to run such a configuration, you will either need
 - One compatible PC with two PCIe slots (we don't know if that exists) or
 - Two separate, compatible PCs or embedded controllers (which is expensive, but probably OK for someone who can afford 3 or 4 modules)
- If a customer wants two M8190A modules in two separate 2-slot chassis (e.g. because he wants to use them separately as well as together), the same applies

