ATM solution requires new test methods

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Asynchronous transfer mode (ATM) designers work harder than ever to meet today's short schedules for ASICs, boards and subsystem design. To ease their load, significant improvements can be made in debug and verification by using more efficient test tools.

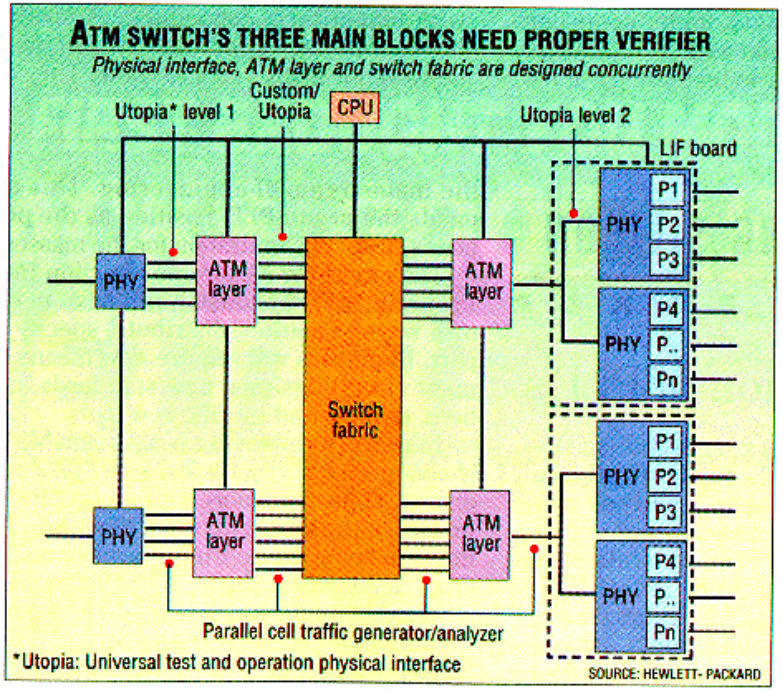
Neither protocol test equipment, focusing on serial standards, nor traditional general-purpose tools, such as data generators and logic analyzers, provides the required cell-stimulating and analyzing capabilities for the parallel standard called Utopia. Self-built tools aren't the answer: they create additional cost and work load for the design team and typically are in the critical path of the project schedules.

Here, three examples of ATM design verification show the requirements for a new kind of test equipment.

The figure shows a block diagram of an ATM switch that usually consists of the concurrently designed main blocks: the physical interface, ATM layer block and switch fabric. Inside the switch, two important changes happen to the ATM cells: first, the serial cells are paralleled to 8 or 16 bits by the physical layer and from there transferred over proprietary or Utopia (for Universal Test and Operation PHY Interface) parallel interfaces. Second, to make switching effective, the ATM layer adds routing information to the cell before passing it to the switch fabric. The routing information is removed by the system after the cell is routed through the switch fabric. This means that the switch fabric runs at a slightly higher clock rate than the serial line rate divided by the multiplexed ratio.

To meet timelines, the individual blocks are typically designed by different groups (concurrent engineering), which must provide their components on time and meet defined quality goals before system integration begins. Defined quality means to achieve the overall performance and Quality of Service for the complete system. This is measured by full functional system test.

The ATM Forum has established Utopia as an 8- or 16-bit wide parallel interface between chips or boards within communication designs. Boards or chips from different design groups or vendors that follow this standard can be easily integrated. Today, practically all available commercial ATM chips or modules (e.g., Line Interfaces) claim to be Utopia compatible.



In proprietary designs, the standard is often used as a basis for the proprietary interface between the ATM layer and switch fabric. The data transfer is achieved by handshake signals, which indicate availability of cells. While Utopia Level 1 connects a single ATM layer device (master device) with one PHY device (slave device), the increasingly popular Utopia Level 2 interface can handle up to 31 physical layer or line interface devices simultaneously (MultiPHY). This means that larger-scale integration can be used in the design to minimize chip count and the physical space needed for the design is decreased.

For Level 2, the ATM layer must poll and select an individual physical layer device for cell transfers. The Utopia standard, especially for Level 2, specifies signal behavior for several situations. The process of polling and selection is efficient and is performed simultaneously with data transfer. The assignment for the next cell transfer is performed before the current cell data transfer is completed. As a consequence, signaling is complex and the verification of Utopia signaling is an additional step in the design verification process. The most efficient way to verify performance is to use dedicated test equipment to functionally test all implemented Utopia modes.

The most critical parameter for Quality of Service and overall performance of an ATM switch is the time needed for cells to pass through the switch. According to the ATM Forum's "Cell Transit Delay" and "Cell Transit Delay Variation," the transit delay must be short as

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New test methods needed for ATM switches

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well as constant within certain limits. This must hold true under various traffic conditions occurring in the real world. Proper design, performance evaluation and functional verification of the switch fabric block, before system integration, is key to reaching the design goal and shortening the design cycle.

To verify the transit delay and the delay variation of the switch fabric, it is necessary to stimulate the system with cells that contain a routing tag and a time stamp stored in the cell payload. On the receive side, the time stamp must be analyzed to calculate transit delay and delay variation. The measurement must be performed in real time to allow realistic application measurement intervals from milliseconds (e.g., raw data transfer) up to several hours (e.g., video). Also, traffic loads from constant bit rate (CBR) up to variable bit rate (VBR) are needed to represent real-world conditions and to find the real corner cases of the design. Deterministic traffic generation allows for repeatable test setup and results.

Verifying an ATM layer block at the system level is difficult and often results in delayed schedules. Trying to verify the layer prior to system integration is also difficult unless the appropriate tools are available. The challenge is to control the number of queues and buffers under test so that each may be stressed individually or in tandem. This is accomplished by loading the selected buffers and shaping the traffic in a manner approximating worst-case, real-world conditions. The functionality of the ATM layer requires testing of all the cell and traffic manipulations, such as:

- routing header generation and insertion;
- policing of the cell stream;
- OAM (operation and maintenance) cell insertion and detection;
- cell discarding in case of overload, and
- traffic shaping.

If design verification and problem analysis on the cell level is done first, smooth system integration and development of higher-level software can be achieved. With design verification, problems are recognized and solutions achieved sooner, leading to early confidence that the ATM block will work in the system. Flexible cell generation and analysis at the parallel interface (Utopia) is required for debug.

More detail

Two measurement problems, cell tagging and cell discarding, are discussed in more detail. Before tagging the cell with the routing information, the ATM layer analyzes the cell header VPI/VCI to find the right routing information from its look-up table. Proper operation of the hardware and the lower-level device drivers controlling the look-up table are key to system integration. To check proper operation of the table, multiple accesses to the same VPI/VCI must be interspersed with accesses to other addresses. The table should be tried from all zeroes to all ones. Several thousand different VPI/VCI combinations are required for an appropriate characterization. In addition, some cells with invalid VPI/VCI must be inserted, in a controlled manner, to check for correct handling of error conditions. On the receive side, cells must be acquired and checked to ensure the correct routing tag was added.

To discard cells, the ATM layer block must monitor the traffic and react in a prescribed manner when given traffic contracts are violated. The first step in discarding cells is to change the cell-loss priority bit (CLP) of the ATM header. Then, the cells are discarded. To change the CLP and to discard cells, traffic must be stimulated in a deterministic way. Traffic is increased to the point at which the device will begin making CLP changes or discarding cells. Controlled cell bursts are used to see if cell buffering works correctly. On the receive side, the cells of importance must be extracted from the stream of received cells and counted over time. This determines the ratio of changed/unchanged CLP bits.

Both examples show the benefit of stimulating and analyzing the ATM block with a deterministic sequence of cells and a controlled traffic profile sent to the ATM layer block. Stimulating and analyzing the ATM block provides an effective and controlled way to verify your design, from relaxed settings to corner cases. Corner cases are difficult to control and force in an ATM system, but appear randomly in live traffic.

Different techniques are used to distribute data within local access systems. The local access network system interfaces with a serial standard—e.g., 155 Mbits/second optical—to the public network that connects to the service provider. The access network ends inside the set-top box at a parallel cell interface, recommended by Davic as the A0 interface.

The difficulty again is to achieve Quality of Service within this system. Noncorrupted data must be guaranteed downstream (service provider to the home), as well as upstream (home to service provider).

Quality loss

Data corruption will decrease the quality of all services, e.g., video and audio quality, at the end-user location. The designer's goal is to make the distributed system robust enough to perform against the large number of interference mechanisms. In this asymmetrical system, it is mandatory to characterize transmission quality for both the upstream and downstream paths.

The industry has picked up a unit for measuring the quality of data transmission: the Bit Error Rate (BER)—the ratio of corrupted bits vs. all bits transferred. It is generally agreed that Quality of Service can be achieved when the BER is below a certain level (typically 10^{10}). The measurement is performed by putting a continuous ITU specified sequence of Pseudo Random Data (PRBS) into the serial port and analyzing it at the other end of the access system, usually at the parallel interface. The PRBS has to be mapped to and extracted from the payload of the ATM cells. Here again, the Utopia interface is the standard for the parallel cell interfaces within the set-top box.

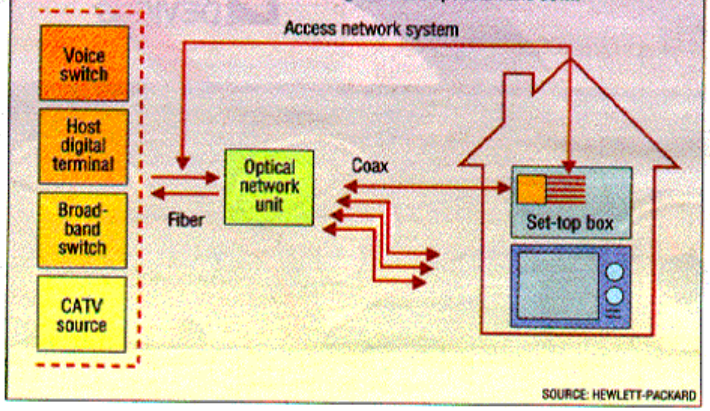
Most test solutions used in the semiconductor industry and at network equipment manufacturers are built by the design teams. For example, in semiconductors large test boards with FPGAs are placed around the DUT. The FPGAs are self-programmed to handle the cell stimulus and acquisition at the parallel interface. This is a time-consuming task and potentially compromising. When designers build their own test equipment, major compromises regarding functionality, usability and maintainability are often made.

However, major manufacturers of test equipment are now addressing this problem. Parallel cell traffic generators are believed to achieve over 30 percent savings in verification time when compared with self-built tools.

For more information and application notes on parallel cell traffic generators, access: *http://www-europe.hp.com/dvt.*

LOCAL-ACCESS NETWORK SYSTEM RELIES ON QUALITY OF SERVICE

Noncorrupted data must be guaranteed upstream and down



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