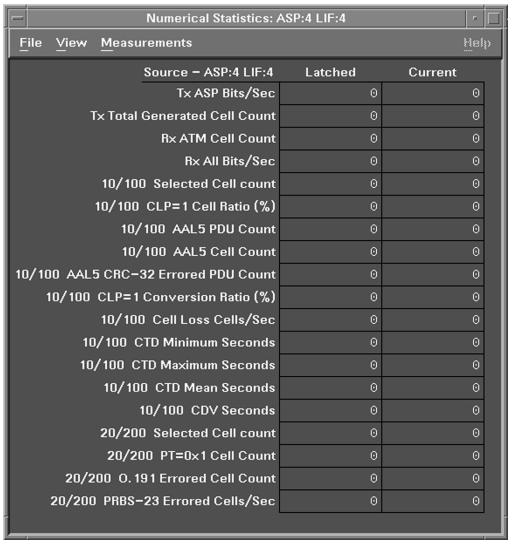
0-155 Mb/s ATM Stream Processor
0-622 Mb/s ATM Stream Processor

Agilent Technologies Broadband Series Test System

E1607A/E1609A



The ATM Stream Processor (ASP) is a product dedicated to traffic management testing, allowing the Agilent BSTS to test the functional and performance characteristics of the latest generation of ATM switches and systems.

Product Features

- Industry-standard O.191 QoS testing
- Real-time, full rate ATM QoS measurements up to 622 Mb/s
- Access to Cell Protocol Processor (CPP) offers an SVC toolkit, including conformance testing
- Easy to use PDU sequence builder
- The Agilent E1609A High Speed ATM Stream Processor (ASP) can be used with any BSTS ATM line interface from T1/E1 to OC-12c/STM-4
- The Agilent E1607A Low Speed ASP can be used with any BSTS ATM line interface from T1/E1 to OC-3c/STM-1
- Shaped multistream traffic generation on upto 16,384 VP/VCs

The Agilent Technologies ATM Stream Processor (ASP) is a single slot module and provides users of the BSTS with a tool for testing the traffic management characteristics of next-generation ATM switches. The product is primarily focussed on testing the key functions described in ATM Forum's Traffic Management Version 4.0 specification. This specification is central to ATM traffic management compliance and interoperability.

The ASP is available in two models; low speed and high speed. The low speed ASP operates at rates up to 155 Mb/s and the high speed ASP at rates up to 622 Mb/s.

The ASP allows a variety of conforming and non-conforming traffic conditions to be simulated and analyzed.

The ATM Stream Processor offers extensive real-time Quality of Service (QoS) performance measurements (ITU-T I.356) using the industry-standard ITU-T O.191 technique.

Real-time summary statistics on eight VP/VCs are displayed on the Link Monitor, enabling measurement of bandwidth utilization and address information. Real-time AAL-5 statistics enable testing of early packet discard, partial packet discard and random early discard are provided on two connections.

If signalling, higher-layer protocol analysis and conformance testing are required, add the Agilent Technologies E4209B Cell Protocol Processor (CPP).

Some of the ATM-centric test scenarios supported by the ASP and companion products for the BSTS include:

- service category compliance
- switch fairness characterization
- congestion management control
- functional UPC conformance
- alarm and error handling
- alarm propagation and response
- switch transfer performance

For test engineers who also require Operations, Administration and Maintenance (OAM), the ATM Stream Processor can be used in association with the Agilent E6270A OAM Protocol Tester for a complete traffic management test solution.

Key Features

Compact Design

The low and high speed variants of the ATM Stream Processor only occupy a single slot of your Agilent BSTS. Add it to an existing system, or build a compact single port (1 Tx/1 Rx) real-time ATM analyzer with an ATM line interface.

Real-Time QoS Measurements

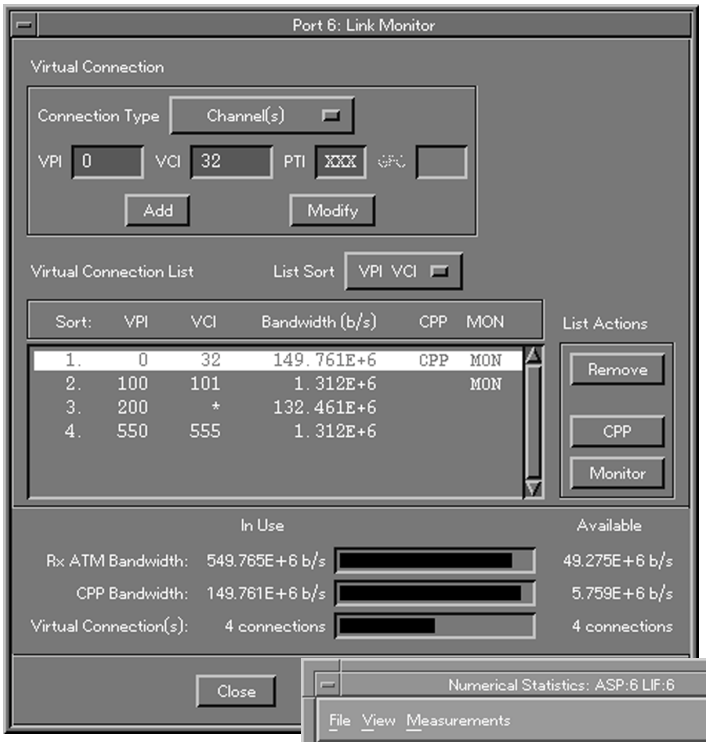
Many equipment manufacturers and service providers are insisting upon test equipment that is compliant to the industry-standard ITU-T 0.191 test methodology. This ensures that your QoS measurements are consistent with those of your partners and customers, and helps you to reliably benchmark the performance of your switch or network against those of your competitors.

The ATM Stream Processor employs the O.191 test cell to measure ATM QoS metrics such as cell loss, cell delay, and cell delay variation – in real-time on multiple channels.

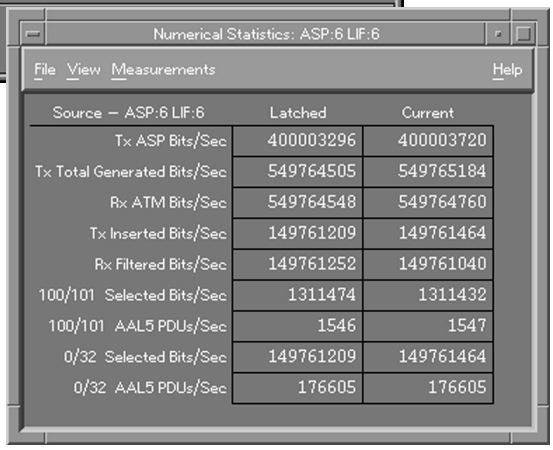
Traffic Generation

To further test the limits of your system's performance, you can easily select individual VP/VCs or multiple ranges of VP/VCs to cover up to 16,384 VP/VCs. Each VP/VC can carry a payload selected from a variety of available payload types.

Today's ATM networks typically carry data traffic using the ATM Adaptation Layer 5 (AAL-5). To simulate live traffic and to test Frame Discard switch mechanisms, you can generate CBR, VBR-rt, VBR-nrt and UBR distributions carrying ATM and AAL-5 traffic.



Up to 8 connections can be viewed in the Link Monitor



2 connections can be selected for detailed real-time statistics

PDU Sequences

Build PDUs and sequences of PDUs to simulate mixed traffic, or build higher-layer protocol PDUs, such as LANE packets, to test edge interworking devices. You can save your PDU and sequence libraries to disk so that your test plan can be easily restored and repeated.

The PDU libraries on the ASP are compatible with those of the Agilent E4209B Cell Protocol Processor (CPP).

Multi-rate Testing

You can take advantage of the real-time QoS and performance measurement capabilities over a variety of line rates from T1/E1 to OC-12c/STM-4.

The Agilent E1609A High Speed ASP can be used with any of the single slot BSTS ATM line interfaces, and the Agilent E1607A Low Speed ASP can be used with any ATM interface up to OC-3c/STM-1

Multi-Channel Real-Time Statistics

ATM and AAL-5 statistics can be monitored in real-time on multiple channels. You can measure AAL-5 reassembly statistics – such as PDU counts and CRC-32 errors – to test Partial Frame Discard implementations.

The industry-standard ITU-T O.191 test cell is used to provide ATM layer performance measurements, including Cell Loss, Cell Transfer Delay and Cell Delay Variation. Because both transmit and receive statistics are available, you can count AAL-5 frames to check higher-layer performance metrics such as frame loss ratio and frame throughput.

Multiple statistics can be graphed simultaneously and updated in real-time, allowing you to correlate statistics to help find the reason for a fault or performance degradation. Measurements can be reported as errored seconds, event counts, ratios, or bandwidths. Logging measurements to disk enables you to analyze many hours or days of test results.

Real-Time Frame Performance

ATM Quality of Service metrics are the basis for ATM traffic contracts. However, these metrics tell only half the story.

Most ATM networks carry a high proportion of data traffic. ATM switches use proprietary schemes – such as Early Frame Discard, Partial Frame Discard, Random Early Discard, and priority queuing – to maximize AAL-5 frame throughput when running near full capacity.

Compatibility

The ATM Stream Processor shares the BSTS' 155 Mb/s cell bus. This gives simultaneous access to the Agilent E4209B Cell Protocol Processor (CPP) and other specialized modules.

ATM payload of up to 149.76 Mb/s can be transmitted from modules that share the 155 Mb/s cell bus. For example, you can generate a modulated ABR stream from the Agilent E6287A ABR Emulator and combine this with multiple CBR and VBR streams from the ASP, allowing real-time validation of the interaction amongst ABR, CBR and VBR traffic.

If two or more traffic streams are generated, it is possible for the sum of the peak bandwidths to exceed the link bandwidth. When this occurs and the traffic generator cannot satisfy all traffic profiles, you are warned by an alarm located on the ASP control panel. This is very important if you need deterministic and repeatable ATM traffic generation.

Received ATM traffic being monitored by the ASP can also be monitored by other modules that share the 155Mb/s cell bus such as the CPP. For example, using just 6 of the 8 ATM header pattern-match filters, you can select

- the signalling channel
- 3 other specified VP/VCs
- all VCs on 2 specified VPs

for CPP analysis. The header pattern-match filters can also be set to select all traffic on the link to be monitored by the CPP.

The 131,072 cell output buffer of the ASP allows the CPP and other specialized modules to monitor bursts of high-speed traffic at rates up to full line rate.

You can use the CPP to run conformance test suites, to analyze LANE and other higher-layer protocols, or for signalling emulation (for example) while the ASP generates ATM and AAL-5 traffic to fill the link.

Traffic Management

For today's equipment manufacturers and service providers, the hardest problem to solve – but the one that offers the largest returns – is getting the greatest utilization from a transmission link, switch, or network, whilst meeting agreed QoS levels for all customers. The performance of a network at full or near-full capacity is determined by its congestion management, call admission control, and other traffic management techniques. This requires a broad range of tests to be performed, including:

- cell tagging and discard measurements across multiple VCs
- QoS measurements of different traffic classes
- testing priority queuing configurations, drop eligibility algorithms, and selective cell discard fairness during congestion
- sending incrementally longer AAL-5 traffic bursts to determine maximum frame burst size
- AAL-5 Early/Partial Frame Discard operation and Random Early Discard fairness
- measuring total switch capacity and examining switch response to multiple SVC connection attempts
- measuring bandwidth utilization and allocation to multiple traffic sources

User Programming Environment

An Application Programming Interface (API) is provided to enable the development of regression tests and automated test suites. Test programs can be built in the industry-standard environment of "C" and Unix. For remote system testing, scripts and user interfaces can be rapidly developed in Tcl/Tk.

Web-Based Online Documentation

All user documentation is provided online in a web-based format that can be accessed and searched using a web browser.

Related Products

- **E1618A** 622 Mb/s Optical Line Interface
- **E4200B** BSTS Form-7 Transportable Chassis
- **E4210B** BSTS Form-13 Mainframe Chassis
- **E4209B** Cell Protocol Processor (CPP)
- **E6270A** OAM Protocol Tester (OPT)

The ATM Stream Processor and existing BSTS tools

There are three key ATM test products available on the BSTS:

- ATM line interface (LIF) – T1/E1 through OC-12c/STM-4c
- Agilent E4209A/B Cell Protocol Processor (CPP)
- Agilent E1607A/E1609A ATM Stream Processor (ASP)

For *access* to the system under test, the ATM Line Interface (LIF) is used:

- access to the system under test
- physical layer stimulus/response tools for transmission engineers
- a companion module to the CPP and/or ASP

For *SVCs and higher layer protocols*, the Cell Protocol Processor (CPP) is used:

- a companion module to the ATM LIF
- focused on signalling and higher layer protocol testing
- limited to 155 Mb/s traffic generation and analysis
- support for signalling, conformance test and protocol analysis

For *traffic generation and analysis*, the ATM Stream Processor (ASP) is used:

- a companion module to the ATM LIF
- a standards based solution focused on traffic management testing
- full rate, multi-channel testing from 0 to 622 Mb/s (Agilent E1609A)
- real-time ATM QoS using industry-standard O.191 technique
- AAL-5 simulation and performance measurements
- support for protocol analysis

Configuring a system for full rate OC-12c/STM-4 testing

For full-rate 622 Mb/s physical and ATM layer testing, a minimal Agilent BSTS configuration consists of:

- E1618A 622 Mb/s Optical Line Interface
- E1609A 0-622 Mb/s ATM Stream Processor (ASP)
- either an E4200B Form-7 transportable or an E4210B Form-13 chassis

The E1609A High Speed ASP provides full-rate ATM and AAL-5 generation and analysis, to meet the need for real-time multi-stream, multi-profile, multi-channel performance measurement, and enables access to other dedicated modules.

If signalling and higher-layer protocol and conformance testing are required, simply add the E4209B Cell Protocol Processor.

Your local Agilent Technologies sales representative will help you select the best test system configuration to meet your needs.

Warranty & Support Options

Hardware

All BSTS hardware components are warranted for a period of 3 years. Products must be returned to an authorized Agilent Technologies service center for service.

Software

Agilent Technologies Broadband Series Test System software and firmware products are supplied on transportable media such as disk, CD or integrated circuits. The warranty covers physical defects in the media, and defective media is replaced at no charge during the warranty period. When installed in an Agilent Broadband Series Test System, the software/firmware media has the same warranty period as the product.

Product Numbers

- **E1607A Low Speed ASP**
  0-155 Mb/s ATM Stream Processor
- **E1609A High Speed ASP**
  0-622 Mb/s ATM Stream Processor
- **E4200/E4210B #040**
  622 Mb/s Real-Time ATM Analyzer Bundle (E1609A, E1618A)
- **E4200/E4210B #140**
  622 Mb/s Real-Time ATM Protocol Test Bundle (E4209B, E1609A, E1618A)

Operational Configuration

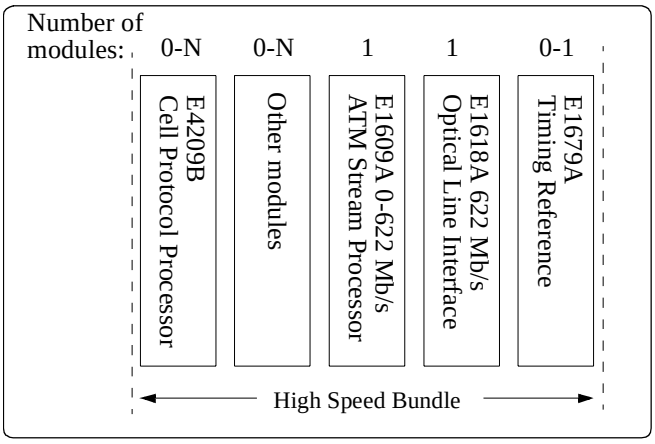
Valid Module Configurations

The E1607A 0-155 Mb/s ATM Stream Processor (ASP) and ATM line interface modules (up to OC-3c/STM-1) communicate via the 155 Mb/s BSTS cell bus. The E1609A 0-622 Mb/s ATM Stream Processor (ASP) and E1618A 622 Mb/s Optical Line Interface communicate via a high-speed 622 Mb/s cell bus.

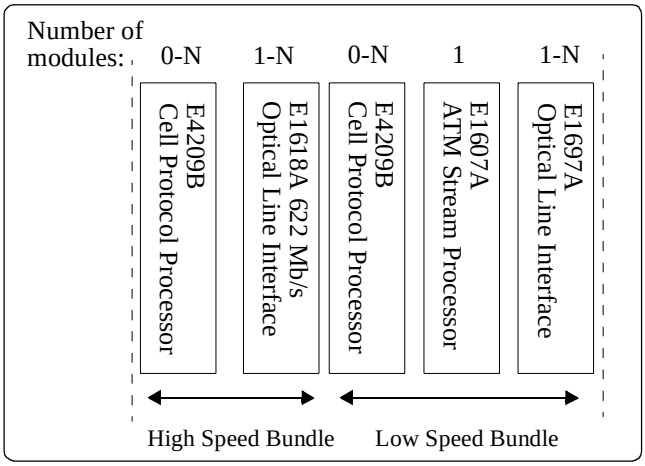
The ASP provides access to the E4209B CPP and other modules on the low-speed 155 Mb/s cell bus. The number of consecutive modules that can operate on the low-speed 155 Mb/s cell bus is controlled by a formula specified in the Test System Manager.

Traffic generated from the CPP and other modules on the low-speed bus can be selected to take precedence over traffic generated from the ATM Stream Processor. This enables signalling, higher-layer, and variable-rate traffic to be generated from the CPP whilst using the ATM Stream Processor to fill the remaining link bandwidth.

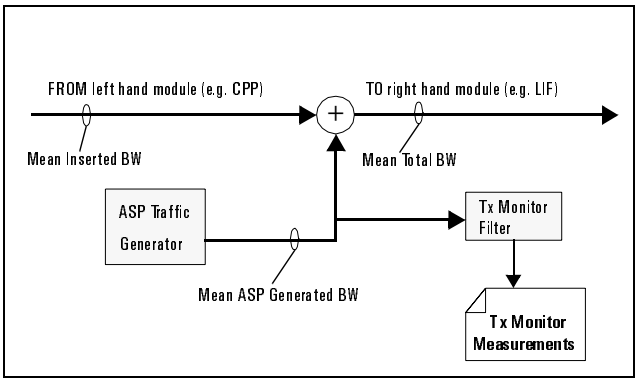
The high speed bundle shown below may be placed adjacent to additional high-speed bundles and to other modules, up to the limits of the chassis.



The low speed bundle shown below may be placed adjacent to additional low or high speed bundles and to other modules.



Transmit Functionality



155 Mb/s Cell Bus Interface

Insert Mode	• Specialized test modules (such as the E4209B Cell Protocol Processor) to the left of this module can insert cells into the generated traffic stream • Limited to the maximum bandwidth of the 155 Mb/s cell bus • Limited to the allowable configurations of the Test System Manager
Pass-Through Mode	• Cells from the 155 Mb/s cell bus to the left of this module are passed unchanged to the 155 Mb/s cell bus to the right of this module • Enables surrounding modules to be used together, bypassing this module

622 Mb/s Cell Bus Interface

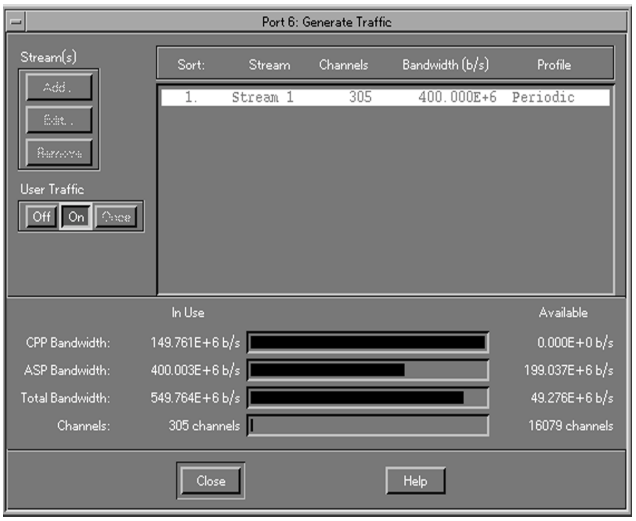
Insert Mode	• High speed ASP generated cells are passed via the 622Mb/s cell bus to the E1618A 622 Mb/s Optical Line Interface, located on the right of the high speed ASP • Limited to the maximum bandwidth of the 622 Mb/s cell bus

Link Control

Network Interface	• Select UNI or NNI
Fill Cells	• Select idle or unassigned (default = idle)

155MB/s Cell Bus Control

Control	• On: ATM cells from the 155 Mb/s cell bus (from modules such as the E4209B Cell Protocol Processor) are inserted into generated traffic – fill cells on the bus are ignored • Off: Cells from the 155 Mb/s cell bus are ignored
Bandwidth	• Cells from the 155 Mb/s cell bus can be inserted up to an ATM bandwidth of 149.76 Mb/s
Distribution	• When the E1609A High Speed ASP is generating cells, 1 in 4 cell opportunities are reserved for cells inserted from the 155 Mb/s cell bus
Priority	• Select Highest or Lowest • In "Highest" mode, cell opportunities are assigned to ATM cells from the 155 Mb/s cell bus in preference to the module's internal traffic generator • In "lowest" mode, cell opportunities are assigned to ATM cells from the module's internal traffic generator in preference to to the 155 Mb/s cell bus
Contention	• If a cell from the internal traffic generator is blocked by the insertion of a cell from the 155 Mb/s cell bus, the blocked cell is queued and generated at the next available opportunity • If a cell from the 155 Mb/s cell bus is blocked by insertion of a cell from the internal traffic generator, the blocked cell is discarded • Traffic cannot be generated from the ATM line interface when generating from the ATM Stream Processor.



Traffic Viewer displays the traffic inserted by the CPP and traffic generated by the ASP in a single screen.

ATM Stream Processor (ASP) Traffic Generator

A user-defined stream has the following properties:

- Independent control
- User-selectable traffic profile
- User-selected PDU, PDU Sequence, Test cell/frame, PRBS Pattern
- Can contain many channels (VPI/VCIs)
- User selectable stream priority

Control	• Select Internal Traffic Generator Once/On/Off • Once: A single burst of user cells is generated • On: User cells generated • Off: Fill cells generated
Number of Streams	• 8
Stream Priority	• User selectable: 1(highest) to 8 (lowest)
Traffic Profiles	• CBR, VBR-rt, VBR-nrt, UBR • Periodic Burst • Single Burst
Bandwidth Parameters	• Resolution: 424 b/s or 1 cell/s • Range (E1607): 424 b/s to 149.76 Mb/s • Range (E1609): 424 b/s to 599.04 Mb/s • 1cell/s bandwidth step • Burst length: 1 to 65,356 cells
Scheduler Modes	• Preserve SCR - in the case of contention between streams, the delayed stream is rescheduled so as to preserve the long term average SCR, possibly at the cost of exceeding the contracted PCR. • Preserve PCR - in the case of contention between streams, the delayed stream is rescheduled so as to ensure the that the contracted PCR is never exceeded.
Contention	• If the traffic profile of a cell stream from the internal traffic generator cannot be satisfied (for example, because of the insertion of cells from the 155 Mb/s cell bus), the TGNS (Traffic Generator Not Satisfied) alarm is set
Number of Channels	• 1 to 16,384 channels, 1 to 2,048 per stream • Each channel specified by VPI/VCI
Channel Selection	• Select individual VPI/VCI • Select range of VCIs with one VPI • Select range of VPIs with one VCI • Select range of VPIs with range of VCIs • Select any combination of above • Duplicate VPI/VCI selection permitted
Channel Distribution	• Stream bandwidth divided equally amongst selected channels • Channel bandwidth = (Stream bandwidth / Number of channels in stream)
Channel Assignment	• Within a single stream, a sequence of "Burst Length" cells are transmitted on each channel in turn, repeating when all channels have been used.

Header Generation

Channel Header Controls	• Interface: UNI or NNI • GFC: 0 to 0xF (UNI mode only) • VPI: 0 to 0xFF (UNI mode); 0 to 0xFFF (NNI mode) • VCI: 0 to 0xFFFF • PTI: 0 to 7 • CLP: 0 or 1

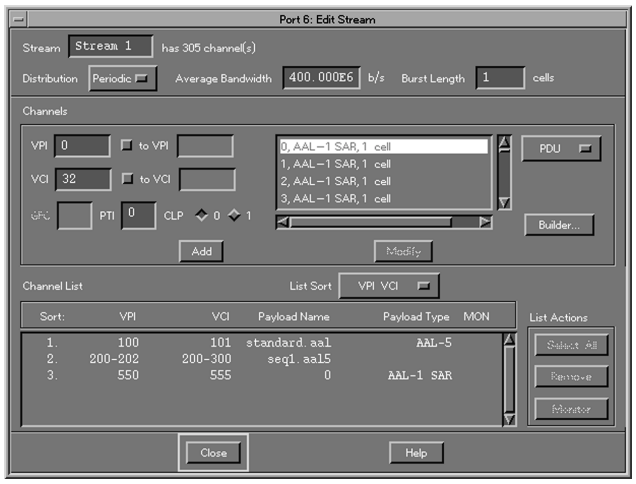
PDU Payload Generation

Adaptation Layer	• AAL-0, AAL-5 CPCS
ATM Cell layer	• Cell type may be set to ATM, OAM, or RM • Interface & Header fields defined by Channel Header Controls • When set to "ATM" mode payload data may be set under user control. Five built in patterns: user value, alternating FF 00, alternating AA 55, incrementing or Single-PRBS9 • When set to OAM or RM modes an appropriate editor is enabled which allows specification of OAM and RM cell fields • Cross-cell PRBS-23 insertion
AAL-5 CPCS	• Payload information length specified under user control. Length may be set from 1 to 65535 • Payload data may be set under user control. Five built in patterns: user value, alternating FF 00, alternating AA 55, incrementing or Single-PRBS9 • Pad length may be specified by the user or may be automatically calculated • Pad octet may be set by the user • CPCS trailer, User-user indication, common part indicator may be specified under user control • CPCS trailer length and CRC-32 may be specified manually or may be automatically calculated
Test cell description	• Employs ITU-T O.191 test cell • 32-bit timestamp insertion • 32-bit sequence number • CRC-16 generation • Scrambler Mode: On or Off
Test frame description	• Test frames can be transmitted with specific frame sizes (cell length) (1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 1365) • Employs O.191 cell sequence with the addition of an AAL-5 CRC-32 insertion for the last cell of the test frame (AAL-5 PDU)

PDU and PDU Sequence Builder

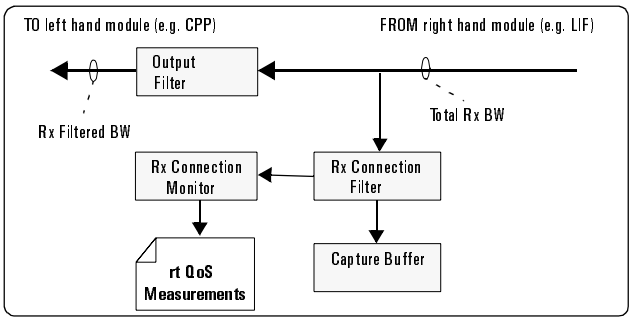
Channel contents may be built using the traffic generator dialog. PDUs (protocol data units) may be built at the ATM cell layer, adaptation layer (AAL–1, AAL–2, AAL–3/4, AAL–5) and service layer. PDUs may be transmitted individually or they may be linked to form complex sequences.

PDU Buffer	• 131,072 cells (shared across all traffic generator streams)
Licensing	• Access to higher layer PDUs and PDU Sequences is available to the ASP. Installation of the appropriate AAL test products and licences is required before loading is attempted
Channel Override	• Encoded PDUs and PDU sequences inherit VPI/VCI from internal traffic generator setting



Traffic Generator Engine: PDUs and PDU Sequences can be developed quickly.

Receive Functionality



155 Mb/s Cell Bus Interface

Output Mode	• Specialized test modules (such as the E4209B Cell Protocol Processor) to the left of this module can monitor cells from the received traffic stream that match the output filters • Limited to the maximum bandwidth of the 155 Mb/s cell bus • Limited to the allowable configurations of the Test System Manager
Pass-Through Mode	• Cells from the 155 Mb/s cell bus to the right of this module are passed unchanged to the 155 Mb/s cell bus to the left of this module • Enables surrounding modules to be used together, bypassing this module

622 Mb/s Cell Bus Interface

Output Mode	• The high speed ASP can monitor cells from other high-speed test modules (such as the E1618A 622 Mb/s Optical Line Interface) to the right of this module • The high speed ASP is limited to the maximum bandwidth of the 622 Mb/s cell bus • The high speed ASP is limited to the allowable configurations of the Test System Manager

Link Control

Network Interface	• Select UNI or NNI
Overflow Mode	• Selects the way in which the drop buffer handles incoming cells after it has been filled. • Select Continuous or Intermittent (default = Intermittent)

155 Mb/s Cell Bus Control

Selection	• On: ATM cells from the received traffic stream that match the output filters are placed on the 155 Mb/s cell bus (for monitoring using modules such as the E4209B Cell Protocol Processor) • Off: No cells are placed on the 155 Mb/s cell bus
Idle/Unassigned Fill Cell Filter	• On: Idle/Unassigned cells are never placed on the 155 Mb/s cell bus • Off: All received cells, including Idle/Unassigned cells, are placed on the 155 Mb/s cell bus

Receive Connection Filters

Number of Connection Filters	• 8
Pattern Match Fields per Filter	• GFC (UNI mode): single value or "any" • VPI: single value or "any" • VCI: single value or "any" • PTI: bit mask and bit value (3 bits) • CLP: single value or "any"
Quick Fill Default Values	• All: VPI = "any", VCI = "any" • Signalling channel: VPI = 0, VCI = 5 • OAM F4 Segment: VPI = "any", VCI = 3 • OAM F4 End-to-End: VPI = "any", VCI = 4 • OAM F5 Segment: VPI = "any", VCI = "any", PT = 100 • OAM F5 End VPI = "any", VCI = "any", PT = 101

Actions	• Output to any module to the left hand side of the ATM Stream Processor (i.e. CPP or OPT) from one to eight connections • Monitor up to two of the eight available connections in detail. Refer to Receive Connection Monitor Measurements in a later section • Capture up to eight connections at full line rate

Output Buffer

The output buffer is used to buffer cells before they are placed on the 155 Mb/s cell bus (for monitoring using specialized modules such as the E4209B Cell Protocol Processor). The buffer smooths short bursts of cells that exceed the maximum bandwidth of the cell bus, to reduce the likelihood of losing cells.

Buffer Size	• 131,072 cells
Time to Fill Buffer	• For input rates greater than 149.76 Mb/s: 55574.528 / (input Mb/s - 149.76) ms • For maximum ATM bandwidth input rate (599.04 Mb/s): 123.7 ms
Time to Empty Full Buffer	• 371.1 ms
Buffer Modes	• Intermittent Mode: Overflow cells are discarded (buffer operates as FIFO and will support CPP emulation applications) • Continuous Mode: If buffer fills and overflows, it is locked from further input until it is empty (providing 123.7 ms snapshots of 131,072 consecutive cells) – used for protocol decoding higher-layer protocol PDUs
Overflow indication	• Drop Overflow (DOVL) alarm measurement and front panel indication • See Measurements and Electrical and Mechanical sections for more detail

Capture Buffer

The capture buffer is used to capture receive traffic for protocol analysis and post-processing.

Buffer Size	• 262,144 cells
Idle/Unassigned Fill Cell Filter	• On: Idle/Unassigned cells are not saved in the capture buffer • Off: All received cells, including Idle/Unassigned cells, are saved in the capture buffer

Real-Time Measurements

Measurements are taken continuously in realtime, collected every 100 milliseconds and accumulated over the user-specified measurement period. Results from the most recent complete measurement period are retained.

Measurement System

Result Types	• Cumulative: Measurements since the start of the Measurement Period • Latched: Measurements during most recently completed measurement period • Last Second: Measurements during most recently completed 1 second period (dynamic update)
Result Formats	• Cells • Seconds • Ratios • Bandwidth – units bits/s, cells/s, or PDUs/s
Accuracy of Counts	• +/–1 for counts < 1000 • +/–0.1% for counts > = 1000
Accuracy of Ratios	• +/–0.2% for counts > = 1000
Accuracy of Bandwidths	• +/–1 count (cell or PDU) per measurement period
Measurement Period	• Range: 1 second to 3 days • Resolution: 1 second
Control	• Start / Stop / Continuous
Visual Update	• Maximum user-interface update period: 5 seconds

Transmit Link and Alarm Measurements

Tx Inserted Cell Bandwidth (bits/s and cells/s)	• Mean bandwidth of ATM cells inserted from the cell bus
Tx Inserted Cell Count (cells)	• Total cell count of ATM cells inserted from the cell bus
Tx ASP Cell Bandwidth (bits/s and cells/s)	• Mean bandwidth of ATM cells transmitted from internal traffic generator
Tx ASP Cell Count (cells)	• Total ATM cells transmitted from the ASP
Tx Total Generated Bandwidth (bits/s and cells/s)	• Total mean bandwidth of ATM cells inserted from cell bus and generated by the ASP
Tx Total Generated Cell Count (cells)	• Total cell count of ATM cells inserted from cell bus and generated by the ASP
Tx Traffic Generator Not Satisfied (errored seconds)	• Traffic generator not satisfied errored seconds

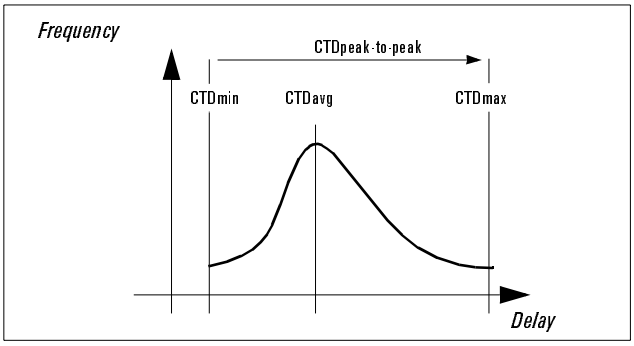
Transmit Monitor Measurements

Number of Monitored Streams	• 1
Number of Channels per Stream	• 1 to 2,048
Number of monitored channels per Stream	• 1 to 2,048
ATM Bandwidth (bits/s and cells/s)	• Aggregate mean bandwidth across all monitored channels
ATM Cell Count (cells)	• Total cell count of ATM cells generated by the ATM Stream Processor across all monitored channels
CLP = 0/CLP = 1 Bandwidth (bits/s and cells/s)	• Aggregate mean bandwidth of ATM cells with CLP = 0/CLP = 1 across all monitored channels

CLP=0/CLP = 1 Cell Count (cells)	• Total cell count of ATM cells with CLP=0/CLP=1 across all monitored channels
CLP=0/CLP=1 Ratio	• The ratio of CLP = 0/CLP=1 cells transmitted to the total cell count (CLP=0+1) across all monitored channels
PT=0X1 Bandwidth (bits/s and cells/s)	• Aggregate mean bandwidth of ATM cells with PT=0X1 across all monitored channels
PT=0X1 Cell Count (cells)	• Total cell count of ATM cells with PT=0X1 across all monitored channels

Receive Link and Alarm Measurements

ATM Cell Count (cells)	• Count of ATM cells received (non-fill)
ATM Cell Bandwidth (bits/s and cell/s)	• Bandwidth of ATM cells received (non-fill)
Total Cell Count (cells)	• Count of total cells received
Total Cell Bandwidth (bits/s and cell/s)	• Bandwidth of total cells received
Filtered Cell Count (cells)	• Count of cells for all connections that have been selected to be dropped to the left of the ASP. • If the output buffer has not overflowed, then this is equal to the count of ATM cells placed on the 155 Mb/s cell bus
Filtered Cell Bandwidth (bits/s and cell/s)	• Bandwidth of cells for all connections that have been selected to be dropped to the left of the ASP.
Rx Drop Overflow (errored seconds)	• Number of whole or partial seconds during which cells selected to be dropped were discarded due to a drop overflow (DOVL)
Rx No Cell Received (errored seconds)	• Number of whole or partial seconds during which no cells were received by the ASP



Calculating CDV and peak-to-peak cell delay variation (CDV)

Receive Connection Monitor Measurements

Number of Monitored Connections	• 2
Monitored Channels per Connection	• 1 to 16,384 VCs
Selected Cell Bandwidth (bits/s and cells/s)	• Total bandwidth of cells for the monitored connection
Selected Cell Count (cells)	• Total cell count for the monitored connection
Selected PT=0X1 Bandwidth (bits/s and cells/s)	• Total PT=0X1 cell bandwidth for the monitored connection
PT=0X1 Count (cells)	• Total PT=0X1 cell count for the monitored connection
Valid AAL-5 PDU Bandwidth (bits/s and cells/s)	• Valid AAL-5 PDU bandwidth (no CRC-32 error, PDU length < 65536 bytes, last cell PT=0X1) for the monitored connection
Valid AAL-5 PDU Count (cells)	• Valid AAL-5 PDU count (no CRC-32 error, PDU length < 65536 bytes, last cell PT=0X1) for the monitored connection
AAL-5 CRC-32 Errored PDUs/s (PDUs/s)	• AAL-5 PDU CRC-32 count (last cell PT=0X1; maximum 1 error per PDU) for the connection
AAL-5 CRC-3 Errored PDU Count (PDUs)	• AAL-5 PDU CRC-32 count (last cell PT=0X1; maximum 1 error per PDU) for the monitored connection
CLP=0/CLP=1 Cell Bandwidth (bits/s and cells/s)	• Bandwidth with Cell Loss Priority bit set to CLP=0/CLP=1 for the monitored connection
CLP=0/CLP=1 Cell Count (cells)	• Count of cells with Cell Loss Priority bit set to CLP=0/CLP=1 for the monitored connection
CLP=0/CLP=1 Ratio	• The ratio of cells with Cell Loss Priority bit set to CLP=0/CLP=1 to the total cell count (CLP=0 + 1) for the monitored connection
CLP=1 Converted Count (cells)	• Count of the number of cells converted from CLP=0 to CLP=1 for the monitored connection
CLP=1 Converted Ratio	• A ratio of the number of cells received with CLP converted from 0 to 1 divided by the number of cells transmitted with CLP=0 for the monitored connection
CLP=1 Converted Bandwidth (bits/s and cells/s)	• For the selected connection the bandwidth of traffic that has been converted from CLP=0 to CLP=1.
Cell Loss (cells)	• Total number of cells lost for the connection
Cell Loss Ratio	• A ratio of the number of received cells to the total number of transmitted cells for the monitored connection
Lost Cell Bandwidth (bits/s and cell/s)	• The lost cell bandwidth for the monitored connection
Cell Transfer Delay (maximum, minimum, average) (seconds)	• The cell transfer delay (CTD) for the monitored connection
Cell Delay Variation (seconds)	• The larger of the difference between either the maximum CTD and the average CTD, or the minimum CTD and the average CTD.

Peak-to-Peak Cell Delay Variation (seconds)	• The difference between the maximum and minimum CTD for the measurement period.
O.191 Errored Cell Count (cells)	• Total O.191 cell error count for the monitored connection
O.191 Errored Bandwidth (bits/s and cell/s)	• Total O.191 errored cell bandwidth for the monitored connection
PRBS-23 Errored Cell Count (cells)	• Total PRBS-23 errored cell count for the monitored connection
PRBS-23 Errored Cell Bandwidth (cells/s)	• Connection bandwidth of PRBS-23 errored cells

Dynamic Measurements

Transmit Total Generated Bandwidth (bits/s and cells/s)	• Total mean bandwidth of ATM cells inserted from cell bus and generated by the internal traffic generator
Transmit ASP Cell Bandwidth (bits/s and cells/s)	• Mean bandwidth of ATM cells transmitted from internal traffic generator
Inserted Cell Bandwidth (bits/s and cells/s)	• Mean bandwidth of ATM cells inserted from the 155 Mb/s cell bus
Remaining Available Transmit Bandwidth (bits/s and cells/s)	• Remaining ATM bandwidth available to internal traffic generator
Receive ATM Cell Bandwidth (bits/s and cell/s)	• Bandwidth of ATM cells received (non-fill)
Filtered Cell Average Bandwidth (bits/s and cells/s)	• Average bandwidth of cells (ATM or total) matched by the output filters, averaged over last complete 1 second period) • If the output buffer has not overflowed, then this is equal to the average bandwidth of cells (ATM or total) placed on the 155 Mb/s cell bus
Connection Average Cell Bandwidth (bits/s or cells/s)	• Selected connection cell bandwidth averaged over last complete 1 second period • Available on up to 8 connections simultaneously

Electrical & Mechanical Specification

Electrical Interface

External Trigger Input Tx	• Connector Type: SMB bulkhead receptacle • Input Levels: TTL sink (V_{IL} < =0.8V, V_{IH} > =2.0V) • Input Impedance: 50 ohm
External Trigger Input Rx	• Connector Type: SMB bulkhead receptacle • Input Levels: TTL sink (V_{IL} < =0.8V, V_{IH} > =2.0V) • Input Impedance: 50 ohm
External Trigger Output Tx	• Connector Type: SMB bulkhead receptacle • Output Levels: TTL source (V_{OL} < =0.8V, V_{OH} > =2.0V) • Output Impedance: 50 ohm
External Trigger Output Rx	• Connector Type: SMB bulkhead receptacle • Output Levels: TTL source (V_{OL} < =0.8V, V_{OH} > =2.0V) • Output Impedance: 50 ohm

Triggers

Nominal Pulse Width	• 50 ns
Triggers	• RX Input Start/Stop Capture • Select positive or negative edge

VXI Module

Size	• 1 slot C-size VXI card
Weight	• 2.0 kg nominal
Power Dissipation	• 79 Watts (max)
Backplane Connectors	• P1, P2
Addressing	• Logical and servant addressing

Front Panel LED Indicators

Tx	• On: module is configured in insert mode by the Test System Manager (to insert generated cells to the cell bus), and cells are being inserted • Off: module is configured to pass-through mode by Test System Manager
Rx	• On: module is configured in output mode to place selected received cells onto the 155 Mb/s cell bus, and at least 1 cell per second is being placed on the bus • Off: module is configured to pass-through mode by Test System Manager
DOVL	• On: 155 Mb/s cell bus output buffer overflows
QoS	• Off: Quality of Service (QoS) does not exceed specified threshold • On: Quality of Service (QoS) exceeds specified threshold • Not used in release 1.2

Environmental Operating Conditions

Operating Temperature	• 0°C to 45°C • Jitter transfer specification maintained over the range 10°C to 55°C
Storage Temperature	• –40°C to 70°C
Humidity	• 0% to 95% relative humidity from 25°C to 40°C

Applicable Standards

ATM Cells	• ITU-T I.361 B-ISDN ATM Layer Specification 1995
ATM Forum TM4.0	• Traffic Management Specification Version 4.0 af-tm-0056.000 4/1996
ITU-T I.356	• B-ISDN ATM Layer Cell Performance 11/1993
ITU-T I.357	• B-ISDN Semipermanent Connection Availability 8/1996
ITU-T I.371	• Traffic Control and Congestion Control in B-ISDN 11/1995
ITU-T I.150	• B-ISDN Asynchronous Transfer Mode Characteristics 3/1993
ATM Test Cell	• ITU-T Recommendation O.191 — Specifications of Measuring Equipment – Equipment to Assess ATM Layer Cell Transfer Performance 12/96
Performance Testing	• ATM Forum Performance Testing (Draft Specification)

Acronyms

AAL-5	ATM Adaptation Layer 5
ABR	Available Bit Rate
ASP	Agilent E1607/E1609A ATM Stream Processor
ATM	Asynchronous Transfer Mode
BSTS	Agilent Broadband Series Test System
BW	Bandwidth
CLP	Cell Loss Priority
CPP	Agilent E4209B Cell Protocol Processor
CRC	Cyclic Redundancy Check
DOVL	Drop Overflow
GFC	Generic Cell Rate Algorithm
LED	Light Emitting Diode
OAM	Operations, Administration and Maintenance
OC-12c	Optical Carrier Level 12 Signal Concatenated
OPT	Agilent E6270A OAM Protocol Tester
PDU	Protocol Data Unit
PRBS	Pseudo Random Binary Sequence
PTI	Payload Type Identifier
PVC	Permanent Virtual Circuit
QoS	Quality of Service
Rx	Receive
SDH	Synchronous Digital Hierarchy
SMB	Subminiature Type B
SONET	Synchronous Optical Network
STM	Synchronous Transfer Mode
SVC	Switched Virtual Circuit
Tcl	Tool Command Language
Tk	Graphical User Interface Toolkit for Tcl
TGNS	Traffic Generator Not Satisfied
Tx	Transmit
UNI	User Network Interface
VBR	Variable Bit Rate
VC	Virtual Circuit
VCI	Virtual Circuit Identifier
VP	Virtual Path
VPI	Virtual Path Identifier
UBR	Unspecified Bit Rate

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The Agilent Technologies BSTS is the industry-standard ATM/BISDN test system for R&D engineering, product development, field trials and QA testing. The latest leading edge, innovative solutions help you lead the fast-packet revolution and reshape tomorrow's networks. It offers a wide range of applications:

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