

Agilent E8877A/AN Agilent EEsof EDA cdma2000-Compliant Design Library

Product Overview

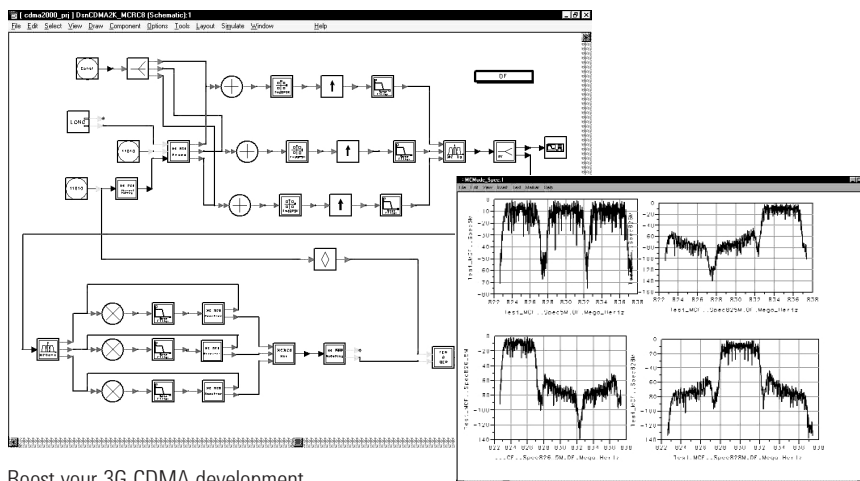
Making the cdma2000-Compliant Design Library a Part of Your Design Flow:

- Speeds your cdma2000 design time-to-market
- Verifies design performance to IS-2000 specifications
- Helps you get your hardware right the first time
- Simplifies signal source configuration with the cdma2000-Compliant DesignGuide

The cdma2000-Compliant Design Library, an Agilent Technologies' EEsof EDA product, helps ensure successful development of code division multiple access (CDMA) communications products based on the physical layer specifications in the TIA IS-2000 standards. With this library, you can design the RF portion of IS-2000 devices and use pre-built test benches to verify that the designs are specification compliant. Seamless links to Agilent test equipment help you perform quick and consistent hardware verification.

A Comprehensive 3G CDMA Solution, from RF/Analog to Baseband/Digital

In addition to a complete set of behavioral models conforming to specifications, this library contains pre-built simulation systems and application examples. This complete tool set allows you to easily explore your cdma2000 designs to achieve higher performance and superior hardware implementation efficiency.



Boost your 3G CDMA development

The cdma2000-Compliant Design Library works with the Advanced Design System, an easy-to-use and powerful design tool in the Agilent EEsof EDA product line.

Advanced Design System gives you access to a wide array of analog, DSP, and RF behavioral models in a user-friendly and highly integrated design environment. Whether your goal is baseband or analog/RF processing or mixed-signal system-on-chip (SOC), Advanced Design System and the cdma2000-Compliant Design Library let you quickly and accurately design and verify cdma2000 system implementations, allowing you to rapidly develop cdma2000 chipsets.

The Advanced Design System development environment provides you with a variety of RF, DSP, system, and RFIC design and simulation tools such as Agilent Ptolemy, Circuit Envelope, SPICE, and MATLAB.® In addition, the Advanced Design System allows you to link test and measurement equipment such as the Agilent ESG-D digital RF signal generator or vector signal analyzer to your design. This link lets you refine your designs comprehensively at the system-level and replace behavioral models with actual circuit designs or measured data. After your design is partitioned into the analog, digital, and high-frequency RF portions, you can use Agilent DSP Synthesis to move DSP designs into register transfer level HDL netlists for subsequent logic synthesis and implementation into silicon.



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cdma2000-Compliant DesignGuide and Application Examples

Configuring the right source is one of the most challenging aspects of circuit simulation. The cdma2000-Compliant DesignGuide provides an easy way to select the right source for the simulation you want to perform. A tab dialog provides choices for the forward and reverse data link as well as single-channel sources and multi-channel sources. This DesignGuide reduces error-prone simulation setup and saves you the effort of configuring the schematic and preparing the data display.

This DesignGuide is available at no additional cost when you purchase the cdma2000-Compliant Design Library.

cdma2000-Compliant Design Library Features

- Rake receivers for both forward link and reverse link
- Forward link transmissions with spreading rate 1 (SR1) and spreading rate 3 (SR3)
- Reverse link transmissions with SR1 and SR3
- Reverse link with HPSK modulation (SR1 and SR3)
- Channel encoding with turbo codes with BER/FER measurement
- Measurement of ACPR, CCDF and EVM
- A variety of radio configurations (RC)
- Transmission power control for both forward and reverse links
- Complete RF transmitter and receiver design capability, including non-linear components, phase noise, and inter-modulation distortion

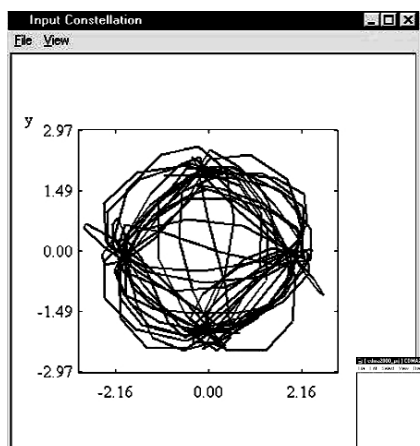
- Fully compliant with the IS-2000 standard specification
- Complete system structure on physical layer
- New pilot-aided coherent demodulation algorithm for reverse link
- New channel coding scheme, including turbo codes
- Mapping and de-mapping for rate matching by puncture and repetition
- Two transmit diversity schemes, including Orthogonal Transmit Diversity (OTD) and Multi-Carrier (MC)
- Advanced simulation structure to support data/packet services simulation
- Easy-to-use, hierarchical and realizable models and sub-networks
- Model verification using Agilent test and measurement equipment

3G CDMA System-Level Design

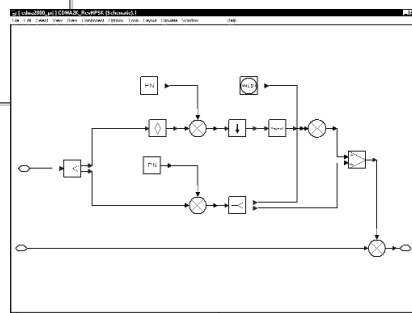
To reduce your cost and time to market, the cdma2000-Compliant Design Library provides the system-level environment you need to complete high-level designs and partitioning. The library models the complete system structure on the physical layer, compliant with IS-2000 specifications.

The library includes advanced features such as hybrid phase-shift keying (HPSK), spreading (reverse link), pilot aided coherent demodulation (reverse link), channel coding including turbo codes, mapping and de-mapping scheme for rate matching, and orthogonal transmit diversity (OTD). For example, turbo codes are employed for higher data rates in order to achieve a near-Shannon limit capacity performance.

With the CDMA and cdma2000 library models and other models available within Agilent Communication Systems Designer or DSP Designer, you can model a complete cdma2000 system, either handset or basestation, including baseband digital signal processors and analog/RF circuits.



You can use the HPSK modulation models and examples to generate coded signals or perform end-to-end simulations.



Hardware Implementation

When your partitioned system-level design meets performance requirements, you can move the partitioned design to implementation. The Advanced Design System includes a full range of technologies to help you design the necessary analog, RF, and DSP circuits. DSP algorithms are prepared for implementation using HDL code generation models, HDL simulation, and DSP behavioral synthesis.

The system's HDL generator outputs either VHDL or Verilog and their test environments. This reduces the need for hand coding and for translating test vectors.

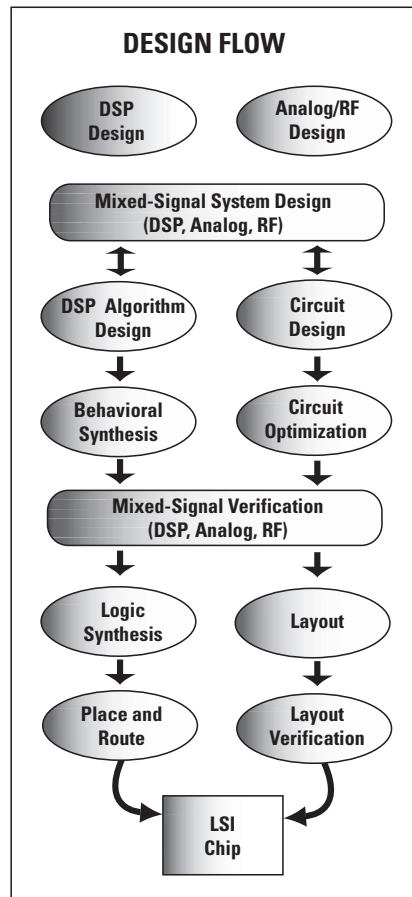
You can download coded signals for hardware testing using a built-in link to the Agilent ESG-D RF digital signal generator. This powerful feature helps to reduce mistakes commonly found during the integration and test phase of design. Agilent EEsof EDA engineers have double-checked the cdma2000 models and test bench designs using the ESG-D instrument with cdma2000 option and have verified that simulation results exactly match those of the signal generator.

The Advanced Design System RFIC Designer and RF Board Designer modules include the necessary technologies for implementing analog and RF circuit designs. Simulation technologies include SPICE, Harmonic Balance, and Circuit Envelope, to allow the widest range of design capabilities. They also include physical design capabilities and links to back-end tools to move your IC or board designs into your company-wide design infrastructure.

Designs with synthesizable models are verified before code generation. Synthesizable models allow you to generate HDL codes and eliminate time-consuming hand coding.

Product Configuration

The cdma2000-Compliant Design Library (E8877A/AN) requires CDMA Design Library (E8857A/AN) and works directly with DSP Designer Pro (E8821A/AN) or Communication Systems Designer Pro or Premier (E8851A/AN or E8852A/AN), all of which work with the Advanced Design System. For other possible product configurations, please consult your local Agilent representative.



An integrated design flow, with the Advanced Design System and cdma2000-Compliant Design Library, increases engineering efficiency and accelerates time-to-market for a 3G CDMA chipset.

Comprehensive Components and Test Benches

Receiver

- Channel Estimator (FL/RL)
- Coherent Receiver (FL/RL)
- Coefficient Down Sampling
- Carrier Frequency Estimator
- Phase Detector
- HPSK Demodulator

Channel Coding

- Block Interleaver
- Block De-Interleaver
- Convolutional Encoder (with tail bits)
- Viterbi Decoder (with tail bits)
- CRC Encoder/Decoder
- Puncture/De-Puncture
- MAP Decoder1
- MAP Decoder2
- Symbol Cyclic Shifter
- Turbo De-interleaver
- Turbo De-multiplexer
- Turbo Interleaver
- Turbo Multiplexer
- Variable Rate CC with Tail
- Variable Rate Convolutional encoder/Viterbi decoder
- Comparator
- De-framing (Variable Rate)
- Framing (Variable Rate)
- Rate De-Matching (Variable Rate)
- Rate Matching (Variable Rate)
- 4 to 1 Selector (Variable Rate)
- Rate Source (Variable Rate)
- Blind Decoder
- OTD De-Interleaver
- OTD Interleaver
- Turbo Base Decoder
- Turbo Decoder
- Turbo Encoder
- Turbo RSC Encoder

Transmission

- -BTS TX-
- Data Scrambling
- PC-Bit Extraction (FL)
- PC-Bit Puncture (FL)
- Power Allocation (FL)
- Long Code Generator
- -MS TX-
- PN Code
- Power Control
- Quasi Orthogonal Mask
- PC-Bit Puncture (RL)
- Variable Length Walsh Code
- Baseband Filter
- Walsh Modulator
- Walsh Rotator
- QPSK (FL) Modulator and Demodulator
- HPSK (RL) Modulator and Demodulator

Sub-network designs

- Blind Decoder for all rate configurations (RL)
- Carrier Frequency Estimator
- MC Mode De-Interleaver
- MC Mode Interleaver
- One-way Decoders for all rate configurations (RL)
- Phase Detector
- HPSK Modulator (RL)
- HPSK Demodulator (RL)
- Turbo Base Decoder
- Turbo Decoder
- Turbo Encoder
- Turbo RSC Encoder
- Amplitude Adjuster
- Walsh Modulator
- Walsh Rotator

For more information about Agilent EEsof EDA visit:

www.agilent.com/eesof-eda

For more assistance with your test & measurement needs visit:

www.agilent.com/find/assist

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