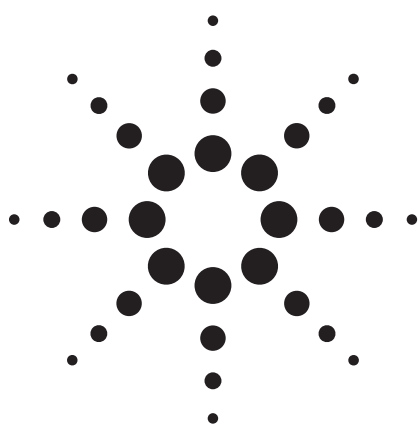


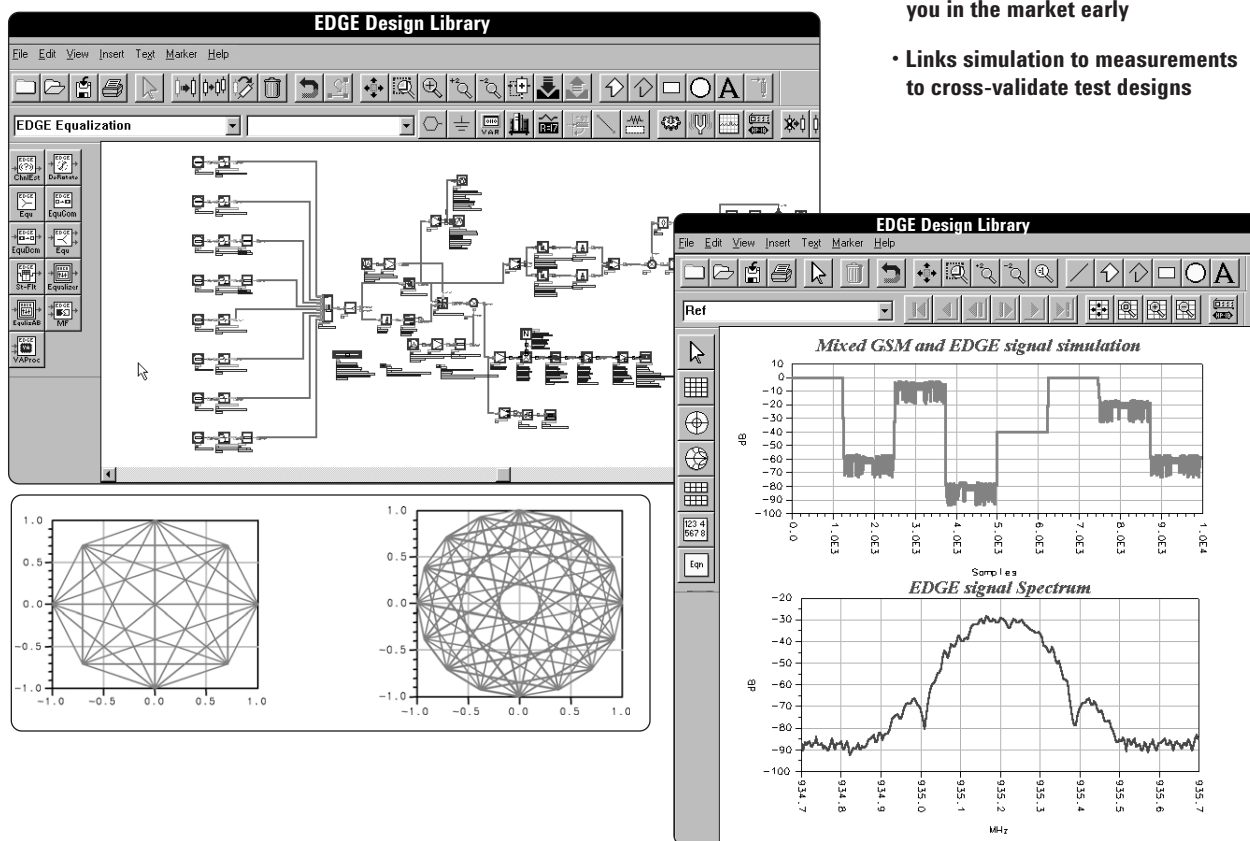


Agilent E8879A/AN EDGE Design Library

Product Overview

Making EDGE Design Library a part of your design flow:

- Simulates and verifies your design against specification
- Tests your RF designs with up-to-date EDGE signal formats – gets you in the market early
- Links simulation to measurements to cross-validate test designs



The EDGE Design Library from Agilent EEsof EDA helps speed development of wireless products that are based on the EDGE (Enhanced Data Rates for GSM Evolution) standard. With this library, you can develop and refine specification-compliant algorithms at the system level, where design choices have the greatest impact. Using seamless links to other Advanced Design System (ADS)

options, in particular analog/RF circuits and DSP implementation, you quickly verify your design based on specification.

EDGE is part of the European Telecommunication Standard Institute's (ETSI) strategy for GSM evolution toward third-generation wideband multimedia services. EDGE uses the 8PSK modulation technique and channel coding

schemes to enable wireless multimedia IP-based data services and applications in GSM at speeds of 384kbit/s with a bit rate of 48kbit/s per timeslot and, under good radio conditions, up to 69.2kbit/s per timeslot. It also uses existing GSM radio bands, the same TDMA (Time Division Multiple Access) frame structure, logic channel, and 200-kHz carrier bandwidth as today's GSM networks, allowing existing cell plans to remain intact.



Agilent Technologies

Innovating the HP Way

A Comprehensive Solution in an Integrated Platform

The EDGE Design Library includes all the necessary models and subcircuits to perform a bit-to-bit simulation of an EDGE system. In addition to the complete set of behavioral models, pre-built test and verification projects are included with this library. This allows you to explore your designs further for higher performance with superior efficiency, and to test and quickly verify your particular implementation based on specification.

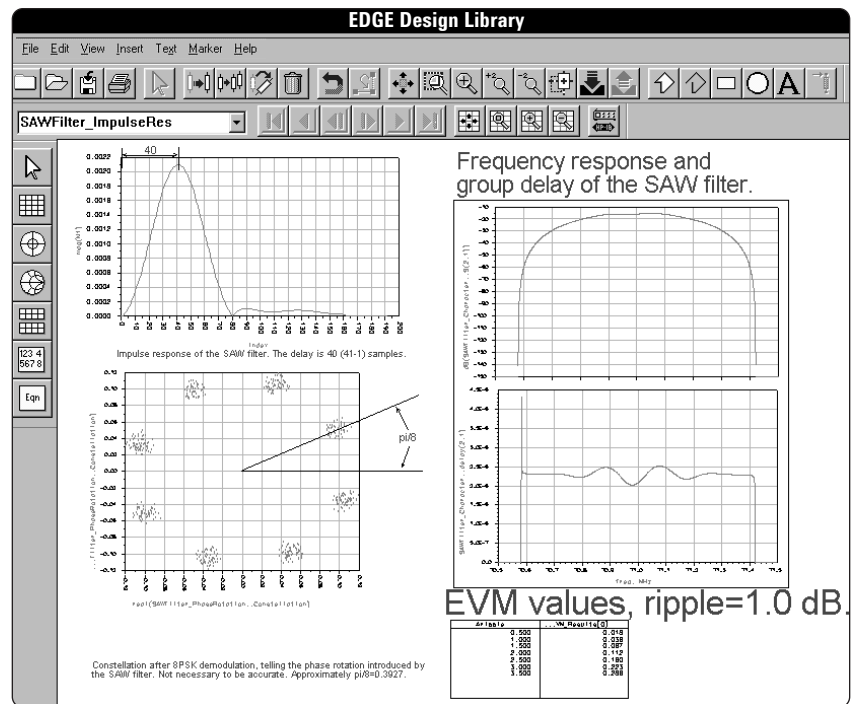
This library is a companion product to Advanced Design System (ADS), a powerful EDA software system that provides access to a wide array of analog, DSP, and RF behavioral models in a user-friendly and highly integrated design environment. It allows quick and accurate modifications to your particular implementation of EDGE, enabling you to build your own proprietary EDGE design. The development environment in ADS offers a variety of design and simulation tools such as Agilent Ptolemy, Circuit Envelope, SPICE, and MATLAB®.

Furthermore, the ADS platform links your test and measurement equipment, such as ESG-D RF digital signal generator or vector signal analyzer, to your design. This link lets you refine your designs comprehensively at the system level and replace behavioral models with actual circuits or measured data.

Complete EDGE Model Set for Baseband Processing and Signal Generation

The EDGE Design Library includes more than 100 models for:

- Channel Coding
- Equalization
- Framing
- Modems
- RF Subsystems
- Synchronization
- Signal Sources
- Measurement
- BTS Test and Verification
- MS Test and Verification



This data display shows Error Vector Magnitude (EVM) simulation results.

This design library includes the key features of the EDGE system in the physical layer, such as channel coding and interleaving (for modulation and coding schemes MCS-1 to MCS-9) in downlink and uplink, burst assembly, 8PSK modulation, bit synchronization, adaptive equalization, and FER, BER, and EVM measurements. It provides a number of EDGE sources for generation of EDGE modulated signal or EDGE frame signal. You can select GMSK or modified 8PSK for any of the time slots in the EDGE frame.

Critical Transmitter and Receiver Test and Verification Projects

With Agilent ADS and EDGE Design Library, you can rapidly design and verify EDGE base stations and handsets based on the EDGE standards. The library includes a number of key test and verification pre-configured projects for base transceiver station (BTS) and mobile station (MS). These designs are based on GSM 11.21, GSM11.10, and corresponding EDGE documents (change requests). The designs include configured data display files and reference data sets.

Test and Verification Projects for BTS (Transmitter and Receiver) Include:

- Modulation Accuracy
- Mean Transmitted RF Carrier Power
- Transmitted RF Carrier Power versus Time
- Adjacent-Channel Power
- Static Reference Sensitivity Level
- Multipath Reference Sensitivity Level
- Reference Interference Level
- Blocking Characteristics

Test and Verification Projects for MS (Transmitter and Receiver) Include:

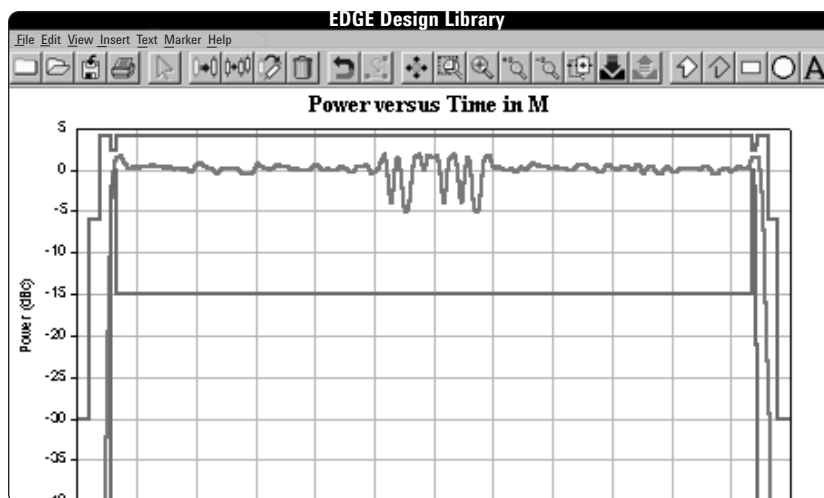
- 8PSK Frequency Error and Modulation Accuracy Measurement
- Transmitter Output Power
- Output RF Spectrum in EGPRS
- Minimum Input Level for Reference Performance
- Co-Channel Rejection
- Adjacent-Channel Rejection

From Concept to Verification

When your partitioned system-level EDGE design meets performance requirements, you can perform simulation at the system level (including RF/analog parts) to verify the design.

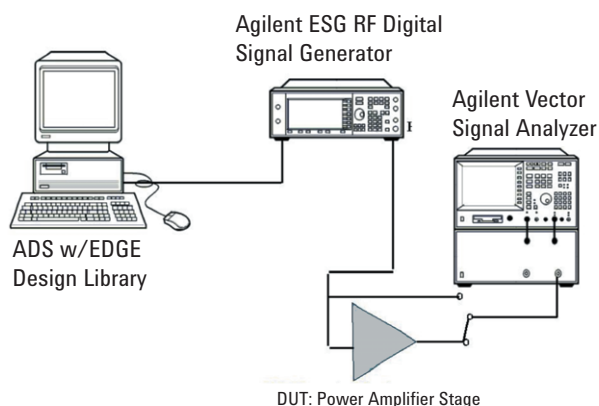
ADS includes a full range of capabilities to help you design analog, RF, and DSP circuits. In addition, using ADS links to instruments such as Agilent ESG-D RF digital signal generator or 89600-series vector signal analyzer (VSA) provide valuable test and verification capability. You can generate clean EDGE signal, pass it through any “virtual” design in ADS, and then send the “distorted” output I&Q data to ESG and VSA to perform desired measurements. You can also include an actual hardware prototype in this loop for further analysis and/or verification.

ADS RFIC Designer and RF Board Designer modules include the technologies needed to implement analog and RF circuit designs. The simulation technologies of the modules include SPICE, Harmonic Balance, and Circuit Envelope to allow the widest range of design capabilities. They also include physical design capabilities and links to back-end tools to move your IC or board designs into the company-wide design framework.



The plot above shows a power versus time simulation compared to the mask specified in the EDGE standard.

Measurement Setup



The illustration shows a typical measurement setup with ADS linked to a digital electronic signal generator and a vector signal analyzer.

Library Components List

EDGE, Channel Coding

Convolutional encoder bit by bit
Bit de-swapping in normal burst
Bit swapping in normal burst
Normal burst demapping
Normal burst mapping
Convolutional encoder with tail
Bits combiner
Systematic cyclic codes decoder
Systematic cyclic codes encoder
Viterbi decoder for convolutional code with tail
De-interleaving for packet data traffic channels
Data depuncturing
Add or remove extra stealing flags for MCS1-4
Header de-interleaver
Header de-puncture
Header interleaver
Header puncture
Interleaving for packet data traffic channels
MCS 1-9 encoder for uplink
MCS 1-9 encoder for downlink
MCS 1-9 decoder for uplink
MCS 1-9 decoder for downlink
Data puncturing

Reed-Solomon decoder

Reed-Solomon encoder
Block splitter for channel coding
Tailing bits adder or remover
USF postdecoder
USF pre-encoder
Viterbi decoder bit by bit for convolutional code

EDGE, RF Subsystems

RF mod
RF demod
RF transmitter with input IF
RF receiver with output IF

EDGE, Framing

Access burst disassembly
Normal burst disassembly
Synchronization burst disassembly
TDMA frame disassembly
Dummy burst construction
Frequency correction burst construction
Normal burst construction
Synchronization burst construction
TDMA frame construction

EDGE, Modems
8PSK modulator
Phase rotator used in 8PSK modulation
Pulse shaping filter
Receive filter
EDGE, Synchronization
Bit synchronization for 8PSK modulated bursts
EDGE burst down sample
Index of sequence with peak correlation value
Training bit generation
EDGE, Equalization
Channel estimator
De-rotator
Bi-directional equalization combiner
Equalization access burst composer
Equalization access burst decomposer
Bi-directional equalization splitter
State index to float translation
Adaptive equalizer for normal and synchronization bursts
Adaptive equalizer for access bursts
Matched filter
Viterbi algorithm processor
EDGE, Signal Sources
BTS MCS5-9 power control source
MS MCS5-9 power control source
Active-idle source
EDGE, Measurement
BER and FER performance
EVM sink for EDGE
Nonlinear power amplifier
Average signal power measurement
Frequency error
Raised-cosine windowed raised-cosine filter
Signal power measurement
EVM with reference data input

Product Configuration

The EDGE Design Library (E8879A/AN) works directly with Communication Systems Designer Pro or Premier (E8851A/AN and E8852A/AN) and DSP Designer Pro (E8821A/AN) in the Advanced Design System family of Agilent EEsof EDA products.

For other possible product configurations, please contact your local Agilent EEsof EDA field sales representative.

For more information about Agilent EEsof EDA visit:
www.agilent.com/eesof-eda

For more assistance with your test & measurement needs visit:
www.agilent.com/find/assist

Phone or Fax:

United States:
(tel) 1 800 452 4844

Canada:

(tel) 1 877 894 4414
(fax) (905) 206 4120

Europe:

(tel) (31 20) 547 2323
(fax) (31 20) 547 2390

Japan:

(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Latin America:

(tel) (305) 269 7500
(fax) (305) 269 7599

Australia:

(tel) 1 800 629 485
(fax) (61 3) 9272 0749

New Zealand:

(tel) 0 800 738 378
(fax) 64 4 495 8950

Asia Pacific:

(tel) (852) 3197 7777
(fax) (852) 2506 9284

**Product specifications and descriptions
in this document subject to change without notice.
Copyright © 2000 Agilent Technologies
Printed in USA 08/00
5980-0773E**



Agilent Technologies

Innovating the HP Way